Click here to ask about the production status of specific part numbers.

MAX20049

Flexible, Compact Quad Power Supply with 2.2MHz, 500mA Buck Converters and Dual LDOs for Automotive Camera Modules

General Description

The MAX20049 is a dual step-down converter IC with two low-dropout regulators (LDOs), providing a single-chip solution for automotive cameras. The two step-down converters are designed for fixed-frequency PWM operation with input voltages from 5V to 17V for MAX20049, 4V to 17V for MAX20049C, and 3.5V to 17V for MAX20049D. The dedicated high-voltage inputs allow for a flexible solution.

The IC provides voltage monitoring on all four output rails. Once an overvoltage or undervoltage is detected, power good gets pulled low. To accommodate long and inexpensive coax cables, the device has a 500mV SUP1 hysteresis. Both bucks offer very low on-time and allow operation from 17V input to 0.9V output. High-frequency operation allows for an all-ceramic capacitor design and small-size external components. The low-resistance on-chip switches ensure high efficiency while minimizing critical inductances.

Output voltages are factory set and cover various sensor imagers needing 3.3V, 3.0V, 2.9V, 2.8V, or 2.7V. The secondary supplies cover the typical 1.8V, 1.2V, 1.1V, and < 1.0V rails for the serializer and memory. The *Output-Voltage Selection* section covers all the voltage options for flexibility in the camera design.

Protection features include cycle-by-cycle current limit, and thermal shutdown with automatic recovery. The buck converters operate 180° out-of-phase from each other to minimize input current ripple

Applications

- Camera Module—Surround, Rear, Front
- Point of Load

Benefits and Features

- Small Solution Size
  - 16-Pin Side-Wettable (3mm x 3mm) TQFN with an Exposed Pad
  - Low On-Time Architecture Eliminates the Need for Cascading Bucks
  - Wide 3.5V to 17V Input Voltage Range for Power-Over-Coax Cables
  - Fixed Output-Voltage Options
- EMI Solutions
  - Optional Spread-Spectrum Frequency Modulation
  - Pinout Placement Allows for Tight PCB Layout of Switching Nodes
- Self-Protected and Robust
  - Overvoltage and Undervoltage Monitoring, Overvoltage Protection, Thermal Shutdown, and Short- Circuit Protection
  - 500mV Input Hysteresis Allows for Long, Low-Cost Cables During Slow Starts
- Automotive Ready
  - Automotive Temperature Range
  - AEC-Q100 Qualified

***Ordering Information* appears at end of data sheet.**

19-100341; Rev 11; 6/21

maxim integrated™

Simplified Block Diagram

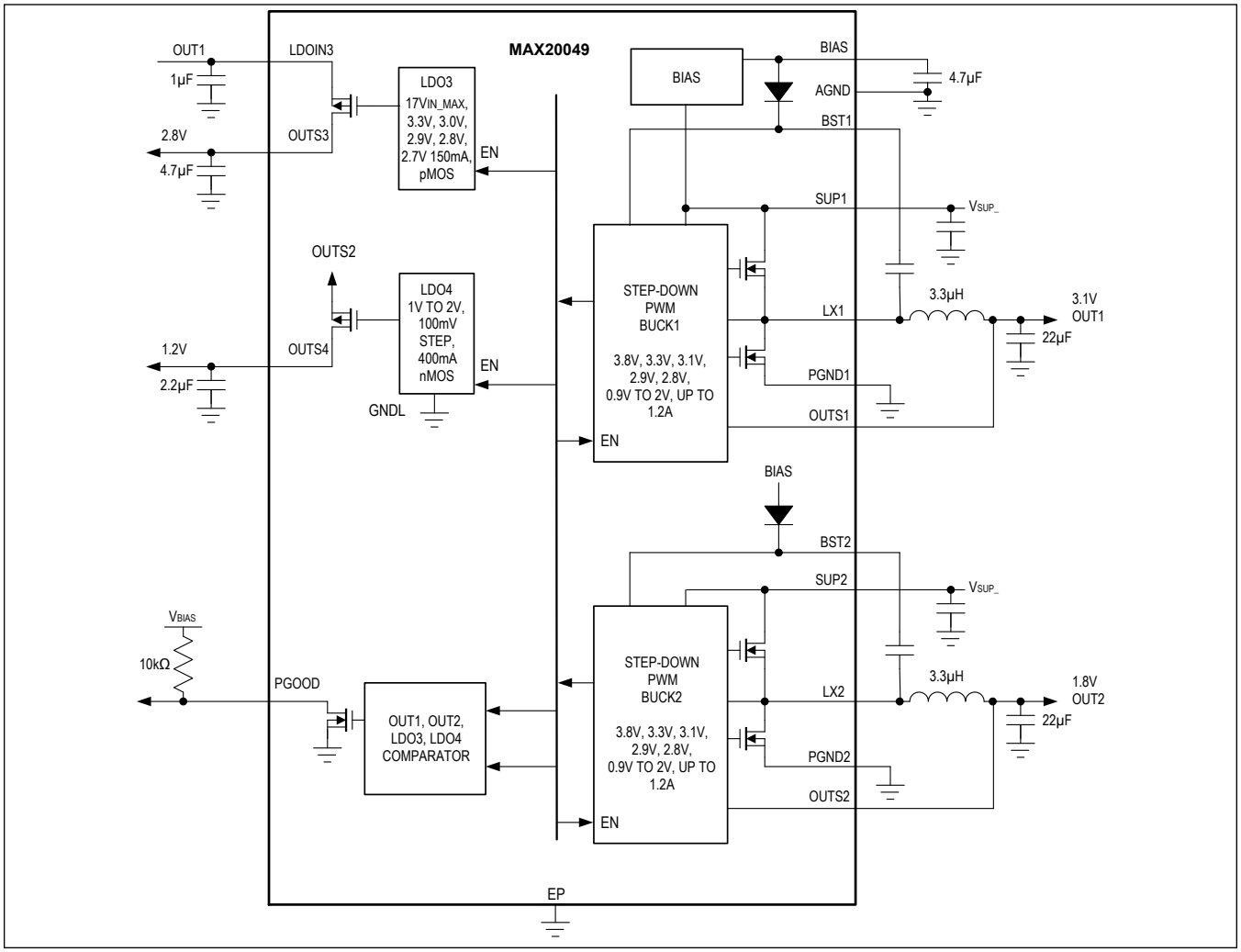


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Absolute Maximum Ratings

SUP1, SUP2, LX1, LX2, LDOIN3 to PGND ..... -0.3V to +18V
OUTS1, OUTS2, OUTS3, OUTS4, PGOOD to AGND.....-0.3V to V_{BIAS} + 0.3V
BST_ to LX_ ..... -0.3V to +6V
AGND, PGND1 to PGND2 ..... -0.3V to +0.3V
BIAS to AGND ..... -0.3V to +6.0V
LX1 Short-Circuit Duration .....
LX2 Short-Circuit Duration .....

Continuous Power Dissipation (T_A = +70°C) Derate 23.09mW/C above +70°C 1847.5mW
Operating Temperature Range ..... -40ºC to +125ºC
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65ºC to +150ºC
Soldering Temperature (reflow) ..... +260ºC
Lead Temperature Range ..... +300ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 SW TQFN

Package Code	T1633Y+5C
Outline Number	21-100150
Land Pattern Number	90-100064

16 SW TQFN

Package Code	T1633Y+6C
Outline Number	21-100330
Land Pattern Number	90-100064
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	43.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	4°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SUP1} = V_{SUP2} = 8V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{SUP1}		5		17	V
		MAX20049C	4		17	
		MAX20049D	3.5		17	
Shutdown Supply Current	$I_{SHUTDOWN}$	V_{SUP1} < 4V, I_{SUP1} + I_{SUP2}		20	30	µA
BIAS Regulator Voltage	V_{BIAS}	V_{SUP1} = 6V to 16V, I_{BIAS} = 0mA to 20mA, C_{BIAS} = 4.7µF		5		V
BIAS Undervoltage Lockout	V_{UVBIAS}	V_{BIAS} falling		2.7	2.9	V

Electrical Characteristics (continued)

(V_{SUP1} = V_{SUP2} = 8V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BIAS Undervoltage-Lockout Hysteresis	$V_{UVBIASHYS}$				400	700	mV
Thermal-Shutdown Threshold		(Note 2)			175		°C
Thermal-Shutdown Threshold Hysteresis		(Note 2)			15		°C
BUCK CONVERTER (BUCK1)							
Output Voltage Range				0.9		3.8	V
Output Voltage	V_{OUT1}	5V < V_{SUP1} < 17V, I_{OUT1} = 0mA to 500mA		-2		+2	%
	V_{OUT2}	5V < V_{SUP1} < 17V, I_{OUT1} = 0mA to 500mA	MAX20049C (Only)	-2		+2.5	
DMOS Peak Current-Limit Threshold	I_{LIM1}			0.8	1	1.2	A
	I_{LIM2}	MAX20049D (factory options)		1.3	1.6	1.9	
High-Side DMOS RDS(ON)	R_{ON_HS1}	I_{LX1} = 300mA, V_{BIAS} = 5V			300	550	mΩ
Low-Side DMOS RDS(ON)	R_{ON_LS1}	I_{LX1} = 300mA, V_{BIAS} = 5V			250	450	mΩ
Soft-Start Ramp Time	t_{SS1}				3		V/ms
LX1 Leakage Current		TA = +25°C				5	µA
Minimum Off-Time	t_{OFF}					80	ns
PWM Switching Frequency	f_{SW}			2	2.2	2.4	MHz
Spread Spectrum		Factory option			±3		%
BUCK CONVERTER (BUCK2)							
Output Voltage Range				0.9		3.8	V
SUP2 Supply Voltage	V_{SUP2}			2.7		17	V
Output Voltage	V_{OUT2}	5V < V_{SUP2} < 17V, I_{OUTS2} = 0 to 500mA		-2		+2	%
	V_{OUT3}		MAX20049C (Only)	-2		+2.5	
DMOS Peak Current-Limit Threshold	I_{LIM2}			0.8	1	1.2	A
	I_{LIM3}	MAX20049D (factory options)		1.3	1.6	1.9	
High-Side DMOS RDS(ON)	R_{ON_HS2}	I_{LX2} = 300mA, V_{BIAS} = 5V			300	550	mΩ
Low-Side DMOS RDS(ON)	RON_LS2	I_{LX2} = 300mA, V_{BIAS} = 5V			250	450	mΩ
Soft-Start Ramp Time	t_{SS2}				3		V/ms
LX2 Leakage Current		T_A = +25°C				5	µA
Minimum Off-Time	t_{OFF}					80	ns
BUCK1, BUCK2 Phasing		(Note 2)			180		Degrees

Electrical Characteristics (continued)

(V_{SUP1} = V_{SUP2} = 8V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUP1 UVLO						
Input Rising Threshold	$V_{SUP1, UVLO}$			5		V
		MAX20049C		4		
		MAX20049D		3.5		
Input Hysteresis		Falling hysteresis		0.5		V
LDO3						
Input Voltage	V_{LDOIN3}		2.9		17	V
Output Voltage Range			2.7		3.3	V
Voltage Accuracy	V_{OUT3}	I_{OUT3} = 1mA to 100mA	-2		+2	%
	V_{OUT4}	I_{OUT3} = 1mA to 150mA (MAX20049D)	-2		+2	
Line Regulation		I_{OUTS3} = 10mA		±0.1		%/V
Output Current Limit			150			mA
PSRR (Note 2)		I_{OUTS3} = 50mA, V_{LDOIN3} = 8V, V_{OUTS3} = 2.8V, 8kHz		88		dB
Startup Response Time (Note 2)	t_{START3}	V_{LDOIN3} = V_{SUP1}, time from when V_{SUP1} crosses UVLO until 98% V_{OUTS3}, I_{OUTS3} = 10mA		121		µs
Dropout		V_{LDOIN3} = 2.8V, V_{OUTS3} = 2.8V, I_{OUTS3} = 100mA			350	mV
LDO4						
Input Voltage	V_{IN4}		1.2		3.8	V
Output Voltage Range		MAX20049	1.0		2.0	V
		MAX20049C/D	1.1		1.825	
Voltage Accuracy	V_{OUT4}	I_{OUTS4} = 0mA to 400mA V_{OUT2} = 1.8V to 3.8V	-2		+2.5	%
Current Limit	I_{LIM4}		400			mA
Line Regulation				±0.3		%
Startup Response Time		Time from when Buck2 tSS begins until 98% VOUTS4, IOUTS4 = 10mA (Note 2)		500		µs
Dropout	V_{DO4}	V_{OUT2} = V_{OUT4} = 0.95V, I_{OUTS4} = 400mA		35	100	mV
PGOOD (ALL OUTPUTS "AND" TOGETHER)						
OUTS1, OUTS2 Undervoltage Threshold		Rising		95		%
		Falling	87	92	96	
OUTS1, OUTS2 Overvoltage Threshold		Rising	102.5	108	115	%
		Falling		106		
OUTS3, OUTS4 Undervoltage Threshold		Rising		95		%
		Falling	89	92	95	
OUTS3, OUTS4 Overvoltage Threshold		Rising	105	108	111	%
		Falling		106		
Debounce Time	t_{DEB}			50		µs

Electrical Characteristics (continued)

(V_{SUP1} = V_{SUP2} = 8V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Leakage Current		T_A = +25°C			1	µA
Low Level		Sinking 1mA			0.4	V

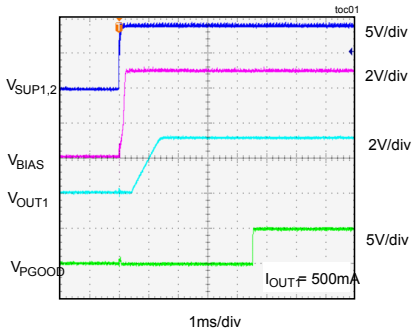
Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at T_A = +25°C.

Note 2: Guaranteed by design; not production tested.

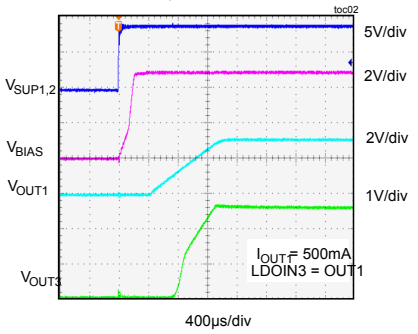
Typical Operating Characteristics

(V_{SUP1} = V_{SUP2} = 9V, V_{LDOIN3} = V_{OUTS1}, V_{OUT1} = 3.1V, V_{OUT2} = 1.8V, V_{OUT3} = 2.8V, V_{OUT4} =1.2V, T_A = +25°C, unless otherwise noted.)

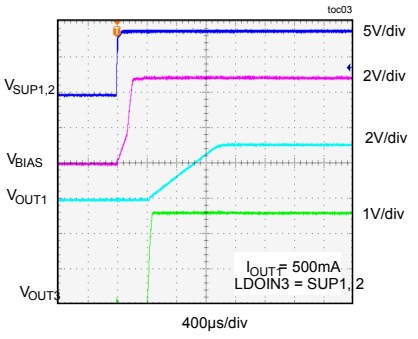
STARTUP PROFILE



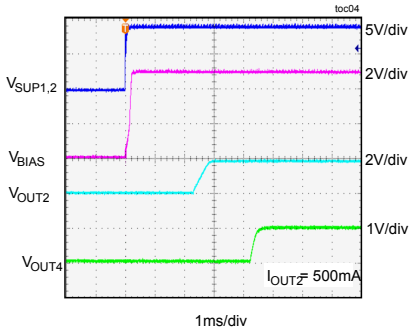
OUT1, 3 STARTUP PROFILE



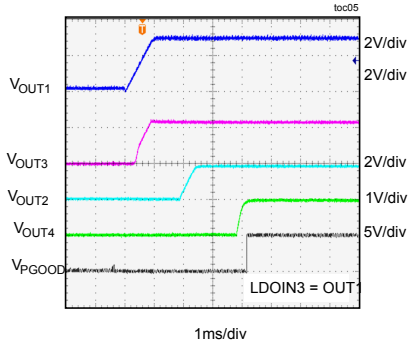
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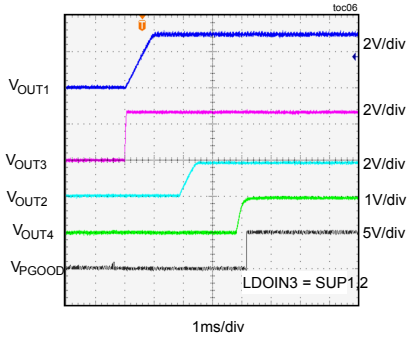
OUT2, 4 STARTUP PROFILE



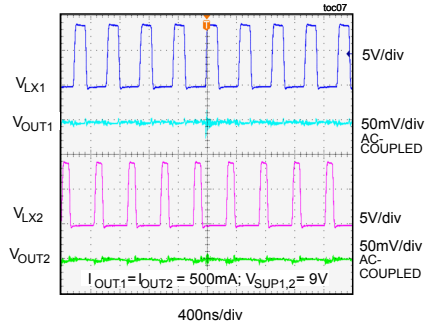
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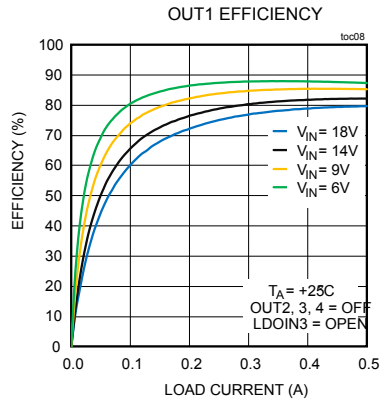
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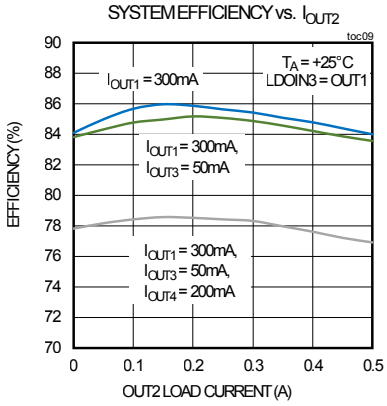
STEPDOWN WAVEFORMS



OUT1 EFFICIENCY



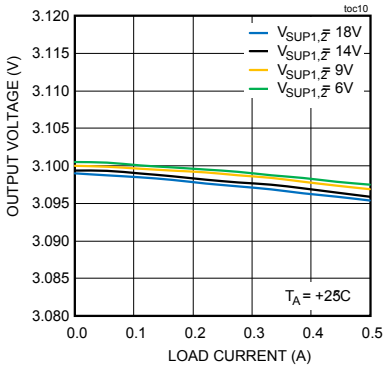
SYSTEM EFFICIENCY vs. I_{OUT2}



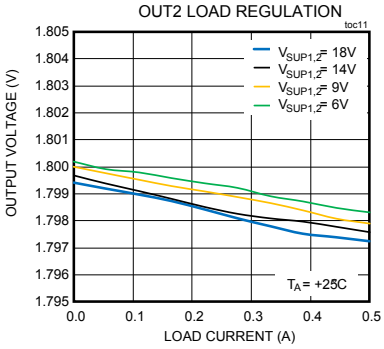
Typical Operating Characteristics (continued)

(V_{SUP1} = V_{SUP2} = 9V, V_{LDOIN3} = V_{OUTS1}, V_{OUT1} = 3.1V, V_{OUT2} = 1.8V, V_{OUT3} = 2.8V, V_{OUT4} =1.2V, T_A = +25°C, unless otherwise noted.)

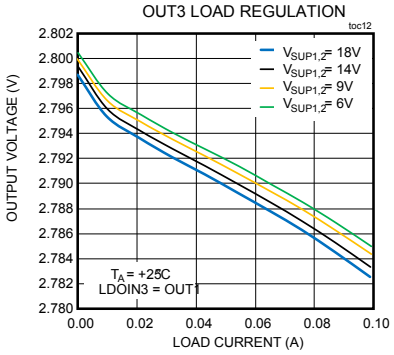
OUT1 LOAD REGULATION



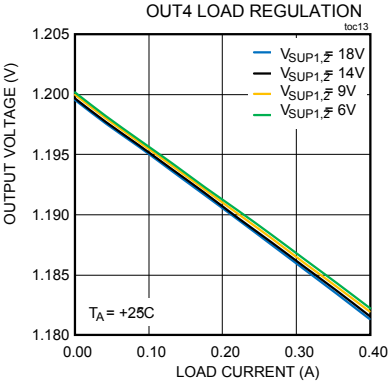
OUT2 LOAD REGULATION



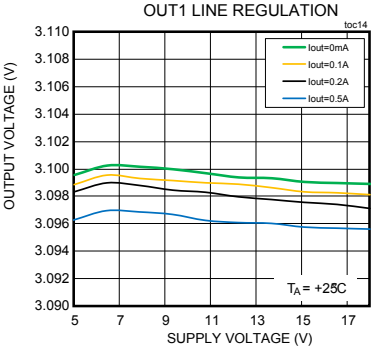
OUT3 LOAD REGULATION



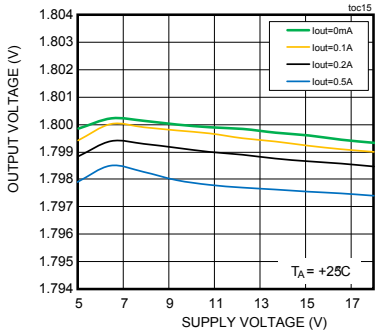
OUT4 LOAD REGULATION



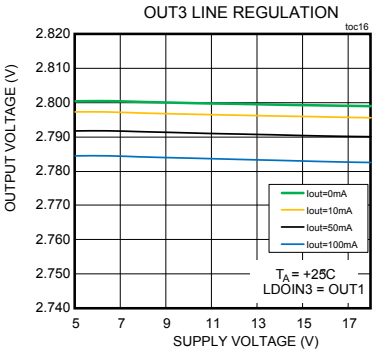
OUT1 LINE REGULATION



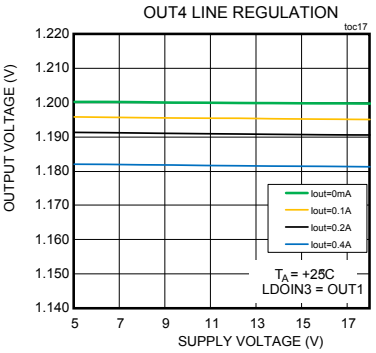
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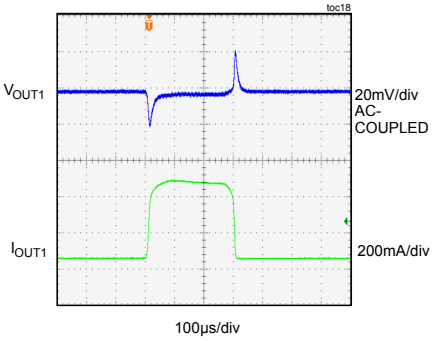
OUT3 LINE REGULATION



OUT4 LINE REGULATION



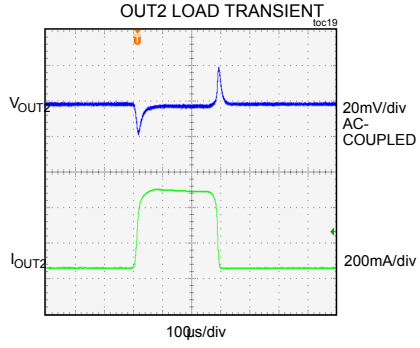
OUT1 LOAD TRANSIENT



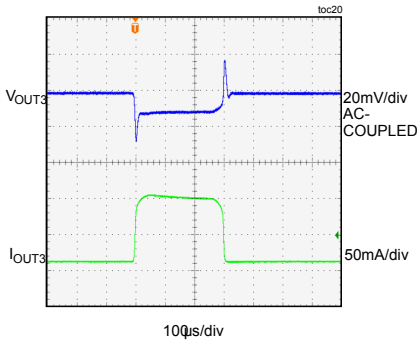
Typical Operating Characteristics (continued)

(V_{SUP1} = V_{SUP2} = 9V, V_{LDOIN3} = V_{OUTS1}, V_{OUT1} = 3.1V, V_{OUT2} = 1.8V, V_{OUT3} = 2.8V, V_{OUT4} =1.2V, T_A = +25°C, unless otherwise noted.)

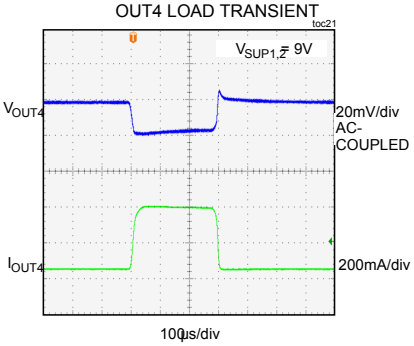
OUT2 LOAD TRANSIENT



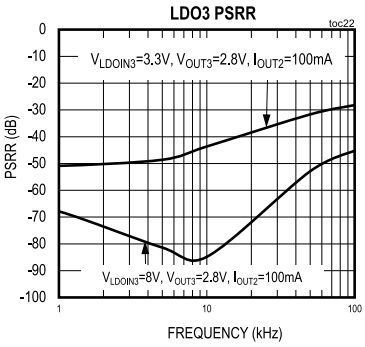
OUT3 LOAD TRANSIENT



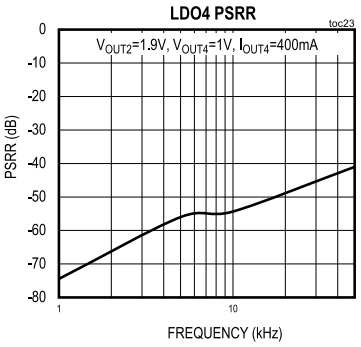
OUT4 LOAD TRANSIENT



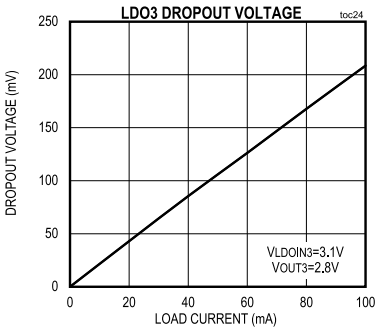
LDO3 PSRR



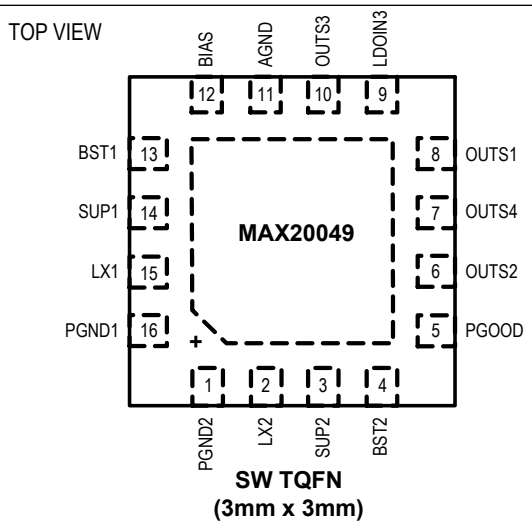
LDO4 PSRR



LDO3 DROPOUT VOLTAGE



Pin Configuration



SW TQFN
(3mm x 3mm)

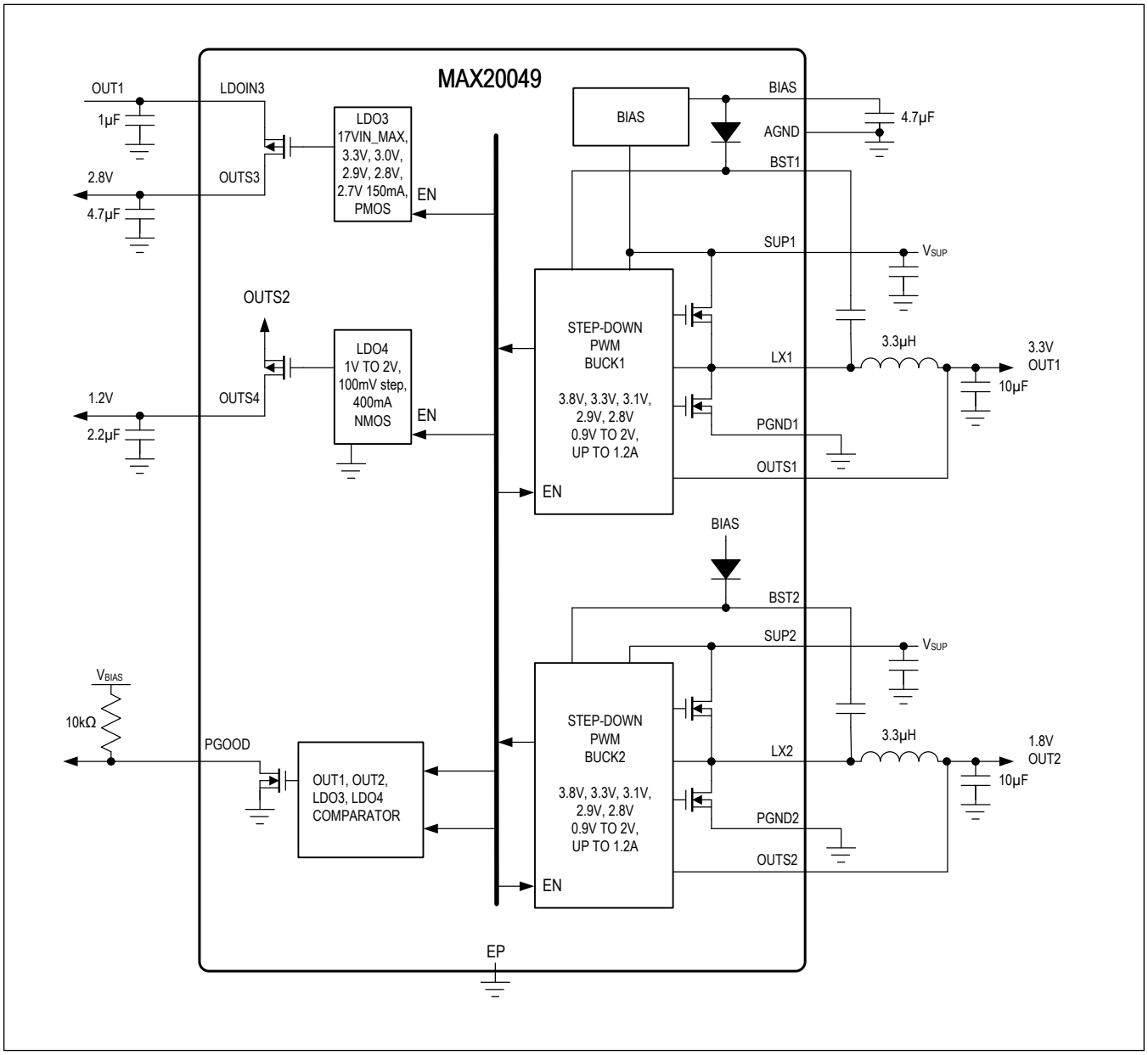
Pin Description

PIN	NAME	FUNCTION
1	PGND2	Power Ground. Connect PGND_ and AGND together.
2	LX2	Inductor Switching Node for Buck Converter 2. High impedance when the IC is off. See the *Inductor Selection* section for more details.
3	SUP2	Buck2 Internal High-Side Switch Supply Input. Connect a 2.2µF ceramic capacitor to ground.
4	BST2	Buck2 Boost-Strap High-Side Driver Supply. Connect a 0.1µF ceramic capacitor between LX2 and BST2 for proper operation.
5	PGOOD	OUT1, OUT2, LDO3, and LDO4 Power-Good Signal. See the *Electrical Characteristics* table for overvoltage/undervoltage thresholds.
6	OUTS2	Sense of Switching Regulator Output 2
7	OUTS4	400mA LDO Output. Connect a 2.2µF ceramic capacitor from OUTS4 to AGND.
8	OUTS1	Sense of Switching Regulator Output 1
9	LDOIN3	Low-Noise LDO Input. Connect a 1µF ceramic capacitor from LDOIN3 to AGND. It is not recommended to connect LDOIN3 directly to SUP1 or SUP2 pins. If LDOIN3 is connected to these pins, then connect a minimum of 22µF capacitor on OUTS3. When LDOIN3 is connected to Buck1 (OUTS1) or Buck2 (OUTS2) output, ensure that the IC is disabled until LDOIN3 voltage drops to less than 2.5V before the next power-up.
10	OUTS3	Low-Noise LDO Output. Connect a 4.7µF ceramic capacitor from OUTS3 to AGND.
11	AGND	Analog Ground. Connect PGND_ and AGND together.
12	BIAS	Linear Regulator Output. BIAS powers up the internal circuitry. Bypass with a 4.7µF ceramic capacitor to ground.
13	BST1	Buck1 Boost-Strap High-Side Driver Supply. Connect a 0.1µF ceramic capacitor between LX1 and BST1 for proper operation.
14	SUP1	Voltage-Supply Input and Internal High-Side-Switch Supply Input. Connect a 2.2µF ceramic capacitor to ground.
15	LX1	Inductor Switching Node for Buck Converter 1. High Impedance when the IC is off. See the *Inductor Selection* section for more details.
16	PGND1	Power Ground. Connect PGND_ and AGND together.

Pin Description (continued)

PIN	NAME	FUNCTION
-	EP	Exposed Pad. EP must be connected to ground plane on PCB, but is not a current-carrying path and is only needed for thermal transfer.

Block Diagram



Detailed Description

The MAX20049 is a dual step-down converter IC with two LDOs providing a single-chip solution for automotive cameras. The two step-down converters are designed for fixed-frequency PWM operation with 4V to 17V input voltages. The dedicated high-voltage input on the LDO allows for cascading from Buck1, or direct from a power-over-coax cable. The higher input voltage on the LDO improves power-supply rejection ratio (PSRR). Both bucks offer very low on-time and allow operation from maximum input voltage to 0.9V output. This eliminates the need for a preregulator or cascading of power supplies for the 1.8V and 1.2V rails. The single conversion increases total efficiency while minimizing PCB area. Output voltage is factory preset, eliminating external resistors and shrinking the PCB area. The IC provides voltage monitoring on all four rails. When an overvoltage (OV) and undervoltage (UV) is detected, power good goes high impedance. To accommodate long and inexpensive coax cables, the IC has a 500mV hysteresis. Protection features include cycle-by-cycle current limit, and thermal shutdown with automatic recovery. The buck converters operate 180° out-of-phase from each other to minimize input-current ripple.

BIAS/UVLO

The IC includes a 5V linear regulator (V_{BIAS}) that provides power to the internal circuit blocks. It is powered from SUP1. Connect a 4.7µF ceramic capacitor from BIAS to ground. Internal logic powers up after V_{BIAS} has exceeded the internal undervoltage-lockout level. V_{UVLO} = 3.1V (typ) rising.

System Enable

The IC uses an internal threshold on SUP1 to activate soft-start and sequencing on the buck converters and LDOs. The input rising threshold is 5V (typ), 4V (typ) for MAX20049C. A 500mV (typ) hysteresis is used to ensure input-voltage drops on the cable at slow startup do not result in the device toggling on and off.

Soft-Start and Sequencing

The IC features an internal soft-start timer. The Buck1 converter starts first, with a ramp rate of 3V/ms. LDO3 starts at the same time as Buck1 with a 100µs soft-start time. Buck2 soft-starts with a ramp rate of 3.3V/ms after V_{OUTS1} has reached regulation. LDO4 begins soft-start once OUTS2 has reached regulation. OUT4 soft-start time is 120µs (see Figure 1 for sequencing). Buck1 and Buck2 offer the same voltage options; therefore, since the Buck1 and Buck2 sequence is set, order the voltage needed per the sequence order.

Note: SUP1 must always be connected to the input voltage since it powers the internal LDO.

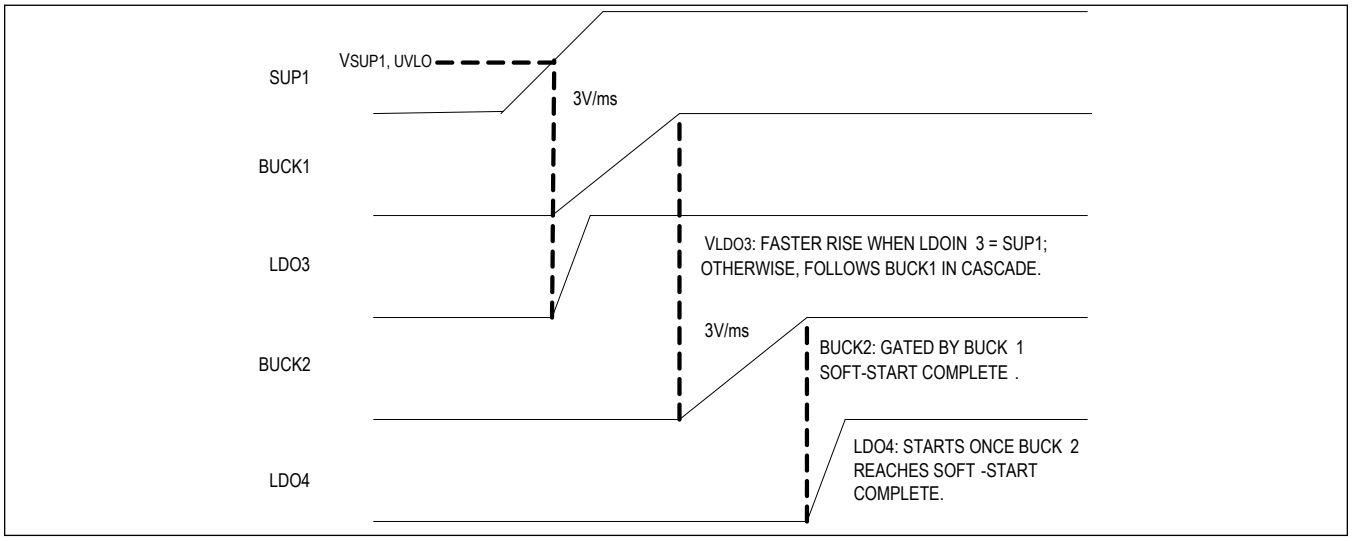


Figure 1. Default Sequencing

By default, LDO3 starts when the VSUP1 reaches a rising UVLO ($V_{SUP1,UVLO}$). LDO3 can be initialized by the other output voltages: OUT1, OUT2, and OUT4.

The output voltages must be within regulation before an LDO3 enable is triggered. The fixed-power sequencing options are set by a factory program.

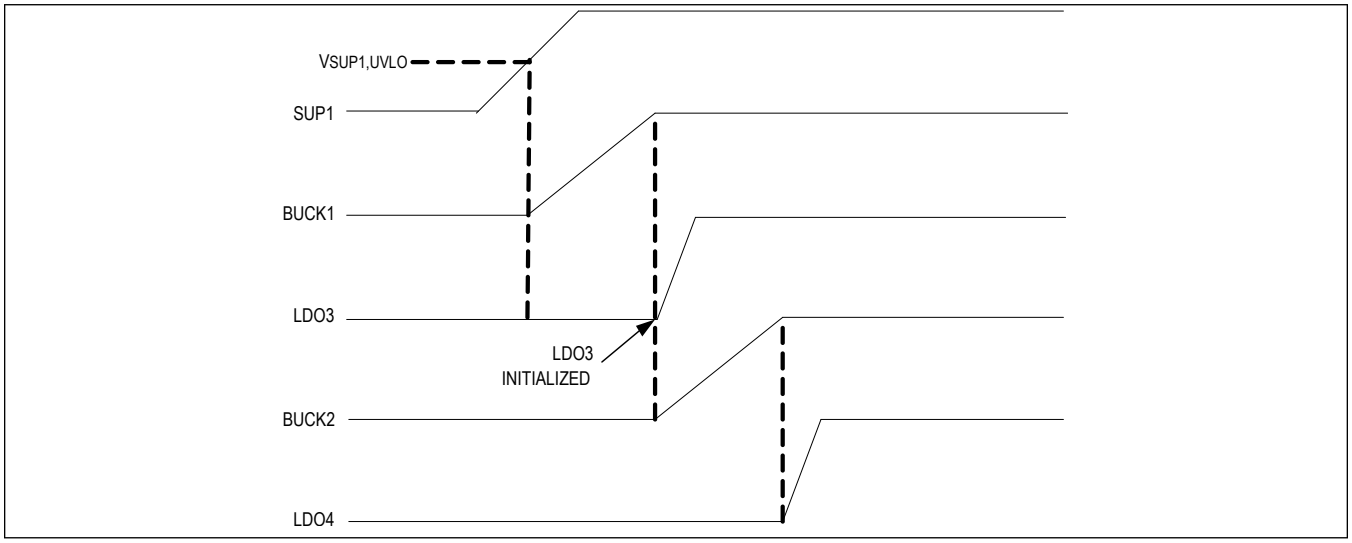


Figure 2. LDO3 Sequenced from Buck1

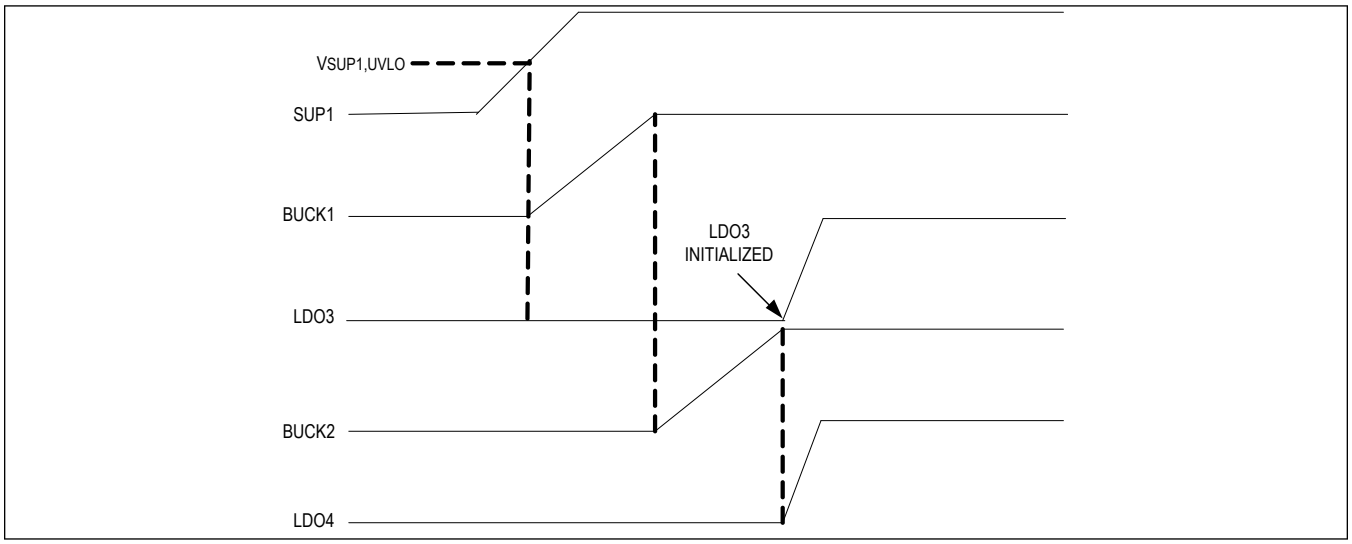


Figure 3. LDO3 Sequenced from Buck2

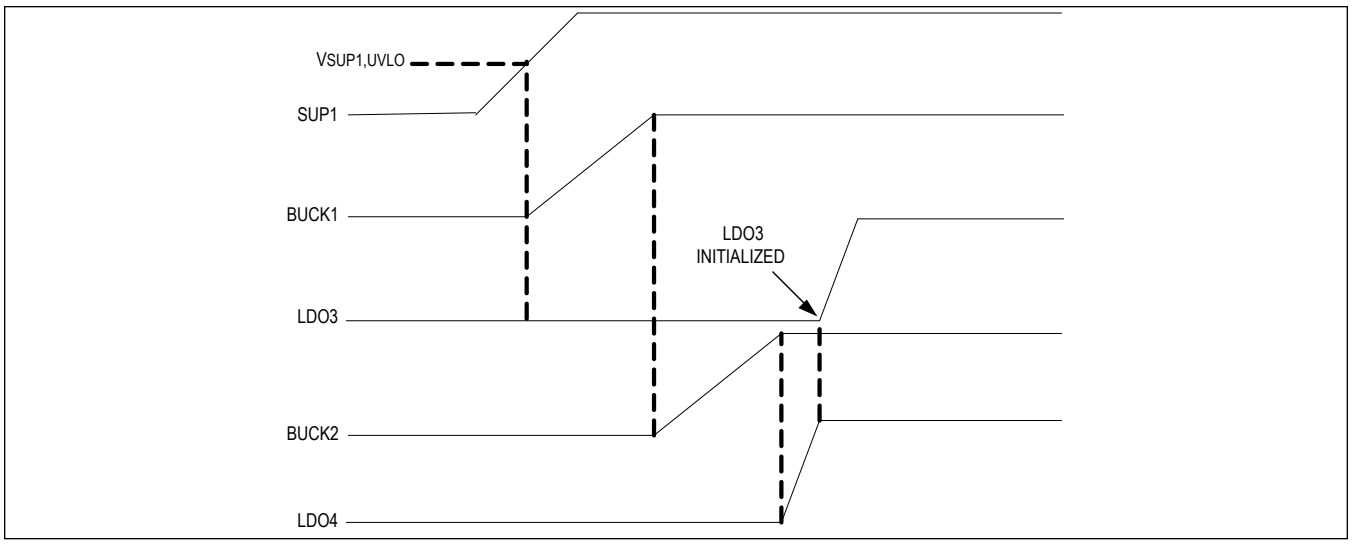


Figure 4. LDO3 Sequenced from LDO4

Current Limit/Short-Circuit Protection

The IC has fault protection designed to protect against abnormal conditions. If either buck output is shorted, the respective converter implements a cycle-by-cycle current limit. If LDOs are cascaded, the respective LDO output tracks the buck output.

Power Good (PGOOD)

The IC features an open-drain power-good output (PGOOD). PGOOD is an output that pulls low when any output voltage falls below the undervoltage falling threshold. PGOOD is high impedance when the output voltage rises above the undervoltage rising threshold. PGOOD pulls low when the output voltage rises above the overvoltage rising threshold and returns high impedance when the output voltage falls below the overvoltage falling threshold. Connect a 10kΩ (typ) pullup resistor to an external supply or the on-chip BIAS output. During startup, all output voltages must be in regulation before PGOOD goes high impedance.

Spread-Spectrum Option

The IC has a factory-programmable spread spectrum that varies the internal operating frequency by ±3%, relative to the internally generated operating frequency of 2.2MHz (typ). Spread spectrum is offered to improve EMI performance of the devices.

Thermal-Overload Protection

The IC features thermal-overload protection. The device turns off when the junction temperature exceeds +175°C (typ). Once the device cools by 15°C (typ), it turns back on with a soft-start sequence.

Applications Information

Output-Voltage Selection

Output voltages are set at the factory (see Table 1 for available voltages). LDO3 is available as 2.7V, 2.8V, 2.9V, 3V, and 3.3V. LDO4 is available from 1V to 2V in 100mV steps. LDO3 targets most image-sensor voltages and can be powered from a power-over-coax cable, or the Buck1 or Buck2 converter. LDO4 is powered from Buck2; contact factory for other options. See the *Typical Application Circuits* for examples.

Table 1. Ouput Voltage Options

MAX20049	OUTPUT VOLTAGE RANGE (100mV STEPS)	FIXED OUTPUT VOLTAGES
Buck1	1V to 2V	2.8V, 2.9V, 3.1V, 3.3V, 3.8V
Buck2	1V to 2V	2.8V, 2.9V, 3.0V, 3.3V, 3.8V
LDO3		2.8V, 2.9V, 3V, 3.3V
LDO4	1V to 2V	

MAX20049C	OUTPUT VOLTAGE RANGE (100mV STEPS)	FIXED OUTPUT VOLTAGES
Buck1	0.9V to 1.9V	2.8V, 2.9V, 3.1V, 3.3V, 3.8V
Buck2	0.9V to 1.9V	2.8V, 2.9V, 3.0V, 3.3V, 3.8V
LDO3		2.7V, 2.8V, 2.9V, 3.3V
LDO4	1.1V to 1.825V	

MAX20049D	OUTPUT VOLTAGE RANGE (100mV STEPS)	FIXED OUTPUT VOLTAGES
Buck1	0.9V to 3.3V	2.8V, 2.9V, 3.1V, 3.3V, 3.8V
Buck2	0.9V to 3.3V	2.8V, 2.9V, 3.0V, 3.3V, 3.8V
LDO3		2.7V, 2.8V, 2.9V, 3.3V
LDO4	1.1V to 1.825V	

Inductor Selection

The design is optimized with 3.3µH or 2.2µH inductors for power over coax input voltages and common camera output voltages. Camera systems are space constrained and require tradeoff in saturation current, case size, and inductor ripple current.

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The minimum capacitance on SUP1 and SUP2 should each be 2.2µF ceramic with an X7R rating.

Buck1 and Buck2 Output Capacitor

The minimum output capacitance should be 10µF ceramic with an X7R rating when the output voltage is set to a voltage of 1.8V or higher. A 22µF ceramic capacitor with an X7R rating should be used with output voltages lower than 1.8V. The allowable output-voltage ripple and the maximum deviation of the output voltage during step-load currents determines the output capacitance and its ESR.

LDO3 and LDO4 Output Capacitor

LDO3 minimum output capacitance is 4.7µF ceramic with an X7R rating. LDO4 minimum output capacitance is 2.2µF ceramic with an X7R rating.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching power losses and clean, stable operation. Use a multilayer board

wherever possible for better noise immunity. Follow the guidelines below for a good PCB layout:

1. Place the input capacitor immediately next to the SUP_ pin. Since the IC operates at 2.2MHz switching frequency, this placement is critical for effective decoupling of high-frequency noise from the SUP_ pins.
2. Solder the exposed pad to a large copper-plane area under the device. To effectively use this copper area as heat exchanger between the PCB and ambient, expose the copper area on the top and bottom side. Add a few small vias, or one large via, on the copper pad for efficient heat transfer. Connect the exposed pad to the ground plane, ideally at the return terminal of the output capacitor.
3. Isolate the power components and high-current paths from sensitive analog circuitry.
4. Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
5. Connect PGND_ and AGND together, preferably at the return terminal of the output capacitor. Do not connect them anywhere else.
6. Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCB to enhance full-load efficiency and power-dissipation capability.
7. Route high-speed switching nodes away from sensitive analog areas. Use internal PCB layers as PGND_ to act as EMI shields, keeping radiated noise away from the device and analog bypass capacitor.

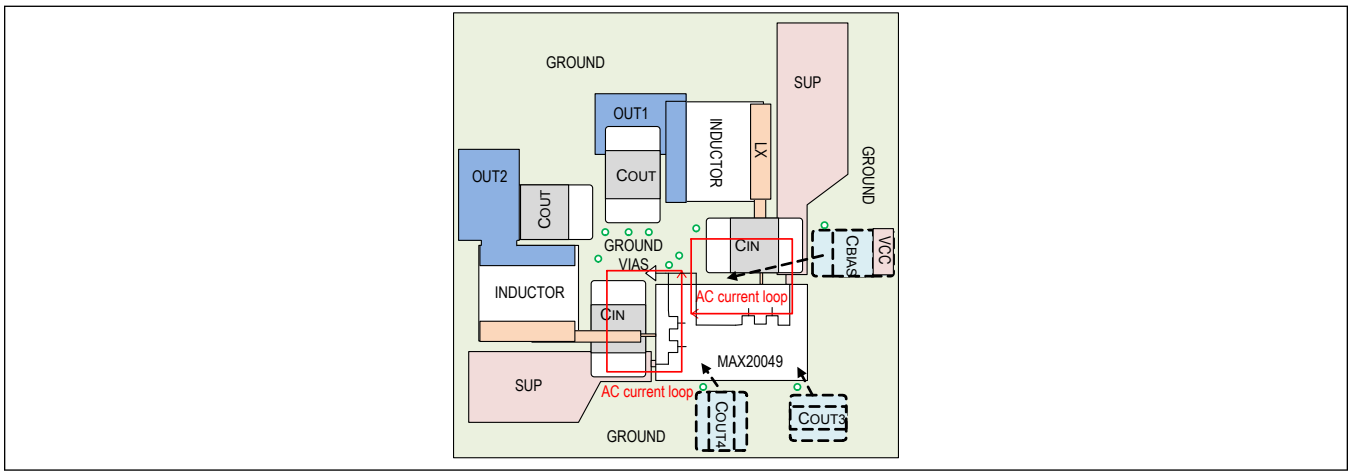


Figure 5. MAX20049 PCB Layout

Typical Application Circuits

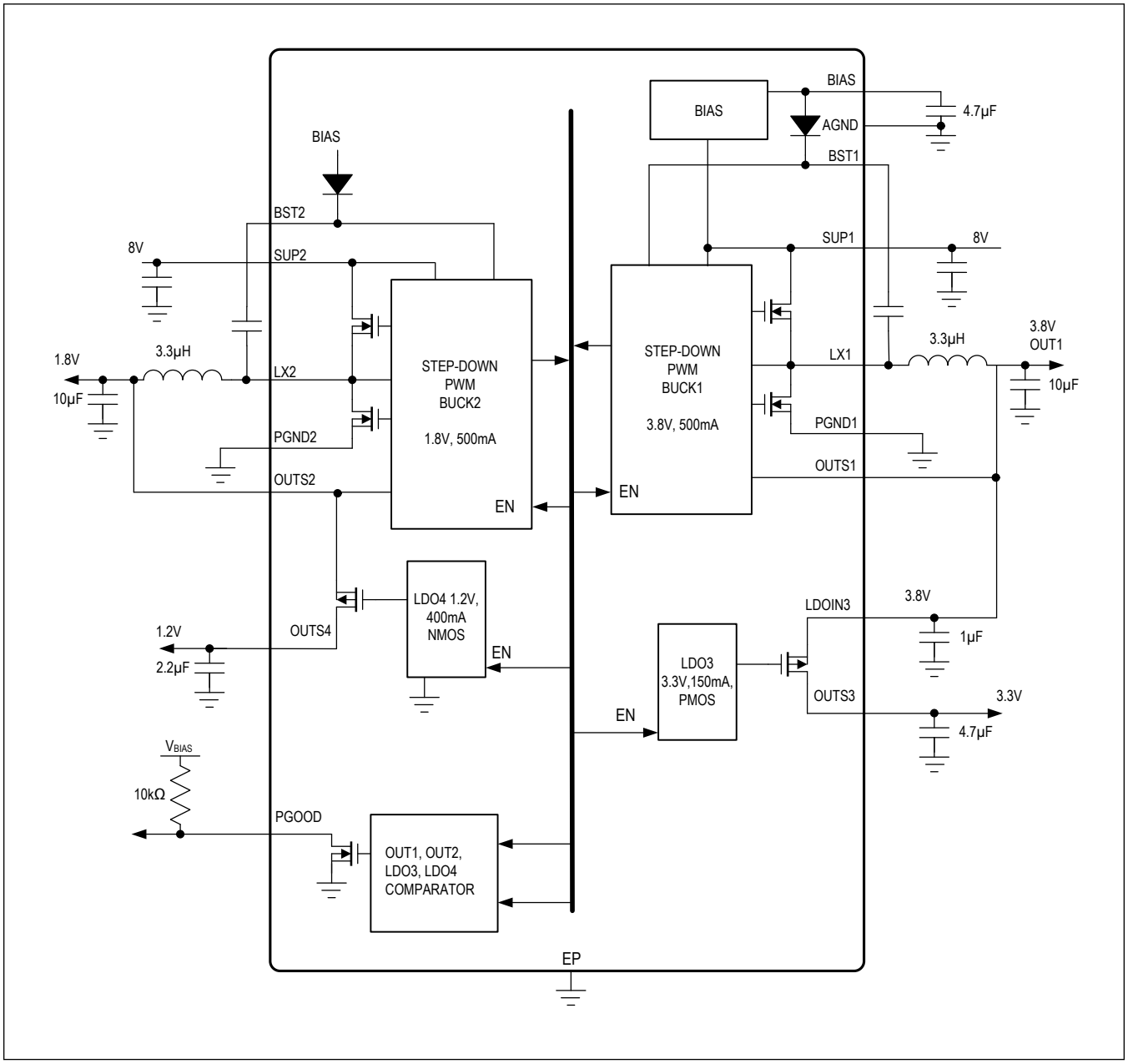


Figure 6. Cascade Buck and LDO for Low-Noise Supply

Typical Application Circuits (continued)

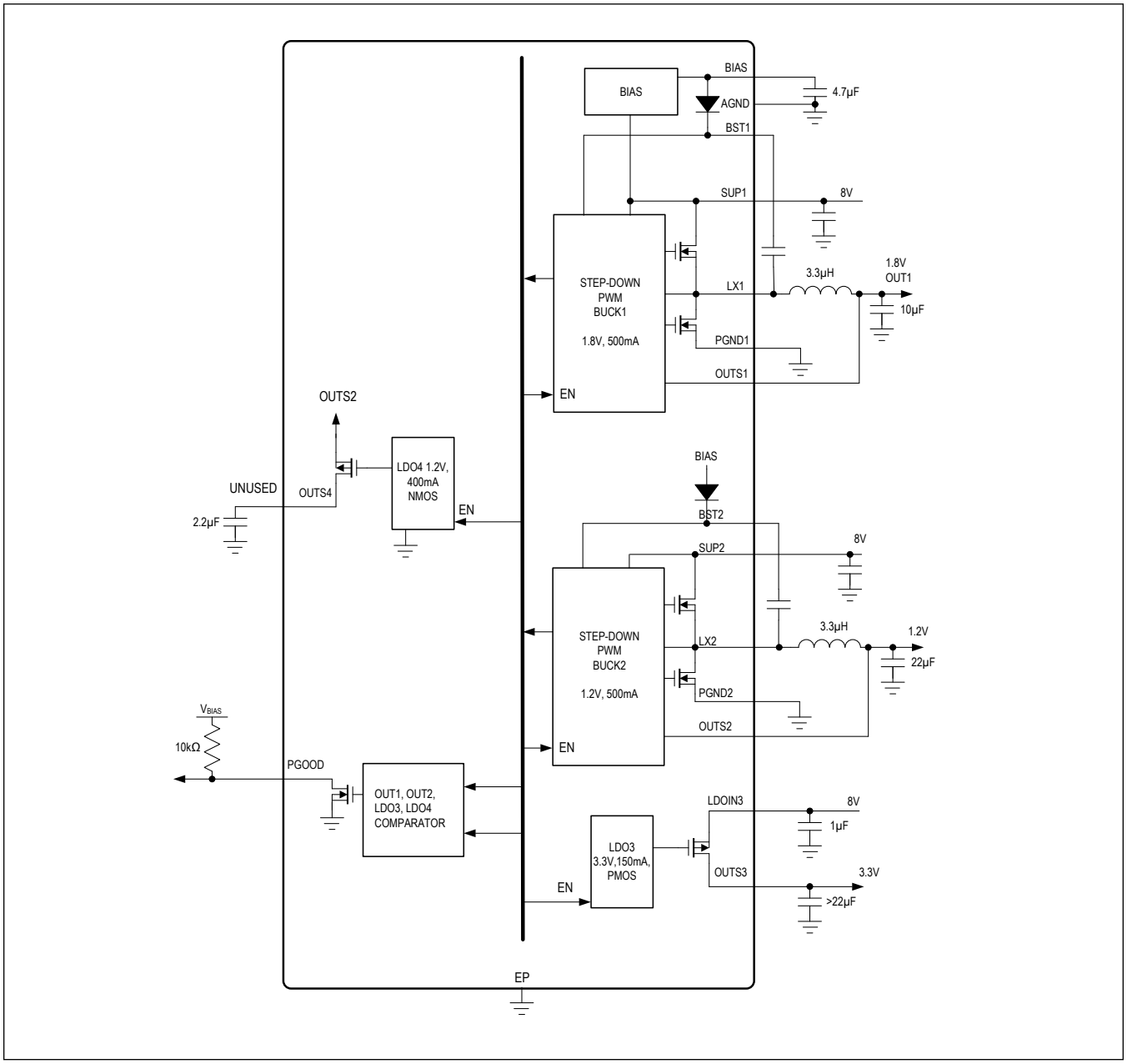


Figure 7. Power-over-Coax Cable Direct to LDO

Ordering Information

PART	BUCK1, LDO3 (V)	BUCK2, LDO4 (V)	SPREAD SPECTRUM	ILIM1, ILIM2 (MIN) (A)	PACKAGE CODE*
MAX20049ATEA/VY+	3.8, 3.3	1.8, 1.2	Off	0.8, 0.8	T1633Y+5C
MAX20049ATEB/VY+	3.3, 2.8	1.85, 1.2	On	0.8, 0.8	T1633Y+5C
MAX20049ATEC/VY+**	3.8, 3.0	1.8, 1.2	Off	0.8, 0.8	T1633Y+5C
MAX20049ATED/VY+	3.3, 2.8	1.8, 1.2	Off	0.8, 0.8	T1633Y+5C
MAX20049ATEE/VY+	3.1, 2.8	1.8, 1.2	Off	0.8, 0.8	T1633Y+5C
MAX20049ATEF/VY+	2.8, 2.8	3.3, 1.8	On	0.8, 0.8	T1633Y+5C
MAX20049ATEG/VY+	1.1, 2.9	1.8, 1.2	On	0.8, 0.8	T1633Y+5C
MAX20049ATEH/VY+	3.3, 2.8	1.8, 1.2	On	0.8, 0.8	T1633Y+5C
MAX20049ATEK/VY+	3.3, 2.9	1.8, 1.1	On	0.8, 0.8	T1633Y+5C
MAX20049CATEA/VY+	3.3, 2.8	1.85, 1.225	On	0.8, 0.8	T1633Y+6C
MAX20049DATEA/VY+	1.8, 3.3	1.8, 1.2	On	0.8, 0.8	T1633Y+6C
MAX20049DATEB/VY+	2.8, 2.8	1.8, 1.2	On	0.8, 0.8	T1633Y+6C
MAX20049DATEE/VY+	1.2, 2.8	3.3, 1.8	On	1.3, 1.3	T1633Y+6C
MAX20049DATEF/VY+	1.2, 2.9	3.3, 1.8	On	1.3, 1.3	T1633Y+6C
MAX20049DATEG/VY+	1.225, 2.9	3.3, 1.8	On	0.8, 0.8	T1633Y+6C
MAX20049DATEJ/VY+	3.3, 2.8	1.8, 1.2	On	1.3, 1.3	T1633Y+6C
MAX20049DATEK/VY+	3.8, 3.3	1.8, 1.2	On	1.3, 1.3	T1633Y+6C
MAX20049DATEL/VY+	3.3, 2.8	1.8, 1.1	On	1.3, 1.3	T1633Y+6C
MAX20049DATEN/VY+	3.8, 3.3	1.8, 1.1	On	0.8, 0.8	T1633Y+6C

/V Denotes an automotive-qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package. Temperature Range is -40°C to +125°C

**Pin-Package = 16 Side-Wettable TQFN Exposed Pad.*

***Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/18	Initial release	—
1	8/18	Updated the General Description, Output-Voltage Selection, and Inductor Selection sections; updated the Package Information, Electrical Characteristics, and Ordering Information tables; replaced Table 1 and TOC09; added MA20049ATEF/VY+, MAX20049ATEG/VY+, MAX20049ATEH/VY+, MAX20049BATEB/VY+, and MAX20049CATEA/VY+ to the Ordering Information table.	1–5, 10, 14
2	8/18	Updated the General Description, Benefits and Features sections; updated the Electrical Characteristics table, Table 1, and added future product designation to MA20049ATEF/VY+, MAX20049ATEG/VY+, MAX20049ATEH/VY+, MAX20049BATEB/VY+, and MAX20049CATEA/VY+ in the Ordering Information table; updated the Block Diagram and the Typical Application Circuits (Figures 6 and 7).	1, 4, 9, 11, 13–15
3	11/18	Added TOC19 and removed future product designation from MAX20049ATEA/VY+ and MAX20049ATEB/VY+	8, 16
4	12/18	Updated the Electrical Characteristics table, TOC08–TOC13, Detailed Description, BIAS/UVLO, System Enable, Output Voltage Selection, and the Ordering Information table; replaced Figure 5; added new TOC19–TOC21 and TOC23–24, and renumbered existing TOC19 to be TOC22	3–8, 1–13, 16
5	2/19	Updated the Power Good (PGOOD) section; removed future product designation from MAX20049ATEF/VY+, MAX20049ATEH/VY+, and MAX20049CATEA/VY+; added MAX20049ATEK/VY+, MAX20049DATEA/VY+, and MAX20049DATEB/VY+ as future products; removed MAX20049BATEB/VY+ from the Ordering Information	12, 16
6	5/19	Updated Package Information, Electrical Characteristics, and Applications Information sections; added Figures 2, 3, and 4; updated Table 1; added MAX20049DATEE/VY+** and MAX20049DATEE/VY+** to Ordering Information	2, 4, 11, 12, 13, 14, 18
7	8/19	Updated General Description, Benefits and Features, Absolute Maximum Ratings, Electrical Characteristics, Detailed Description, Applications Information, and Ordering Information	1–5, 12–14, 18
8	3/20	Updated Ordering Information to add future-product notation	18
9	6/20	Updated Electrical Characteristics, Pin Descriptions, Applications Information, Typical Application Circuits, and Ordering Information	5, 9, 14, 18
10	3/21	Updated Electrical Characteristics and Ordering Information	6, 22
11	6/21	Updated Absolute Maximum Ratings, TOC22, TOC23, TOC24, and Ordering Information	6, 12, 23

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