Click here to ask about the production status of specific part numbers.

MAX20004E/MAX20006E/ MAX20008E

Automotive, 36V, 4A/6A/8A Integrated Step-Down Converters with Integrated Compensation

General Description

The MAX20004E/MAX20006E/MAX20008E are small, synchronous buck converters with integrated high-side and low-side MOSFETs. The device family can deliver up to 8A with input voltages from 3.5V to 36V, while using only 15µA quiescent current at no load (except for MAX20006EAFOD/VY+ which has FPWM mode only). Voltage quality can be monitored by observing the $\overline{\text{RESET}}$ signal. The devices can operate in dropout by running at 98% duty cycle, making them ideal for automotive applications.

The devices offer fixed output voltages of 5V, 3.9V, or 3.3V. Compensation is internal to the device, providing excellent transient response. Frequency can be 400kHz or 2.1MHz. The devices offer a forced fixed-frequency mode and skip mode with ultra-low quiescent current of 15µA. The device has a pin-selectable (SSEN) spread-spectrum enable to further assist systems designers with better EMC management.

The MAX20004E/MAX20006E/MAX20008E are available in a small 3.5mm x 3.75mm 17-pin FC2QFN package and use very few external components.

Applications

- Point-of-Load Applications in Automotive
- Distributed DC Power Systems
- Navigation and Radio Head Units

Benefits and Features

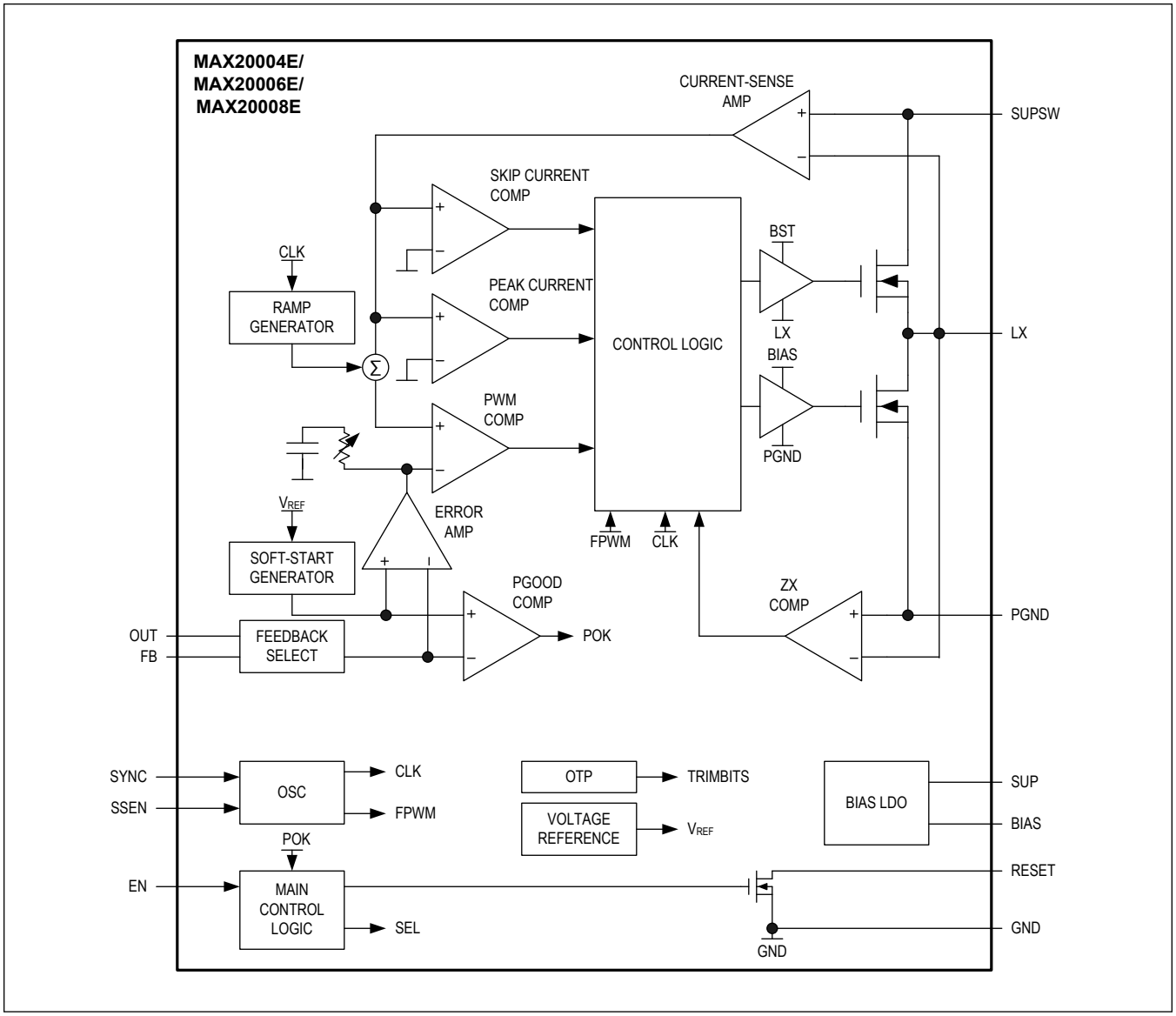
- Multiple Functions for Small Size
  - Operating V_{IN} Range of 3V to 36V
  - 15µA Quiescent Current in Skip Mode
  - Synchronous DC-DC Converter with Integrated FETs
  - 400kHz or 2.1MHz Switching Frequency
  - Fixed 5ms(default) Internal Soft-Start
  - 3.3V/3.9V/5.0V Fixed Output Options
  - 98% Duty-Cycle Operation with Low Dropout
  - $\overline{\text{RESET}}$ Output
- High Precision
  - ±2% Output-Voltage Accuracy
  - Good Load-Transient Performance
- Robust for the Automotive Environment
  - Current-Mode, Forced-PWM, and Skip Operation
  - Overtemperature and Short-Circuit Protection
  - 3.5mm x 3.75mm 17-Pin FC2QFN
  - Symmetrical Pinout with Pin-Selectable Spread Spectrum for Optimized EMI Performance
  - -40°C to +150°C Junction Operating Range
  - 40V Load-Dump Tolerant
  - AEC-Q100 Qualified

***Ordering Information* appears at end of datasheet.**

19-100562; Rev 6; 7/20

maxim integrated™

Simplified Block Diagram



Absolute Maximum Ratings

EN, SUPSW, SUP to PGND ..... -0.3V to +40V
LX to PGND (Note 1) ..... -0.3V to SUPSW+0.3V
SYNC, BIAS to GND ..... -0.3V to +6V
RESET to GND ..... -0.3V to +6V
GND to PGND ..... -0.3V to +0.3V
SSEN, FB, OUT to GND ..... -0.3V to BIAS+0.3V
BST to LX ..... -0.3V to +6V
LX Continuous RMS Current 8A

Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
17-FCQFN (derate 29.4mW/°C > 70°C) 2553mW
Operating Temperature ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature Range ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Note 1: Self-protected from transient voltages exceeding these limits in circuit under normal operation.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Ambient Temperature Range			-40 to 125	ºC

Note: These limits are not guaranteed.

Package Information

FC2QFN

Package Code	F173A3FY+7
Outline Number	21-100383
Land Pattern Number	90-100124
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	38.8°C/W
Junction to Case (θ_{JC})	8°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SUP} = V_{SUPSW} = V_{EN} = 14V, T_J = -40°C to +150°C unless otherwise noted, (Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}, V_{SUPSW}		3.5		36	V
		After startup	3			
		t < 1s			40	
Supply Current	I_{SUP}	V_{OUT} = 3.3V, SKIP mode, no load		13	33	µA
		V_{OUT} = 3.9V (MAX20006EAFOE/VY+ only), SKIP mode, no load (Note 3)		15	35	
		V_{OUT} = 5.0V, SKIP mode, no load		20	42	

Electrical Characteristics (continued)

(V_{SUP} = V_{SUPSW} = V_{EN} = 14V, T_J = -40°C to +150°C unless otherwise noted, (Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Supply Current	I_{SHDN}	EN = 0V		5	10	µA
BIAS Regulator Voltage	V_{BIAS}	V_{SUP} = V_{SUPSW} = 6V to 36V, I_{BIAS} < 10mA, BIAS not switched over to V_{OUT}	4.7	5	5.4	V
BIAS Undervoltage Lockout	V_{UVBIAS}	V_{BIAS} rising	2.7	3	3.3	V
		V_{BIAS} falling		2.5	2.95	
Thermal Shutdown Temperature		T_J rising		175		°C
Thermal Shutdown Hysteresis				15		°C
OUTPUT VOLTAGE						
PWM-Mode Output Voltage	$V_{OUT_3.3V}$	6V < V_{SUP} < 36V, no load, PWM	3.23	3.3	3.37	V
SKIP-Mode Output Voltage	$V_{SKIP_3.3V}$	6V < V_{SUP} < 36V, no load, FB = BIAS	3.23	3.3	3.4	V
PWM-Mode Output Voltage	$V_{OUT_3.9V}$	6V < V_{SUP} < 36V, no load, PWM	3.82	3.9	3.98	V
SKIP-Mode Output Voltage	$V_{SKIP_3.9V}$	6V < V_{SUP} < 36V, no load, FB = BIAS, (MAX20006EAFOE/VY+ only, Note 3)	3.82	3.9	4.02	V
PWM-Mode Output Voltage	V_{OUT_5V}	6V < V_{SUP} < 36V, no load, PWM	4.9	5	5.1	V
SKIP-Mode Output Voltage	V_{SKIP_5V}	6V < V_{SUP} < 36V, no load, FB = BIAS	4.9	5	5.15	V
Load Regulation		V_{FB} = V_{BIAS}, 30mA < I_{LOAD} < I_{MAX}		0.2		%
Line Regulation		V_{FB} = V_{BIAS}, 6V < V_{SUPSW} < 36V		0.02		%/V
BST Input Current	I_{BST_ON}	High-side MOSFET on, V_{BST} – V_{LX} = 5V		1.5		mA
	I_{BST_OFF}	High-side MOSFET off, V_{BST} – V_{LX} = 5V		1.5		µA
LX Current Limit	I_{LX}	MAX20004E (4A)	5.25	7	8.75	A
		MAX20006E (6A)	7.5	10	12.5	
		MAX20008E (8A)	10.5	14	17.5	
LX Rise Time				2		ns
Spread Spectrum		Spread spectrum enabled		±3		%
High-Side Switch On-Resistance		V_{BIAS} = 5V, I_{LX} = 1A		38	76	mΩ
High-Side Switch Leakage		High-side MOSFET off, V_{SUPSW} = 36V, V_{LX} = 0V, T_A = +25°C		1	5	µA
Low-Side Switch On-Resistance		V_{BIAS} = 5V, I_{LX} = 1A		18	36	mΩ
Low-Side Switch Leakage		Low-side MOSFET off, V_{SUPSW} = 36V, V_{LX} = 36V, T_A = +25°C		1	5	µA
FB Input Current	I_{FB}	T_A = +25°C		20	100	nA

Electrical Characteristics (continued)

(V_{SUP} = V_{SUPSW} = V_{EN} = 14V, T_J = -40°C to +150°C unless otherwise noted, (Note 2))

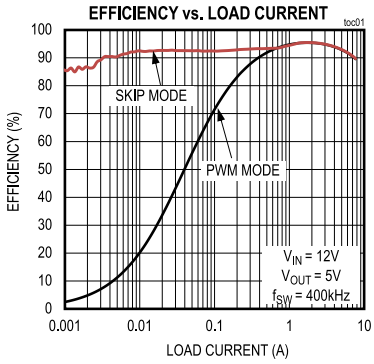
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FB Regulation Voltage	V_{FB}	FB connected to an external resistive divider, 6V < V_{SUPSW} < 36V	0.99	1.005	1.02	V
Transconductance (from FB to internal COMP)	gm		50	66	90	µS
Minimum On-Time	t_{ON_MIN}	f_{SW} = 2.1MHz			80	ns
Maximum Duty Cycle	DC_{MAX}		97	98		%
Oscillator Frequency		f_{SW} = 400kHz	360	400	440	kHz
		f_{SW} = 2.1MHz	1.9	2.1	2.3	MHz
Soft-Start Time	t_{SS}			5		ms
SYNC, SSEN, EN						
External Input Clock Acquisition Time	t_{SYNC}			1		Cycles
External Input Clock Frequency		f_{SW} = 400kHz	300		1200	kHz
		f_{SW} = 2.1MHz	1.8		2.6	MHz
SYNC, SSEN High Threshold	V_{SS_HI}		1.4			V
SYNC, SSEN Low Threshold	V_{SS_LO}				0.4	V
SYNC, SSEN Leakage Current	I_{SS}	T_A = +25°C		0.1	1	µA
EN High Threshold	V_{EN_HI}		2.4			V
EN Low Threshold	V_{EN_LO}				0.6	V
EN Hysteresis	V_{EN_HYS}			0.2		V
EN Leakage Current	I_{EN}	T_A = +25°C		0.1	1	µA
$\overline{\text{RESET}}$						
UV Hysteresis				3		%
UV Threshold		Falling	86	88	90	%
Hold Time				10		ms
UV Debounce Time				25		µs
OV Protection Threshold		Rising	104	107	110	%
		Falling		105		
Leakage Current		V_{OUT} in regulation, T_A = +25°C			1	µA
Output Low Level		I_{SINK} = 5mA			0.4	V

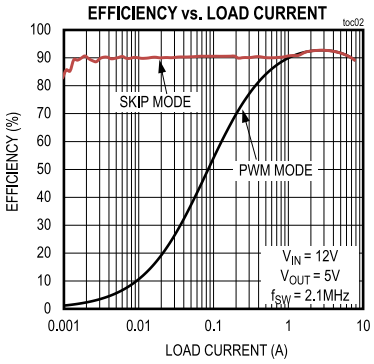
Note 2: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

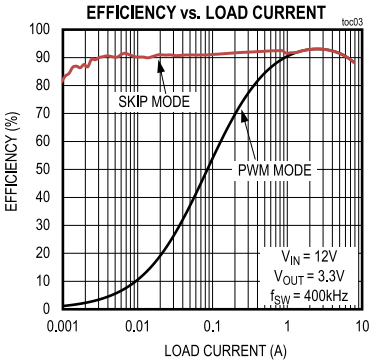
Note 3: The MAX20006EAFOD/VY+ does not support skip mode operation and is FPWM mode only

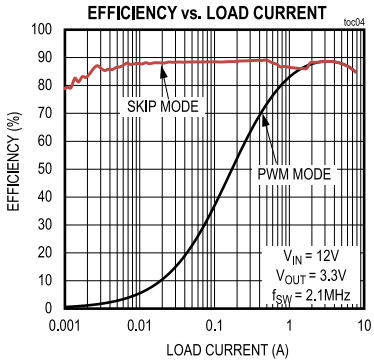
Typical Operating Characteristics

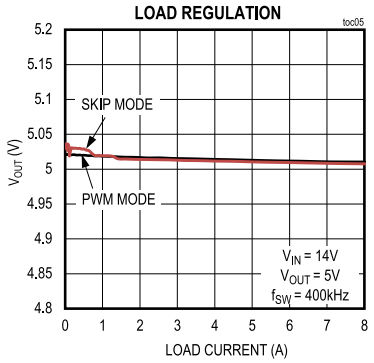
((V_{SUP} = V_{EN} = +14V, T_A = +25°C, unless otherwise noted.))

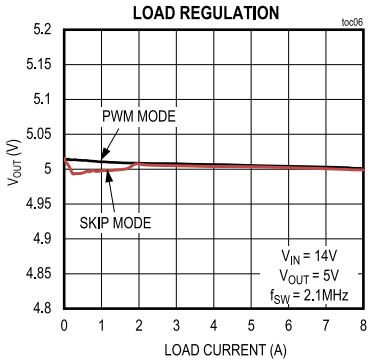


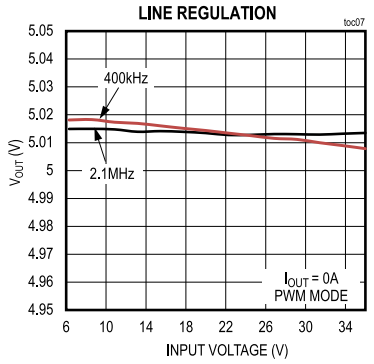


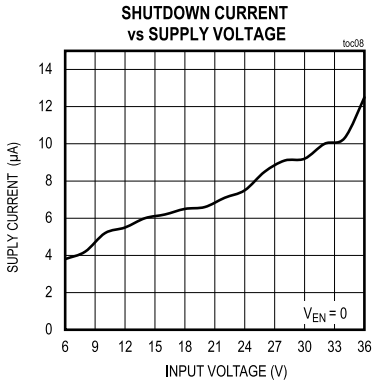


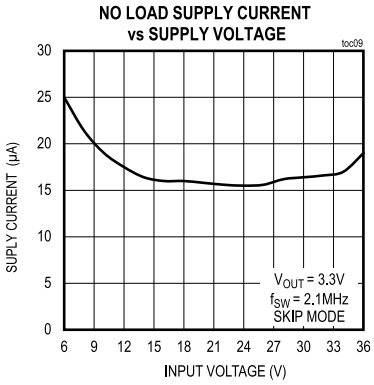








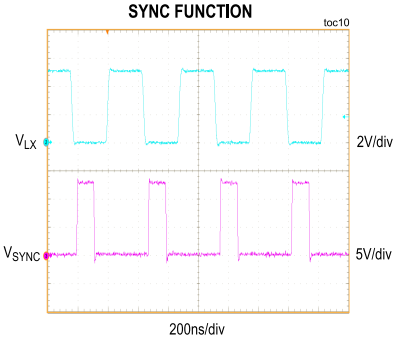




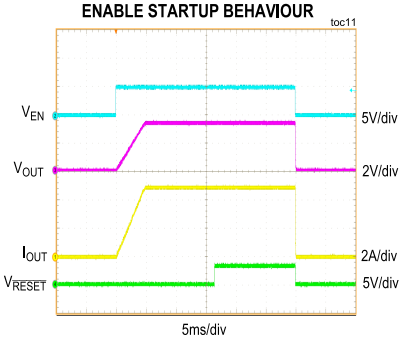
Typical Operating Characteristics (continued)

((V_{SUP} = V_{EN} = +14V, T_A = +25°C, unless otherwise noted.))

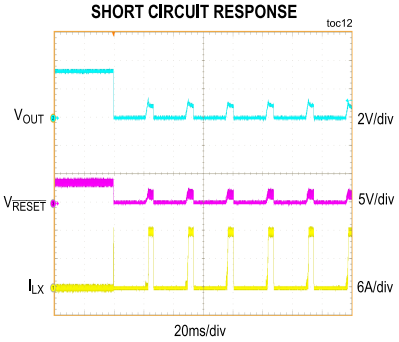
SYNC FUNCTION



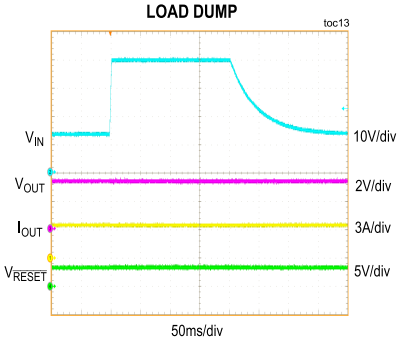
ENABLE STARTUP BEHAVIOUR



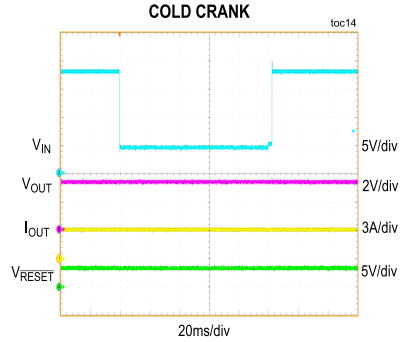
SHORT CIRCUIT RESPONSE



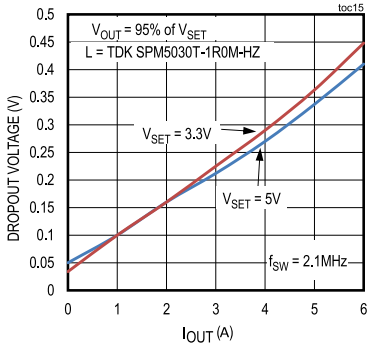
LOAD DUMP



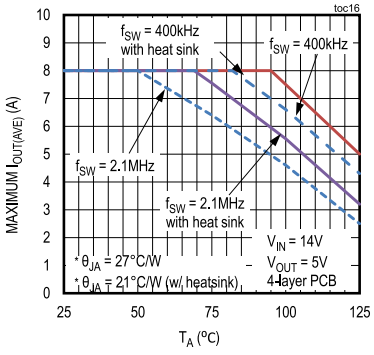
COLD CRANK



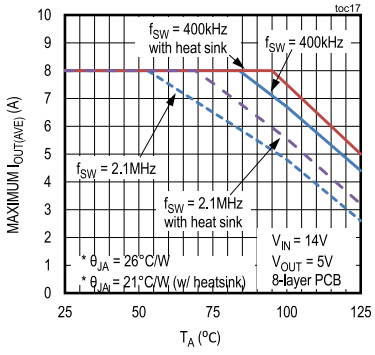
DROPOUT VOLTAGE vs I_{OUT}



MAXIMUM $I_{OUT(AVE)}$

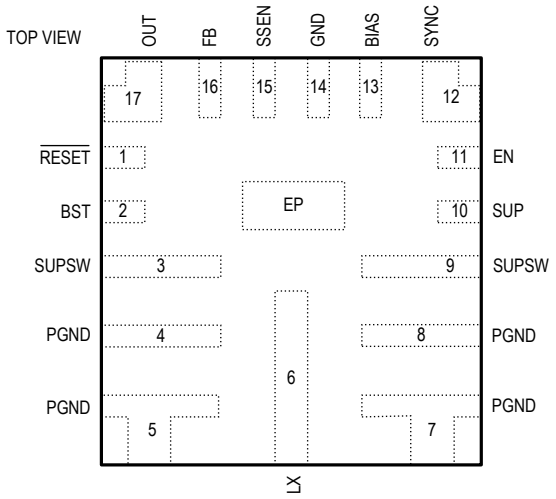


MAXIMUM $I_{OUT(AVE)}$



Pin Configuration

F173A3FY+7



F173A3FY+7
(3.5mm x 3.75mm)

Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{RESET}}$	Open-Drain $\overline{\text{RESET}}$ Output. To obtain a logic signal, pull $\overline{\text{RESET}}$ up with an external resistor.
2	BST	High-Side Driver Supply. Connect a 0.1µF capacitor between LX and BST for proper operation.
3	SUPSW	Supply Input
4, 5	PGND	Power Ground. Connect all PGND pins together.
6	LX	Inductor Connection. Connect LX to the switched side of the inductor. Connect all LX pins together.
7, 8	PGND	Power Ground. Connect all PGND pins together.
9	SUPSW	Internal High-Side Switch Supply Input. SUPSW provides power to the internal switch. Bypass SUPSW to PGND with 0.1µF and 4.7µF ceramic capacitors. Place the 0.1µF as close to the SUPSW and PGND pins as possible, followed by the 4.7µF capacitor.
10	SUP	Voltage Supply Input. SUP powers up the internal linear regulator. SUP is fused directly to SUPSW, so it must be connected directly to SUPSW as close to the IC as possible.
11	EN	SUP Voltage-Compatible Enable Input. Drive EN low to disable the devices. Drive EN high to enable the devices.
12	SYNC	Synchronization Input. Connect SYNC to GND to enable skip-mode operation under light loads. Connect SYNC to BIAS or an external clock to enable fixed-frequency forced-PWM-mode operation. When driving SYNC externally do not exceed the BIAS voltage. The BIAS pin may transition from 5V to the output voltage after startup to increase efficiency. For MAX20006EAFOD/VY+, do not ground SYNC pin, as the part only supports FPWM mode.
13	BIAS	Linear Regulator Output. BIAS powers up the internal circuitry. Bypass with a minimum 2.2µF ceramic capacitor to ground.

Pin Description (continued)

PIN	NAME	FUNCTION
14	GND	Analog Ground.
15	SSEN	Spread Spectrum Enable Input. Connect to BIAS to enable spread spectrum.
16	FB	Feedback Input. Connect a resistor-divider from OUT to FB to GND to set the output voltage. Connect FB to BIAS to select a 3.3V, 3.9V, or 5V fixed output voltage (P/N dependent).
17	OUT	Switching Regulator Output. OUT also provides power to the internal circuitry when the output voltage of the converter is set between 3V and 5V during standby mode.
EP	SUPSW	Exposed pad on the internal high-side switch supply input. Connect to SUPSW pins 3 and 9 on the PCB.

Detailed Description

The MAX20004E/MAX20006E/MAX20008E are 4A, 6A, and 8A current-mode step-down converters, respectively, with integrated high-side and low-side MOSFETs with integrated programmable compensation. The low-side MOSFET enables fixed-frequency FPWM operation in light-load applications. The devices operate at 3.5V (3V after start-up) to 36V input voltages, while using only 15µA (typ) quiescent current at no load (except for MAX20006EAFOD/VY+ which is FPWM mode only). The switching frequency is factory-selectable between 400kHz and 2.1MHz and can be synchronized to an external clock. The devices' output voltage is available as fixed 5V, 3.9V or 3.3V, or adjustable between 1V and 5V. The wide input voltage range, along with the ability to operate at 99% duty cycle during undervoltage transients, make these devices ideal for automotive applications.

In light-load applications, a logic input (SYNC) allows the devices to operate either in skip mode for reduced current consumption, or fixed-frequency FPWM mode to eliminate frequency variation and help minimize EMI. Protection features include cycle-by-cycle current limit and thermal shutdown with automatic recovery.

MAXQ Power Architecture (No Wasted Performance)

The MAXQ power architecture allows the device to achieve the maximum dynamic performance under all worst-case conditions. Without the MAXQ power architecture, typical AC performance would have to be reduced below the device capabilities to guarantee that the device would be stable under all worst-case application conditions. The MAXQ power architecture prevents this wasted capability by keeping the device operating at peak performance.

Thermal Considerations

The devices are available in 4A, 6A, or 8A versions; however, the average output-current capability is dependent on several factors. Some of the key factors include the maximum ambient temperature ($TA_{(MAX)}$), switching frequency (f_{SW}), and the number of layers and the size of the PCB. See the Typical Operating Characteristics for a guideline.

Wide Input Voltage Range

The device is specified to operate over a wide 3V to 36V input voltage range. Conditions such as cold crank can cause the voltage at the SUP and SUPSW pins to drop below the programmed output voltage. Under such conditions, the devices operate in a high duty-cycle mode (dropout mode) and continuously attempt to turn on the HSFET to facilitate minimum dropout from input to output. To maintain gate charge on the HSFET, the BST capacitor must be periodically recharged. To ensure proper charge on the BST capacitor when in dropout, the HSFET is turned off every 13.5µs and the LSFET is turned on for approximately 150ns. This gives an effective duty cycle of greater than 98% in dropout.

For high input voltages, the required duty cycle to regulate its output may be smaller than the minimum on-time (80ns, max). In this event, the device is forced to lower its switching frequency by skipping pulses.

Maximum Duty-Cycle Operation

The device has a maximum duty cycle of 98% (typ). The IC continuously monitors the time between low-side FET switching cycles in both PWM and skip modes. Whenever the low-side FET has not switched for more than 13.5µs (typ), the low-side FET is forced on for 150ns (typ) to refresh the BST capacitor. The input voltage at which the device enters dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design. The input voltage at which the device enters dropout can be approximated as follows:

$$V_{SUP} = \frac{V_{OUT}}{0.98} + I_{OUT} \times R_{HS}$$

where R_{HS} is the high-side switch on-resistance, which should also include the inductor DC resistance for better accuracy.

Linear Regulator Output (BIAS)

The devices include a 5V linear regulator (V_{BIAS}) that provides power to the internal circuit blocks. Connect a 2.2µF ceramic capacitor from BIAS to GND. Under certain conditions, the BIAS regulator turns off and the BIAS pin switches to

OUT (i.e., switches over) after startup to increase efficiency. For IC versions that are factory trimmed for 3.3V/3.9V fixed output, BIAS switches to OUT under light-load conditions in skip mode only. For IC versions that are factory trimmed for 5V fixed output, the BIAS pin switches to OUT after startup regardless of load or skip/PWM mode. In any case, BIAS only switches over if OUT is between 2.8V and 5V. In summary, BIAS can transition from 5V to V_{OUT} after startup depending on load, mode, and IC version.

Soft-Start

The devices include a fixed internal soft-start with factory-selectable options of 5ms and 10ms. Soft-start limits startup inrush current by forcing the output voltage to ramp up towards its regulation point.

RESET Output

The devices feature an open-drain reset output ($\overline{RESET}$). $\overline{RESET}$ asserts when V_{OUT} drops below the specified falling threshold. $\overline{RESET}$ deasserts when V_{OUT} rises above the specified rising threshold after the specified hold time. Connect $\overline{RESET}$ to the output, bias, or I/O voltage of choice with a pullup resistor.

Synchronization Input (SYNC)

SYNC is a logic-level input used for operating-mode selection and frequency control. Connecting SYNC to BIAS or to an external clock enables forced fixed-frequency (FPWM) operation. Connecting SYNC to GND enables automatic skip-mode operation for high light-load efficiency (except for MAX20006EAFOD/VY+ which is FPWM mode only). The IC synchronizes to an external clock frequency at SYNC in two cycles and runs in FPWM mode when the external frequency is within the range specified in the *Electrical Characteristics Table*. When the external clock signal at SYNC is absent for more than two clock cycles, the devices use the internal clock.

System Enable (EN)

An enable control input (EN) activates the devices from their low-power shutdown mode. EN is compatible with inputs from automotive battery level down to 3V. EN turns on the internal linear (BIAS) regulator. Once V_{BIAS} is above the internal lockout threshold (V_{UVBIAS} = 3V (typ)), the converter activates and the output voltage ramps up with the programmed soft-start time. A logic-low at EN shuts down the device. During shutdown, the BIAS regulator and gate drivers turn off. Shutdown is the lowest power state and reduces the quiescent current to 5µA (typ). Drive EN high to bring the device out of shutdown.

Spread-Spectrum Option

Each device has an optional spread spectrum enabled by the SSEN pin. When the SSEN pin is pulled high, the operating frequency is varied ±3% centered on the internal switching frequency (f_{SW}). The modulation signal is a triangular wave with a frequency of 4.5kHz at 2.1MHz. For operation at f_{SW} = 400kHz, the modulation signal scales proportionally (i.e., the modulation frequency reduces by 0.4MHz/2.1MHz). The internal spread spectrum is disabled if the devices are synchronized to an external clock. However, the devices do not filter the input clock on the SYNC pin, and pass any modulation present (including spread spectrum), driving the external clock. Spread spectrum is offered to improve EMI performance of the device.

Thermal Shutdown Protection

Thermal shutdown protects the device from excessive operating temperature. When the junction temperature exceeds the specified threshold, an internal sensor shuts down the internal bias regulator and the step-down converter, allowing the IC to cool. The sensor turns the IC on again after the junction temperature cools by the specified hysteresis.

Current Limit / Short-Circuit Protection

The devices feature a current limit that protects them against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side MOSFET remains on until the inductor current reaches the specified LX current-limit threshold. The converter then turns the high-side MOSFET off and the low-side MOSFET on to allow the inductor current to ramp down. Once the inductor current crosses below the current-limit threshold, the

converter turns on the high-side MOSFET again. This cycle repeats until the short or overload condition is removed.

A hard short is detected when the output voltage falls below 50% of the target while in current limit. If this occurs, hiccup mode activates, and the output turns off for four times the soft-start time. The output then enters soft-start and powers back up. This repeats indefinitely while the short circuit is present. Hiccup mode is disabled during soft-start.

Overvoltage Protection

If the output voltage exceeds the OV protection rising threshold, the high-side MOSFET turns off and the low-side MOSFET turns on. Normal operation resumes when the output voltage goes below the falling OV threshold.

Applications Information

Maximum Output Current

While there are device versions that supply up to 8A, there are many factors that may limit the average output current to less than the maximum. The devices can be thermally limited based on the selected f_{SW}, number of PCB layers, PCB size, and the maximum ambient temperature. See the Typical Operating Characteristics section for guidance on the maximum average current. For a more precise value, the θ_{JA} needs to be measured in the application environment.

Setting the Output Voltage

Connect FB to BIAS for a fixed 5V, 3.3V, or 3.9V output voltage. To set the output to other voltages between 1V and 5V, connect a resistor-divider from the FB output (OUT) to GND (see Figure 1). Select R_{FB2} (FB to GND resistor) less than or equal to 100kΩ. Calculate R_{FB1} (OUT to FB resistor) with the following equation:

Equation 1:

$$R_{FB1} = R_{FB2}\left[\left[\frac{V_{OUT}}{V_{FB}}\right] - 1\right]$$

where V_{FB} is the feedback regulation voltage. See the *Electrical Characteristics* table.

Add a capacitor, C_{FB1}, as shown to compensate the pole formed by the divider resistance and FB pin capacitance as follows:

Equation 2:

$$C_{FB1} = 10pF \times \left[\frac{R_{FB2}}{R_{FB1}}\right]$$

Note: Applications that use a resistor-divider to set output voltages below 4.5V should use IC versions that are factory-trimmed for 3.3V/3.9V fixed output voltage to ensure full output current capability.

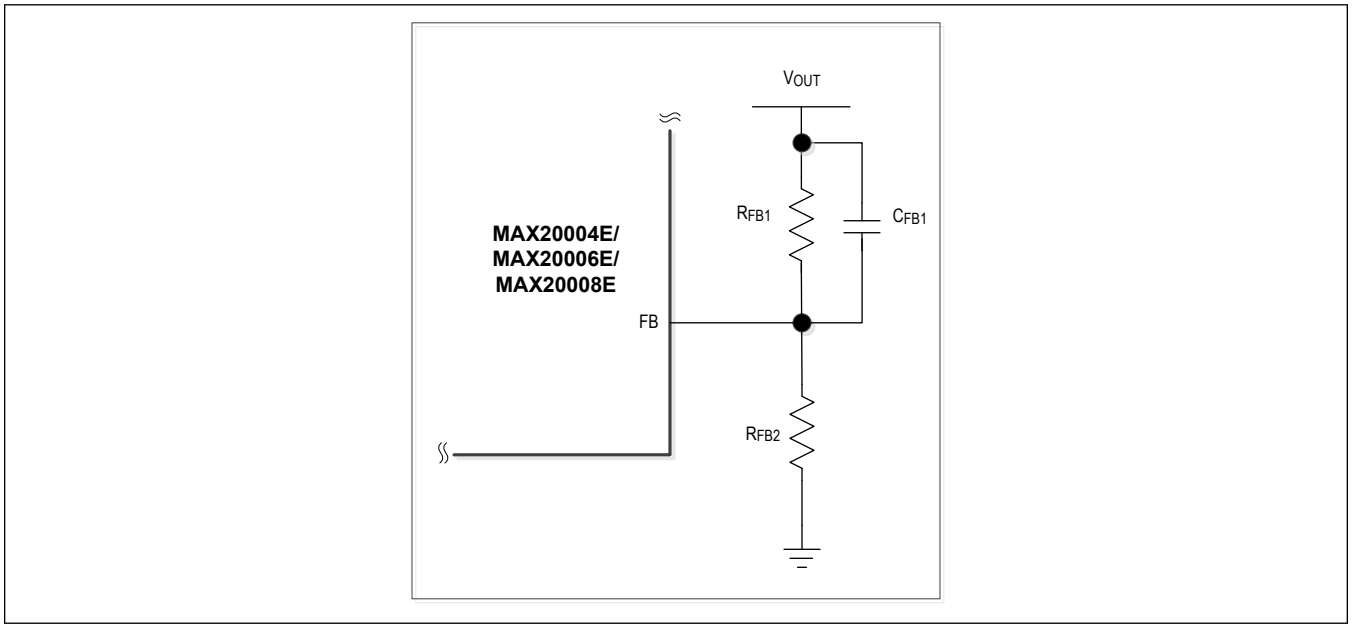


Figure 1. Adjustable Output Voltage Setting

Forced-PWM and Skip Modes

In forced-PWM (FPWM) mode, the devices switch at a constant frequency with variable on-time. In skip mode, the converter's switching frequency is load-dependent. At higher load current, the switching frequency becomes fixed and operation is similar to PWM mode. Skip mode helps improve efficiency in light-load applications by allowing switching only when the output voltage falls below a set threshold. Since the effective switching frequency is lower in skip mode at light load, gate charge and switching losses are lower and efficiency is increased.

Load Regulation

MAX20004E/MAX20006E/MAX20008E devices are designed to have large DC gain by having an integrator at origin in the compensation design. This gives the devices tight load regulation and only 0.2% (typ) variation in output voltage from full load to no load (refer to the *Electrical Characteristics* table). The DC load regulation as a percentage of V_{OUT} can be calculated using the following equation: **Equation 3:** DC load reg (%) = R_{CS} x I_{OUT}/ (G_m x R_{EADC}) where R_{CS} = Current-sense gain I_{OUT} = Maximum DC output current G_m = Internal error amplifier gain R_{EADC} = Output impedance of the error amplifier Using the worst-case numbers for the above parameters gives a worst-case load regulation of 0.6% for MAX20004E/MAX20006E/MAX20008E devices.

Inductor Selection

Three key parameters must be considered when selecting an inductor: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). The devices are designed to operate with the ratio of inductor peak-to-peak AC current to DC average current (LIR) between 15% and 30% (typ). The switching frequency, input voltage, and output voltage then determine the inductor value as follows:

Equation 4:

$$L_{MIN1} = \frac{\left(V_{SUP} - V_{OUT_}\right) \times V_{OUT}}{V_{SUP} \times f_{SW} \times I_{MAX} \times 30\,\%}$$

where V_{SUP} and V_{OUT} are typical values (so that efficiency is optimum for typical conditions) and I_{MAX} is 4A for MAX20004E, 6A for MAX20006E, and 8A for MAX20008E, and f_{SW} is the switching frequency. Note that I_{MAX} is the maximum rated output current for the device, not the maximum load current in the application. The following equation ensures that the internal compensating slope is greater than 50% of the inductor current downslope:

Equation 5:

$$-m \geq \frac{m2}{2}$$

where m is the internal compensating slope and m2 is the sensed inductor current downslope as follows:

Equation 6:

$$m2 = \frac{V_{OUT}}{L} \times R_{CS}$$

where R_{CS} is 0.39 for MAX20004E, 0.29 for MAX20006E, and 0.22 for MAX20008E.

$$m = 1.35 \times \frac{V}{\mu s} \times \frac{f_{SW}}{2.2MHz}$$

Solving for L and using a 1.3x multiplier to account for tolerances in the system:

$$L_{MIN2} = V_{OUT} \times \frac{R_{CS}}{2 \times m} \times 1.3$$

To satisfy both L_{MIN1} and L_{MIN2}, L_{MIN} must be set to the larger of the two as follows:

$$L_{MIN} = \max\left(L_{MIN1}, L_{MIN2}\right)$$

The maximum nominal inductor value recommended is 1.6 times the chosen value from the above formula.

$$L_{MAX} = 2 \times L_{MIN}$$

Select a nominal inductor value based on the following formula:

$$L_{MIN} < L_{NOM} < L_{MAX}$$

The best choice of inductor is usually the standard inductor value closets to L_{NOM}. A summary of typical inductor values for a given operating frequency is provided in Table 1:

Table 1. Inductor Selection Table

FREQUENCY	I_{OUT} (A)	RECOMMENDED INDUCTANCE (µH)
f_{SW} = 2.1MHz	4	1.5
f_{SW} = 2.1MHz	6	1
f_{SW} = 2.1MHz	8	0.8
f_{SW} = 400kHz	4	8.2
f_{SW} = 400kHz	6	6.8
f_{SW} = 400kHz	8	4.7

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

MAX20004E/MAX20006E/MAX20008E incorporate a symmetrical pinout that can be leveraged for better EMI performance. Connect two high-frequency 0603 or smaller capacitors on two SUP pins on either side of the package for good EMI performance. Connect a high-quality, 4.7µF (or larger) low-ESR ceramic capacitor on the SUP pin for low-input voltage ripple. A bulk capacitor with higher ESR (such as an electrolytic capacitor) is normally required as well to lower the Q of the front-end circuit and provide the remaining capacitance needed to minimize input-voltage ripple.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

Equations 7:

$$I_{RMS} = I_{LOAD(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{SUP} - V_{OUT})}}{V_{SUP}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage:

$$V_{SUP} = 2 \times V_{OUT}$$

Therefore:

$$I_{RMS} = \frac{I_{LOAD(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input-voltage ripple consists of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input-voltage ripple using the following equations:

Equations 8:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{\left(V_{SUP} - V_{OUT}\right) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1 - D)}{\Delta V_Q \times f_{SW}}$$

$$D = \frac{V_{OUT}}{V_{SUPSW}}$$

where: I_{OUT} is the maximum output current and D is the duty cycle.

Output Capacitor

Output capacitance is selected to satisfy the output load-transient, output-voltage ripple, and closed-loop stability requirements. During a load step, the output current changes almost instantaneously, whereas the inductor is slow to react. During this transition time, the load-charge requirements are supplied by the output capacitor, which causes an undershoot/overshoot in the output voltage. For a buck converter that is controlled by peak-current, as employed in MAX20004E/MAX20006E/MAX20008E, output capacitance also affects the control-loop stability.

The output ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR}(caused by the ESR of the output capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For aluminum electrolytic capacitors, the entire output ripple is contributed by ΔV_{ESR}. Use Equation 4 to calculate the ESR requirement and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output-ripple voltage from the ESR and the capacitor discharge to be equal. The following equations show the output capacitance and ESR requirement for a specified output-voltage ripple.

Equation 9:

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{p-p}}$$

$$C_{OUT} = \frac{\Delta I_{p-p}}{8 \times \Delta V_Q \times f_{SW}}$$

where

$$\Delta I_{p-p} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

$$V_{OUT_RIPPLE} = \Delta V_{ESR} + \Delta V_Q$$

ΔI_{P-P} is the peak-to-peak inductor current as calculated above, and f_{SW} is the converter's switching frequency.

The output capacitor supplies the step-load current until the converter responds with a greater duty cycle. The resistive drop across the output capacitor's ESR and the capacitor discharge causes a voltage droop during a step load. Use a combination of low-ESR tantalum and ceramic capacitors for better transient-load and ripple/noise performance. Keep the maximum output-voltage deviations below the tolerable limits of the electronics being powered. When using a ceramic capacitor, assume an 80% and 20% contribution from the output-capacitance discharge and the ESR drop, respectively. Use the following equations to calculate the required ESR and capacitance value:

Equation 10:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} \geq \left(\frac{I_{STEP}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times D_{MAX} \times \Delta V_Q}\right) + \left(\frac{I_{STEP} \times t_{DELAY}}{\Delta V_Q}\right)$$

where I_{STEP} is the load step and t_{DELAY} is the delay for the PWM mode, the worst-case delay would be (1-D) t_{SW} when

the load step occurs right after a turn-on cycle. This delay is higher in Skip mode.

Based on internal-compensation design of MAX20004E/MAX20006E/MAX20008E, for optimal phase margin (> 60°, typ), the recommended output capacitances for standard configuration are shown in Table 2. Recommended values are the actual capacitances, after accounting for voltage derating. If a lower or higher output capacitance is required for the application, contact the factory for an optimized solution.

Table 2. Output Capacitance Selection

PARAMETER	I_{OUT} (A)	V_{OUT} (V)	NOMINAL OUTPUT CAPACITANCE (µF)	MINIMUM OUTPUT CAPACITANCE (µF)
f_{SW} = 2.1MHz	4	5	28	24
f_{SW} = 2.1MHz	4	3.3	32	24
f_{SW} = 2.1MHz	6	5	30	22
f_{SW} = 2.1MHz	6	3.3/3.9	36	28
f_{SW} = 400kHz	6	5	50	40
f_{SW} = 400kHz	6	3.3	70	56
f_{SW} = 400kHz	8	5	70	60
f_{SW} = 400kHz	8	3.3	80	70

Compensation Network

An optimized compensation network ensures stable operation of the closed-loop system of the power supply while maximizing the unity gain bandwidth of the loop to meet transient requirements. MAX20004E/MAX20006E/MAX20008E come with internal compensation, which makes the design easy and compact for the engineer. In default mode, the compensation is optimized to be used with the recommended output capacitance as suggested in the previous sections. Depending on the system requirements, the output capacitance required to meet system specifications may change. To facilitate such designs, MAX20004E/MAX20006E/MAX20008E come with a highly configurable compensation network that can be optimized to meet system needs. Trim-selectable wide range of R_{COMP} value, in steps of 10kΩ, allow flexibility in the dynamic performance of the IC. Table 3 shows some of the values of R_{COMP} as a reference, and the corresponding recommended output capacitance for the MAX20006E family with $5V_{OUT}$. Similar customization can be done for different output voltages, current rating, and f_{SW}. Contact the factory for any customized requirements.

Table 3. Output Capacitance Guidelines for Customized Compensation

V_{OUT}	R_{COMP}	FREQUENCY	NOMINAL RECOMMENDED C_{OUT}	MINIMUM RECOMMENDED C_{OUT}	APPROX. BANDWIDTH
5V	185kΩ	2.1MHz	30µF	22µF	200kHz
5V	250kΩ	2.1MHz	40µF	32µF	190kHz
5V	300kΩ	2.1MHz	60µF	44µF	180kHz
5V	209kΩ	400kHz	54µF	46µF	55kHz
5V	300kΩ	400kHz	75µF	60µF	50kHz
5V	400kΩ	400kHz	100µF	72µF	50kHz

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Refer to Figure 2 and the following guidelines for good PC board layout:

1. Use the correct footprint for the IC and place as many copper planes as possible under the IC footprint to insure efficient heat transfer.
2. Place the ceramic input-bypass capacitors, C_{BP} and C_{IN}, as close as possible to the SUPSW and PGND pins on both sides of the IC. Use low-impedance connections (no vias or other discontinuities) between the capacitors and IC pins. C_{BP} should be located closest to the IC and should have very good high-frequency performance (small package size

and high capacitance). Use flexible terminations or other technologies instead of series capacitors for these functions if failure modes are a concern. This will provide the best EMI rejection and minimize internal noise on the device, which can degrade performance.

3. Place the inductor (L), output capacitors (C_{OUT}), boost capacitor (C_{BST}) and BIAS capacitor (C_{BIAS}) in such a way as to minimize the area enclosed by the current loops. Place the inductor (L) as close as possible to the IC LX pin and minimize the area of the LX node. Place the output capacitors (C_{OUT}) near the inductor so that the ground side of C_{OUT} is near the C_{IN} ground connection to minimize the current-loop area. Place the BIAS capacitor (C_{BIAS}) next to the BIAS pin.
4. Use a contiguous copper GND plane on the layer next to the IC to shield the entire circuit. GND should also be poured around the entire circuit on the top side. Ensure that all heat-dissipating components have adequate connections to copper for cooling. Use multiple vias to interconnect GND planes/areas for low impedance and maximum heat dissipation. Place vias at the GND terminals of the IC and input/output/bypass capacitors. Do not separate or isolate PGND and GND connections with separate planes or areas.
5. Place the feedback resistor-divider (if used) near the IC and route the feedback and OUT connections away from the inductor and LX node and other noisy signals.

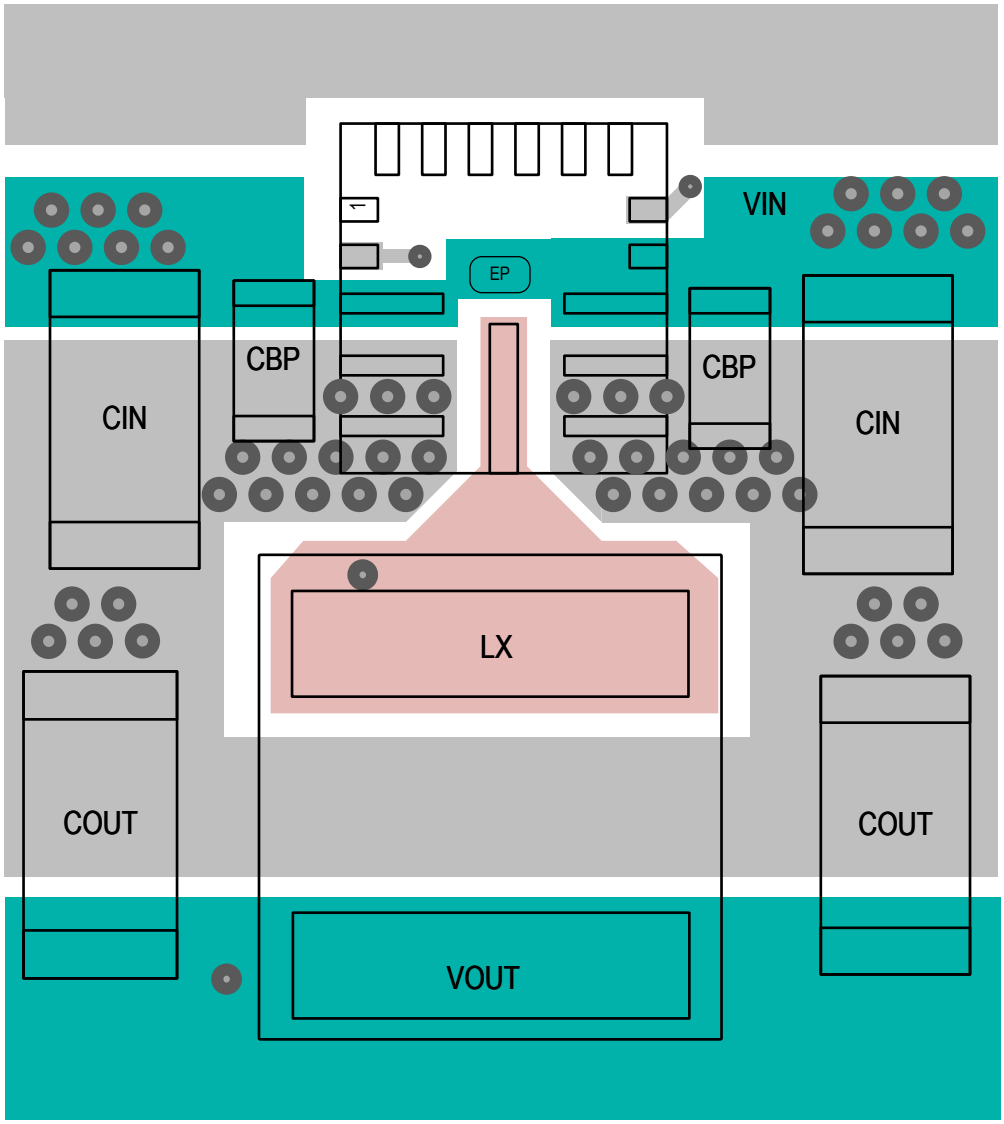
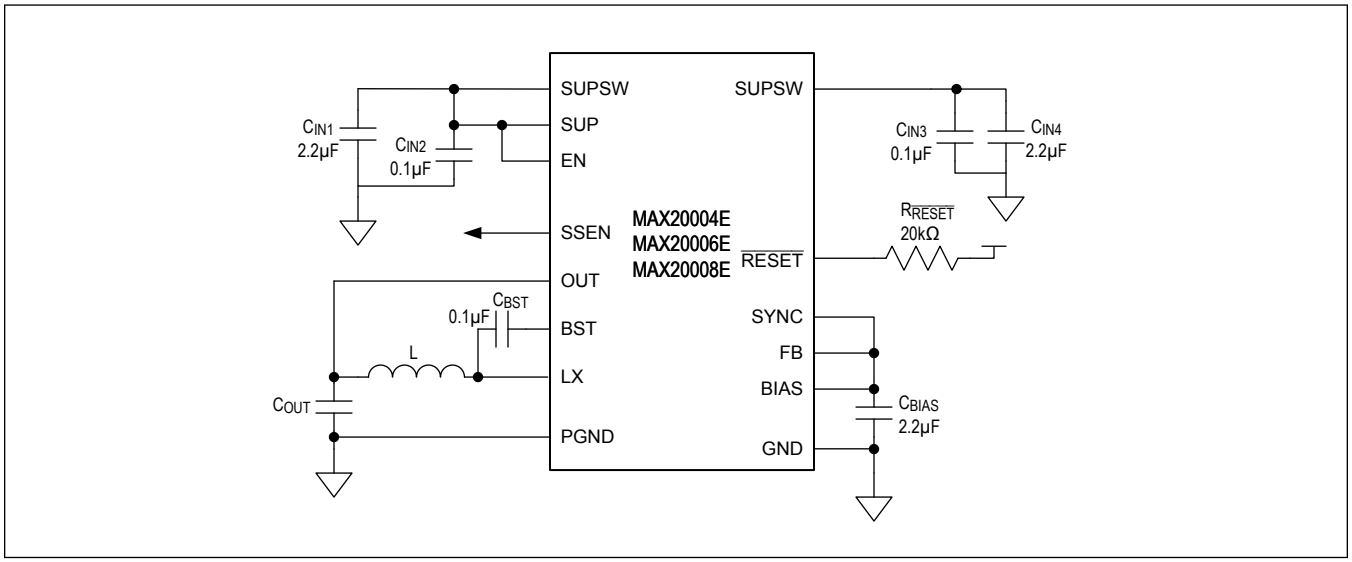


Figure 2. Simplified Layout Example

Typical Application Circuits

Typical Application Circuit for f_{SW} = 2.1MHz, I_{OUT} = 6A and Fixed Output Voltage Version



Ordering Information

PART NUMBER	Skip/FPWM Mode	V_{OUT} (FB TIED TO BIAS) (V)	MAXIMUM OPERATING CURRENT (A)	FREQUENCY (kHz) [1]	SOFT START (ms) [2]	T_{HOLD} (ms) [3]	R_{COMP} (kΩ) [4]
MAX20004EAFOA/VY+	Both	5	4	2100	5	10	209
MAX20004EAFOB/VY+	Both	3.3	4	2100	5	10	233
MAX20006EAFOA/VY+	Both	5	6	2100	5	10	185
MAX20006EAFOB/VY+	Both	3.3	6	2100	5	10	173
MAX20006EAFOD/VY+	FPWM Only	3.9	6	2100	5	10	173
MAX20006EAFOE/VY+*	Both	3.9	6	2100	5	10	173
MAX20008EAFOC/VY+	Both	3.3	8	400	5	10	161
MAX20008EAFOD/VY+	Both	5	8	400	5	10	161

Contact factory for variants with different options.

1 - 2100kHz or 400kHz

2 - 5ms or 10ms

3 - 0.2ms or 10ms

4 - 70kΩ to 1000kΩ in 10kΩ steps

/V+ Denotes Automotive Qualified Parts

+ Indicates a lead (Pb) free/RoHS compliant package

** Future product - contact factory for availability*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/19	Initial release	-
1	7/19	Updated *Electrical Characteristics*, *Applications Information*, and *Ordering Information*	4, 5, 12, 17
2	8/19	Updated *Applications Information* and *Ordering Information*	14, 16, 17
3	10/19	Remove the FC2QFN from *Package Information*, remove the F173A3FY+5 from *Pin Configurations*, remove MAX20006EAFOC/VY+, add MAX20004EAFOB/VY+	3, 8, 17
4	1/20	Removed future-product notation from MAX20006EAFOA/VY+ and MAX20006EAFOB/VY+ in *Ordering Information*	17
5	5/20	Updated *Pin Configurations*, *Pin Descriptions*, and *Applications Information*	8, 9, 17, 19
6	7/20	Updated *General Description*, *Electrical Characteristics*, *Pin Descriptions*, *Detailed Description*, *Typical Application Circuits*, and *Ordering Information*	1, 3, 4, 8, 10, 20

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