EVALUATION KIT AVAILABLE

MAX17710

Energy-Harvesting Charger and Protector

General Description

The MAX17710 is a complete system for charging and protecting micropower-storage cells such as Infinite Power Solutions' THINERGY® microenergy cells (MECs). The IC can manage poorly regulated sources such as energy-harvesting devices with output levels ranging from 1µW to 100mW. The device also includes a boost regulator circuit for charging the cell from a source as low as 0.75V (typ). An internal regulator protects the cell from overcharging.

Output voltages supplied to the target applications are regulated using a low-dropout (LDO) linear regulator with selectable voltages of 3.3V, 2.3V, or 1.8V. The output regulator operates in a selectable low-power or ultra-low-power mode to minimize drain of the cell. Internal voltage protection prevents the cell from overdischarging.

The device is available in an ultra-thin, 3mm x 3mm x 0.5mm 12-pin UTDFN package.

Applications

- Powered/Smart Cards
- Remote Wireless Sensors
- Memory and Real-Time Clock Backup
- Semiactive RFID Tags
- Medical Devices
- High-Temperature Applications
- Military/DoD and Aerospace
- Toys

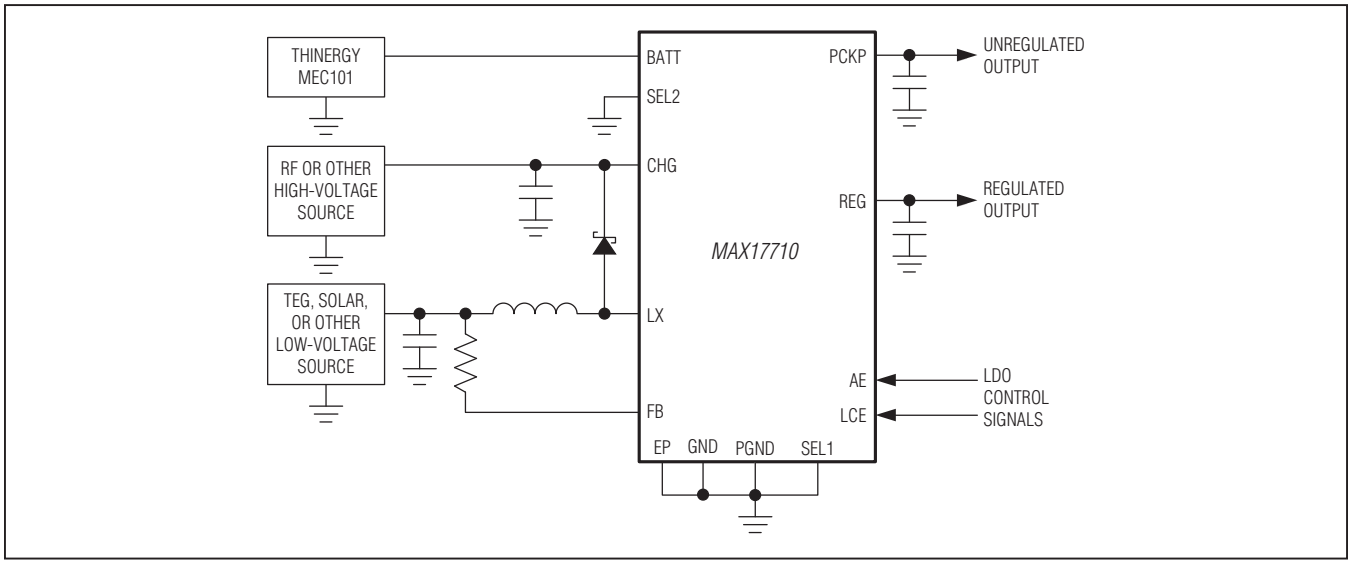
Features

- **Integrated Power-Management IC for Energy Storage and Load Management**
- **Lithium Charger**
  - **1nA Standby I_{QBATT}**
  - **625nA Linear Charging**
  - **1µW Boost Charging**
- **Lithium Cell Undervoltage Protection**
- **Charger Overvoltage Shunt Protection**
- **1.8V, 2.3V, or 3.3V LDO (150nA I_{QBATT})**
- **Lithium Cell Output Buffering**
- **Ultra-Thin, 3mm x 3mm x 0.5mm UTDFN Package**

***Ordering Information* appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to: **www.maximintegrated.com/MAX17710.related**.*

Simplified Operating Circuit



THINERGY is a registered trademark of Infinite Power Solutions, Inc.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-5872; Rev 2; 12/12

ABSOLUTE MAXIMUM RATINGS

BATT to GND ..... -0.3V to +6V
CHG to GND ..... -0.3V to +6V
LX to PGND ..... -0.3V to +6V
GND to PGND ..... -0.3V to +0.3V
FB, AE, LCE, SEL1, SEL2, REG, PCKP to GND ..... -0.3V to V_{BATT} + 0.3V
CHG Continuous Current (limited by power dissipation of package) 100mA
Continuous Power Dissipation (T_A = +70°C) UTDFN (derate 15mW/°C above +70°C) 1200mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CHG} = +4.3V, Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHG Input Maximum Voltage		Limited by shunt regulator (Note 2)	4.875	5.3	5.7	V
CHG Enable Threshold	V_{CE}		4.07	4.15	4.21	V
CHG Quiescent Current	I_{QCHG}	V_{CHG} = 4.0V rising, V_{BATT} = 4.0V		625	1300	nA
CHG Shunt Delay				25		µs
CHG Input Shunt Limit		(Note 2)			50	mA
CHG Maximum Input Current		V_{CHG} input current limited by Absolute Maximum Ratings	50	100		mA
CHG-to-BATT Dropout Voltage		V_{CHG} = 4.0V, I_{CHG} = 1µA		45		mV
		V_{CHG} = 4.0V, I_{BATT} = -6mA		55		
		V_{CHG} = 4.0V, I_{BATT} = -20mA		65		
		V_{CHG} = 4.0V, I_{BATT} = -40mA		100		
BATT REG						
BATT Regulator Voltage			4.065	4.125	4.160	V
BATT Regulation Delay		V_{CHG} = 4.2V, starting at 4V		30		µs
BATT Quiescent Current	I_{QBATT}	Regulator in dropout; V_{CHG} = 4.15V, V_{BATT} = 4.12V		450	1030	nA
		Harvest standby (AE pulse low) V_{CHG} = 0V, V_{BATT} = 2.1V to 4.0V		1	165	
		AE regulator on, boost off; V_{CHG} = 0V, V_{BATT} = 4.0V, AE high		725	1650	
		LCE regulator on, boost off; V_{BATT} = 4.0V, LCE mode (Note 3)		150	550	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CHG} = +4.3V, Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LINEAR LDO REGULATOR						
REG Voltage		V_{PCKP} = 4.0V, I_{REG} = 50µA, SEL1 = open	3.22	3.3	3.37	V
		V_{PCKP} = 4.0V, I_{REG} = 50µA, SEL1 = GND	2.25	2.3	2.375	
		V_{PCKP} = 4.0V, I_{REG} = 50µA, SEL1 = BATT	1.75	1.8	1.9	
REG Voltage, LCE Mode (Note 3)		V_{PCKP} = 4.0V, I_{REG} = 50µA, SEL1 = open	2.9	3.3	3.7	V
		V_{PCKP} = 4.0V, I_{REG} = 50µA, SEL1 = GND	2.1	2.3	2.5	
		V_{PCKP} = 4.0V, I_{REG} = 50µA, SEL1 = BATT	1.6	1.8	2.05	
REG Current Limit		V_{REG} = 2.15V, V_{PCKP} = 3.8V, AE high	75			mA
		V_{REG} = 2.15V, V_{PCKP} = 3.8V, LCE mode (Note 3)	50			µA
REG Startup Time		V_{PCKP} = 4.0V, AE rising, C_{REG} = 1µF		5.3		ms
LCE Threshold High (Note 4)	V_{IH-LCE}	SEL1 = open	2.175			V
		SEL1 = GND	1.575			
		SEL1 = BATT	1.30			
LCE Threshold Low (Note 5)	V_{IL-LCE}	SEL1 = open			0.9	V
		SEL1 = GND			0.6	
		SEL1 = BATT			0.5	
PCKP REGULATOR						
AE Threshold High	V_{IH-AE}		1.13			V
AE Threshold Low	V_{IL-AE}				0.15	V
AE Low Input Current		V_{AE} = 0V, persists < 1µs	-4	-2		µA
		V_{AE} = 0V, persists > 1µs		1		nA
AE High Input Current		V_{AE} = 3.6V		1		nA
PCKP Enable Threshold		REG enabled	3.62	3.7	3.78	V
PCKP Charge Current		V_{PCKP} = 0V, V_{BATT} = 2.2V		100		mA
PCKP Impedance Ramp Rate		V_{BATT} = 4.0V, resistance between BATT and PCKP from high impedance to 5Ω		5		ms
BATT Undervoltage Lockout (UVLO) Delay	t_{UVLO1}	V_{BATT} = 2.15V, AE high, first ramp of PCKP		5		s
BATT UVLO Delay	t_{UVLO2}	V_{BATT} = 2.15V, AE high, not first PCKP ramp		0.5		ms
BATT UVLO Threshold		AE regulator active, LCE regulator inactive	1.990	2.15	2.30	V
		LCE regulator active, AE regulator inactive		3		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CHG} = +4.3V, Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BOOST REGULATOR						
CHG Regulation Voltage		V_{BATT} = 4.125V	4.3	4.5	4.7	V
Frequency		V_{BATT} = 3.9V, V_{CHG} = 3.95V	0.73	1	1.27	MHz
Boost Turn-On Time	$t_{BOOST-ON}$	Design guidance, typical only		850		ns
FB Threshold	FB_{ON}	Rising (enable)	0.485	0.75	1.0	V
	FB_{OFF}	Falling (disable), V_{CHG} = 3.8V	0.22	0.25	0.27	
FB Input Current Low		V_{FB} = GND, momentary		600		nA
LX nMOS On-Resistance	R_{DS-ON}	I_{LX} = 20mA, V_{BATT} = 3.8V, SEL2 = GND	0.275	0.5	0.7	Ω
		I_{LX} = 10mA, V_{BATT} = 3.8V, SEL2 = open	4	8	12	

Note 1: Specifications are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.

Note 2: Since the CHG shunt regulator has a 25µs delay, the user must limit the voltage to the Absolute Maximum Rating until the internal CHG shunt provides the voltage limit at the pin in response to 50mA input. Larger currents must be shunted with an external clamp to protect the CHG pin from damage.

Note 3: LCE mode is entered by pulsing AE high, then pulsing AE low.

Note 4: For logic-high, connect LCE to the REG output. Do not connect to the BATT or PCKP pins.

Note 5: Since LCE is compared to the REG pin voltage for operation, the low-power regulator cannot be switched off under conditions where the REG output is shorted to GND.

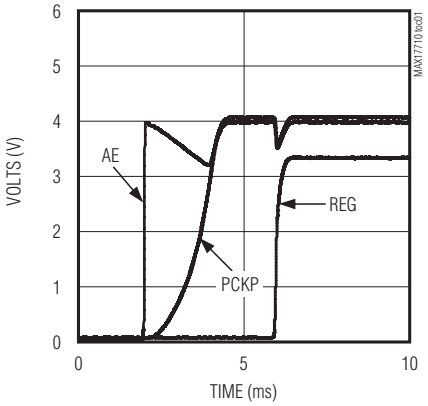
Table 1. Summary of Typical Quiescent Current vs. Operating Conditions

NAME	MODE	CONDITIONS	I_{QBATT} (nA)	I_{QCHG} (nA)	TOTAL QUIESCENT CURRENT (nA)
Standby	Cell Connection: Regulator outputs off, no charger present	Cell connected to circuit during assembly	1	—	1 (from cell)
Shutdown	UVLO or Shutdown: Regulator outputs off, no charger present	V_{BATT} falls below 2.15V or AE and LCE pulsed low	1	—	1 (from cell)
Full Charge	Charger Present: Regulator outputs off, cell charging	V_{CHG} = 4V, $V_{CHG} > V_{BATT}$, AE pulsed low	1	625	626 (from energy-harvesting cell); **can harvest down to 1µW**
Dropout Charge	Charger in Dropout: Regulator outputs off, charger present, but below regulation voltage	V_{CHG} = 4.15V, V_{BATT} = 4.12V, AE pulsed low	450	—	450 (from cell)
AE Active	AE Regulator On: Boost off, no charge source present	AE pulsed high	725	—	725 (from cell)
AE and LCE Active	AE and LCE Regulators On: Boost off, no charge source present	LCE pulsed high after AE pulsed high	875	—	875 (from cell)
LCE Active	LCE Regulator On: Boost off, no charge source present	AE pulsed high, then LCE pulsed high, then AE pulsed low	150	—	150 (from cell)

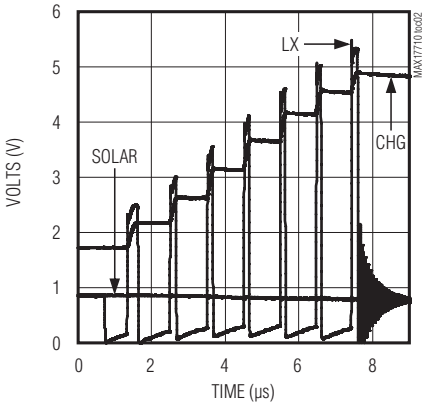
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

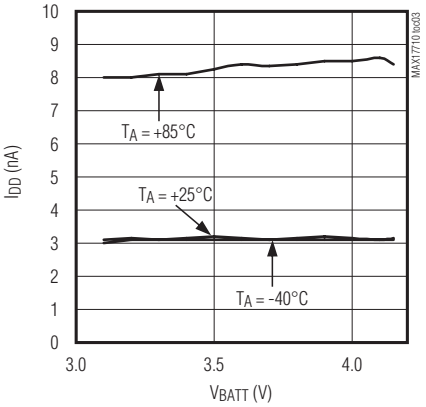
REGULATOR STARTUP



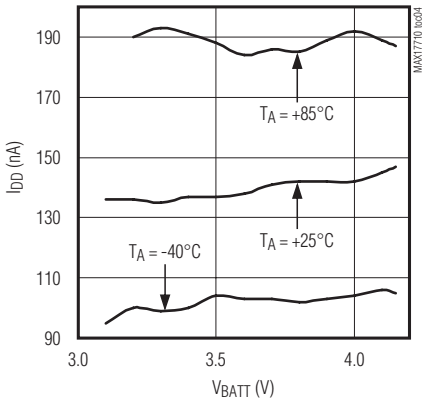
BOOST STARTUP



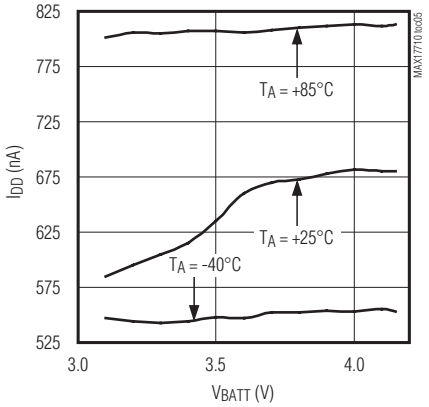
I_{DD} vs. V_{BATT} OVERTEMPERATURE LCE AND AE AND SEL1 = GND



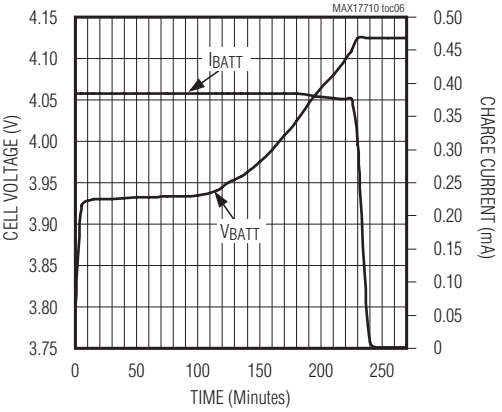
I_{DD} vs. V_{BATT} OVERTEMPERATURE LCE = VREG, AE, AND SEL1 = GND



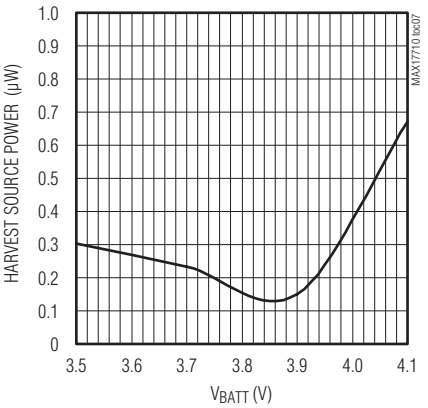
I_{DD} vs. V_{BATT} OVERTEMPERATURE AE = BATT, LCE, AND SEL1 = GND



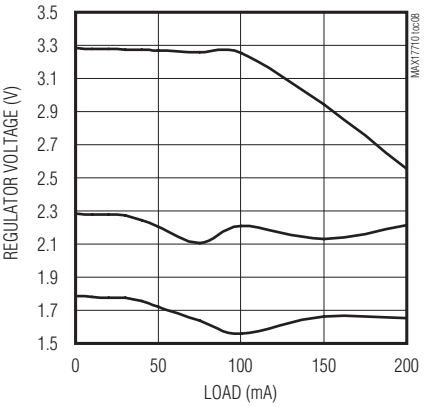
MEC101 CELL CHARGE PROFILE 2.5mW CHARGE SOURCE



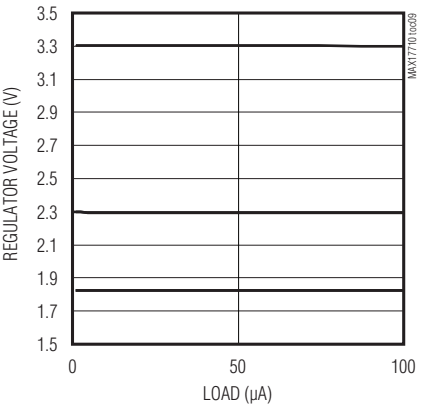
BOOST CIRCUIT BREAK-EVEN THRESHOLD vs. CELL VOLTAGE (STANDARD APPLICATION CIRCUIT)



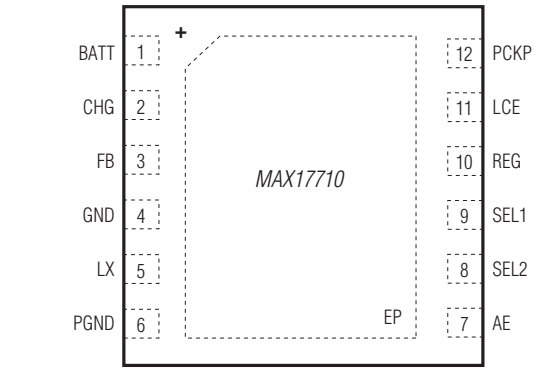
AE LOAD REGULATION



LCE LOAD REGULATION



Pin Configuration



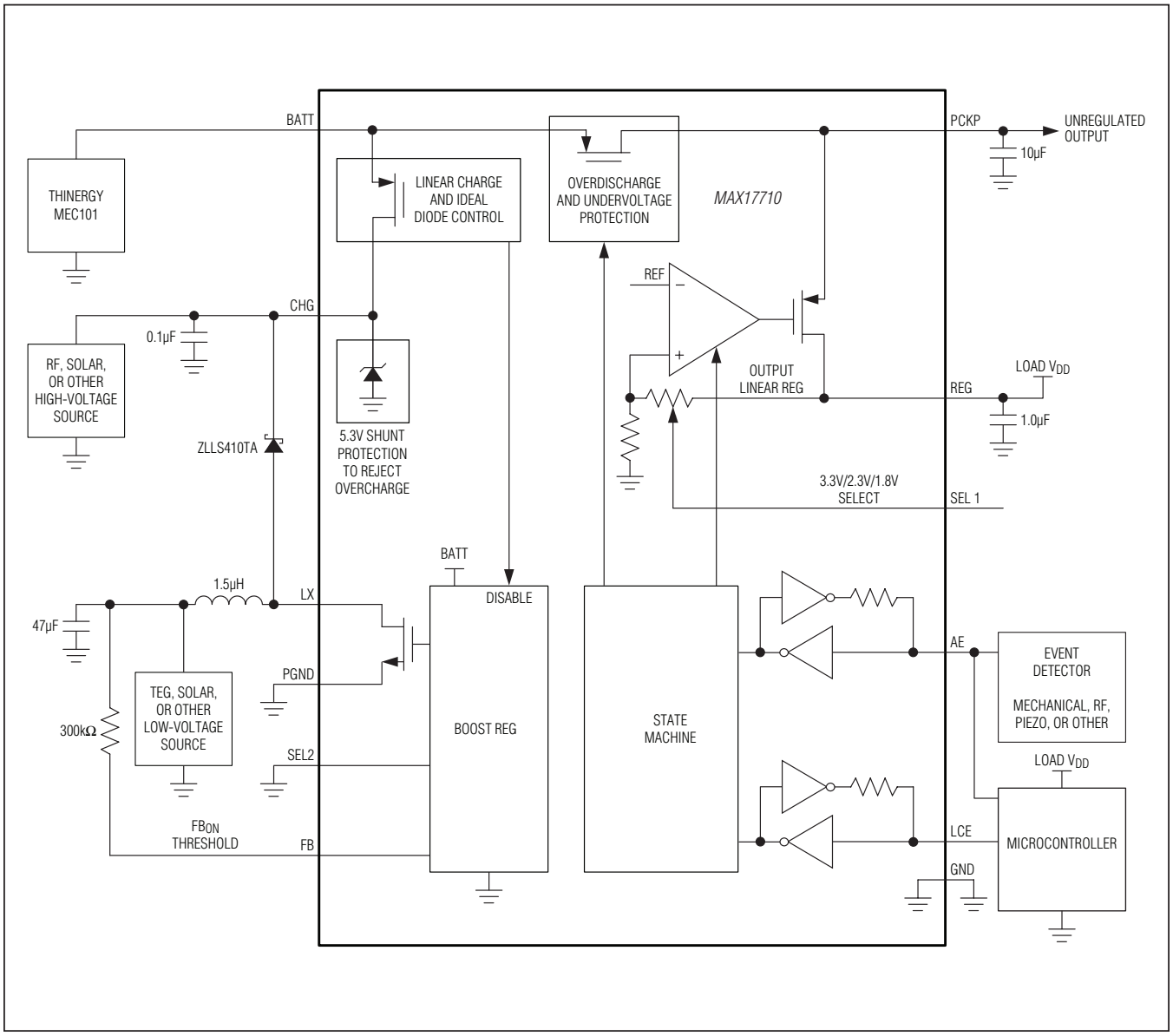
UTDFN

Pin Description

PIN	NAME	FUNCTION
1	BATT	Cell Input. Connect to the positive terminal of the cell without a bypass capacitor.
2	CHG	Charge Input. The IC charges the cell from the power source applied to this pin. Connect to the output of the boost circuit or directly to a 4.21V or higher charge source.
3	FB	Boost Enable. The boost circuit is enabled by driving this pin above the FB_{ON} threshold. Afterwards, the boost circuit is disabled by driving this pin below FB_{OFF}.
4	GND	Device Ground. Connect to system ground.
5	LX	Boost Input. Controls current drive through inductor of external boost circuit.
6	PGND	Power Ground. Connect to system ground.
7	AE	Active Enable. Pulse high to enable high-power regulator output. Pulse low to disable regulator output.
8	SEL2	Boost R_{DS-ON} Select. Connect to system ground to select a boost R_{DS-ON} of 0.5Ω for typical applications.
9	SEL1	Regulator Voltage Select. Ground this pin to select a regulator output voltage of 2.3V, leave disconnected for a regulator output voltage of 3.3V, or connect to the BATT pin for a regulator output voltage 1.8V.
10	REG	Regulator Output. Connect to load circuit. Bypass to system ground with a 1µF (typ) capacitor.
11	LCE	Low-Current Enable. Pulse high to enable the low-current regulator output after the high-current regulator output is already active. Pulse low to disable.
12	PCKP	Protected Output of Pack. Connect an external capacitor to PCKP to support energy buffering to the load, especially in low-temperature applications (see Table 4). PCKP is used for pulsed current storage.
—	EP	Exposed Pad. Connect to GND.

Energy-Harvesting Charger and Protector

Block Diagram



Detailed Description

Operation

The MAX17710 controls two main functions related to management of an energy-harvesting application: charging a low-capacity cell with overcharge protection and an LDO regulator output with overdischarge protection. With the exception of protection features, charging and regulation functions operate completely independently of one another.

Initial power-up of the device occurs when a cell is connected to the BATT pin. In this state, the device pulls only 1nA (typ) from the cell and LDO functions are disabled. Only after a charger has been applied and V_{CHG} rises above 4.15V (V_{CE}) does the device initialize to full operation and allow discharging.

Charge-Regulator Operation

The device charges the cell from an external energy source connected to the CHG pin. Whenever the voltage on CHG is greater than the voltage on BATT, the energy-harvesting circuit directly passes current to the cell without any interaction from the device. When CHG rises above V_{CE}, the input linear regulator turns on to limit the charging voltage to 4.125V and protects the cell from overcharge. Also at this time, any UVLO is reset, allowing the LDO to power the application load. This release of the lockout is latched by CHG exceeding V_{CE} and remains active after the removal of the charge voltage. The state of this latch is off when initial power is applied to the BATT pin.

While charging, the device consumes approximately 625nA from the CHG source until the voltage on CHG exceeds 4.15V. Above 4.15V, the IC enters dropout and BATT quiescent current increases from 1nA to 450nA.

CHG Shunt

Whenever a harvest source pulls the CHG pin above 5.3V, an internal shunt regulator enables a path to GND to limit the voltage at the CHG pin. The internal shunt path can sustain currents up to 50mA. If it is possible for the harvest source to exceed this power limit, an external protection circuit is required to prevent damage to the device. Figure 1 shows the typical application charge circuit harvesting from high-voltage charge sources. Note that a 0.22µF on CHG is recommended for shunt stability when charging from high-voltage sources.

In the application circuit example, the cell is charged by several high-voltage harvest sources. Whenever either harvest source voltage is higher than the cell voltage, charge is transferred directly. If either charge source exceeds 4.15V, the device begins to limit current flow to regulate the cell's voltage to 4.125V. If either charge source exceeds 5.3V, the internal CHG shunt discharges up to 50mA through the device to GND to protect the CHG pin.

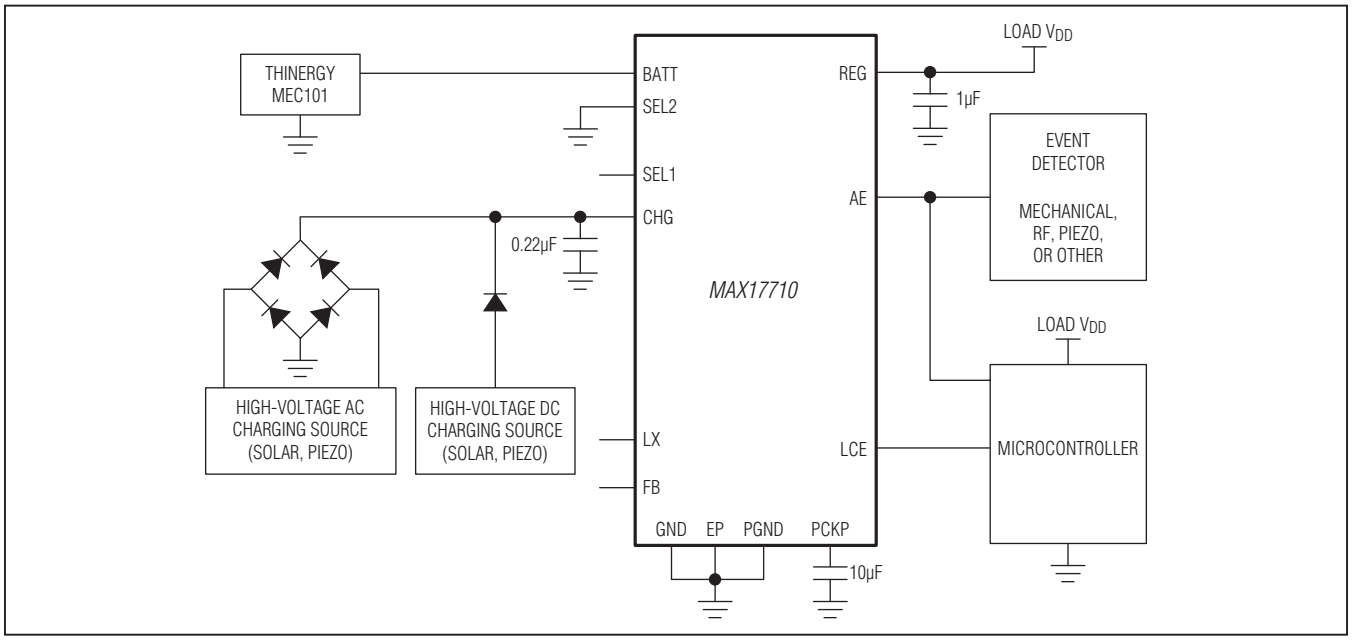


Figure 1. Typical Application Charge Circuit Harvesting from High-Voltage Charge Sources

Boost Regulator Operation

The device includes a simple boost regulator controller to support energy harvesting from low-voltage solar or thermoelectric generator (TEG) devices. The boost converter can harvest energy down to approximately 1µW when operated in pulsed harvest mode and as high as 100mW in continuous conversion. For a 0.8V harvest source and a 4.1V cell, the device can deliver over 20mA (80mW), as long as the harvest source can support it. Figure 2 shows the typical application boost circuit boost harvesting from a low-voltage solar-cell array.

In the application circuit example, the solar cell array charges the 47µF harvest-source capacitor until the voltage on FB exceeds the FB_{ON} threshold. At this time, the LX pin is pulled low to force current through the external inductor. LX begins to oscillate at a fixed 1.0MHz with 90% duty cycle. Each time LX is released by the device, the external inductor forces the voltage of LX above CHG and charges the 0.1µF CHG pin capacitor. When CHG rises above the voltage of V_{BATT}, charge is delivered to the cell. If the CHG pin exceeds 4.5V during this time, the boost converter enters a skip-mode operation to limit voltage on CHG to 4.5V. Operation continues until the voltage of the harvest-source capacitor collapses, driving FB below the FB_{OFF} threshold, which disables the boost circuit. The process repeats after the harvest source capacitor is recharged.

Because the boost converter draws its quiescent current directly from the cell (for startup reasons), it is important to only enable the boost converter when it can provide more power than the boost converter consumes from the cell. This can be guaranteed as long as the capacitor across the TEG is large enough to boost CHG above the BATT pin. Note that it is important to use a high-speed Schottky diode between LX and CHG to guarantee LX does not exceed its absolute maximum voltage rating during boost operation.

Charge Regulator Component Selection

External component selection depends on the charge sources available to the device. Proper component selection provides the highest efficiency operation of the IC during energy harvesting. See Figure 2 as a reference. This section describes component selection for boost sources with operational voltages of 1.0V or high-voltage sources. For boost charge sources with operational voltages between 1.0V and 2.0V, additional components are required. See the *FB Divider* section for a detailed description.

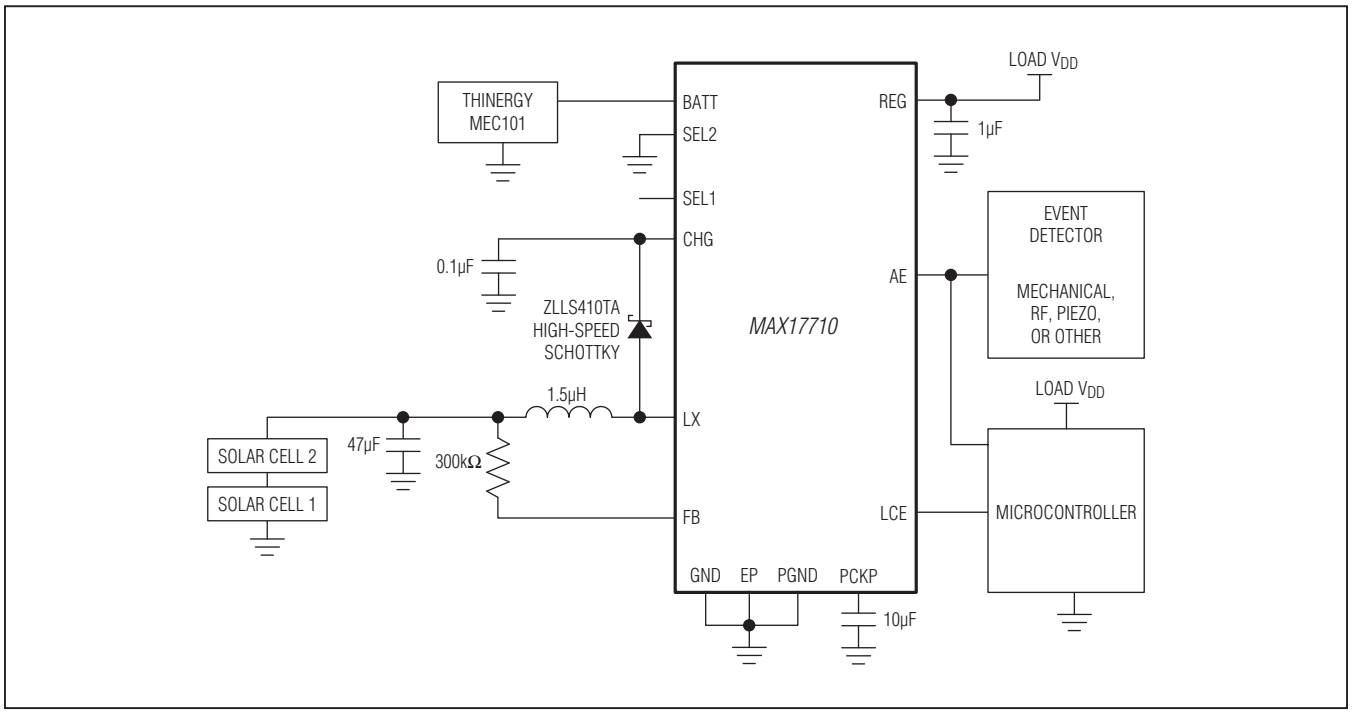


Figure 2. Typical Application Boost Circuit Boost Harvesting from a Low-Voltage Solar-Cell Array

CHG Capacitor

The CHG pin capacitor should be minimized to 0.1µF for highest charge efficiency. However, when charging from a high-voltage source, at least 0.22µF is required for shunt stability.

LX Inductor

The LX pin inductor is not required for high-voltage charge sources. For low-voltage sources, a minimum inductor value of 0.68µH is required to prevent the maximum current rating of the LX pin from being exceeded. Minimum inductor value is calculated as follows:

$$\text{LX inductor} = V_{FB\text{-}ON} \times t_{BOOST\text{-}ON}/LX_{IMAX} = 1.0V \times 850ns/1A = 0.85\mu H$$

Boost Diode

The boost circuit diode must be a high-speed Schottky, such as the ZLLS410TA from Diodes Incorporated. The diode must turn on quickly to clamp the LX pin voltage rise at 6.0V or lower when the LX driver turns off. The LX pin can be damaged if the maximum voltage is exceeded.

Harvest Source Capacitor

The harvest source capacitor must be a minimum of 70 times larger than the CHG pin capacitor to boost the charge pin to the maximum charge voltage under worst-case conditions:

$$\text{Source capacitor} = (4.125V)^2/(0.485V)^2 \times \text{CHG capacitor}$$

This is the minimum size required for operation. Increasing the size of the harvest source capacitor beyond this level improves charge circuit efficiency at extremely low input power (< 10µW), but care should be taken not to increase the capacitor so large that the harvest source cannot overcome the capacitor's leakage. A maximum value of 47µF is recommended.

Table 2 lists boost converter external component values. Minimum capacitor and inductor values are required for proper operation of the charge circuit. Recommended capacitor and inductor values provide optimum charge efficiency. Components should be sized as close to the recommended values that the application allows. Component values below the minimum values, or above the optimum values, are not recommended.

FB Divider

Charge sources with operational voltages between 1.0V and 2.0V require boosting, but are too high a voltage to control the boost circuit efficiently. Under these conditions, a voltage-divider is required to lower the voltage seen by the FB pin (see Figure 3). The divider formed by R1 and R2 allows the voltage on the FB pin to transition properly between the FB_{ON} and FB_{OFF} thresholds during boosting. The value for R2 is calculated as follows:

$$V_{HARVEST\text{-}ON} = F_{BON} \times (R1 + R2)/R1$$

$$R2 = (V_{HARVEST\text{-}ON} - 1.0V) \times 500k\Omega$$

where $V_{HARVEST\text{-}ON}$ is the operational voltage of the harvest source.

Table 2. Boost Converter External Component Values

APPLICATION CHARGE SOURCE	CHG CAPACITOR (µF)	MINIMUM LX INDUCTOR (µH)	RECOMMENDED LX INDUCTOR (µH)	MINIMUM HARVEST SOURCE CAPACITOR (µF)	RECOMMENDED HARVEST SOURCE CAPACITOR (µF)
High voltage	0.22	N/A	N/A	N/A	N/A
Low voltage < 10µW	0.1	0.85	1.5	7.0	47
Low voltage > 10µW	0.1	0.85	1.5	7.0	7.0
High voltage and low voltage < 10µW	0.22	0.85	1.5	15.4	47
High voltage and low voltage > 10µW	0.22	0.85	1.5	15.4	15.4

The C1 1nF capacitor acts as a voltage-level feed forward to increase the responsiveness of the divider circuit as the harvest source capacitor is discharged. The minimum voltage is defined as:

$$V_{HARVEST-OFF} \sim= V_{HARVEST-ON} - (FB_{ON} - FB_{OFF})$$

$$V_{HARVEST-OFF} \sim= V_{HARVEST-ON} - 0.5V\ (typ)$$

where $V_{HARVEST-OFF}$ is the lowest voltage of the harvest source capacitor during boost.

Because of the divider on the FB pin, the voltage seen by the LX pin inductor is higher than the typical circuit. The inductor must be resized so that the LX pin current limits are not exceeded:

$$LX\ Inductor = V_{HARVEST-ON} \times t_{BOOST-ON}/LX_{IMAX} = V_{HARVEST-ON} \times (8.5 \times 10^{-7})$$

All other components are selected as normal.

Energy-Harvesting Design Approaches

When designing an optimal energy harvest system, there are three types of design approaches: linear harvest, boost harvest, and maximum-power-point tracking (MPPT). In harvesting applications, it is very critical to not discharge the cell when charging is failing. When the harvesting power is low enough, eventually the system discharges the cell rather than charges. This is the break-even point of the harvester. For linear harvesting, this break-even point is lower because the required quiescent current is less. However, for boost harvesting, the breakeven threshold is 1µA. While an MPPT system can utilize the harvesting source more intelligently in high-power situations, it inevitably results in higher quiescent current and a poorer break-even threshold. MPPT systems must measure the current and voltage, multiply to determine power, and make decisions to improve the power. **These required measurements automatically significantly increase the quiescent current budget by tens of µA**. Figure 4 shows energy-harvesting modes of operation vs. charge efficiency.

LDO Output Operation

The device regulates voltage from the cell to a load circuit on the REG pin through an LDO regulator. The regulator can be configured for 3.3V, 2.3V, or 1.8V operation. The LDO supports loads up to 75mA (high-current mode). For lighter load applications, a low-power mode of operation reduces the quiescent current drain on the cell. A UVLO circuit prevents the regulator from starting up or disabling the regulator when active if the cell becomes overdischarged.

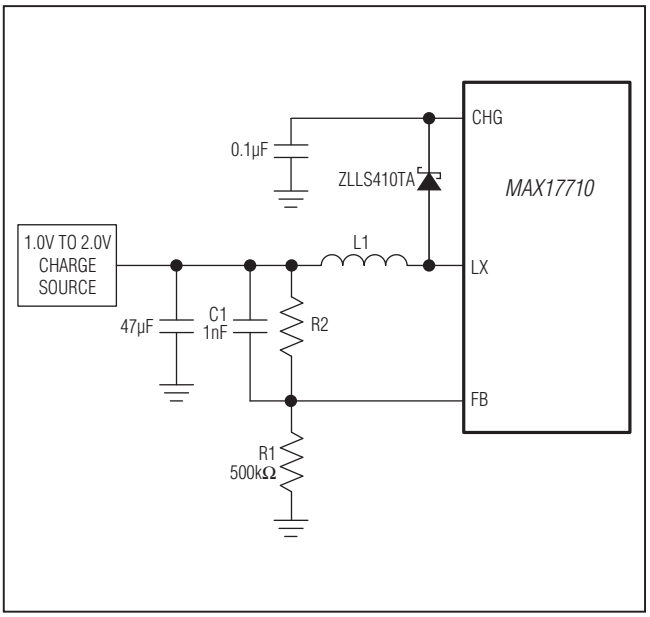


Figure 3. FB Divider Circuit to Improve Boost Efficiency for Charge Sources Between 1.0V and 2.0V

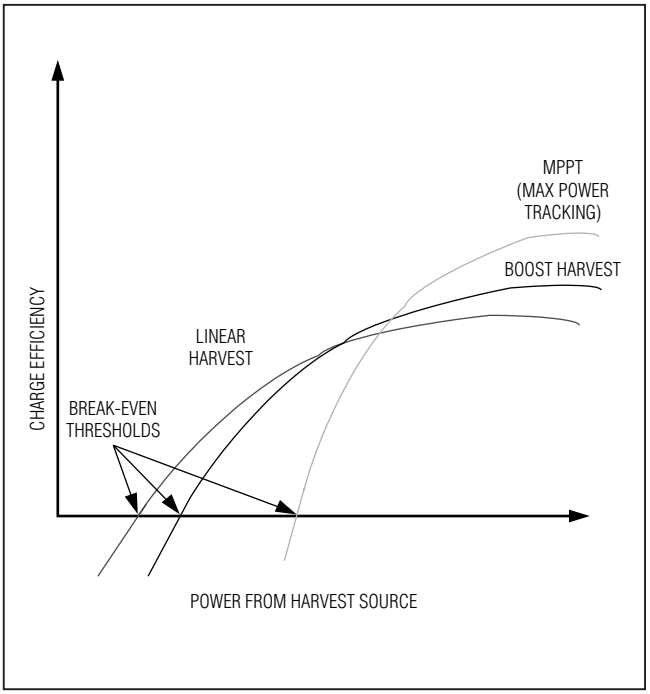


Figure 4. Energy-Harvesting Modes of Operation vs. Charge Efficiency

The LDO becomes active when the AE pin is pulsed above or held above its logic-high threshold, but the regulator output is not immediately enabled. The device first charges the external capacitor on PCKP. When the voltage level on PCKP reaches 3.7V, the regulator output is enabled in high-current mode. Powering the LDO from PCKP instead of directly from the cell allows the device to support large surge or startup inrush currents from the load that the cell would be unable to handle directly.

Once in high-current mode, the AE pin can remain logic-high or transition to an open state, and the ouput remains active. The LDO returns to shutdown only when the AE pin is driven below its logic-low threshold. Alternatively, the LDO is transitioned to low-current mode by pulsing or holding the LCE to the REG pin voltage, followed by pulsing or holding the AE pin logic-low. Note that the regulator transitions through a state where both high-current and low-current modes are active at the same time. While in low-current mode, the quiescent current drain of the cell is reduced to 150nA, while the maximum load current able to be supplied becomes 50µA. Similar to the AE pin operation, the regulator remains active if the LCE pin is open or pulled to REG, and returns to shutdown mode when LCE is driven below its logic-low threshold. Figure 5 is the regulator output state diagram.

Cell Undervoltage Lockout (UVLO)

If the cell and PCKP capacitance cannot provide sustained support for the load, then the voltage at PCKP collapses. When PCKP collapses, the system load typically stops and allows the PCKP voltage to recover, resulting in a perpetual retry in a futile attempt to support a load that cannot be supported. When PCKP fails in this way, the device shuts off the REG output to prevent futile load retries and protect the cell from overdischarge. When the REG output is latched off, the BATT quiescent current reduces to 1nA (typ). Once UVLO occurs, the regulator output remains disabled until the device detects that a charge source has been connected to the system (V_{CHG} > 4.15V). Figure 6 shows the UVLO protection modes.

Connecting any load to REG or PCKP instead of connecting directly to the cell is highly recommended. This controls the quiescent current during shutdown, enables the device to support startup during cold, and also protects the cell from overdischarge.

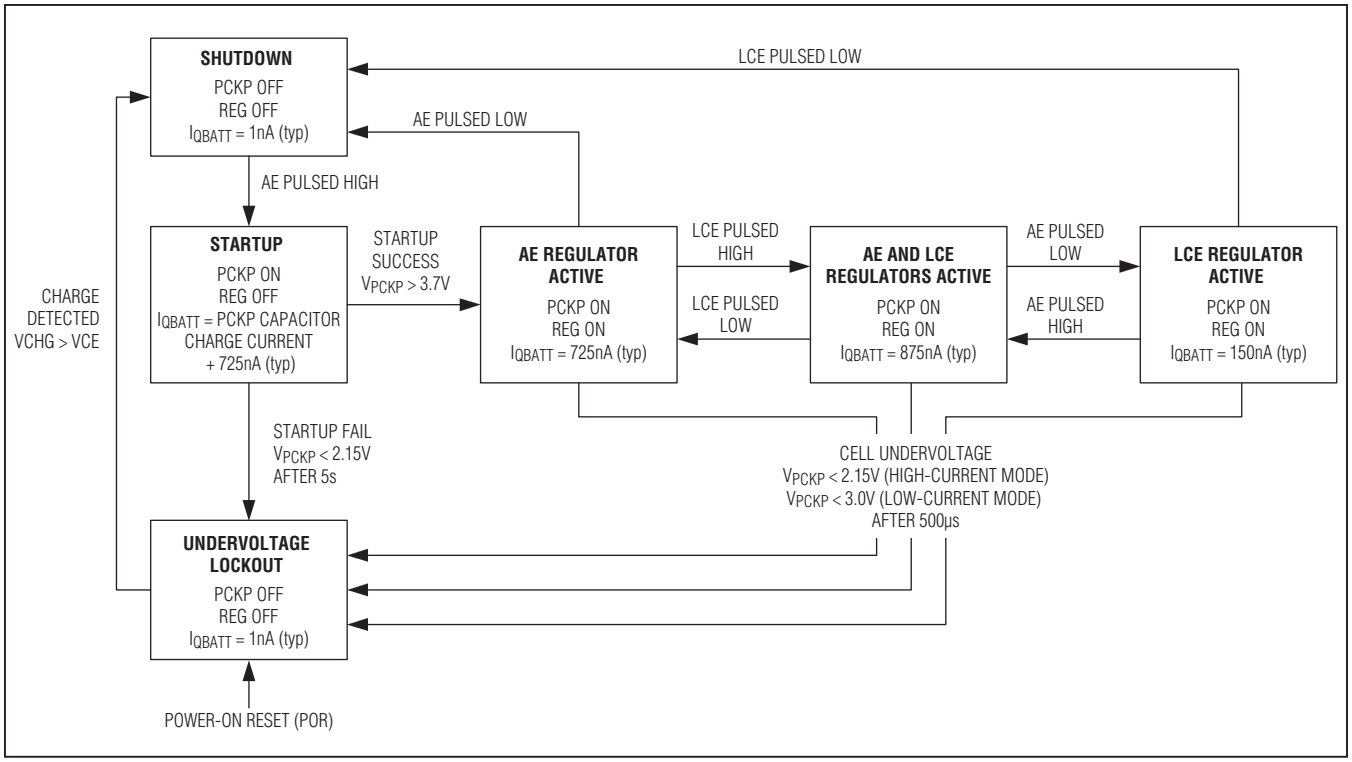
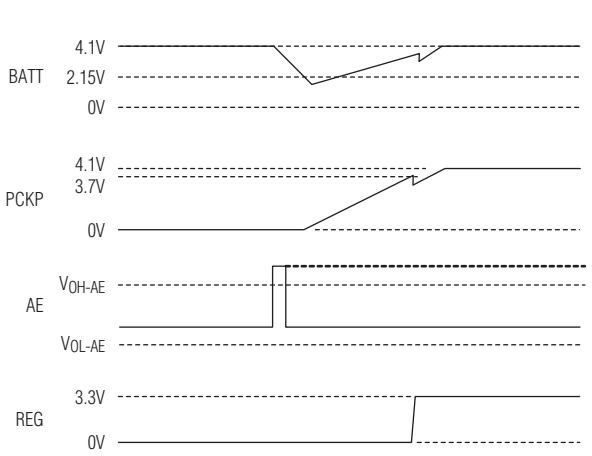
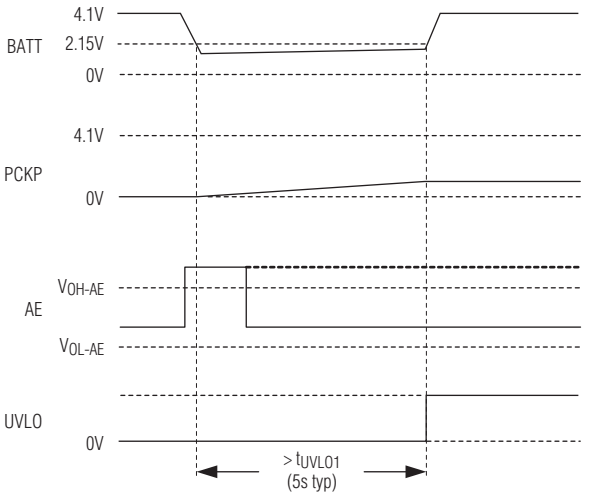


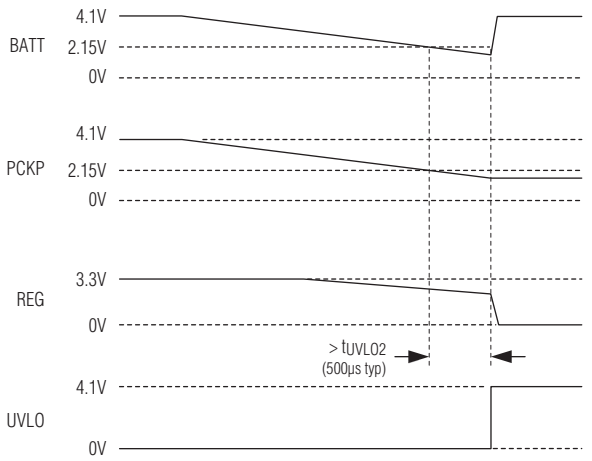
Figure 5. Regulator Output State Diagram



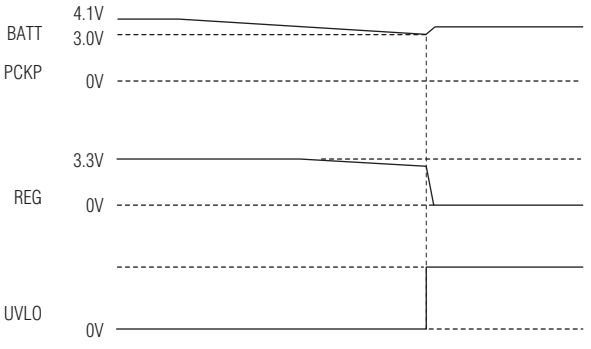
a. NORMAL REGULATOR OUTPUT ENABLE SEQUENCE



b. REGULATOR OUTPUT ENABLE FAIL DUE TO UVLO TIMEOUT



c. HIGH-CURRENT MODE REGULATOR OUTPUT DISABLED DUE TO UVLO TIMEOUT



d. LOW-CURRENT MODE REGULATOR OUTPUT DISABLED DUE TO UVLO DETECTION

Figure 6. ULVO Protection Modes

Regulator Voltage Selection

The SEL1 pin selects at which voltage REG operates. Connect SEL1 to BATT for 1.8V operation, three-state for 3.3V operation, or connect to GND for 2.3V operation. Note that the voltage regulation value is latched when enabled. To change the regulation voltage point, the regulator must be disabled and then reenabled. See Table 3.

PCKP Pin Capacitor Selection

There are several cases when the system might overload the cell, potentially causing damage. They are prevented with the PCKP load switch block and external capacitor:

- During startup, when there is an inrush current due to the application's load and capacitance.
- When the cell is cold (such as -40°C), and due to increased cell resistance, it is unable to support high-load currents.
- If the system requires a load current higher than can be supported by the cell alone.

The device provides cell undervoltage protection by limiting the current from BATT to PCKP and guaranteeing that the cell voltage does not fall below 2.15V. In addition to voltage protection, the ramp of the PCKP switch impedance is changed slowly (5ms to full on) to gradually load the cell and not collapse the voltage on a room-temperature cell. Because of these protection features, an application can now support brief high-current pulses by including a large capacitance at PCKP. This allows support for pulse loads many times higher than that naturally supported by the cell alone.

A large PCKP capacitance can be selected to support a pulse load even while the cell is very cold, and would normally be incapable of supporting a significant load. Choose this capacitor according to Table 4 or the following equation:

$$C_{PCKP} = I_{TASK} \times t_{TASK}/(3.7 - V_{MIN})$$

where:

I_{TASK} is the current required to sustain a required task, t_{TASK} is the time duration of the task, and V_{MIN} is the minimum voltage of the load doing the task.

This equation assumes that the BATT impedance is high and cannot support the load.

Table 3. Regulator Output Voltage Selection

SEL1 PIN CONNECTION	REG PIN OUTPUT VOLTAGE (V)
Connect to BATT	1.8
Open circuit	3.3
Connect to GND	2.3

Table 4. PCKP Pin Capacitor Values by Application

V_{MIN}	t_{TASK} (ms)	I_{TASK} (mA)	C_{PCKP} (µF)*
3.0	5	8	100
3.0	5	4	50
2.8	5	5	28
2.8	5	2.5	14
2.3	5	5	18
2.3	5	10	36

**Capacitance value tolerances need to be considered.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
12 UTDFN-EP	V1233N+1	21-0451	90-0339

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17710G+T*	-40°C to +85°C	12 UTDFN-EP**
MAX17710G+U*	-40°C to +85°C	12 UTDFN-EP**
MAX17710GB+	-40°C to +85°C	12 UTDFN-EP**
MAX17710GB+T	-40°C to +85°C	12 UTDFN-EP**

+Denotes a lead(Pb)-free/RoHS-compliant package.
U = Signifies tape cut.
T = Tape and reel.
**Not recommended for new designs.*
***EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/12	Initial release	—

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