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MAX17690

60V, No-Opto Isolated Flyback Controller

General Description

The MAX17690 is a peak current mode, fixed-frequency switching controller specifically designed for the isolated flyback topology operating in Discontinuous Conduction Mode (DCM). The device senses the isolated output voltage directly from the primary-side flyback waveform during the off-time of the primary switch. No auxiliary winding or optocoupler is required for output-voltage regulation.

The MAX17690 is designed to operate over a wide supply range from 4.5V to 60V. The switching frequency is programmable from 50kHz to 250kHz. A EN/UVLO pin allows the user to turn on/off the power supply precisely at the desired input voltage. The MAX17690 provides an input overvoltage protection through the OVI pin. The 7V internal LDO output of the MAX17690 makes it suitable for switching both logic-level and standard MOSFETs used in flyback converters. With 2A/4A source/sink currents, the MAX17690 is ideal for driving low $R_{DS(ON)}$ power MOSFETs with fast gate transition times. The MAX17690 provides an adjustable soft-start feature to limit the inrush current during startup.

The MAX17690 provides temperature compensation for the output diode forward voltage drop. The MAX17690 has robust hiccup-protection and thermal protection schemes, and is available in a space-saving 16-pin 3mm x 3mm TQFN package with a temperature range from -40°C to 125°C.

Benefits and Features

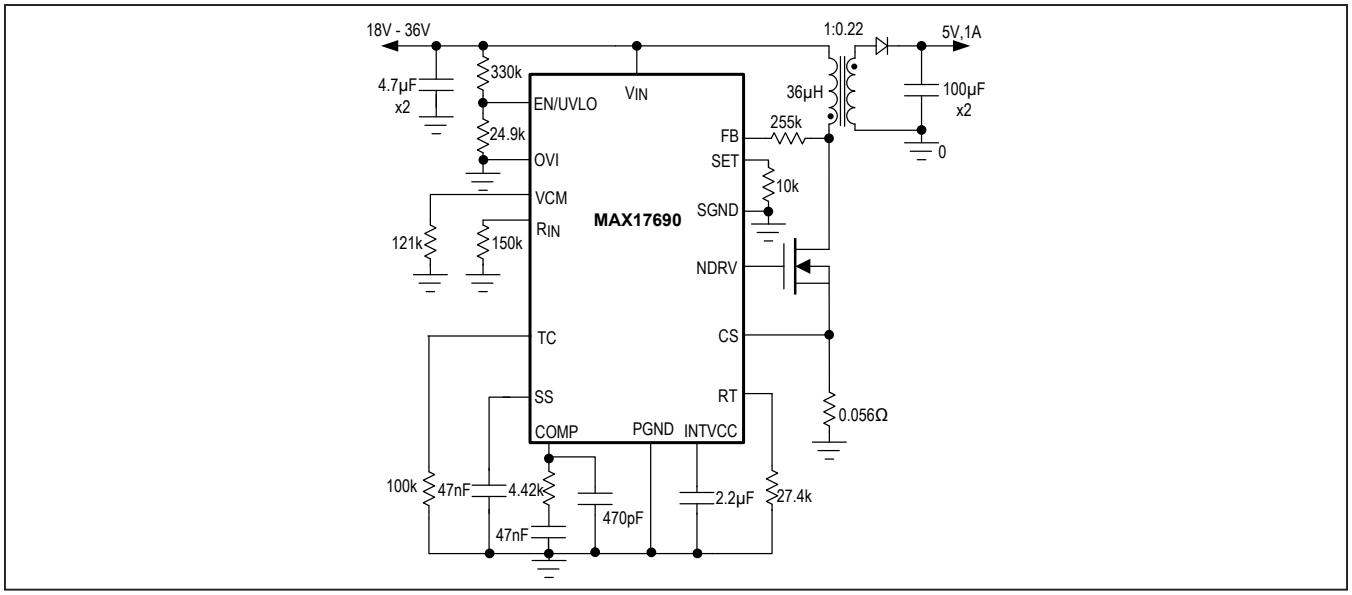
- 4.5V to 60V Input Voltage Range
- No Optocoupler or Third Winding Required to Derive Feedback Signal Across Isolation Boundary
- 2A/4A Peak Source/Sink Gate Drive Currents
- 50kHz to 250kHz Programmable Switching Frequency
- Input EN/UVLO Feature
- Input Overvoltage Protection
- Programmable Soft-Start
- Hiccup-Mode Short-Circuit Protection
- Thermal Shutdown Protection
- -40°C to 125°C Operating Temperature Range
- Space-Saving, 16-Pin 3 x 3 TQFN Package

Applications

- Isolated Flyback Converters
- Wide-Range DC-Input Isolated Power Supplies
- Industrial and Telecom Applications
- PLC I/O modules

***Ordering Information* appears at end of data sheet.**

Application Circuit



Absolute Maximum Ratings

INTVCC to SGND.....-0.3V to +16V
V_{IN}, EN/UVLO to SGND .....-0.3V to +70V
V_{IN} to FB .....-0.3V to +0.3V
OVI to SGND .....-0.3V to +6V
RIN, RT, VCM, COMP, SS,
SET, TC and CS to SGND .....-0.3V to +6V
NDRV to PGND..... -0.3V to V_{INTVCC} + 0.3V

Continuous Power Dissipation (single-layer board)
(T_A = +70°C, derate 15.6mW/°C above +70°C).....1250mW
Continuous Power Dissipation (multilayer board)
(T_A = +70°C, Derate 20.8mW/°C above +70°C)....1666.7mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 16 TQFN	
Package Code	T1633+4C
Outline Number	**21-0136**
Land Pattern Number	**90-0031**
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction to Ambient (θ_{JA})	64°C/W
Junction to Case (θ_{JC})	7°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	48°C/W
Junction to Case (θ_{JC})	7°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 24V, $V_{EN/UVLO}$ = 2V, V_{OVI} = 0V, R_{RT} = 49.9kΩ, C_{INTVCC} = 2.2µF to PGND; V_{PGND} = V_{SGND} = 0V, NDRV = SS = VCM = COMP = OPEN, CS = PGND, V_{IN} to FB = 0V, R_{SET} = 10kΩ, R_{TC} = 27.5K, R_{RIN} = 60kΩ,T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (V_{IN})						
V_{IN} Voltage Range	V_{IN}		4.5		60	V
Input Supply Shutdown Current	IIN_SH	$V_{EN/UVLO}$ = 0V (shutdown mode)		2.5	4	µA
		V_{IN} = 60V		3.5		µA
Input Switching Current	I_{SW}	No capacitor at NDRV		1.8		mA

Electrical Characteristics (continued)

(V_{IN} = 24V, $V_{EN/UVLO}$ = 2V, V_{OVI} = 0V, R_{RT} = 49.9kΩ, C_{INTVCC} = 2.2µF to PGND; V_{PGND} = V_{SGND} = 0V, NDRV = SS = VCM = COMP = OPEN, CS = PGND, V_{IN} to FB = 0V, R_{SET} = 10kΩ, R_{TC} = 27.5K, R_{RIN} = 60kΩ,T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE (EN/UVLO)						
EN/UNVO Threshold	V_{ENR}	V_{EN} rising	1.19	1.215	1.24	V
	V_{ENF}	V_{EN} falling	1.07	1.1	1.12	V
True Shutdown EN/UVLO Threshold	V_{ENSHDN}			0.7		V
EN/UVLO Input Leakage Current	I_{ENLKG}	$V_{EN/UVLO}$ = 2V, T_A = T_J = +25°C	-100		+100	nA
INTVCC LDO						
INTVCC Output Voltage Range	V_{INTVCC}	V_{IN} = 8V, 1mA ≤ I_{INTVCC} ≤ 25mA	6.65	7.0	7.35	V
		8V ≤ V_{IN} ≤ 60V, I_{INTVCC} = 1mA	6.65	7.0	7.35	V
INTVCC Current Limit	$I_{INTVCCMAX}$	V_{IN} = 8V, INTVCC = 6V	26	60		mA
INTVCC Dropout	$V_{INTVCC-DO}$	V_{IN} = 4.5V, I_{INTVCC} = 10mA	4.1			V
INTVCC ULVO	$V_{INTVCC-UVR}$	Rising	4.2	4.32	4.45	V
	$V_{INTVCC-UVF}$	Falling	3.9	4.03	4.15	V
OVI						
OVI Threshold	V_{OVIR}	V_{OVI} rising	1.19	1.215	1.24	V
	V_{OVIF}	V_{OVI} falling	1.07	1.1	1.12	V
OVI Input Leakage Current	I_{OVILKG}	V_{OVI} = 2V, T_A = T_J = +25°C	-100		+100	nA
NDRV						
RT Bias Voltage	V_{RT}			1.215		V
NDRV Switching Frequency Range	f_{SW}		50		250	kHz
NDRV Switching Frequency Accuracy			-6		+6	%
Maximum Duty Cycle			66	69	71	%
Minimum NDRV On-Time	t_{ON_MIN}			200	235	ns
Minimum NDRV Off-Time	t_{OFF_MIN}			430	490	ns
NDRV Pullup Resistance	R_{NDRV_P}	I_{NDRV} = 100mA (sourcing)		1.6	2.8	Ω
NDRV Pulldown Resistance	R_{NDRV_N}	I_{NDRV} = 100mA (sinking)		0.45	0.9	Ω
NDRV Peak Source Current	I-SOURCE			2		A
NDRV Peak Sink Current	I-SINK			4		A
NDRV Fall time	T_{NDRV_F}	C_{NDRV} = 3.3nF		11		ns
NDRV Rise Time	T_{NDRV_R}	C_{NDRV} = 3.3nF		16		ns

Electrical Characteristics (continued)

(V_{IN} = 24V, $V_{EN/UVLO}$ = 2V, V_{OVI} = 0V, R_{RT} = 49.9kΩ, C_{INTVCC} = 2.2µF to PGND; V_{PGND} = V_{SGND} = 0V, NDRV = SS = VCM = COMP = OPEN, CS = PGND, V_{IN} to FB = 0V, R_{SET} = 10kΩ, R_{TC} = 27.5K, R_{RIN} = 60kΩ,T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 1)

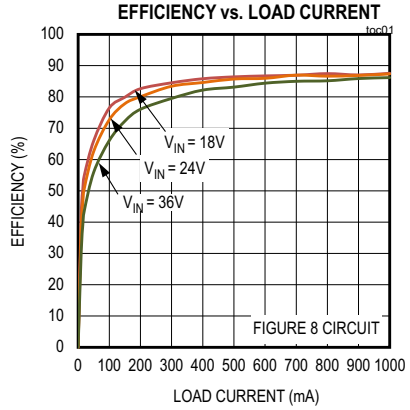
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SOFT-START (SS)						
Soft-Start Charging current	I_{SS}	V_{SS} = 1V	4.75	5	5.25	µA
Soft-Start Done Threshold		V_{SS} rising		0.98		V
CURRENT SENSE (CS)						
Maximum CS Current-Limit Threshold	V_{CS_MAX}	V_{SET} = 0.8V	90	100	110	mv
Minimum CS Current-Limit Threshold	V_{CS_MIN}	V_{SET} = 1.2V		20		mv
CS Input Bias Current	I_{CS}	V_{CS} = 0V	7.5	10	13.5	µA
Runaway Current-Limit Threshold	$V_{CS\_RUNAWAY}$		108	120	132	mV
Overcurrent Hiccup Timeout		V_{SET} < 0.7V		16,384		cycles
SET						
SET Regulation Voltage	V_{SET}		0.988	1	1.012	V
SET Undervoltage Trip Level to Cause Hiccup	V_{SET_HICF}			0.7		V
TC						
TC Pin Bias Voltage	V_{TC}	T_A = T_J = +25°C		0.55		V
TC Current	I_{TC}	R_{TC} = 27.5kΩ		20		µA
COMP						
Error Amplifier Transconductance	Gm			1.6		mS
COMP Source Current	I_{COMP_SOURCE}	V_{COMP} = 2V and V_{SET} = 0.8V	95	136	190	µA
COMP Sink Current	I_{COMP_SINK}	V_{COMP} = 2V and V_{SET} = 1.2V	95	136	190	µA
MAX COMP Voltage	V_{COMPH}	R_{SET} = 8kΩ		2.9		V
MIN COMP Voltage	V_{COMPL}	R_{SET} = 12kΩ		1.55		V
COMP-to-CS Gain	ACS-PWM	$\Delta V_{COMP}/\Delta V_{CS}$	10.0	10.3	10.7	V/V
VCM						
VCM Pullup Current		VCM = PGND	9.4	10	10.6	µA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	T_{SHDNR}	Temperature rising		+160		°C
Thermal-Shutdown Hysteresis	T_{SHDNHY}			+20		°C

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the temperature range and relevant supply voltage range are guaranteed by design and characterization.

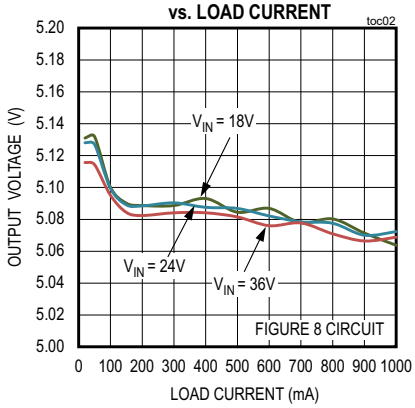
Typical Operating Characteristics

(V_{IN} = 24V, $V_{EN/UVLO}$ = +2V, V_{OVI} = SGND, C_{VIN} = 1uF, C_{INTVCC} = 2.2µF, T_A = +25°C, unless otherwise noted.)

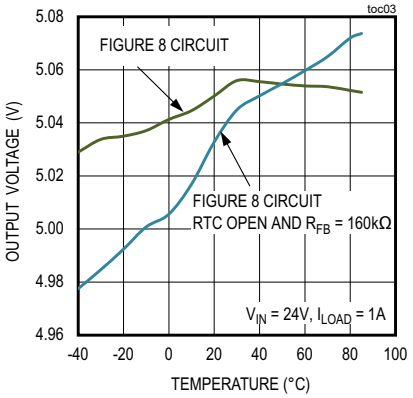
EFFICIENCY vs. LOAD CURRENT



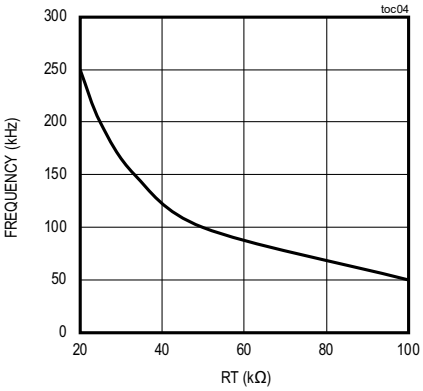
OUTPUT VOLTAGE vs. LOAD CURRENT



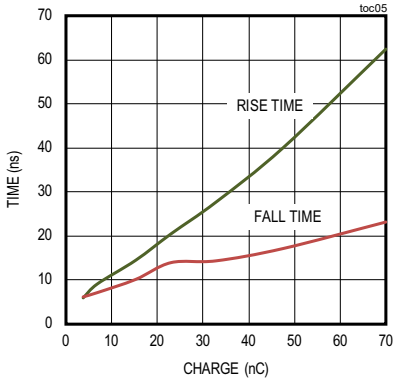
OUTPUT VOLTAGE vs. TEMPERATURE



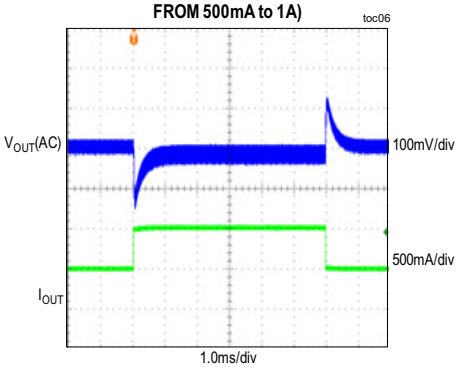
SWITCHING FREQUENCY vs. RT



NDRV CHARGE vs. NDRV RISE/FALL TIME



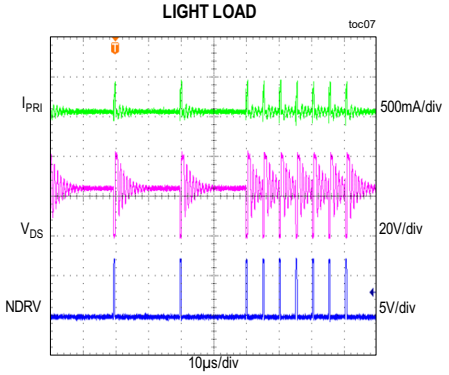
LOAD TRANSIENT RESPONSE, (LOAD CURRENT STEPPED FROM 500mA to 1A)



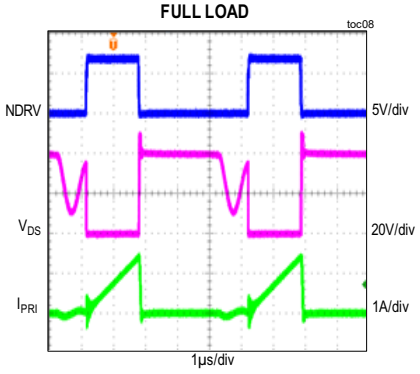
Typical Operating Characteristics (continued)

(V_{IN} = 24V, $V_{EN/UVLO}$ = +2V, V_{OVI} = SGND, C_{VIN} = 1uF, C_{INTVCC} = 2.2µF, T_A = +25°C, unless otherwise noted.)

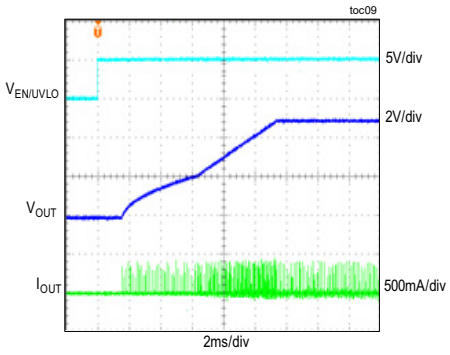
STEADY-STATE WAVEFORMS LIGHT LOAD



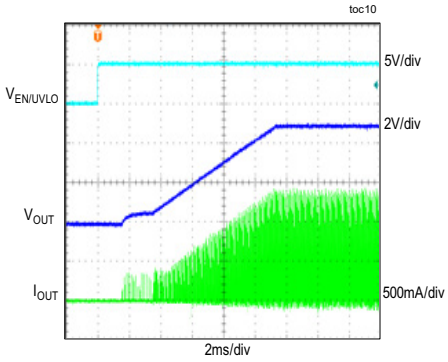
STEADY-STATE WAVEFORMS FULL LOAD



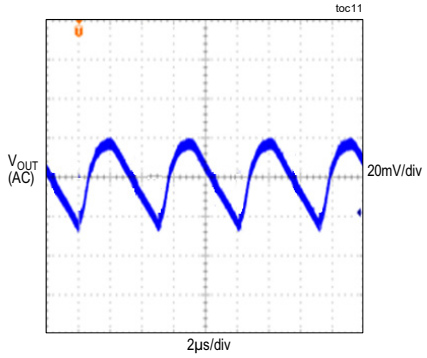
SOFT-START, LIGHT LOAD



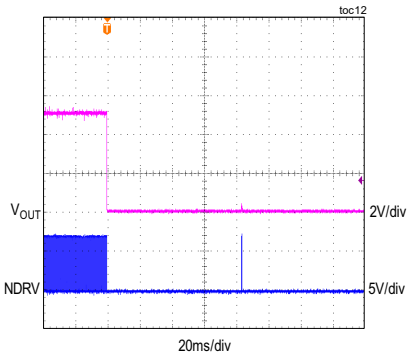
SOFT-START, FULL LOAD



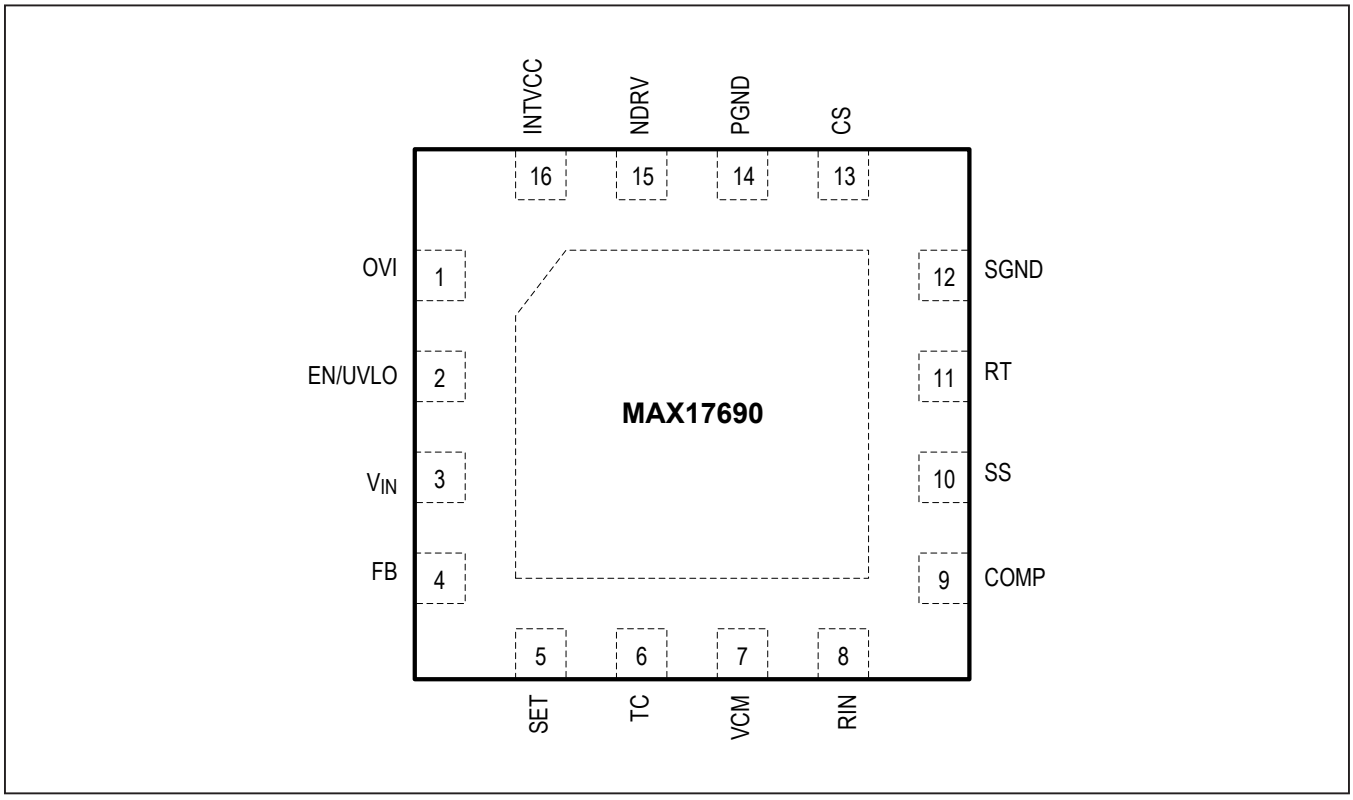
OUTPUT-VOLTAGE RIPPLE FULL LOAD



OVERLOAD PROTECTION



Pin Configuration



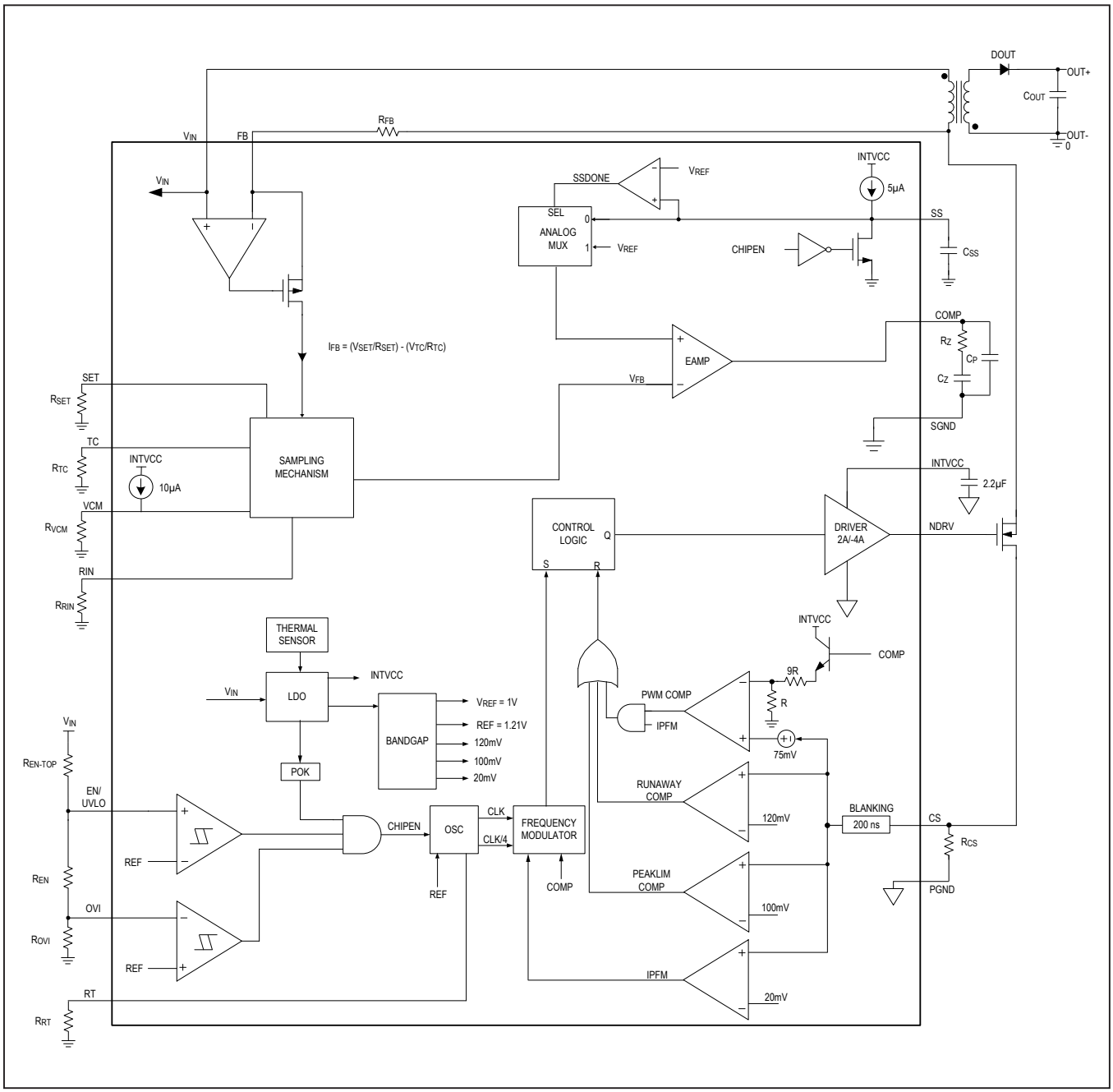
Pin Description

PIN	NAME	FUNCTION
1	OVI	Input Overvoltage Detection. Connect a resistive-divider between the input supply, OVI, and SGND to set the input overvoltage threshold. The MAX17690 stops switching when the voltage at the OVI pin exceeds 1.215V and resumes switching when the voltage at the OVI pin falls below 1.1V.
2	EN/UVLO	Enable/Undervoltage Lockout Pin. Connect a resistive-divider between the input supply, EN/UVLO, and SGND to set the input turn-on threshold. The MAX17690 starts switching when the voltage at the EN/UVLO pin exceeds 1.215V and stops switching when the voltage at the EN/UVLO pin falls below 1.1V.
3	V_{IN}	Input Supply Voltage. The input supply voltage range is 4.5V to 60V. This pin acts as a reference pin for the feedback circuitry connected to the FB pin. Connect a minimum of 1µF ceramic capacitor between the V_{IN} pin and SGND.
4	FB	Feedback input for sensing the reflected output voltage during Flyback period. See the *Selection of R_{IN}, R_{FB}, and R_{SET} Resistor* section for selecting an appropiate R_{FB} resistor.
5	SET	Input for the External Ground-Referred Reference Resistor. Connect a 10kΩ resistor from the SET pin to SGND and place as close as possible to the MAX17690 IC.

Pin Description (continued)

PIN	NAME	FUNCTION
6	TC	Output Voltage Temperature Compensation. Connect the resistor R_{TC} from the TC pin to SGND to set the temperature compensation. Current through TC pin is given by $0.55/R_{TC}$.
7	VCM	Common-Mode Voltage Selector for Internal Zero Current Detector Block. Connect a resistor R_{VCM} from the VCM pin to SGND. See the *Selection of R_{VCM} Resistor* section for selecting an appropriate R_{VCM} resistor.
8	RIN	A current proportional to V_{IN} flows through RIN resistor. Connect a resistor R_{RIN} from the RIN pin to SGND.
9	COMP	Error Amplifier Output. Connect the frequency compensation network between COMP and SGND.
10	SS	Soft-Start. Connect a capacitor C_{SS} from the SS pin to SGND to program the soft-start time interval. Pullup current at this pin is 5µA.
11	RT	Switching Frequency Programming Resistor. Connect a resistor R_{RT} from RT to SGND to set the PWM switching frequency. This pin is regulated to 1.215V. See the *Switching Frequency* section for selecting an appropriate R_{RT} resistor.
12	SGND	Signal Ground.
13	CS	Current Sense Input. See the *Setting Peak Current Limit* section for selecting an R_{CS} resistor.
14	PGND	Power Ground.
15	NDRV	Driver Output. Connect this pin to the external MOSFET gate. Switches between INTVCC to PGND.
16	INTVCC	Linear Regulator Output and Driver Input. Connect a minimum of 2.2µF bypass capacitor from INTVCC pin to PGND as close as possible to the MAX17690 IC. This pin is typically regulated to 7V.
	EP	Exposed Pad. Connect this pin to the signal ground plane.

Functional Diagram



Detailed Description

For low and medium-power applications, the flyback converter is the preferred choice due to its simplicity and low cost. However, in isolated applications, the use of optocoupler or auxiliary winding for voltage feedback across the isolation boundary increases the number of components, and design complexity. The MAX17690 eliminates the optocoupler or auxiliary winding, and achieves ±5% output voltage regulation over line, load, and temperature variations.

The MAX17690 implements an innovative algorithm to sample and regulate the output voltage by primary-side sensing. During the flyback period, the reflected voltage across the primary winding is the sum of output voltage, diode forward voltage and the drop across transformer parasitic elements, multiplied by the primary-secondary turns ratio. By sampling and regulating this reflected voltage close to the secondary zero current, the algorithm minimizes the effect of transformer parasitics and the diode forward voltage on the output voltage regulation.

Theory of No-Opto Flyback Operation

The MAX17690 senses the drain-node of the primary nMOSFET (Q1) while the secondary diode (D) is conducting (see Figure 1). During this sensing period, the drain-node voltage is the sum of the input voltage and reflected secondary winding voltage. Using an internal differential amplifier, the MAX17690 generates a current (I_{RFB}) in the feedback resistor (R_{FB}), which is proportional to the secondary winding voltage. This current through the R_{FB} resistor also flows through the R_{SET} resistor placed between SET and SGND and produces a ground referenced voltage on the SET pin.

The MAX17690 uses a built-in algorithm to sample the SET pin voltage when the secondary winding current is close to zero; hence, the resistive drops in the voltage across the secondary winding can be neglected. The sampled voltage on the SET pin is proportional to the sum of the output voltage and secondary diode forward voltage drop. This sampled voltage feeds the inverting input of the internal error amplifier, whereas the internal reference voltage feeds the non-inverting input of the error amplifier. The control loop regulates the sampled SET pin voltage to the internal reference voltage. The above description applies to a case where the TC pin is left unconnected (for applications where no temperature compensation is needed). The above operation can be expressed as:

$$\frac{(V_{OUT} + V_D)}{K} \times \frac{1}{R_{FB}} \times R_{SET} = V_{SET}$$

where,
V_{OUT} = Output voltage
V_D = Output diode forward voltage drop
K = Transformer secondary-to-primary turns ratio (N_S / N_P)
V_{SET} = SET pin regulation voltage (1V)

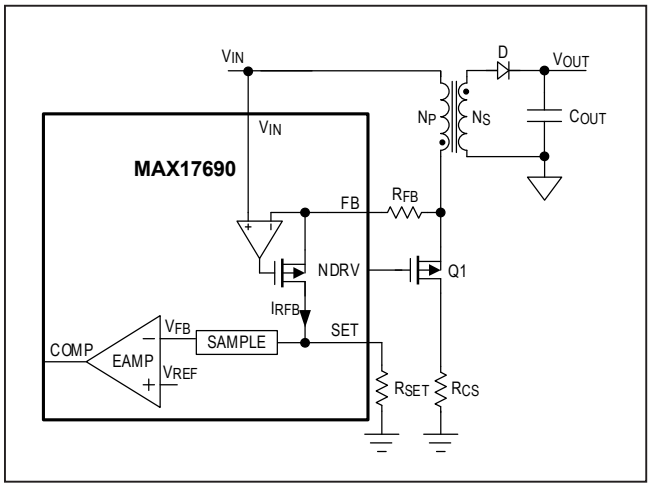


Figure 1. Simplified Diagram of No-Opto Flyback Operation

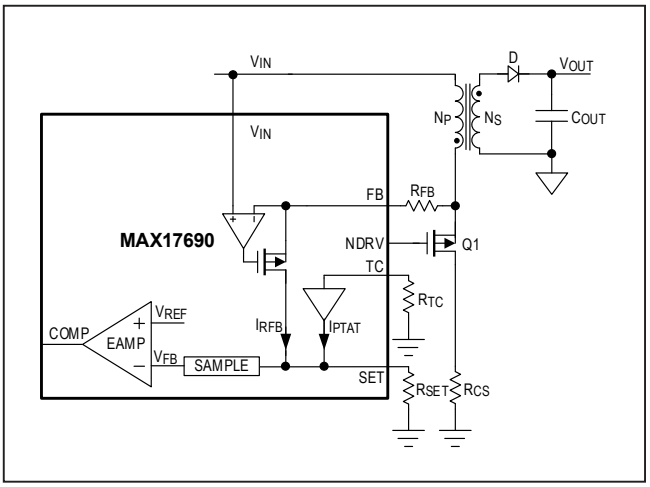


Figure 2. Simplified Diagram of No-Opto Flyback with Temperature Compensation

The output diode forward voltage (V_D) in the reflected secondary winding voltage has a significant negative temperature coefficient (–1mV/°C to –2mV/°C), which produces approximately 2% to 5% variation on the output voltage across temperature in low output voltage applications, such as 3.3V and 5V. The MAX17690 compensates for the temperature variations of the diode forward voltage (V_D) by adding a proportional-to-absolute-temperature (P_{TAT}) current (I_{PTAT}) on to the SET pin as shown in Figure 2. The I_{PTAT} current, V_{TC} / R_{TC} is programmable using a resistor R_{TC} connected between the TC pin and SGND. The TC pin voltage, V_{TC} is regulated at 0.55V at room temperature and has a +1.85mV/°C positive temperature coefficient. This compensation scheme assumes that the output diode temperature change tracks the MAX17690 temperature.

$$\left[\frac{(V_{OUT}+V_D)}{K}\times\frac{1}{R_{FB}}+\frac{V_{TC}}{R_{TC}}\right]\times R_{SET}=V_{SET}$$

By differentiating the above equation for temperature change,

$$\frac{\frac{\delta V_D}{\delta T}}{K}\times\frac{1}{R_{FB}}=-\left(\frac{\delta V_{TC}}{\delta T}\times\frac{1}{R_{TC}}\right)$$

where,

V_{TC} = TC pin bias voltage, 0.55V at room temperature

$\frac{\delta V_D}{\delta T}$ = Temperature coefficient of the secondary rectifier diode in mV/°C, which can be obtained from the diode data sheet

$\frac{\delta V_{TC}}{\delta T}$ = Temperature coefficient of the internal V_{TC}, +1.85mV/°C

Supply Voltage

The IC supports a wide operating input voltage range from 4.5V to 60V. The MAX17690 regulates the FB pin to the voltage sensed on the V_{IN} pin during the flyback period, thus resulting in a current in R_{FB} that is proportional to the reflected voltage on the primary winding. This current is used by the MAX17690 as a feedback signal for output voltage regulation. Therefore, the V_{IN} pin should be directly connected to the input supply with a minimum of 1µF ceramic capacitor between V_{IN} pin and SGND, placed as close to the IC as possible for robust operation.

EN/UVLO and OVI

This device's EN/UVLO pin serves as an enable/disable input, as well as an accurate programmable input UVLO pin. The MAX17690 do not commence startup operation until the EN/UVLO pin voltage exceeds 1.215V (typ). The MAX17690 turns-off if the EN/UVLO pin voltage falls below 1.1V (typ). A resistor-divider from V_{IN} to SGND can be used to divide and apply a fraction of the input voltage (V_{IN}) to the EN/UVLO pin. The values of the resistor-divider can be selected so that the EN/UVLO pin voltage exceeds the 1.215V (typ) turn-on threshold at the desired input bus voltage. The same resistor-divider can be modified with an additional resistor (R_{OVI}) to implement input overvoltage protection in addition to the EN/UVLO functionality, as shown in Figure 3. When the voltage at the OVI pin exceeds 1.215V (typ), the device stops switching. The device resumes switching operations only if the voltage at the OVI pin falls below 1.1V (typ). For given values of startup input voltage (V_{START}) and input overvoltage-protection voltage (V_{OVI}), the resistor values for the divider can be calculated as follows, assuming a 10kΩ resistor for R_{OVI}:

$$R_{EN}=R_{OVI}\times\left[\frac{V_{OVI}}{V_{START}}-1\right]$$

Where R_{OVI} is in kΩ, while V_{START} and V_{OVI} are in volts

$$R_{EN-TOP}=\left[R_{OVI}+R_{EN}\right]\times\left[\frac{V_{START}}{1.215}-1\right]$$

Where R_{EN} , R_{OVI} is in kΩ, while V_{START} is in volts.

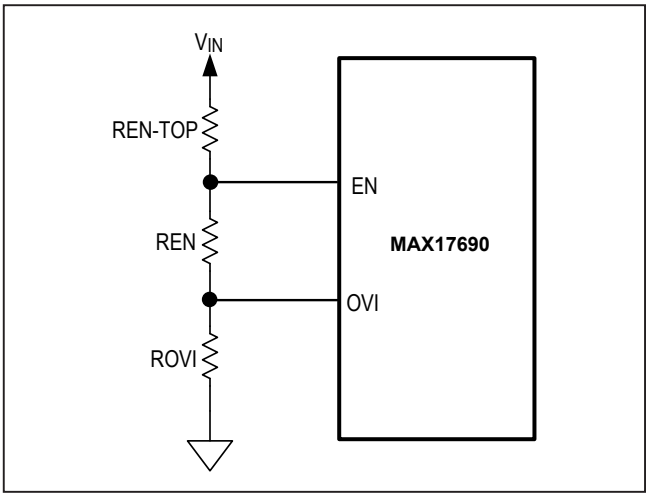


Figure 3. Programming EN/UVLO and OVI

INTVCC

The V_{IN} powers internal LDO of the MAX17690. The regulated output of the LDO is connected to the INTVCC pin. The LDO output voltage is 7V (typ). Connect a 2.2µF (min) ceramic capacitor between the INTVCC and PGND pins for the stable operation over the full temperature range. Place this capacitor as close as close possible to the IC. Although there is no need for an auxiliary winding for the voltage feedback, for high input-voltage applications, an additional winding used to overdrive the INTVCC may improve overall system efficiency. Also, to avoid internal LDO body diode conduction, the auxiliary-winding voltage should be less than the input-supply voltage during the entire operation. The auxiliary winding should be designed to output a voltage between 8V and 16V to ensure that the internal LDO turns off and the IC is supplied from the auxiliary winding output. The typical circuit for overdriving the INTVCC is shown in Figure 4.

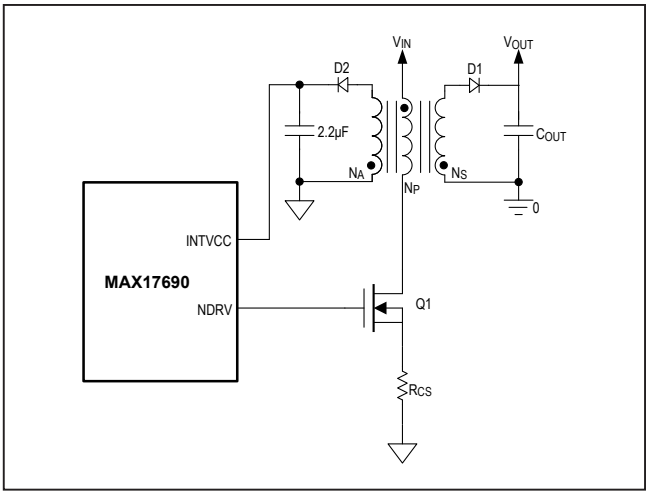


Figure 4. INTVCC Pin Configuration.

Programming Soft-start time

The capacitor connected between the SS pin to SGND programs the soft-start time. Internally generated 5µA of precise current source charges the soft-start capacitor. When the EN/UVLO voltage is above 1.215V (typ), the device initiates a soft-start sequence. During the soft-start time, the SS pin voltage is used as a reference for the internal error amplifier. The soft-start feature reduces the input inrush current during startup. The reference ramp-up allows the output voltage to increase monotonically from zero to the target output value.

$$C_{SS} = 5 \times t_{SS}$$

where,

C_{SS} = Soft-start capacitor in nF

t_{SS} = Soft-start time in ms

Switching Frequency

The MAX17690 switching frequency is programmable between 50kHz and 250kHz with a resistor R_{RT} connected between RT and SGND. Based on the sampling algorithm requirements, for the given minimum and maximum input voltage the maximum switching frequency is determined by,

$$f_{SW} \le \left(\frac{720000 \times D_{MAX} \times V_{IN\ MIN}}{V_{IN\ MAX}} \right) \text{ where}$$

$$D_{MAX} = \left(\frac{V_{IN\ MAX}}{V_{IN\ MAX} + (2 \times V_{IN\ MIN})} \right)$$

where,

$V_{IN\ MIN}$ = Minimum Input Voltage in Volts at which the part reaches D_{MAX}. Based on design requirements, either minimum operating input voltage or part startup voltage (V_{START}) set by the EN/UVLO divider can be selected as $V_{IN\ MIN}$.

$V_{IN\ MAX}$ = Maximum Input Voltage in Volts

f_{SW} = Switching frequency in Hz.

D_{MAX} = Maximum operating duty cycle. If the calculated D_{MAX} is > 0.65, then choose D_{MAX} = 0.65

Use the following formula to determine the appropriate value of R_{RT} to program the selected f_{SW}, D_{MAX}

$$R_{RT} = \frac{5 \times 10^6}{f_{SW}}$$

where,

R_{RT} = Resistor value in kohm

f_{SW} = Switching frequency in Hz

Selection of R_{IN}, R_{FB}, R_{SET} and R_{TC} Resistors:

Connect a fixed 10kΩ resistor (R_{SET} = 10kΩ) between the SET pin and SGND for proper MAX17690 operation. The equations given in the *Theory of No-Opto Flyback Operation* section can be rearranged to arrive at the equations for R_{FB} and R_{TC} to program the output voltage and temperature compensation.

For applications that do not require temperature compensation, the TC pin is left unconnected and the R_{FB} resistor is calculated using below equation.

$$R_{FB} = \frac{R_{SET}}{V_{SET}} \times \frac{(V_{OUT} + V_D)}{K}$$

For applications that require temperature compensation, use below equations to calculate R_{FB} and R_{TC} values.

$$R_{FB} = \frac{R_{SET}}{V_{SET}} \times \frac{1}{K} \times \left[(V_{OUT} + V_D) - \frac{V_{TC} \times \left(\frac{\delta V_D}{\delta T} \right)}{\frac{\delta V_{TC}}{\delta T}} \right]$$

$$R_{TC} = -K \times R_{FB} \times \frac{\left(\frac{\delta V_{TC}}{\delta T} \right)}{\left(\frac{\delta V_D}{\delta T} \right)}$$

For both with and without temperature compensation cases, R_{IN} is calculated using the equation given below:

$$R_{IN} = 0.6 \times R_{FB}$$

In practice, due to the drop across the secondary leakage inductance of the transformer and the error caused by the difference between the actual V_D and the V_D used to calculate the R_{FB}, the measured output voltage may deviate from the target output voltage. Use below equations to readjust the output voltage to the desired value,

$$R_{FB(NEW)} = \frac{V_{0(TARGET)}}{V_{0(MEASURED)}} \times R_{FB}$$

$$R_{RIN(NEW)} = 0.6 \times R_{FB(NEW)}$$

Selection of R_{VCM} Resistor

The device generates an internal voltage proportional to the on-time Volt-seconds, to determine the correct sampling instant for the reflected output voltage on primary winding during the off-time. The R_{VCM} resistor is used to scale this internal voltage to the acceptable internal voltage limits. Follow the steps below to select the R_{VCM} resistor,

Table 1. R_{VCM} Resistor Selection

S.NO	K_C	R_{VCM} (Ω)
1	640	0
2	320	75k
3	160	121k
4	80	220k
5	40	Open

1) Using the below formula, calculate the scaling constant (K_C)

$$K_C = \frac{100\mu \times (1 - D_{MAX})}{\left(f_{SW} \times 3 \times 10^{-12} \right)}$$

where f_{SW} is in Hz.

2) From Table 1, choose the row that has the equal or higher value for K_C with regard to the calculated K_C in step 1. Select the R_{VCM} resistor value from the corresponding row.

For example, if the calculated K_C is 100 then choose the row with K_C equal to 160. Select the corresponding 121kΩ for the R_{VCM} value.

Short-Circuit Protection/Hiccup

The device offers a hiccup scheme that protects and reduces power dissipation in the design under output short-circuit conditions. One occurrence of the runaway current limit or output voltage less than 70% of regulated voltage would trigger a hiccup mode that protects the converter by immediately suspending the switching for the period of 16,384 clock cycles. The runaway current limit is set at a $V_{CS-RUNAWAY}$ of 120mV (typ).

Applications Information

Transformer Selection

Since the DCM is the recommended mode of operation for the MAX17690 based flyback converter, use the below equation to determine the appropriate value for the L_{MAG},

$$L_{MAG} = \frac{0.5 \times \eta \times \left(V_{IN\ MIN} \times D_{MAX}\right)^2}{V_{OUT} \times I_{OUT} \times f_{SW}}$$

where,

V_{OUT} = Desired output voltage in Volts

I_{OUT} = Desired output current in Amps

L_{MAG} = Transformer magnetizing inductance in Henry

D_{MAX} = Maximum duty cycle, use the value calculated in Switching frequency section

η = converter target efficiency assumed to be in the range of 0.8 to 0.9

f_{SW} = Switching frequency in Hz, select the frequency equal to or less than the value calculated for the f_{SW} in the switching frequency section.

For the selected L_{MAG} and the f_{SW}, recalculate the operating duty cycle using the below formula

$$D = \frac{1}{V_{IN\ MIN}} \times \sqrt{\frac{2 \times L_{MAG} \times V_{OUT} \times I_{OUT} \times f_{SW}}{\eta}}$$

The following equation is used to determine the value of K,

$$K = \frac{N_S}{N_P} = \frac{0.8 \times \left(V_{OUT} + V_D\right) \times \left(1 - D\right)}{V_{IN\ MIN} \times D}$$

The above selection of L_{MAG} and K allows for a ±10% tolerance in L_{MAG} that most manufacturers can support while ensuring DCM operation at the full load (V_{OUT} x I_{OUT}) of the converter, down to minimum operating input voltage. With this L_{MAG}, the converter enters continuous conduction mode (CCM) when delivering an output power greater than the full-load power (V_{OUT} x I_{OUT}). As the load power is further increased, the converter continues to regulate the average output voltage before hitting primary peak current limit. When the primary peak current limit is reached, the energy delivered to the secondary is limited, causing V_{OUT} to fall for increasing load current. When V_{OUT} falls to a value that results in the sampled voltage at SET being less the 70% of the nominal, the MAX17690 enters Hiccup mode operation.

When the part is operating in CCM, the output regulation degrades marginally due to errors caused by the secondary diode forward drop and transformer secondary DC-resistance drop in the primary-side sensing algorithm.

When delivering full-load power, the different nominal currents in the transformer can be calculated using the equations given below.

The peak current in the transformer primary winding,

$$I_{LIM} = \sqrt{\frac{2 \times V_{OUT} \times I_{OUT}}{\eta \times L_{MAG} \times f_{SW}}}$$

The RMS current in the transformer primary winding,

$$I_{PRI\ RMS} = I_{LIM} \times \sqrt{\frac{L_{MAG} \times I_{LIM} \times f_{SW}}{3 \times V_{IN\ MIN}}}$$

The RMS current in the transformer secondary winding,

$$I_{SEC\ RMS} = \frac{I_{LIM}}{K} \times \sqrt{\frac{L_{MAG} \times I_{LIM} \times f_{SW} \times K}{3 \times \left(V_{OUT} + V_D\right)}}$$

A current sense resistor, connected between the nMOSFET source and PGND, sets the peak current limit of the part. Use the following equation to calculate the value of R_{CS} to deliver full-load power without hitting peak current limit of the part,

$$R_{CS} = \frac{0.08}{I_{LIM}}$$

The transformer primary saturation current should be greater than or equal to 1.1 x I_{LIM}. This recommendation corresponds to about 88mV of peak current limit voltage across R_{CS} and ensures that the transformer can reliably deliver full-load power across all operating conditions for variation of ±10% in L_{MAG}. Although the MAX17690 peak current-limit voltage tolerance can be up to 110mV, it is not necessary to design the transformer to be compatible with this maximum peak current limit specification since the runaway current limit feature of the MAX17690 protects the design if the transformer should saturate above 88mV. This allows the transformer size to be optimized to match the required full-load power.

To achieve ±5% voltage regulation over line, load and temperature, the leakage inductance should be limited to 1.5% to 2% of the transformer magnetizing inductance. and the transformer turns-ratio (K) tolerance should be specified as ±1%. Refer Table 2 for the list of standard transformers developed for different applications using the MAX17690.

For the stable operation, the recommended minimum on-time ($t_{ON\ MIN}$) and the minimum off-time ($t_{OFF\ MIN}$) are 230ns(max) and 490ns(max) respectively. Use the below equations to check these values for the selected transformer magnetizing inductance, turns ratio and current sense resistor.

$$t_{ON\ MIN} = \frac{L_{MAG} \times 0.02}{R_{CS} \times V_{IN\ MAX}} \geq 230n$$

$$t_{OFF\ MIN} = \frac{K \times L_{MAG} \times 0.02}{R_{CS} \times V_{OUT}} \geq 490n$$

If the above conditions are not met, reduce the f_{SW} and recalculate the L_{MAG}, K and R_{CS}. Repeat this step till the conditions given above for the $t_{ON\ MIN}$ and the $t_{OFF\ MIN}$ are satisfied.

Minimum Load Requirement

The MAX17690 samples the reflected output voltage information on the primary winding during the time when the primary NMOSFET is turned-off, and energy stored during the on-time is being delivered to the secondary. It is therefore mandatory for the MAX17690 to switch the external NMOSFET to sample the reflected output voltage. A minimum packet of energy needs to be delivered to the output even during light load conditions, in order to sample and regulate the output voltage. This minimum deliverable energy creates a minimum load requirement on the output that depends on the minimum peak primary current. For a discontinuous Flyback converter, the load power P_O is proportional to the square of the primary peak current(I_{pk_pry}).

$$P_O = 0.5 \times L_{MAG} \times I^2pk\_pry \times f_{SW} \times \eta$$

The minimum peak primary current directly depends on the selection of R_{CS} value, since the minimum

MAX17690 primary peak current cannot go lower than

$$\frac{V_{CS\_MIN}}{R_{CS}} \quad \text{where } V_{CS\_MIN} = 20mV(typ).$$

At low output power levels that demand energy less than that corresponding to the minimum primary current, the MAX17690 modulates the switching frequency between $f_{SW}/4$ and f_{SW} to adjust the energy delivered to the correct level required to regulate the output voltage. As the load current is lowered further, the MAX17690 spends more and more switching cycles at $f_{SW}/4$, until the device completely settles down at $f_{SW}/4$. At this point the MAX17690 has reached its minimum load condition, and cannot regulate the output voltage without this minimum load connected to the output. This small minimum load can easily be provided on the output by connecting a fixed resistor. In the absence of a minimum load, or a load less than the “minimum load” the output voltage will rise to higher values. To protect for this condition, a Zener diode of appropriate breakdown voltage rating may be installed on the output. Care should be taken to ensure that the Zener breakdown voltage is outside the output voltage envelope in both steady state and transient conditions.

Given that maximum load power corresponds to a V_{CS_MAX} = 100 mV, and noting that the deliverable load current is proportional to the square of the primary peak current in a discontinuous mode Flyback converter, V_{CS_MIN} = 20mV corresponds to a 4% of full load at 100% efficiency, and switching frequency of f_{SW}. Since the MAX17690 can drop its switching frequency to $f_{SW}/4$, the minimum load requirement reduces further to 1%. In practice, the efficiency is less than 100%, resulting in a minimum load requirement of less than 1%.

Table 2. Predesigned Transformers—Typical Specifications Unless Otherwise Noted

TRANSFORMER PART NUMBER	SIZE (W x L x H) (mm)	L_{PRI} (µH)	L_{LEAK} (nH)	NPS (NP:NS)	I_{SAT} (A)	R_{PRI} (mΩ)	R_{SEC} (mΩ)	MANUFACTURER	TARGET APPLICATION	
									INPUT (V)	OUTPUT
750343444	13.34 x 15.24 x 11.43	36	900	4.5:1	1.6	80	8	Wurth Elektronik	18-36	5V/1A
750343182	13.46 x 17.75 x 12.7	33	500	1:1	2.2	46	129	Wurth Elektronik	18-36	+15V/200mA -15V/200mA

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input bus caused by the converter switching. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equations to limit the ripple voltage amplitude ΔV_{IN} to less than 5% of the input voltage when operating at nominal input voltage,

$$C_{IN} \geq \frac{I_{LIM} \times D \times \left(1 - \frac{D}{2}\right)^2}{2 \times f_{SW} \times \Delta V_{IN}}$$

where,

C_{IN} = Input capacitance in Farads.

D = Operating duty cycle.

ΔV_{IN} = Target value of input voltage ripple in Volts.

In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Output Capacitor Selection

X7R ceramic output capacitors are preferred in industrial applications due to their stability over temperature. It should be noted that dielectric materials used in ceramic capacitors exhibit reduction of capacitance due to DC bias levels and should be appropriately derated to ensure the required output capacitance is obtained in the application.

For the target output ripple, the output capacitance required is given by:

$$C_{OUT\_RIPPLE} \geq \frac{I_{OUT} \times (I_{LIM} - K \times I_{OUT})^2}{I_{LIM}^2 \times f_{SW} \times V_{OUTRIPP}}$$

where,

C_{OUT_RIPPLE} = Derated output capacitance in F.

f_{SW} = Switching frequency in Hz.

$V_{OUTRIPP}$ = Target value of output-voltage ripple in V.

The output capacitance for a given load step (I_{STEP}), output voltage deviation (ΔV_{OUT}) can be estimated as:

$$C_{OUT\_STEP} = \frac{I_{STEP} \times t_{RESPONSE}}{2 \times \Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right)$$

where,

I_{STEP} = Load step in Amperes.

$t_{RESPONSE}$ = Response time of the converter.

ΔV_{OUT} = Allowable output voltage dip in Volts.

f_C = Target closed-loop bandwidth to be selected between 1/20 to 1/40 of the f_{SW}

The output capacitance, C_{OUT} for MAX17690 should be selected to be larger of C_{OUT_RIPPLE} and C_{OUT_STEP}.

Loop Compensation

The MAX17690 is compensated using an external resistor capacitor network on the COMP pin. The loop compensation network are connected as shown in Figure 5.

The loop compensation values are calculated as follows:

$$R_Z = 12500 \times R_{CS} \times \left[\frac{f_C}{f_P}\right] \sqrt{\frac{V_{OUT} \times I_{OUT}}{2 \times L_{MAG} \times f_{SW}}}\ \Omega$$

$$C_Z = \frac{1}{2\pi \times R_Z \times f_P}\ \text{Farad}$$

$$C_P = \frac{1}{\pi \times R_Z \times f_{SW}}\ \text{Farad}$$

where :

$$f_P = \frac{1}{\pi \times \frac{V_{OUT}}{I_{OUT}} \times C_{OUT}}\ \text{Hz}$$

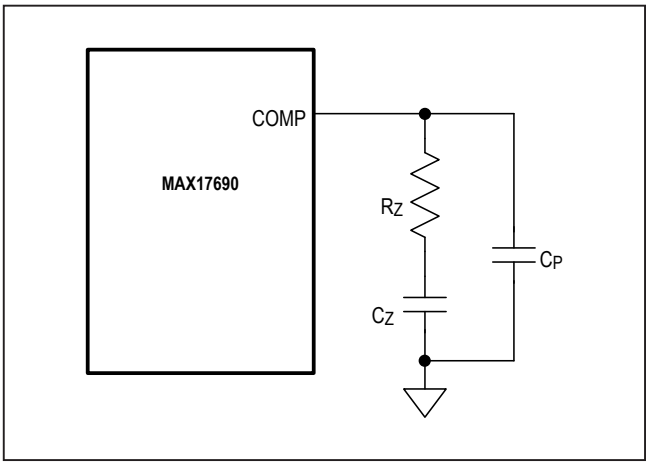


Figure 5. Loop Compensation Arrangement

Selection of Primary MOSFET

MOSFET selection criteria includes maximum drain voltage, primary peak/RMS current, the on-state resistance ($R_{DS(ON)}$), total gate charge(Q_G), the parasitic capacitance(Coss) and the maximum allowable power dissipation of the package without exceeding the junction temperature limits. The voltage seen by the MOSFET drain is the sum of the input voltage, the reflected secondary voltage on the transformer primary, and the leakage inductance spike. The MOSFET's absolute maximum VDS rating must be higher than the worst-case drain voltage,

$$V_{DS\,MAX} = V_{IN\,MAX} + \left(\frac{2.5 \times (V_{OUT} + V_D)}{K}\right)$$

RCD and RC snubber Circuit section covers the selection of snubber components to limit the drain-to-source voltage to $V_{DS\,MAX}$ value selected in the above equation.

Since the MAX17690 converter is operated in DCM, turn-on and turn-off transition losses can be ignored in loss budget. Mainly conduction loss and switching loss contribute to the total loss in the MOSFET.

The conduction loss in the MOSFET during full load can be calculated using the formula below:

$$P_{CONDUCTION} = I^2_{PRI\,RMS} \times R_{DS(ON)}$$

where $R_{DS(ON)}$ is the drain-source on-resistance of the MOSFET, which can be obtained from the MOSFET data sheet.

The switching loss due to drain-source capacitive energy being dissipated in the primary MOSFET depends on the drain-to-source voltage at the turn-on instant of the MOSFET. The worst-case switching losses can be estimated using the equation given below:

$$P_{SWITCHING} = \frac{1}{2} \times C_{OSS} \times \left[V_{IN\,MAX} + \frac{(V_{OUT} + V_D)}{K}\right]^2 \times f_{SW}$$

where, C_{OSS} is the Drain-source capacitance of the MOSFET, which can be obtained from the MOSFET data sheet.

The total loss in the MOSFET is,

$$P_{TOTAL} = P_{CONDUCTION} + P_{SWITCHING}$$

Estimate the junction temperature of the MOSFET using the total loss calculated above and the thermal characteristics of the MOSFET available from the data sheet. It is important to select a proper MOSFET and package that limits the junction temperature of the MOSFET to safe levels specified in the MOSFET data sheet.

Selection of Secondary Diode

In a flyback converter, since the secondary diode is reverse biased when the primary MOSFET is conducting, the voltage stress on the diode is the sum of the output voltage and the reflected primary voltage. Reverse-blocking voltage across the diode under steady-state conditions can be calculated using the equation below:

$$V_{SEC,DIODE} = K \times V_{IN\,MAX} + V_{OUT}$$

In practice due to parasitic inductance in the secondary loop and parasitic capacitance on the anode node of the diode, there exists an additional voltage ringing across the diode while the diode is reverse biased. To accommodate the additional voltage ringing, select a DC blocking voltage of the diode with the necessary margin (1.5 x $V_{SEC,\,DIODE}$ to 2.5 x $V_{SEC,\,DIODE}$).

Select a diode with low forward-voltage drop to minimize the power loss (given as the product of forward-voltage drop and the average output current) in the diode. Select fast-recovery diodes with a recovery time less than 50ns, or Schottky diodes with low junction capacitance for this purpose.

RCD and RC Snubber Circuit

Ideally, the external MOSFET experiences a drain-source voltage stress equal to the sum of the input voltage and reflected output voltage across the primary winding during the off period of the MOSFET. In practice, parasitic inductors and capacitors in the circuit, such as leakage inductance of the flyback transformer and the MOSFET output capacitance cause voltage overshoot and ringing on the drain node of the MOSFET. Snubber circuits are used to limit the voltage overshoot to safe levels, within the voltage rating of the external MOSFET. The widely used RCD snubber circuit is shown in Figure 6 and the operating waveforms with the snubber circuit are shown in Figure 7.

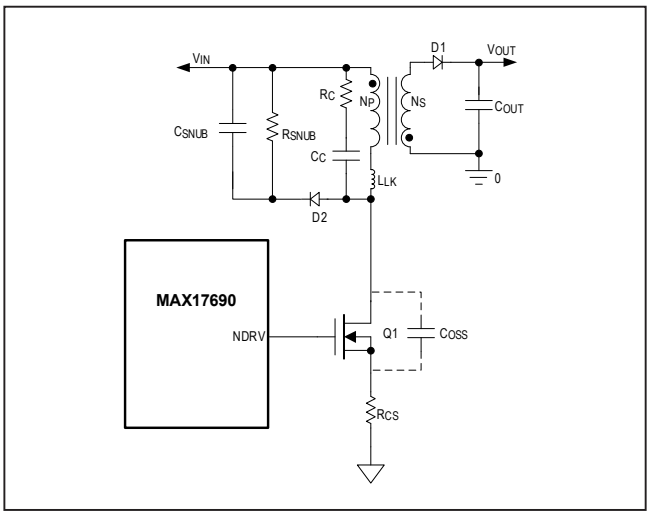


Figure 6. RC and RCD Clamp Circuitry

Use the following procedure to calculate the RCD clamp components:

The voltage across the leakage inductance (V_{LLK}) at the primary nMOSFET turn-off instant is given by,

$$V_{LLK} = \left(V_{CSN} - \frac{\Delta V_{CSN}}{2}\right) - \left(\frac{V_{OUT} + V_D}{K}\right)$$

where,

V_{CSN} = Peak voltage across C_{SNUB}

$\left(V_{CSN} - \frac{\Delta V_{CSN}}{2}\right)$ = Average voltage across C_{SNUB}

Since,

$$V_{LLK} = L_{LK} \times \frac{I_{LIM}}{t_S}$$

By rearranging:

$$t_S = \frac{L_{LK} \times I_{LIM}}{\left(V_{CSN} - \frac{\Delta V_{CSN}}{2}\right) - \left(\frac{V_{OUT} + V_D}{K}\right)}$$

Both the equations given below estimate the average power dissipated in the snubber resistor R_{SNUB},

$$P_{SN(AVG)} = \frac{1}{2} \times \left(V_{CSN} - \frac{\Delta V_{CSN}}{2}\right) \times I_{LIM} \times t_S \times f_{SW}$$

$$P_{SN(AVG)} = \frac{\left(V_{CSN(RMS)}\right)^2}{R_{SNUB}}$$

where,

$$V_{CSN(RMS)} = \sqrt{\frac{(V_{CSN})^2 + (V_{CSN}) \times (V_{CSN} - \Delta V_{CSN}) + (V_{CSN} - \Delta V_{CSN})^2}{3}}$$

Combining the last two equations we have an expression for R_{SNUB}:

$$R_{SNUB} = \frac{(V_{CSN})^2 + (V_{CSN}) \times (V_{CSN} - \Delta V_{CSN}) + (V_{CSN} - \Delta V_{CSN})^2}{3 \times P_{SN(AVG)}}$$

Over one switching period charge balance equation for C_{SNUB} can be approximated as below:

$$\frac{V_{CSN}}{R_{SNUB}} \times \frac{1}{f_{SW}} = C_{SNUB} \times \Delta V_{CSN}$$

Now use the equation below to calculate the C_{SNUB} for the target ΔV_{CSN}. Generally, ΔV_{CSN} is kept as approximately 10% to 40% of V_{CSN}.

$$C_{SNUB} = \frac{V_{CSN}}{\Delta V_{CSN} \times R_{SNUB} \times f_{SW}}$$

Choosing too small a value for V_{CSN} results in higher power losses in the snubber resistor. Typically, V_{CSN} is selected between 1.5 x to 2.5 x the reflected output voltage to limit the losses in the snubber. In the *Selection of Primary MOSFET* section the MOSFET absolute V_{DS} rating is selected for 2.5 x the reflected voltage. Hence, V_{CSN} should be selected using below equation with necessary design margin.

$$V_{CSN} < 2.5 \times \frac{(V_{OUT} + V_D)}{K}$$

The reverse blocking voltage rating for the snubber diode (D2) is given by,

$$V_{D2} = V_{IN\,MAX} + \left(2.5 \times \frac{V_{OUT}}{K}\right)$$

The RCD clamp only limits the maximum voltage stress on the primary MOSFET during the clamping period but at the end of the clamping period due to the remaining stored energy in the leakage inductance, oscillations are observed on the drain node due to interaction between Llk and the drain node capacitance (C_{PAR}). The MAX17690 uses the drain voltage information to sample the output voltage and the earliest sampling instant is 350ns from the NDRV falling edge. Therefore, it is important to damp the drain node ringing within 350ns from the NDRV falling.

For designs, with dominant ringing on the drain node after 350ns from the NDRV falling, an additional RC snubber across the transformer primary winding is required. Use the following steps for designing an effective RC snubber,

1) Measure the ringing time period t_1 for the oscillations on the drain node immediately after the clamp period.

$$t_1 = 2\pi\sqrt{L_{LK} \times C_{PAR}}$$

2) Add a test capacitance on the drain node until the time period of this ringing is increased to 1.5 to 2 times of t_1. Start with a 100pF capacitor. With the added capacitance C_D measure the new ringing time period (t_2),

$$t_2 = 2\pi\sqrt{L_{LK} \times (C_{PAR} + C_D)}$$

3) Use the following formula to calculate the drain node capacitance (C_{PAR}),

$$C_{PAR} = \frac{C_D}{\left(\left(\frac{t_2}{t_1}\right)^2 - 1\right)}$$

4) Use the following formula to calculate the leakage inductance,

$$L_{LK} = \frac{t_1^2}{(4 \times \pi^2 \times C_{PAR})}$$

5) Now, use the following equations to calculate the RC snubber values,

$$C_C = 1.5 \text{ to } 2 \text{ times the } C_{PAR}$$

$$R_C = \sqrt{\frac{L_{LK}}{C_{PAR}}}$$

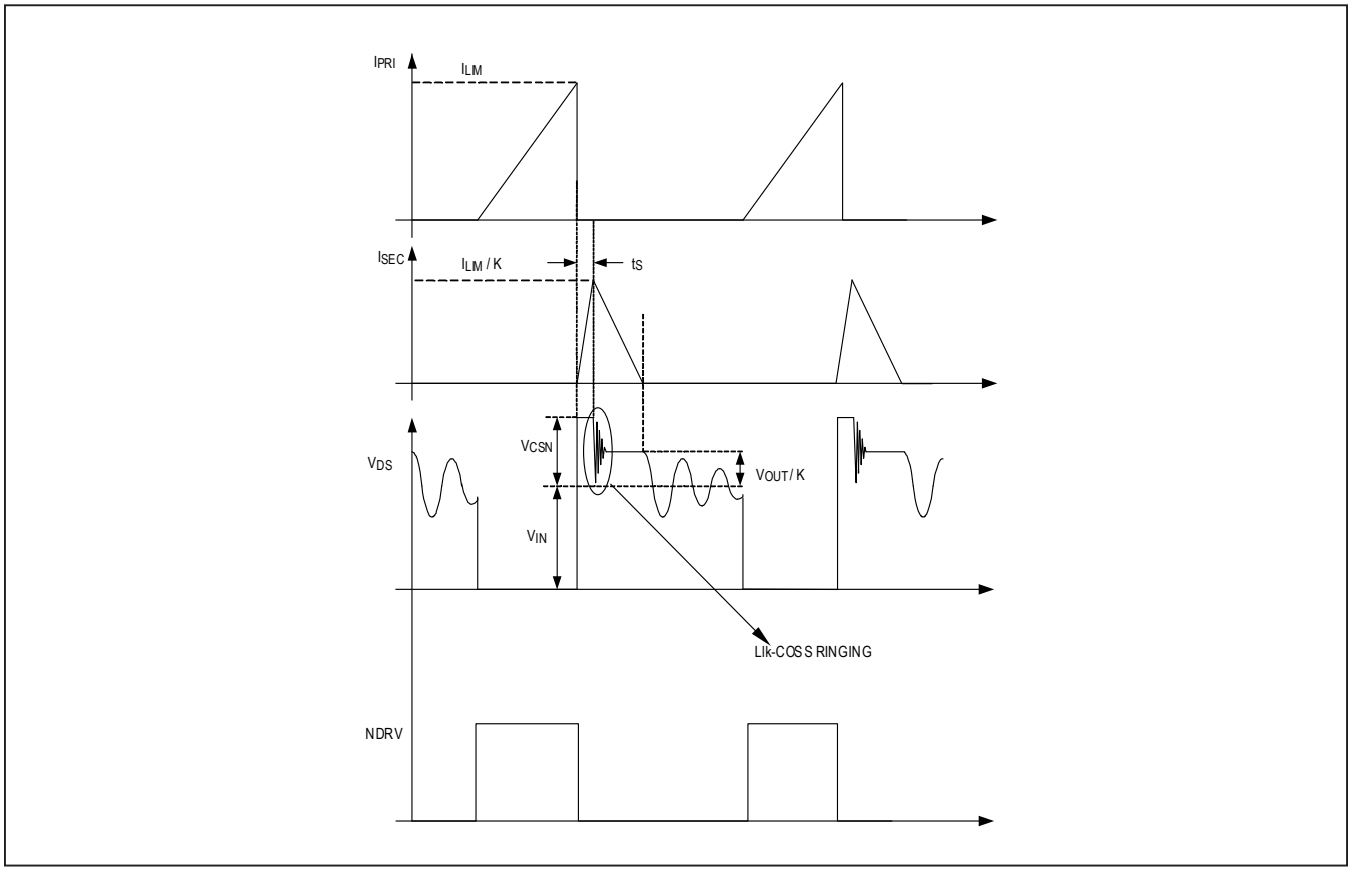


Figure 7. Waveforms with RCD Clamp.

Design Example:

The following industrial specification is used to demonstrate the design calculations for the MAX17690 based flyback converter,

Input voltage range: 18V to 36V

Output voltage: 5V

Load current: 1A

1. Selection of Duty cycle

Plug-in the $V_{IN\ MIN}$ and $V_{IN\ MAX}$ from the above specification in the formula below to calculate the D_{MAX},

$$D_{MAX} = \left(\frac{V_{IN\ MAX}}{V_{IN\ MAX} + (2 \times V_{IN\ MIN})} \right) = 0.5p.\ u$$

2. Switching Frequency

Use the below formula established earlier in this data sheet to calculate the maximum possible f_{SW},

$$f_{SW} \le \left(\frac{720000 \times D_{MAX} \times V_{IN\ MIN}}{V_{IN\ MAX}} \right)$$

$$f_{SW} \le \left(\frac{720000 \times 0.5 \times 18}{36} \right)$$

$$f_{SW} \le 180kHz$$

With minimum converter target efficiency (η) of 0.8,

For the present application, the switching frequency is selected as 180kHz. The R_{RT} is calculated for the selected f_{SW},

$$R_{RT} = \frac{5 \times 10^6}{f_{SW}} \Omega$$

$$R_{RT} = \frac{5 \times 10^9}{180k} = 27.7k\Omega,$$

standard resistor of 27.4kΩ is selected for R_{RT},

3. Transformer magnetizing inductance and Turns Ratio

Once the switching frequency and duty cycle are selected, the transformer magnetizing inductance(L_{MAG}) can be calculated from the energy balance equation given in the data sheet,

$$L_{MAG} = \frac{0.5 \times \eta \times (V_{IN\ MIN} \times D_{MAX})^2}{V_{OUT} \times I_{OUT} \times f_{SW}}$$

$$L_{MAG} = \frac{0.4 \times (18 \times 0.5)^2}{5 \times 1 \times 180k} = 36\mu H.$$

For the present design L_{MAG} is chosen to be 36µH. Use the following equation to calculate the maximum duty cycle of the converter for the selected frequency and magnetizing inductance,

$$D = \frac{\sqrt{2.5 \times L_{MAG} \times V_{OUT} \times I_{OUT} \times f_{SW}}}{V_{IN\ MIN}}$$

$$D = \frac{\sqrt{2.5 \times 36\mu \times 5 \times 1 \times 180k}}{18} = 0.5p.u$$

Calculate the required transformer turns ratio (K) using the below formula,

$$K = \frac{N_S}{N_P} = \frac{0.8 \times (V_{OUT} + V_D) \times (1 - D)}{V_{IN\ MIN} \times D}$$

$$K = \frac{0.8 \times (5 + 0.3) \times (1 - 0.5)}{18 \times 0.5} = 0.235$$

For the present design, K is chosen as 1:0.222

4. Selection of Current Sense Resistor

The transformer primary peak current value depends on the output power, L_{MAG} and the f_{SW}. Use the below formula to calculate the peak current,

$$I_{LIM} = \sqrt{\frac{2 \times V_{OUT} \times I_{OUT}}{\eta \times L_{MAG} \times f_{SW}}}$$

$$I_{LIM} = \sqrt{\frac{2.5 \times 5 \times 1}{36\mu \times 180k}} = 1.38A$$

With minimum converter target efficiency (η) of 0.8,

The value of R_{CS} decides the peak current limit and the runaway current limit. Use the below formula to select the R_{CS},

$$R_{CS} = \frac{0.08}{I_{LIM}} = 57.9m\Omega$$

For the present application, a standard resistor of 56mΩ is selected.

5. Calculate the Min t_{ON} and Min t_{OFF}

The MAX17690 has the minimum current sense voltage threshold limit at 20mV. For the selected current sense resistor, the minimum primary peak current allowed by the converter is,

$$I_{PY\ MIN} = \frac{0.02}{R_{CS}} = \frac{0.02}{0.056} = 0.357A$$

The minimum time required by the converter to reach the minimum primary peak current is,

$$t_{ON\ MIN} = \frac{L_{MAG} \times I_{PY\ MIN}}{V_{IN\ MAX}} = \frac{36\mu \times 0.357}{36} = 357ns$$

The calculated $t_{ON\ MIN}$ value (357ns) is higher than the MAX17690 $t_{ON\ MIN}$ (230ns). Similarly, the minimum off-time of the converter is calculated as,

$$t_{OFF\ MIN} = \frac{K \times L_{MAG} \times I_{PY\ MIN}}{V_{OUT}} = \frac{0.22 \times 36\mu \times 0.357}{5} = 565ns$$

The calculated $t_{OFF\ MIN}$ value (565ns) is higher than the MAX17690 $t_{OFF\ MIN}$ (490ns).

6. Selection of Secondary Diode

The maximum operating reverse-voltage rating must be higher than the sum of the output voltage and the reflected input voltage.

$$V_{SEC,\ DIODE} = 1.5 \times (K \times V_{IN\ MAX} + V_{OUT})$$

$$V_{SEC,\ DIODE} = 1.5 \times (0.22 \times 36 + 5) = 19.38V$$

The current rating of the secondary diode should be selected so that the power loss in the diode be low enough to ensure that the junction temperature is within limits. For the present design, SBR8U60P5 is selected as the secondary diode rectifier.

7. R_{IN}, R_{FB}, and R_{SET} Resistor Selection

$$R_{FB} = \frac{R_{SET}}{V_{SET}} \times \frac{1}{K} \times \left[(V_{OUT} + V_D) - \frac{V_{TC} \times \left(\frac{\delta V_D}{\delta T} \right)}{\frac{\delta V_{TC}}{\delta T}} \right]$$

Using the temperature coefficient of the selected secondary diode, $\frac{\delta V_D}{\delta T}$ = -1mV/°C

$$R_{FB} = \frac{10 \times 10^3}{1} \times \frac{1}{0.22} \times \left[(5 + 0.3) - \frac{0.55 \times (-1)}{1.85} \right] = 255k\Omega$$

R_{IN} = 0.6 x R_{FB} = 153kΩ, a standard resistor 150kΩ is selected.

8. Temperature Compensation

For the selected secondary diode, from the forward characteristics of the diode data sheet note the diode temperature coefficient. To compensate the change in output voltage caused due to the diode temperature coefficient, select the R_{TC} resistor to be

$$R_{TC} = -K \times R_{FB} \times \frac{\left(\frac{\delta V_{TC}}{\delta T} \right)}{\left(\frac{\delta V_D}{\delta T} \right)}$$

$$R_{TC} = -0.222 \times 255 \times 10^3 \times \frac{(1.85)}{(-1)} = 104.7k\Omega$$

A standard resistor value of 100kΩ is selected for the RTC resistor.

9. Soft-Start Capacitor

For the desired soft-start time (t_{SS} = 10ms), the SS capacitor is selected using

$$C_{SS} = 5 \times t_{SS} = 50nF$$

47nF is selected as the soft-start capacitor.

10. Selection of R_{VCM} Resistor

Follow the below steps to select the R_{VCM} resistor value.

1) Calculate the internal scaling factor:

$$K_C = \frac{100\mu \times (1-D)}{3 \times f_{SW} \times 10^{-12}}$$

$$K_C = \frac{100 \times 10^{-6} \times (1-0.5)}{3 \times 180k \times 10^{-12}} = 92.6$$

From Table 3, choose the next higher value for the calculated K_C. K_C = 160.

Select the resistor value corresponding to the choice of capacitor, as the R_{VCM}. R_{VCM} = 121kΩ

11. MOSFET Selection

The voltage on the MOSFET drain is the sum of the input voltage, the reflected secondary voltage on the transformer primary, and the leakage inductance spike. The MOSFET's absolute maximum VDS rating should be selected

$$V_{DS\ MAX} = V_{IN\ MAX} + 2.5 \times \frac{(V_{OUT} + V_D)}{K}$$

$$V_{DS\,MAX} = 36 + \left(\frac{2.5 \times (5 + 0.3)}{0.22}\right) = 96.2V$$

For this application, the SIR698DP-T1-GE3 is selected as the primary MOSFET.

12. Output Capacitor Selection

For the target output ripple of 50mV,

$$C_{OUT\_RIPPLE} \geq \frac{I_{OUT} \times (I_{LIM} - K \times I_{OUT})^2}{I_{LIM}^2 \times f_{SW} \times V_{OUTRIPP}}$$

$$C_{OUT\_RIPPLE} = \frac{1 \times (1.38 - 0.22 \times 1)^2}{1.38^2 \times 180 \times 10^3 \times 50 \times 10^{-3}} = 78\mu F$$

The output capacitor is chosen to have 3% output voltage deviation for a 50% load step of the rated output current. The bandwidth is usually selected in the range of f_{SW}/20 to f_{SW}/40. For the present design, the bandwidth is chosen as 8kHz.

$$T_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right) = 46.8\mu s.$$

$$C_{OUT\_STEP} = \frac{I_{STEP} \times T_{RESPONSE}}{2 \times \Delta V_{OUT}}$$

$$C_{OUT\_STEP} = \frac{0.5 \times 46.8m}{2 \times 0.03 \times 5} = 78\mu F$$

Table 3. R_{VCM} Resistor Selection

K_C	R_{VCM} (KΩ)
640	0
320	75
160	121
80	220
40	Open

Due to the dc-bias characteristics, the 100µF, 6.3V, 1210 capacitor offers 42.7µF at 5V. Hence two 100µF, 6.3V, 1210 capacitors are selected for the present design.

13. Loop Compensation

The loop compensation values are calculated as follows

$$\text{LOAD POLE } F_P = \frac{I_{OUT}}{\pi \times V_{OUT} \times C_{OUT}} = 800Hz$$

$$R_Z = 12500 \times R_{CS} \left(\frac{f_C}{f_P}\right) \sqrt{\frac{V_{OUT} \times I_{OUT}}{2 \times L_{PRI} \times f_{SW}}}$$

$$R_Z = 12500 \times 56m \times \left(\frac{8k}{800}\right) \sqrt{\frac{5 \times 1}{2 \times 36\mu \times 180k}} = 4.37k\Omega,$$

A standard 4.42kΩ is selected.

$$C_Z = \frac{1}{2\pi \times R_Z \times f_P} = 47nF$$

$$C_P = \frac{1}{\pi \times R_Z \times f_{SW}} = 470pF$$

14. Input Capacitor Selection

Calculate the input capacitance using the following equations to limit the ripple voltage amplitude ΔV_{IN} to less than 2% of the nominal input voltage (0.48V of ripple voltage),

$$C_{IN} \geq \frac{1.38 \times 0.5 \times \left(1 - \frac{0.5}{2}\right)^2}{2 \times 180 \times 10^3 \times 0.48} = 2.25\mu F$$

Due to the DC-bias characteristics, the 4.7µF, 50V, 1210 capacitor offers 2.1µF at 36V. Hence, 2 x 4.7µF, 50V, 1210 capacitors are selected for the present design.

PCB Layout guidelines

Careful PCB layout is critical to achieve clean and stable operation. Follow the below guidelines for good PCB layout:

1) Keep the loop area of paths carrying the pulsed currents as small as possible. In flyback design, the high frequency current path from the V_{IN} bypass capacitor through the primary-side winding, the MOSFET switch and sense resistor is a critical loop. Similarly, the high frequency current path for the MOSFET gate switching from the INTVCC capacitor through the source of the MOSFET and sense resistor is critical as well.
2) INTVCC bypass cap should be connected right across the INTVCC and PGND pins of the IC.
3) A bypass capacitor should be connected across to V_{IN} and SGND pins, and should be placed close to the IC.
4) The exposed pad of the IC should be directly connected to SGND pin of the IC. The exposed pad should also be connected to SGND plane in other layers by means of thermal vias under the exposed pad so that the heat flows to the large “signal ground” (SGND) plane.
5) The R_{FB} resistor trace length should be kept as small as possible.
6) The PGND connection from the INTVCC capacitor and the SGND plane should be star connected at the negative terminal of the current sense resistor.

To see the actual implementation of above guidelines, refer the MAX17690 evaluation kit layouts available at **www.maximintegrated.com**.

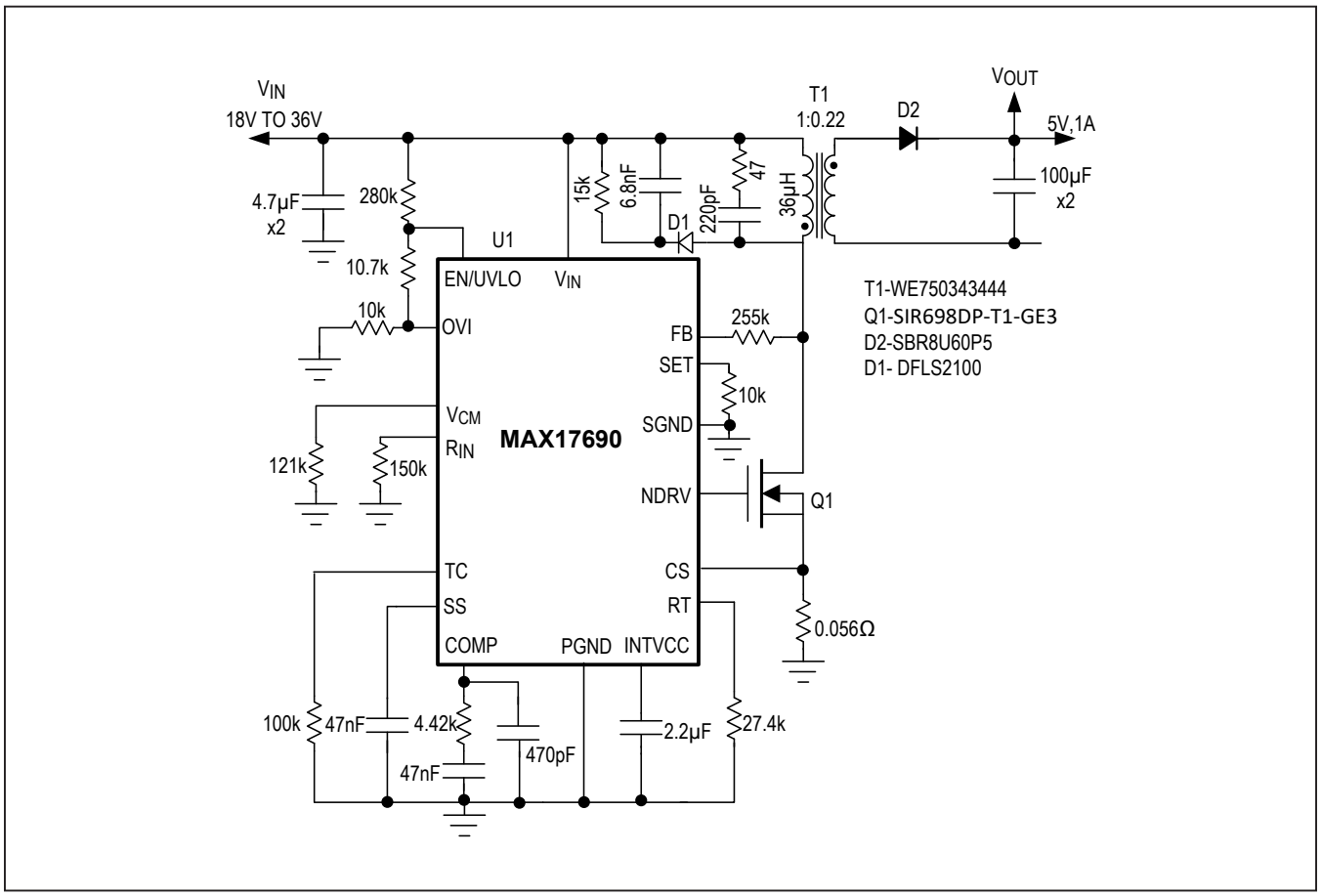


Figure 8. 24V to 5V, 1A No-Opto Flyback Application Circuit

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17690ATE+	-40°C to +125°C	16 TQFN

+Denotes a lead(pB)-free/RoHS-compliant package.

Chip Information

PROCESS: CMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/16	Initial release	—
1	12/16	Updated *General Description*, *Application Circuit*, and *Absolute Maximum Ratings* sections. Updated *Electrical Characteristics* and *Pin Description* tables, and Table 1. Updated *Typical Operating Characteristics* TOC03, TOC05, and replaced TOC01–TOC02 and TOC06–TOC08. Updated *Pin Configuration*, Figure 1 and Figure 2, and added Figures 4–5. Replaced *Functional Diagram* and *Typical Application Circuit*, which also changed from *Typical Application Circuit* to Figure 6. Updated *Detailed Description*, *INTVCC*, and *Output Capacitor Selection* sections. Replaced *Supply Voltage*, *Switching Frequency, Selection of R_{IN}, R_{FB}, and R_{SET} Resistor, Selection of R_{VCM} Resistor, Temperature Compensation,* and *PCB Layout* sections. Added *Applications Information* section. Deleted *Setting Peak Current Limit, Transformer Magnetizing Inductance and Leakage Inductance*, and *Minimum Load Requirement* sections.	1–21
2	3/19	Updated the *Functional Diagram*; corrected style throughout in equation descriptions and changed VIN references to V_{IN}	9
3	7/19	Updated the *Benefits and Features, Application Circuit, Package Information, Electrical Characteristics, Typical Operating Characteristics, Pin Description, Functional Diagram, Detailed Description, Applications Information, PCB Layout Guidelines,* and *Ordering Information* sections	1–3, 5, 7, 9–11 14–17, 20, 21
3.1		Corrected error in an equation in the *Applications Information* section	16
4	8/19	Updated the *Package Information* section	2
5	1/20	Updated the *Benefits and Features, Application Circuit, Package Information, Electrical Characteristics, Typical Operating Characteristics, Pin Description, Functional Diagram, Detailed Description, Applications Information, PCB Layout Guidelines,* and *Ordering Information* sections	1–3, 5, 7, 9–11 14–17, 20, 21
6	7/20	Updated TOC01–TOC03; updated the *INTVCC, Switching Frequency, Short-Circuit Protection/Hiccup, Transformer Selection, Loop Compensation, Selection of Primary MOSFET, Selection of Secondary Diode, RCD and RC Snubber Circuit* and *Design Example* sections, and Figure 9 (after renumbering); added the *Theory of No-Opto Flyback Operation* and *Input Capacitor Selection* sections, new Figures 1 and 2, and renumbered other figures; replaced the *Selection of R_{IN}, R_{FB}, R_{SET}, and R_{TC} Resistors* and *Output Capacitor Selection* sections; removed the *Temperature Compensation* and *Setting Peak Current Limit* sections	5, 10–22
7	8/20	Updated the *Selection of R_{IN}, R_{FB}, R_{SET} and R_{TC} Resistors* section	12

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