*Click here to ask about the production status of specific part numbers.*

# MAX17576

# 4.5V to 60V, 4A, High-Efficiency, Synchronous Step-Down DC-DC Converter with Internal Compensation

## General Description

The Himalaya series of voltage regulator ICs, power modules, and chargers enable cooler, smaller, and simpler power supply solutions. The MAX17576, high-efficiency, high-voltage, Himalaya synchronous step-down DC-DC converter with integrated MOSFETs operates over an input voltage range of 4.5V to 60V. The converter can deliver up to 4A current. Output voltage is programmable from 0.9V up to 90% of $V_{IN}$. The feedback voltage regulation accuracy over -40°C to +125°C is ±0.9%. Built-in compensation across the output-voltage range eliminates the need for external compensation components.

The MAX17576 features a peak-current-mode control architecture. The device can operate either in constant-frequency based pulse-width modulation (PWM) or pulse-frequency modulation (PFM), or discontinuous-conduction mode (DCM) control schemes. A programmable soft-start feature allows users to reduce input inrush current. The device also incorporates an output enable/undervoltage lockout pin (EN/UVLO) that allows the user to turn on the part at the desired input voltage level. The MAX17576 offers a low minimum on time that allows high switching frequencies and a small solution size.

The MAX17576 is available in a 24-pin (4mm x 5mm) TQFN package. Simulation models are available.

## Applications

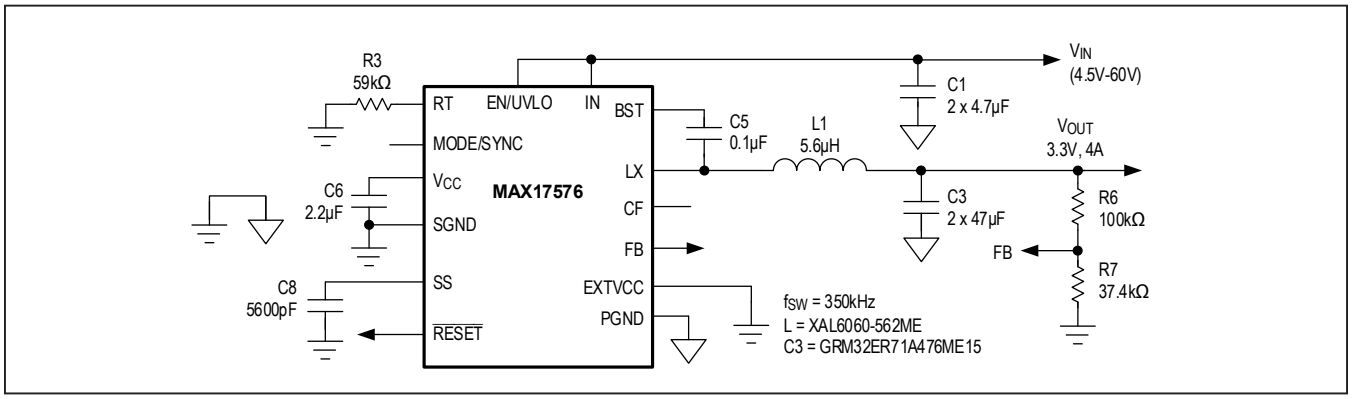
- Industrial Control Power Supplies
- General Purpose Point-of-Load
- Distributed Supply Regulation
- Base Station Power Supplies
- Wall Transformer Regulation
- High-Voltage, Single-Board Systems

## Benefits and Features

- Reduces External Components and Total Cost
  - No Schottky-Synchronous Operation
  - Internal Compensation for Any Output Voltage
  - All-Ceramic Capacitors, Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4.5V to 60V Input
  - Adjustable Output Voltage Range from 0.9V up to 90% of $V_{IN}$
  - 100kHz to 2.2MHz Adjustable Switching Frequency with External Clock Synchronization
- Reduces Power Dissipation
  - Peak Efficiency of 94.8%
  - PFM and DCM Modes Enable Enhanced Light-Load Efficiency
  - Auxiliary Bootstrap Supply (EXTVCC) for Improved Efficiency
  - 2.8µA Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Hiccup Mode Overload Protection and Auto-Retry Startup
  - Adjustable Soft-Start and Prebiased Power-Up
  - Built-In Output-Voltage Monitoring with $\overline{RESET}$
  - Programmable EN/UVLO Threshold
  - Monotonic Startup with Prebiased Output Voltage
  - Overtemperature Protection
  - Wide -40°C to +125°C Ambient Operating Temperature Range/-40°C to +150°C Junction Temperature Range

***Ordering Information* appears at end of data sheet.**

## Typical Application Circuit



## Absolute Maximum Ratings

IN to PGND .....-0.3V to +65V
EN/UVLO to SGND .....-0.3V to +65V
LX to PGND..... -0.3V to $V_{IN}$ + 0.3V
EXTVCC to SGND .....-0.3V to +26V
BST to PGND .....-0.3V to +70V
BST to LX .....-0.3V to +6.5V
BST to $V_{CC}$ .....-0.3V to +65V
$\overline{RESET}$, SS, MODE/SYNC, $V_{CC}$, RT, CF to SGND.....-0.3V to +6.5V
FB to SGND .....-0.3V to +1.5V
PGND to SGND.....-0.3V to +0.3V
LX Total RMS Current ..... ±5.6A
Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (multilayer Board) ($T_A$ = +70°C, derate 41.7mW/°C above +70°C.).....3333mW
Operating Temperature Range (Note 1)..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

| **PACKAGE TYPE: 24 TQFN** | |
|---|---|
| Package Code | T2445+2C |
| Outline Number | **21-0201** |
| Land Pattern Number | **90-0083** |
| **THERMAL RESISTANCE, FOUR-LAYER BOARD (Note 2)** | |
| Junction to Ambient ($\theta_{JA}$) | 24°C/W |
| Junction to Case ($\theta_{JC}$) | 1.8°C/W |

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

**Note 1:** Junction temperature greater than +125°C degrades operating lifetimes.
**Note 2:** Package thermal resistances were obtained using the MAX17576 evaluation kit with no airflow.

## Electrical Characteristics

($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $R_{RT}$ = 40.2KΩ ($f_{SW}$ = 500kHz), $C_{VCC}$ = 2.2µF, $V_{SGND}$ = $V_{PGND}$ = $V_{MODE/SYNC}$ = $V_{EXTVCC}$ = 0V, $V_{FB}$ = 1V, LX = SS = CF = $\overline{RESET}$ = OPEN, $V_{BST}$ to $V_{LX}$ = 5V, $T_A$ = -40°C to 125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **INPUT SUPPLY (IN)** | | | | | | |
| Input Voltage Range | $V_{IN}$ | | 4.5 | | 60 | V |
| Input Shutdown Current | $I_{IN-SH}$ | $V_{EN/UVLO}$ = 0V (shutdown mode) | | 2.8 | 4.5 | µA |
| Input Quiescent Current | $I_{Q_PFM}$ | MODE/SYNC = RT = open, $V_{EXTVCC}$ = 5V | | 61 | | µA |
| | | MODE/SYNC = open, $V_{EXTVCC}$ = 5V | | 71 | | µA |
| | $I_{Q_DCM}$ | DCM Mode, $V_{LX}$ = 0.1V | | 1.2 | 1.8 | mA |
| | $I_{Q_PWM}$ | Normal switching mode, $f_{SW}$ = 500kHz, $V_{FB}$ = 0.8V | | 14 | | mA |
| **ENABLE/UVLO (EN)** | | | | | | |
| EN/UVLO Threshold | $V_{ENR}$ | $V_{EN/UVLO}$ rising | 1.19 | 1.215 | 1.26 | V |
| EN/UVLO Threshold | $V_{ENF}$ | $V_{EN/UVLO}$ falling | 1.068 | 1.09 | 1.131 | V |
| EN/UVLO Threshold | $V_{EN-TRUESD}$ | $V_{EN/UVLO}$ falling | | 0.8 | | V |
| EN Input Leakage Current | $I_{EN}$ | $V_{EN/UVLO}$ = 0V, $T_A$ = +25°C | -50 | 0 | +50 | nA |
| **$V_{CC}$ LDO** | | | | | | |
| $V_{CC}$ Output Voltage Range | $V_{CC}$ | 1mA ≤ $I_{VCC}$ ≤ 25mA | 4.75 | 5 | 5.25 | V |
| | | 6V ≤ $V_{IN}$ ≤ 60V; $I_{VCC}$ = 1mA | 4.75 | 5 | 5.25 | V |
| $V_{CC}$ Current Limit | $I_{VCC(MAX)}$ | $V_{CC}$ = 4.3V, $V_{IN}$ = 7V | 40 | 65 | 130 | mA |
| $V_{CC}$ Dropout | $V_{CC-DO}$ | $V_{IN}$ = 4.5V , $I_{VCC}$ = 20mA | 4.2 | | | V |
| $V_{CC}$ UVLO | $V_{CC-UVR}$ | Rising | 4.05 | 4.2 | 4.3 | V |
| | $V_{CC-UVF}$ | Falling | 3.65 | 3.8 | 3.9 | V |
| **EXT LDO** | | | | | | |
| EXTVCC Operating Voltage Range | | | 4.84 | | 24 | V |
| EXTVCC Switchover Threshold | $V_{EXTVCC_R}$ | Rising | 4.56 | 4.7 | 4.84 | V |
| | $V_{EXTVCC_F}$ | Falling | 4.3 | 4.45 | 4.6 | V |
| EXTVCC Dropout | $V_{EXTVCC_DO}$ | $V_{EXTVCC}$ = 4.75V, $I_{VCC}$ = 20mA | | | 0.3 | V |
| EXTVCC Current Limit | | $V_{CC}$ = 4.5V, $V_{EXTVCC}$ = 7V | 40 | 85 | 160 | mA |

## Electrical Characteristics (continued)

($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $R_{RT}$ = 40.2KΩ ($f_{SW}$ = 500kHz), $C_{VCC}$ = 2.2µF, $V_{SGND}$ = $V_{PGND}$ = $V_{MODE/SYNC}$ = $V_{EXTVCC}$ = 0V, $V_{FB}$ = 1V, LX = SS = CF = $\overline{RESET}$ = OPEN, $V_{BST}$ to $V_{LX}$ = 5V, $T_A$ = -40°C to 125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER MOSFETS** | | | | | | |
| High-Side nMOS On-Resistance | $R_{DS-ONH}$ | $I_{LX}$ = 0.3A ,sourcing | | 90 | 180 | mΩ |
| Low-Side nMOS On-Resistance | $R_{DS-ONL}$ | $I_{LX}$ = 0.3A , sinking | | 55 | 110 | mΩ |
| LX Leakage Current | $I_{LX_LKG}$ | $T_A$ = 25°C, $V_{LX}$ = ($V_{PGND}$ + 1V) to ($V_{IN}$ - 1V) | -2 | | +2 | µA |
| **SOFT-START (SS)** | | | | | | |
| Soft-Start Current | $I_{SS}$ | $V_{SS}$ = 0.5V | 4.7 | 5 | 5.3 | µA |
| **FEEDBACK (FB)** | | | | | | |
| FB Regulation Voltage | $V_{FB_REG}$ | MODE/SYNC = SGND or $V_{MODE/SYNC}$ = $V_{CC}$ | 0.892 | 0.9 | 0.908 | V |
| FB Regulation Voltage | $V_{FB_REG}$ | MODE/SYNC = OPEN | 0.892 | 0.916 | 0.934 | V |
| FB Input Leakage Current | $I_{FB}$ | 0 < $V_{FB}$ < 1V, $T_A$ = 25°C | -50 | | +50 | nA |
| **MODE/SYNC** | | | | | | |
| MODE Threshold | $V_{M-DCM}$ | $V_{MODE/SYNC}$ = $V_{CC}$ (DCM Mode) | $V_{CC}$ – 0.65 | | | V |
| MODE Threshold | $V_{M-PFM}$ | MODE/SYNC = OPEN (PFM Mode) | | $V_{CC}$/2 | | V |
| MODE Threshold | $V_{M-PWM}$ | MODE/SYNC = SGND (PWM Mode) | | | 0.75 | V |
| SYNC Frequency Capture Range | | $f_{SW}$ set by $R_{RT}$ | 1.1 x $f_{SW}$ | | 1.4 x $f_{SW}$ | kHz |
| SYNC Pulse Width | | | 50 | | | ns |
| SYNC Threshold | $V_{IL}$ | | | | 0.8 | V |
| | $V_{IH}$ | | 2.1 | | | V |
| **CURRENT LIMIT** | | | | | | |
| Peak Current Limit Threshold | $I_{PEAK-LIMIT}$ | | 5.5 | 6.5 | 7.5 | A |
| Runaway Current Limit Threshold | $I_{RUNAWAY-LIMIT}$ | | 6.1 | 7.2 | 8.3 | A |
| Valley Current-Limit Threshold | $I_{VALLEY-LIMIT}$ | MODE/SYNC = OPEN or $V_{MODE/SYNC}$ = $V_{CC}$ | -0.25 | 0 | +0.25 | A |
| Valley Current-Limit Threshold | $I_{VALLEY-LIMIT}$ | MODE/SYNC = SGND | | -1.8 | | A |
| PFM Current-Limit Threshold | $I_{PFM}$ | MODE/SYNC = OPEN | 0.75 | 1 | 1.3 | A |

## Electrical Characteristics (continued)

($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $R_{RT}$ = 40.2KΩ ($f_{SW}$ = 500kHz), $C_{VCC}$ = 2.2µF, $V_{SGND}$ = $V_{PGND}$ = $V_{MODE/SYNC}$ = $V_{EXTVCC}$ = 0V, $V_{FB}$ = 1V, LX = SS = CF = $\overline{RESET}$ = OPEN, $V_{BST}$ to $V_{LX}$ = 5V, $T_A$ = -40°C to 125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 3)

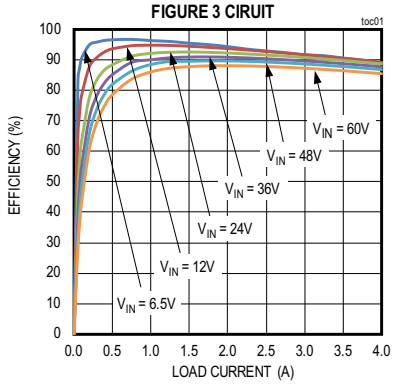
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **RT** | | | | | | |
| Switching Frequency | $f_{SW}$ | $R_{RT}$ = 40.2KΩ | 475 | 500 | 525 | kHz |
| | | $R_{RT}$ = OPEN | 460 | 500 | 540 | kHz |
| | | $R_{RT}$ = 8.06KΩ | 1950 | 2200 | 2450 | kHz |
| | | $R_{RT}$ = 210KΩ | 90 | 100 | 110 | kHz |
| $V_{FB}$ Undervoltage Trip Level to Cause HICCUP | $V_{FB_HICF}$ | | 0.56 | 0.58 | 0.65 | V |
| HICCUP Timeout | | | | 32768 | | Cycles |
| Minimum On-Time | $t_{ON_MIN}$ | | | 60 | 80 | ns |
| Minimum off-Time | $t_{OFF_MIN}$ | | 140 | | 160 | ns |
| LX Dead Time | | | | 5 | | ns |
| **$\overline{RESET}$** | | | | | | |
| $\overline{RESET}$ Output Level Low | $V_{RESETL}$ | $I_{\overline{RESET}}$ = 10mA | | | 400 | mV |
| $\overline{RESET}$ Output Leakage Current | $I_{RESETLKG}$ | $T_A$ = $T_J$ = 25°C, $V_{\overline{RESET}}$ = 5.5V | -0.1 | | +0.1 | µA |
| FB Threshold for $\overline{RESET}$ Deassertion | $V_{FB-OKR}$ | $V_{FB}$ rising | 93.8 | 95 | 97.8 | % |
| FB Threshold for $\overline{RESET}$ Assertion | $V_{FB-OKF}$ | $V_{FB}$ falling | 90.5 | 92 | 94.6 | % |
| $\overline{RESET}$ De-Assertion Delay After FB Reaches 95% Regulation | | | | 1024 | | Cycles |
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal Shutdown Threshold | $T_{SHDNR}$ | Temp rising | | 165 | | °C |
| Thermal Shutdown Hysteresis | $T_{SHDNHY}$ | | | 10 | | °C |

**Note 3:** All Electrical Specifications are 100% production tested at $T_A$ = +25°C. Specifications over the operating temperature range are guaranteed by design and characterization

## Typical Operating Characteristics

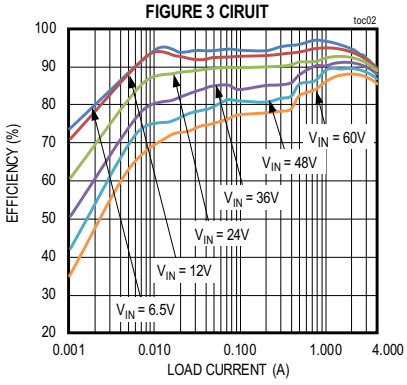
($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $V_{SGND}$ = $V_{PGND}$ = 0V, $C_{IN}$ = 2 x 4.7µF, $C_{VCC}$ = 2.2µF, $C_{BST}$ = 0.1µF, $C_{SS}$ = 5600pF, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C. All voltages are referenced to PGND, unless otherwise noted.)

**EFFICIENCY vs. LOAD CURRENT**
**FIGURE 3 CIRUIT**



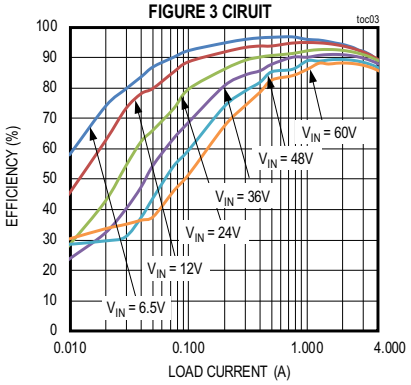

CONDITIONS: 5V OUTPUT, PWM MODE, $f_{SW}$ = 350kHz

**EFFICIENCY vs. LOAD CURRENT**
**FIGURE 3 CIRUIT**



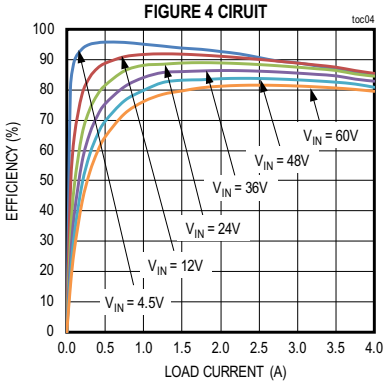

CONDITIONS: 5V OUTPUT, PFM MODE, $f_{SW}$ = 350kHz

**EFFICIENCY vs. LOAD CURRENT**
**FIGURE 3 CIRUIT**



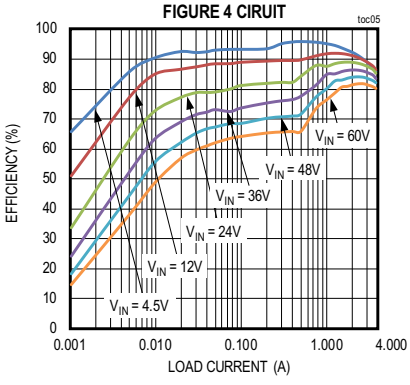

CONDITIONS: 5V OUTPUT, DCM MODE, $f_{SW}$ = 350kHz

**EFFICIENCY vs. LOAD CURRENT**
**FIGURE 4 CIRUIT**



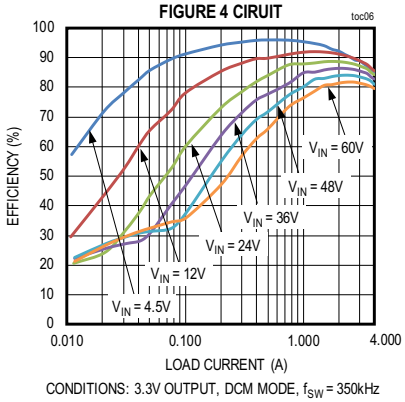

CONDITIONS: 3.3V OUTPUT, PWM MODE, $f_{SW}$ = 350kHz

**EFFICIENCY vs. LOAD CURRENT**
**FIGURE 4 CIRUIT**



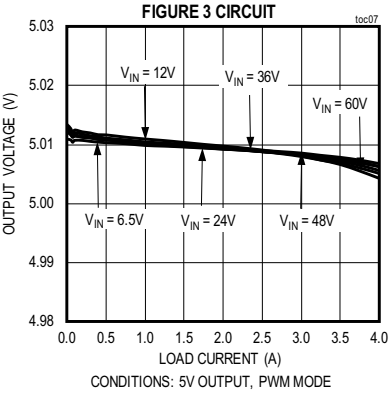

CONDITIONS: 3.3V OUTPUT, PFM MODE, $f_{SW}$ = 350kHz

**EFFICIENCY vs. LOAD CURRENT**
**FIGURE 4 CIRUIT**




CONDITIONS: 3.3V OUTPUT, DCM MODE, $f_{SW}$ = 350kHz

**LOAD AND LINE REGULATION**
**FIGURE 3 CIRCUIT**

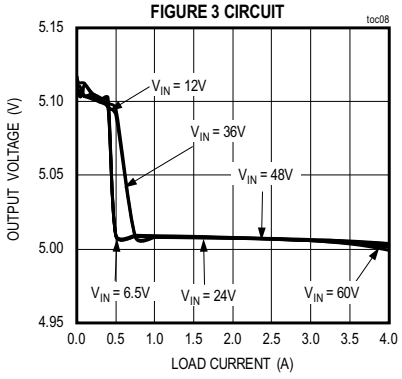



CONDITIONS: 5V OUTPUT, PWM MODE

## Typical Operating Characteristics (continued)

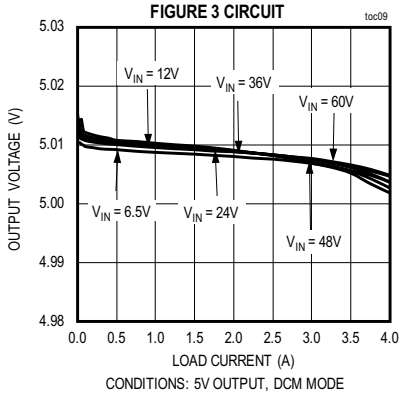
($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $V_{SGND}$ = $V_{PGND}$ = 0V, $C_{IN}$ = 2 x 4.7µF, $C_{VCC}$ = 2.2µF, $C_{BST}$ = 0.1µF, $C_{SS}$ = 5600pF, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C. All voltages are referenced to PGND, unless otherwise noted.)

LOAD AND LINE REGULATION
FIGURE 3 CIRCUIT



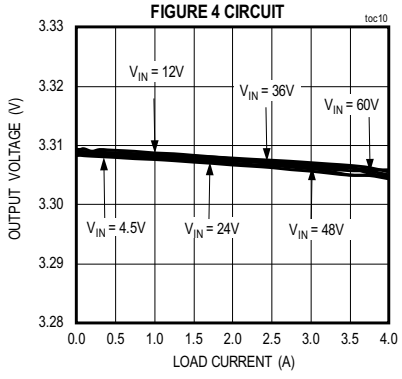

CONDITIONS: 5V OUTPUT, PFM MODE

LOAD AND LINE REGULATION
FIGURE 3 CIRCUIT



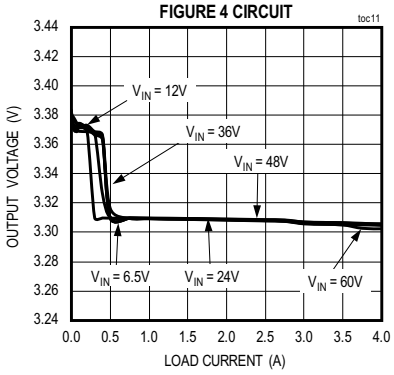

CONDITIONS: 5V OUTPUT, DCM MODE

LOAD AND LINE REGULATION
FIGURE 4 CIRCUIT



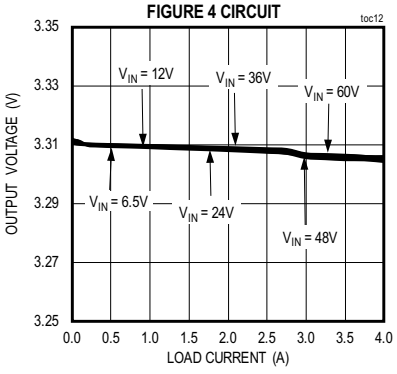

CONDITIONS: 3.3V OUTPUT, PWM MODE

LOAD AND LINE REGULATION
FIGURE 4 CIRCUIT



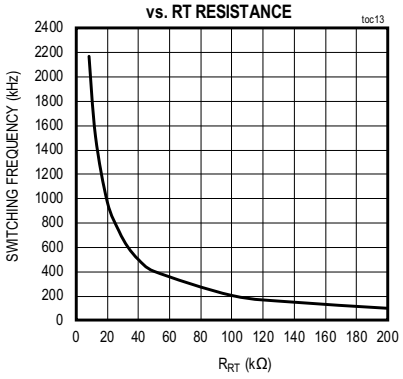

CONDITIONS: 3.3V OUTPUT, PFM MODE

LOAD AND LINE REGULATION
FIGURE 4 CIRCUIT

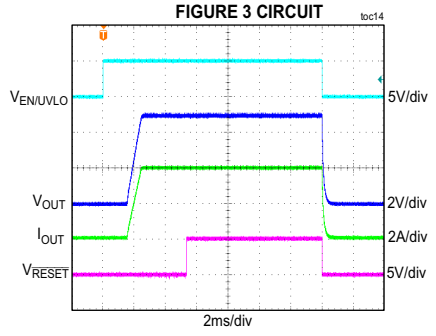



CONDITIONS: 3.3V OUTPUT, DCM MODE

SWITCHING FREQUENCY
vs. RT RESISTANCE




SOFT-START/SHUTDOWN THROUGH EN/UVLO
FIGURE 3 CIRCUIT

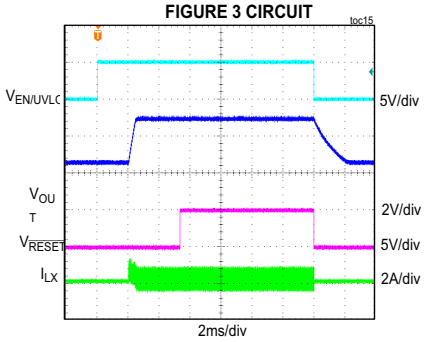



CONDITIONS: 5V OUTPUT, PWM MODE, 1.25Ω LOAD
$\overline{RESET}$ IS PULLED UP TO $V_{CC}$ WITH A 10kΩ RESISTOR

## Typical Operating Characteristics (continued)

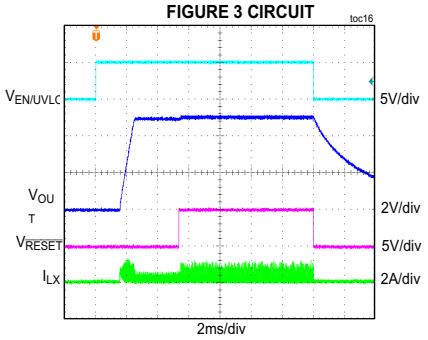
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**SOFT-START WITH PREBIAS VOLTAGE OF 2.5V**
**FIGURE 3 CIRCUIT**



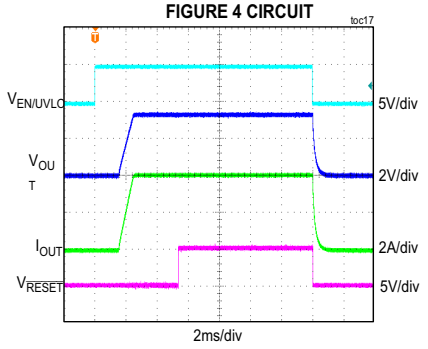

CONDITIONS: 5V OUTPUT, PWM MODE, 250Ω LOAD
$\overline{RESET}$ IS PULLED UP TO $V_{CC}$ WITH A 10kΩ RESISTOR

**SOFT-START/SHUTDOWN THROUGH EN/UVLO**
**FIGURE 3 CIRCUIT**



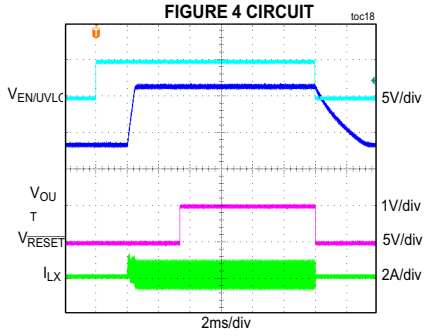

CONDITIONS: 5V OUTPUT, PFM MODE, 250Ω LOAD
$\overline{RESET}$ IS PULLED UP TO $V_{CC}$ WITH A 10kΩ RESISTOR

**SOFT-START/SHUTDOWN THROUGH EN/UVLO**
**FIGURE 4 CIRCUIT**



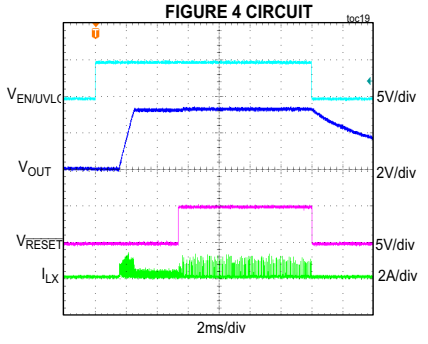

CONDITIONS: 3.3V OUTPUT, PWM MODE, 0.825Ω LOAD
$\overline{RESET}$ IS PULLED UP TO $V_{CC}$ WITH A 10kΩ RESISTOR

**SOFT-START WITH PREBIAS VOLTAGE OF 1.65V**
**FIGURE 4 CIRCUIT**



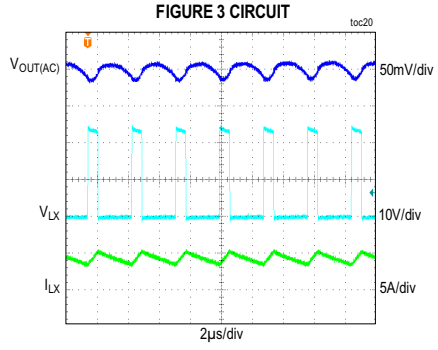

CONDITIONS: 3.3V OUTPUT, PWM MODE, 165Ω LOAD
$\overline{RESET}$ IS PULLED UP TO $V_{CC}$ WITH A 10kΩ RESISTOR

**SOFT-START/SHUTDOWN THROUGH EN/UVLO**
**FIGURE 4 CIRCUIT**




CONDITIONS: 3.3V OUTPUT, PFM MODE, 165Ω LOAD
$\overline{RESET}$ IS PULLED UP TO $V_{CC}$ WITH A 10kΩ RESISTOR

**STEADY STATE PERFORMANCE**
**FIGURE 3 CIRCUIT**

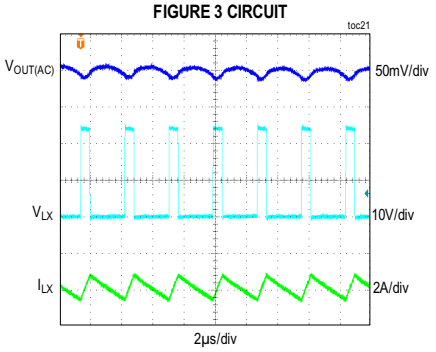



CONDITIONS: 5V OUTPUT, PWM MODE, 4A LOAD

## Typical Operating Characteristics (continued)

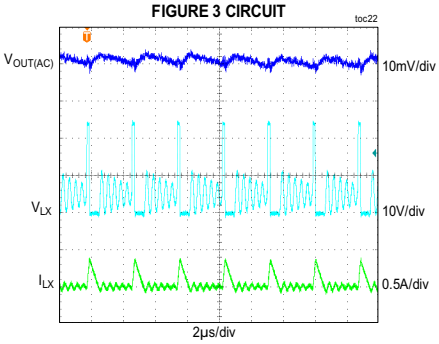
($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $V_{SGND}$ = $V_{PGND}$ = 0V, $C_{IN}$ = 2 x 4.7µF, $C_{VCC}$ = 2.2µF, $C_{BST}$ = 0.1µF, $C_{SS}$ = 5600pF, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C. All voltages are referenced to PGND, unless otherwise noted.)

STEADY STATE PERFORMANCE
FIGURE 3 CIRCUIT



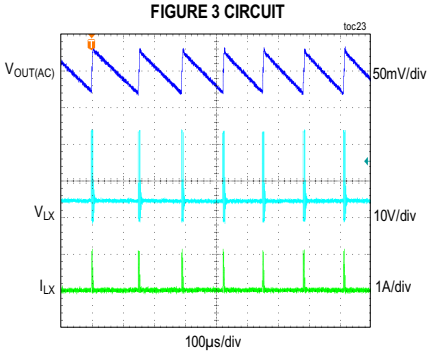

CONDITIONS: 5V OUTPUT, PWM MODE, NO LOAD

STEADY STATE PERFORMANCE
FIGURE 3 CIRCUIT



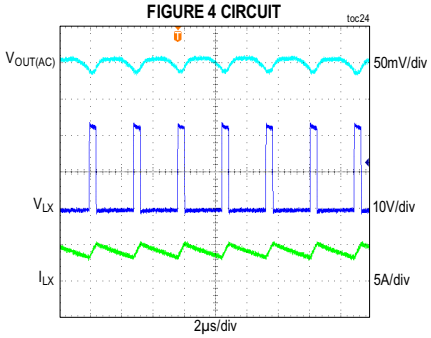

CONDITIONS: 5V OUTPUT, DCM MODE, 40mA LOAD

STEADY STATE PERFORMANCE
FIGURE 3 CIRCUIT



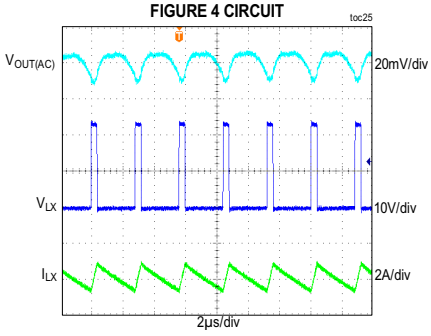

CONDITIONS: 5V OUTPUT, PFM MODE, 20mA LOAD

STEADY STATE PERFORMANCE
FIGURE 4 CIRCUIT



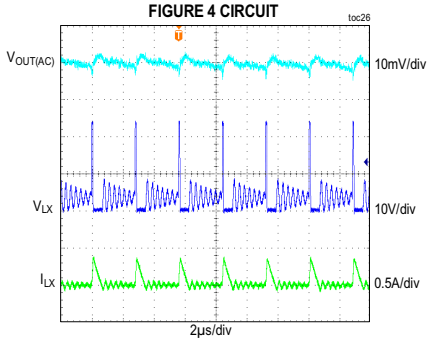

CONDITIONS: 3.3V OUTPUT, PWM MODE, 4A LOAD

STEADY STATE PERFORMANCE
FIGURE 4 CIRCUIT



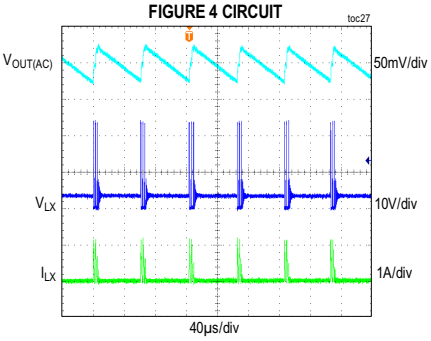

CONDITIONS: 3.3V OUTPUT, PWM MODE, NO LOAD

STEADY-STATE PERFORMANCE
FIGURE 4 CIRCUIT




CONDITIONS: 3.3V OUTPUT, DCM MODE, 40mA LOAD

STEADY-STATE PERFORMANCE
FIGURE 4 CIRCUIT

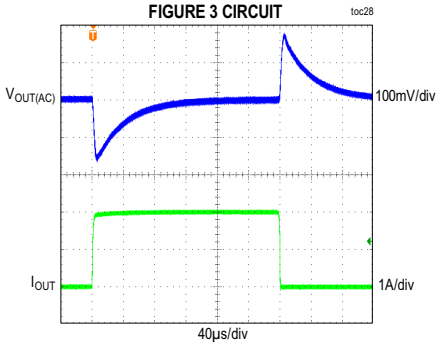



CONDITIONS: 3.3V OUTPUT, PFM MODE, 20mA LOAD

## Typical Operating Characteristics (continued)

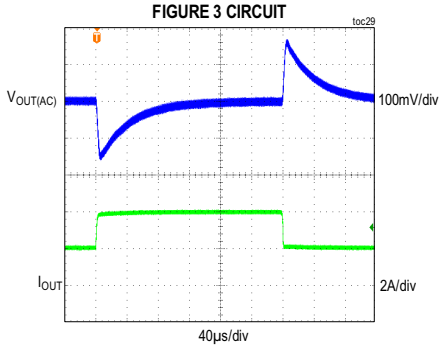
($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $V_{SGND}$ = $V_{PGND}$ = 0V, $C_{IN}$ = 2 x 4.7µF, $C_{VCC}$ = 2.2µF, $C_{BST}$ = 0.1µF, $C_{SS}$ = 5600pF, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C. All voltages are referenced to PGND, unless otherwise noted.)

**LOAD TRANSIENT BETWEEN 0A AND 2A**
**FIGURE 3 CIRCUIT**



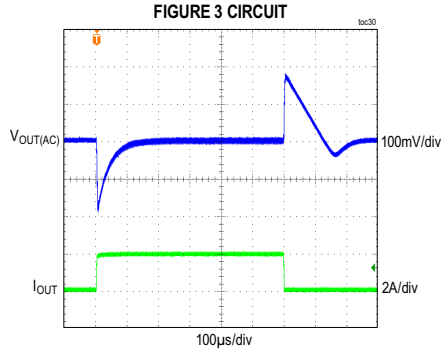

CONDITIONS: 5V OUTPUT, PWM MODE

**LOAD TRANSIENT BETWEEN 2A AND 4A**
**FIGURE 3 CIRCUIT**



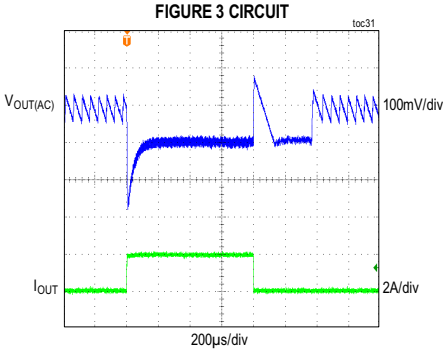

CONDITIONS: 5V OUTPUT, PWM MODE

**LOAD TRANSIENT BETWEEN 80mA AND 2A**
**FIGURE 3 CIRCUIT**



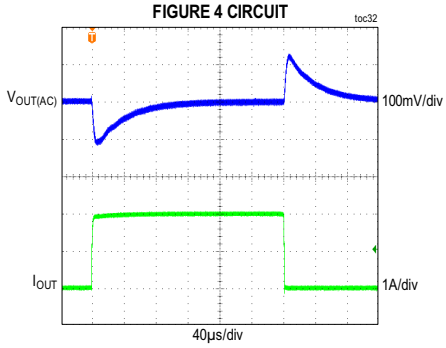

CONDITIONS: 5V OUTPUT, DCM MODE

**LOAD TRANSIENT BETWEEN 50mA AND 2A**
**FIGURE 3 CIRCUIT**



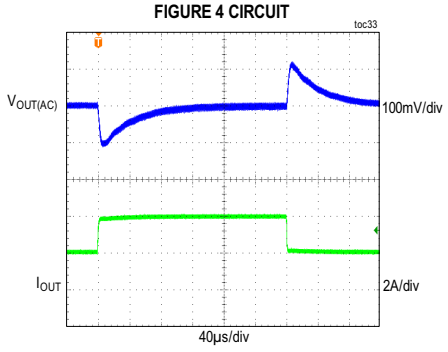

CONDITIONS: 5V OUTPUT, PFM MODE

**LOAD TRANSIENT BETWEEN 0A AND 2A**
**FIGURE 4 CIRCUIT**




CONDITIONS: 3.3V OUTPUT, PWM MODE

**LOAD TRANSIENT BETWEEN 2A AND 4A**
**FIGURE 4 CIRCUIT**

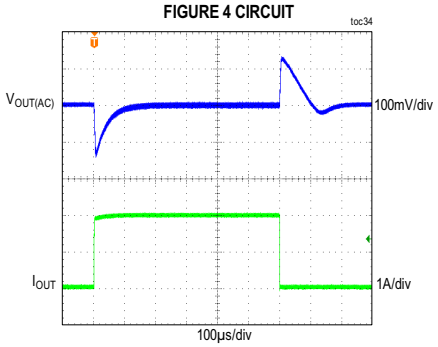



CONDITIONS: 3.3V OUTPUT, PWM MODE

## Typical Operating Characteristics (continued)

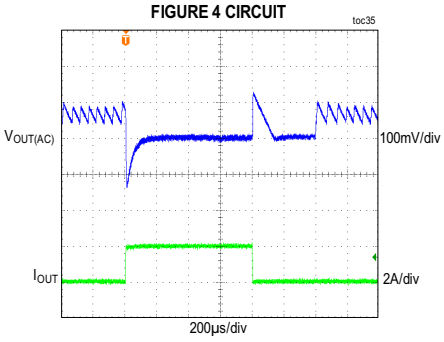
($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $V_{SGND}$ = $V_{PGND}$ = 0V, $C_{IN}$ = 2 x 4.7µF, $C_{VCC}$ = 2.2µF, $C_{BST}$ = 0.1µF, $C_{SS}$ = 5600pF, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C. All voltages are referenced to PGND, unless otherwise noted.)

**LOAD TRANSIENT BETWEEN 80mA AND 2A**
**FIGURE 4 CIRCUIT**



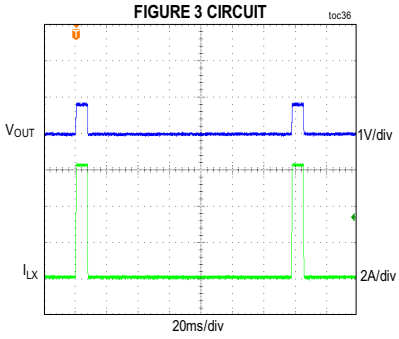

CONDITIONS: 3.3V OUTPUT, DCM MODE

**LOAD TRANSIENT BETWEEN 50mA AND 2A**
**FIGURE 4 CIRCUIT**



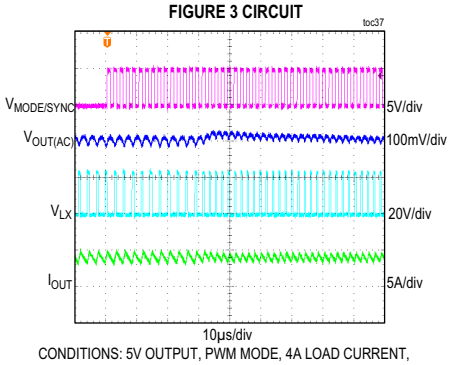

CONDITIONS: 3.3V OUTPUT, PFM MODE

**OVERLOAD PROTECTION**
**FIGURE 3 CIRCUIT**



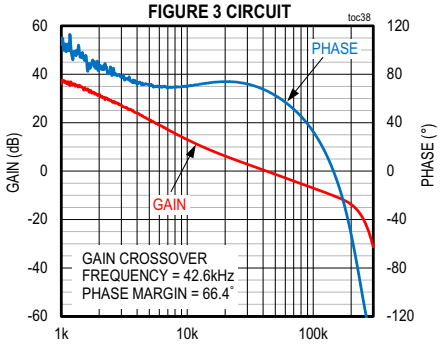

CONDITIONS: 5V OUTPUT, PWM MODE

**EXTERNAL CLOCK SYNCHRONIZATION**
**FIGURE 3 CIRCUIT**



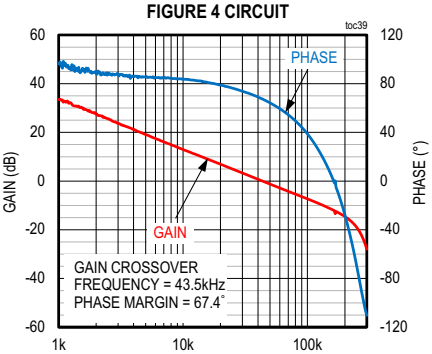

CONDITIONS: 5V OUTPUT, PWM MODE, 4A LOAD CURRENT, $f_{SW}$ = 350kHz, EXTERNAL CLOCK FREQUENCY = 490kHz

**BODE PLOT**
**FIGURE 3 CIRCUIT**



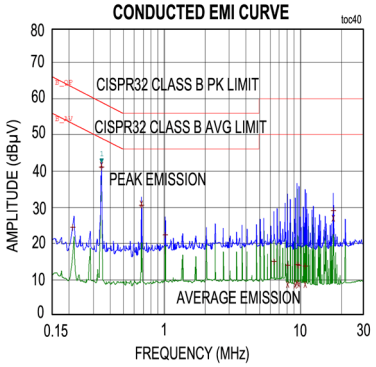

CONDITIONS: 5V OUTPUT, 1.25Ω LOAD

**BODE PLOT**
**FIGURE 4 CIRCUIT**



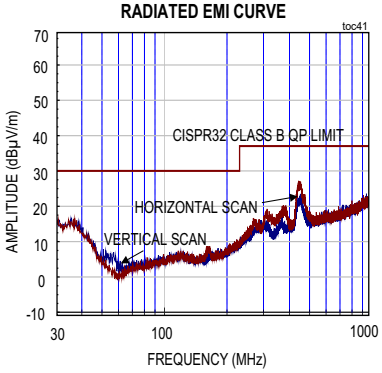

CONDITIONS: 3.3V OUTPUT, 0.825Ω LOAD

**MAX17576, 5V OUTPUT, 4A LOAD CURRENT**
**CONDUCTED EMI CURVE**



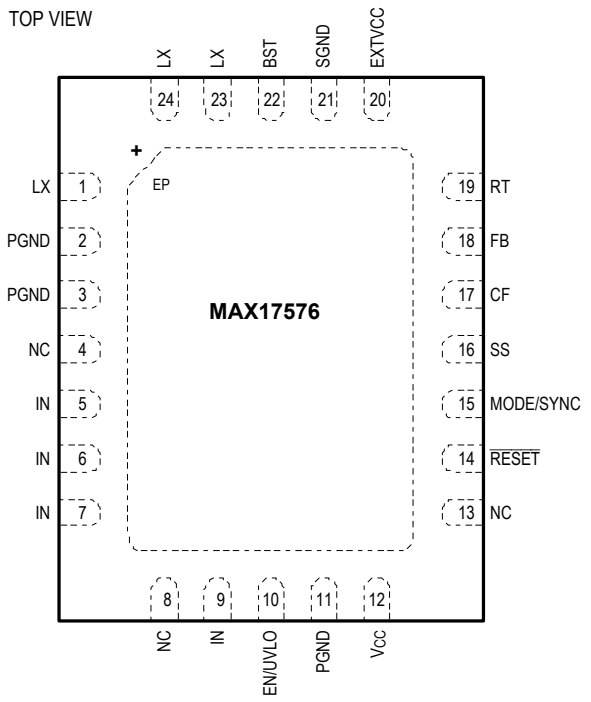

TESTED ON MAX17576EVKITB# WITH CIN7 = CIN9 = 4.7µF/100V/X7R/1206, L1 = 22µH

**MAX17576, 5V OUTPUT, 4A LOAD CURRENT**
**RADIATED EMI CURVE**




TESTED ON MAX17576EVKITB# WITH CIN7 = CIN9 = OPEN, L1 = SHORT

## Pin Configuration




**24-PIN TQFN (4mm × 5mm)**

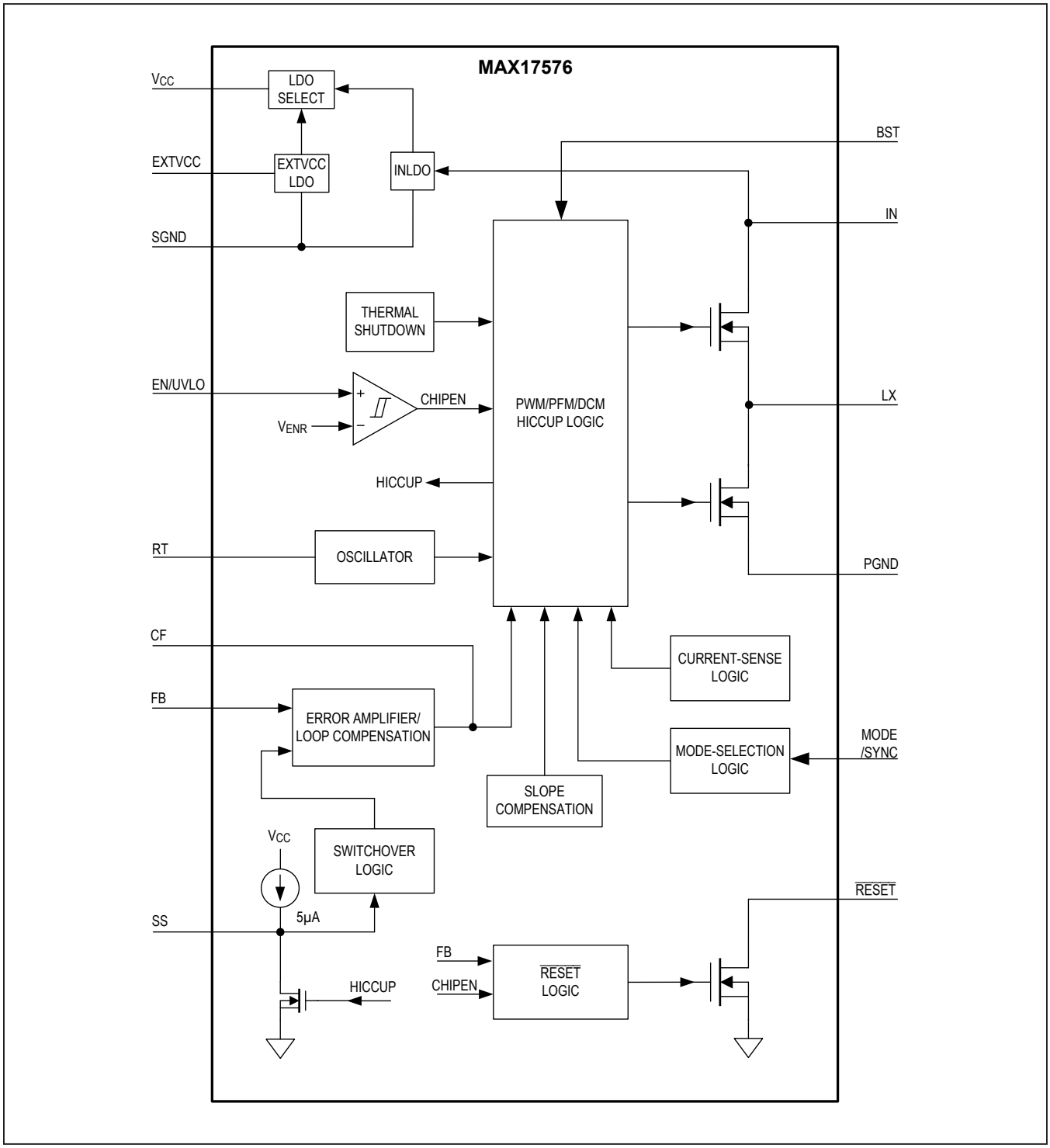
## Pin Description

| NAME | PIN | FUNCTION |
|---|---|---|
| 1, 23, 24 | LX | Switching Node Pins. Connect LX pins to the switching side of the inductor. |
| 2, 3, 11 | PGND | Power Ground Pins of the Converter. Connect externally to the power ground plane. Connect the SGND and PGND pins together at the ground return path of the $V_{CC}$ bypass capacitor. Refer to the *MAX17576 Evaluation Kit* data sheet for a layout example |
| 4, 8, 13 | NC | No Connect. Keep these pins open. |
| 5–7, 9 | IN | Power-Supply Input Pins. The input supply range is from 4.5V to 60V. Connect the IN pins together. Decouple to PGND with 2 x 4.7µF capacitors; place the capacitors close to the IN and PGND pins. Refer to the *MAX17576 EV kit data sheet* for a layout example. |

## Pin Description (continued)

| NAME | PIN | FUNCTION |
|---|---|---|
| 10 | EN/UVLO | Enable/Undervoltage Lockout Pin. Drive EN/UVLO high to enable the output. Connect to the center of the resistor-divider between IN and SGND to set the input voltage at which the part turns on. Connect to IN pins for always-on operation. Pull lower than $V_{ENF}$ for disabling the converter. |
| 12 | $V_{CC}$ | 5V LDO Output. Bypass $V_{CC}$ with 2.2µF ceramic capacitor to SGND. LDO does not support the external loading on $V_{CC}$. |
| 14 | $\overline{\text{RESET}}$ | Open-Drain $\overline{\text{RESET}}$ Output. The $\overline{\text{RESET}}$ output is driven low if FB drops below 92% of its set value. $\overline{\text{RESET}}$ goes high 1024 cycles after FB rises above 95% of its set value. |
| 15 | MODE/ SYNC | Mode Selection and External Clock Synchronization Input. MODE/SYNC Configures the MAX17576 to Operate either in PWM, PFM or DCM Modes of Operation. Leave MODE/SYNC unconnected for PFM operation (pulse skipping at light loads). Connect MODE/SYNC to SGND for constant-frequency PWM operation at all loads. Connect MODE/SYNC to $V_{CC}$ for DCM operation.The device can be synchronized to an external clock using this pin. See the *Mode Selection and External Frequency Synchronization (MODE/SYNC)* section for more details. |
| 16 | SS | Soft-Start Input. Connect a capacitor from SS to SGND to set the soft-start time. |
| 17 | CF | Internal Compensation Node. At switching frequencies lower than 500kHz, connect a capacitor from CF to FB. Leave CF open if switching frequency is equal or more than 500kHz. |
| 18 | FB | Feedback Input. Connect FB to the center tap of an external resistor-divider from the output to SGND to set the output voltage. See the *Adjusting Output Voltage* section for more details. |
| 19 | RT | Switching Frequency Programming Input. Connect a resistor from RT to SGND to set the regulator's switching frequency between 100kHz and 2.2MHz. Leave RT open for the default 500kHz frequency. See the *Switching Frequency Selection (RT)* section for more details. |
| 20 | EXTVCC | External Power Supply Input for the Internal LDO. Applying a voltage between 4.84V and 24V at EXTVCC pin will bypass the internal LDO and improve efficiency. Add a local bypassing capacitor of 0.1µF on the EXTVCC pin to SGND. Also, add a 4.7Ω resistor from the buck converter output node to the EXTVCC pin to limit $V_{CC}$ bypass capacitor discharge current and to protect the EXTVCC pin from reaching its absolute maximum rating (-0.3V) during output short-circuit condition. Connect the EXTVCC pin to SGND when the pin is not being used. |
| 21 | SGND | Analog Ground. |
| 22 | BST | Boost Flying Capacitor. Connect a 0.1µF ceramic capacitor between BST and LX. |
| — | EP | Exposed Pad. Always connect EP to the SGND pin of the IC. Also, connect EP to a large SGND plane with several thermal vias for best thermal performance. Refer to the MAX17576 EV kit data sheet for an example of the correct method for EP connection and thermal vias. |

## Functional (or Block) Diagram



## Detailed Description

The MAX17576, high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4.5V to 60V input. The converter can deliver up to 4A current. Output voltage is programmable from 0.9V up to 90% of $V_{IN}$. The feedback voltage regulation accuracy over -40°C to +125°C is ±0.9%.

The device features a peak-current-mode control architecture. An internal transconductance error amplifier produces an integrated error voltage at an internal node, which sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the high-side MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side MOSFET's on-time, the inductor current ramps up. During the second half of the switching cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as its current ramps down and provides current to the output.

The device can operate either in the pulse-width modulation (PWM), pulse-frequency modulation (PFM), or discontinuous-conduction mode (DCM) control schemes. A programmable soft-start feature allows users to reduce input inrush current. The device also incorporates an output enable/undervoltage lockout pin (EN/UVLO) that allows the user to turn on the part at the desired input voltage level. An open-drain $\overline{RESET}$ pin provides a delayed power-good signal to the system upon achieving successful regulation of the output voltage.

### Mode Selection and External Frequency Synchronization (MODE/SYNC)

The logic state of the MODE/SYNC pin is latched when $V_{CC}$ and EN/UVLO voltages exceed the respective UVLO rising thresholds and all internal voltages are ready to allow LX switching. If the MODE/SYNC pin is open at power-up, the device operates in PFM mode at light loads. If the MODE/SYNC pin is grounded at power-up, the device operates in constant-frequency PWM mode at all loads. Finally, if the MODE/SYNC pin is connected to $V_{CC}$ at power-up, the device operates in constant-frequency DCM mode at light loads. State changes on the MODE/SYNC pin are ignored during normal operation.

The internal oscillator of the MAX17576 can be synchronized to an external clock signal on the MODE/SYNC pin. The external synchronization clock frequency must be between 1.1 x $f_{SW}$ and 1.4 x $f_{SW}$, where $f_{SW}$ is the frequency programmed by the RT resistor. When an external clock is applied to MODE/SYNC pin, the internal oscillator frequency changes to external clock frequency (from original frequency based on RT setting) after detecting 16 external clock edges. The converter will operate in PWM mode during synchronization operation.

When the external clock is applied on-fly then the mode of operation will change to PWM from the initial state of PFM/DCM/PWM. When the external clock is removed on-fly then the internal oscillator frequency changes to the RT set frequency and the converter will still continue to operate in PWM mode. The minimum external clock pulse-width high should be greater than 50ns. See the MODE/SYNC section in the *Electrical Characteristics* table for details.

### PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation at all loads, and is useful in applications sensitive to switching frequency. However, the PWM mode of operation gives lower efficiency at light loads compared to PFM and DCM modes of operation.

### PFM Mode Operation

PFM mode of operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak of $I_{PFM}$ (1A typ) every clock cycle until the output rises to 102.3% of the nominal voltage. Once the output reaches 102.3% of the nominal voltage, both the high-side and low-side FETs are turned off and the device enters hibernate operation until the load discharges the output to 101.1% of the nominal voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101.1% of the nominal voltage, the device comes out of hibernate operation, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches 102.3% of the nominal output voltage. The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply. The trade-off is that the output-voltage ripple is higher compared to PWM or DCM modes of operation and switching frequency is not constant at light loads.

### DCM Mode Operation

DCM mode of operation features constant frequency operation down to lighter loads than PFM mode, by not skipping pulses but only disabling negative inductor current at light loads. DCM operation offers efficiency performance that lies between PWM and PFM modes at light loads. The output-voltage ripple in DCM mode is comparable to PWM mode and relatively lower compared to PFM mode at light loads.

### Linear Regulator ($V_{CC}$ and EXTVCC)

The MAX17576 has two internal LDO (Low Dropout) regulators which powers $V_{CC}$. One LDO is powered from input supply (IN) (INLDO) and the other LDO is powered from EXTVCC (EXTVCC LDO). Only one of the two LDOs is in operation at a time, depending on the voltage levels present at EXTVCC pin. If EXTVCC voltage is greater than $V_{EXTVCC}$ (4.7V typ), $V_{CC}$ is powered from EXTVCC. If EXTVCC is lower than $V_{EXTVCC}$, $V_{CC}$ is powered from input supply (IN). Powering $V_{CC}$ from EXTVCC increases efficiency at higher input voltages. EXTVCC voltage should not exceed 24V.

Typical $V_{CC}$ output voltage is 5V. Bypass $V_{CC}$ to GND with a 2.2µF ceramic capacitor. $V_{CC}$ powers the internal blocks and the low-side MOSFET driver and recharges the external bootstrap capacitor. Both INLDO and EXTVCC LDO can source up to 40mA for bias requirements. The MAX17576 employs an undervoltage lockout circuit that forces both the regulators off when $V_{CC}$ falls below $V_{CC-UVF}$. The regulators can be immediately enabled again when $V_{CC}$ goes above $V_{CC-UVR}$. The 400mV UVLO hysteresis prevents chattering on power-up/power-down.

Add a local bypassing capacitor of 0.1µF on the EXTVCC pin to SGND. Also, add a 4.7Ω resistor from the buck converter output node to the EXTVCC pin to limit $V_{CC}$ bypass capacitor discharge current and to protect the EXTVCC pin from reaching its absolute maximum rating (-0.3V) during output short-circuit condition. In applications where the buck converter output is connected to EXTVCC pin, if the output is shorted to ground then the transfer from EXTVCC LDO to INLDO happens seamlessly without any impact on the normal functionality. Connect the EXTVCC pin to SGND when the pin is not used.

### Switching Frequency Selection (RT)

The switching frequency of the device can be programmed from 100kHz to 2.2MHz by using a resistor connected from the RT pin to SGND. The switching frequency ($f_{SW}$) is related to the resistor connected at the RT pin ($R_{RT}$) by the following equation:

$$R_{RT} = \frac{21 \times 10^3}{f_{SW}} - 1.7$$

where $R_{RT}$ is in kΩ and $f_{SW}$ is in kHz. Leaving the RT pin open causes the device to operate at the default switching frequency of 500kHz. See Table 1 for RT resistor values for a few common switching frequencies.

### Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + \left(I_{OUT(MAX)} \times \left(R_{DCR(MAX)} + R_{DS_ONL(MAX)}\right)\right)}{1 - \left(f_{SW(MAX)} \times t_{OFF_MIN(MAX)}\right)} + \left(I_{OUT(MAX)} \times \left(R_{DS_ONH(MAX)} - R_{DS_ONL(MAX)}\right)\right)$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON_MIN(MAX)}}$$

where:

$V_{OUT}$ = Steady-state output voltage
$I_{OUT(MAX)}$ = Maximum load current
$R_{DCR(MAX)}$ = Worst-case DC resistance of the inductor
$f_{SW(MAX)}$ = Maximum switching frequency
$t_{OFF_MIN(MAX)}$ = Worst-case minimum switch off-time (160ns)
$t_{ON_MIN(MAX)}$ = Worst-case minimum switch on-time (80ns)
$R_{DS_ONH(MAX)}$ = Worst-case on-state resistances and high-side internal MOSFET
$R_{DS_ONL(MAX)}$ = Worst-case on-state resistances and low-side external MOSFET

## Table 1. Switching Frequency vs. RT Resistor

| SWITCHING FREQUENCY (kHz) | RT RESISTOR (kΩ) |
|---|---|
| 500 | OPEN |
| 100 | 210 |
| 200 | 102 |
| 350 | 59 |
| 1000 | 19.1 |
| 2200 | 8.06 |

### Overcurrent Protection/Hiccup Mode

The device is provided with a robust overcurrent protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of $I_{PEAK-LIMIT}$ 6.5A (typ). A runaway current limit on the high-side switch current at $I_{RUNAWAY-LIMIT}$ 7.2A (typ) protects the device under high input voltage, short-circuit conditions when there is insufficient output voltage available to restore the inductor current that was built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. In addition, if, due to a fault condition, feedback voltage drops to $V_{FB-HICF}$ any time after soft-start is complete, and hiccup mode is triggered. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32,768 clock cycles of half the programmed switching frequency. Once the hiccup timeout period expires, soft-start is attempted again. Note that when soft-start is attempted under overload condition, if feedback voltage does not exceed $V_{FB-HICF}$, the device switches at half the programmed switching frequency for the time duration of the programmed soft-start time and 1024 clock cycles. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

### $\overline{\text{RESET}}$ Output

The device includes a $\overline{\text{RESET}}$ comparator to monitor the status of the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high impedance) 1024 switching cycles after the regulator output increases above $V_{FB-OKR}$ (95% typ) of the designed nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops to below $V_{FB-OKF}$ (92% typ) of the set nominal output regulated voltage. $\overline{\text{RESET}}$ also goes low during thermal shutdown or when the EN/UVLO pin goes below $V_{ENF}$.

### Prebiased Output

When the MAX17576 starts into a prebiased output, both the high-side and the low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

### Thermal Shutdown Protection

Thermal shutdown protection limits total power dissipation in the device. When the junction temperature of the device exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The MAX17576 turns on with soft-start after the junction temperature reduces by 10°C. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown protection in normal operation.

## Application Information

### Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement ($I_{RMS}$) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ is the maximum load current. $I_{RMS}$ has a maximum value when the input voltage equals twice the output voltage ($V_{IN}$ = 2 x $V_{OUT}$), so $I_{RMS(MAX)}$ = $I_{OUT(MAX)}/2$. Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1-D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where D = $V_{OUT}/V_{IN}$ is the duty ratio of the converter, $f_{SW}$ is the switching frequency, $\Delta V_{IN}$ is the allowable input voltage ripple, and η is the efficiency.

In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

### Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current ($I_{SAT}$) and DC resistance ($R_{DCR}$). The switching frequency and output voltage determine the inductor value as follows:

$$L = \frac{0.6 \times V_{OUT}}{f_{SW}}$$

Where $V_{OUT}$ and $f_{SW}$ are nominal values and $f_{SW}$ is in Hz. Select an inductor whose value is nearest to the value calculated by the previous formula.

Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating ($I_{SAT}$) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value of $I_{PEAK-LIMIT}$ 6.5A (typ).

### Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are usually sized to support a step load of 50% of the maximum output current in the application, so the output voltage deviation is contained to 3% of the output voltage change. The minimum required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \frac{0.35}{f_C}$$

where $I_{STEP}$ is the load current step, $t_{RESPONSE}$ is the response time of the controller, $\Delta V_{OUT}$ is the allowable output-voltage deviation, $f_C$ is the target closed-loop crossover frequency, and $f_{SW}$ is the switching frequency. Select $f_C$ to be 1/9th of $f_{SW}$ if the switching frequency is less than or equal to 500kHz. If the switching frequency is more than 500kHz, select $f_C$ to be 55kHz. Actual derating of ceramic capacitors with DC bias voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

### Soft-Start Capacitor Selection

The device implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time. The selected output capacitance ($C_{SEL}$) and the output voltage ($V_{OUT}$) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 28 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time ($t_{SS}$) is related to the capacitor connected at SS ($C_{SS}$) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-6}}$$

For example, to program a 1ms soft-start time, a 5.6nF capacitor should be connected from the SS pin to GND.

### Setting the Input Undervoltage-Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from IN to SGND. Connect the center node of the divider to EN/UVLO. (see Figure 1) Choose R1 to be 3.3MΩ and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.215}{(V_{INU} - 1.215)}$$

where $V_{INU}$ is the voltage at which the device is required to turn on. Ensure that $V_{INU}$ is higher than 0.8 x $V_{OUT}$ to avoid hiccup during slow power-up (slower than soft-start) and power-down. If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1kΩ is recommended to be placed between the output pin of signal source and the EN/UVLO pin to reduce voltage ringing on the line.

### Loop Compensation

The device is internally loop compensated. However, if the switching frequency is less than 500kHz, connect a 0402 capacitor C12 between the CF pin and the FB pin. Use Table 2 to select the value of C12.

## Table 2. C12 Capacitor Value at Various Switching Frequencies

| SWITCHING FREQUENCY RANGE (kHz) | C12 (pF) |
|---|---|
| 100–150 | 3.9 |
| 151–200 | 2.2 |
| 201–300 | 1 |
| 301–2200 | OPEN |

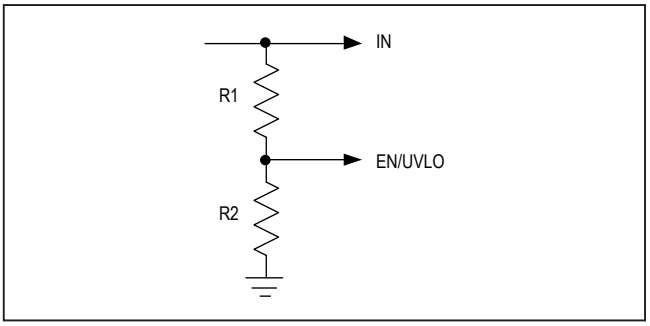



*Figure 1. Setting the Input Undervoltage Lockout*

## Adjusting Output Voltage

Set the output voltage with a resistive voltage-divider connected from the positive terminal of the output capacitor ($V_{OUT}$) to SGND (see Figure 2). Connect the center node of the divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R6 from the output to the FB pin as follows:

$$R6 = \frac{216 \times 10^3}{f_C \times C_{OUT_SEL}}$$

where R6 is in kΩ, crossover frequency $f_C$ is in kHz, $C_{OUT_SEL}$ is the actual derated capacitance of selected output capacitor at DC-bias voltage in µF. Calculate resistor R7 from the FB pin to SGND as follows:

$$R7 = \frac{R6 \times 0.9}{(V_{OUT} - 0.9)}$$

R7 is in kΩ.

## Power Dissipation

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{LOSS} = (P_{OUT} \times (\frac{1}{\eta} - 1)) - \left(I_{OUT}{}^2 \times R_{DCR}\right)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

Where $P_{OUT}$ is the output power, η is the efficiency of the converter and $R_{DCR}$ is the DC resistance of the inductor (see the *Typical Operating Characteristics* for more information on efficiency at typical operating conditions).

For a typical multilayer board, the thermal performance metrics for the package are given below:

$$\theta_{JA} = 24°C / W$$

$$\theta_{JC} = 1.8°C / W$$

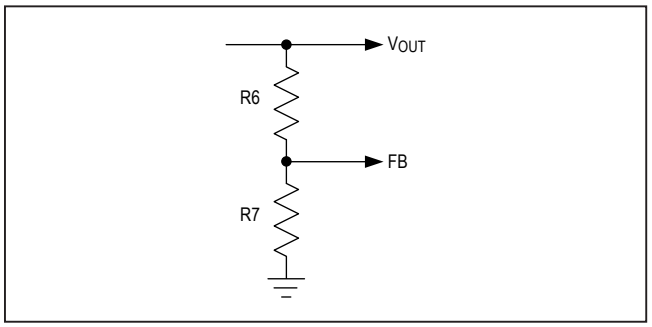



*Figure 2. Adjusting Output Voltage*

The junction temperature of the device can be estimated at any given maximum ambient temperature ($T_{A_MAX}$) from the following equation:

$$T_{J_MAX} = T_{A_MAX} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature ($T_{EP_MAX}$) by using proper heat sinks, then the junction temperature of the device can be estimated at any given maximum ambient temperature as:

$$T_{J_MAX} = T_{EP_MAX} + (\theta_{JC} \times P_{LOSS})$$

Junction temperatures greater than +125°C degrades operating lifetimes.

## PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI.

A ceramic input filter capacitor should be placed close to the IN pins of the IC. This eliminates as much trace inductance effects as possible and gives the IC a cleaner voltage supply. A bypass capacitor for the $V_{CC}$ pin also should be placed close to the pin to reduce effects of trace impedance.

When routing the circuitry around the IC, the analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at a minimum, typically the return terminal of the $V_{CC}$ bypass capacitor. This helps keep the analog ground quiet. The ground plane should be kept continuous/unbroken as far as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity.

PCB layout also affects the thermal performance of the design. A number of thermal throughputs that connect to a large ground plane should be provided under the exposed pad of the part, for efficient heat dissipation.

For a sample layout that ensures first pass success, refer to the MAX17576 evaluation kit layout available at www.maximintegrated.com.

## Typical Application Circuits

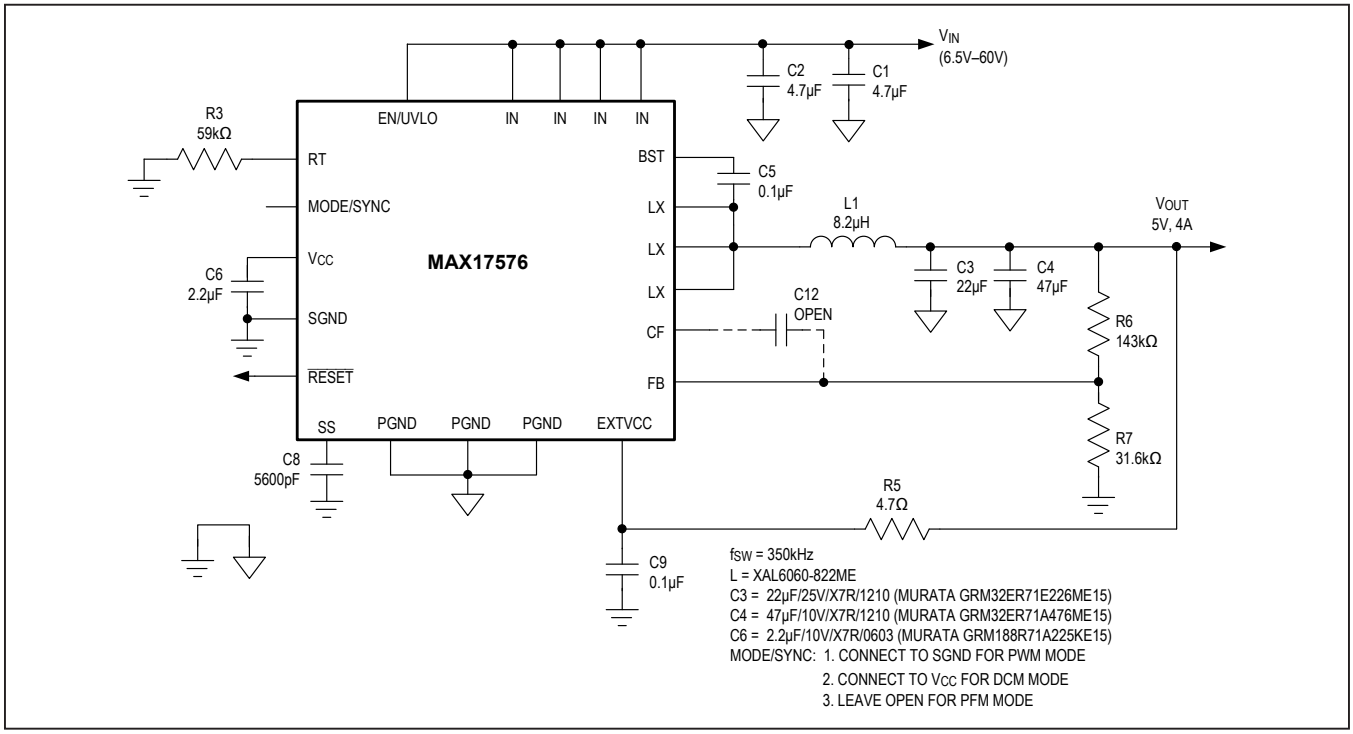



*Figure 3. 5V Output Application Circuit*

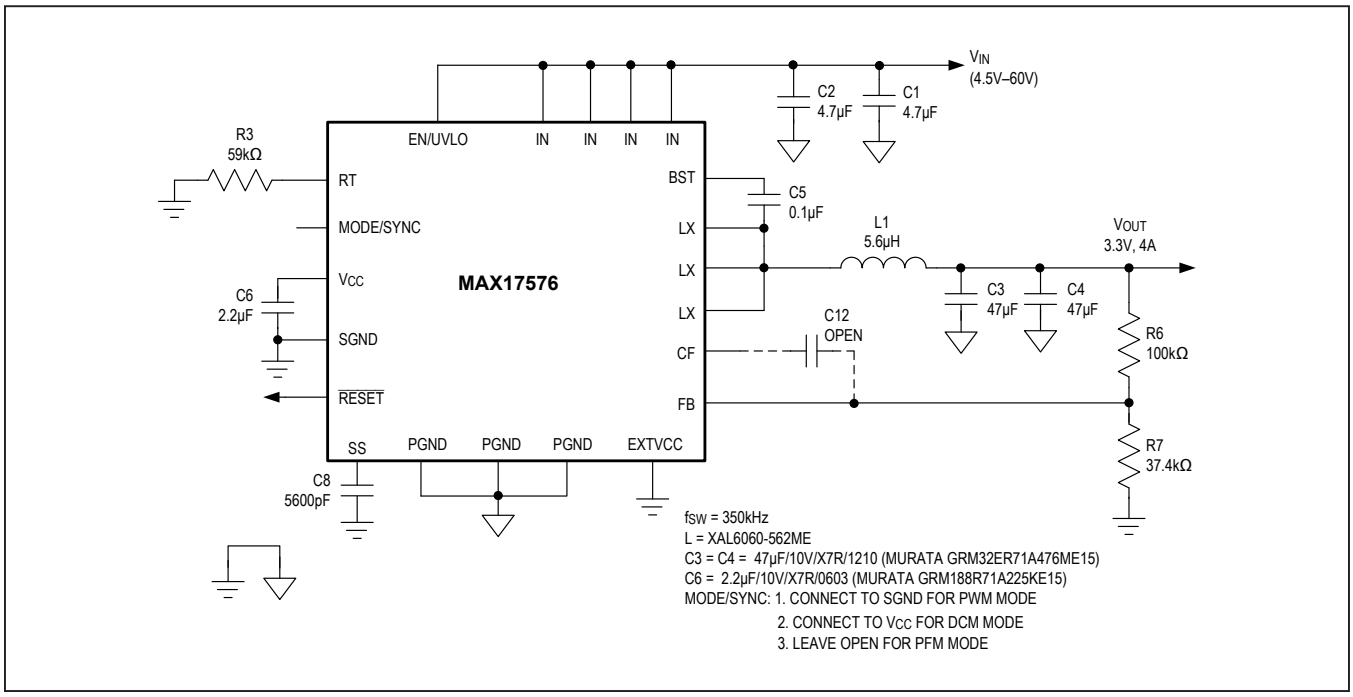



*Figure 4. 3.3V Output Application Circuit*

## Ordering Information

| PART | PIN-PACKAGE | PACKAGE-SIZE |
|---|---|---|
| MAX17576ATG+ | 24-TQFN EP* | 4mm x 5mm |
| MAX17576ATG+T | 24-TQFN EP* | 4mm x 5mm |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*
*T = Tape-and-reel.*
**EP = Exposed pad.*

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 9/18 | Initial release | — |
| 1 | 9/20 | Updated *General Description*, *Benefits and Features, Electrical Characteristics*, *Pin Description, Functional Diagram*, *PFM Mode Operation*, *DCM Mode Operation*, *Linear Regulator ($V_{CC}$ and EXTVCC)*, *Overcurrent Protection/Hiccup Mode*, *$\overline{RESET}$ Output*, *Output Capacitor Selection*, *Soft-Start Capacitor Selection, Setting the Input Undervoltage-Lockout Level,* and *Ordering Information* sections; updated TOC14–TOC19, TOC37–TOC39, and added TOC40–TOC41 | 1, 3–18, 21 |

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

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