MAX17521

60V, 1A, Dual-Output, High-Efficiency, Synchronous Step-Down DC-DC Converter

General Description

The MAX17521 dual-output, high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4.5V to 60V input. The converter can deliver up to 1A at each output. Each output is programmable from 0.9V to 92%V_{IN}. The feedback voltage regulation accuracy over -40°C to +125°C is ±1.7%.

The MAX17521 uses peak-current-mode control. Each output can be operated in the pulse-width modulation (PWM) or pulse-frequency modulation (PFM) control schemes.

The MAX17521 is available in a 24-pin (4mm x 5mm) TQFN package. Simulation models are available.

Applications

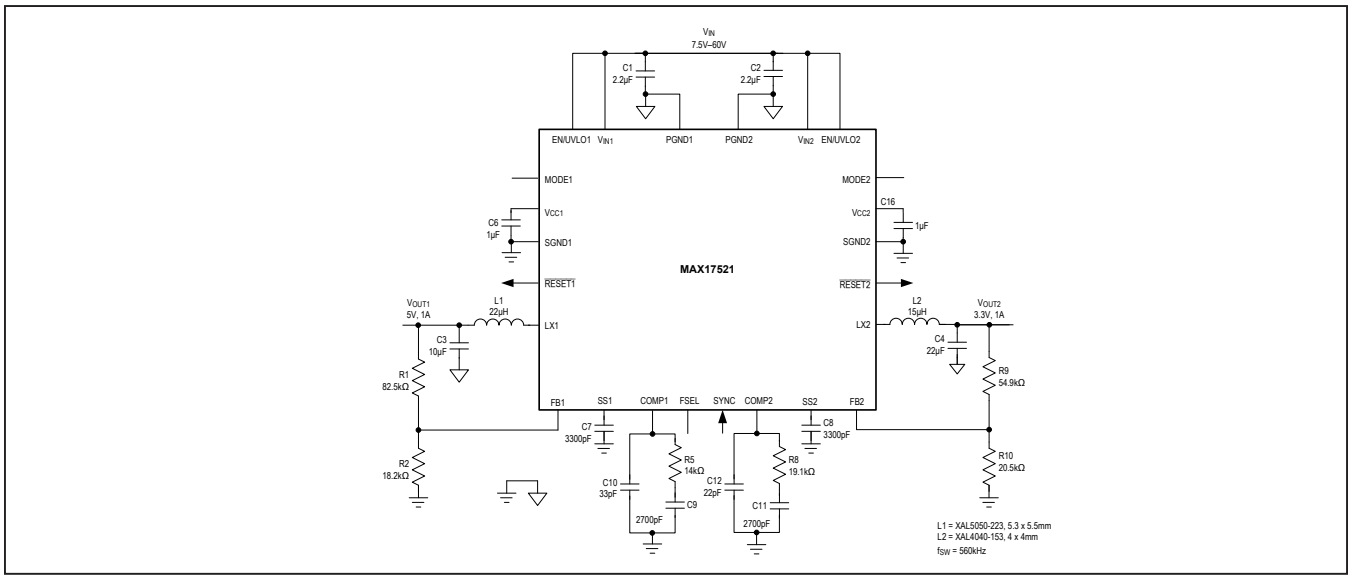
- Industrial Control Power Supplies
- CPU, DSP, or FPGA Power
- Distributed Supply Regulation
- General-Purpose Point of Load

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Reduces External Components and Total Cost
  - No Schottky—Synchronous Operation
  - All-Ceramic Capacitors, Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4.5V to 60V Input
  - Each Output Adjustable From 0.9V to 92%V_{IN}
  - Pin-Selectable 560kHz or 300kHz Switching Frequency
  - Independent Input Voltage Pin for Each Output
- Reduces Power Dissipation
  - Peak Efficiency > 90%
  - PFM Mode Enables Enhanced Light-Load Efficiency
  - 1µA Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Hiccup Mode Overload Protection
  - Adjustable Soft-Start Pin for Each Output
  - Built-In Output Voltage Monitoring with $\overline{\text{RESET}}$ for Each Output
  - Adjustable EN/UVLO Threshold for Each Output
  - Monotonic Startup Into Prebiased Load
  - Overtemperature Protection
  - High Industrial -40°C to +125°C Ambient Operating Temperature Range/-40°C to +150°C Junction Temperature Range

Typical Application Circuit



maxim integrated™

Absolute Maximum Ratings

$V_{IN_}$ to PGND_ ..... -0.3V to +65V
EN/UVLO_ to SGND_ ..... -0.3V to ($V_{IN_}$ + 0.3V)
LX_ to PGND_ ..... -0.3V to ($V_{IN_}$ + 0.3V)
FB_, $\overline{RESET_}$, FSEL, MODE_, COMP_, $V_{CC_}$, SYNC, SS_ to SGND_ ..... -0.3V to +6V
SGND_ to PGND_ ..... -0.3V to +0.3V
LX Total RMS Current ..... ±1.6A
Continuous Power Dissipation (T_A = +70°C) (derate 28.6mW/°C above +70°C) (multilayer board) 2285.7mW
Output Short-Circuit Duration ..... Continuous
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 24-PIN TQFN	
Package Code	T2445+1C
Outline Number	**21-0201**
Land Pattern Number	**90-0083**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	35°C/W
Junction to Case (θ_{JC})	1.8°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

($V_{IN_}$ = +24V, $V_{SGND_}$ = $V_{PGND_}$ = V_{FSEL} = 0V, $C_{IN_}$ = 2.2µF, $C_{VCC_}$ = 1µF, $V_{EN/UVLO_}$ = 1.5V, $C_{SS_}$ = 0.01µF, FB_ = 0.98 x V_{FB-REG}, COMP_ = unconnected, LX_ = unconnected, $\overline{RESET_}$ = unconnected. T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND_, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})							
Input Voltage Range	$V_{IN_}$			4.5		60	V
Input Shutdown Current	I_{IN-SH}	$V_{EN_}$ = 0V, shutdown mode			1	3.5	µA
Input Switching Current	$I_{Q_PFM_}$	$V_{MODE_}$ > 2V			135	260	µA
	$I_{Q_PWM_}$	$V_{MODE_}$ < 0.8V, $V_{COMP_}$ = 0.8V	V_{FSEL} > 2V		5		mA
			V_{FSEL} < 0.8V		3.7		

Electrical Characteristics (continued)

($V_{IN_}$ = +24V, $V_{SGND_}$ = $V_{PGND_}$ = V_{FSEL} = 0V, $C_{IN_}$ = 2.2µF, $C_{VCC_}$ = 1µF, $V_{EN/UVLO_}$ = 1.5V, $C_{SS_}$ = 0.01µF, FB_ = 0.98 x V_{FB-REG}, COMP_ = unconnected, LX_ = unconnected, $\overline{RESET_}$ = unconnected. T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND_, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE/UVLO (EN_)						
EN_ Threshold	V_{EN_R}	$V_{EN_}$ rising	1.19	1.215	1.24	V
	V_{EN_F}	$V_{EN_}$ falling	1.11	1.135	1.16	
	$V_{EN_-TRUESD}$	$V_{EN_}$ falling, true shutdown		0.75		
EN_ Input Leakage Current	$I_{EN_}$	$V_{EN_}$ = V_{IN} = 60V, T_A = +25°C			300	nA
FREQUENCY SELECTOR (FSEL)						
FSEL Threshold	V_{FSELR}	V_{FSEL} low level			0.8	V
	V_{FSELF}	V_{FSEL} high level	2			
FSEL Input Leakage Current	I_{FSEL}	V_{FSEL} = V_{CC}, T_A = +25°C	-2.5		+2.5	µA
MODE SELECTOR (MODE_)						
MODE_ Threshold	V_{MODE_R}	$V_{MODE_}$ low level			1.9	V
	V_{MODE_F}	$V_{MODE_}$ high level	2.5			
MODE_ Input Leakage Current	$I_{MODE_}$	V_{MODE} = V_{CC}, T_A = +25°C			300	nA
LDO ($V_{CC_}$)						
$V_{CC_}$ Output Voltage Range	$V_{VCC_}$	6V < $V_{IN_}$ < 12V, 0mA < $I_{VCC_}$ < 10mA 12V < $V_{IN_}$ < 60V, 0mA < $I_{VCC_}$ < 2mA	4.65	5	5.35	V
$V_{CC_}$ Current Limit	I_{VCC_-MAX}	$V_{CC_}$ = 4.3V, $V_{IN_}$ = 12V	17	40	80	mA
$V_{CC_}$ Dropout	V_{CC_-DO}	$V_{IN_}$ = 4.5V, $I_{VCC_}$ = 5mA	4.1			V
$V_{CC_}$ UVLO	V_{VCC_-UVR}	$V_{CC_}$ rising	3.85	4	4.15	V
	V_{CC_-UVF}	$V_{CC_}$ falling	3.55	3.7	3.85	
POWER MOSFETs						
High-Side_ pMOS On-Resistance	R_{DS_-ONH}	$I_{LX_}$ = 0.5A (sourcing), T_A = +25°C		0.6	0.8	Ω
		$I_{LX_}$ = 0.5A (sourcing), T_A = T_J = +125°C (Note 3)			1.2	
Low-Side_ nMOS On-Resistance	R_{DS_-ONL}	$I_{LX_}$ = 0.5A (sinking), T_A = +25°C		0.2	0.35	Ω
		$I_{LX_}$ = 0.5A (sinking), T_A = T_J = +125°C (Note 3)			0.45	
LX_ Leakage Current	I_{LX_LKG}	$V_{EN_}$ = 0V, T_A = +25°C, $V_{LX_}$ = ($V_{PGND_}$ + 1V) to ($V_{IN_}$ – 1V)			3	µA
SOFT-START (SS_)						
Charging Current_	$I_{SS_}$	$V_{SS_}$ = 0.5V	4.7	5	5.3	µA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB_REG}	MODE_ = SGND_	0.885	0.9	0.915	V
		MODE_ = unconnected		0.915		
FB Input Bias Current	I_{FB}	V_{FB} = 0.9V		15	100	nA

Electrical Characteristics (continued)

($V_{IN_}$ = +24V, $V_{SGND_}$ = $V_{PGND_}$ = V_{FSEL} = 0V, $C_{IN_}$ = 2.2µF, $C_{VCC_}$ = 1µF, $V_{EN/UVLO_}$ = 1.5V, $C_{SS_}$ = 0.01µF, FB_ = 0.98 x V_{FB-REG}, COMP_ = unconnected, LX_ = unconnected, $\overline{RESET_}$ = unconnected. T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND_, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE (V_{OUT})							
Output Voltage Range	V_{OUT}	V_{FSEL} > 2V; no load (Note 3)		0.92		0.92 x V_{IN}	V
		V_{FSEL} < 0.8V; no load (Note 3)		0.92		0.96 x V_{IN}	
TRANSCONDUCTANCE AMPLIFIER (COMP)							
Transconductance	$GM_$	$I_{COMP_}$ = ±2.5µA		510	590	650	µS
COMP_ Source Current	$I_{COMP__SRC}$			19	33	55	µA
COMP_ Sink Current	$I_{COMP__SINK}$			19	33	55	µA
Current Sense Transresistance	$R_{CS_}$			0.455	0.5	0.545	Ω
CURRENT LIMIT							
Peak Current Limit Threshold	I_{PEAK_-LIMIT}			1.35	1.6	1.85	A
Runaway Current Limit Threshold	$I_{RUNAWAY_-LIMIT}$			1.45	1.85	2.05	A
Sink Current Limit Threshold	$I_{SINK-LIMIT}$	$V_{MODE_}$ < 0.8V			0.65		A
		$V_{MODE_}$ > 2V			0		A
PFM Peak Current	$I_{PFM_}$	$V_{MODE_}$ > 2V		0.2	0.3	0.4	A
TIMINGS							
Switching Frequency	$f_{SW_}$	$V_{FB_}$ > V_{OUT_-HICF}	V_{FSEL} > 2V	510	560	600	kHz
			V_{FSEL} < 0.8V	280	300	320	
		$V_{FB_}$ <V_{OUT_-HICF}	V_{FSEL} > 2V	280	300	320	
$V_{FB_}$ Under Voltage Trip Level to Cause HICCUP	V_{OUT_-HICF}	$V_{SS_}$ > 0.95V (soft-start is done)		68.5	70	72.5	%
HICCUP Timeout					4096		Cycles
Minimum On-Time	$t_{ON__MIN}$				85	120	ns
Maximum Duty Cycle	$D_{MAX_}$	$V_{FB_}$ = 0.98 x V_{FB_-REG}	V_{FSEL} > 2V	92	94	96	%
			V_{FSEL} < 0.8V	96	97	98	
LX_ Dead Time					5		ns

Electrical Characteristics (continued)

($V_{IN_}$ = +24V, $V_{SGND_}$ = $V_{PGND_}$ = V_{FSEL} = 0V, $C_{IN_}$ = 2.2µF, $C_{VCC_}$ = 1µF, $V_{EN/UVLO_}$ = 1.5V, $C_{SS_}$ = 0.01µF, FB_ = 0.98 x V_{FB-REG}, COMP_ = unconnected, LX_ = unconnected, $\overline{RESET_}$ = unconnected. T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND_, unless otherwise noted.) (Note 2)

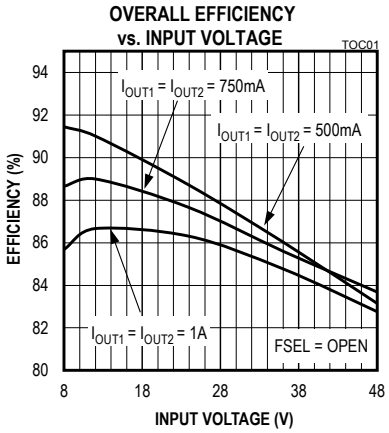
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FREQUENCY SYNCHRONIZATIONS (SYNC)						
SYNC Threshold	V_{SYNC_R}				0.8	V
	V_{SYNC_F}		2			
SYNC Input Leakage Current	I_{SYNC}	V_{SYNC} = 5V ; T_A = +25°C			300	nA
SYNC Pulse Duration	T_{SYNC}		50			ns
SYNC Frequency	f_{SYNC}	f_{SW} = 300kHz or 560kHz		1.1x f_{SW}	1.4x f_{SW}	kHz
$\overline{RESET_}$						
$\overline{RESET_}$ Output Level Low		$I_{\overline{RESET_}}$ = 1mA			0.02	V
$\overline{RESET_}$ Output Leakage Current High		$V_{FB_}$ = 1.01 x V_{FB_-REG}, T_A = 25°C			0.5	µA
$V_{OUT_}$ Threshold for $\overline{RESET}$ Falling	$V_{OUT_}$ -OKF	$V_{FB_}$ falling	90.5	92.5	94.5	%
$V_{OUT_}$ Threshold for $\overline{RESET_}$ Rising	$V_{OUT_}$-OKR	$V_{FB_}$ rising	93.5	95.5	97.5	%
$\overline{RESET}$ _ Delay After FB_ Reaches 95% Regulation				1024		Cycles
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		Temperature rising		165		°C
Thermal-Shutdown Hysteresis				10		°C

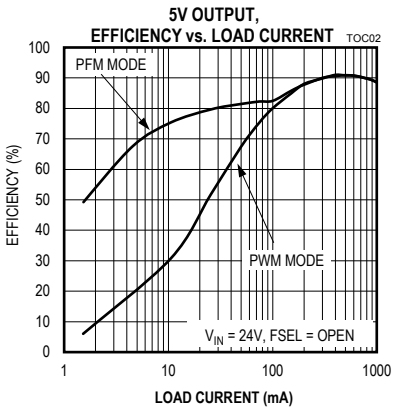
Note 2: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

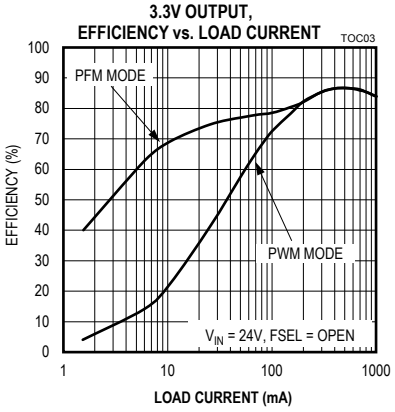
Note 3: Guaranteed by design, not production tested.

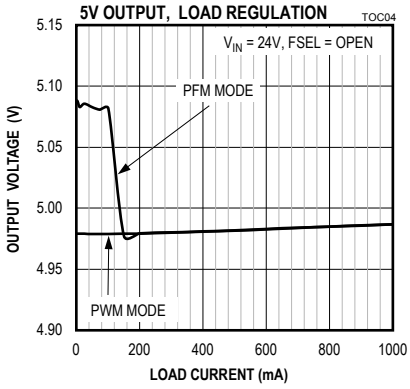
Typical Operating Characteristics

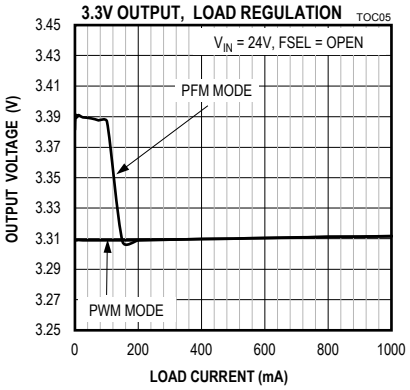
All data measured on the Typical Application Circuit.

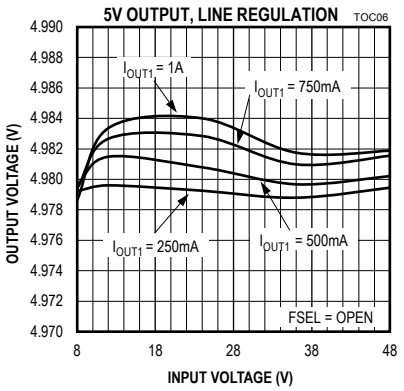


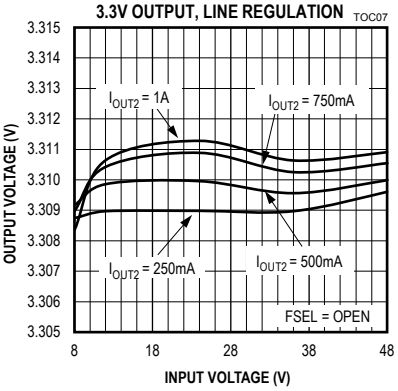








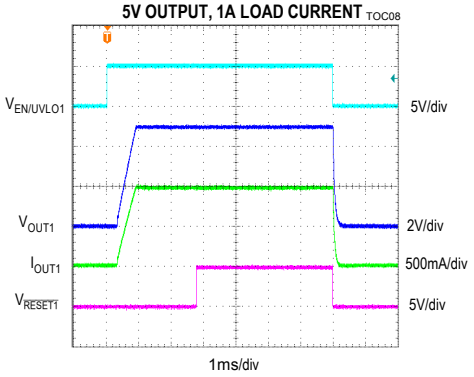




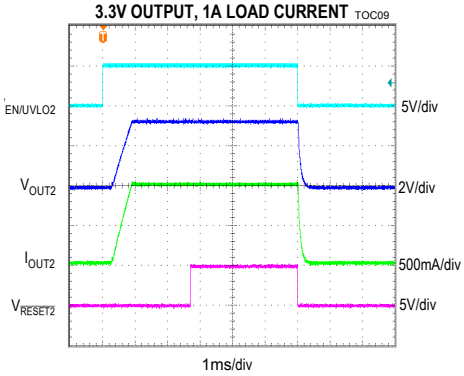
Typical Operating Characteristics (continued)

All data measured on the Typical Application Circuit.

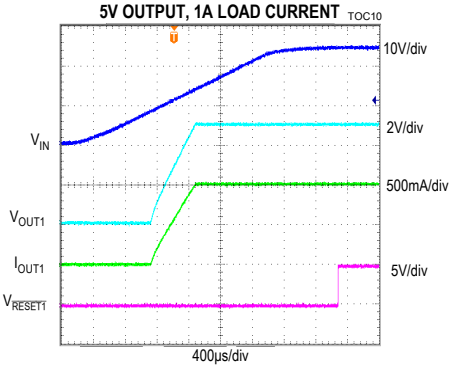
STARTUP FROM EN/UVLO, 5V OUTPUT, 1A LOAD CURRENT TOC08



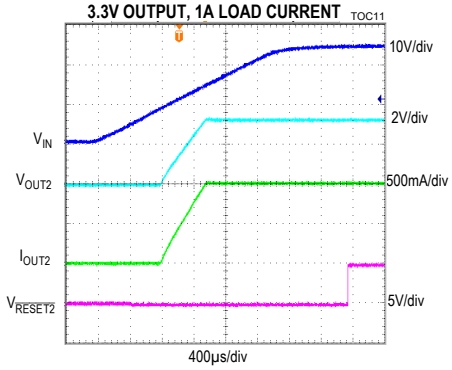
STARTUP FROM EN/UVLO, 3.3V OUTPUT, 1A LOAD CURRENT TOC09



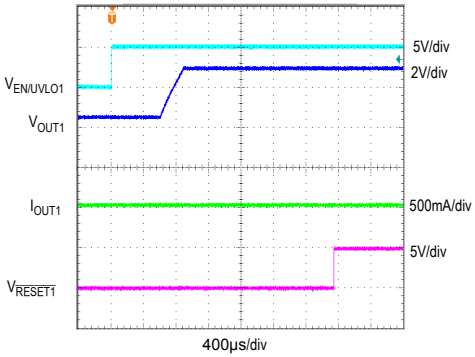
STARTUP FROM VIN, 5V OUTPUT, 1A LOAD CURRENT TOC10



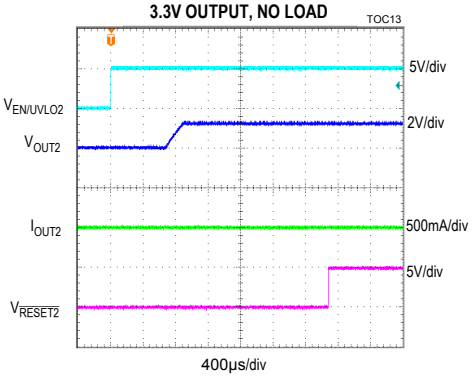
STARTUP FROM VIN, 3.3V OUTPUT, 1A LOAD CURRENT TOC11



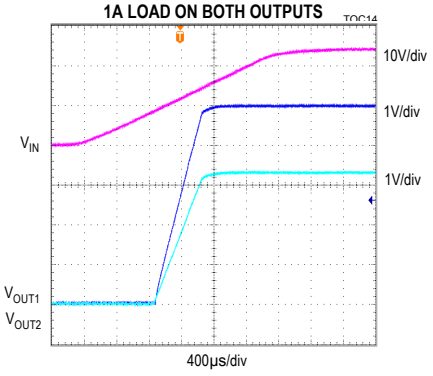
STARTUP WITH 2.5V PREBIAS, 5V OUTPUT, NO LOAD TOC12



STARTUP WITH 2V PREBIAS, 3.3V OUTPUT, NO LOAD TOC13



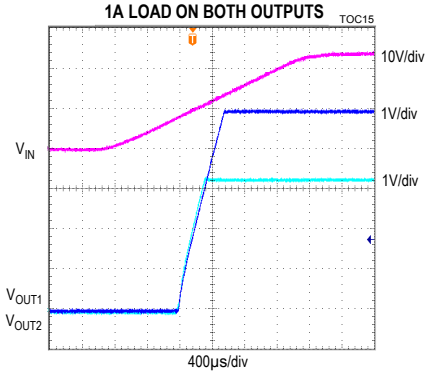
STARTUP IN RATIOMETRIC TRACKING MODE, 1A LOAD ON BOTH OUTPUTS TOC14



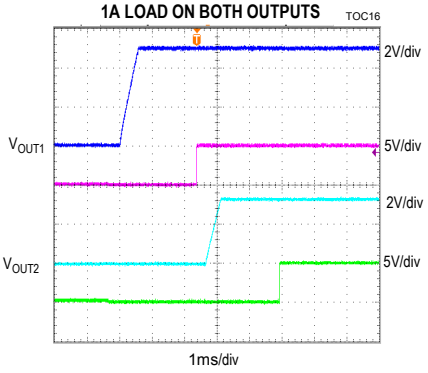
Typical Operating Characteristics (continued)

All data measured on the Typical Application Circuit.

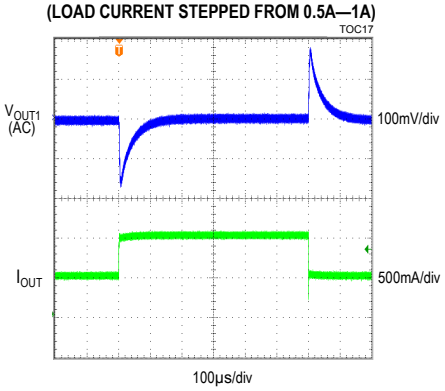
STARTUP IN COINCIDENT TRACKING MODE, 1A LOAD ON BOTH OUTPUTS



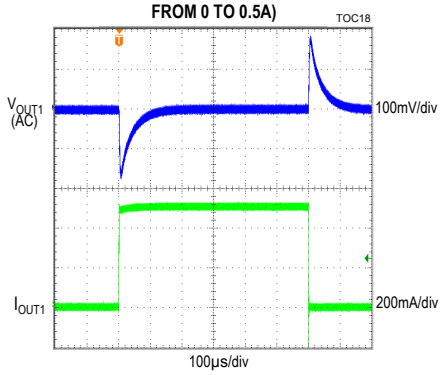
STARTUP IN SEQUENTIAL TRACKING MODE, 1A LOAD ON BOTH OUTPUTS



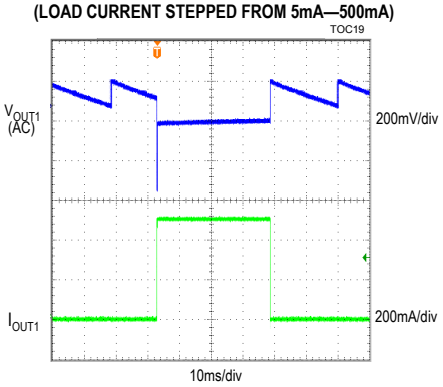
5V OUTPUT,PWM MODE, (LOAD CURRENT STEPPED FROM 0.5A—1A)



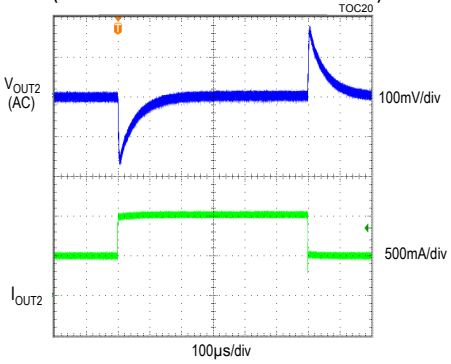
5V OUTPUT, PWM MODE, (LOAD CURRENT STEPPED FROM 0 TO 0.5A)



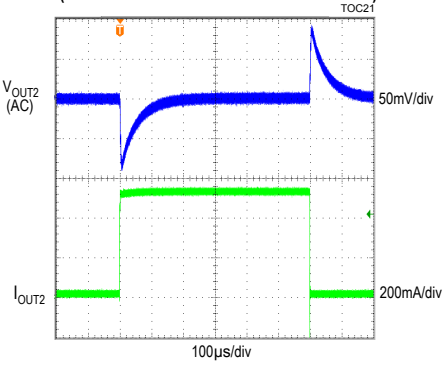
5V OUTPUT, PFM MODE, (LOAD CURRENT STEPPED FROM 5mA—500mA)



3.3V OUTPUT,PWM MODE, (LOAD CURRENT STEPPED FROM 0.5A—1A)



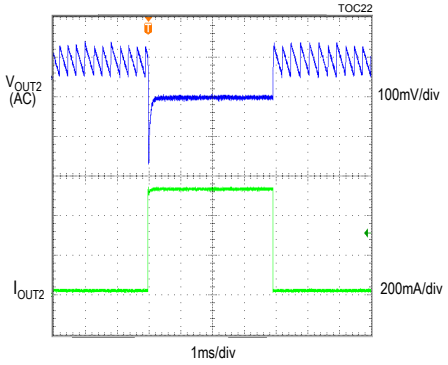
3.3V OUTPUT, PWM MODE, (LOAD CURRENT STEPPED FROM 0—0.5A)



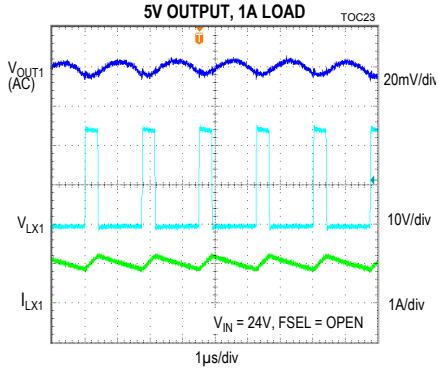
Typical Operating Characteristics (continued)

All data measured on the Typical Application Circuit.

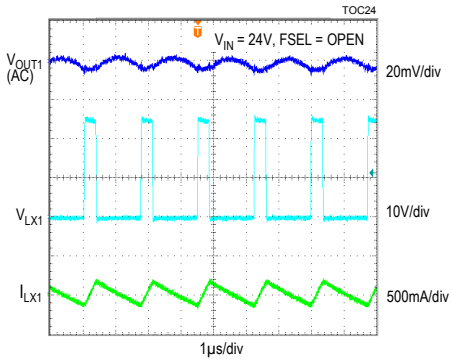
3.3V OUTPUT, PFM MODE, (LOAD CURRENT STEPPED FROM 5mA—0.5A)



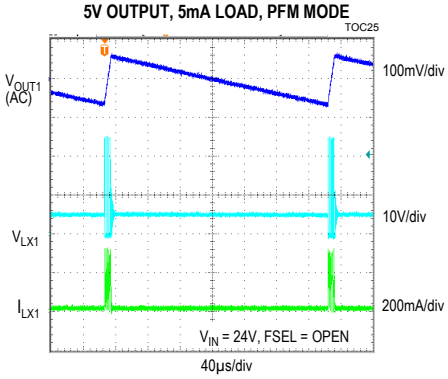
STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, 1A LOAD



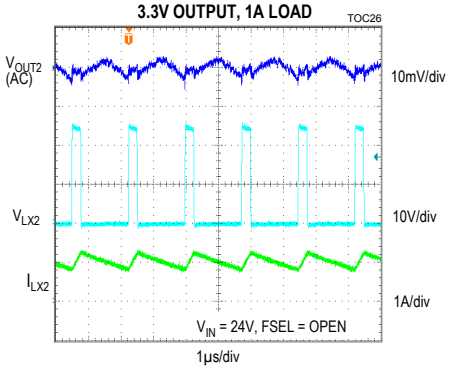
STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, NO LOAD, PWM MODE



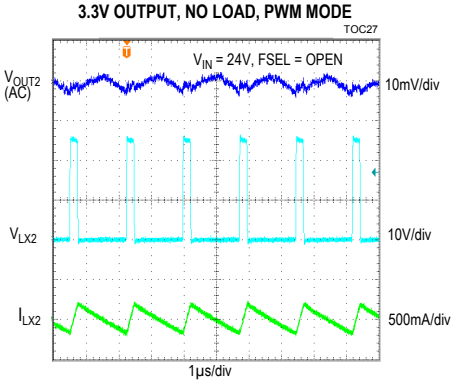
STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, 5mA LOAD, PFM MODE



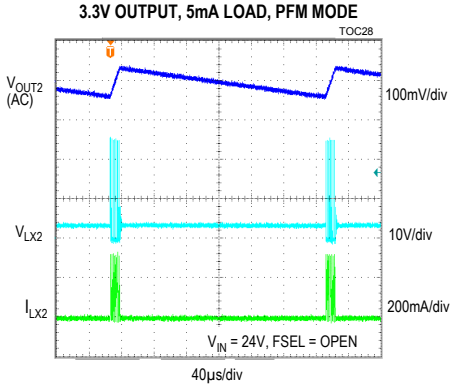
STEADY-STATE SWITCHING WAVEFORMS, 3.3V OUTPUT, 1A LOAD



STEADY-STATE SWITCHING WAVEFORMS, 3.3V OUTPUT, NO LOAD, PWM MODE



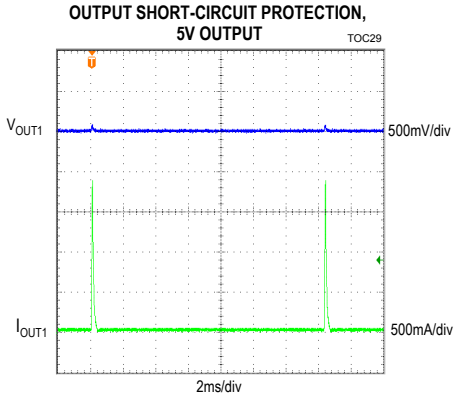
STEADY-STATE SWITCHING WAVEFORMS, 3.3V OUTPUT, 5mA LOAD, PFM MODE



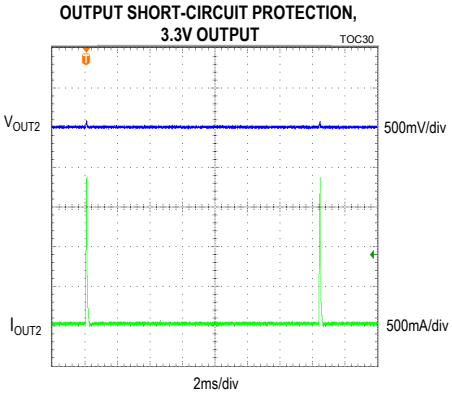
Typical Operating Characteristics (continued)

All data measured on the Typical Application Circuit.

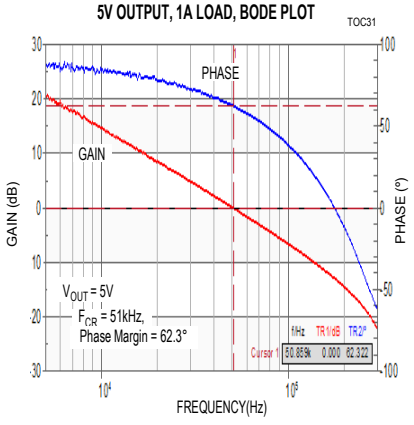
OUTPUT SHORT-CIRCUIT PROTECTION, 5V OUTPUT



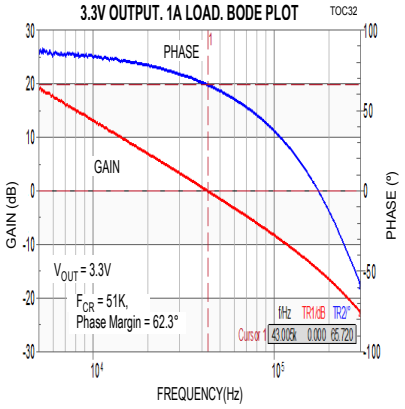
OUTPUT SHORT-CIRCUIT PROTECTION, 3.3V OUTPUT



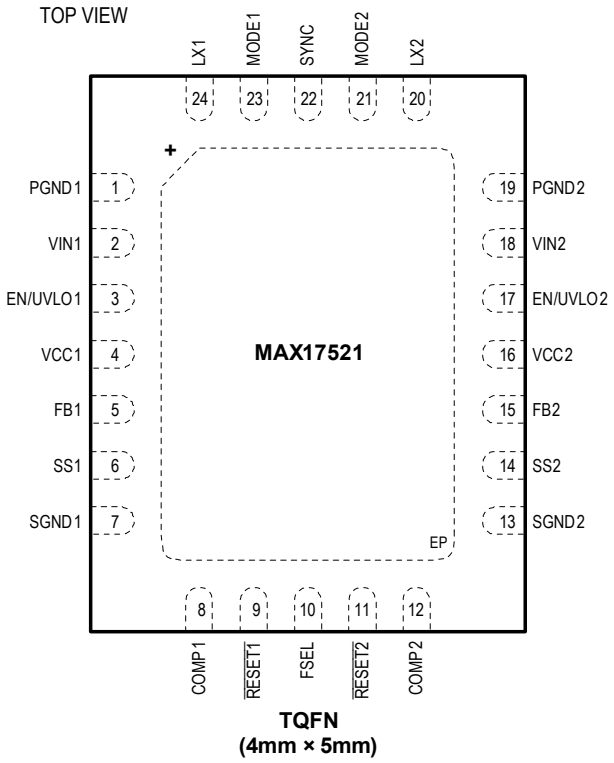
5V OUTPUT, 1A LOAD, BODE PLOT



3.3V OUTPUT. 1A LOAD. BODE PLOT



Pin Configuration



TQFN
(4mm × 5mm)

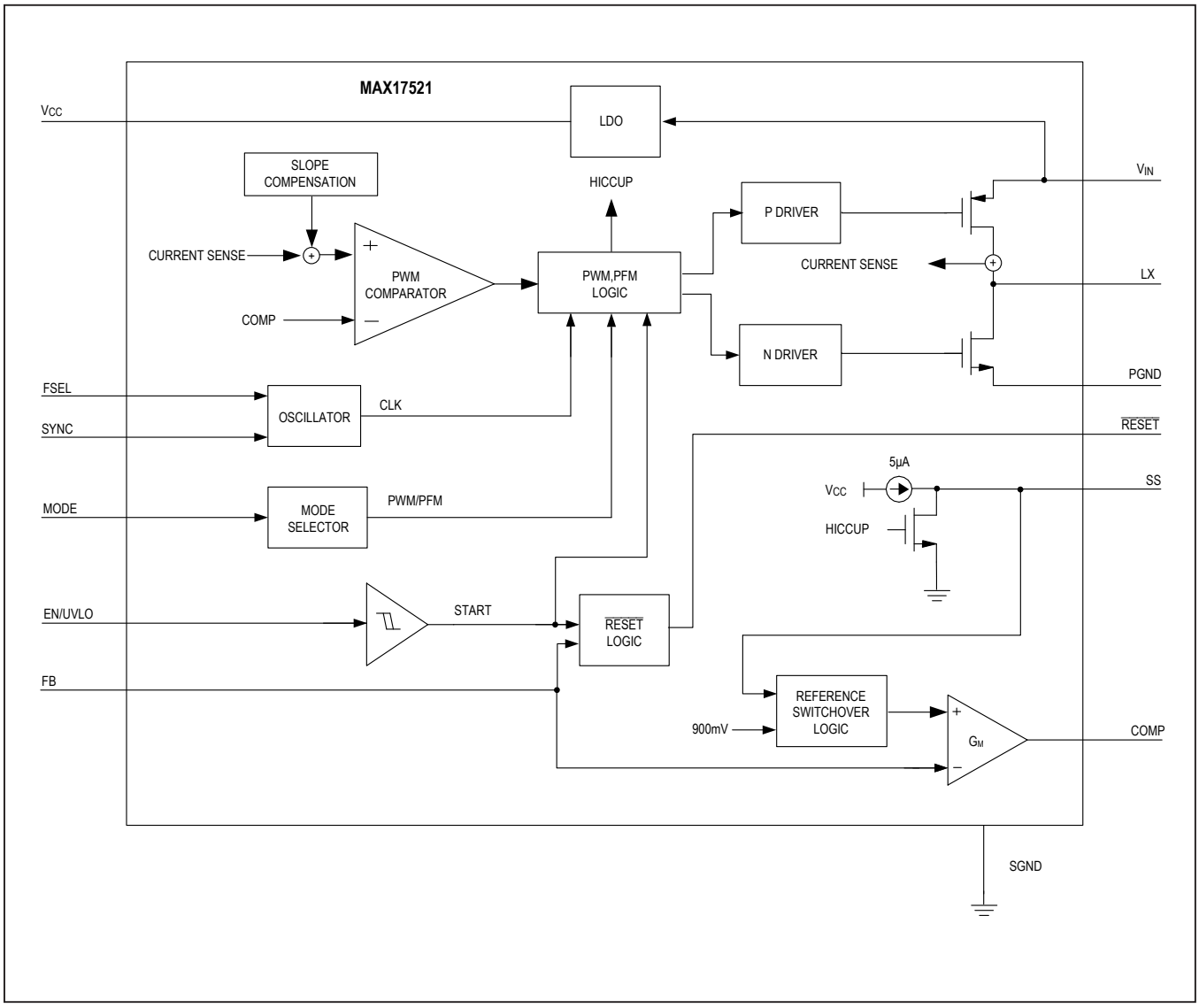
Pin Description

PIN	NAME	FUNCTION
1	PGND1	Power Ground Connection of Converter 1. Connect PGND1 externally to the power ground plane. Connect SGND and PGND pins together at the ground return path of the V_{CC} bypass capacitors.
2	VIN1	Power-Supply Input of Converter 1. The input supply range is from 4.5V to 60V. Decouple to PGND1 with a 2.2µF capacitor; place the capacitor close to the V_{IN1} and PGND1 pins.
3	EN/UVLO1	Enable/Undervoltage Lockout Input for Converter 1. Drive EN/UVLO1 high to enable converter 1. Connect to the center of the resistive divider between V_{IN1} and SGND1 to set the input voltage at which the converter 1 turns on. Pull up to V_{IN1} for always-on operation.
4	VCC1	5V LDO Output for Converter 1. Bypass V_{CC1} with 1µF ceramic capacitance to SGND1.
5	FB1	Feedback Input for Converter 1. Connect FB1 to the center of the resistive divider between V_{OUT1} and SGND1. See the *Adjusting Output Voltage* section for more details.
6	SS1	Soft-start Input for Converter 1. Connect a capacitor from SS1 to SGND1 to set the soft-start time for converter 1.
7	SGND1	Analog Ground Connection for Converter 1.
8	COMP1	Loop Compensation Pin for Converter 1. Connect an RC network from COMP1 to SGND1. See the *Loop Compensation* section for more details.

Pin Description (continued)

PIN	NAME	FUNCTION
9	$\overline{\text{RESET1}}$	Open-Drain $\overline{\text{RESET1}}$ Output. The $\overline{\text{RESET1}}$ output is driven low if FB1 drops below 92.5% of its set value. $\overline{\text{RESET1}}$ goes high 1024 clock cycles after FB1 rises above 95.5% of its set value. $\overline{\text{RESET1}}$ is valid when the device is enabled and V_{IN} is above 4.5V.
10	FSEL	Configures the Switching Frequency of the MAX17521. Leaving FSEL unconnected sets the switching frequency of both the converters at 560kHz. Connecting FSEL pin to SGND_ sets the switching frequency of both the converters at 300kHz.
11	$\overline{\text{RESET2}}$	Open-Drain $\overline{\text{RESET2}}$ Output. The $\overline{\text{RESET2}}$ output is driven low if FB2 drops below 92.5% of its set value. $\overline{\text{RESET2}}$ goes high 1024 clock cycles after FB2 rises above 95.5% of its set value. $\overline{\text{RESET2}}$ is valid when the device is enabled and V_{IN} is above 4.5V.
12	COMP2	Loop Compensation Pin for Converter 2. Connect an RC network from COMP2 to SGND2. See the *Loop Compensation* section for more details.
13	SGND2	Analog Ground Connection for Converter 2.
14	SS2	Soft-Start Input for Converter 2. Connect a capacitor from SS2 to SGND2 to set the soft-start time for converter 2.
15	FB2	Feedback Input for Converter 2. Connect FB2 to the center of the resistive divider between V_{OUT2} and SGND2. See the *Adjusting Output Voltage* section for more details.
16	VCC2	5V LDO Output for converter 2. Bypass V_{CC2} with 1µF ceramic capacitance to SGND2.
17	EN/UVLO2	Enable/Undervoltage Lockout Input for Converter 2. Drive EN/UVLO2 high to enable converter 2. Connect to the center of the resistive divider between V_{IN2} and SGND2 to set the input voltage at which the converter 2 turns on. Pull up to V_{IN2} for always on operation.
18	VIN2	Power-Supply Input of Converter 2. The input supply range is from 4.5V to 60V. Decouple to PGND2 with a 2.2µF capacitor; place the capacitor close to the V_{IN2} and PGND2 pins.
19	PGND2	Power Ground Connection of Converter 2. Connect PGND2 externally to the power ground plane. Connect SGND and PGND pins together at the ground return path of the V_{CC} bypass capacitors.
20	LX2	Switching Node of Converter 2. Connect LX2 to the switching side of the inductor.
21	MODE2	Configures Converter 2 to Operate in PWM or PFM Modes of Operation. Leave MODE2 unconnected for PFM operation (pulse skipping at light loads). Connect MODE2 to SGND2 for constant frequency PWM operation at all loads. See the *MODE Setting* section for more details.
22	SYNC	Synchronizes Device to an External Clock. See the *External Frequency Synchronization* section for more details.
23	MODE1	Configures Converter 1 to Operate in PWM or PFM Modes of Operation. Leave MODE1 unconnected for PFM operation (pulse skipping at light loads). Connect MODE1 to SGND1 for constant frequency PWM operation at all loads. See the *MODE Setting* section for more details.
24	LX1	Switching Node of Converter 1. Connect LX1 to the switching-side of the inductor.
–	EP	Exposed Pad. Connect to the SGND pins. Connect to a large copper plane below the IC to improve heat dissipation capability.

Block Diagram



Detailed Description

The MAX17521 dual step-down regulator operates from 4.5V to 60V and delivers up to 1A load current on each output. Feedback voltage regulation accuracy meets ±1.7% over load, line and temperature.

The device uses a peak-current-mode control scheme. For each output, an internal transconductance error amplifier generates an integrated error voltage. The error voltage sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the high-side pMOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected.

During the high-side MOSFET's on-time, the inductor current ramps up. During the second half of the switching cycle, the high-side MOSFET turns off and the low-side nMOSFET turns on and remains on until either the next rising edge of the clock arrives or sink current limit is detected. The inductor releases the stored energy as its current ramps down, and provides current to the output (the internal low R_{DSON} pMOS/nMOS switches ensure high efficiency at full load).

This device also integrates switching frequency selector pin and individual mode of operation selector pins, enable/undervoltage lockout (EN/UVLO) pins, programmable soft-start pins, and open-drain $\overline{RESET}$ signals for each output.

Mode of Operation Selection

The logic state of the MODE pins are latched when V_{CC} and EN/UVLO voltages exceed the respective UVLO rising thresholds and all internal voltages are ready to allow LX switching. If the MODE pin is open at power-up, the corresponding output operates in PFM mode at light loads. If the MODE pin is grounded at power-up, the corresponding output operates in constant-frequency PWM mode at all loads. State changes on the MODE pins are ignored during normal operation.

PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation at all loads, and is useful in applications sensitive to switching frequency. However, the PWM mode of operation gives lower efficiency at light loads compared to the PFM mode of operation.

PFM Mode Operation

PFM mode of operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak of 300mA every clock cycle until the output rises to 103% of the nominal voltage. Once the output reaches 103% of the nominal voltage, both the high-side and low-side FETs are turned off and the device enters hibernate operation until the load discharges the output to 101% of the nominal voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101% of the nominal voltage, the device comes out of hibernate operation, turns on all internal blocks and again commences the process of delivering pulses of energy to the output until it reaches 103% of the nominal output voltage.

The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply. The disadvantage is that the output-voltage ripple is higher compared to PWM mode of operation and switching frequency is not constant at light loads.

Linear Regulator (V_{CC})

Two internal linear regulators (V_{CC1}, V_{CC2}) provide 5V nominal supplies to power the internal blocks and the low-side MOSFET drivers. The output of the V_{CC} linear regulators should be bypassed with 1µF ceramic capacitors to SGND. The device employs two undervoltage-lockout circuits that disable the internal linear regulators when V_{CC} falls below 3.7V (typ). Each of the V_{CC} regulators can source up to 40mA (typ) to supply the device and to power the low-side gate drivers.

Switching Frequency Selection

The FSEL pin programs the switching frequency of both the converters. If the FSEL pin is open at power-up, both the outputs operate at 560 kHz switching frequency. If the FSEL pin is grounded at power-up, both the outputs operate at 300kHz switching frequency.

Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + (I_{OUT(MAX)} \times (R_{DCR} + R_{DSONLS}))}{D_{MAX}} + (I_{OUT(MAX)} \times R_{DSONHS} - R_{DSONLS})$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON(MIN)}}$$

where V_{OUT} is the steady-state output voltage, $I_{OUT(MAX)}$ is the maximum load current, R_{DCR} is the DC resistance of the inductor, D_{MAX} is the maximum allowable duty ratio, $f_{SW(MAX)}$ is the maximum switching frequency and t_{ON-MIN} is the worst-case minimum switch on-time (120ns). The following table lists the $f_{SW(MAX)}$ and D_{MAX} values to be used for calculation for different switching frequency selection

FSEL	$f_{SW(MAX)}$ (kHz)	D_{MAX}
OPEN	600	0.92
SGND	320	0.96

External Frequency Synchronization (SYNC)

The internal oscillator of the device can be synchronized to an external clock signal on the SYNC pin. The external synchronization clock frequency must be between 1.1 x f_{SW} and 1.4 x f_{SW}, where f_{SW} is the frequency selected by the FSEL pin. The minimum external clock pulse-width high should be greater than 50ns. See the SYNC section in the *Electrical Characteristics* table for details.

Overcurrent Protection/HICCUP Mode

The device is provided with a robust overcurrent-protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of 1.6A (typ). A runaway current limit on the high-side switch current at 1.85A (typ) protects the device under high input voltage, short-circuit conditions when there is insufficient output voltage available to restore the inductor current that built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. In addition, if due to a fault condition, output voltage drops to 70% (typ) of its nominal value any time after soft-start is complete, hiccup mode is triggered.

In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 4096 clock cycles. Once the hiccup timeout period expires, soft-start is attempted again. This operation results in minimal power dissipation under overload fault conditions.

$\overline{\text{RESET}}$ Output

The device includes two $\overline{\text{RESET}}$ comparators to monitor the output voltages. The open-drain $\overline{\text{RESET}}$ outputs require an external pull-up resistor. $\overline{\text{RESET}}$ can sink 2mA of current while low. $\overline{\text{RESET}}$ goes high (high impedance) 1024 switching cycles after the corresponding output voltage increases above 95.5% of the nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the output voltage drops to below 92.5% of the nominal regulated voltage. $\overline{\text{RESET}}$ also goes low during thermal shutdown. $\overline{\text{RESET}}$ is valid when the device is enabled and V_{IN} is above 4.5V.

Coincident/Ratiometric Tracking and Output Voltage Sequencing

The soft-start pins (SS_) can be used to track the output voltages to that of another power supply at startup. This requires connecting the SS_ pins to an external resistor divider from the supply which needs to be tracked. The following figures (Figure 1 to Figure 3) show the possible ways of configuring the MAX17521 in various tracking modes.

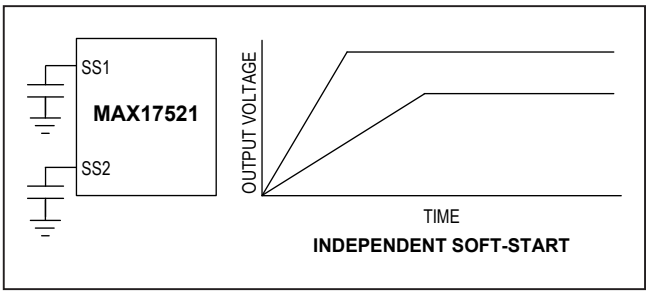


Figure 1. Independent Soft-Start of Each Output

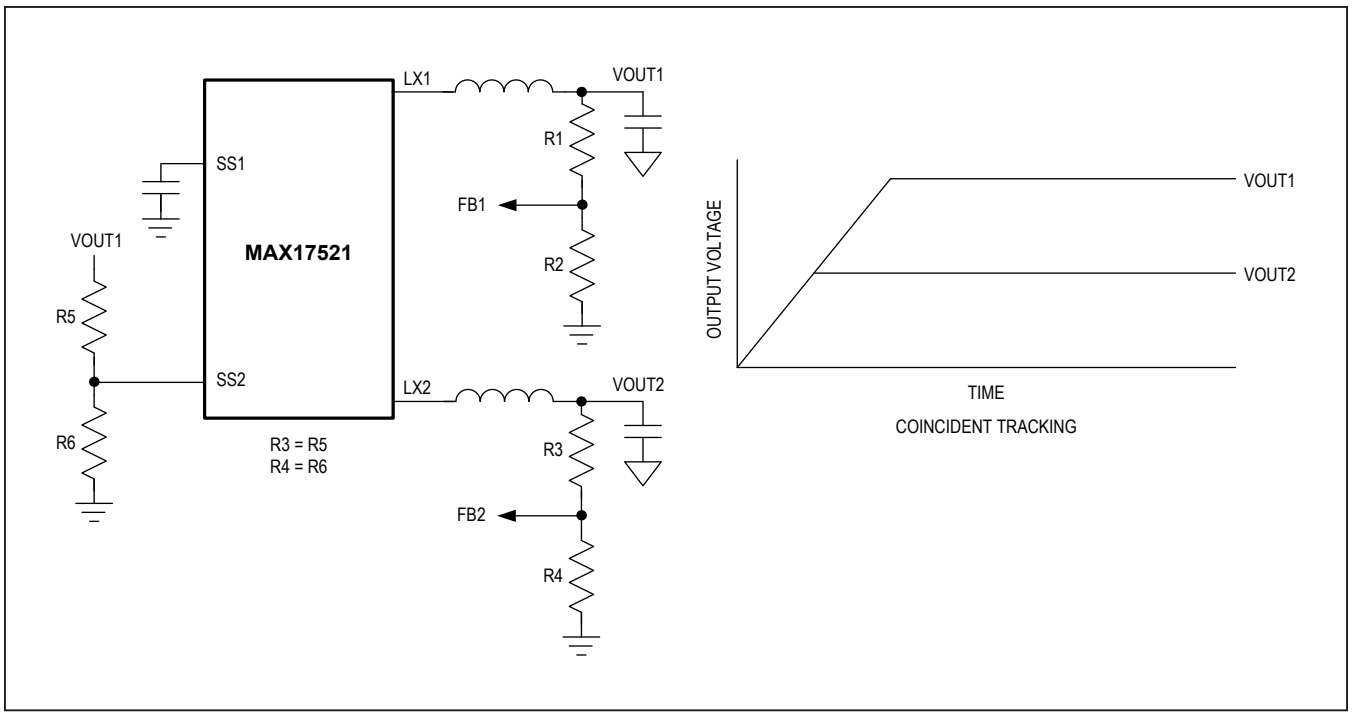


Figure 2. Coincident Tracking of the Outputs

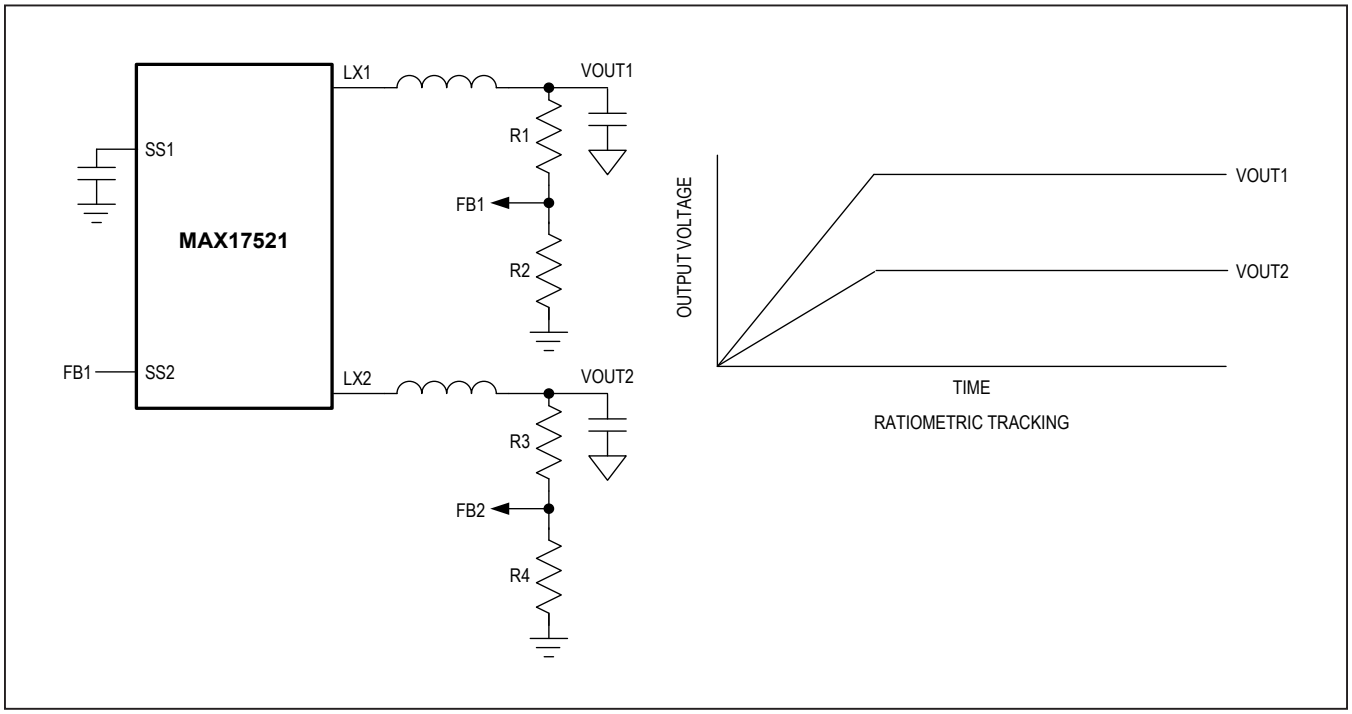


Figure 3. Ratiometric Tracking of the Outputs

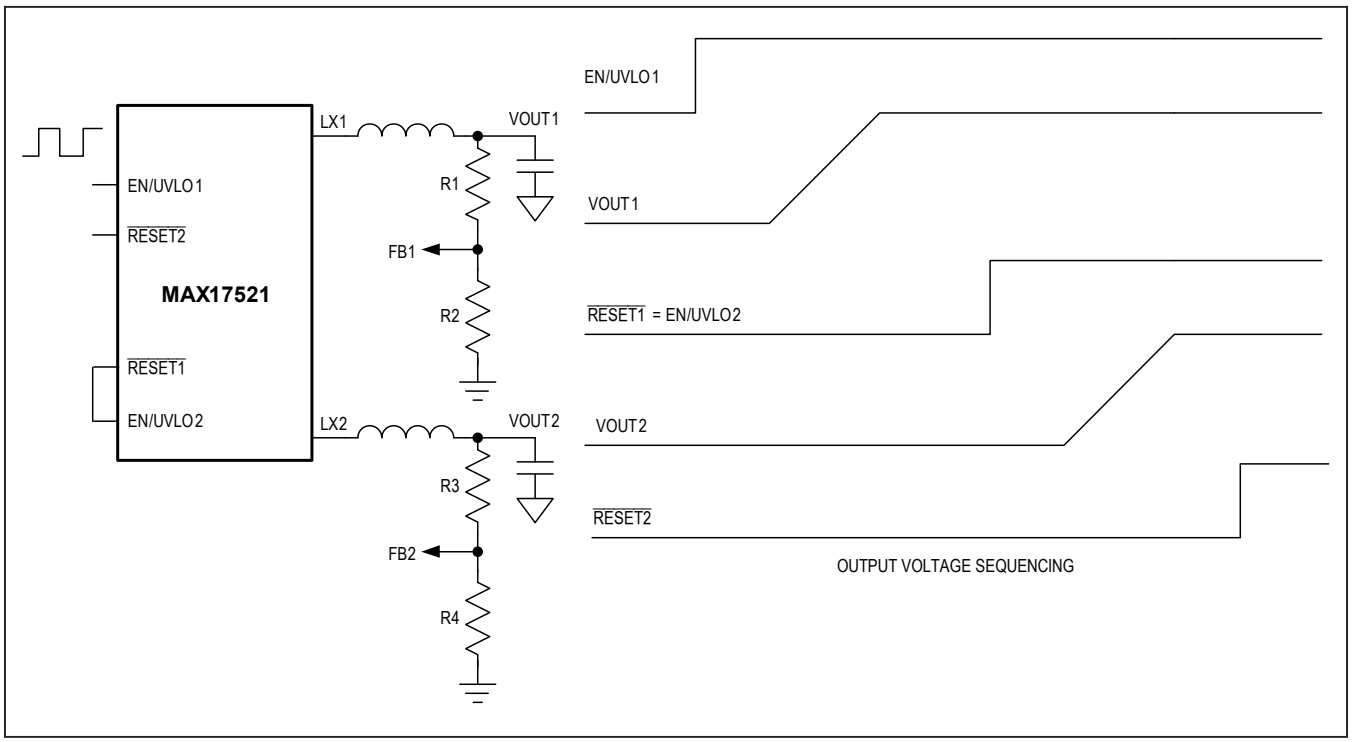


Figure 4. Output Voltage Sequencing

During power-off, the output voltages discharge to ground at a rate which depends on the respective output capacitor and load.

The $\overline{\text{RESET}}$_ pins and EN/UVLO_ pins can be daisy-chained to generate power sequencing, as shown in Figure 4.

Prebiased Output

When the device starts into a prebiased output, both the high-side and low-side switches of the corresponding channel are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences first with the high-side switch. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the device. When the junction temperature of the device exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 10°C. Soft-start resets during thermal shutdown. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal-overload protection in normal operation.

Applications Information

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) for a single output is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so $I_{RMS(MAX)}$ = $I_{OUT(MAX)}/2$ when only one converter is enabled. When both the converters are enabled and are operating out-of-phase, the RMS current is shared by both the input capacitors and therefore the maximum RMS current carried by each of the input capacitors is $I_{OUT(MAX)}/4$.

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. When both the converters are enabled, calculate the input capacitance using the following equation:

$$C_{IN} = \frac{0.5 \times I_{OUT(MAX)} \times D \times (1-D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where $D = V_{OUT}/V_{IN}$ is the duty ratio of the controller, f_{SW} is the switching frequency, ΔV_{IN} is the allowable input voltage ripple, and η is the efficiency.

In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}) and DC resistance (R_{DCR}). The switching frequency and output voltage determine the inductor value as follows:

$$L = \frac{2.2 \times V_{OUT}}{f_{SW}}$$

where V_{OUT} and f_{SW} are nominal values. Select an inductor whose value is nearest to the value calculated by the previous formula.

Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value of 1.85A.

Output Capacitor Selection

X7R Ceramic Output capacitors are preferred due to their stability over temperature in Industrial applications. The output capacitor is usually sized to support a step load of 50% of the maximum output current in the application, such that the output voltage deviation is contained to 3% of the output voltage change. The output capacitance may be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{sw}}\right)$$

Where I_{STEP} is the load current step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output voltage deviation, f_C is the target closed-loop crossover frequency and f_{SW} is the switching frequency. f_C is generally chosen to be $1/9^{th}$ of f_{SW}.

Soft-Start capacitor selection

The device implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time for the corresponding output voltage. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 56 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} \geq \frac{C_{SS}}{5.55 \times 10^{-6}}$$

For example, to program a 1ms soft-start time, a 5.6nF capacitor should be connected from the SS pin to SGND.

Adjusting Output Voltage

Set the output voltages with resistive voltage-dividers connected from the positive terminal of the output capacitor (V_{OUT}) to SGND (see Figure 5). Connect the centre node of the divider to the FB pin. To optimize efficiency and output accuracy, use the following calculations to choose the resistive divider values:

$$R4 = \frac{15 \times V_{OUT}}{0.9}$$

$$R5 = \frac{R4 \times 0.9}{(V_{OUT} - 0.9)}$$

where R4 and R5 are in kΩ.

Setting the Undervoltage-Lockout Level

The device offers an adjustable input undervoltage-lockout level for each output. Set the voltage at which each converter turns on with a resistive voltage-divider connected from VIN to SGND (see Figure 6). Connect the center node of the divider to EN/UVLO pin.

Choose R1 to be 3.3MΩ, and then calculate R2 as:

$$R2 = \frac{R1 \times 1.218}{(V_{INU} - 1.218)}$$

where V_{INU} is the input voltage at which a particular converter is required to turn on.

Loop Compensation for Adjustable Output Version

The MAX17521 uses peak current-mode control scheme and needs only simple RC networks connected from the COMP pins to SGND to have a stable, high-bandwidth control loop. The basic regulator loop is modeled as a power modulator, an output feedback divider, and an error amplifier. The power modulator has DC gain $G_{MOD(dc)}$, with a pole and zero pair. The following equation defines the power modulator DC gain:

$$G_{MOD(dc)} = \frac{2}{\frac{1}{R_{LOAD}} + \frac{0.4}{V_{IN}} + \frac{(0.5 - D)}{f_{SW} \times L_{SEL}}}$$

Where $R_{LOAD} = V_{OUT}/I_{OUT(MAX)}$, f_{SW} is the switching frequency, L_{SEL} is the selected output inductance, D is the duty ratio, $D = V_{OUT}/V_{IN}$.

The compensation network is shown in Figure 7.

R_Z can be calculated as:

$$R_Z = 6000 \times f_C \times C_{SEL} \times V_{OUT}$$

where R_Z is in Ω. Choose f_C to be 1/9th of the switching frequency.

C_Z can be calculated as follows:

$$C_Z = \frac{C_{SEL} \times G_{MOD(dc)}}{2 \times R_Z}$$

C_P can be calculated as follows:

$$C_P = \frac{1}{\pi \times R_Z \times f_{SW}}$$

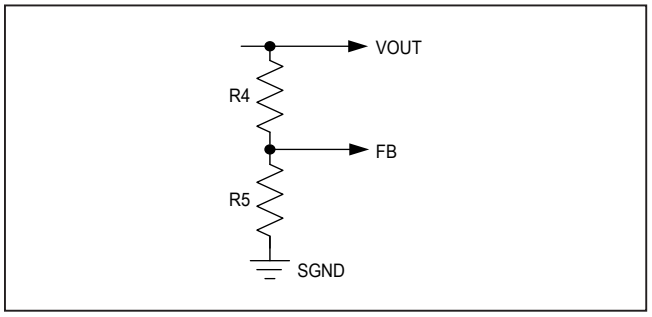


Figure 5. Adjusting Output Voltage

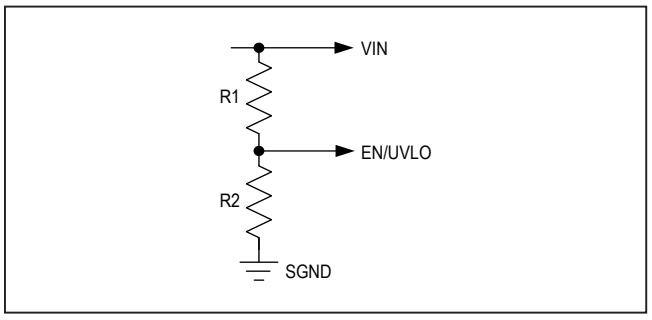


Figure 6. Setting the Undervoltage Lockout Level

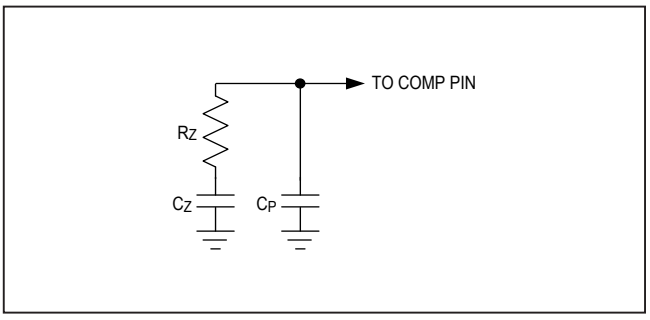


Figure 7. Loop Compensation for Adjustable Output Version

Power Dissipation

The exposed pad of the IC should be properly soldered to the PCB to ensure good thermal contact.

At a particular operating condition, the power losses that lead to temperature rise of the device are estimated as follows:

$$P_{LOSS} = (P_{OUT} \times (\frac{1}{\eta} - 1)) - \left(I_{OUT}{}^2 \times R_{DCR}\right)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where P_{OUT} is the output power, η is the efficiency of the device and R_{DCR} is the DC resistance of the output inductor (refer to the *Typical Operating Characteristics* for more information on efficiency at typical operating conditions).

For a typical multilayer board, the thermal performance metrics for the package are given as:

$$\theta_{JA} = 35°C / W$$

$$\theta_{JC} = 1.8°C / W$$

The junction temperature of the device can be estimated at any given maximum ambient temperature (T_{A_MAX}) from the following equation:

$$T_{J_MAX} = T_{A_MAX} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature (T_{EP_MAX}) by using proper heat sinks, then the junction temperature of the device can be estimated at any given maximum ambient temperature as:

$$T_{J_MAX} = T_{EP_MAX} + (\theta_{JC} \times P_{LOSS})$$

Junction temperatures greater than +125°C degrades operating lifetimes.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and stable operation. For a sample layout that ensures first-pass success, refer to the MAX17521 evaluation kit layouts available at **www.maximintegrated.com**. Follow these guidelines for good PCB layout:

- All connections carrying pulsed currents must be very short and as wide as possible. The loop area of these connections must be made very small to reduce stray inductance and radiated EMI.
- A ceramic input filter capacitor should be placed close to the VIN pins of the device. The bypass capacitor for the VCC pins should also be placed close to the VCC pins. External compensation components should be placed close to the IC and far from the inductor. The feedback trace should be routed as far as possible from the inductor.
- The analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at minimum, typically the return terminal of the VCC bypass capacitors. The ground plane should be kept continuous as much as possible.
- A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the device, for efficient heat dissipation.

Ordering Information

PART	PIN-PACKAGE	PACKAGE-SIZE
MAX17521ATG+	24 TQFN-EP*	4mm X 5mm

**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/15	Initial release	—
1	2/17	Updated operating and junction temperature values	1–10, 12, 20
2	6/17	Updated the *Typical Application Circuit* on first page and replaced the *Block Diagram*. Updated *Typical Operating Characteristics* conditions and *Operating Input Voltage Range* section.	1, 6–10, 13, 15

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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