MAXIM

Serial Output 5.6µs 12-Bit A/D Converter

MAX170

General Description

The MAX170 is a complete CMOS 12-bit A/D converter that combines high speed and accurate performance with a cost and space saving serial interface in an 8-lead DIP or 16-lead surface mount SO package. It uses a high speed DAC and an accurate comparator in a successive approximation loop to achieve a 5.6µs conversion time. An on-chip buried-zener reference provides low-drift performance over the full temperature range.

External components are limited only to supply and reference decoupling capacitors. The CLOCK input can be driven from an external clock source such as a divided-down microprocessor clock. The MAX170 works with +5V and -12V to -15V supply voltages, typically dissipating 135mW.

The MAX170 is designed to work with general purpose serial-to-parallel converters, such as the 74HC595. It can also be used with digital-signal-processors such as the TMS32020, TMS320C25, NEC µPD7720 or the DSP56000. The MAX170 has a three-wire interface that serially outputs a leading one, followed by 12 data bits (MSB first)

When the MAX170 is used with an external sample-and-hold amplifier, a maximum sampling rate of 125kHz is possible.

Applications

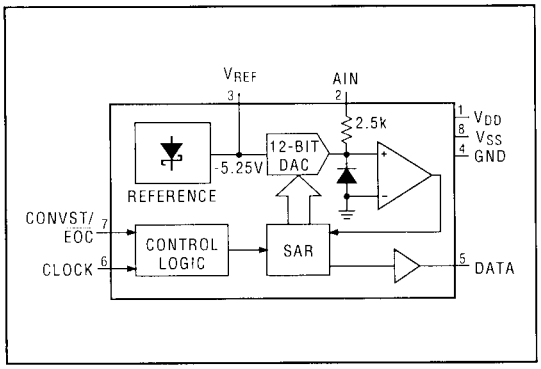
Telecommunication

Digital Signal Processing (DSP)

Sonar/Radar Signal Processing

Isolated Industrial Data Acquisition

Functional Diagram



Features

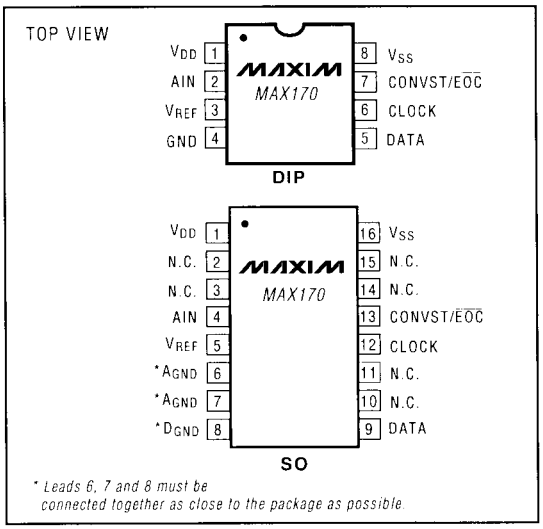
- ♦ 12-Bit Resolution and Linearity
- ♦ 5.6µs Fast Conversion Time
- ♦ Serial Output
- ♦ Self-Start Mode
- ♦ Complete with On-Chip Reference
- ♦ Low Power (135mW)
- ♦ Easy to Opto- or Transformer-Isolate
- ♦ Small Footprint 8-Lead DIP, 16-Lead SO

Ordering Information

PART	TEMP. RANGE	PACKAGE	ERROR
MAX170CCPA	0°C to +70°C	Plastic DIP	±1/2 LSB
MAX170DCPA	0°C to +70°C	Plastic DIP	±1 LSB
MAX170CCWE	0°C to +70°C	Wide SO	±1/2 LSB
MAX170DCWE	0°C to +70°C	Wide SO	±1 LSB
MAX170DC/D	0°C to +70°C	Dice	±1 LSB
MAX170CEPA	-40°C to +85°C	Plastic DIP	±1/2 LSB
MAX170DEPA	-40°C to +85°C	Plastic DIP	±1 LSB
MAX170CEWE	-40°C to +85°C	Wide SO	±1/2 LSB
MAX170DEWE	-40°C to +85°C	Wide SO	±1 LSB
MAX170CMJA	-55°C to +125°C	CERDIP	±1/2 LSB
MAX170DMJA	-55°C to +125°C	CERDIP	±1 LSB

All DIP packages are 8 leads; all SO packages are 16 leads.
Contact factory for "A" and "B" grades.

Pin Configurations



** Leads 6, 7 and 8 must be connected together as close to the package as possible.*

Call toll free 1-800-998-8800 for free samples or literature.

Serial Output 5.6µs 12-Bit A/D Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3 to +7V
V_{SS} to GND ..... +0.3V to -17V
AIN to AGND ..... ±15V
Digital Input Voltage to GND ..... -0.3V, V_{DD} +0.3V (Pins 6, 7, DIP)
Digital Output Voltage to GND ..... -0.3V, V_{DD} +0.3V (Pin 5, DIP)

Operating Temperature Ranges
MAX170XC ..... 0°C to +70°C
MAX170XE ..... -40°C to +85°C
MAX170XM ..... -55°C to +120°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any package) to +70°C 500mW
Derates Above +75°C by ..... 6.25mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V; f_{CLK} = 2.5MHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				12			Bits
		T_A = 25°C	MAX170C			±1/2	
Integral Nonlinearity	INL		MAX170CC/CE			±1/2	LSB
			MAX170CM			±3/4	
			MAX170D			±1	
Differential Nonlinearity	DNL	Guaranteed Monotonic Over Temperature				±1	LSB
Offset Error (Note 1)			MAX170C			+4	LSB
			MAX170D			±5	
Full Scale Error (Note 2)		T_A = 25°C				±10	LSB
Full Scale Tempco (Notes 3,4)			MAX170C			±25	ppm/°C
			MAX170D			±45	
Conversion Time	t_{CONV}	14 Clock Cycles				5.6	µs
ANALOG INPUT							
Input Voltage Range				0		+5	V
Input Current		AIN = 0V to +5V				3.5	mA
INTERNAL REFERENCE							
V_{REF} Output Voltage		T_A = 25°C		-5.2	-5.25	-5.3	V
V_{REF} Output Tempco (Note 5)			MAX170C		±20		ppm/°C
			MAX170D		±40		
Output Current Sink Capability		(Note 6)				5	mA
POWER SUPPLY REJECTION							
Positive Supply Rejection	V_{DD}	FS Change, V_{SS} = -15V or -12V, V_{DD} = 4.75V to 5.25V			±1/2		LSB
Negative Supply Rejection	V_{SS}	FS Change, V_{DD} = +5V	V_{SS} = -14.25V to -15.75V		±1/8		LSB
			V_{SS} = -11.4V to -12.6V		±1/8		
LOGIC INPUTS							
Input Low Voltage	V_{IL}					0.8	V
Input High Voltage	V_{IH}			2.4			V
Input Capacitance (Note 7)	C_{IN}					10	pF
Input Current	I_{IN}	AIN = 0 to V_{DD}	CLOCK			+10	µA
			CONVST/EOC	±200		±500	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V; f_{CLK} = 2.5MHz; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC OUTPUT						
Output Low Voltage	V_{OL}	DATA I_{SINK} = 1.6mA			0.4	V
		DATA I_{SINK} = 6.0mA		0.3	1.5	
Output High Voltage	V_{OH}	DATA I_{SOURCE} = 200µA	4			V
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}	±5% for Specified Performance		5		V
Negative Supply Voltage (Note 8)	V_{SS}	±5% for Specified Performance		-15 to -12		V
Positive Supply Current	I_{DD}	CONVST/$\overline{EOC}$ = V_{DD}, AIN = 0V		5	8	mA
Negative Suply Current	I_{SS}	CONVST/$\overline{EOC}$ = V_{DD}, AIN = 0V		-6	-11	mA
Power Dissipation		V_{DD} = +5V, V_{SS} = -15V		115	205	mW
TIMING CHARACTERISTICS (Note 9) (V_{DD} = +5V, V_{SS} = -12V or -15V; T_A = T_{MIN} to T_{MAX})						
CLOCK Pulse Width	t_{CH} t_{CL}	CLOCK HIGH CLOCK LOW	40 60			ns
CONVST/$\overline{EOC}$ Pulse Width	t_{SH} t_{SL}	CONVST/$\overline{EOC}$ HIGH CONVST/$\overline{EOC}$ LOW	40 60			ns
CONVST/$\overline{EOC}$ to CLOCK Skew	t_{SC0} t_{SC1}	Leading CLOCK Leading CLOCK + 1	 275		50	ns
CLOCK to DATA Delay	t_{PD}		25		155	ns

Note 1: Typical change over temp is +1 LSB.
Note 2: FS = +5.000V. Ideal last code transition = FS - 3/2 LSB. Adjusted for offset error.
Note 3: Full Scale Tempco = ΔFS/ΔT, where ΔFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 4: Includes internal reference drift.
Note 5: V_{REF} Tempco = $\Delta V_{REF}/\Delta T$, where ΔV_{REF} is reference voltage change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 6: Output current should not change during conversion.
Note 7: Guaranteed by design, not subject to test.
Note 8: Specified performance with -12V supply is guaranteed by testing offset and full scale errors.
Note 9: Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.

Converter Operation

The MAX170 uses a successive approximation technique to convert an unknown analog input to a 12-bit digital output code. The digital interface requires only three digital lines. Most applications require only a few external passive components to perform the analog-to-digital function. Figure 1 shows the MAX170 in its simplest operational configuration.

Figure 2 shows the MAX170 analog equivalent circuit. The internal voltage output digital-to-analog converter (DAC) is controlled by a successive approximation register (SAR) and has an output impedance of 2.5kΩ. The analog input is connected to the DAC output with a 2.5kΩ resistor. The comparator is essentially a zero-crossing detector with its output feeding back to the SAR input.

Timing and Control

The MAX170 can be used in two different modes: Forced-Start Mode requires an external conversion start signal to initiate the conversions. Self-Start Mode uses an internally generated conversion start signal and causes the MAX170 to convert continuously.

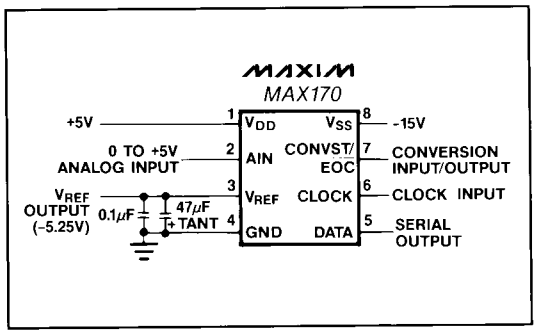


Figure 1. MAX170 Operational Diagram

Serial Output 5.6µs 12-Bit A/D Converter

Pin Description

PIN DIP	PIN SO	NAME	FUNCTION
1	1	V_{DD}	Positive Supply, +5V
2	4	AIN	Analog Input, 0V to +5V Unipolar
3	5	V_{REF}	Reference Voltage Output, -5.25V
	6,7	AGND	Analog Ground. Must be tied to the GND pin.
4	8	GND	Ground
5	9	DATA	Serial Data Output
6	12	CLOCK	Clock Input, TTL/+5V CMOS compatible.
7	13	CONVST/$\overline{EOC}$	Conversion Start Input for three-wire mode; End-of-Conversion output for two-wire mode.
8	16	V_{SS}	Negative Supply, -12V or -15V

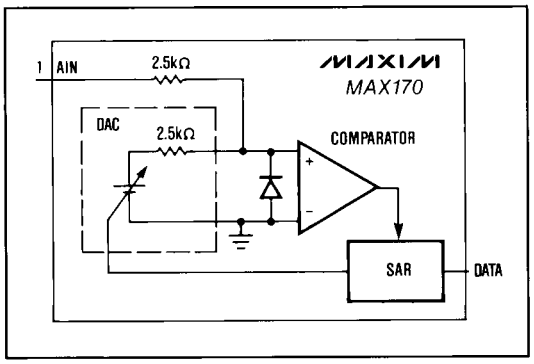


Figure 2. MAX170 Analog Equivalent Circuit

Forced-Start Mode

A conversion cycle is initiated on the rising edge of the conversion start signal (CONVST/$\overline{EOC}$) that is coincident with a falling edge of the CLOCK signal. Figure 3 shows a single conversion cycle with a continuous CLOCK. Once started, a conversion cannot be stopped and transitions at the CONVST/$\overline{EOC}$ input have no effect until the current conversion is completed (minimum of 14 clock cycles from the last rising edge of the conversion start signal).

The conversion start transition causes the SAR to set B11 (MSB) which drives the DAC output to half-scale. The analog input is compared to this value from the time of the conversion start transition until the second falling edge of CLOCK which latches the MSB result and sets the SAR to compare the next bit. The MSB result appears at the DATA output after a delay T_{PD} from the falling edge of CLOCK. Each subsequent bit conversion proceeds similarly until all 12 bits of the DAC have been tried. Conversion is completed at the falling edge of the 13th CLOCK cycle. The DATA output returns high at the falling edge of the 14th CLOCK cycle and remains so until the next conversion sends out its MSB result.

The next conversions can be started on the 14th CLOCK cycle of a previous conversion as shown in Figure 4. This results in the maximum throughput rate of one conversion per 14 CLOCK cycles.

Conversion start transitions must arrive within the setup limits t_{SC0} and t_{SC1} relative to the falling edges of the CLOCK signal to guarantee that the serial DATA output stream will start at the second CLOCK cycle, as shown in Figure 4. Limits t_{SC0} and t_{SC1} apply whether conversion is started directly after a previous cycle on the 14th CLOCK, or if idle CLOCK pulses exist between conversions. Note that bringing CONVST/$\overline{EOC}$ input high on the falling edge of CLOCK 14 allows the maximum time for the internal DAC to settle.

It is possible to operate the MAX170 at a higher or lower clock rate than specified. At higher than 2.5MHz clock rates, the INL will degrade as shown in Figure 5. But at lower speeds, there will be no degradation of the INL.

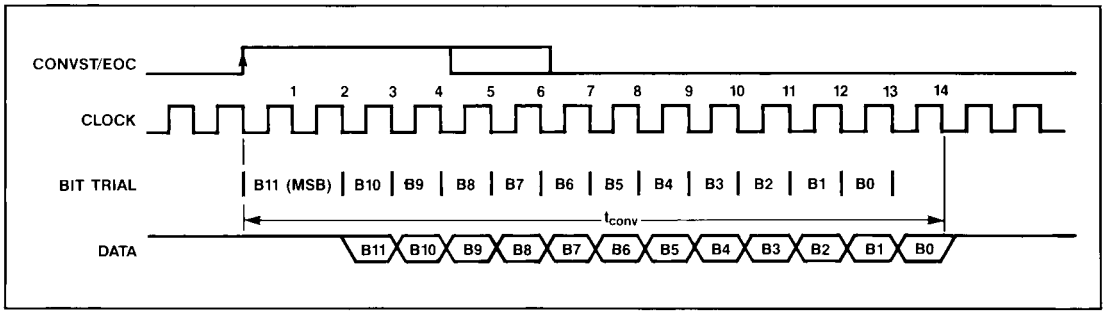


Figure 3. Forced-Start Mode Timing (14 Clocks Per Conversion Cycle)

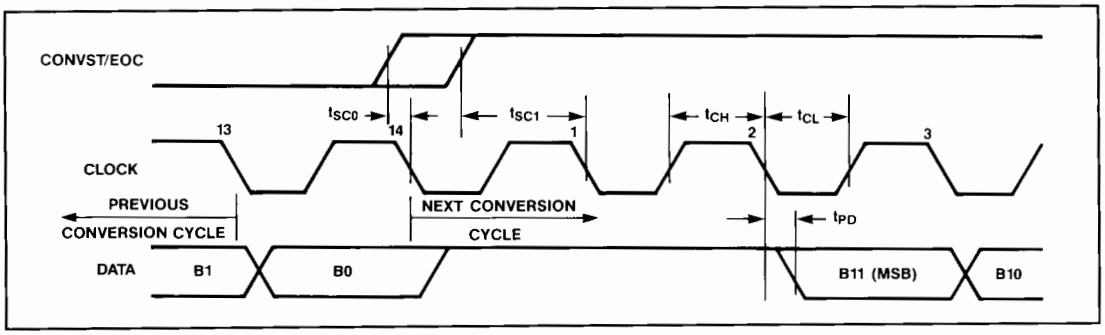


Figure 4. MAX170 Timing Diagram

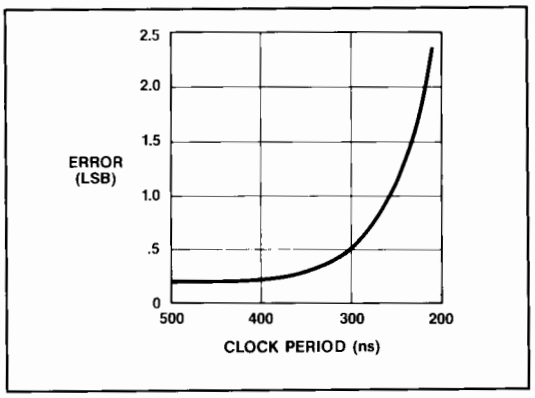


Figure 5. Typical INL vs Clock Rate for MAX170

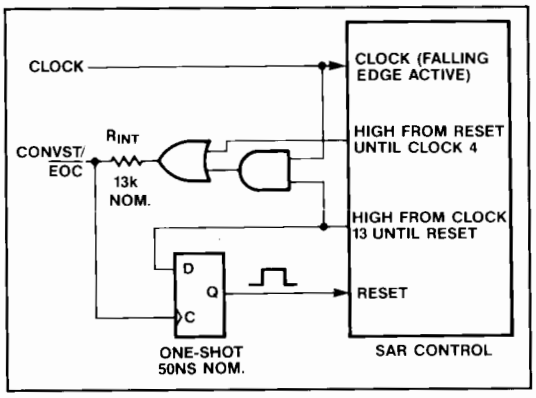


Figure 6. MAX170 Logic Equivalent for Start and Clock Inputs

Self-Start Mode

The CONVST/$\overline{EOC}$ pin is internally driven by a conversion complete signal through a 13kΩ (typical value) resistor, R_{INT} (Figure 6). By leaving this pin open-circuited, the MAX170 will generate its own conversion start input and run at a rate of one conversion for every 13 CLOCK cycles. The signal at the CONVST/$\overline{EOC}$ pin can be buffered and used as a framing signal to synchronize the serial data (Figure 7).

The CLOCK rate in the self-start mode will be limited by capacitive loading of the CONVST/$\overline{EOC}$ pin. Therefore, no more than one HCMOS logic input and a minimum of PC board capacitance should be connected to this pin when high speed conversions are desired. The maximum CLOCK rate for this mode will be limited by the requirement that the conversion start signal must cross the logic high threshold (V_{IH} = 2.4V) of this input at least 200ns before the falling edge of the first clock cycle (t_{SC1}).

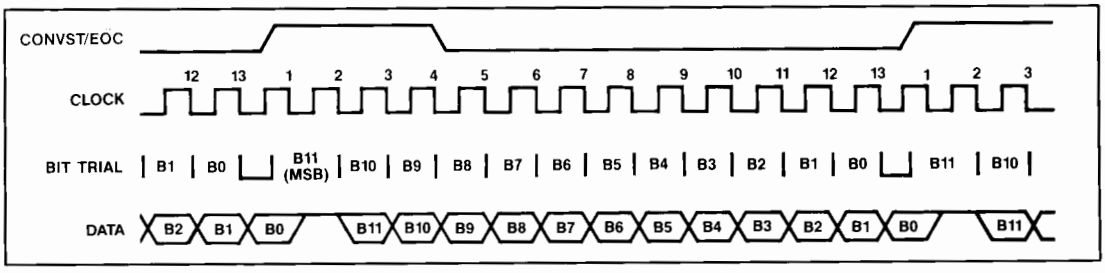


Figure 7. Self-Start Mode Timing (13 Clocks Per Conversion Cycle)

Serial Output 5.6µs 12-Bit A/D Converter

For instance, a minimal buffer circuit of one HCMOS gate input (10pF) connected to the CONVST/EOC pin and 15pF of PC board capacitance result in a total load of 25pF. Since the CONVST/EOC pin is internally driven high through the R_{INT} during the 13th clock period, an R-C charging delay results. (The value of R_{INT} depends on process variations, and can have a maximum value of 17kΩ.) The R-C delay plus the 200ns required setup time cannot exceed the half-period of the CLOCK signal. Assuming a 50% duty cycle, the maximum CLOCK frequency that can be used in the self-start mode would be:

f_{CLOCK} (MAX) = 1 / (2 (0.7 $R_{INT}C_{LOAD}$ + 200ns)) = 1MHz

with R_{INT} = 17kΩ, and C_{LOAD} = 25pF.

Output Coding

The data output from MAX170 is in the Straight Binary Code. Other common binary codes, such as 2's complement, offset binary or complementary codes, can be obtained by inverting either the serial data, or the proper bit(s) of the parallel data in software or hardware.

Applications

Unipolar Input Operation

Figure 8 shows the nominal input/output transfer function of the MAX170. Code transitions occur halfway between successive integer LSB values. The output coding is binary with 1LSB = 1.22mV (5V/4096).

Offset and Full Scale Adjustment

In applications where the offset and full scale range have to be adjusted for the ADC, use the circuit shown in Figure 9. Note that the amplifier shown could also have been a sample-and-hold. The offset should be adjusted first. Apply 1/2 LSB (0.61mV) at the analog input and adjust the offset of the amplifier until the digital output code changes between 0000 0000 0000 and 0000 0000 0001.

To adjust the full scale range, apply FS - 3/2LSB (4.9817V) at the analog input and adjust R1 until the output code changes between 1111 1111 1110 and 1111 1111 1111.

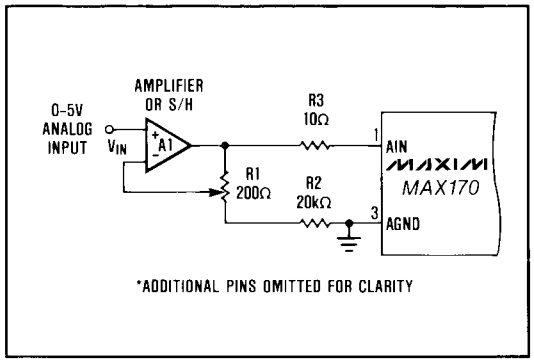


Figure 9. Full-Scale Adjustment

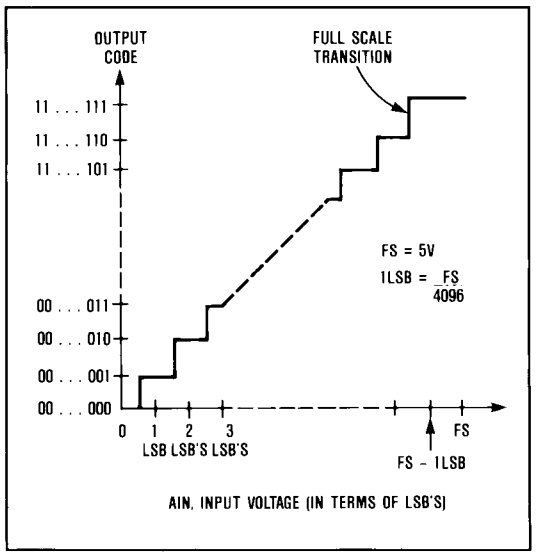


Figure 8. MAX170 Transfer Function

Bipolar Input Operation

Bipolar operation can be achieved in two modes: non-inverting and inverting. For both cases the amplifier shown in the circuits can be replaced by the AD585 or HA5320 sample-and-hold amplifiers. Several different input ranges are possible by selecting the values for the scaling resistors as shown in Tables 1 and 2.

Figure 10 shows the bipolar operation in the non-inverting mode, where the output coding is offset binary. Figure 11 shows the ideal transfer function for this mode.

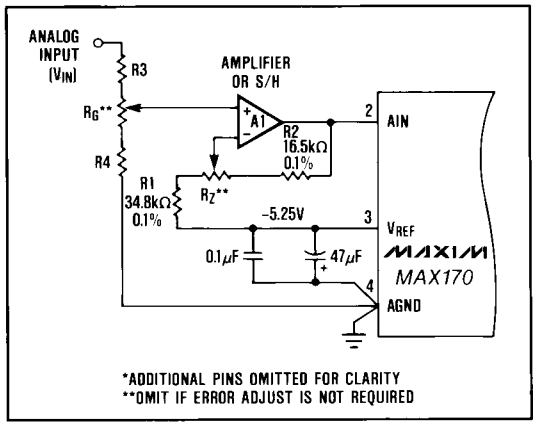


Figure 10. MAX170 Non-Inverting Bipolar Operation

Table 1. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 10

V_{IN} Range (Volts)	R3* (kΩ)	R4* (kΩ)	R_Z (Ω)	R_G (Ω)	1/2LSB (mV)	FS/2-3/2LSBs (Volts)
±2.5	3.83	8.25	500	500	0.61	2.49817
±5.0	33.2	16.9	500	1000	1.22	4.99634
±10.0	47.5	9.53	500	500	2.44	9.99268

*R3 and R4 have a 0.1% tolerance. All resistors are standard EIA/MIL decade values.

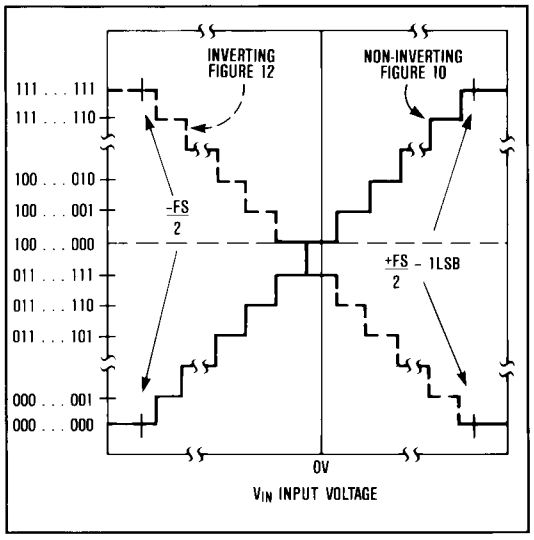


Figure 11. Ideal Input/Output Transfer Characteristics for the Bipolar Circuits Shown in Figures 10 and 12

Figure 12 shows the bipolar operation in the inverting mode where the output coding is complementary offset binary. Figure 11 shows the ideal transfer function for the circuit in Figure 12.

The resistors used in bipolar applications should be of the same type and from the same manufacturer to obtain low temperature drift. 0.1% resistors are recommended for applications where offset and full scale adjustments must be made in bipolar circuits. If high tolerances are used, larger value potentiometers must be used and this results in poor sensitivity and higher temperature drifts.

Offset and Full Scale Adjustment

Offset should always be adjusted before full scale. For both circuits apply +1/2LSB to the analog input (see Tables 1 and 2) and adjust R_Z until the output code flickers bewteen the following codes:

For Non-Inverting (Figure 10) 1000 0000 0000
1000 0000 0001

For inverting (Figure 12) 0111 1111 1111
0111 1111 1110

Apply FS - 3/2LSB (See Tables 1 and 2) to the input and adjust R_G until the ADC output code flickers between the following codes:

For Non-inverting (Figure 10) 1111 1111 1110
1111 1111 1111

For inverting (Figure 12) 0000 0000 0001
0000 0000 0000

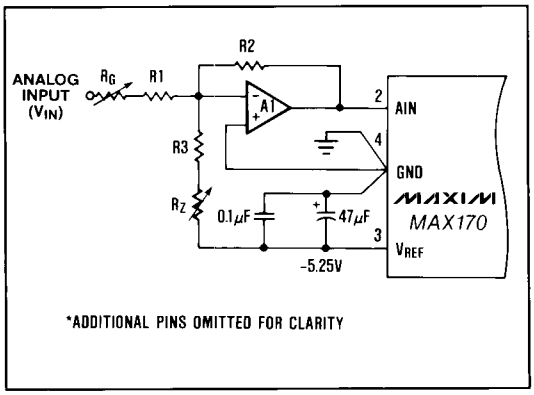


Figure 12. MAX170 Inverting Bipolar Operation

Table 2. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 12

V_{IN} Range (Volts)	R1* (kΩ)	R2* (kΩ)	R3* (kΩ)	R_Z (Ω)	R_G (Ω)	1/2LSB (mV)	FS/2-3/2 LSBs (Volts)
±2.5	20	20.5	42.2	2000	1000	0.61	2.49817
±5.0	20	10.2	21	1000	1000	1.22	4.99634
±10.0	20	5.11	10.5	500	1000	2.44	9.99268

*R1, R2 and R3 have a 0.1% tolerance. All resistors are standard EIA/MIL decade values.

MAX170 to Sample-and-Hold Interface

The analog input to the MAX170 must be stable to within ±1/2LSB during the entire conversion for specified 12-bit accuracy. This limits the input signal bandwidth to a few Hz for sinusoidal inputs. For higher bandwidth signals, a sample-and-hold should be used.

The signal that starts the MAX170 conversions can be used to provide the TRACK/HOLD signal to the sample-and-hold amplifier. The MAX170's DAC is switched at approximately the same time as the sample-and-hold amplifier starts holding the signal. The sample-and-hold amplifier should switch to the HOLD mode before there are any disturbances on the input signal, otherwise code dependent errors will be observed. These can be avoided by starting the MAX170 slightly after the TRACK/HOLD signal by using a gate delay. For synchronous conversion start and CLOCK as described above, the maximum allowable hold settling time for the sample-and-hold is 600ns.

Serial Output 5.6μs 12-Bit A/D Converter

Figure 13 shows the MAX170 to AD585 sample-and-hold interface circuit. In this example the analog input range is ±2.5V but other voltage ranges can also be configured.

The maximum sampling rate is 125kHz with a 2.5MHz clock and 64.5kHz with a 1MHz clock allowing for a 3μs sample-and-hold acquisition time. At the 2.5MHz clock rate a faster sample-and-hold amplifier, such as the HA-5320, is recommended (Figure 14).

MAX170 in Remote Applications

Figure 15 shows a MAX170 operating in the self-start mode with a three-wire digital interface to a 12-bit parallel output port. The analog input is referenced to signal ground at the GND pin of the MAX170. CMOS inverters isolate the CONVST/$\overline{EOC}$ pin from the capacitive load of the wire interface and the multiple register inputs. The parallel data outputs are updated at the rising edge of the $\overline{DATA\ VALID}$ signal.

MAX170 with Opto-Isolators

Serial interface simplifies opto-coupled or transformer-coupled A/D converter applications. For example, transducer outputs often require electrical isolation to separate the control electronics from hazardous electrical conditions, provide noise immunity or bridge large differences in ground potential. Isolation amplifiers that are typically used for accomplishing this cost up to $100 per channel. The MAX170 provides a low cost alternative to isolation amplifiers, and it performs the A/D conversion as well (Figure 16A). The A/D converter results are transmitted across a 1500V isolation barrier provided by three 6N136 optical isolators. 74HC595 3-statable shift registers then reconstruct a 12-bit parallel data output. Figure 16B shows the timing diagram for this application. The conversion speed is limited by the speed of the opto-isolators, and with a 140kHz clock conversion time is 100μs. For those who prefer even greater space savings, Maxim's MAX171 that combines the MAX170, three opto-isolators and load resistors in a 16-lead DIP package, is recommended.

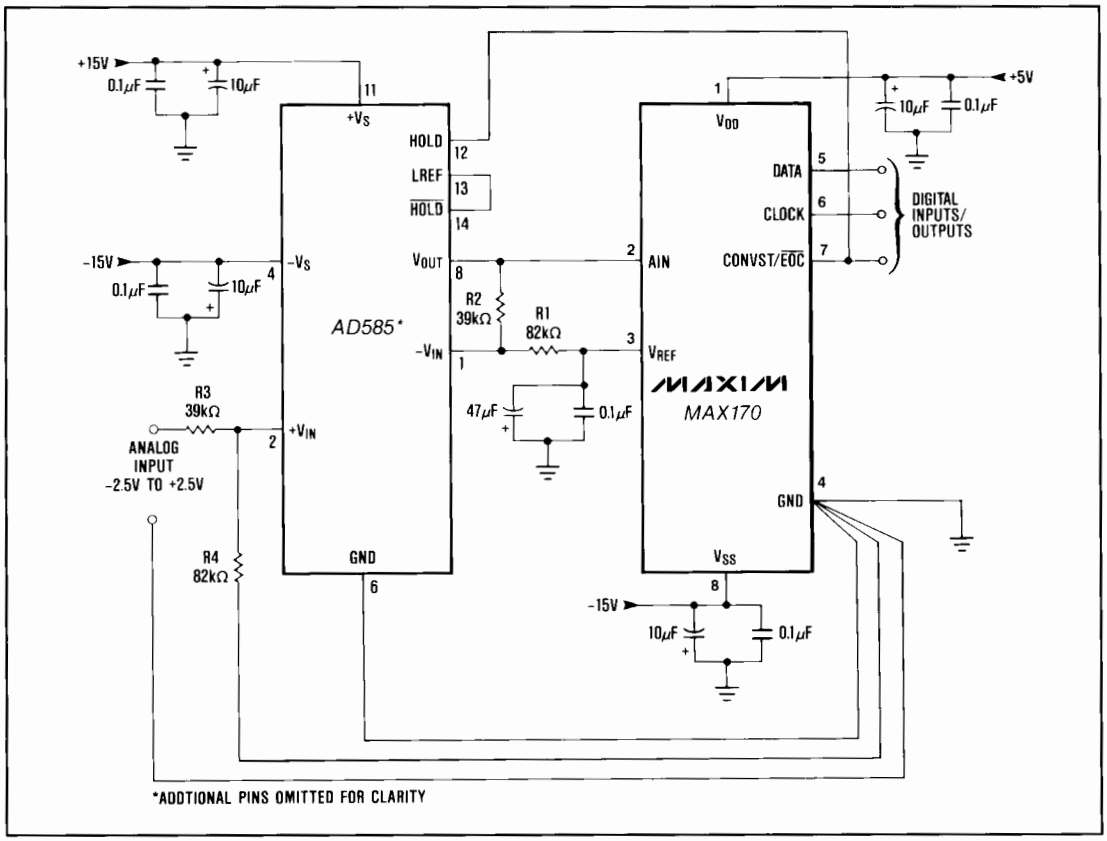


Figure 13. MAX170-AD585 Sample-and-Hold Interface

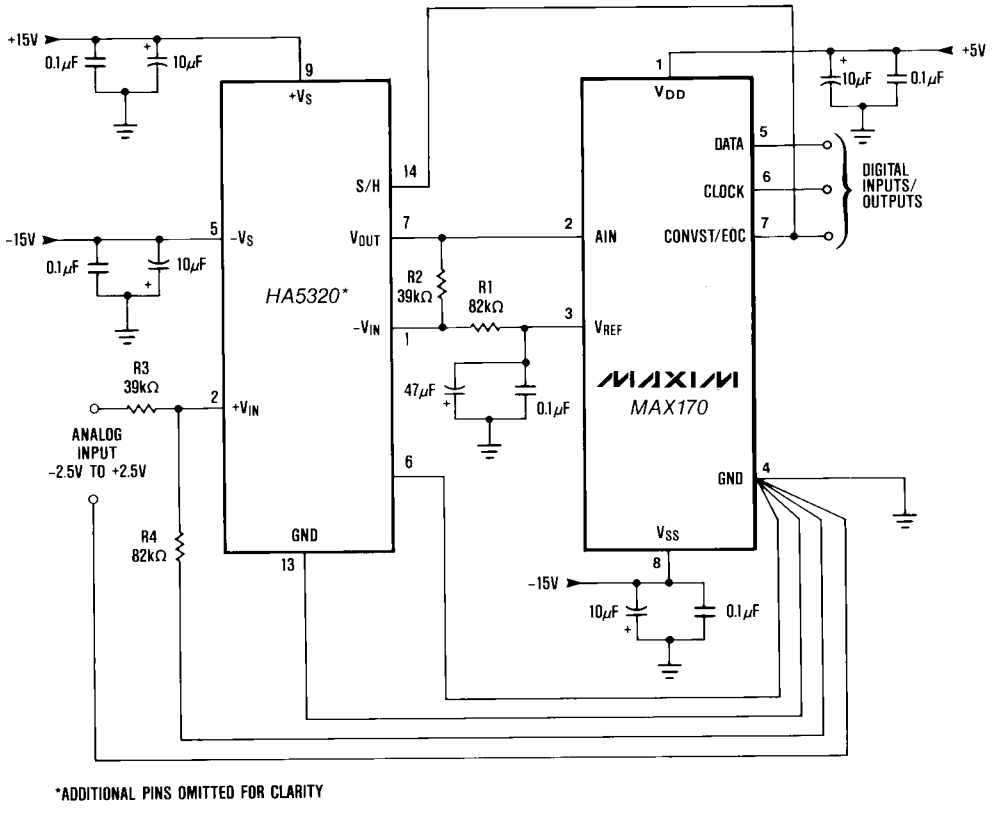


Figure 14. MAX170-HA5320 Sample-and-Hold Interface

Serial Output 5.6µs 12-Bit A/D Converter

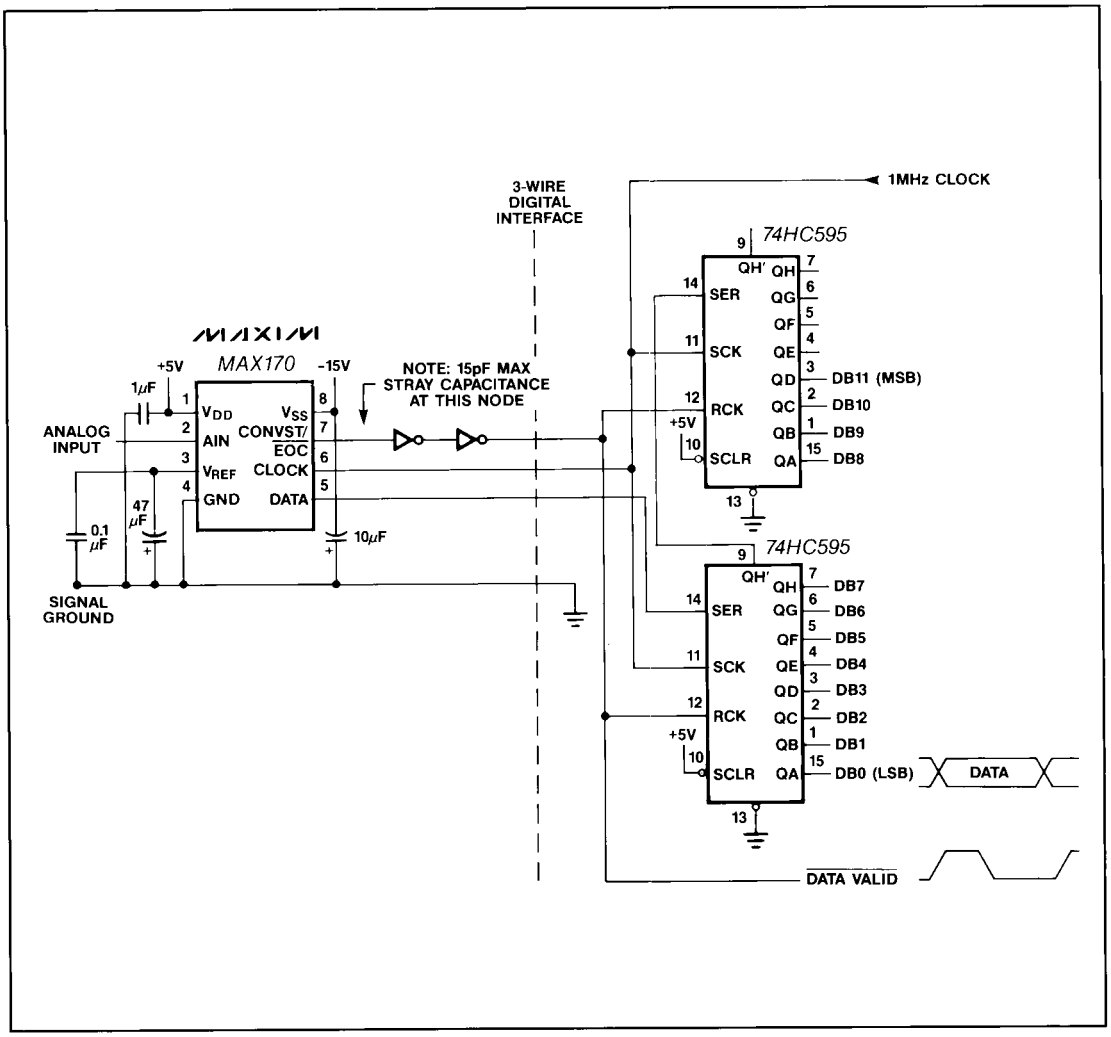


Figure 15. Self-Start Mode

Application Hints

Physical Layout

For best system performance printed circuit boards should be used for the MAX170. Wire wrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are kept separated from each other as much as possible. Care should be taken not to run analog and digital lines parallel to each other or digital lines underneath the MAX170 package.

Grounding

Figure 17 shows the recommended system ground connections. A single point analog STAR ground should be established at pin 4 (GND) of the MAX170. All grounds should be connected to this STAR ground. The ground return to the power supply from this STAR ground should be low impedance for noise-free operation of the MAX170.

Serial Output 5.6µs 12-Bit A/D Converter

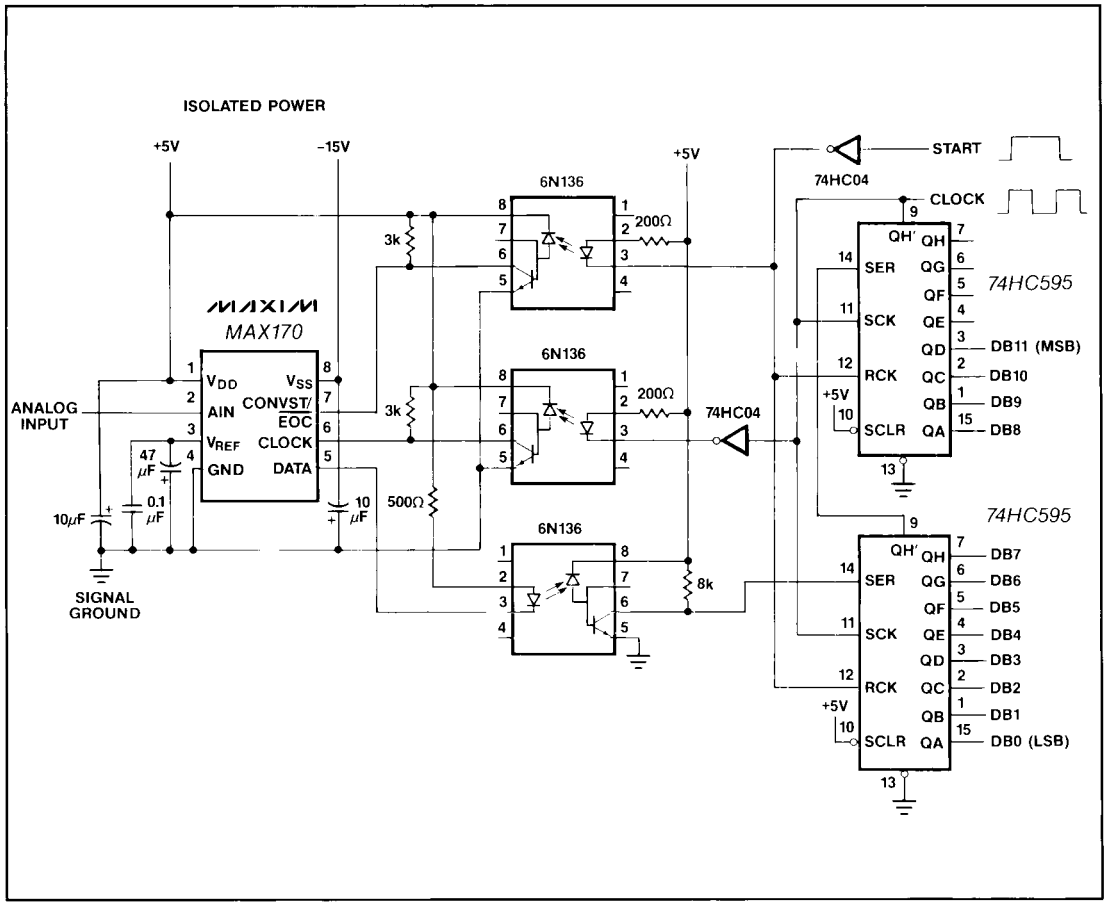


Figure 16A. 12-Bit Isolated A/D Converter. Conversion Time in 100µs

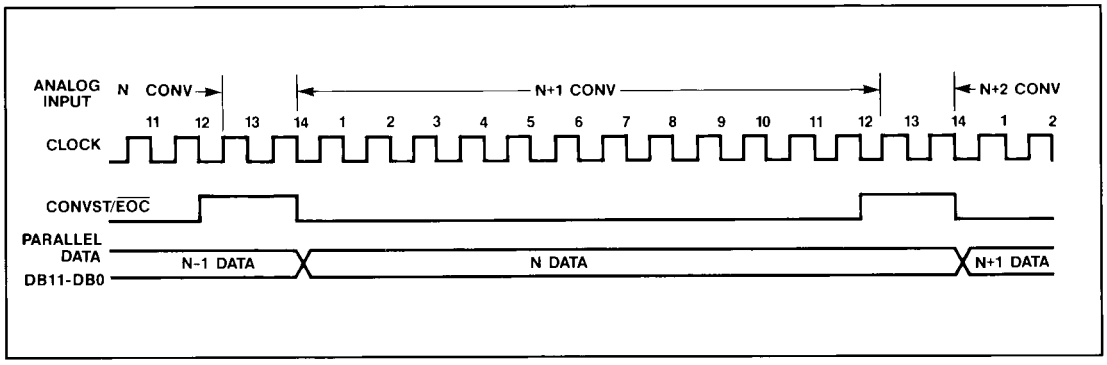


Figure 16B. Timing for Isolated A/D Interface

Serial Output 5.6μs 12-Bit A/D Converter

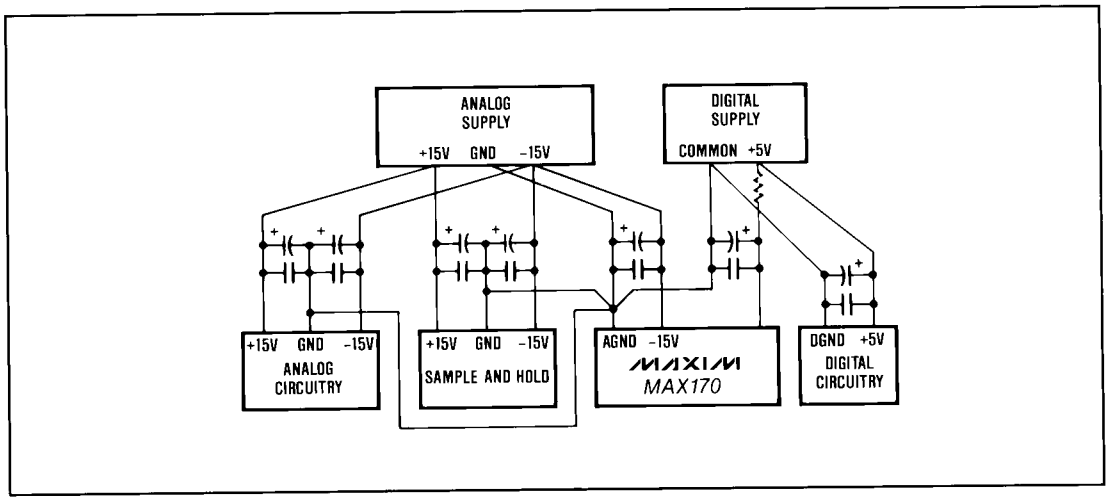


Figure 17. Power Supply Grounding

Power Supply Bypassing

The high speed comparator in the MAX170 is sensitive to high frequency noise in the V_{DD} and V_{SS} power supplies. These supplies should be by-passed to the analog STAR ground with 0.1μF and 10μF by-pass capacitors with minimum lead length for supply noise rejection. If the +5V power supply is very noisy, a small resistor (10-20Ω) can be connected as shown in Figure 17 to filter external noise.

Internal Reference

The MAX170 has an on-chip reference that is built with a buffered and temperature compensated buried zener diode, laser-trimmed to -5.25V ±1%. Its output is connected to the V_{REF} pin and also drives the internal DAC. This output can be used as a reference voltage source for other components.

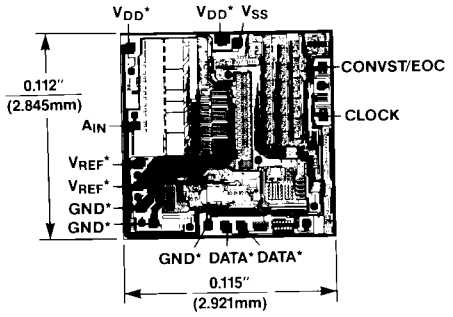
For minimal transition noise, the V_{REF} pin must be decoupled with a 47μF tantalum capacitor in parallel with a 0.1μF capacitor to filter out the wideband noise of the zener diode and to provide low impedance at high frequencies (Figure 1). This capacitor also creates the dominant pole of the reference buffer amplifier for stability. If this capacitor is not used, the reference will oscillate. Since the MAX170 buffer amplifier is designed to be stable with this capacitor, no series resistance should be used between the V_{REF} pin and the capacitor. This capacitor must not be less than 4.7μF.

Driving the Analog Input

The input signal leads to AIN and GND should be as short as possible to minimize noise pick-up. If the leads must be long, use shielded cables to minimize noise pick-up.

The input impedance at the AIN pin is typically 2.5kΩ. The amplifier driving AIN must have low enough DC output impedance for low gain error. Furthermore, low AC output impedance is also required since the analog input current is modulated at the clock rate during a conversion. The output impedance of the driving amplifier is reduced by the loop gain at the frequency of interest. With a maximum clock rate of 2.5MHz, it is possible to drive the MAX170 with amplifiers like the OP-42, AD711, or OP-27. At 1MHz clock rate a MAX400 or OP-07 can also be used.

Chip Topography



** Pads with the same name must be bonded together.*

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