19-1488; Rev 0; 7/99

Chemistry-Independent, Level 2 Smart Battery Charger

General Description

The MAX1667 provides the power control necessary to charge batteries of any chemistry. All charging functions are controlled through the Intel System Management Bus (SMBus™) interface. The SMBus 2-wire serial interface sets the charge voltage and current and provides thermal status information. The MAX1667 functions as a Level 2 charger, compliant with the Duracell/Intel Smart Battery Charger Specification.

In addition to the feature set required for a Level 2 charger, the MAX1667 generates interrupts to signal the host when power is applied to the charger or when a battery is installed or removed. Additional status bits allow the host to check whether the charger has enough input voltage, and whether the voltage on or current into the battery is being regulated. This allows the host to determine when lithium-ion (Li+) batteries have completed the charge without interrogating the battery.

The MAX1667 is available in a 20-pin SSOP with a 2mm profile height.

Applications

Notebook Computers
Personal Digital Assistants
Charger Base Stations
Phones

Pin Configuration appears at end of data sheet.

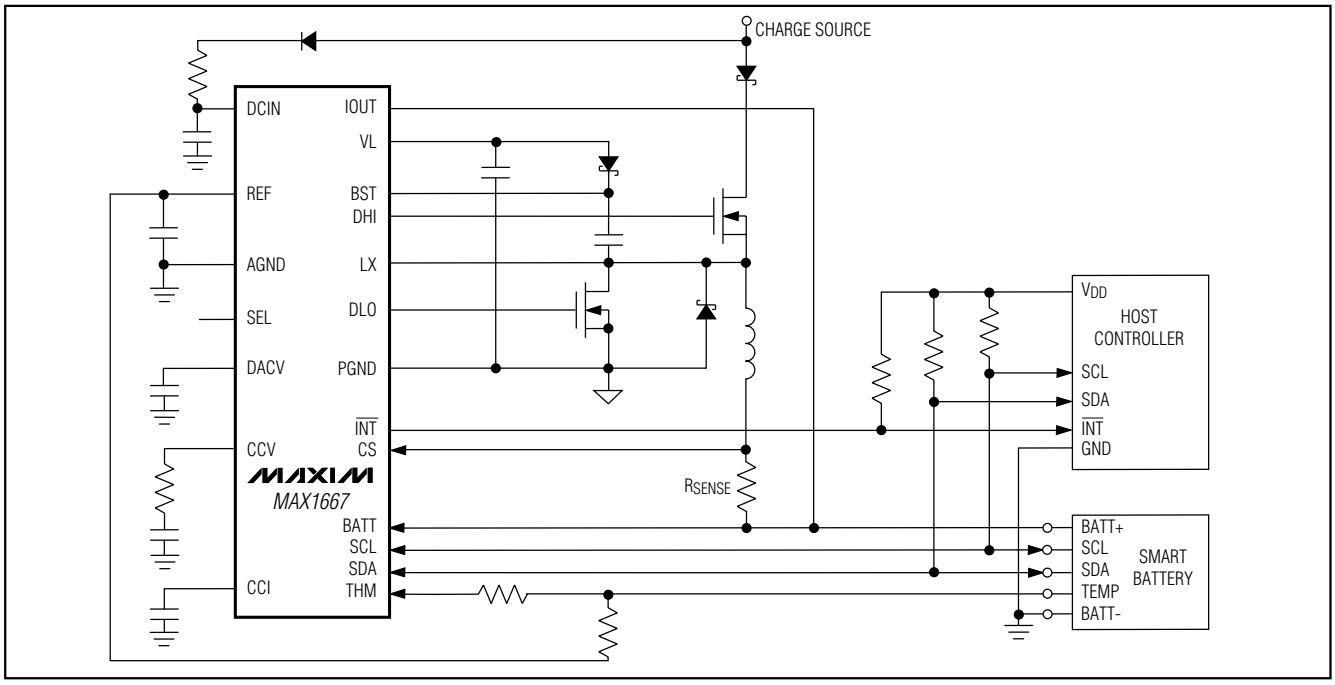
Features

- **Charges Any Battery Chemistry: Li+, NiCd, NiMH, Lead Acid, etc.**
- **SMBus 2-Wire Serial Interface**
- **Compliant with Duracell/Intel Smart Battery Charger Specification Rev. 1.0**
- **4A, 3A, or 1A (max) Battery Charge Current**
- **5-Bit Control of Charge Current**
- **Up to 18.4V Battery Voltage**
- **11-Bit Control of Voltage**
- **±1% Voltage Accuracy**
- **Up to +28V Input Voltage**
- **Battery Thermistor Fail-Safe Protection**
- **Greater than 95% Efficiency**
- **Synchronous Rectifier**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1667EAP	-40°C to +85°C	20 SSOP

Typical Operating Circuit



SMBus is a trademark of Intel Corp.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 1-800-835-8769.

Chemistry-Independent, Level 2 Smart Battery Charger

ABSOLUTE MAXIMUM RATINGS

DCIN to AGND .....-0.3V to +30V
BST to AGND.....-0.3V to +36V
BST, DHI to LX.....-0.3V to +6V
LX, IOUT to AGND.....-0.3V to +30V
THM, CCI, CCV, DACV, REF, DLO to AGND .....-0.3V to (VL + 0.3V)
VL, SEL, $\overline{INT}$, SDA, SCL to AGND .....-0.3V to +6V
BATT, CS+ to AGND .....-0.3V to +20V
PGND to AGND .....-0.3V to +0.3V
SDA, $\overline{INT}$ Current 50mA
VL Current 50mA
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 8mW/°C above +70°C) 640mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DCIN} = 18V, internal reference, 1µF capacitor at REF, 1µF capacitor at VL, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY AND REFERENCE						
DCIN Input Voltage Range			7.5		28	V
DCIN Quiescent Current	7.5V < V_{DCIN} < 28V, logic inputs = VL			4	6	mA
VL Output Voltage	7.5V < V_{DCIN} < 28V, no load		5.15	5.4	5.65	V
VL Load Regulation	I_{LOAD} = 0 to 10mA				100	mV
VL AC_PRESENT Trip Point			3.20	4	5.15	V
REF Output Voltage	0 < I_{SOURCE} < 500µA		4.055	4.096	4.137	V
SWITCHING REGULATOR						
Oscillator Frequency	Not in dropout		200	250	300	kHz
DHI Maximum Duty Cycle	In dropout		96.5	97.7		%
DHI On-Resistance	High or low			4	7	Ω
DLO On-Resistance	High or low			5	8	Ω
BATT Input Current (Note 1)	VL < 3.2V, V_{BATT} = 12V			1	5	µA
	VL > 5.15V, V_{BATT} = 12V			350	500	
CS Input Current (Note 1)	VL < 3.2V, V_{CS} = 12V			1	5	µA
	VL > 5.15V, V_{CS} = 12V			170	400	
BATT, CS Input Voltage Range			0		19	V
CS to BATT Single-Count Current-Sense Voltage	ChargingCurrent() = 0x0080 (128mA)			5		mV
CS to BATT Full-Scale Current-Sense Voltage	SEL = VL (4A), ChargingCurrent() = 0x0F80 (3968mA)		145	160	175	mV
Voltage Accuracy	ChargingVoltage() = 0x3130 (12,592mV) and 0x41A0 (16,800mV)	T_A = +25°C	-0.8		0.8	%
		T_A = T_{MIN} to T_{MAX}	-1.0		1.0	
	ChargingVoltage() = 0x1060 (4192mV) and 0x20D0 (8400mV)	T_A = +25°C	-1.0		1.0	
		T_A = T_{MIN} to T_{MAX}	-3.0		3.0	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = 18V, internal reference, 1µF capacitor at REF, 1µF capacitor at VL, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ERROR AMPLIFIERS						
GMV Amplifier Transconductance				1.4		mA/V
GMI Amplifier Transconductance				0.2		mA/V
GMV Amplifier Maximum Output Current				±80		µA
GMI Amplifier Maximum Output Current				±200		µA
CCV Clamp Voltage with Respect to CCI	1.1V < V_{CCI} < 3.5V		25	80	200	mV
CCI Clamp Voltage with Respect to CCV	1.1V < V_{CCV} < 3.5V		25	80	200	mV
TRIP POINTS AND LINEAR CURRENT SOURCES						
BATT POWER_FAIL Threshold	BATT rising		93	95	97	% of V_{DCIN}
BATT POWER_FAIL Threshold Hysteresis				1		% of V_{DCIN}
THM THERMISTOR_OR Overrange Trip Point	THM falling		89	91	93	% of V_{REF}
THM THERMISTOR_COLD Trip Point	THM falling		74	75.5	77	% of V_{REF}
THM THERMISTOR_HOT Trip Point	THM falling		22	23.5	25	% of V_{REF}
THM THERMISTOR_UR Underrange Trip Point	THM falling		3	4.5	6	% of V_{REF}
THM THERMISTOR_OR, _COLD, _HOT, _UR Trip Point Hysteresis				0.5		% of V_{DCIN}
IOUT Output Current	V_{IOUT} = 0	ChargingCurrent() = 0x0001 to 0x007F (127mA)	5	7	9	mA
		ChargingCurrent() = 0x0000			10	µA
	V_{IOUT} = 17V, ChargingCurrent() = 0x0001 to 0x007F (127mA)		5			mA
IOUT Leakage Current	V_{DCIN} = 0, V_{IOUT} = 20V				10	µA
CURRENT- AND VOLTAGE-SETTING DACs						
CDAC Current-Setting DAC Resolution	Guaranteed monotonic		5			Bits
VDAC Voltage-Setting DAC Resolution	Guaranteed monotonic		11			Bits
LOGIC LEVELS						
SDA, SCL Input Voltage Low					0.8	V
SDA, SCL Input Voltage High			2.2			V
SDA, SCL Input Bias Current			-1		1	µA
SDA Output Low Sink Current	V_{SDA} = 0.6V		6			mA

Note 1: When DCIN is less than 4V, VL is less than 3.2V, causing the battery current to be typically 2µA (CS plus BATT input current).

Chemistry-Independent, Level 2 Smart Battery Charger

ELECTRICAL CHARACTERISTICS

(V_{DCIN} = 18V, internal reference, 1µF capacitor at REF, 1µF capacitor at VL, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. Limits over this temperature range are guaranteed by design.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND REFERENCE					
DCIN Quiescent Current	7.5V < V_{DCIN} < 28V, logic inputs = VL		4	6	mA
VL Output Voltage	7.5V < V_{DCIN} < 28V, no load	5.15	5.4	5.65	V
REF Output Voltage	0 < I_{SOURCE} < 500µA	4.055		4.137	V
SWITCHING REGULATOR					
Oscillator Frequency	Not in dropout	200	250	310	kHz
DHI Maximum Duty Cycle	In dropout	96.5			%
DHI On-Resistance	High or low		4	7	Ω
DLO On-Resistance	High or low		5	8	Ω
BATT Input Current (Note 1)	VL < 3.2V, V_{BATT} = 12V			5	µA
CS Input Current (Note 1)	VL < 3.2V, V_{CS} = 12V			5	µA
CS to BATT Full-Scale Current-Sense Voltage	V_{SEL} = VL, ChargingCurrent() = 0x0F80 (128mA)	145	160	175	mV
Voltage Accuracy	ChargingVoltage() = 0x3130 (12,592mV), ChargingVoltage() = 0x41A0 (16,800mV)	-1.0		1.0	%
	ChargingVoltage() = 0x1060 (4192mV), ChargingVoltage() = 0x20D0 (8400mV)	-3.0		3.0	
TRIP POINTS AND LINEAR CURRENT SOURCES					
THM THERMISTOR_OR Overrange Trip Point	THM falling	88.5		93.5	% of V_{REF}
THM THERMISTOR_COLD Trip Point	THM falling	73.5		77.5	% of V_{REF}
THM THERMISTOR_HOT Trip Point	THM falling	21.5		25.5	% of V_{REF}
THM THERMISTOR_UR Underrange Trip Point	THM falling	2.5		6.5	% of V_{REF}
THM THERMISTOR_OR, _COLD, _HOT, _UR Trip Point Hysteresis			1		%
LOGIC LEVELS					
SDA, SCL Input Voltage Low				0.5	V
SDA, SCL Input Voltage High		2.2			V
SDA, SCL Input Bias Current		-1		1	µA
SDA Output Low Sink Current	V_{SDA} = 0.6V	6			mA

TIMING CHARACTERISTICS (Figures 1 and 2)

(**T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Serial-Clock High Period	t_{HIGH}		4			µs
SCL Serial-Clock Low Period	t_{LOW}		4.7			µs
Start-Condition Setup Time	$t_{SU:STA}$		4.7			µs
Start-Condition Hold Time	$t_{HD:STA}$		4			µs
SDA Valid to SCL Rising-Edge Setup Time, Slave Clocking in Data	$t_{SU:DAT}$		250			ns
SCL Falling Edge to SDA Transition	$t_{HD:DAT}$		0			ns
SCL Falling Edge to SDA Valid, Master Clocking in Data	t_{DV}				1	µs

TIMING CHARACTERISTICS (Figures 1 and 2)

(**T_A = -40°C to +85°C**, unless otherwise noted. Limits over this temperature range are guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Serial-Clock High Period	t_{HIGH}		4			µs
SCL Serial-Clock Low Period	t_{LOW}		4.7			µs
Start-Condition Setup Time	$t_{SU:STA}$		4.7			µs
Start-Condition Hold Time	$t_{HD:STA}$		4			µs
SDA Valid to SCL Rising-Edge Setup Time, Slave Clocking in Data	$t_{SU:DAT}$		250			ns
SCL Falling Edge to SDA Transition	$t_{HD:DAT}$		0			ns
SCL Falling Edge to SDA Valid, Master Clocking in Data	t_{DV}				1	µs

Chemistry-Independent, Level 2 Smart Battery Charger

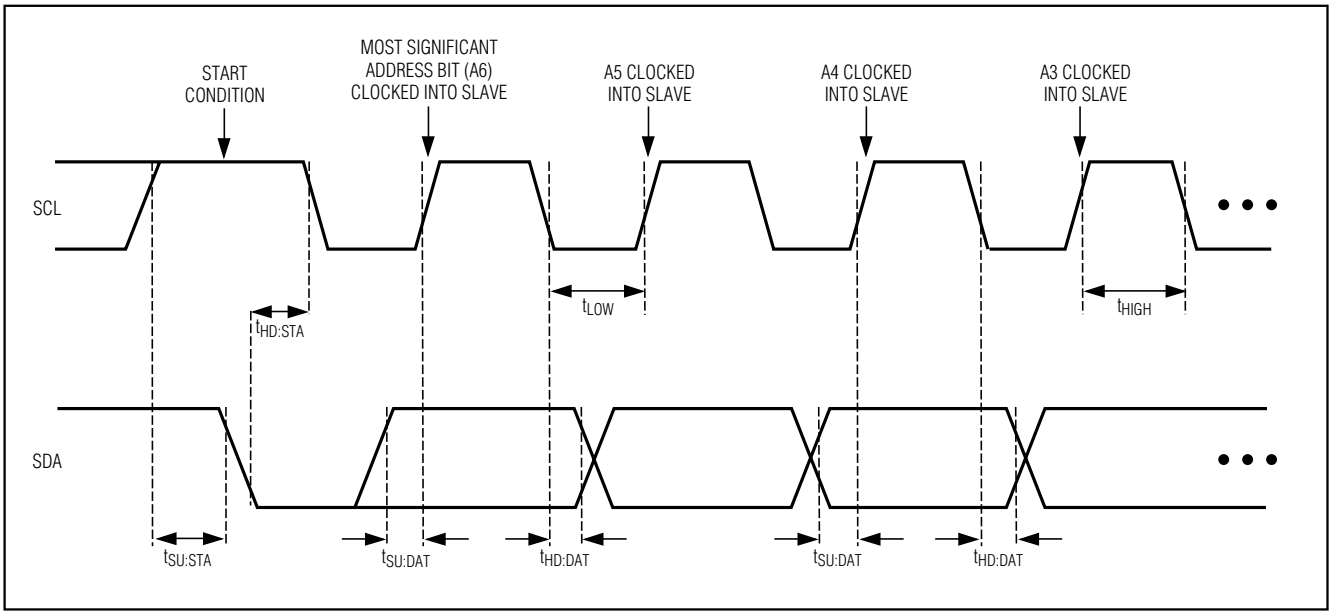


Figure 1. SMBus Serial-Interface Timing—Address

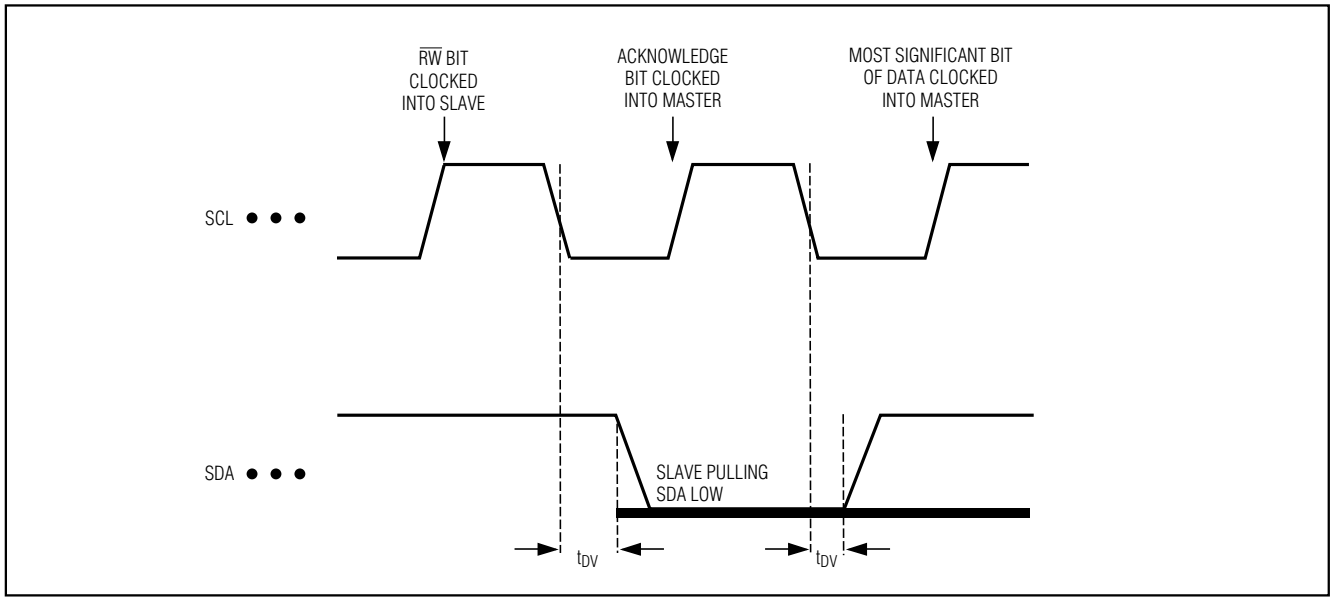
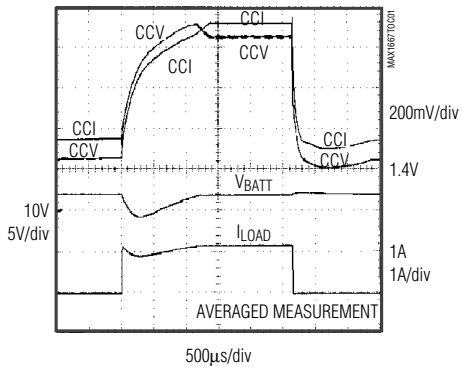


Figure 2. SMBus Serial-Interface Timing—Acknowledge

Typical Operating Characteristics

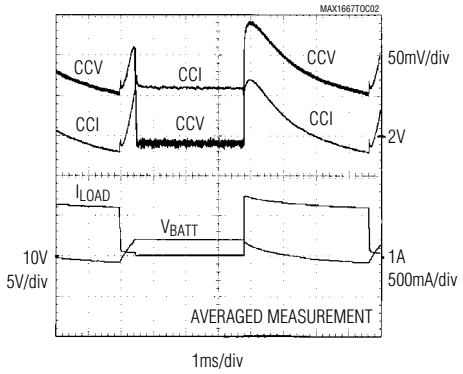
(Circuit of Figure 7, T_A = +25°C, unless otherwise noted.)

LOAD TRANSIENT (VOLTAGE REGULATION WITH CURRENT LIMIT)



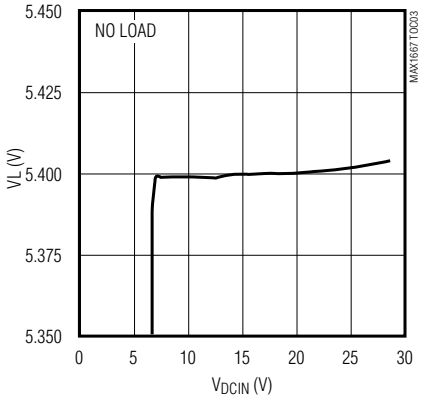
V_{DCIN} = 18V
ChargingVoltage() = 12,000mV
ChargingCurrent() = 1500mA

LOAD TRANSIENT (WITH CHANGE IN REGULATION LOOP)

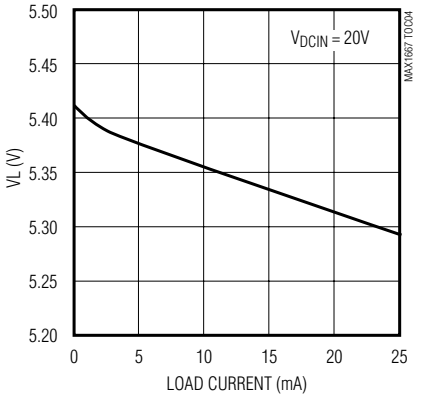


V_{DCIN} = 18V
ChargingVoltage() = 12,000mV
ChargingCurrent() = 1500mA

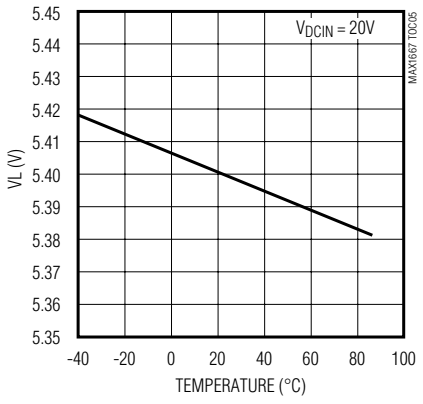
VL LINE REGULATION



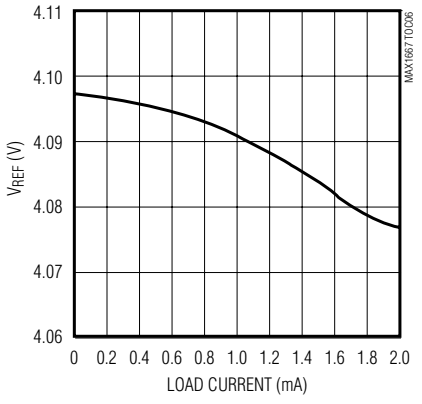
VL LOAD REGULATION



VL vs. TEMPERATURE



V_{REF} LOAD REGULATION

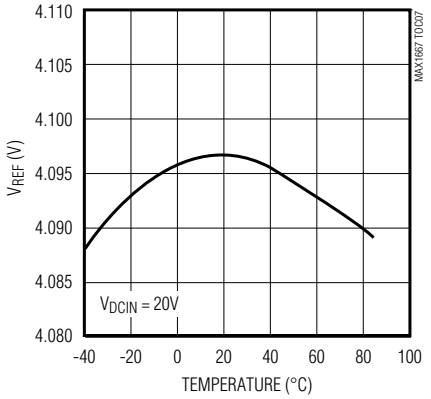


Chemistry-Independent, Level 2 Smart Battery Charger

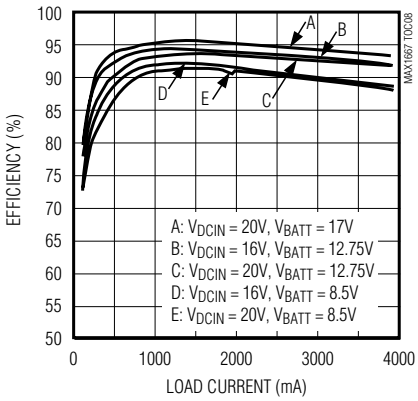
Typical Operating Characteristics (continued)

(Circuit of Figure 7, T_A = +25°C, unless otherwise noted.)

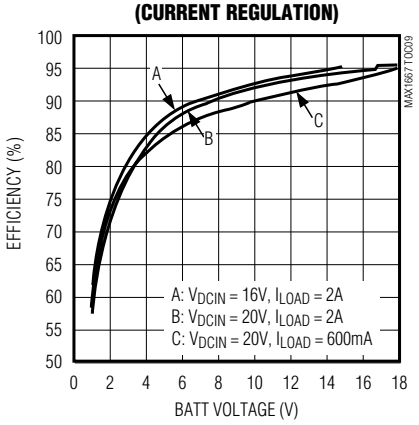
V_{REF} vs. TEMPERATURE



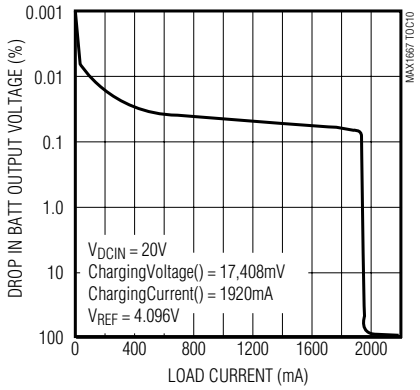
EFFICIENCY vs. LOAD CURRENT (VOLTAGE REGULATION)



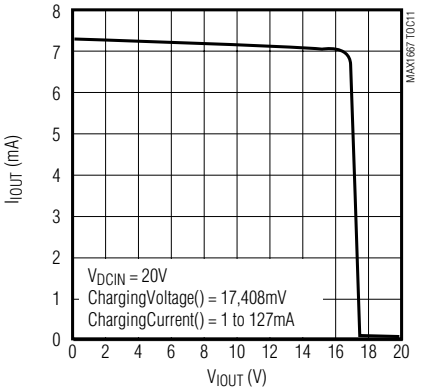
EFFICIENCY vs. BATT VOLTAGE (CURRENT REGULATION)



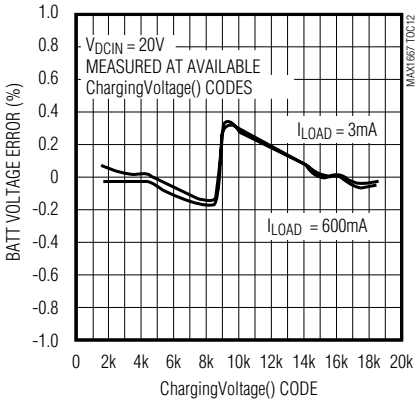
OUTPUT V-I CHARACTERISTIC (SWITCHING REGULATOR)



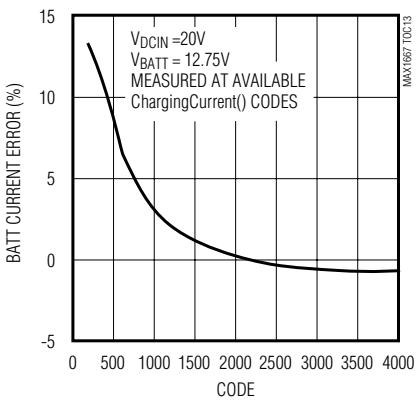
OUTPUT V-I CHARACTERISTIC (LINEAR SOURCE)



BATT VOLTAGE ERROR vs. ChargingVoltage() CODE



LOAD CURRENT ERROR



Pin Description

PIN	NAME	FUNCTION
1	IOUT	Linear Current-Source Output
2	DCIN	Input Voltage for Powering Charger
3	VL	IC Power Supply. 5.4V linear-regulator output from DCIN.
4	CCV	Voltage-Regulation-Loop Compensation Point
5	CCI	Current-Regulation-Loop Compensation Point
6	SEL	Current-Range Selector. Connecting SEL to VL sets a 4A full-scale current. Leaving SEL open sets a 3A full-scale current. Connecting SEL to AGND sets a 1A full-scale current.
7	CS	Current-Sense Positive Input
8	BATT	Battery Voltage Input and Current-Sense Negative Input
9	REF	+4.096V Reference Voltage Output or External Reference Input
10	AGND	Analog Ground
11	$\overline{INT}$	Open-Drain Interrupt Output
12	THM	Thermistor Sense Voltage Input
13	SCL	Serial Clock (need external pull-up resistor)
14	SDA	Serial Data (need external pull-up resistor)
15	DACV	Voltage DAC Output Filtering Point
16	PGND	Power Ground
17	DLO	Low-Side Power MOSFET Driver Output
18	DHI	High-Side Power MOSFET Driver Output
19	LX	Power Connection for the High-Side Power MOSFET Driver
20	BST	Power Connection for the High-Side Power MOSFET Driver

Chemistry-Independent, Level 2 Smart Battery Charger

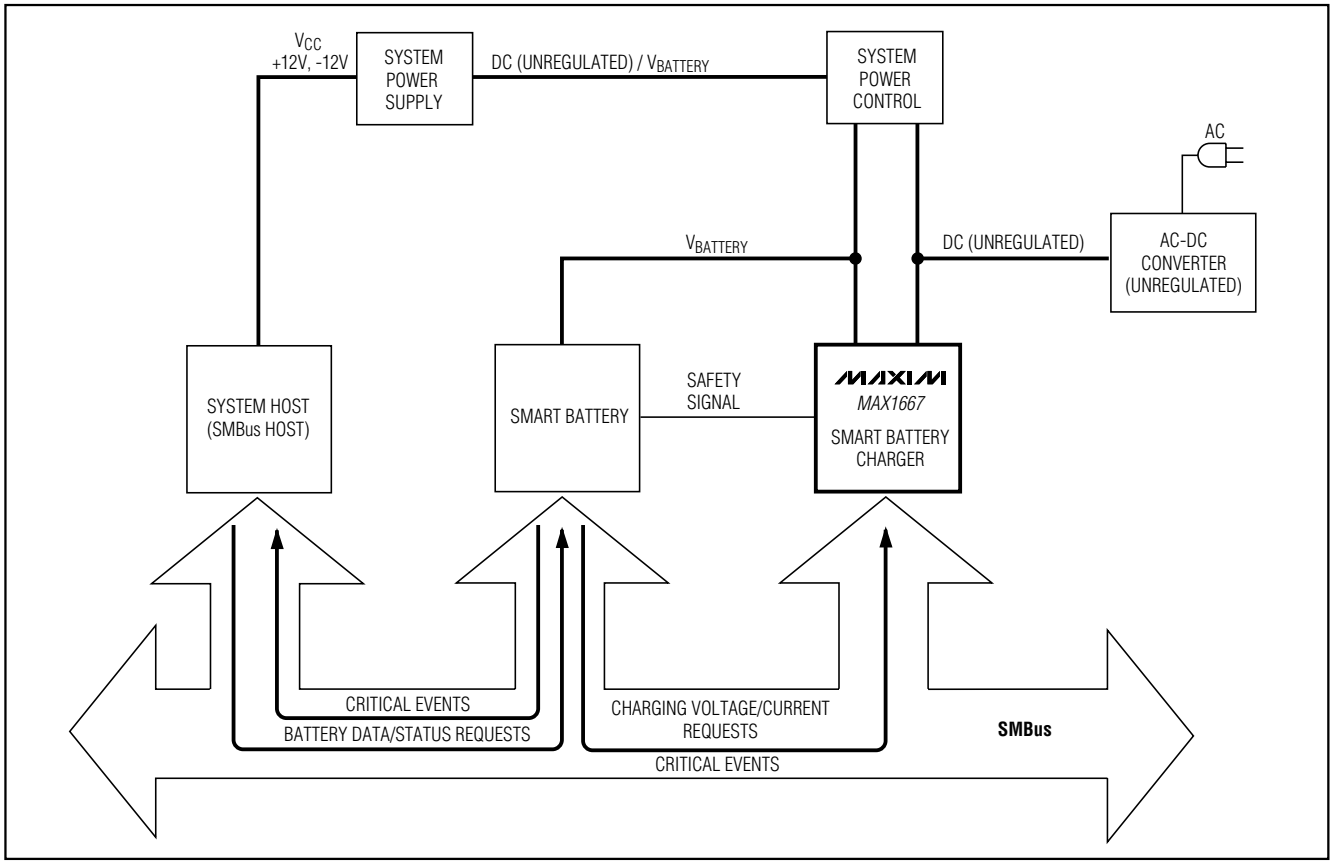


Figure 3. Typical Single Smart Battery System

Smart Battery Charging System

A smart battery charging system, at a minimum, consists of a smart battery and smart battery charger compatible with the Smart Battery System specifications using Intel's system management bus (SMBus).

Smart Battery System Block Diagrams

A system may use one or more smart batteries. The block diagram of a smart battery charging system shown in Figure 3 depicts a single battery system. This is typically found in notebook computers, video cameras, cellular phones, and other portable electronic equipment.

Another possibility is a system that uses two or more smart batteries. A block diagram for a system featuring multiple batteries is shown in Figure 4. The smart battery selector is used to connect batteries to either the smart battery charger or the system, or to disconnect them, as appropriate. For a standard smart battery, the following connections must be made: power (the battery's positive and negative terminals), SMBus (clock and data), and safety signal (resistance, typically temperature dependent). Additionally, the system host must be able to query any battery in the system so it can display the state of all batteries present in the system.

Figure 4 shows a two-battery system where Battery 2 is being charged while Battery 1 is powering the system. This configuration may be used to "condition" Battery 1, allowing it to be fully discharged prior to recharge.

Smart Battery Charger Types

Two types of smart battery chargers are defined: Level 2 and Level 3. All smart battery chargers communicate with the smart battery using the SMBus; the two types differ in their SMBus communication mode and in whether they modify the charging algorithm of the smart battery as shown in Table 1. Level 3 smart battery chargers are supersets of Level 2 chargers and as such support all Level 2 charger commands.

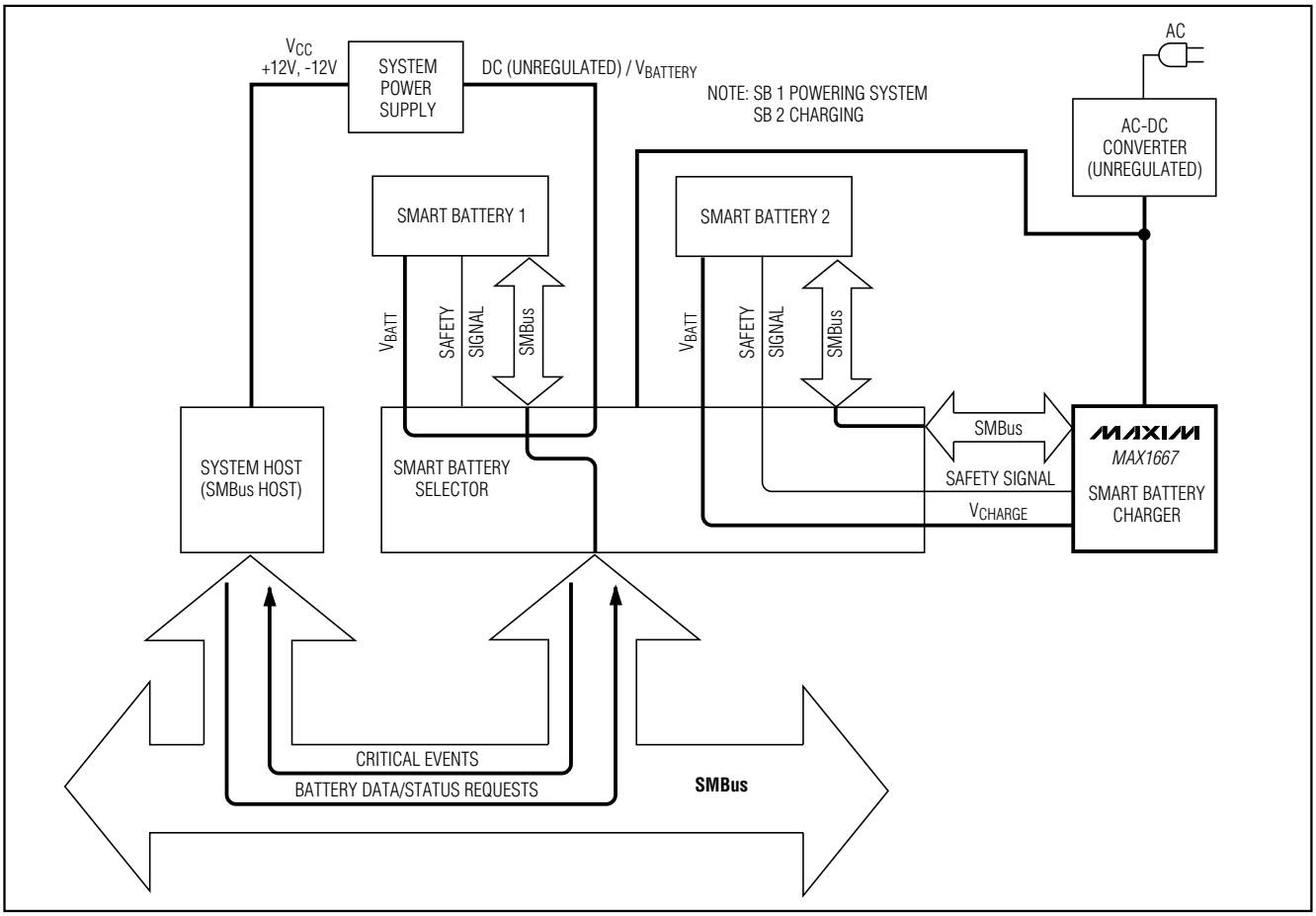


Figure 4. Typical Multiple Smart Battery System

Table 1. Charger Type by SMBus Mode and Charge Algorithm Source

SMBus MODE	CHARGE ALGORITHM SOURCE	
	Battery	Modified from Battery
Slave Only	Level 2	Level 3
Slave/Master	Level 3	Level 3

Note: *Level 1 smart battery chargers are defined in the version 0.95a specification. While they can correctly interpret smart battery end-of-charge messages minimizing overcharge, they do not provide truly chemistry-independent charging. They are no longer defined by the Smart Battery Charger specification and are explicitly not compliant with this and subsequent Smart Battery Charger specifications.*

Level 2 Smart Battery Charger

The Level 2 or "smart-battery-controlled" smart battery charger interprets the smart battery's critical warning messages, and operates as an SMBus slave device that responds to ChargingVoltage() and ChargingCurrent() messages sent to it by a smart battery. The charger is obliged to adjust its output characteristics in direct response to the messages it receives from the battery. In Level 2 charging, the smart battery is completely responsible for initiating communication and for providing the charging algorithm to the charger. The smart battery is in the best position to tell the smart battery charger how it needs to be charged. The charging algorithm in the battery may request a static charge condition or may choose to periodically adjust the smart battery charger's output to meet its present needs. A Level 2 smart battery charger is truly chemistry independent, and since it is defined as an SMBus slave device only, it is relatively inexpensive and easy to implement.

Chemistry-Independent, Level 2 Smart Battery Charger

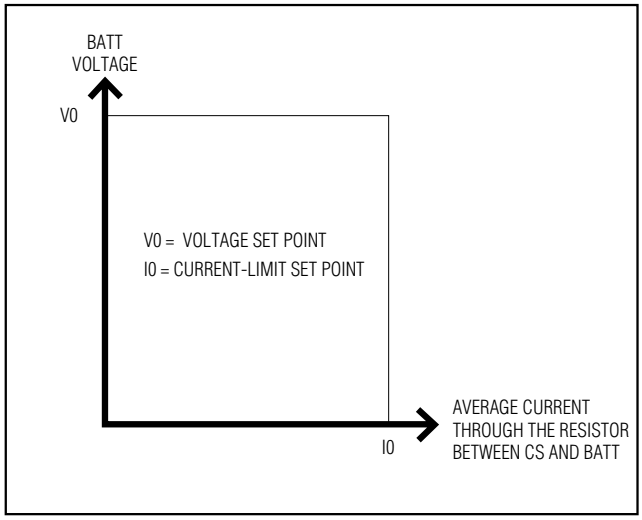


Figure 5. Output V-I Characteristic

Detailed Description

Output Characteristics

The MAX1667 contains both a voltage-regulation loop and a current-regulation loop. Both loops operate independently of each other. The voltage-regulation loop monitors BATT to ensure that its voltage never exceeds the voltage set point (V0). The current-regulation loop monitors current delivered to BATT to ensure that it never exceeds the current-limit set point (I0). The current-regulation loop is in control as long as BATT voltage is below V0. When BATT voltage reaches V0, the current loop no longer regulates, and the voltage-regulation loop takes over. Figure 5 shows the V-I characteristic at the BATT pin.

Setting V0 and I0

Set the MAX1667's voltage and current-limit set points via the Intel SMBus 2-wire serial interface. The MAX1667's logic interprets the serial-data stream from the SMBus interface to set internal digital-to-analog converters (DACs) appropriately. The power-on-reset value for V0 and I0 is 18.4V and 7mA, respectively. See *Digital Section* for more information.

Analog Section

The MAX1667 analog section consists of a current-mode pulse-width-modulated (PWM) controller and two transconductance error amplifiers—one for regulating current and the other for regulating voltage. The device uses DACs to set the current and voltage level, which are controlled via the SMBus interface. Since separate amplifiers are used for voltage and current control, both control loops can be compensated separately for optimum stability and response in each state.

Whether the MAX1667 is controlling the voltage or current at any time depends on the battery's state. If the battery has been discharged, the MAX1667's output reaches the current-regulation limit before the voltage limit, causing the system to regulate current. As the battery charges, the voltage rises until the voltage limit is reached, and the charger switches to regulating voltage. The transition from current to voltage regulation is done by the charger and need not be controlled by the host. Figure 6 shows the MAX1667 block diagram.

Voltage Control

The internal GMV amplifier controls the MAX1667's output voltage. The voltage at the amplifier's noninverting input is set by an 11-bit DAC, which is controlled by a ChargingVoltage() command on the SMBus (see *Digital Section* for more information). The battery voltage is fed to the GMV amplifier through a 5:1 resistive voltage divider. The set voltage ranges between 0 and 18.416V with 16mV resolution. This allows up to four Li+ cells in series to be charged.

The GMV amplifier's output is connected to the CCV pin, which compensates the voltage-regulation loop. Typically, a series-resistor/capacitor combination can be used to form a pole-zero doublet. The pole introduced rolls off the gain starting at low frequencies. The zero of the doublet provides sufficient AC gain at mid-frequencies. The output capacitor then rolls off the mid-frequency gain to below 1 to guarantee stability before encountering the zero introduced by the output capacitor's equivalent series resistance (ESR). The GMV amplifier's output is internally clamped to between one-fourth and three-fourths of the voltage at REF.

Current Control

An internal 7mA linear current source is used in conjunction with the PWM regulator to set the battery charge current. When the current is set to 0, the voltage regulator is on but no current is available. A current setting between 1mA and 127mA turns on the linear current source, providing a maximum of 7mA for trickle charging. For current settings above 127mA, the linear current source is disabled and the charging current is provided by the switching regulator set by the 5-bit current-control DAC.

The GMI amplifier's noninverting input is driven by a 4:1 resistive voltage divider, which is driven by the 5-bit DAC. With the internal 4.096V reference, this input is approximately 1.0V at full scale, and the resolution is 31mV. The current-sense amplifier drives the inverting input to the GMI amplifier. It measures the voltage

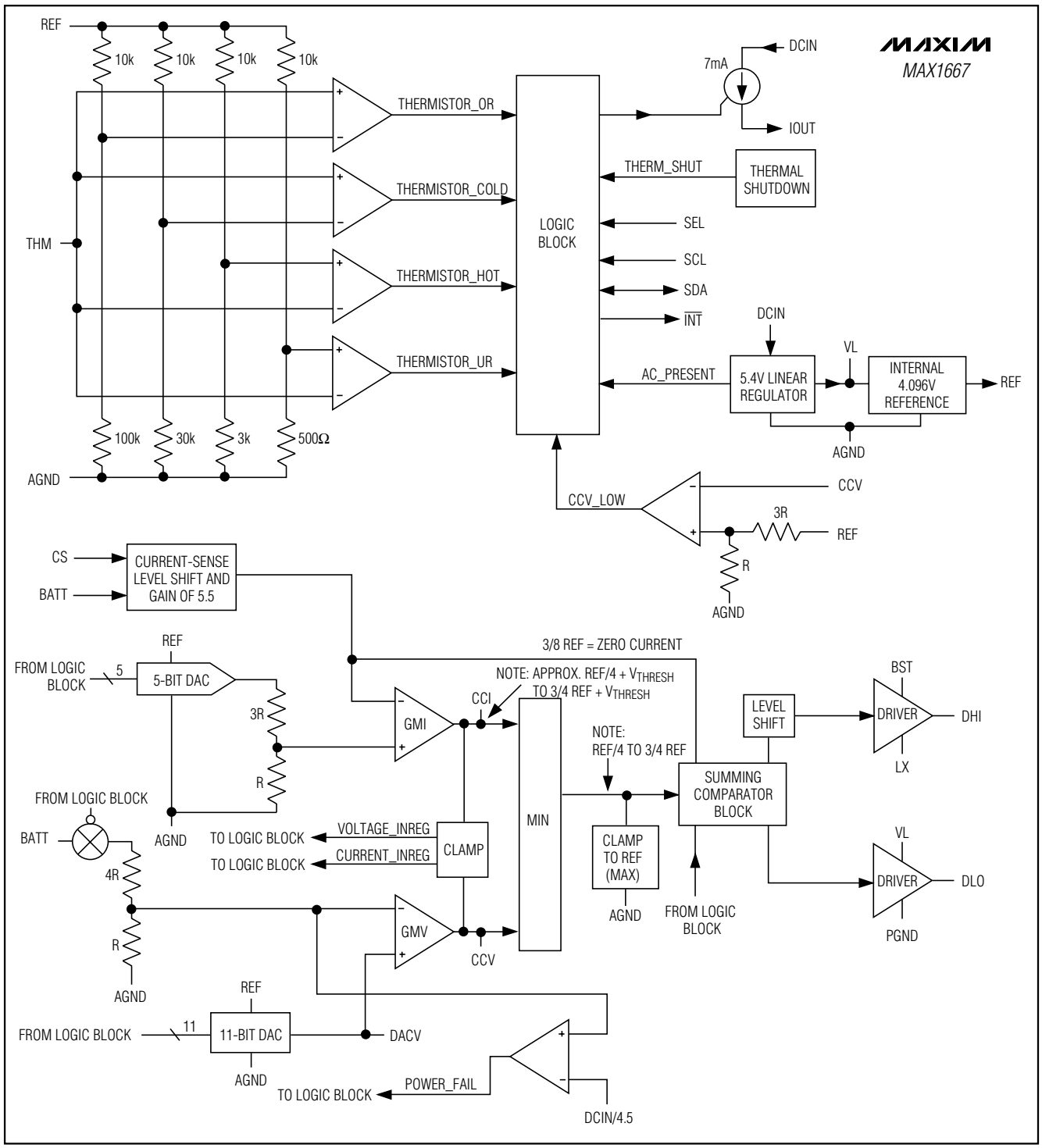


Figure 6. Functional Diagram

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across the current-sense resistor (R_{SEN}) (which is between the CS and BATT pins), amplifies it by approximately 5.45, and level shifts it to ground. The full-scale current is approximately 0.16V/R_{SEN}, and the resolution is 5mV/R_{SEN}.

The current-regulation loop is compensated by adding a capacitor to the CCI pin. This capacitor sets the current-feedback loop's dominant pole. The GMI amplifier's output is clamped to between approximately one-fourth and three-fourths of the REF voltage. While the current is in regulation, the CCV voltage is clamped to within 80mV of the CCI voltage. This prevents the battery voltage from overshooting when the DAC voltage setting is updated. The converse is true when the voltage is in regulation and the current is not at the current DAC setting. Since the linear range of CCI or CCV is about 1.5V to 3.5V (about 2V), the 80mV clamp results in a relatively negligible overshoot when the loop switches from voltage to current regulation or vice versa.

PWM Controller

The battery voltage or current is controlled by the current-mode, PWM, DC-DC converter controller. This controller drives two external N-channel MOSFETs, which switch the voltage from the input source. This switched voltage feeds an inductor, which filters the switched rectangular wave. The controller sets the pulse width of the switched voltage so that it supplies the desired voltage or current to the battery.

The heart of the PWM controller is the multi-input comparator. This comparator sums three input signals to determine the pulse width of the switched signal, setting the battery voltage or current. The three signals are the current-sense amplifier's output, the GMV or GMI error amplifier's output, and a slope-compensation signal, which ensures that the controller's internal current-control loop is stable.

The PWM comparator compares the current-sense amplifier's output to the lower output voltage of either the GMV or the GMI amplifier (the error voltage). This current-mode feedback corrects the duty ratio of the switched voltage, regulating the peak battery current and keeping it proportional to the error voltage. Since the average battery current is nearly the same as the peak current, the controller acts as a transconductance amplifier, reducing the effect of the inductor on the output filter LC formed by the output inductor and the battery's parasitic capacitance. This makes stabilizing the circuit easy, since the output filter changes from a complex second-order RLC to a first-order RC. To preserve the inner current-control loop's stability, slope compensation is also fed into the comparator. This damps out perturbations in the pulse width at duty ratios greater than 50%.

At heavy loads, the PWM controller switches at a fixed frequency and modulates the duty cycle to control the battery voltage or current. At light loads, the DC current through the inductor is not sufficient to prevent the current from going negative through the synchronous rectifier (Figure 7, M2). The controller monitors the current through the sense resistor R_{SEN}; when it drops to zero, the synchronous rectifier turns off to prevent negative current flow.

MOSFET Drivers

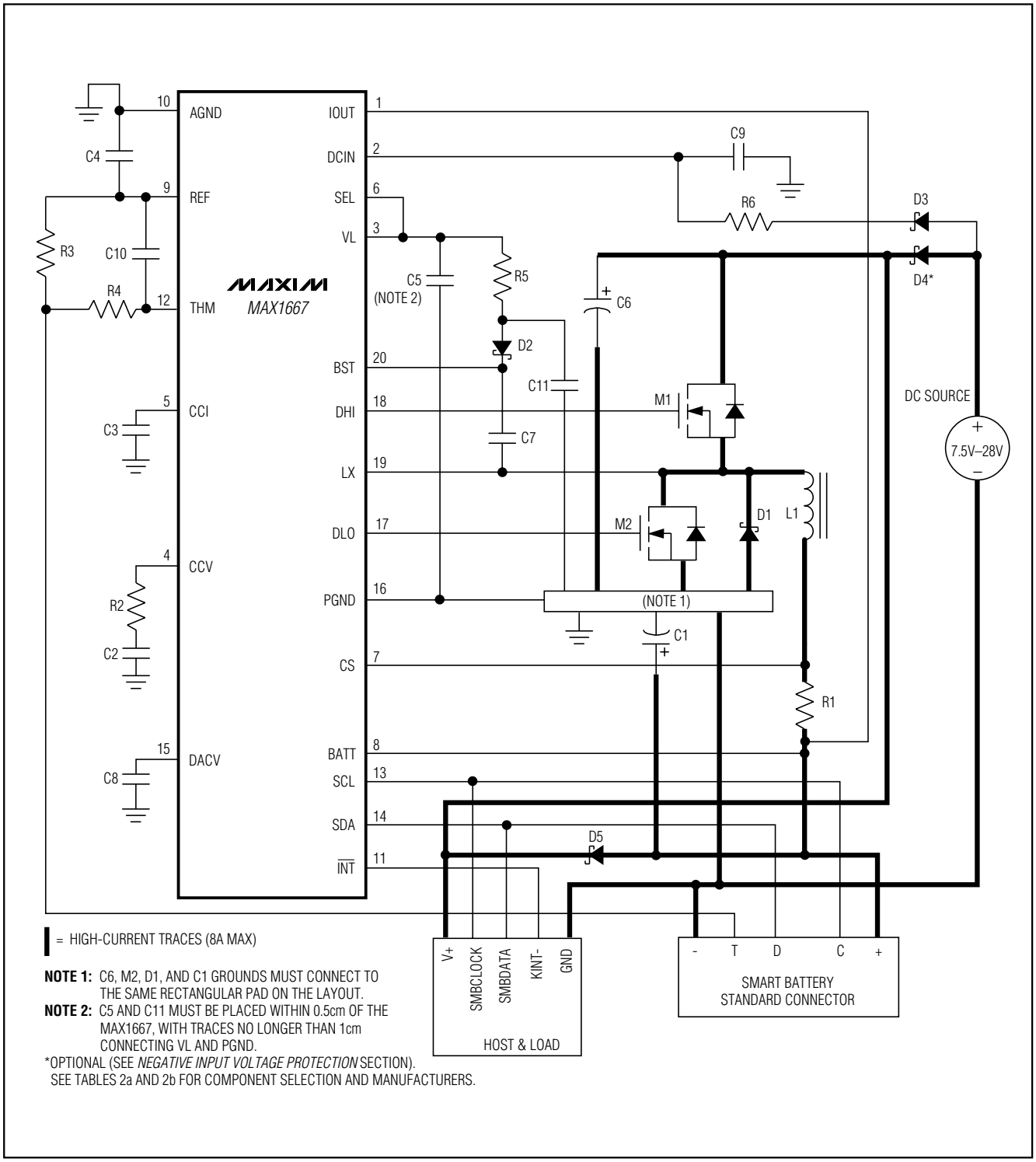
The MAX1667 drives external N-channel MOSFETs to regulate battery voltage or current. Since the high-side N-channel MOSFET's gate must be driven to a voltage higher than the input source voltage, a charge pump is used to generate such a voltage. The capacitor C7 (Figure 7) charges to approximately 5V through D2 when the synchronous rectifier turns on. Since one side of C7 is connected to the LX pin (the source of M1), the high-side driver (DHI) can drive the gate up to the voltage at BST (which is greater than the input voltage) when the high-side MOSFET turns on.

The synchronous rectifier may not be completely replaced by a diode because the BST capacitor charges while the synchronous rectifier is turned on. Without the synchronous rectifier, the BST capacitor may not fully charge, leaving the high-side MOSFET with insufficient gate drive to turn on. Use a small MOSFET, such as a 2N7002, to guarantee that the BST capacitor is allowed to charge. In this case, most of the current at high currents is carried by the Schottky diode and not by the synchronous rectifier.

Internal Regulator and Reference

The MAX1667 uses an internal low-dropout linear regulator to create a 5.4V power supply (VL), which powers its internal circuitry. VL can supply up to 20mA, less than 10mA powers the internal circuitry, and the remaining current can power the external circuitry. The current used to drive the MOSFETs comes from this supply, which must be considered when calculating how much power can be drawn. To estimate the current required to drive the MOSFETs, multiply the total gate charge of each MOSFET by the switching frequency (typically 250kHz). To ensure VL stability, bypass the VL pin with a 1µF or greater capacitor.

The MAX1667 has an internal, accurate 4.096V reference voltage. This guarantees a voltage-setting accuracy of ±1% max. Bypass the reference with a 1µF or greater capacitor.



NOTE 1: C6, M2, D1, AND C1 GROUNDS MUST CONNECT TO THE SAME RECTANGULAR PAD ON THE LAYOUT.

NOTE 2: C5 AND C11 MUST BE PLACED WITHIN 0.5cm OF THE MAX1667, WITH TRACES NO LONGER THAN 1cm CONNECTING VL AND PGND.

*OPTIONAL (SEE *NEGATIVE INPUT VOLTAGE PROTECTION* SECTION).

SEE TABLES 2a AND 2b FOR COMPONENT SELECTION AND MANUFACTURERS.

Figure 7. Typical Application Circuit

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Table 2a. Component Selection

DESIGNATION	MANUFACTURER	1A	3A	4A
C1 Output Capacitor		68µF, 20V, low ESR		
	AVX	TPSE686M020R0150		
	Sprague	594D686X0025R2T		
C2, C7, C11		0.1µF		
C3		47nF		
C4, C5, C9, C10		1µF		
C6 Input Capacitor		2 x 22µF, 35V, low ESR		
	AVX	TPSE226M035R0200		
	Sprague	594D226X0035R2T		
C8		22nF		
D1, D4, D5 Schottky Diodes		1N5819 equivalent	1N5821 equivalent	1N5821 equivalent
	Motorola	MBRS130LT3	MBRS340T3	MBRS340T3
	Central		CMSH3-40	CMSH5-40
	NIEC	EC31	NSQ03A04	CMSH5-40
D2, D3	Central	Schottky diode, 50mA I_{DC}, 30V, CMPSH-3		
L1 Inductor		33µH, 1A ISAT	33µH, 3A ISAT, 30V	33µH, 4A ISAT, 30V
	Sumida	CDH74-330	CDRH127-330	CDRH127-270
	Coiltronics	UP1B-330	UP3B-330	
	Coilcraft	DS3316P-333		
M1 High-Side MOSFET	IR	IRF7603	IRF7201	IRF7805
	Fairchild	FDN359A	FDS4410	FDS6680
	Motorola	MTSF3N03HD	MMDF3N03HD	
M2 Low-Side MOSFET		2N7002 equivalent		
	Motorola	MMBF1170LT1		
R1 Sense Resistor		40mΩ ±1%, 1W		
	IRC	LR251201R040F		
	Dale	WSL-2512/0.04W/±1%		
R2, R4		10kΩ ±5%, 1/16W		
R3		10kΩ ±1%, 1/16W		
R5, R6		33Ω ±5%, 1/16W		

Digital Section

SMBus Interface

The MAX1667 uses serial data to control its operation. The serial interface complies with the SMBus specification (see *System Management Bus Specification*, from the SBS forum at www.sbs-Forum.org or from Intel Architecture Labs: 800-253-3696). Charger functionality complies with the Duracell/Intel Smart Charger Specification for a Level 2 charger.

The MAX1667 uses the SMBus Read-Word and Write-Word protocols to communicate with the battery it is charging, as well as with any host system that monitors the battery to charger communications. The MAX1667 acts only as a slave device and never initiates communication on the bus; it receives commands and responds to queries for status information. Figures 8a and 8b show the SMBus Write-Word and Read-Word protocols.

Each communication with the MAX1667 begins with the master issuing a START condition, which is a high-to-low transition on SDA while SCL is high (Figure 1).

Table 2b. Component Suppliers

MANUFACTURER	PHONE	FAX
AVX	803-946-0690	803-626-3123
Central Semiconductor	516-435-1110	516-435-1824
Coilcraft	847-639-6400	847-639-1469
Coiltronics	561-241-7876	561-241-9339
Dale	605-668-4131	605-665-1627
IR	310-322-3331	310-322-3332
IRC	512-992-7900	512-992-3377
NIEC	805-867-2555	805-867-2698
Siliconix	408-988-8000	408-970-3950
Sprague	603-224-1961	603-224-1430
Sumida	847-956-0666	847-956-0702
Zetex	516-543-7100	516-864-7630

When the master has finished communicating with the slave, the master issues a STOP condition, which is a low-to-high transition on SDA while SCL is high. The bus is then free for another transmission. Figures 1 and 2 show timing diagrams for signals on the SMBus interface. The address byte, control byte, and data bytes are transmitted between the START and STOP conditions. Data is transmitted in 8-bit words, and after each byte either the slave or the master issues an acknowledgment (Figure 2); therefore, nine clock cycles are required to transfer each byte. The SDA state is allowed to change only while SCL is low, except for the START and STOP conditions.

The MAX1667 7-bit address is preset to 0b0001001. The eighth bit indicates a Write-Word ($\overline{W}$ = 0) or a Read-Word (R = 1) command. This can also be denoted by the hexadecimal number 0x12 for a Write-Word command or a 0x13 for a Read-Word command.

The following commands use the Write-Word protocol (Figure 8a): ChargerMode(), ChargingVoltage(), ChargingCurrent(), and AlarmWarning(). The ChargerStatus command uses the Read-Word protocol (Figure 8b).

ChargerMode()

The ChargerMode() command uses Write-Word protocol (Figure 8a). The command code for ChargerMode() is 0x12 (0b00010010). Table 3 describes the functions of the 16 data bits (D0–D15). Bit 0 refers to the D0 bit in the Write-Word protocol.

Whenever the BATTERY_PRESENT status bit (bit 14) of ChargerStatus() is clear, the HOT_STOP bit is set, regardless of any previous ChargerMode() command. To charge a battery that has a thermistor impedance in the HOT range (i.e., THERMISTOR_HOT = 1 and THERMISTOR_UR = 0), the host must use the ChargerMode() command to clear HOT_STOP **after** the battery is inserted. The HOT_STOP bit returns to its default power-up condition ('1') whenever the battery is removed.

ChargingVoltage()

The ChargingVoltage() command uses Write-Word protocol (Figure 8a). The command code for ChargingVoltage() is 0x15 (0b00010101). The 16-bit binary number formed by D15–D0 represents the voltage set point (V0) in millivolts; however, since the MAX1667 has only 16mV of resolution in setting V0, the D0, D1, D2, and D3 bits are ignored.

The maximum voltage delivered by the MAX1667 is 18.416V, corresponding to a ChargingVoltage() value of 0x47F0. This is also the floating voltage set by the power-on reset (POR). ChargingVoltage() values above 0x47F0 deliver the floating voltage and set the VOLTAGE_OR status bit. Any time the BATTERY_PRESENT status bit is clear, the ChargingVoltage() register returns to its POR state.

Figure 9 shows the mapping between V0 (the voltage-regulation-loop set point) and the ChargingVoltage() data.

ChargingCurrent()

The ChargingCurrent() command uses Write-Word protocol (Figure 8a). The command code for ChargingCurrent() is 0x14 (0b00010100). The 16-bit binary number formed by D15–D0 represents the current-limit set point (I0) in milliamps (Table 4). Connecting SEL to AGND selects a 0.896A maximum setting for I0. Leaving SEL open selects a 2.944A maximum setting for I0. Connecting SEL to VL selects a 3.968A maximum setting for I0.

Two sources of current in the MAX1667 charge the battery: a linear current source begins from IOUT, and a switching regulator controls the current flowing through the current-sense resistor (R1). IOUT provides a trickle-charge current to compensate for battery self-discharge, while the switching regulator provides large currents for fast charging.

IOUT sources 7mA, while the switching regulator sources from 128mA to 3968mA with a 5-bit resolution (LSB = 5.12mV / RSENSE = 128mA with a 40mΩ sense resistor). In Table 4, DA4–DA0 denotes the bits in the current DAC code. Table 5 shows the relationship between the value programmed with the ChargingCurrent() command and IOUT source current. The CCV_LOW comparator checks to see if the output volt-

Table 3. ChargerMode() Bit Functions

BIT NAME	BIT POSITION*	POR VALUE**	FUNCTION
INHIBIT_CHARGE	0 (LSB)	0	0 = Allow normal operation; clear the CHG_INHIBITED status bit. 1 = Turn the charger off; set the CHG_INHIBITED status bit.
ENABLE_POLLING	1	—	Not implemented. Write 0 into this bit.
POR_RESET	2	—	0 = No change in any non-ChargerMode() settings. 1 = Change the voltage and current settings to 0xFFFF and 0x0007 respectively; clear the THERMISTOR_HOT and ALARM_INHIBITED bits.
RESET_TO_ZERO	3	—	Not implemented. Write 0 into this bit.
N/A	4	—	Not implemented. Write 1 into this bit.
BATTERY_PRESENT_MASK	5	0	0 = Interrupt on either edge of the BATTERY_PRESENT status bit. 1 = Do not interrupt because of a BATTERY_PRESENT bit change.
POWER_FAIL_MASK	6	1	0 = Interrupt on either edge of the POWER_FAIL status bit. 1 = Do not interrupt because of a POWER_FAIL bit change.
N/A	7–9	—	Not implemented. Write 1 into this bit.
HOT_STOP	10	1	0 = The THERMISTOR_HOT status bit does not turn the charger off. 1 = THERMISTOR_HOT turns the charger off.
N/A	11–15 (MSB)	—	Not implemented. Write 1 into this bit.

**Bit position in the D15–D0 data. **Power-on reset value.*
N/A = Not applicable

age is too high by comparing CCV to REF/4. If CCV_LOW = 1 (when CCV < REF/4), IOUT shuts off. This prevents the output voltage from exceeding the voltage set point specified by the ChargingVoltage() register. VOLTAGE_NOTREG = 1 whenever the internal clamp pulls down on CCV. (The internal clamp pulls down on CCV to keep its voltage close to CCI's voltage.)

With the switching regulator on, the current through R1 (Figure 7) is regulated by sensing the average voltage between CS and BATT. Figure 10 shows the relationship between the ChargingCurrent() data and the average voltage between CS and BATT.

When the switching regulator is off, DHI is forced to LX and DLO is forced to ground. This prevents current from flowing through inductor L1. Table 6 shows the relationship between the ChargingCurrent() register value and the switching regulator current DAC code (DA4–DA0).

To ensure that the actual output current matches the data value programmed with the ChargingCurrent() command, R1 should be as close as possible to 40mΩ. The SEL pin setting affects the full-scale current but not the step size. ChargingCurrent() values above the full-scale setting set the CURRENT_OR status bit. Note that whenever any current DAC bits are set, the linear-current source is turned off.

The power-on reset value for the ChargingCurrent() register is 0x0007. Any time the BATTERY_PRESENT status bit is clear (battery removed), the ChargingCurrent() register returns to its power-on reset state. This ensures that upon insertion of a battery, the initial charging current is 7mA.

AlarmWarning()

The AlarmWarning() command uses Write-Word protocol (Figure 8a). The command code for AlarmWarning() is 0x16 (0b00010110). The AlarmWarning() command sets the ALARM_INHIBITED status bit. The MAX1667 responds to the following alarms: OVER_CHARGED_ALARM (D15), TERMINATE_CHARGE_ALARM (D14), and OVER_TEMP_ALARM (D12). Table 7 summarizes the AlarmWarning() command's function. The ALARM_INHIBITED status bit remains set until BATTERY_PRESENT = 0 (battery removed), a ChargerMode() command is written with the POR_RESET bit set, or a new ChargingVoltage() or ChargingCurrent() is written.

a) Write-Word Format

S	SLAVE ADDRESS	$\overline{W}$	ACK	COMMAND BYTE	ACK	S	LOW DATA BYTE	ACK	HIGH DATA BYTE	ACK	P
	7 bits	1b	1b	8 bits	1b		7 bits	1b	8 bits	1b	
	MSB LSB	0		MSB LSB			MSB LSB		MSB LSB		

Preset to 0b0001001

ChargerMode() = 0x12
ChargingCurrent() = 0x14
ChargerVoltage() = 0x15
AlarmWarning() = 0x16

D7 D0 D15 D8

b) Read-Word Format

S	SLAVE ADDRESS	$\overline{W}$	ACK	COMMAND BYTE	ACK	S	SLAVE ADDRESS	R	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	NACK	P
	7 bits	1b	1b	8 bits	1b		7 bits	1b	1b	8 bits	1b	8 bits	1b	
	MSB LSB	0		MSB LSB			MSB LSB	1		MSB LSB		MSB LSB		

Preset to 0b0001001

ChargerStatus() = 0x13

Preset to 0b0001001

D7 D0 D15 D8

Legend:
S = Start Condition or Repeated Start Condition
ACK = Acknowledge (logic low)
$\overline{W}$ = Write Bit (logic low)
P = Stop Condition
NACK = NOT Acknowledge (logic high)
R = Read Bit (logic high)

MASTER TO SLAVE
SLAVE TO MASTER

Figure 8. SMBus a) Write-Word and b) Read-Word Protocols

ChargerStatus()

The ChargerStatus() command uses Read-Word protocol (Figure 8b). The command code for ChargerStatus() is 0x13 (0b00010011). The ChargerStatus() command returns information about thermistor impedance and the MAX1667's internal state. The Read-Word protocol returns D15–D0. Table 8 describes the meaning of the individual bits. The latched bits, THERMISTOR_HOT and ALARM_INHIBITED, are cleared whenever BATTERY_PRESENT = 0 or ChargerMode() is written with POR_RESET = 1.

Interrupts and the Alert-Response Address

An interrupt is triggered ($\overline{INT}$ goes low) whenever power is applied to DCIN, the BATTERY_PRESENT bit changes, or the POWER_FAIL bit changes. BATTERY_PRESENT and POWER_FAIL have interrupt masks that can be set or cleared via the ChargerMode() command. $\overline{INT}$ stays low until the interrupt is cleared. There are two methods for clearing the interrupt: issuing a ChargerStatus() command, and using a modified Receive Byte protocol with a 0x19 (0b0011001) Alert-Response address. The MAX1667 responds to the Alert-Response address with its address (0x13) left justified as the most significant bits of the returned byte.

Applications Information

Negative Input Voltage Protection

In most portable equipment, the DC power to charge batteries enters through a two-conductor cylindrical power jack. It is easy for the end user to add an adapter to switch the DC power's polarity. Polarized capacitor C6 would be destroyed if a negative voltage were applied. Diode D4 in Figure 7 prevents this from happening.

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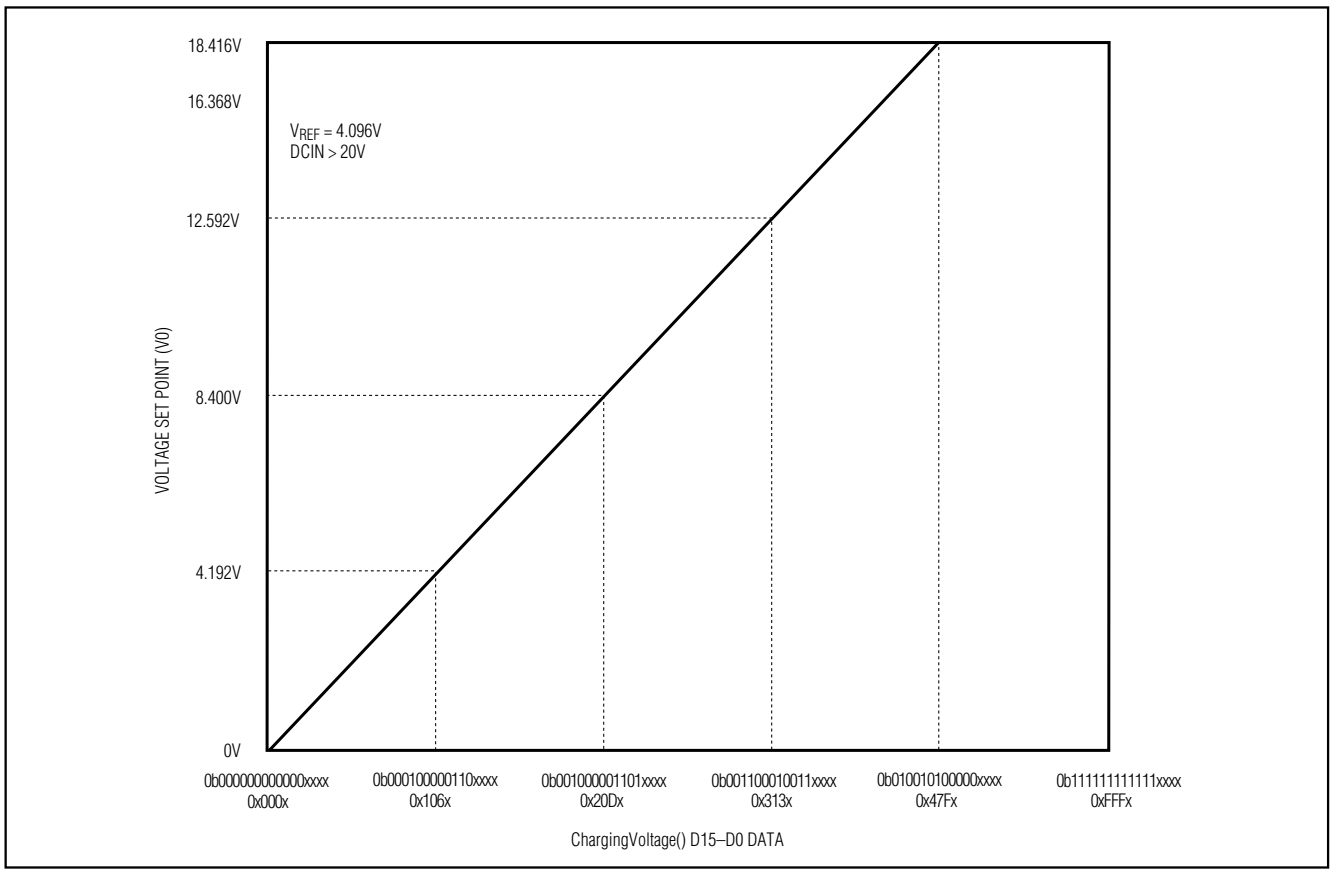


Figure 9. ChargingVoltage() Data to Voltage Mapping

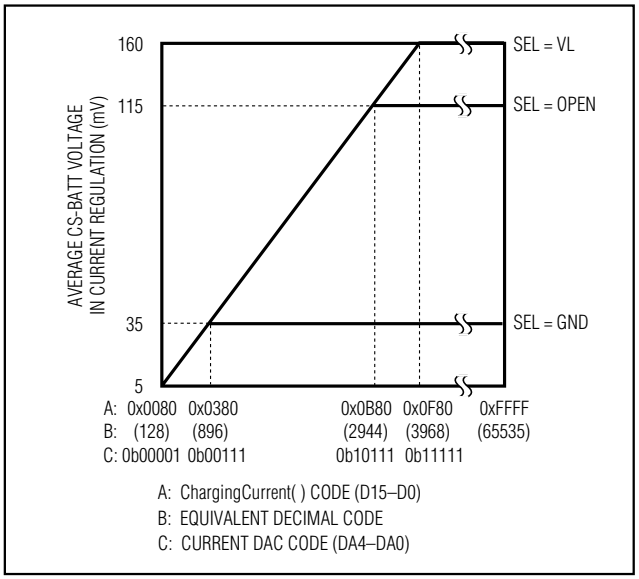


Figure 10. Average Voltage Between CS and BATT vs. Code

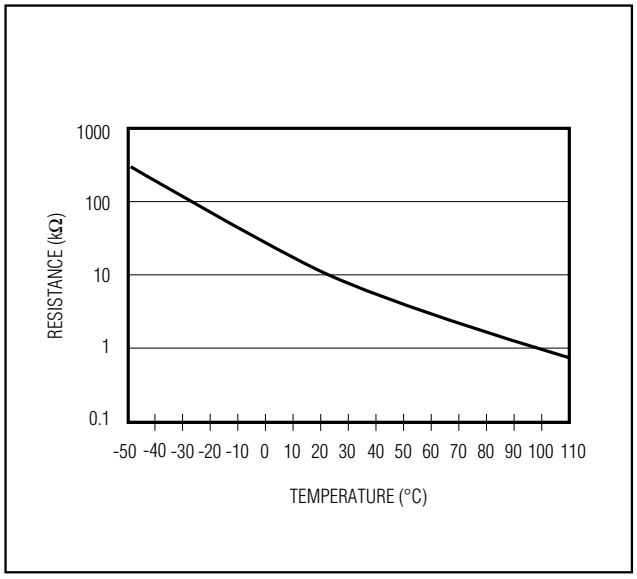


Figure 11. Typical Thermistor Characteristics

Table 4. ChargingCurrent() Bit Functions

BIT POSITION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FUNCTION	FS*				DA4	DA3	DA2	DA1	DA0	IOUT**						
WEIGHT IN mA (R_{SENSE} = 40mΩ)	3968*				2048	1024	512	256	128	7**						

* *When SEL = VL, values above 0x0F80 set the output current to 3.968A.*
When SEL = OPEN, values above 0x0B80 set the output current to 2.944A.
When SEL = GND, values above 0x0380 set the output current to 0.896A.

** *Values below 0x0080 set the output current to 7mA.*

Table 5. Relationship Between IOUT Source Current and ChargingCurrent() Value

CHARGE_ INHIBITED	(Note 1)	ALARM_ INHIBITED	ChargingVoltage()	ChargingCurrent()	CCV_LOW	VOLTAGE_ NOTREG	I_{OUT} OUTPUT CURRENT (mA)
0	0	0	0x0000–0x000F	x	x	x	0
0	0	0	x	0x0000	x	x	0
0	0	0	0x0010–0xFFFF	0x0001–0x0007	0	x	7
0	0	0	0x0010–0xFFFF	0x0001–0x0007	1	0	0
0	0	0	0x0010–0xFFFF	0x0001–0x0007	1	1	7
0	0	0	0x0010–0xFFFF	0x0008–0x007F	0	x	7
0	0	0	0x0010–0xFFFF	0x0008–0x007F	1	0	0
0	0	0	0x0010–0xFFFF	0x0008–0x007F	1	1	7
0	0	0	x0x0010–0xFFFF	0x0080–0xFFFF	x	x	0
0	0	1	x	x	x	x	0
0	1	x	x	x	x	x	0
1	x	x	x	x	x	x	0

Note 1: THERMISTOR_HOT and HOT_STOP and NOT (THERMISTOR_UR).

If reverse-polarity protection for the DC input power is not necessary, diode D4 can be omitted. This eliminates the power lost due to the voltage drop on diode D4.

Thermistor Characterization

Figure 11 represents the expected electrical behavior of a 103ETB-type thermistor (nominally 10kΩ at +25°C ±5% or better) to be used with the MAX1667. The graph is typical of the suggested thermistor's characteristics.

THERMISTOR_OR bit is set only when the thermistor value is > 100kΩ. This indicates that the thermistor is open.

THERMISTOR_COLD bit is set only when the thermistor value is > 30kΩ. The thermistor indicates a cold battery.

THERMISTOR_HOT bit is set only when the thermistor value is < 3kΩ.

THERMISTOR_UR bit is set only when the thermistor value is < 500Ω.

Multiple bits may be set depending on the values of the thermistor (e.g., a 450Ω thermistor will cause both the THERMISTOR_HOT *and* the THERMISTOR_UR bits to be set). The thermistor may be replaced by fixed-value resistors in battery packs that do not require the thermistor as a secondary fail-safe indicator. In this case, it is the responsibility of the battery pack to manipulate the resistance to obtain correct charger behavior.

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Table 6. Relationship Between Current DAC Code and the ChargingCurrent() Value

CHARGE_INHIBITED	(Note 1)	ALARM_INHIBITED	ChargingVoltage()	ChargingCurrent()	SEL = GND CURRENT DAC CODE	SEL = GND SW REG ON?	SEL = GND CURRENT_OR	SEL = OPEN CURRENT DAC CODE	SEL = OPEN SW REG ON?	SEL = OPEN CURRENT_OR	SEL = VL CURRENT DAC CODE	SEL = VL SW REG ON?	SEL = VL CURRENT_OR
0	0	0	0x0000–0x000F	x	N/A	No	0	N/A	No	0	N/A	No	0
0	0	0	0x000F–0xFFFF	0x0000–0x007F	0	No	0	0	No	0	0	No	0
0	0	0	0x000F–0xFFFF	0x0080–0x00FF	1	Yes	0	1	Yes	0	1	Yes	0
0	0	0	0x000F–0xFFFF	0x0100–0x037F	2–6	Yes	0	2–6	Yes	0	2–6	Yes	0
0	0	0	0x000F–0xFFFF	0x0380–0x03FF	7	Yes	0	7	Yes	0	7	Yes	0
0	0	0	0x000F–0xFFFF	0x0400–0x047F	7	Yes	1	8	Yes	0	8	Yes	0
0	0	0	0x000F–0xFFFF	0x0480–0x0B7F	7	Yes	1	9–22	Yes	0	9–22	Yes	0
0	0	0	0x000F–0xFFFF	0x0B80–0x0BFF	7	Yes	1	23	Yes	0	23	Yes	0
0	0	0	0x000F–0xFFFF	0x0C00–0x0C7F	7	Yes	1	23	Yes	1	24	Yes	0
0	0	0	0x000F–0xFFFF	0x0C80	7	Yes	1	23	Yes	1	25–30	Yes	0
0	0	0	0x000F–0xFFFF	0x0F80–0x0FFF	7	Yes	1	23	Yes	1	31	Yes	0
0	0	0	0x000F–0xFFFF	0x1000–0xFFFF	7	Yes	1	23	Yes	1	31	Yes	1
0	0	1	x	x	N/A	No	N/A	N/A	No	N/A	N/A	No	N/A
0	1	x	x	x	N/A	No	N/A	N/A	No	N/A	N/A	No	N/A
1	x	x	x	x	N/A	No	N/A	N/A	No	N/A	N/A	No	N/A

Note 1: THERMISTOR_HOT and HOT_STOP and NOT (THERMISTOR_UR).

Table 7. Effect of the AlarmWarning() Command

AlarmWarning() DATA BITS																RESULT
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Set ALARM_INHIBITED
x	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Set ALARM_INHIBITED
x	x	x	1	x	x	x	x	x	x	x	x	x	x	x	x	Set ALARM_INHIBITED

Table 8. ChargerStatus() Bit Descriptions

NAME	BIT POSITION	LATCHED?	DESCRIPTION
CHARGE_INHIBITED	0	Yes	0 = Ready to charge a smart battery 1 = Charger is off; IOUT current = 0mA; DLO = PGND; DHI = LX
MASTER_MODE	1	N/A	Always returns '0'
VOLTAGE_NOTREG	2	No	0 = BATT voltage is limited at the voltage set point (BATT = V0). 1 = BATT voltage is less than the voltage set point (BATT < V0).
CURRENT_NOTREG	3	No	0 = Current through R1 is at its limit (I_{BATT} = I0). 1 = Current through R1 is less than its limit (I_{BATT} < I0).
LEVEL_2	4	N/A	Always returns 1
LEVEL_3	5	N/A	Always returns 0
CURRENT_OR	6	No	0 = ChargingCurrent() value is valid for MAX1667. 1 = ChargingCurrent() value exceeds what MAX1667 can actually deliver.
VOLTAGE_OR	7	No	0 = ChargingVoltage() value is valid for MAX1667. 1 = ChargingVoltage() value exceeds what MAX1667 can actually deliver.
THERMISTOR_OR	8	No	0 = THM voltage < 91% of REF voltage 1 = THM voltage > 91% of REF voltage
THERMISTOR_COLD	9	No	0 = THM voltage < 75% of REF voltage 1 = THM voltage > 75% of REF voltage
THERMISTOR_HOT	10	Yes	This bit reports the state of an internal SR flip-flop (denoted THERMISTOR_HOT flip-flop). The THERMISTOR_HOT flip-flop is set whenever THM is below 23% of REF. It is cleared whenever BATTERY_PRESENT = 0 or ChargerMode() is written with POR_RESET = 1.
THERMISTOR_UR	11	No	0 = THM voltage > 5% of REF voltage 1 = THM voltage < 5% of REF voltage
ALARM_INHIBITED	12	Yes	This bit reports the state of an internal SR flip-flop (denoted ALARM_INHIBITED flip-flop). The ALARM_INHIBITED flip-flop is set whenever the AlarmWarning() command is written with D15, D14, or D12 set. The ALARM_INHIBITED flip-flop is cleared whenever BATTERY_PRESENT = 0, or ChargerMode() is written with POR_RESET = 1, or ChargingVoltage() or ChargingCurrent() is written.
POWER_FAIL	13	No	0 = BATT voltage < 89% of DCIN voltage 1 = BATT voltage > 89% of DCIN voltage
BATTERY_PRESENT	14	No	0 = No battery is present (THERMISTOR_OR = 1). 1 = A battery is present (THERMISTOR_OR = 0).
AC_PRESENT	15	No	0 = VL voltage < 4V 1 = VL voltage > 4V

**Bit position in the D15–D0 data*

N/A = Not applicable

Chemistry-Independent, Level 2 Smart Battery Charger

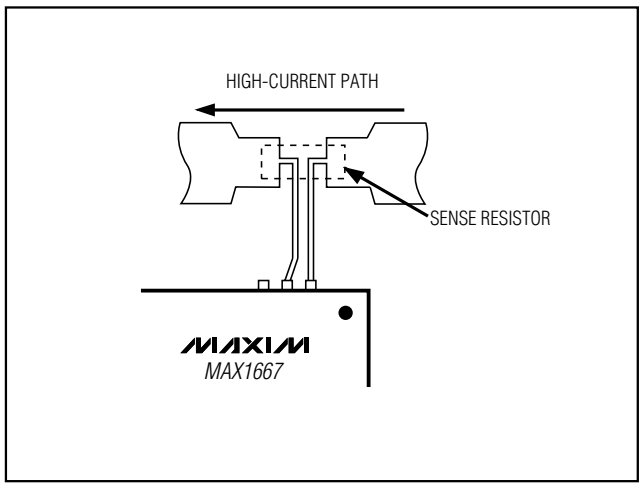


Figure 12. Kelvin Connections for the Current-Sense Resistors

PC Board Layout Considerations

Good PC board layout is required to achieve specified noise, efficiency, and stable performance. The PC board layout artist must be given explicit instructions, preferably a pencil sketch showing the placement of power-switching components and high-current routing. Refer to the PC board layout in the MAX1667 evaluation kit manual for examples. A ground plane is essential for optimum performance. In most applications, the circuit will be located on a multilayer board, and full use of the four or more copper layers is recommended. Use the top layer for high-current connections, the bottom layer for quiet connections (REF, CCV, CCI, DACV, GND), and the inner layers for an uninterrupted ground plane. Use the following step-by-step guide:

1) Place the high-power components (C1, C6, M1, M2, D1, L1, and R1) first, with their grounds adjacent:
   - *Minimize current-sense resistor trace lengths* and ensure accurate current sensing with Kelvin connections (Figure 12).
   - *Minimize ground trace lengths* in the high-current paths.
   - *Minimize other trace lengths* in the high-current paths:
     — Use > 5mm-wide traces.
     — Connect CIN to high-side MOSFET drain: 10mm max length.
     — Connect rectifier diode cathode to low side.
     — MOSFET: 5mm max length.
     — LX node (MOSFETs, rectifier cathode, inductor): 15mm max length.

Ideally, surface-mount power components are butted up to one another with their ground terminals almost touching. These high-current grounds are then connected to each other with a wide, filled zone of top-layer copper so they do not go through vias. The resulting top-layer subground plane is connected to the normal inner-layer ground plane at the output ground terminals, which ensures that the IC's analog ground is sensing at the supply's output terminals without interference from IR drops and ground noise. Other high-current paths should also be minimized, but focusing primarily on short ground and current-sense connections eliminates about 90% of all PC board layout problems.

2) Place the IC and signal components. Keep the main switching nodes (LX nodes) away from sensitive analog components (current-sense traces and REF capacitor). Place the IC and analog components on the opposite side of the board from the power-switching node. **Important**: The IC must be no further than 10mm from the current-sense resistors. Keep the gate-drive traces (DH, DL, and BST) shorter than 20mm and route them away from CSH, CSL, and REF. Place ceramic bypass capacitors close to the IC. The bulk capacitors can be placed further away.
3) Use a single-point star ground where the input ground trace, power ground (subground plane), and normal ground plane meet at the supply's output ground terminal. Connect both IC ground pins and all IC bypass capacitors to the normal ground plane.

Upgrading from MAX1647 to MAX1667

The MAX1667 is a pin- and software-compatible upgrade to the MAX1647, with the following functional differences:

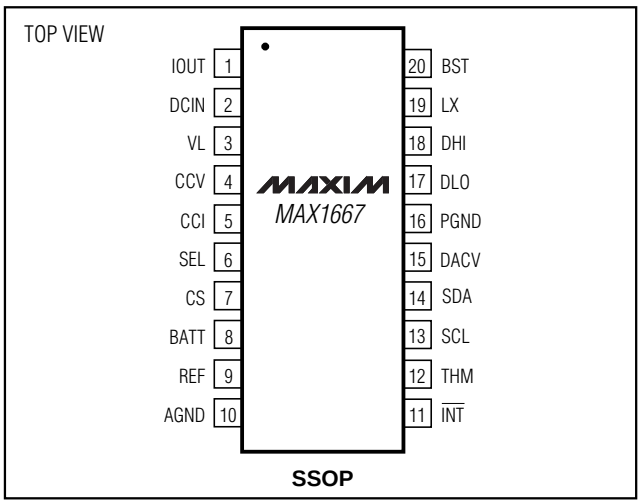
1) The PWM duty cycle has been extended to 97%.
2) The internal reference has been changed to +4.096V with 1% accuracy over line, load, and temperature.
3) The internal voltage DAC has been changed to allow a program voltage of 18,416mV. Up to four Li+ cells can be charged.
4) The linear current source (IOUT) has been reduced to 7mA and turns off when the switching regulator is on.
5) An internal diode has been added to the IOUT pin to prevent reverse current from BATT when the DC source is removed.
6) The internal current DAC was changed from 6-bit to 5-bit resolution.

7) The SEL pin digitally limits the output current to 4A, 3A, or 1A without a change in sense resistor value between the three modes.
8) The single count current-sense voltage has been changed to 5mV. R1 required is now 40mΩ.
9) After the AlarmWarning() message, the charger is not locked off. Subsequent ChargingVoltage() or ChargingCurrent() commands allow the MAX1667 to resume the charge.
10) The Alert-Response address is 0x13 (0b00010011).

When upgrading a MAX1647 design, follow these recommended or required changes (part numbers refer to Figure 3 of the MAX1647 data sheet):

1) Change R1 to 40mΩ (required).
2) Remove diodes D5 and D6, transistor Q1, and resistor R6. Connect IOUT directly to BATT (recommended).
3) Remove the external +4.096V reference (recommended).
4) Remove D6 (recommended). When doing this, also place a small-signal diode in series with R7 and connect it directly to the DC source (see D3 and R5 on Figure 3 of the MAX1647 data sheet).

Pin Configuration



Chip Information

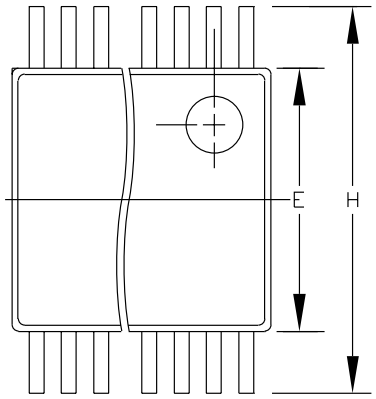
TRANSISTOR COUNT: 6378

SUBSTRATE CONNECTED TO AGND

Chemistry-Independent, Level 2 Smart Battery Charger

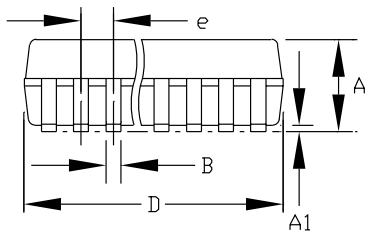
Package Information

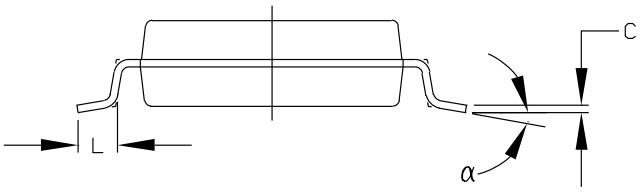
SSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, SSOP, 5.3X.65mm

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0056	A	1/1

NOTES

NOTES

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