Click here for production status of specific part numbers.

MAX16152/MAX16153/ MAX16154/MAX16155

nanoPower Supervisor and Watchdog Timer

General Description

The MAX16152/MAX16153/MAX16154/MAX16155 ultra-low-current supervisory circuits monitor a single system supply voltage and the integrity of code execution by a microprocessor or microcontroller. These supervisors assert the reset output whenever the V_{CC} supply voltage is greater than the minimum operating voltage, but less than the reset threshold. After the supply voltage rises above the reset threshold, the reset output remains asserted for the reset timeout period, and then de-asserts. Reset voltage thresholds are available from 1.50V to 5.0V in approximately 100mV increments.

A watchdog timer circuit monitors microprocessor or microcontroller activity. During normal operation, the microprocessor or microcontroller should repeatedly toggle the watchdog input (WDI) before the supervisor's watchdog timeout period elapses to confirm that the system is executing code properly. If the microprocessor or microcontroller does not provide a valid watchdog input transition before the timeout period expires, the supervisor asserts a watchdog ($\overline{WDO}$) output to signal that the system is not executing code as expected. The watchdog output pulse can be used to reset the microprocessor or microcontroller, or it may be used to interrupt the system to warn of execution errors. The MAX16152 and MAX16153 feature a manual reset input ($\overline{MR}$) to allow an external pushbutton or logic signal to initiate a reset pulse. The MAX16154 and MAX16155 feature a logic input (WD_EN) that allows the system to enable and disable the watchdog function.

The MAX16152 and MAX16154 are offered in a 0.86mm x 1.27mm 6-bump WLP, while the MAX16153 and MAX16155 are offered in 6-pin SOT23 package. All devices operate over the -40ºC to +125ºC temperature range.

Applications

- Portable/Battery-Powered Equipment
- Tablets/e-Readers/Mobile Devices
- Glucose Monitors/Patient Monitor
- Metering

Benefits and Features

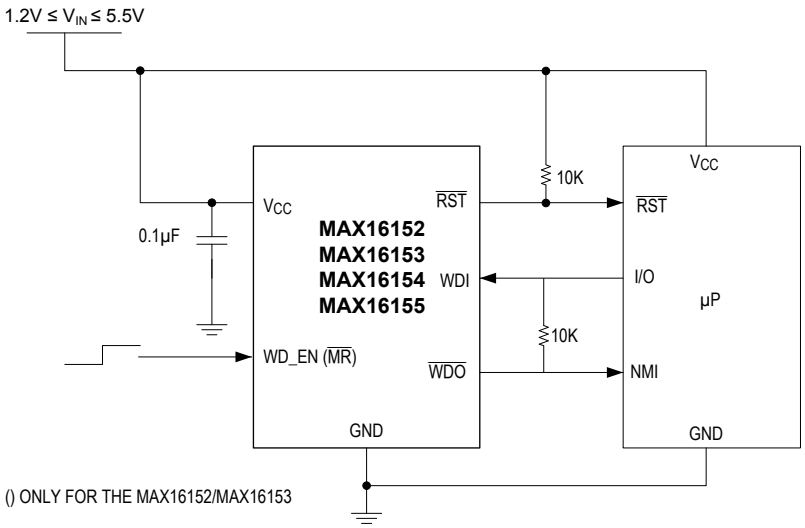
- 400nA (typ) Supply Current
- 1.2V to 5.5V Operating Supply Range
- Monitors Supply Voltage and Provides System Reset Signal
- 1.5V to 5V Input Threshold Range in 100mV Increments
- Watchdog Function Detects Faulty Code Execution
- Open-Drain Reset and Watchdog Outputs
- Watchdog Timer Enable Input
- 6-Bump WLP Package
- 6-Pin SOT23 Package
- -40°C to +125°C Operating Temperature Range

***Ordering Information* appears at end of data sheet.**

19-100532; Rev 2; 8/19

maxim integrated™

Typical Application Circuit



Absolute Maximum Ratings

V_{CC} to GND ..... -0.3V to +6V
WDI, WD_EN to GND ..... -0.3V to V_{CC} + 0.3V
WDO, RST to GND ..... -0.3V to +6V
Maximum Current, Any Pin (input/output) 20mA
Continuous Power Dissipation (WLP) (T_A = +70°C, derate 10.5 mW/°C above +70°C) 840mW
Continuous Power Dissipation (SOT23) (T_A = +70°C, derate 8.70mW/°C above +70°C) 696mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

6 SOT23

Package Code	U6+1
Outline Number	21-0058
Land Pattern Number	90-0175
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	115
Junction-to-Case Thermal Resistance (θ_{JC})	80

6 WLP

Package Code	W60C1+2
Outline Number	21-100258
Land Pattern Number	—
Thermal Resistance, Four-Layer Board:	
Junction-to-Case Thermal Resistance (θ_{JC})	95

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

((V_{CC} = 1.2V to 5.5V, T_A = -40ºC to +125ºC. Limits over the operating temperature range and relevant supply voltage range are guaranteed by production test and/or characterization. Typical values are at T_A = +25ºC and V_{CC} = V_{TH} + 150mV.))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range			1.2		5.5	V
Supply Current		Outputs not asserted, V_{CC} = V_{TH} + 150mV		400	900	nA
V_{CC} Threshold Range			1.5		5	V
V_{CC} Reset Threshold Accuracy	V_{TH_AC}	V_{CC} falling	-2.5		+2.5	%
V_{CC} Reset Threshold Hysteresis		V_{CC} rising		0.4		%
V_{CC} to Reset Delay	t_{RD}	V_{CC} falling from (V_{TH} + 100mV) to (V_{TH} - 100mV)		80		µs
Reset Timeout Period Accuracy	t_{RP_AC}	Note 1	-50		+50	%
WATCHDOG						
Watchdog Timeout Period Accuracy	t_{WD_AC}		-50		+50	%
Watchdog Startup Delay Accuracy	$t_{START-UP_AC}$		-50		+50	%
Watchdog Setup Time	t_{SETUP}	Time between low-to-high transition of WD_EN and watchdog timer enabled.		300		µs
Output Voltage Low	V_{OL}	V_{CC} ≥ 1.0V, I_{SINK} = 50µA			0.3	V
		V_{CC} > 2.7V, I_{SINK} = 1.2mA			0.3	
		V_{CC} > 4.5V, I_{SINK} = 3.2mA			0.4	
Watchdog Input Pulse Width	t_{WDI}	After $\overline{WDO}$ deasserted	1			µs
Watchdog Output Pulse Width	t_{WDO}		100		300	ms
Input Voltage High	V_{IH}		0.8 x V_{CC}			V
Input Logic-Low	V_{IL}	WDI, $\overline{MR}$, WD_EN; V_{CC} ≥ 3.3V			0.3 x V_{CC}	V
		WDI, $\overline{MR}$, WD_EN; V_{CC} ≥ 1.5V			0.3 x V_{CC}	
Watchdog Output Leakage Current		$V_{\overline{WDO}}$ = 0 to 5.5V, output deasserted			1	µA
Reset Ouput Leakage Current		$V_{\overline{RST}}$ = 0 to 5.5V, reset output deasserted			1	µA
WD_EN Input Glitch Rejection				300		ns
Manual Reset Input Glitch Rejection				200		ns

Electrical Characteristics (continued)

((V_{CC} = 1.2V to 5.5V, T_A = -40ºC to +125ºC. Limits over the operating temperature range and relevant supply voltage range are guaranteed by production test and/or characterization. Typical values are at T_A = +25ºC and V_{CC} = V_{TH} + 150mV.))

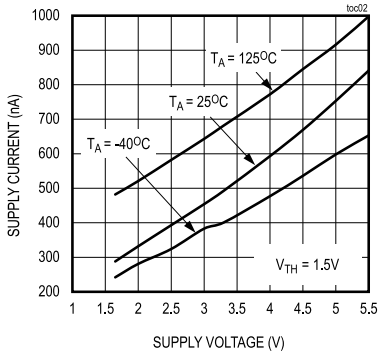
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Manual Reset Input to Reset Output Delay	t_{MRD}			250		ns
Manual Reset Internal Pullup Resistor			70	100	145	kΩ
Input Leakage Current		$\overline{MR}$, WDI, WD_EN. Input connected GND or V_{CC}	-1		+1	µA

Note 1: In addition to the specified tolerance, t_{RP} has an uncertainty of ±4ms due to the power-up delay of internal blocks.

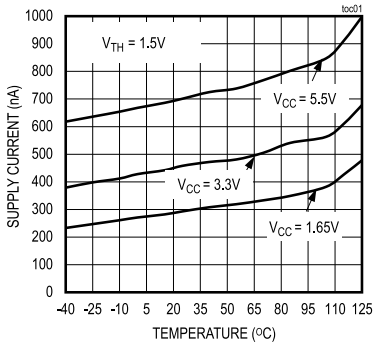
Typical Operating Characteristics

(V_{CC} = 1.2V TO 5.5V, T_A = -40ºC TO 125ºC)

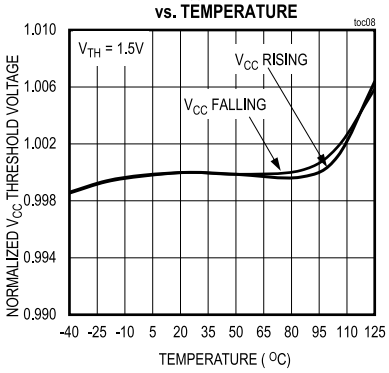
SUPPLY CURRENT vs. SUPPLY VOLTAGE



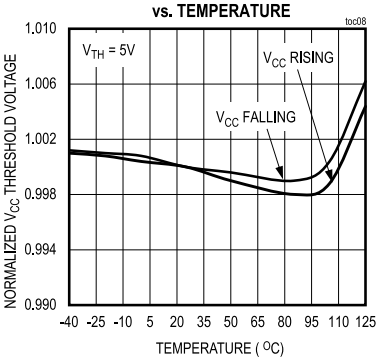
SUPPLY CURRENT vs. TEMPERATURE



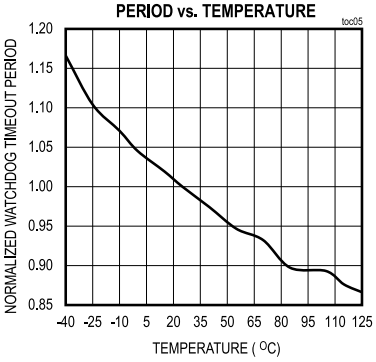
NORMALIZED V_{CC} THRESHOLD VOLTAGE vs. TEMPERATURE



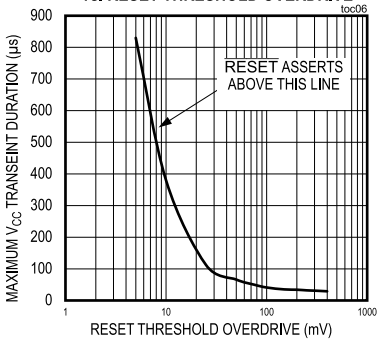
NORMALIZED V_{CC} THRESHOLD VOLTAGE vs. TEMPERATURE



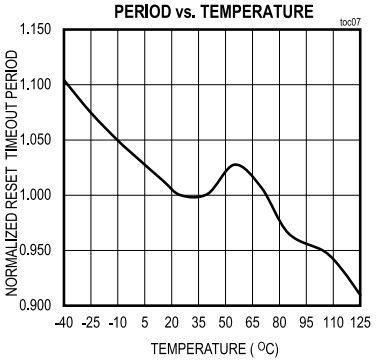
NORMALIZED WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



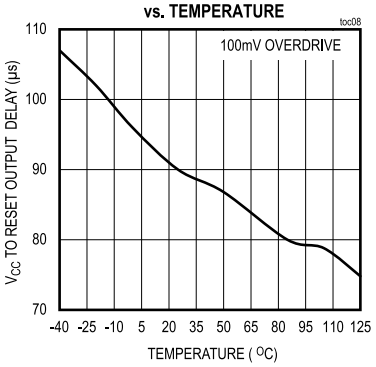
MAXIMUM V_{CC} TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



NORMALIZED RESET TIMEOUT PERIOD vs. TEMPERATURE

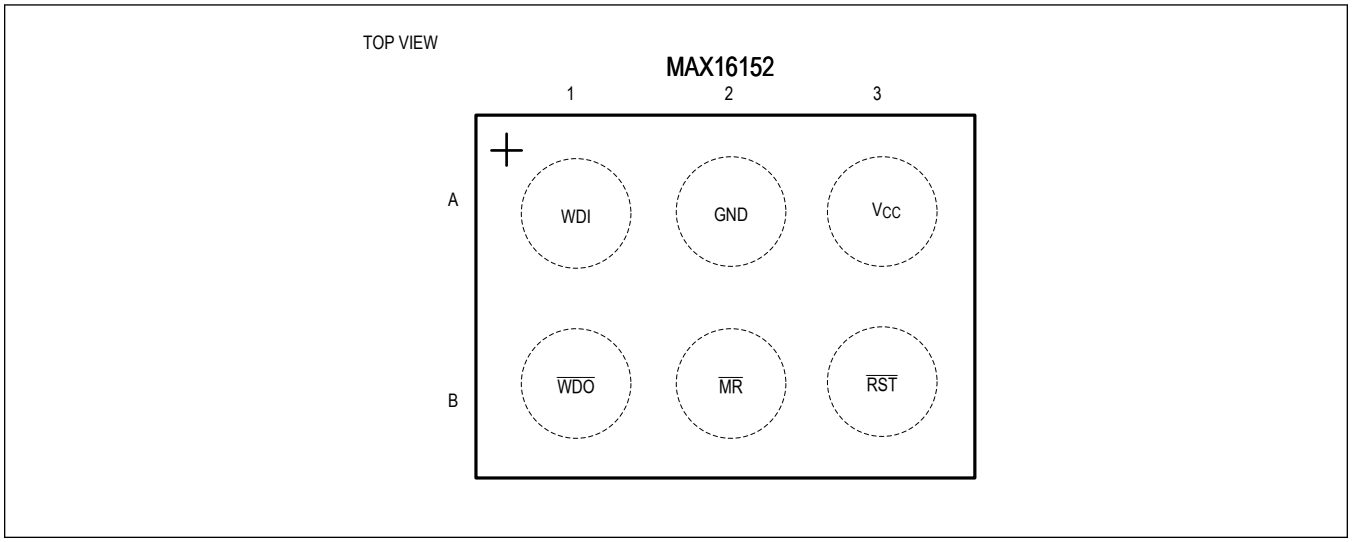


V_{CC} TO RESET OUTPUT DELAY vs. TEMPERATURE

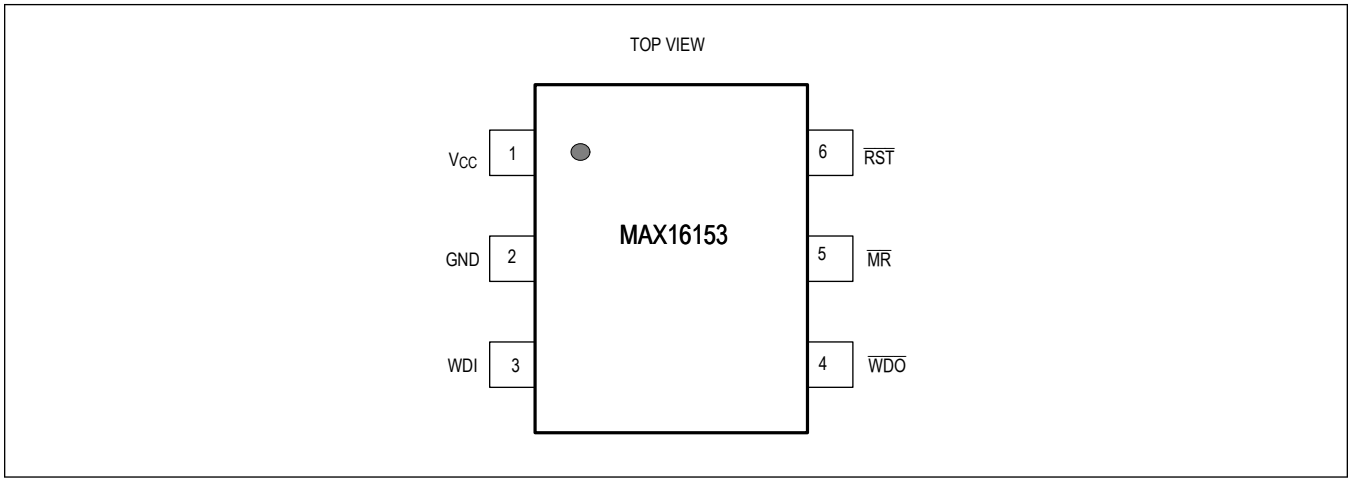


Pin Configurations

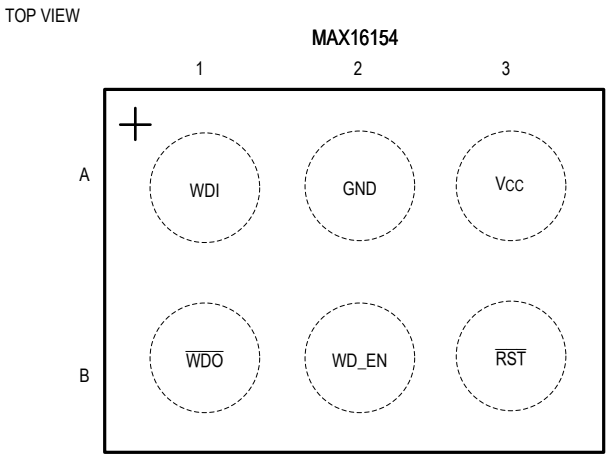
6 WLP



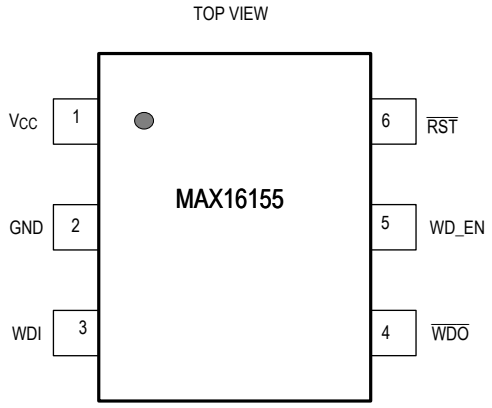
6 SOT23



6 WLP



6 SOT23



Pin Description

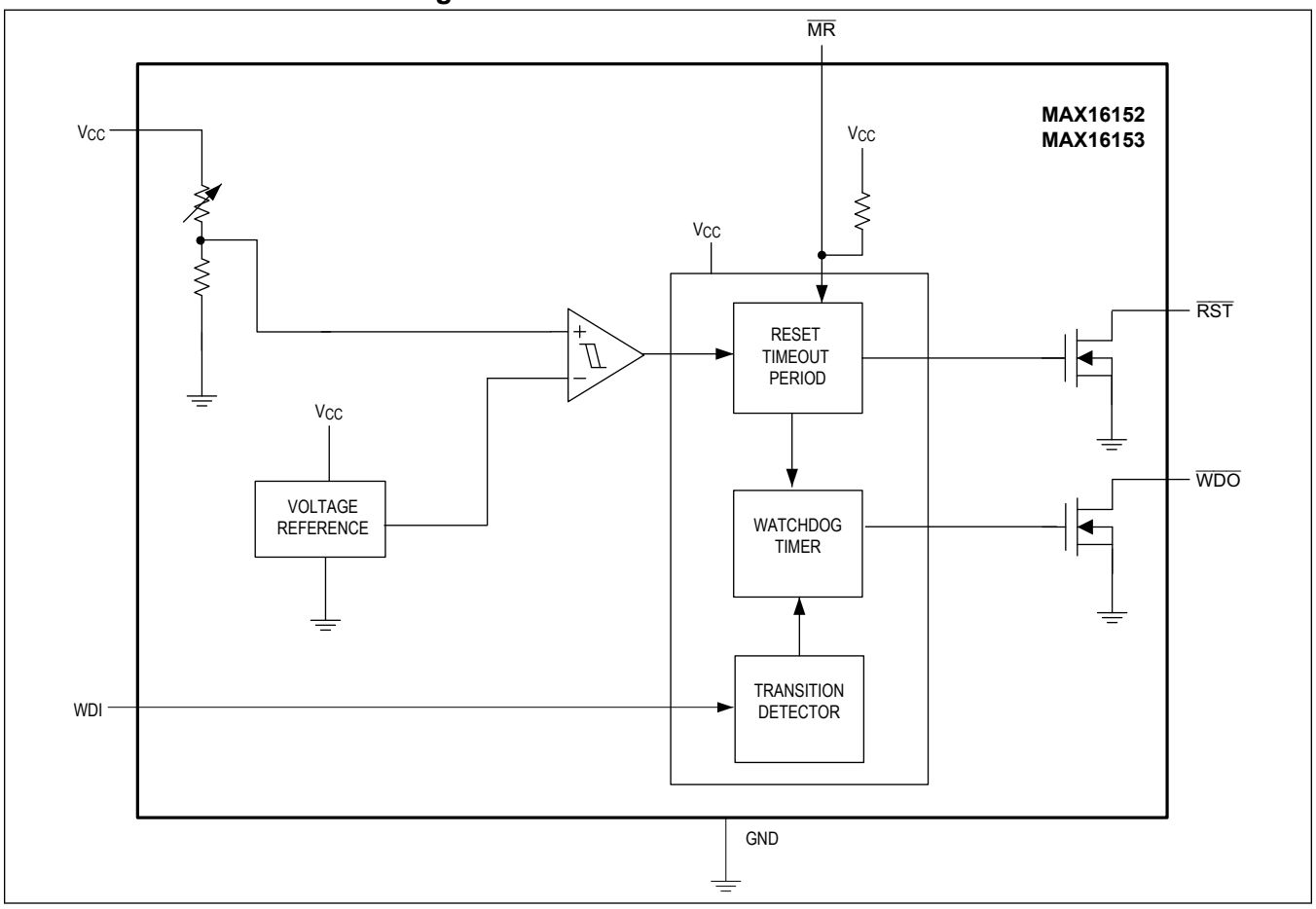
PIN				NAME	FUNCTION
MAX16152	MAX16153	MAX16154	MAX16155		
A3	1	A3	1	V_{CC}	Supply Voltage. V_{CC} is the power supply input and the monitoring input. Bypass with a 0.1µF capacitor to GND.
A2	2	A2	2	GND	Ground
A1	3	A1	3	WDI	Watchdog Input. If WDI remains either high or low for the duration of the watchdog timeout period (t_{WD}), $\overline{WDO}$ pulses low for the watchdog output pulse width, t_{WDO}. The internal watchdog timer clears whenever $\overline{RST}$ is de-asserted or whenever WDI sees a falling edge.

Pin Description (continued)

PIN				NAME	FUNCTION
MAX16152	MAX16153	MAX16154	MAX16155		
B1	4	B1	4	$\overline{WDO}$	Watchdog Output. $\overline{WDO}$ pulses low for the watchdog output pulse width, t_{WDO}, when the internal watchdog times out. $\overline{WDO}$ is an open-drain output and requires a pull-up resistor.
B2	5	—	—	$\overline{MR}$	Manual Reset Input. Drive $\overline{MR}$ low to manually reset the device. $\overline{RST}$ remains asserted for the reset timeout period after $\overline{MR}$ is released. $\overline{MR}$ is internally pulled up to V_{CC} with a 100kΩ resistor.
—	—	B2	5	WD_EN	Watchdog Enable Input. Drive WD_EN high to enable the watchdog timer. Drive WD_EN low to disable the watchdog timer.
B3	6	B3	6	$\overline{RST}$	Reset Output. $\overline{RST}$ asserts when V_{CC} falls below the factory-set threshold. When V_{CC} goes above V_{TH}+ V_{HYS}, $\overline{RST}$ remains asserted for the reset timeout period t_{RP} and then de-asserts. $\overline{RST}$ is an open-drain output and requires a pull up resistor.

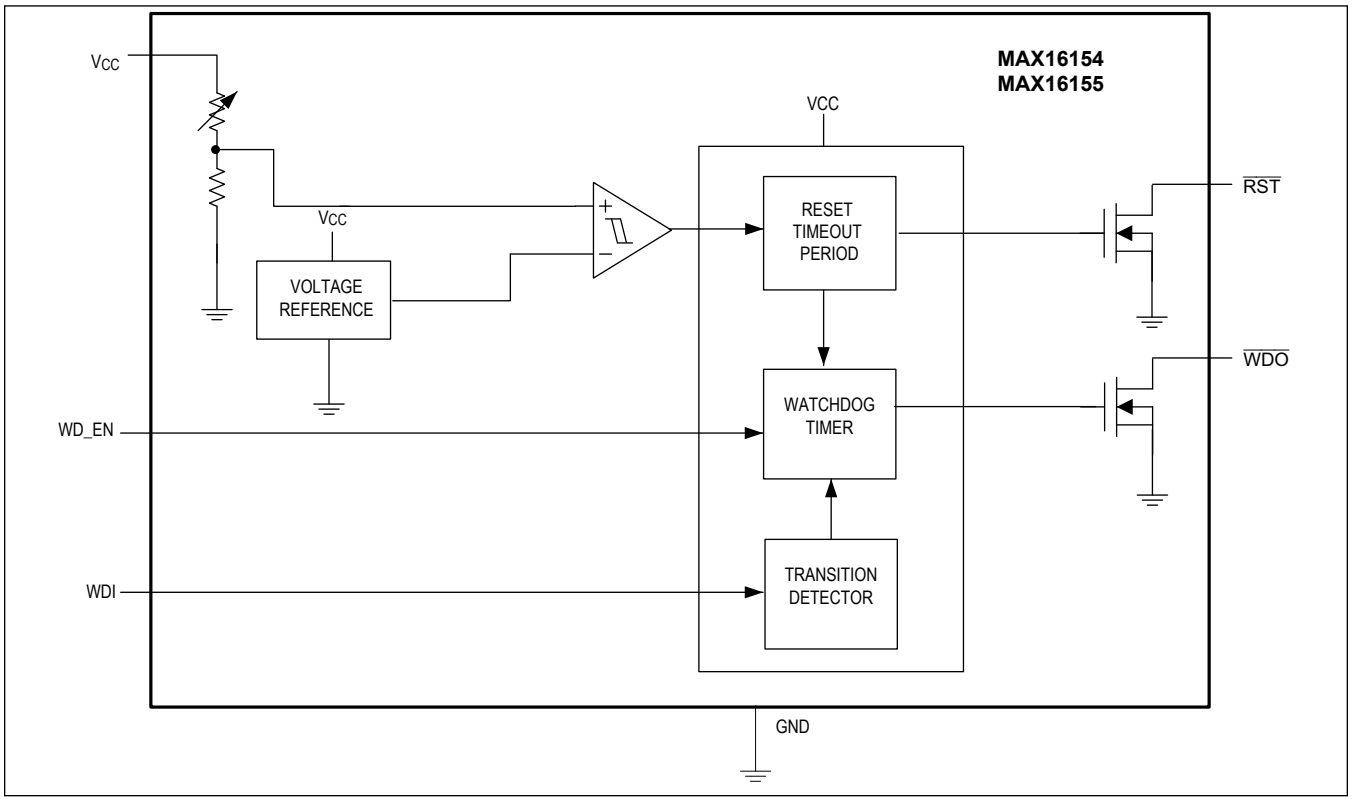
Functional Diagrams

MAX16152/MAX16153 Block Diagram



Functional Diagrams (continued)

MAX16154/MAX16155 Block Diagram



Detailed Description

The MAX16152/MAX16153/MAX16154/MAX16155 are ultra-low-current supervisory circuits that monitor a single system supply voltage and assert an active-low reset signal when the supply voltage drops below the factory-trimmed reset threshold. After the supply voltage rises above the threshold voltage, the reset output remains asserted during the reset timeout period, and finally asserts after the timeout period ends. In addition, a watchdog timer circuit monitors microprocessor or microcontroller activity. During normal operation, the microprocessor or microcontroller toggles the WDI input periodically with a valid logic transition (low to high or high to low). If the WDI input is toggled within the watchdog timeout period (t_{WD}), the internal timer is cleared and restarted, and the $\overline{WDO}$ output remains high. If the input is not strobed before the timeout period expires, the watchdog output is asserted low for a period equal to the watchdog output pulse width (t_{WDO}).

Input Threshold

The MAX16152/MAX16153/MAX16154/MAX16155 monitor V_{CC} with ±2.5% accuracy across the full temperature and supply voltage ranges. The input threshold is programmable from 1.5V to 5V in approximately 100mV increments. Contact Maxim for thresholds not listed in the *Ordering Information* table.

Watchdog

The MAX16152/MAX16153/MAX16154/MX16155 offer flexible watchdog circuits for monitoring microprocessor or microcontroller activity. During normal operation, the internal timer is cleared and restarted each time the WDI input undergoes a valid logic transition (high-to-low) within the selected timeout period (t_{WD}). The WDO remains high as long as the WDI input is strobed within the selected timeout period. If the WDI input is not strobed before the timeout period expires, the watchdog output is asserted low for the watchdog output pulse width (t_{WDO}). The MAX16154 and MAX16155 feature a logic input to enable/disable the watchdog timer during normal operation while the MAX16152 and MAX16153 does not. The watchdog timer for the MAX16152 and MAX16153 can be disabled by leaving the WDI floating.

Watchdog Startup Delay

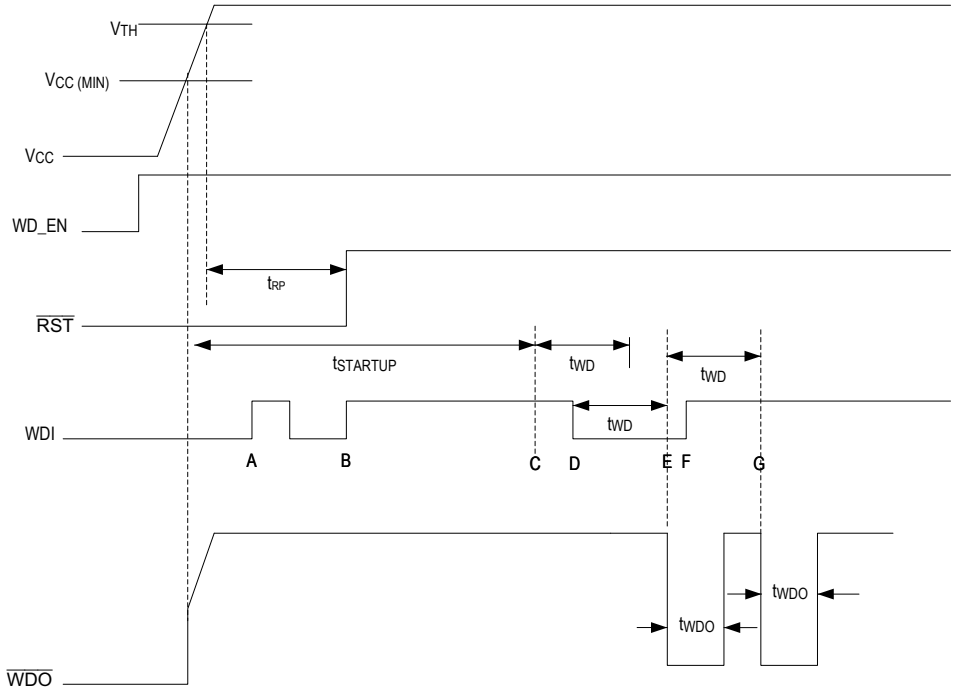
All devices feature a factory-set startup delay. The startup delay provides an initial delay for the watchdog timer circuit to power up and initialize before assuming responsibility for normal watchdog input monitoring. For the MAX16152 and MAX16153, monitoring of the WDI input begins after the start-up time is complete. For the MAX16154 and MAX16155, monitoring of the WDI input begins after the start-up delay if WD_EN is pulled high. To ensure that the system generates no undesired watchdog outputs, the routine watchdog input transitions should begin before the minimum startup delay period has expired. The startup delay is activated after the reset output is de-asserted. See the *Selector Guide* for available watchdog startup delay options.

Watchdog Timeout Period

An open-drain, active-low watchdog output ($\overline{WDO}$) asserts if a valid watchdog input transition is not received before the timeout period elapses. See the *Selector Guide* for available watchdog timeout period options.

Watchdog Enable Input (WD_EN)

The MAX16154 and MAX16155 feature an active-high logic input (WD_EN) to enable or disable the watchdog function. Applying a logic-low to WD_EN disables the watchdog function, causing the MAX16154 and MAX16155 to ignore any signals applied to WDI. Applying a logic-high to WD_EN enables the watchdog function after 300µs (max) of set up time t_{SETUP}. See Figure 1, Figure 2, and Figure 3 for more details.



A B TRANSITION(S) ON WDI INGORED DURING STARTUP DELAY PERIOD.

C WATCHDOG TIMER STARTS AFTER STARTUP DELAY AND $\overline{WDO}$ IS DEASSERTED.

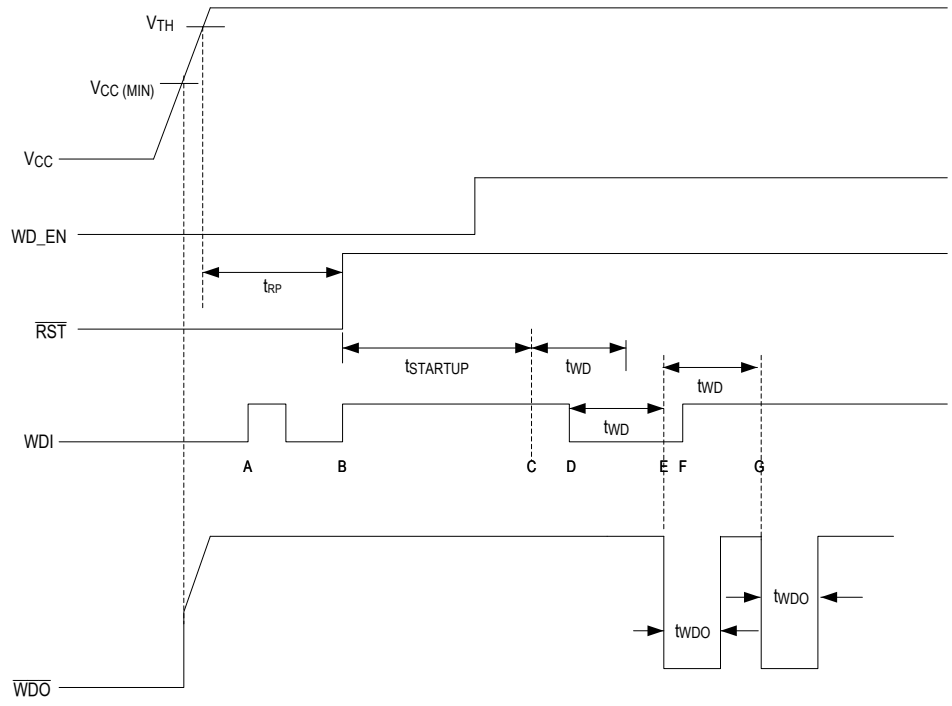
D TRANSITION ON WDI OCCURS BEFORE WATCHDOG TIMEOUT PERIOD. WATCHDOG TIMER CLEARS AND RESTARTS TIMER EVERY TIME THERE IS A HIGH-TO-LOW TRANSITION WITH t_{WD}.

E WATCHDOG TIMES OUT, $\overline{WDO}$ ASSERTS AND THE NEXT WATCHDOG TIMER STARTS AT THE FALLING EDGE OF $\overline{WDO}$.

F TRANSITIONS ON WDI INGNORED WHEN $\overline{WDO}$ ASSERTED.

G WATCHDOG TIMES OUT, $\overline{WDO}$ ASSERTS.

Figure 1. Watchdog Timing Characteristics with WD_EN Active During Power-Up



A B TRANSITIONS ON WDI INGORED DURING t_{RP} and $t_{STARTUP}$ DELAY.

C WATCHDOG TIMER STARTS AFTER STARTUP DELAY AND WD_EN IS DRIVEN HIGH.

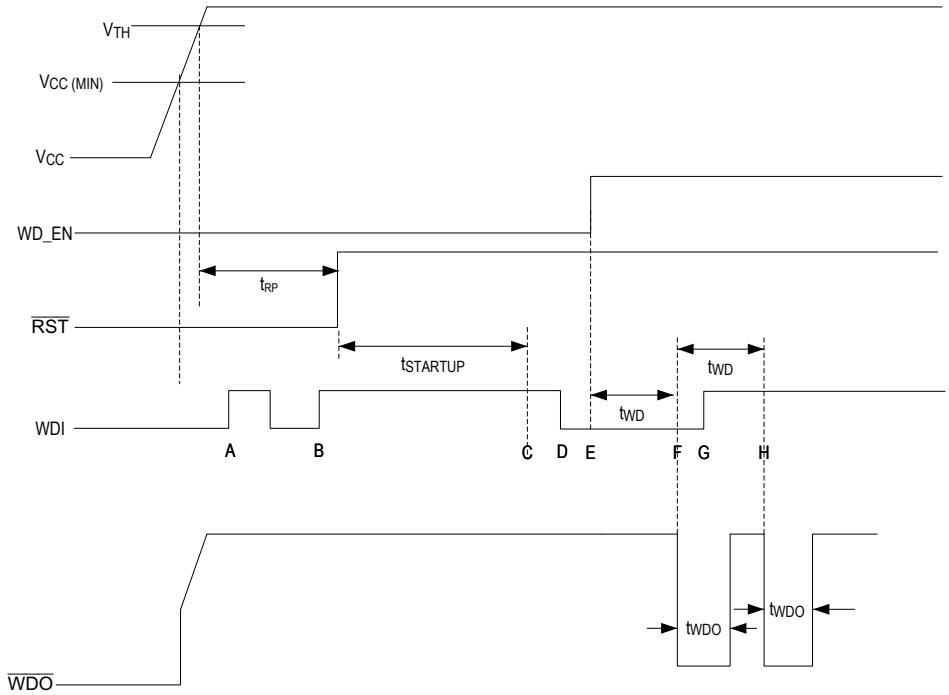
D TRANSITION ON WDI OCCURS BEFORE WATCHDOG TIMEOUT PERIOD. WATCHDOG TIMER CLEARS AND RESTARTS TIMER EVERY TIME THERE IS A HIGH- TO-LOW TRANSITION WITH t_{WD}.

E WATCHDOG TIMES OUT, $\overline{WDO}$ ASSERTS AND THE NEXT WATCHDOG TIMER STARTS AT THE FALLING EDGE OF $\overline{WDO}$.

F TRANSITIONS ON WDI INGNORED WHEN $\overline{WDO}$ ASSERTED.

G WATCHDOG TIMES OUT, $\overline{WDO}$ ASSERTS.

Figure 2. Watchdog Timing Characteristics with WD_EN Active During Startup



A B TRANSITIONS ON WDI INGORED DURING t_{RP} and $t_{STARTUP}$ DELAY.

C WATCHDOG DOES NOT START AFTER STARTUP PERIOD SINCE WD_EN IS HELD LOW.

D TRANSITION ON WDI IGNORED WHEN WD_EN IS HELD LOW.

E WATCHDOG TIMER STARTS AFTER RISING EDGE ON WD_EN.

F WATCHDOG TIMES OUT, $\overline{WDO}$ ASSERTS AND THE NEXT WATCHDOG TIMER STARTS AT THE FALLING EDGE OF $\overline{WDO}$.

G TRANSITION ON WDI IGNORED AFTER $\overline{WDO}$ ASSERTS.

H WATCHDOG TIMES OUT, $\overline{WDO}$ ASSERTS.

Figure 3. Watchdog Timing Characteristics with WD_EN Active After Startup Time

Watchdog Input Signal

Watchdog timing is measured from the last WDI falling edge associated with a pulse of at least 1µs (min) in width. WDI transitions are ignored when $\overline{WDO}$ and/or $\overline{RST}$ are asserted, and during the startup delay period. Watchdog input transitions are also ignored for a setup period (t_{SETUP}) of up to 300µs after WD_EN is asserted.

Reset Timeout Period

The MAX16152/MAX16153/MAX16154/MAX16155 feature an active-low open-drain reset output ($\overline{RST}$) that asserts low when V_{CC} drops below the factory-set threshold voltage, V_{TH}. The reset output remains asserted as long as V_{CC} remains below the threshold voltage. When V_{CC} rises above the threshold voltage plus the required hysteresis, the reset output remains asserted during the reset timeout period, and then de-asserts. See Figure 4 for more details. Contact Maxim for reset timeout period options not listed in the *Ordering Information* table.

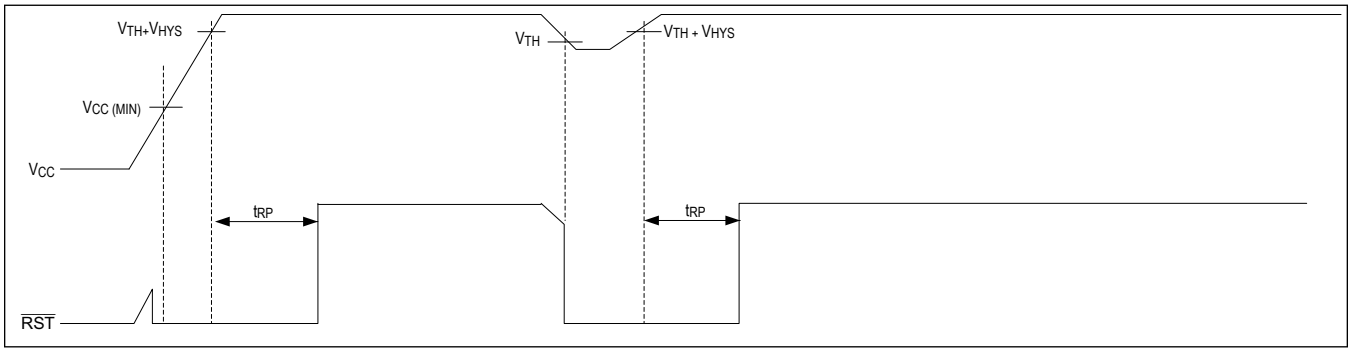


Figure 4. Reset Output Timing Diagram

Note: The reset timeout period does not include additional power up delay specified in the *Electrical Characteristics* table.

Manual Reset

The MAX16152 and the MAX16153 include an active-low manual reset input, $\overline{MR}$. Forcing $\overline{MR}$ low asserts the reset output after 250ns (typ) delay period (t_{MRD}). The reset output remains asserted as long as $\overline{MR}$ is held low. The reset output de-asserts after the reset timeout period when $\overline{MR}$ is released. See Figure 5 below for $\overline{MR}$ timing characteristics. $\overline{MR}$ has an internal pullup resistor to V_{CC} and can be left unconnected if not used.

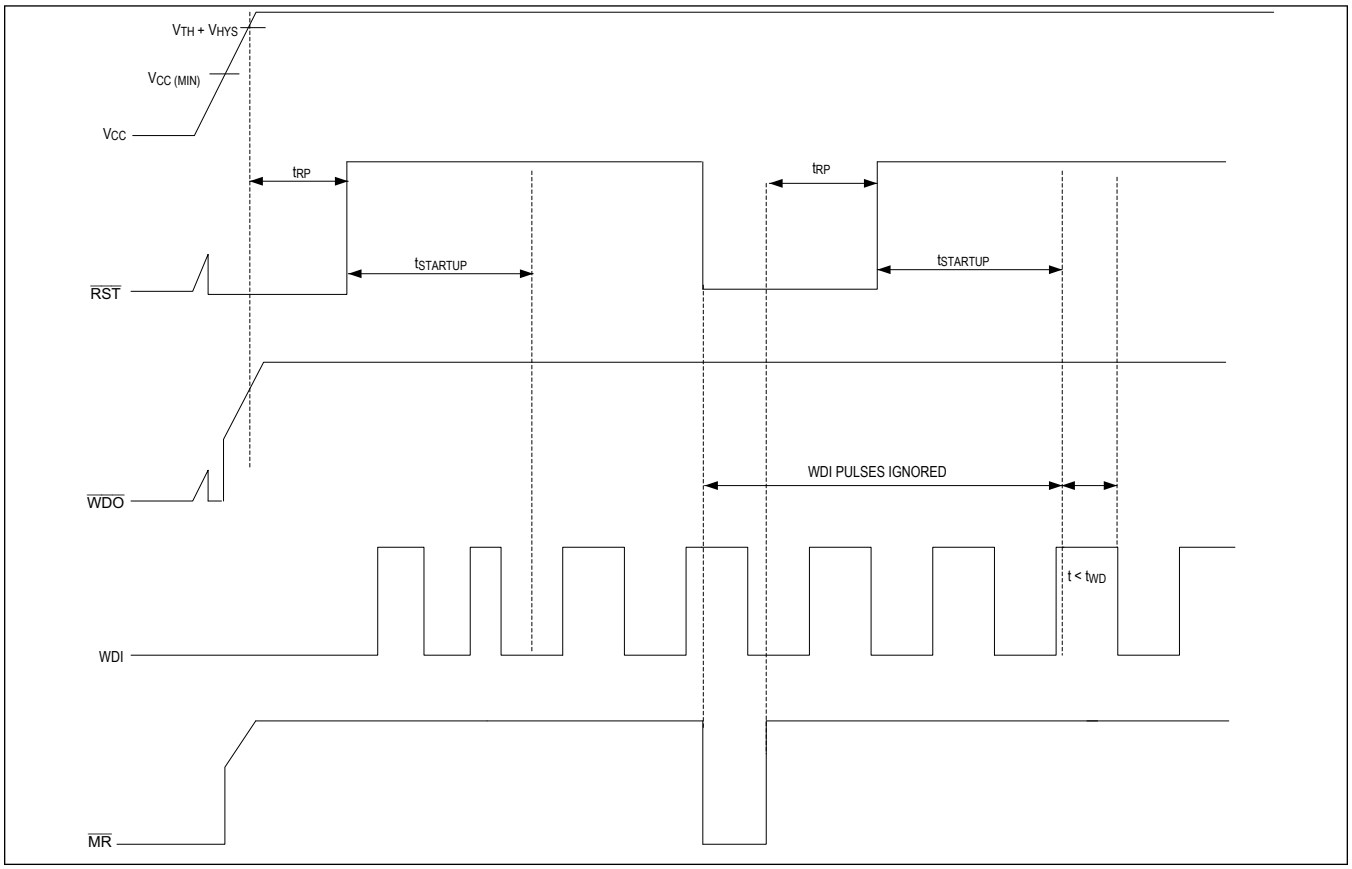


Figure 5. Manual Reset Input Timing Characteristics

Applications Information

Power Supply Bypassing

The MAX16152/MAX16153/MAX16154/MAX16155 operate from a 1.20V to 5.5V supply. Bypass V_{CC} to ground with a 0.1µF capacitor as close to the device as possible to improve transient immunity. For fast-rising V_{CC} transients, additional capacitance may be required. V_{CC} rise time >50µs ensures proper operation.

Watchdog Software Considerations

To help the watchdog timer monitor software execution more closely, set and reset the watchdog input at different points in the program, rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop, in which the watchdog timer would continue to be reset inside the loop, keeping the watchdog from timing out. Figure 6 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the end of every subroutine or loop, then set high again when the program returns to the beginning. If the program should hang in any subroutine, the problem would be quickly corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing $\overline{WDO}$ to pulse.

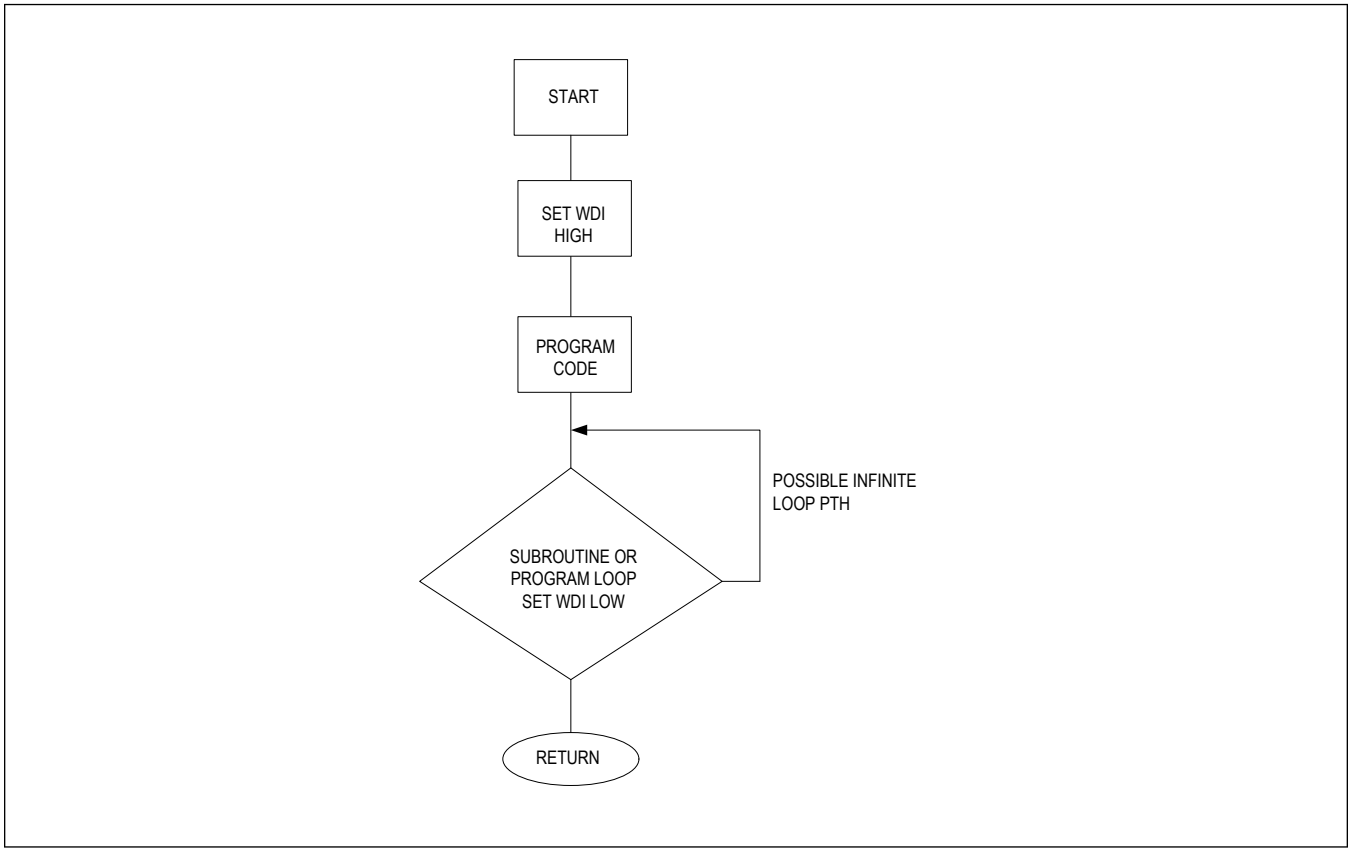
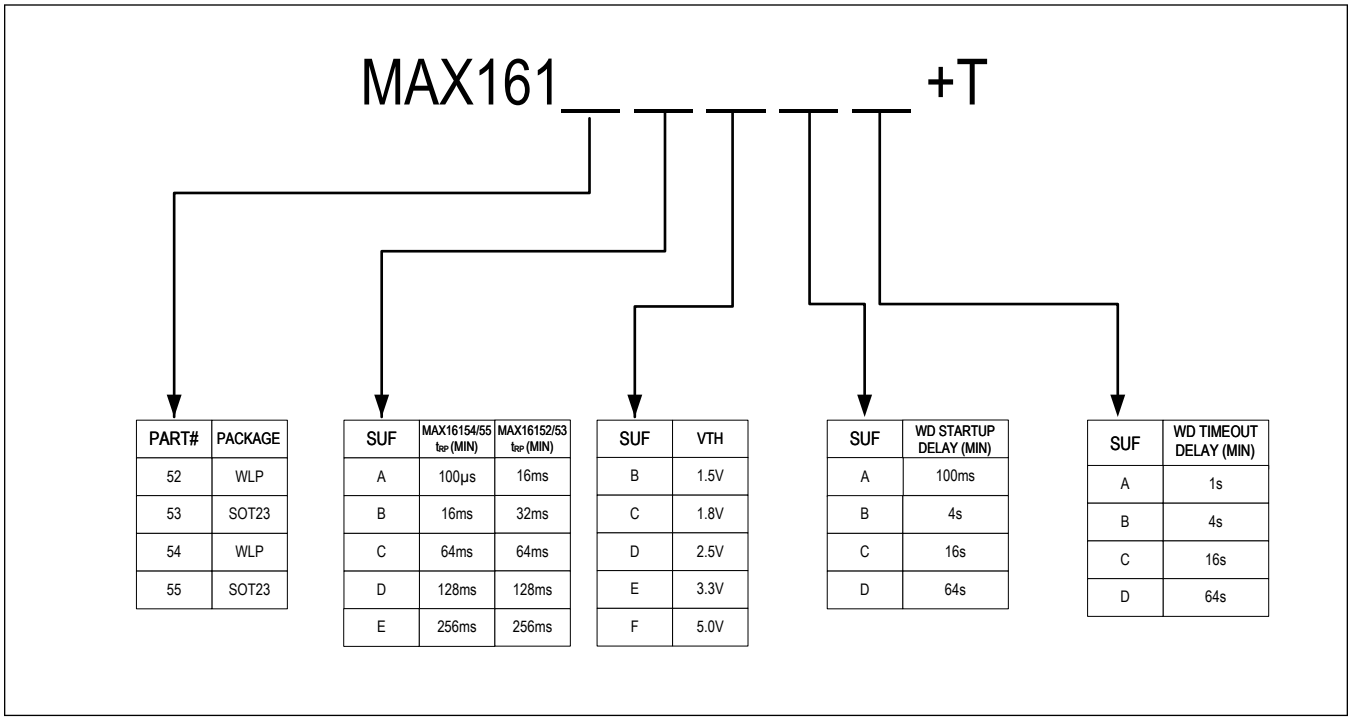


Figure 6. Watchdog Flow Diagram

Negative-Going V_{CC} Transients Protection

The MAX16152/MAX16153/MAX16154/MAX16155 are relatively immune to short-duration negative-going V_{CC} transients (glitches). It is usually undesirable to reset the system when V_{CC} experiences only small glitches. The *Typical Operating Characteristics* show Maximum *Transient Duration vs. Reset Threshold Overdrive*, for which reset pulses are not generated. The graph was produced using negative-going V_{CC} pulses, starting above V_{TH} and ending below the reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. A 0.1µF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

Selector Guide



PART#	PACKAGE
52	WLP
53	SOT23
54	WLP
55	SOT23

SUF	MAX16154/55 t_{RP} (MIN)	MAX16152/53 t_{RP} (MIN)
A	100µs	16ms
B	16ms	32ms
C	64ms	64ms
D	128ms	128ms
E	256ms	256ms

SUF	VTH
B	1.5V
C	1.8V
D	2.5V
E	3.3V
F	5.0V

SUF	WD STARTUP DELAY (MIN)
A	100ms
B	4s
C	16s
D	64s

SUF	WD TIMEOUT DELAY (MIN)
A	1s
B	4s
C	16s
D	64s

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX16152ABAD+T	-40ºC to +125ºC	6 WLP
MAX16153_ _ _ _ +T*	-40ºC to +125ºC	6 SOT23
MAX16154_ _ _ _+T*	-40ºC to +125ºC	6 WLP
MAX16155ABAD+T	-40ºC to +125ºC	6 SOT23

Note: See the Selector Guide for reset timeout period, threshold voltage, watchdog start up delay, and watchdog timeout options. For additional options and future products, please visit www.maximintegrated.com.

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape-and-reel.

**Future product—Contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/19	Initial release	—
1	4/19	Updated *Package Information* section	3
2	8/19	Updated *Typical Application Circuit, Electrical Characteristics* table, *Pin Configuration* diagrams, *Pin Description* table, Figures 1–3, *Selector Guide*, and *Ordering Information* table	2, 4, 5, 7–9, 13–15, 19

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