MAX15090B/MAX15090C

2.7V to 18V, 12A, Hot-Swap Solution with Current Report Output

General Description

The MAX15090B/MAX15090C ICs are integrated solutions for hot-swap applications requiring the safe insertion and removal of circuit line cards from a live backplane. The devices integrate a hot-swap controller, 6mΩ power MOSFET, and an electronic circuit-breaker protection in a single package.

The devices integrate an accurate current-sense circuitry and provide 220µA/A of proportional output current. The devices are designed for protection of 2.7V to 18V supply voltages.

These devices implement a foldback current limit during startup to control inrush current lowering di/dt and keep the MOSFET operating under safe operating area (SOA) conditions. After the startup cycle is complete, on-chip comparators provide VariableSpeed/BiLevel™ protection against short-circuit and overcurrent faults, and immunity against system noise and load transients. The load is disconnected in the event of a fault condition. The devices are factory calibrated to deliver accurate overcurrent protection with ±10% accuracy. During a fault condition, the MAX15090B latches off, while the MAX15090C enters autoretry mode.

The devices feature an IN-to-OUT short-circuit detection before startup. The devices provide a power-MOSFET GATE pin to program the slew rate during startup by adding an external capacitor. The devices have overvoltage/undervoltage input pins that can detect an overvoltage/undervoltage fault and disconnect the IN from the OUT. Additional features include internal overtemperature protection, power-good output, and fault-indicator output.

The MAX15090B/MAX15090C ICs are available in a 28-bump, 2.07mm x 3.53mm, power wafer-level package (WLP) and are rated over the -40°C to +85°C extended temperature range.

Applications

- RAID Systems
- Storage Bridge Bay
- Disk Drive Power
- Server I/O Cards
- Industrial

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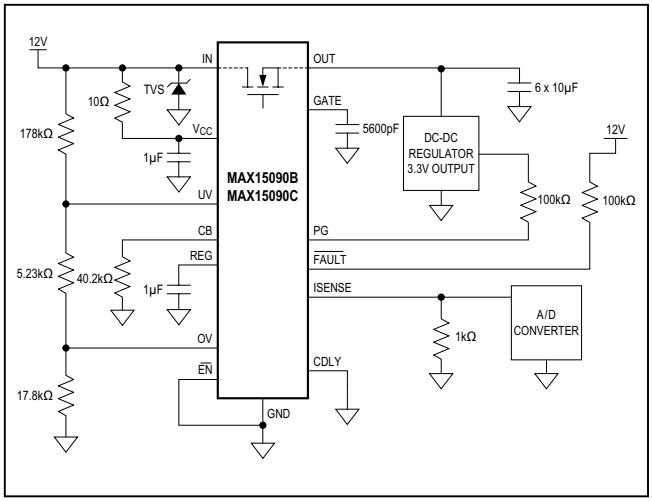
Benefits and Features

- Integration Reduces Solution Size for Blade Servers and Other Space-Constrained Designs
  - Integrated 6mΩ (typ) Internal Power MOSFET Overvoltage Protection
  - Power-Good and Fault Outputs
  - Programmable Undervoltage Lockout
  - Current Reporting Without Need for External R_{SENSE}
  - Thermal Protection
- Flexibility Enables Use in Many Unique Designs
  - 2.7V to 18V Operating Voltage Range
  - Adjustable Circuit-Breaker Current/Current-Limit Threshold
  - Programmable Slew-Rate Control
  - Variable-Speed Circuit-Breaker Response
  - Latchoff or Automatic Retry Options
- Safety Features Ensure Accurate, Robust Protection
  - 12A (max) Load Current Capability
  - ±10% Circuit-Breaker Threshold Accuracy
  - Inrush Current Regulated at Startup with Foldback
  - Implementation for di/dt Control
  - IN-to-OUT Short-Circuit Detection

***Ordering Information* and *Recommended Application Circuit for Hot-Swap Applications* appear at end of data sheet.**

Typical Application Circuit



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Absolute Maximum Ratings

V_{CC} to GND .....-0.3V to +20V
IN to GND.....-0.3V to +20V
OUT to GND.....-0.3V to (V_{IN} + 0.3V)
GATE to OUT .....-0.3V to +6V
CDLY, ISENSE to GND .....-0.3V to (V_{REG} + 0.3V)
$\overline{EN}$, CB, UV, OV to GND .....-0.3V to +6V
REG to GND.....-0.3V to min (+6V, (V_{CC} + 0.3V))
PG, $\overline{FAULT}$ to GND .....-0.3V to +20V

Continuous Power Dissipation (T_A = +70°C)
WLP (derate 23.8mW/°C above +70°C).....1500mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}) .....42°C/W

Junction-to-Case Thermal Resistance (θ_{JC}).....7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial. Thermal resistance can be lowered with improved board design.

Electrical Characteristics

(V_{IN} = V_{CC} = 2.7V to 18V, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 12V, R_{CB} = 33.2kΩ, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V_{CC} Operating Range	V_{CC}		2.7		18	V
IN Operating Range	V_{IN}		2.7		18	V
V_{CC} Supply Current	I_{CC}	V_{IN} = 3V		0.5	0.75	mA
IN Supply Current	I_{IN}	R_{CB} = 40.2kΩ, no load		5.1	6.2	mA
		R_{CB} = 10kΩ, no load		1.4	1.8	
V_{CC} Default Undervoltage Lockout	V_{UVLO}	V_{CC} rising	2.35	2.5	2.65	V
V_{CC} Default Undervoltage-Lockout Hysteresis	V_{UVLO_HYS}			0.1		V
REG Regulator Voltage	V_{REG}	No load, V_{CC} > 4V	3.15	3.35	3.55	V
UV Turn-On Threshold	V_{UV_TH}	V_{UV} rising	1.21	1.23	1.25	V
UV Turn-On Threshold Hysteresis	V_{UV_HYS}	V_{UV} falling		0.1		V
OV Turn-On Threshold	V_{OV_TH}	V_{OV} rising	1.21	1.23	1.25	V
OV Turn-On Threshold Hysteresis	V_{OV_HYS}	V_{OV} falling		0.1		V
$\overline{EN}$ Threshold	$V_{\overline{EN}\_TH}$	$V_{\overline{EN}}$ rising	0.95	1	1.05	V
$\overline{EN}$ Threshold Hysteresis	$V_{\overline{EN}\_HYS}$	$V_{\overline{EN}}$ falling		0.1		V

Electrical Characteristics (continued)

(V_{IN} = V_{CC} = 2.7V to 18V, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 12V, R_{CB} = 33.2kΩ, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OV, UV, $\overline{EN}$ Input Leakage Current	I_{LEAK}	V_{OV} = V_{UV} = $V_{\overline{EN}}$ = 0 to 5V		-1		+1	µA
CB Source Current	I_{THCB_NORM}	Power-on mode			12		µA
CURRENT LIMIT							
Circuit-Breaker Accuracy (Note 3)	$I_{CB,TH}$	V_{IN} = 12V	R_{CB} = 40.2kΩ	10.85	12.06	13.27	A
			R_{CB} = 10kΩ	2.7	3	3.3	
Circuit-Breaker Accuracy Deviation		R_{CB} = 10kΩ to 40.2kΩ, compared to nominal current-limit value		-10		+10	%
Slow-Comparator Response Time (Note 4)	t_{SCD}	0.6% overcurrent			1.5		ms
		30% overcurrent			200		µs
Maximum Current Limit During Startup	I_{LIM_MAX}	(see Figure 2)			0.5 x $I_{CB,TH}$		A
Fast-Comparator Threshold	I_{FC_TH}				1.5 x $I_{CB,TH}$		A
Minimum CB Voltage Reference During Foldback (Note 5)	V_{THCB_MIN}	V_{IN} - V_{OUT} > 10V, R_{CB} = 40.2kΩ			60		mV
Maximum CB Voltage Reference During Foldback (Note 5)	V_{THCB_MAX}	V_{IN} - V_{OUT} < 2V, R_{CB} = 40.2kΩ			240		mV
TIMING							
Startup Maximum Time Duration	t_{SU}			43	48	53	ms
Autorestart Delay Time	$t_{RESTART}$				3.2		s
Time Delay Comparator High Threshold	V_{DLY_TH}			1.85	2	2.15	V
Time Delay Pullup Current	I_{DLY}			1.6	1.9	2.2	µA
Output Short Detection at Startup	t_{SHORT}			10.8	12	13.2	ms
MOSFET							
Total On-Resistance	R_{ON}	T_A = +25°C			5.5	7.5	mΩ
		T_A = -40°C to +85°C				9	
GATE Charge Current	I_{GATE}			4.5	5.7	7	µA

Electrical Characteristics (continued)

(V_{IN} = V_{CC} = 2.7V to 18V, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 12V, R_{CB} = 33.2kΩ, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUTS						
$\overline{FAULT}$, PG Output Low Voltage	V_{OL}	Low-impedance state, $I_{\overline{FAULT}}$ = +5mA, I_{PG} = +5mA			0.4	V
$\overline{FAULT}$, PG Output High Leakage Current	I_{OH}	High-impedance state, $V_{\overline{FAULT}}$ = 16V, V_{PG} = 16V			1	µA
CURRENT REPORT						
ISENSE Full-Scale Current	I_{ISENSE}			2.64		mA
ISENSE Gain Ratio		I_{SENSE}/I_{OUT}		220		µA/A
ISENSE Voltage Range	V_{ISENSE}	V_{IN} = 12V	0		2.5	V
ISENSE Offset Error	I_{ISENSE_OFF}	T_A = +25°C	-30		+30	µA
		T_A = -40°C to +85°C	-50		+50	
ISENSE Differential Gain Error	I_{ISENSE_ERROR}	T_A = +25°C, I_{OUT} = 1A, ΔI_{OUT} = 100mA	-2.5		+2.5	%
		T_A = -40°C to +85°C, I_{OUT} = 1A, ΔI_{OUT} = 100mA	-4		+4	
PG THRESHOLD						
PG Threshold	V_{PG}	Measured at V_{OUT}		0.9 x V_{IN}		V
PG Assertion Delay	t_{PG}	From V_{OUT} > V_{PG} and (V_{GATE} - V_{IN}) > 3V	12	16	20	ms
OUT to IN Short-Circuit Detection Threshold	V_{IOSHT}	Measured at V_{OUT}		0.9 x V_{IN}		
OUT Precharge Threshold	V_{PC}	Measured at V_{OUT}		0.5 x V_{IN}		V
THERMAL SHUTDOWN						
Thermal Shutdown	T_{SD}	T_J rising		+150		°C
Thermal-Shutdown Hysteresis		T_J falling		20		°C

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

Note 3: 40.2kΩ is the maximum allowed external resistance value to be connected at CB pin to GND for safe operation. All devices are tested with10kΩ, the parameter specified at R_{CB} = 40.2kΩ is guaranteed by bench characterization and correlation, with respect to the tested parameter at R_{CB} = 10kΩ. The formula that describes the relationship between R_{CB} and the circuit-breaker current threshold is: I_{CB} = R_{CB}/3333.3.

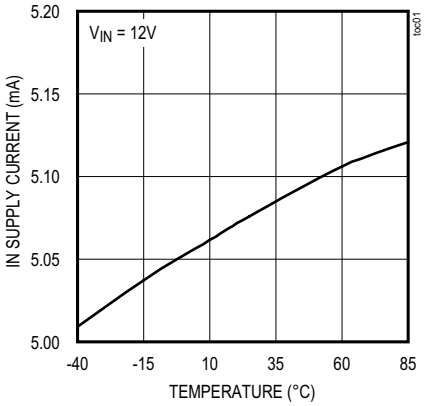
Note 4: The current-limit slow-comparator response time is weighed against the amount of overcurrent so the higher the overcurrent condition, the faster the response time.

Note 5: Foldback is active during the startup phase so the internal power MOSFET operates within SOA.

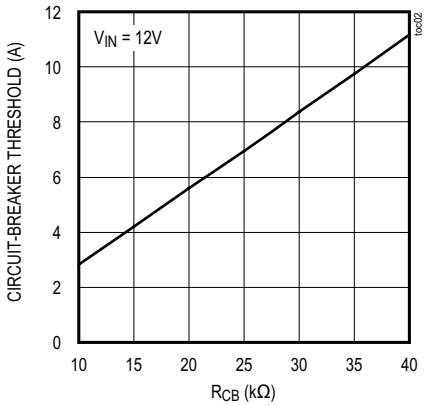
Typical Operating Characteristics

(V_{IN} = V_{CC} = 2.7V to 18V, T_J = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 12V, R_{CB} = 33.2kΩ, and T_J = +25°C.) (Note 3)

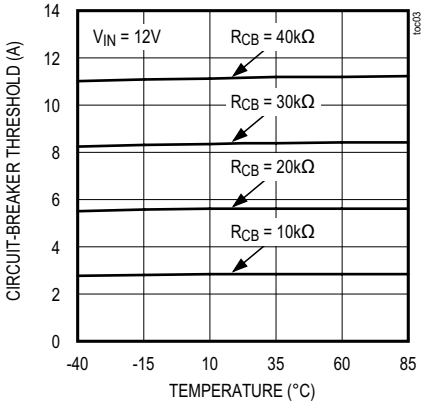
IN SUPPLY CURRENT vs. TEMPERATURE



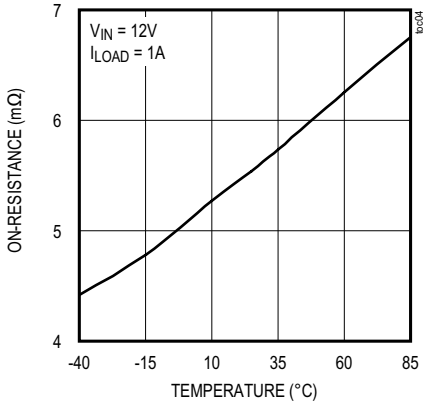
CIRCUIT-BREAKER THRESHOLD vs. CIRCUIT-BREAKER RESISTANCE



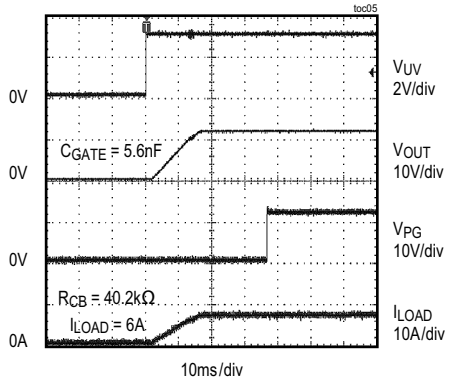
CIRCUIT-BREAKER THRESHOLD vs. TEMPERATURE



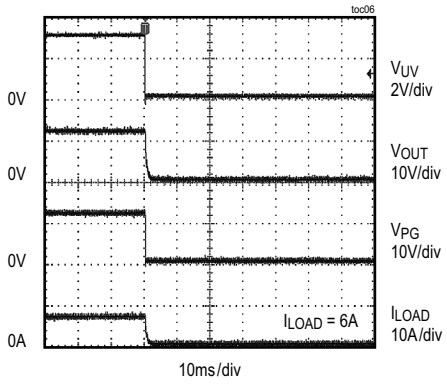
ON-RESISTANCE vs. TEMPERATURE



TURN-ON WAVEFORM



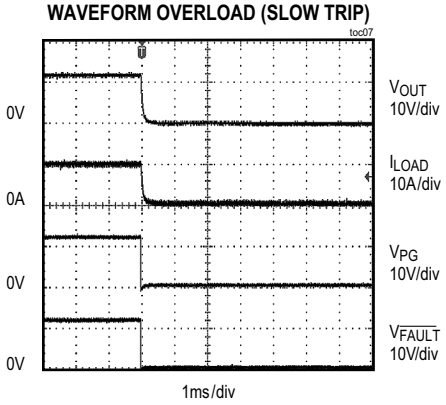
NORMAL TURN-OFF WAVEFORM



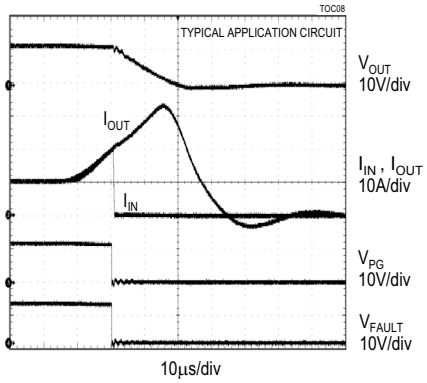
Typical Operating Characteristics (continued)

(V_{IN} = V_{CC} = 2.7V to 18V, T_J = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 12V, R_{CB} = 33.2kΩ, and T_J = +25°C.) (Note 3)

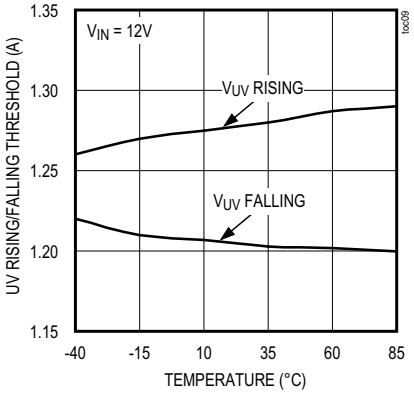
FAULT-SHUTDOWN WAVEFORM OVERLOAD (SLOW TRIP)



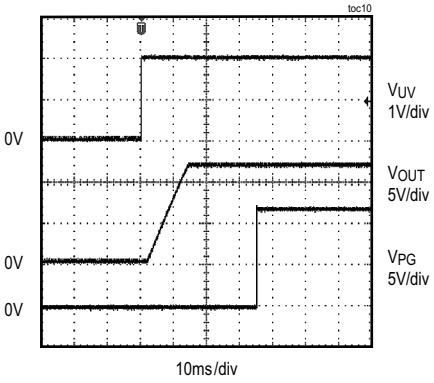
FAULT-SHUTDOWN WAVEFORM OVERLOAD (SHORT CIRCUIT)



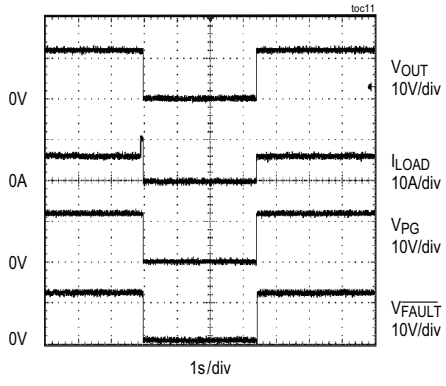
UV RISING/FALLING THRESHOLD VOLTAGE vs. TEMPERATURE



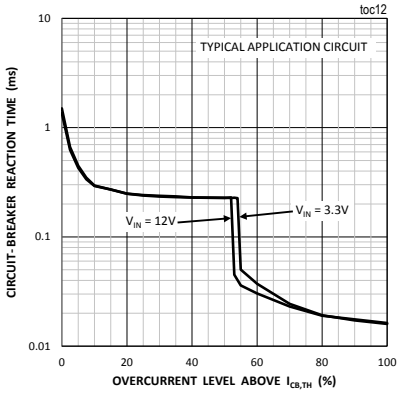
PG ASSERTION DELAY



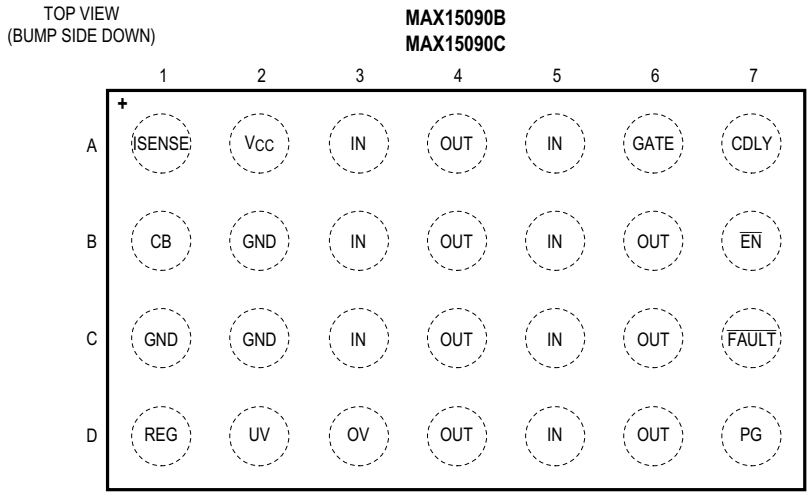
AUTORETRY FUNCTIONALITY



CIRCUIT-BREAKER REACTION TIME vs. OVERCURRENT LEVEL



Bump Configuration



WLP
(2.07mm x 3.53mm)

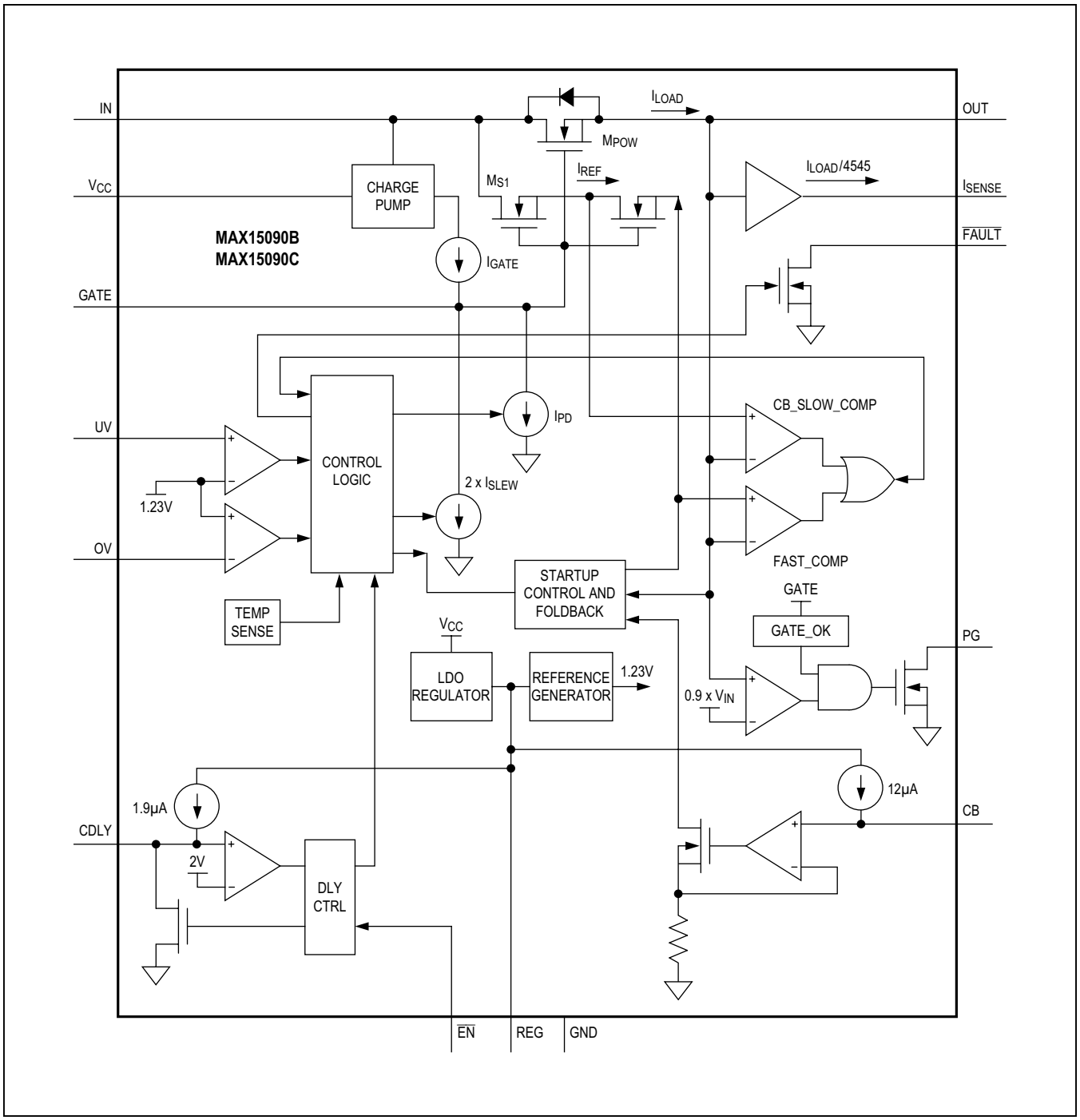
Bump Description

BUMP	NAME	FUNCTION
A1	ISENSE	Current-Sense Output. The ISENSE output sources a current that is proportional to the output current. Connect a resistor between ISENSE and GND to produce a scaled voltage.
A2	V_{CC}	Power-Supply Input. Connect V_{CC} to a voltage between 2.7V and 18V. Connect a Schottky diode (or 6Ω resistor) from IN to V_{CC} and a 1µF bypass capacitor to GND to guarantee full operation in the event V_{IN} collapses during a strong short from OUT to GND.
A3, A5, B3, B5, C3, C5, D5	IN	Supply Voltage Input. IN is connected to the drain of the internal 6mΩ MOSFET. Bypass IN with a transient voltage-suppressor diode to GND for clamping inductive kick transients in the case of fast output short-circuit to GND.
A4, B4, B6, C4, C6, D4, D6	OUT	Load Output. Source of the internal power MOSFET.

Bump Description (continued)

BUMP	NAME	FUNCTION
A6	GATE	GATE of Internal MOSFET. During startup, a 5.7µA current is sourced to enhance the internal MOSFET with a 10V/ms slew rate. Connect an external capacitance from GATE to GND to reduce the output slew rate during startup.
A7	CDLY	Enable Timer Input. Connect a capacitor between CDLY and GND to set a 1s/µF duration timeout delay. The $\overline{EN}$ input has to be pulled low before the timeout delay elapses, to prevent internal MOSFET shutdown after power-up. Minimum required capacitor for CDLY is 1000pF; short to GND if not needed.
B1	CB	Current-Limit Threshold Set. Connect a resistor from CB to GND to set the circuit-breaker threshold. Maximum value of 40.2kΩ can be accepted for safe operation. Having the CB pin connected to GND sets the circuit-breaker threshold at 0A.
B2, C1, C2	GND	Ground
B7	$\overline{EN}$	Enable Input. This input does not function like a traditional enable input (see UV description). Externally pulled up to logic-high state through a resistor normally connected to REG. The $\overline{EN}$ input must be pulled down (for at least 1ms) by the external circuit before a programmable timeout delay has elapsed, otherwise a shutdown occurs. The timeout timer starts counting when the internal MOSFET is turned on. Connect a capacitor between CDLY and GND to program the duration of the timeout delay. Connect $\overline{EN}$ to GND to disable this feature.
C7	$\overline{FAULT}$	Fault Status Output. $\overline{FAULT}$ is an open-drain, active-low output. See the *Fault-Status Output ($\overline{FAULT}$)* section for conditions that make $\overline{FAULT}$ assert low. $\overline{FAULT}$ is disabled during startup.
D1	REG	Internal Regulator Output. Bypass to ground with a 1µF capacitor. Do not power external circuitry using the REG output (except a resistor > 50kΩ connected from REG to $\overline{EN}$). Optional: For V_{CC} values lower than V_{REG_MAX}, REG can be connected to V_{CC} to maximize the voltage on the REG pin (see the *Electrical Characteristics* table).
D2	UV	Active-High Enable Comparator Input. Pulling UV high enables the internal MOSFET to turn on. UV also sets the undervoltage threshold. See the *Setting* the *Undervoltage Threshold* section.
D3	OV	Overvoltage Enable Input. Pull OV high to turn off the internal MOSFET. Connect OV to an external resistive divider to set the overvoltage-disable threshold. See the *Setting the Overvoltage Threshold* section.
D7	PG	Power-Good Output. PG is an open-drain, active-high output. PG pulls low until the internal power MOSFET is fully enhanced.

Functional Diagram



Detailed Description

Enable Logic and Undervoltage/Overvoltage-Lockout Threshold

The MAX15090B/MAX15090C ICs enable the output, as shown in Table 1. The devices are ready to drive the output when the V_{CC} supply rises above the V_{UVLO} threshold. The devices turn on the output when $V_{CC} > V_{UVLO}$, V_{UV} is high ($V_{UV} > 1.23V$) and V_{OV} is low ($V_{OV} < 1.23V$). The devices turn off the output when V_{UV} falls below ($1.23V - V_{UV\_HYS}$) or V_{OV} rises above 1.23V. An external resistive divider from IN to UV, OV, and ground provide the flexibility to set the undervoltage/overvoltage-lockout threshold to any desired level between V_{UVLO} and 18V. See Figure 1 and the *Setting the Undervoltage Threshold* and *Setting the Overvoltage Threshold* sections.

Startup

Once the device output is enabled, the device provides controlled application of power to the load. The voltage at OUT begins to rise at approximately 10V/ms default until the programmed circuit-breaker current level is reached, while the devices actively limit the inrush current at the circuit-breaker setting. An external capacitor connected to the GATE pin allows the user to program the slew rate to a value lower than the default. The inrush current can be programmed by selecting the appropriate value of R_{CB}. During startup, a foldback current limit is active to protect the internal MOSFET to operate within the SOA (Figure 2).

An internal 48ms timer (t_{SU}) starts counting when the devices enter the startup phase. The devices complete the startup phase and enter normal operation mode if the voltage at OUT rises above the precharge threshold (0.9 x V_{IN}) and ($V_{GATE} - V_{OUT}$) > 3V. An open-drain power-good output (PG) goes high-impedance 16ms after the startup successfully completes. Device enters fault mode if start-up does not complete before t_{SU} expires. Startup time is nominally V_{OUT} ramp time plus 6ms, including the time it takes for GATE to get to V_{OUT} +3V.

The thermal-protection circuit is always active and the internal MOSFET immediately turned off when the thermal-shutdown threshold condition is reached.

Table 1. Output Enable Truth Table

POWER SUPPLY	PRECISION ANALOG INPUTS		OUT
V_{CC}	UV	OV	
$V_{CC} > V_{UVLO}$	$V_{UV} > V_{UV\_TH}$	$V_{OV} < V_{OV\_TH}$	On
$V_{CC} < V_{UVLO}$	X	X	Off
X	$V_{UV} < (V_{UV\_TH} - V_{UV\_HYS})$	X	Off
X	X	$V_{OV} > V_{OV\_TH}$	Off

X = Don't care.
V_{UV_TH} and V_{OV_TH} = 1.23V (typ).

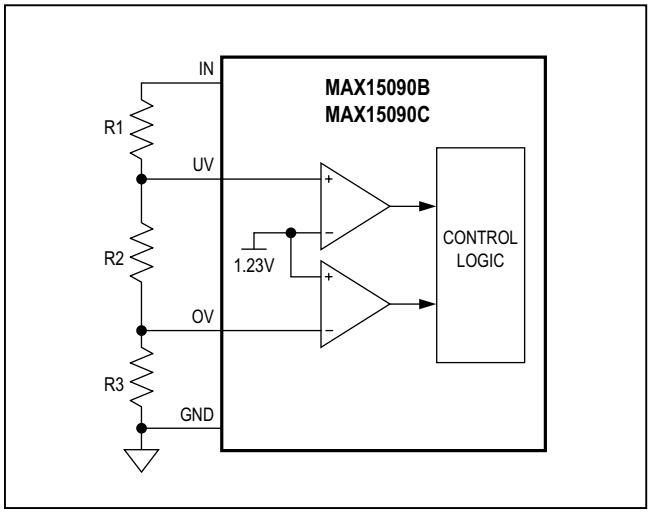


Figure 1. Undervoltage/Overvoltage-Threshold Setting

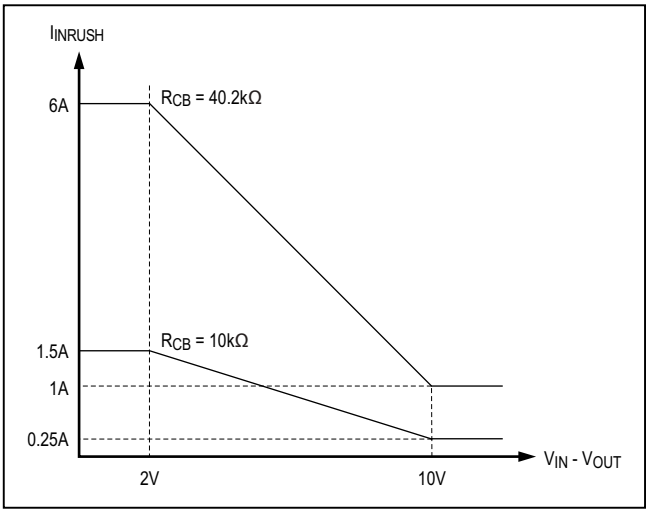


Figure 2. Startup Inrush Current Foldback Characteristics

VariableSpeed/BiLevel Fault Protection

VariableSpeed/BiLevel fault protection incorporates comparators with different thresholds and response times to monitor the load current (see the *Typical Operating Characteristics* section). Protection is provided in normal operation (after the startup period has expired) by discharging the MOSFET gate in response to a fault condition. During a fault condition, the MAX15090C enters autoretry mode, while the MAX15090B latches off (see the *Autoretry and Latchoff Fault Management* section).

Enable Input ($\overline{EN}$)

After a startup phase is successfully completed and the power-good output asserted, the $\overline{EN}$ input has to be pulled low (for at least 1ms) before the t_{DLY} delay elapses. If the $\overline{EN}$ input is not pulled low before the t_{DLY} elapses, then the devices turn off the internal MOSFET immediately and a new cycle is required for entering power-up mode. Connect a capacitor between CDLY and GND to set a 1s/µF duration timeout delay. If this function in is not implemented, connect $\overline{EN}$ to GND for proper operation.

Charge Pump

An integrated charge pump provides the gate-drive voltage for the internal power MOSFET. The charge pump generates the proper gate drive voltage above V_{IN} to fully enhance the internal power MOSFET and guarantee low R_{ON} operation during normal state conditions.

During startup, the internal charge pump drives the GATE of the MOSFET with a fixed 5.7µA current to enhance the internal MOSFET with 10V/ms slew rate (typ). Connect an external capacitor (C_{GATE}) from GATE to GND to reduce the output slew rate during startup. C_{GATE} can be calculated according to the following formula:

$$C_{GATE} = I_{GATE} \times (t_{ON}/V_{OUT})$$

where I_{GATE} is 5.7µA (typ), t_{ON} is the desired output ramp-up time, and V_{OUT} is assumed to start from zero.

The slew rate of the OUT pin during startup can be controlled by I_{GATE}/C_{GATE} under light-load driving conditions, or by the limited inrush current and the external capacitive load, whichever is less.

$$(\Delta V_{OUT}/\Delta t) = I_{LIM}/C_{LOAD}$$

I_{LIM} varies during startup as V_{OUT} ramps up. See the Electrical Characteristics table and Figure 2.

Circuit-Breaker Comparator and Current Limit

The current that passes through the internal power MOSFET is compared to a circuit-breaker threshold. An external resistor between CB and GND sets this threshold according to the following formula:

$$I_{CB} = R_{CB}/3333.3$$

where I_{CB} is load current in amps and R_{CB} (the resistor between CB and GND) is in ohms.

The circuit-breaker comparator is designed so the load current can exceed the threshold for some amount of time before tripping. The time delay varies inversely with the overdrive above the threshold. The greater the overcurrent condition, the faster the response time, allowing the devices to tolerate load transients and noise near the circuit-breaker threshold. The maximum allowed external resistor value is 40.2kΩ, which corresponds to a 12A CB threshold setting. Programming the CB threshold to a value higher than 12A could cause unsafe operating conditions, resulting in damage to the devices.

The devices also feature catastrophic short-circuit protection. During normal operation, if OUT is shorted directly to GND, a fast protection circuit forces the gate of the internal MOSFET to discharge quickly and disconnect the output from the input.

Autoretry and Latchoff Fault Management

During a fault condition, the devices turn off the internal MOSFET, disconnecting the output from the input. The MAX15090C enters autoretry mode and restarts after a $t_{RESTART}$ time delay has elapsed. The MAX15090B latches off and remains off until the UV input is cycled off and on after a $t_{RESTART}$ delay. The delay prevents the latchoff device to restart and operate with an unsafe power-dissipation duty cycle.

Fault-Status Output ($\overline{FAULT}$)

$\overline{FAULT}$ is an open-drain output that asserts low when the following conditions occur: Current limit, overtemperature, IN-to-OUT short at startup (see the *"IN-to-OUT Short-Circuit Protection"* section), and if device does not complete startup before the t_{SU} timer expires (see the *Startup* section). $\overline{FAULT}$ remains low until the next startup cycle. $\overline{FAULT}$ is capable of sinking up to 5mA current when asserted.

Power-Good (PG) Delay

The devices feature an open-drain, power-good output that asserts after a t_{PG} delay, indicating that the OUT voltage has reached (0.9 x V_{IN}) voltage and (V_{GATE} - V_{OUT}) > 3V.

Internal Regulator Output (REG)

The devices include a linear regulator that outputs 3.3V at REG. REG provides power to the internal circuit blocks of the devices and must not be loaded externally (except for a resistor > 50kΩ connected from REG to $\overline{EN}$). REG requires at least a 1µF capacitor to ground for proper operation.

Current Report Output (ISENSE)

The ISENSE pin is the output of an accurate current-sense amplifier and provides a source current that is proportional to the load current flowing into the main switch. The factory-trimmed current ratio is set to 220µA/A. This produces a scaled voltage by connecting a resistor between I_{SENSE} and ground. This voltage signal then goes to an ADC and provides digitized information of the current supplied to the powered system.

Thermal Protection

The devices enter a thermal-shutdown mode in the event of overheating caused by excessive power dissipation or high ambient temperature. When the junction temperature exceeds T_J = +150°C (typ), the internal thermal-protection circuitry turns off the internal power MOSFET. The devices recover from thermal-shutdown mode once the junction temperature drops by 20°C (typ).

IN-to-OUT Short-Circuit Protection

At startup, after all the input conditions are satisfied (UV, OV, V_{UVLO}), the devices immediately check for an IN-to-OUT short-circuit fault. If V_{OUT} is greater than 90% of V_{IN}, the internal MOSFET cannot be turned on so $\overline{FAULT}$ is asserted and the MAX15090C enters autoretry mode in 3.2s, while the MAX15090B latches off.

If V_{OUT} is lower than 90% of V_{IN} but greater than 50% of V_{IN}, the internal MOSFET still cannot be turned on. No fault is asserted and the MOSFET can turn on as soon as V_{OUT} is lower than 50% of V_{IN}.

Applications Information

Setting the Undervoltage Threshold

The devices feature an independent on/off control (UV) for the internal MOSFET. The devices operate with a 2.7V to 18V input voltage range and have a default 2.5V (typ) undervoltage-lockout threshold.

The internal MOSFET remains off as long as V_{CC} < 2.5V or V_{UV} < V_{UV_TH}. The undervoltage-lockout threshold is programmable using a resistive divider from IN to UV, OV, and GND (Figure 1). When V_{CC} is greater than 2.7V and V_{UV} exceeds the 1.23V (typ) threshold, the internal MOSFET turns on and goes into normal operation. Use the following equation to calculate the resistor values for the desired undervoltage threshold:

$$R1 = \left(\frac{V_{IN}}{V_{UV\_TH}} - 1 \right) \times (R2 + R3)$$

where V_{IN} is the desired turn-on voltage for the output and V_{UV_TH} is 1.23V. R1 and (R2 + R3) create a resistive divider from IN to UV. During normal operating conditions, V_{UV} must remain above its 1.23V (typ) threshold. If V_{UV} falls 100mV (V_{UV_HYS}) below the threshold, the internal MOSFET turns off, disconnecting the load from the input.

Setting the Overvoltage Threshold

The devices also feature an independent overvoltage-enable control (OV) for the internal MOSFET.

When V_{OV} exceeds the 1.23V (typ) threshold, the internal MOSFET turns off.

The overvoltage-lockout threshold is programmable using a resistive divider from IN to UV, OV, and GND (Figure 1). Use the following equation to calculate the resistor values for the desired overvoltage threshold:

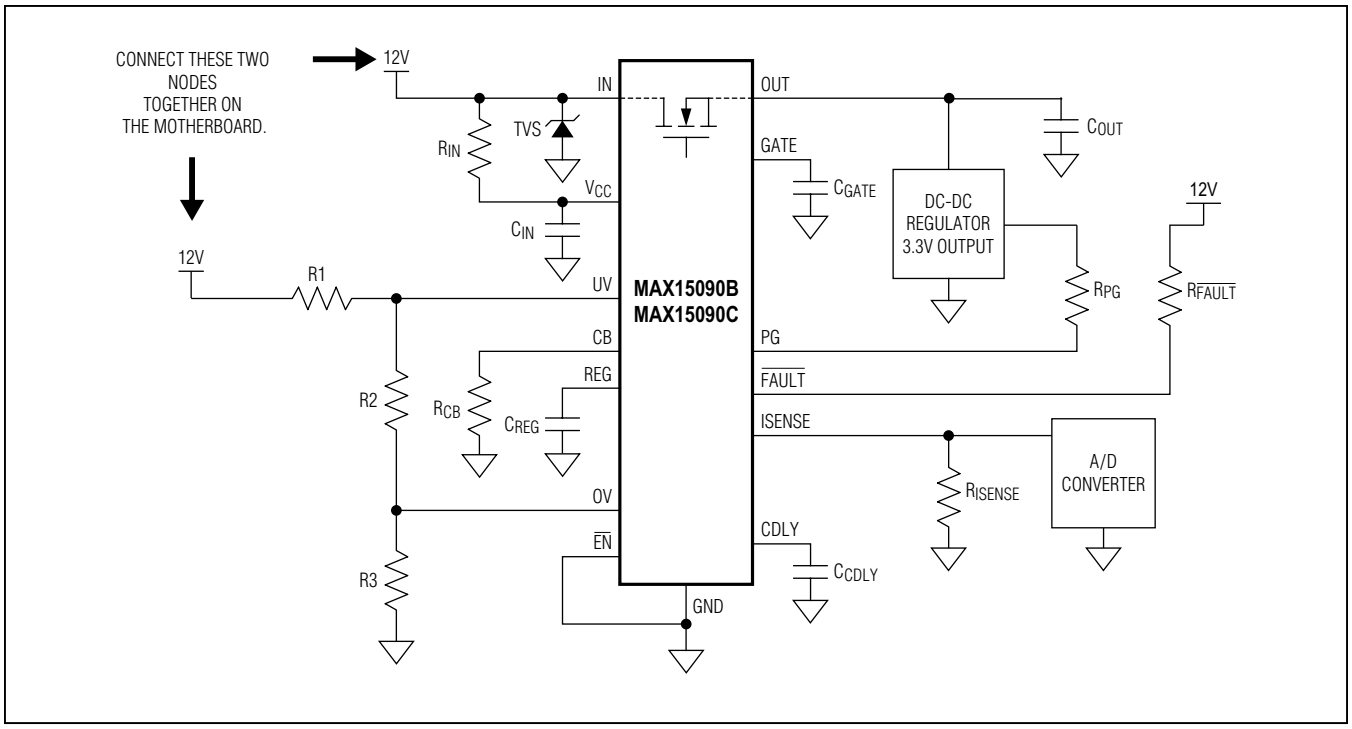
$$(R1 + R2) = \left(\frac{V_{IN}}{V_{OV\_TH}} - 1 \right) \times R3$$

where V_{IN} is the desired turn-off voltage for the output and V_{OV_TH} is 1.23V. R1 and (R2 + R3) create a resistive divider from IN to OV. During normal operating conditions, V_{OV} must remain below its 1.23V (typ) threshold. If V_{OV} rises above the V_{OV_TH} threshold, the internal MOSFET turns off and disconnects the load from the input.

Wafer-Level Packaging (WLP) Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to Application Note 1891: *Wafer-Level Packaging (WLP) and its Applications.*

Recommended Application Circuit for Hot-Swap Applications



Chip Information

PROCESS: BiCMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	FAULT MANAGEMENT
MAX15090BEWI+T	-40°C to +85°C	28 WLP	Latched Off
MAX15090CEWI+T	-40°C to +85°C	28 WLP	Autoretry

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 WLP	W282B3Z+1	21-0577	Refer to Application note 1891

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/15	Initial release	—
1	8/15	Updated *Typical Application Circuit* and *Recommended Application Circuit for Hot-Swap Applications*, *Electrical Characteristics* table, replaced TOCs 8 and 12 in the *Typical Operating Characteristics* section, updated Bumps A7 and D1 in the *Bump Description* table, Startup and *Variable Speed/BiLevel Fault Protection* sections, and deleted Figure 3	1–3, 6, 8, 10, 11, 14

