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MAX14906

Quad-Channel Industrial Digital Output/Digital Input

General Description

The MAX14906 is an IEC 61131-2 compliant, high-speed, four-channel industrial digital output, digital input device that can be configured on a per-channel basis as a high-side (HS) switch, push-pull (PP) driver, or a Type 1 and 3, or Type 2 digital input. The MAX14906 is specified for operation with a supply voltage up to 40V and is tolerant to 65V.

The high-side switch current limiting is settable from 130mA to 1.2A with the option of 2x load inrush current. The high-side driver on-resistance is 120mΩ (typ) at 25°C ambient temperature. Optional push-pull operation allows high speed driving of cables and fast discharge of load capacitance. For digital input operation, current sinks for 2.3mA (Type 1 and 3) or 7mA (Type 2) are provided.

The SPI interface has a built-in chip addressing decoder, allowing communication with multiple MAX14906 devices utilizing a shared SPI with a common chip select ($\overline{CS}$). The SPI interface provides flexibility for global and per-channel configuration and diagnostics, including supply overvoltage and undervoltage detection, wire-break or open-wire detection, thermal overload and current limit reporting, and more. For high-speed operation, the digital input and output states can be monitored and changed directly using pins for increased system speed and throughput.

Open-wire detection monitors open-wire/open-load conditions with switches in the off state. LED drivers provide indication of per-channel fault, status, and supply undervoltage conditions. Internal active clamps allow for fast turn-off of inductive loads. Integrated line-to-ground and line-to-line surge protection only requires a TVS on V_{DD}.

The MAX14906 is available in a compact 48-pin 7mm x 7mm QFN package.

Applications

- Industrial Digital Output and Input Module
- Configurable Digital Input/Output
- Motor Control
- PLC Systems
- Distributed Control Systems (DCS)

Benefits and Features

- Per-Channel Configurability Enables Wide Range of Applications
  - Digital Output: High-Side (HS) Switch or Push-Pull (PP) Driver
  - Digital Input: Software Selectable Type 1 and 3, or Type 2
  - Current Limit Settable from 130mA to 1.2A
  - Serial (SPI) or Direct Operation Using Pins
  - Independent Channel Powering
- Fault Tolerant with Built-In Diagnostics
  - Per-Channel Diagnostics
  - Integrated Voltage Supply Monitoring and Short-to-V_{DD} Detection
  - Open-Wire/Open-Load Detection
  - Thermal Shutdown Protection
  - Watchdog Timer
  - 5-Bit CRC Code Generation and Checking for SPI Error Detection
- High Integration Reduces BOM Count and PCB Space
  - Integrated LDO Compatible with 5V Logic Devices
  - Internal Active Clamps for Fast Inductive Load Turn-Off
  - 0.6µs (typ) DO and 1µs (typ) DI Propagation Delays
  - Addressable SPI
  - 7mm x 7mm TQFN Package
- Reduced Power and Heat Dissipation
  - Low R_{DSON} for High-Side Switches, 120mΩ (typ)
  - Accurate Output Current Limiting
  - Accurate Input Current Sinks, Type 1 and 3, or Type 2
- Robust Design
  - 10V to 40V Operating Supply Range, 65V Tolerant
  - SafeDemag™ Allows Fast Turn-Off of Unlimited Inductance
  - ±16kV Air-Gap ESD and ±8kV Contact ESD
  - ±1kV Surge Tolerant Using TVS Protection on V_{DD} to GND
  - -40°C to +125°C Operating Temperature

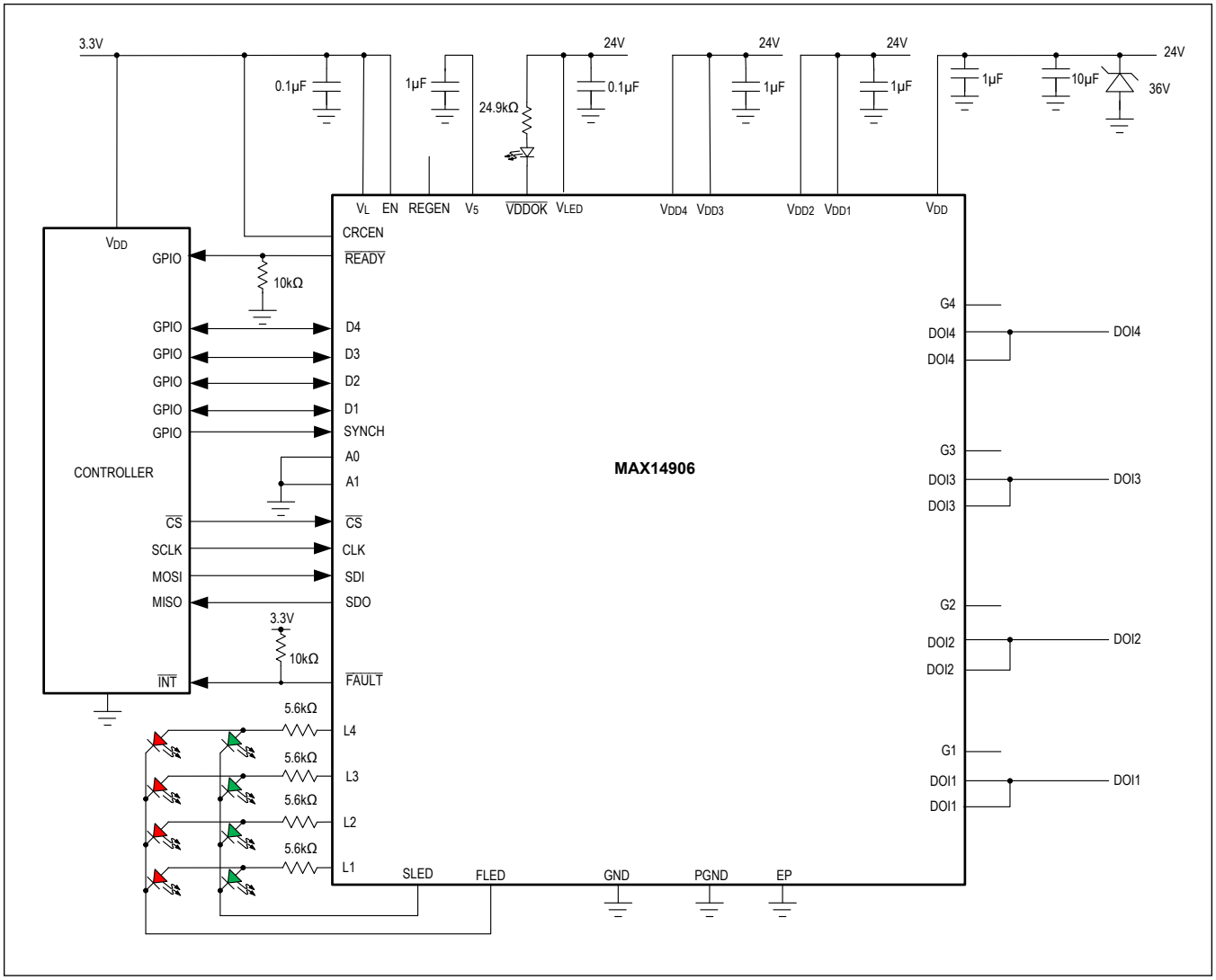
***Ordering Information* appears at end of datasheet.**

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19-100736; Rev 1; 2/20

maxim integrated™

Quad Industrial Digital Output, Digital Input



Absolute Maximum Ratings

V_{DD}, V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, V_{LED} ..... -0.3V to +65V
DOI1, DOI2, DOI3, DOI4
  $V_{DD} < V_{DD_OVTH}$ ..... (V_{DD} - 49V) to (V_{DD} + 0.3V)
  $V_{DD} > V_{DD_OVTH}$ ..... -1V to (V_{DD} + 0.3V)
V_5, V_L ..... -0.3V to +6V
SDI, CLK, $\overline{CS}$, EN, A0, A1, SYNCH, REGEN ..... -0.3V to +6V
$\overline{FAULT}$ ..... -0.3V to +6V
D1, D2, D3, D4, SDO, $\overline{READY}$ ..... -0.3V to (V_L + 0.3V)
SLED, FLED, L1, L2, L3, L4, $\overline{VDDOK}$ ..... -0.3V to (V_{LED} + 0.3V)
G1, G2, G3, G4 ..... -0.3V to min(40V, V_{DD} + 0.3V)

Continuous Current
  DOI_ Load Current ..... Internally Limited
  All Pins other than DOI_ ..... -100mA to +100mA
Inductive Demagnetization Energy ($I_{DOI_}$ < 0.6A) ..... Unlimited
Continuous Power Dissipation (T_A = +70ºC)
  TQFN 48 (derate 40mW/°C above 70°C) 3200mW
Junction Temperature ..... Internally Limited
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Note 1: All voltages relative to GND.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

48 TQFN

Package Code	T4877+6C
Outline Number	21-0144
Land Pattern Number	90-0130
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	25°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = +10V to +40V, V_{LED} = +3.0V to +40V, V_5 = +4.5V to +5.5V, V_L = +2.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC, V_{DD} = $V_{DD_}$ = V_{LED} = +24V, V_L = 3.3V, REGEN = Open, and V_5 = 5V.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} AND $V_{DD_}$ SUPPLY VOLTAGES						
Supply Voltage V_{DD} and $V_{DD_}$	V_{DD}	Normal Operating Conditions	10		40	V
		Overvoltage Lockout Tolerance	V_{DD_OVTH}		65	
V_{DD} Supply Current	I_{DD_ON}	All channels in HS mode, V_{DD} = 40V, REGEN = GND, DOI_ not loaded, no load on V_5		2.5	4.5	mA
		All channels in PP mode, V_{DD} = 40V, REGEN = GND, 10kHz switching, no load on DOI_, no load on V_5		4	7	
		All channels in DI mode, REGEN = GND		2.5	4.5	
V_{DD} Supply Current Increase	$I_{DD_ON_IN}$	All G_ turn on		0.5	1.4	mA

Electrical Characteristics (continued)

(V_{DD} = V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = +10V to +40V, V_{LED} = +3.0V to +40V, V_5 = +4.5V to +5.5V, V_L = +2.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC, V_{DD} = $V_{DD_}$ = V_{LED} = +24V, V_L = 3.3V, REGEN = Open, and V_5 = 5V.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overvoltage Lockout Threshold	V_{DD_OVTH}	V_{DD} rising	41.5	43.5	45	V
Overvoltage Lockout Hysteresis	V_{DD_OVHYST}			1		V
Undervoltage Lockout Threshold	$V_{DD_UVLO_R}$	V_{DD} rising			9.6	V
	$V_{DD_UVLO_F}$	V_{DD} falling	7.9			
Undervoltage Lockout Hysteresis	V_{DD_UVHYST}			1		V
Undervoltage V_{DD} Warning Threshold	$V_{DD_WARN_R}$	V_{DD} rising			14	V
	$V_{DD_WARN_F}$	V_{DD} falling	12			
Undervoltage V_{DD} Warning Hysteresis	$V_{DD_WARN_H}$			1		V
Undervoltage V_{DD} Good Threshold	$V_{DD_GOOD_R}$	V_{DD} rising			17	V
	$V_{DD_GOOD_F}$	V_{DD} falling	15			
Undervoltage V_{DD} Good Hysteresis	$V_{DD_GOOD_H}$			1		V
LOGIC INTERFACE SUPPLY (V_L)						
V_L Supply Voltage	V_L		2.5		5.5	V
V_L Supply Current	I_{VL}	All logic inputs high or low, logic outputs unloaded		18	40	µA
V_L POR Threshold	V_{L_POR}	V_L voltage falling	1	1.27	1.55	V
5V SUPPLY (V_5)						
V_5 Supply Voltage	V_5	REGEN = GND	4.75	5.0	5.25	V
V_5 Supply Current in HS Mode	$I_{V5_ON_HS}$	All channels in HS mode, REGEN = GND, all DOI_ switches ON and unloaded		1	1.8	mA
V_5 Supply Current in Active-Clamp PP Mode	$I_{V5_ON_PP_AC}$	All channels in active clamp PP mode, REGEN = GND, all DOI_ switches ON and unloaded		1.1	2	mA
V_5 Supply Current in Simple PP Mode	$I_{V5_ON_PP}$	All channels in simple PP mode, REGEN = GND, all DOI_ switches ON and unloaded		1.1	2	mA
V_5 Supply Current in DI Mode	$I_{V5_ON_DI}$	All channels in DI mode, REGEN = GND, all DOI_ at 30V		1.1	2	mA
V_5 Undervoltage Lockout Threshold	V_{5_UVLO}	V_5 rising	3.8		4.4	V
V_5 Undervoltage Lockout Hysteresis	V_{5UVLO_HYS}			0.3		V
5V LINEAR REGULATOR (V_5, REGEN)						
V_5 Regulator Output Voltage	V_5	REGEN = open, 0mA to 20mA external load current	4.75	5.0	5.25	V

Electrical Characteristics (continued)

(V_{DD} = V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = +10V to +40V, V_{LED} = +3.0V to +40V, V_5 = +4.5V to +5.5V, V_L = +2.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC, V_{DD} = $V_{DD_}$ = V_{LED} = +24V, V_L = 3.3V, REGEN = Open, and V_5 = 5V.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_5 Regulator Current Limit	I_{CL_V5}	REGEN = open	25			mA
REGEN Pullup Current	I_{PU_REGEN}	REGEN = GND	5		30	µA
REGEN Threshold	V_{TH_REGEN}	REGEN rising	1	1.6	2.5	V
DRIVER OUTPUTS (DOI_)						
High-Side On-Resistance	R_{ON_HS}	HS or PP modes, $I_{DOI_}$ = 500mA		120	240	mΩ
Low-Side On-Resistance	R_{ON_LS}	DoMode_ = 11 (Simple PP mode), $I_{DOI_}$ = 100mA		1	3	Ω
Low-Side Output Low Voltage	V_{OL_LS}	Active clamp PP mode, $I_{DOI_}$ = 100mA			1.2	V
		Simple PP mode, $I_{DOI_}$ = 100mA			0.4	
DOI_ Clamp Voltage	V_{CL}	Relative to $V_{DD_}$, $I_{DOI_}$ = 10mA, $V_{DD_}$ < V_{DD_OVTH}	-63	-55	-49	V
		Relative to GND, $I_{DOI_}$ = 10mA, V_{DD_OVTH} < $V_{DD_}$ < 60V	-6	-4.5	-3	
DOI_ Leakage	I_{LK40_DOI}	$V_{DD_}$ = 40V, HS mode, DOI_ = off, 0V < DOI_ < $V_{DD_}$	-60		+60	µA
	I_{LKDOI_ANA}	$V_{DD_}$ = 40V, low-leakage high-impedance mode, 0V < DOI_ < $V_{DD_}$	-2.4		+2.4	µA
OFF STATE DIAGNOSTICS (DOI_)						
Diagnostic Test Current	I_{DIAG1}	OWOffEn_ = 1, $V_{DOI_}$ < 5V or $V_{DOI_}$ > 9V, OWOffCs = 00, Both Open-Wire and Short-to-V_{DD}	20	60	120	µA
	I_{DIAG2}	OWOffEn_ = 1, $V_{DOI_}$ < 5V or $V_{DOI_}$ > 9V, OWOffCs = 01, Both Open-Wire and Short-to-V_{DD}	60	100	180	
	I_{DIAG3}	OWOffEn_ = 1, $V_{DOI_}$ < 5V or $V_{DOI_}$ > 9V, OWOffCs = 10, Both Open-Wire and Short-to-V_{DD}	200	300	440	
	I_{DIAG4}	OWOffEn_ = 1, $V_{DOI_}$ < 5V or $V_{DOI_}$ > 9V, OWOffCs = 11, Both Open-Wire and Short-to-V_{DD}	460	600	760	
DOI_ Open Voltage, OWOff_	V_{OUT_OFF}	OWOffEn_ = 1, $I_{DOI_}$ = 0mA	5.8	6.7	7.6	V
Open-Wire Detection Threshold, OWOff_	V_{TH_OWOFF}	OWOffEn_ = 1	5		5.8	V
Short-to-V_{DD} Detection Threshold	V_{TH_SHVDD1}	ShVddEn_ = 1, ShtVddThr = 00	8.2	9	10	V
	V_{TH_SHVDD2}	ShVddEn_ = 1, ShtVddThr = 01	9.1	10	10.9	
	V_{TH_SHVDD3}	ShVddEn_ = 1, ShtVddThr = 10	11	12	13	
	V_{TH_SHVDD4}	ShVddEn_ = 1, ShtVddThr = 11	13	14	15	

Electrical Characteristics (continued)

(V_{DD} = V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = +10V to +40V, V_{LED} = +3.0V to +40V, V_5 = +4.5V to +5.5V, V_L = +2.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC, V_{DD} = $V_{DD_}$ = V_{LED} = +24V, V_L = 3.3V, REGEN = Open, and V_5 = 5V.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT LIMITING (DOI_)						
HS Current Limit	I_{CLIM}	DO HS or PP modes, CL_ = 01, OVL_ = X, t > t_{INRUSH}, see Table 2	130	175	220	mA
		DO HS or PP modes, CL_ = 01, OVL_ = 1, t < t_{INRUSH}, see Table 2	300	350	400	
		DO HS or PP modes, CL_ = 10, OVL_ = X, t > t_{INRUSH}, see Table 2	300	350	400	
		DO HS or PP modes, CL_ = 10, OVL_ = 1, t < t_{INRUSH}, see Table 2	600	700	800	
		DO HS or PP modes, CL_ = 00, OVL_ = X, t > t_{INRUSH}, see Table 2	600	700	800	
		DO HS or PP modes, CL_ = 00, OVL_ = 1, t < t_{INRUSH}, see Table 2	1.2	1.4	1.6	A
		DO HS or PP modes, CL_ = 11 OVL_ = X, t > t_{INRUSH}, see Table 2	1.2	1.4	1.6	
		DO HS or PP modes, CL_ = 11 OVL_ = 1, t < t_{INRUSH}, see Table 2	2.4	2.8	3.2	
LS Current Limit	I_{CLIM_LS}	DO PP modes	150	200	280	mA
DIGITAL INPUT (DOI_)						
Threshold Voltage	$V_{TH_DOI_DI}$	DI mode, DOI_ rising	6.7		8.0	V
Hysteresis Voltage	$V_{HYS_DOI_DI}$	DI mode		1.2		V
Current Sink	$I_{DOI_DI_L}$	DI mode, Typ2Di = 0, 0V < $V_{DOI_}$ < 5V	0		2.6	mA
	$I_{DOI_DI_H}$	DI mode, Typ2Di = 0, 8V < $V_{DOI_}$ < 40V, $V_{DOI_}$ < $V_{DD_}$	2.0	2.3	2.6	
	$I_{DOI_DI_L}$	DI mode, Typ2Di = 1, 0V < $V_{DOI_}$ < 5V	0		7.5	
	$I_{DOI_DI_H}$	DI mode, Typ2Di = 1, 8V < $V_{DOI_}$ < 40V, $V_{DOI_}$ < $V_{DD_}$	6.0	7.0	7.7	
LOGIC INTERFACE I/O						
Input Voltage High	V_{IH}		0.7 x V_L			V
Input Voltage Low	V_{IL}				0.3 x V_L	V
Input Threshold Hysteresis	V_{IHYS}			0.11 x V_L		V
Input Pull-Down Resistor	R_{IN_PD}	EN pin	110	200	260	kΩ
Input Leakage	I_{LEAK}	GND < V_{IN} < V_L	-1		+1	µA
Output Logic High	V_{OH}	I_{LOAD} = -5mA	V_L - 0.33			V
Output Logic Low	V_{OL}	I_{LOAD} = +5mA			0.33	V
Output Leakage D_	I_{LEAK_DOI}	DO modes	-1		+1	µA
Output Leakage SDO	I_{LEAK_SDO}	$\overline{CS}$ is high	-1		+1	µA

Electrical Characteristics (continued)

(V_{DD} = V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = +10V to +40V, V_{LED} = +3.0V to +40V, V_5 = +4.5V to +5.5V, V_L = +2.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC, V_{DD} = $V_{DD_}$ = V_{LED} = +24V, V_L = 3.3V, REGEN = Open, and V_5 = 5V.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GATE DRIVER (G_)						
V_{DD} Threshold for G_ Turn-on	V_{DDTH_G}	G_ driver clamp voltage to GND	43	48	59	V
G_ On Voltage	V_{ON_G}	DO modes, DOI_ ≤ $V_{DD_}$	$V_{DD_}$ - 14		$V_{DD_}$ - 10	V
G_ Off Switch Resistance	R_{ON_G}	DI modes		50		Ω
OPEN-DRAIN OUTPUTS ($\overline{FAULT}$, $\overline{VDDOK}$, $\overline{READY}$)						
Output Logic Low ($\overline{FAULT}$, $\overline{VDDOK}$)	V_{ODL}	I_{LOAD} = +5mA			0.33	V
Output Logic High ($\overline{READY}$)	V_{ODH}	I_{LOAD} = -5mA	V_L - 0.33			V
Leakage ($\overline{FAULT}$)	I_{ODL}	Open-drain output off, V_{OD} = 5.5V	-1		+1	µA
Leakage ($\overline{VDDOK}$)	I_{ODL}	Open-drain output off, V_{OD} = 40V	-5		+5	µA
Leakage ($\overline{READY}$)	I_{ODL}	Open-drain output off, V_{OD} = GND	-1		+1	µA
LED DRIVERS (L_, FLED, SLED)						
LED Supply Voltage	V_{LED}		3.0		V_{DD}	V
LED Supply Current	I_{LED}	V_{LED} = 40V, SLED = Off, FLED = Off			1	µA
L_ Voltage High	V_{OH_L}	L_ = On, $I_{L_}$ = 5mA	V_{LED} - 0.33			V
L_ Off Leakage Current	I_{LEAK_L}	L_ = Off, $V_{L_}$ = 0V			5	µA
SLED Output Voltage Low	V_{OL_SLED}	SLED = On, I_{SLED} = 5mA			0.33	V
SLED Off Leakage Current	I_{LEAK_SLED}	SLED = Off, V_{SLED} = V_{LED}			5	µA
FLED Output Voltage Low	V_{OL_FLED}	FLED = On, I_{FLED} = 5mA			0.33	V
FLED Off Leakage Current	I_{LEAK_FLED}	FLED = Off, V_{FLED} = V_{LED}			5	µA
DO MODES PROPAGATION DELAY (D_ or SYNCH to DOI_)						
DOI Output Propagation Delay Low-to-High	t_{PD_LH}	Delay from D_ (or SYNCH) to DOI_ rising by 0.5V, HS or PP modes		0.4	1.5	µs
DOI Output Propagation Delay High-to-Low	t_{PD_HL}	Delay between D_ switching low (or SYNCH high) to DOI_ falling by 0.5V, $V_{DD_}$ = 24V, R_L = 10kΩ, C_L = 0.1nF, HS or $\overline{PP}$ modes		0.6	1.5	µs
DOI Output Rise Time	t_R	HS or PP modes, 20% to 80% $V_{DD_}$, $V_{DD_}$ = 24V, R_L = 10kΩ, C_L = 0.1nF		0.6	1.5	µs

Electrical Characteristics (continued)

(V_{DD} = V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = +10V to +40V, V_{LED} = +3.0V to +40V, V_5 = +4.5V to +5.5V, V_L = +2.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC, V_{DD} = $V_{DD_}$ = V_{LED} = +24V, V_L = 3.3V, REGEN = Open, and V_5 = 5V.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DOI Output Fall Time	t_F	HS modes, 80% to 20% $V_{DD_}$, $V_{DD_}$ = 24V, R_L = 10kΩ, C_L = 0.1nF		1		µs
		PP modes, 80% to 20% $V_{DD_}$, $V_{DD_}$ = 24V, R_L = 10kΩ, C_L = 0.1nF		0.9	2	
DI MODES PROPAGATION DELAY (DOI_ to D_)						
Propagation Delay High-to-Low	$t_{PD_HL_DI}$	DI modes, SYNCH = high, delay from DOI_ falling to 5V to D_ low		0.9	1.8	µs
Propagation Delay Low-to-High	$t_{PD_LH_DI}$	DI modes, SYNCH = high, delay from DOI_ rising to 8V to D_ high		1.1	2	µs
SPI TIMING CHARACTERISTICS (Figure 1)						
CLK Clock Period	t_{CLK}		100			ns
CLK Pulse Width High	t_{CH}		40			ns
CLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to CLK Rise Time	t_{CSS}		40			ns
SDI Hold Time	t_{DH}		10			ns
SDI Setup Time	t_{DS}		10			ns
SDO Propagation Delay	t_{DO}	C_L = 10pF, CLK falling edge to SDO stable			30	ns
SDO Rise and Fall Times	t_{FT}	C_L = 10pF		1		ns
$\overline{CS}$ Hold Time	t_{CSH}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSPW}		40			ns
WATCHDOG TIMING CHARACTERISTICS						
Watchdog Timeout	t_{WD}	WDTo = 01		200		ms
		WDTo = 10		600		
		WDTo = 11		1200		
Watchdog Timeout Accuracy	t_{WD_ACC}	SynchWDEn = 1, see *Config2* register for watchdog timeout	-30		+30	%
LED MATRIX TIMING CHARACTERISTICS						
LED Driver Scan Rate	f_{LED}	Update rate for each LED		1		kHz
THERMAL PROTECTION						
Driver Thermal Shutdown Temperature	T_{JSHDN}	Junction temperature rising		170		°C
Driver Thermal Shutdown Hysteresis	T_{JSHDN_HYST}			15		°C
Chip Thermal Shutdown	T_{CSHDN}	Temperature rising		150		°C
Chip Thermal Shutdown Hysteresis	T_{CSHDN_HYST}			10		°C
LDO Thermal Shutdown	T_{LDSHDN}			165		ºC

Electrical Characteristics (continued)

(V_{DD} = V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = +10V to +40V, V_{LED} = +3.0V to +40V, V_5 = +4.5V to +5.5V, V_L = +2.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25ºC, V_{DD} = $V_{DD_}$ = V_{LED} = +24V, V_L = 3.3V, REGEN = Open, and V_5 = 5V.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EMC PROTECTION						
ESD	V_{ESD}	DOI_ pin, IEC 61000-4-2, Contact Discharge, add a 470pF capacitor on each DOI_ to GND (Note 3)		±8		kV
		DOI_ pin, IEC 61000-4-2 Air-Gap Discharge (Note 3)		±16		
		All pins, Human Body Model		±2		
Surge	V_{SURGE}	DOI_ to PGND or Earth GND, IEC 61000-4-5 (42Ω/0.5µF) (Note 4)		±1		kV

Note 2: All units are production tested at T_A = +25ºC. Specifications over temperature are guaranteed by design.

Note 3: Bypass V_{DD} and $V_{DD_}$ pins to GND with 1µF capacitor as close as possible to the device for high ESD protection. If an external transistor is used on $V_{DD_}$, place the FET as close to $V_{DD_}$ as possible with 1µF capacitor on the other side of the FET to PGND.

Note 4: At typical application value of V_{DD} = 24V with a TVS protection on V_{DD} to GND.

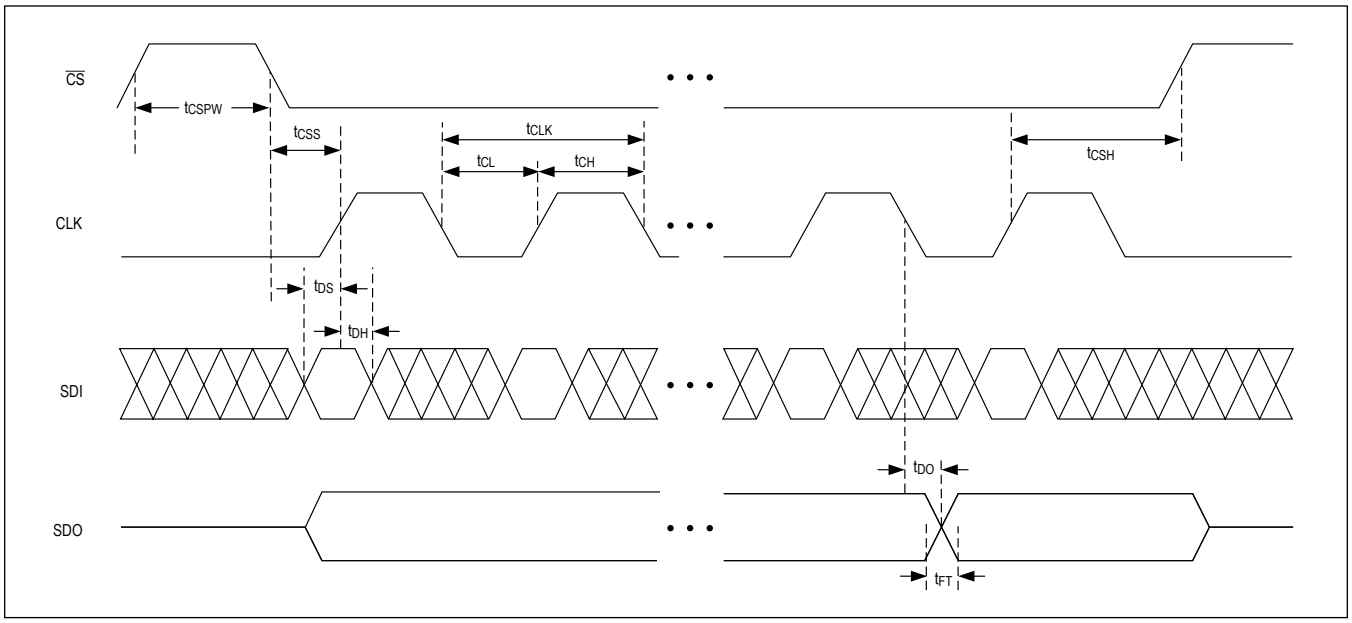
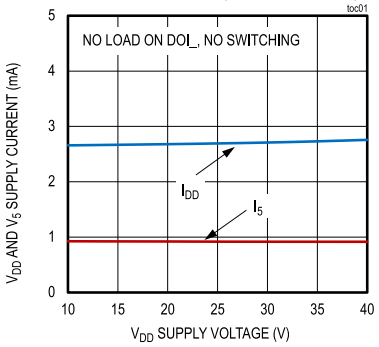


Figure 1. SPI Timing Diagram

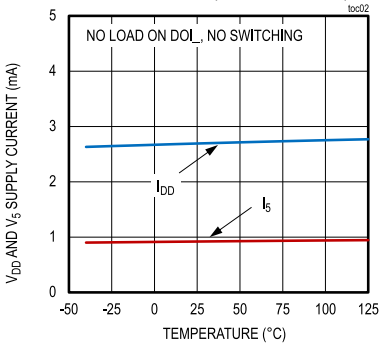
Typical Operating Characteristics

(V_{DD} = $V_{DD_}$ = V_{LED} = +24V, V_L = +5V, REGEN = GND, V_5 = +5V, no load on V_5, T_A = +25ºC, unless otherwise noted.)

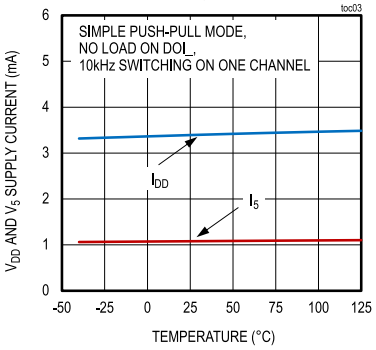
V_{DD} AND V_5 SUPPLY CURRENT vs. SUPPLY VOLTAGE (HIGH-SIDE MODE)



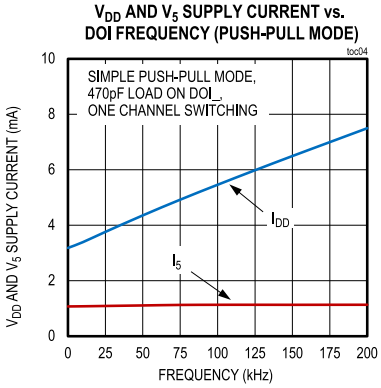
V_{DD} AND V_5 SUPPLY CURRENT vs. TEMPERATURE (HIGH-SIDE MODE)



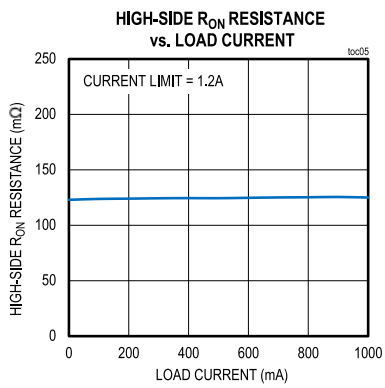
V_{DD} AND V_5 SUPPLY CURRENT vs. TEMPERATURE (PUSH-PULL MODE)



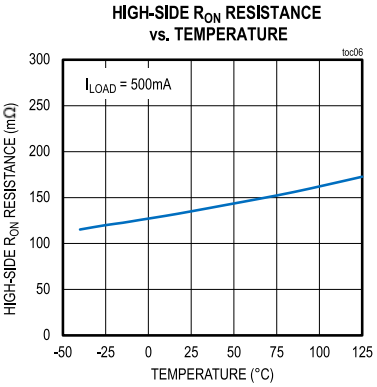
V_{DD} AND V_5 SUPPLY CURRENT vs. DOI FREQUENCY (PUSH-PULL MODE)



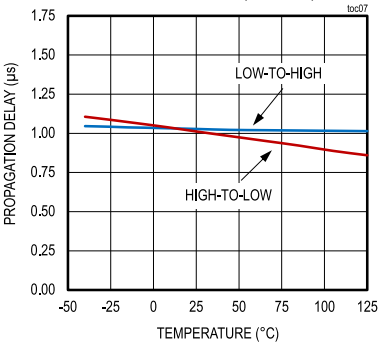
HIGH-SIDE R_{ON} RESISTANCE vs. LOAD CURRENT



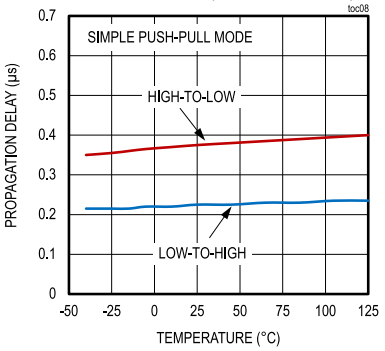
HIGH-SIDE R_{ON} RESISTANCE vs. TEMPERATURE



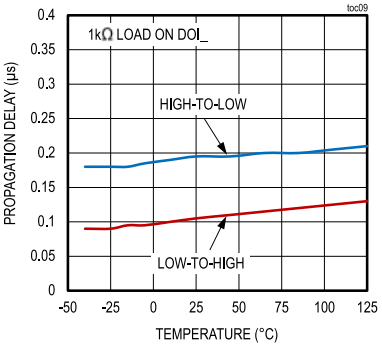
PROPAGATION DELAY vs. TEMPERATURE (DI MODE)



PROPAGATION DELAY vs. TEMPERATURE (PUSH-PULL MODE)



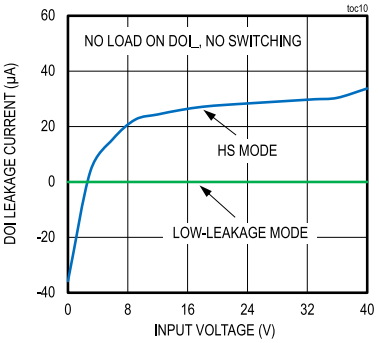
PROPAGATION DELAY vs. TEMPERATURE (HIGH-SIDE MODE)



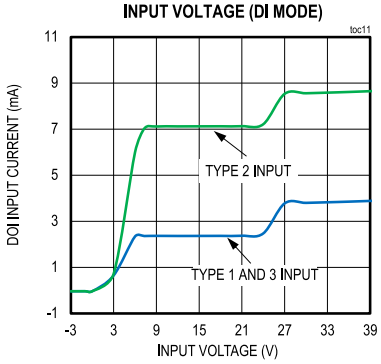
Typical Operating Characteristics (continued)

(V_{DD} = $V_{DD_}$ = V_{LED} = +24V, V_L = +5V, REGEN = GND, V_5 = +5V, no load on V_5, T_A = +25ºC, unless otherwise noted.)

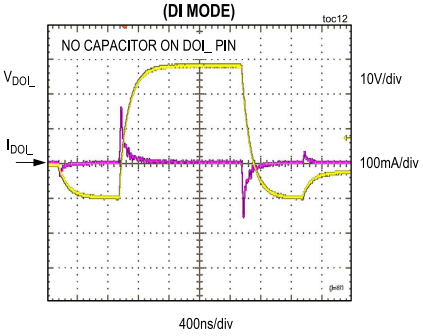
DOI LEAKAGE CURRENT vs. DOI VOLTAGE



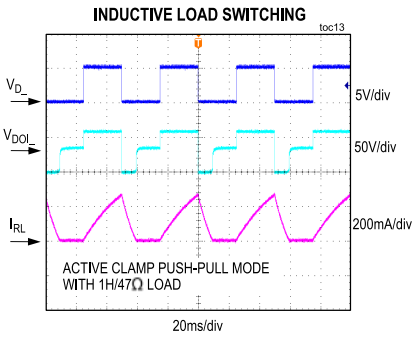
DOI INPUT CURRENT vs. INPUT VOLTAGE (DI MODE)



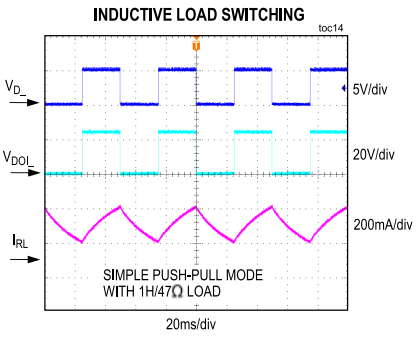
DOI INPUT CURRENT vs. TIME (DI MODE)



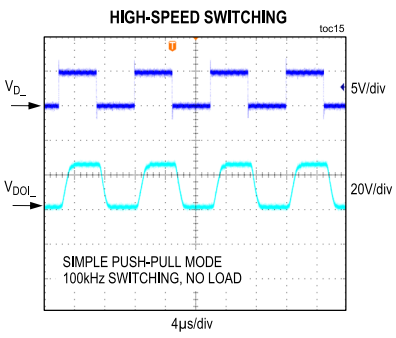
INDUCTIVE LOAD SWITCHING



INDUCTIVE LOAD SWITCHING

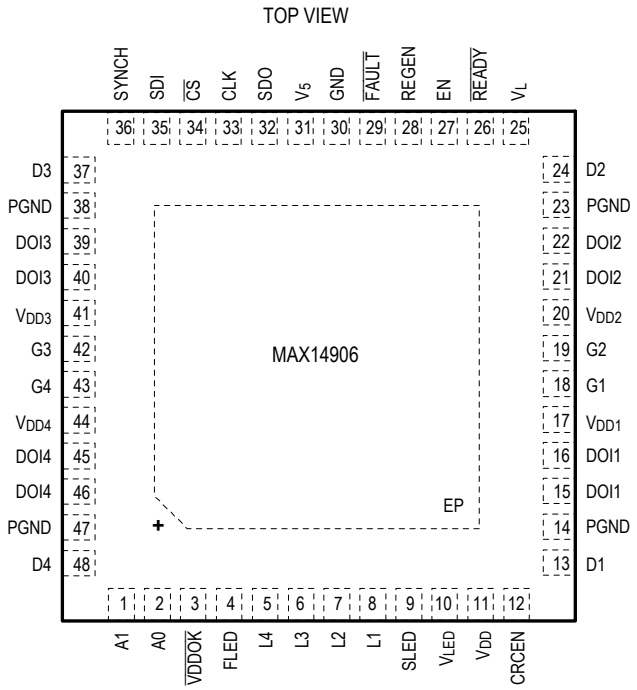


HIGH-SPEED SWITCHING



Pin Configuration

MAX14906



TQFN
7mm x 7mm

Pin Description

PIN	NAME	FUNCTION
POWER SUPPLY		
11, 17, 20, 41, 44	V_{DD}, V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}	Supply Voltage (Nominally 24V). If using a common $V_{DD_}$ supply for all channels, connect all $V_{DD_}$ together. $V_{DD_}$ can also be independently supplied. Bypass V_{DD} to GND using a 1µF capacitor. Bypass the $V_{DD_}$ supplies on the same package side to GND using a shared 1µF capacitor. In order to allow DOI_ to go higher than V_{DD}, an optional pMOS transistor can be used on $V_{DD_}$ supply. In this case connect a 1µF capacitor between its drain and PGND.
30	GND	Logic/Analog Ground
14, 23, 38, 47	PGND	Power Ground. Connect all PGND pins together to GND
31	V_5	Analog Supply Voltage/LDO Output. When REGEN is unconnected, the LDO is enabled and V_5 is a 5V supply output. If REGEN = GND, an external 5V supply has to be connected to V_5. Bypass V_5 to GND using a 1µF ceramic capacitor.
28	REGEN	V_5 Regulator Enable Input. Leave REGEN unconnected for enabling/using the internal 5V regulator. Connect REGEN to GND to disable the internal regulator for powering V_5 from an external regulator.
25	V_L	Logic Reference Input. V_L defines the levels on all I/O logic interface pins. Bypass V_L to GND using a 0.1µF ceramic capacitor.
—	EP	Exposed Pad. Connect the exposed pad to GND.

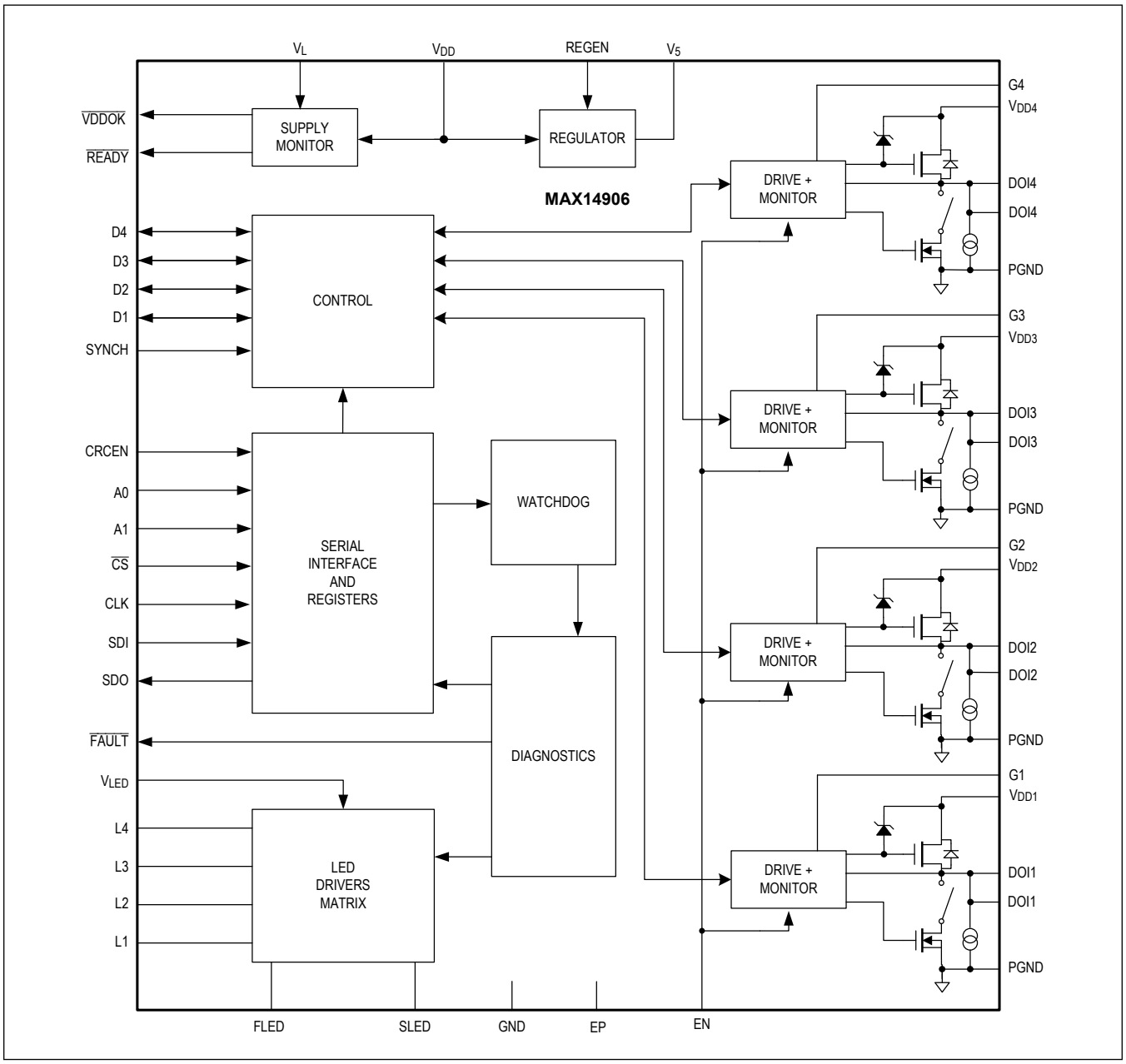
Pin Description (continued)

PIN	NAME	FUNCTION
24V DIGITAL OUTPUT/INPUT		
15, 16	DOI1	Channel 1: High-Side/Push-Pull Output or Digital Input
21, 22	DOI2	Channel 2: High-Side/Push-Pull Output or Digital Input
39, 40	DOI3	Channel 3: High-Side/Push-Pull Output or Digital Input
45, 46	DOI4	Channel 4: High-Side/Push-Pull Output or Digital Input
LOGIC INTERFACE		
13	D1	Logic I/O Pin. When channel 1 is in digital output mode, the D1 input switches the DOI1 output when SYNCH is high. When channel 1 is in digital input mode, the D1 output represents the logic state of the DOI1 input when SYNCH is high.
24	D2	Logic I/O Pin. When channel 2 is in digital output mode, the D2 input switches the DOI2 output when SYNCH is high. When channel 2 is in digital input mode, the D2 output represents the logic state of the DOI2 input when SYNCH is high.
37	D3	Logic I/O Pin. When channel 3 is in digital output mode, the D3 input switches the DOI3 output when SYNCH is high. When channel 3 is in digital input mode, the D3 output represents the logic state of the DOI3 input when SYNCH is high.
48	D4	Logic I/O Pin. When channel 4 is in digital output mode, the D4 input switches the DOI4 output when SYNCH is high. When channel 4 is in digital input mode, the D4 output represents the logic state of the DOI4 input when SYNCH is high.
36	SYNCH	SYNCH Control Input. When DOI_ are configured as digital outputs, they are updated simultaneously on the rising SYNCH edge, as determined by the contents of the SetOUT register or the D_ input pins. The DOI_ output states do not change when SYNCH is held low. When SYNCH is high, the DOI_ output states change immediately when a new value is written into the SetOUT register or the associated D_ input pin. All DOI_ logic levels (both in DO and DI modes) are read and latched on the falling SYNCH edge. The results are stored in the DoiLevel register and the D_ output pins if the DOI_ channels are configured in DI mode.
27	EN	DOI Enable Pin. Drive the EN pin high to enable the DOI_ outputs. Drive EN low to disable/three-state all DOI_ outputs.
12	CRCEN	CRC Enable Pin. Drive the CRCEN pin high to enable CRC on the SPI interface. Drive CRCEN low if CRC is not used.
3	$\overline{\text{VDDOK}}$	Active-Low Open-Drain Logic Output. $\overline{\text{VDDOK}}$ is asserted low when the V_{DD} supply voltage is OK. Connect a pullup resistor to a voltage level between V_L and V_{LED}.
29	$\overline{\text{FAULT}}$	Active-Low Open-Drain Fault Output. $\overline{\text{FAULT}}$ is asserted low when a diagnostic fault is detected on any of the channels. Connect a pullup resistor to V_5 or V_L.
26	$\overline{\text{READY}}$	High-Side Open-Drain Output. $\overline{\text{READY}}$ is passive low when the internal logic supply is higher than the UVLO threshold, indicating that the registers have adequate supply voltage. When the internal register supply falls below the UVLO threshold, the register contents are lost and $\overline{\text{READY}}$ transitions high. Connect a pulldown resistor from $\overline{\text{READY}}$ to GND.
35	SDI	Serial Data Input. SPI MOSI data input from controller.
32	SDO	Serial Data Output. SPI MISO data output to controller.
33	CLK	Serial Clock Input from Controller
34	$\overline{\text{CS}}$	Chip Select Input from Controller
2	A0	Chip Address LSB for Addressable SPI. See Table 7.
1	A1	Chip Address MSB for Addressable SPI. See Table 7.

Pin Description (continued)

PIN	NAME	FUNCTION
GATE DRIVERS		
18, 19, 42, 43	G1, G2, G3, G4	Gate Driver Outputs for Optional pMOS Transistors. Gate driver outputs are required for reverse current protection and full IEC 61131-2 Digital Input compatibility. G1 to G4 can be left unconnected when external pMOS transistors are not used.
LED DRIVER MATRIX		
10	V_{LED}	Supply for LED drivers. Apply supply voltage of 3.0V to V_{DD}.
9	SLED	Status LED Cathode Connection
4	FLED	Fault LED Cathode Connection
8	L1	Channel 1 LED Common Anode Connection. Connect a resistor in series to set the LED current.
7	L2	Channel 2 LED Common Anode Connection. Connect a resistor in series to set the LED current.
6	L3	Channel 3 LED Common Anode Connection. Connect a resistor in series to set the LED current.
5	L4	Channel 4 LED Common Anode Connection. Connect a resistor in series to set the LED current.

Functional Diagram



Detailed Description

The MAX14906 is a high-speed, four-channel IEC 61131-2-compliant industrial digital-output, digital-input device that can be configured on a per-channel basis as a high-side switch, push-pull driver, or a Type 1- and 3-, or Type 2-compliant digital input. The MAX14906 is specified for operation with a supply voltage up to 40V and is tolerant to 65V. Each channel can be supplied with an individual supply voltage that can be set at different levels.

The high-side switch current limiting is settable from 130mA to 1.2A with the option of 2x load inrush current. The high-side driver on-resistance is 120mΩ (typ) at 25°C ambient temperature. Optional push-pull operation allows high speed driving of cables and fast discharge of load capacitance. For Digital Input operation current sinks for 2.3mA (Type 1 and 3) or 7mA (Type 2) are provided.

Operating Modes

Each DOI_ channel can be individually configured for digital output operation by setting the corresponding SetDi_ bit within the SetOUT register to 0. For digital input operation, set the corresponding SetDi_ bit within the SetOUT register to 1. By default all four channels power up as outputs.

Two DoMode bits for each channel (DoMode_[1:0]) in the ConfigDO register set the output mode, high-side or push-pull, and the bit Typ2Di in the ConfigDI register controls input configuration mode, to Type 1 and 3, or Type 2. Table 1 lists the options and appropriate bit settings.

For setting or reading the I/O levels, the user can use the SPI interface or directly control the four bidirectional logic pins D1 to D4.

Table 1. Operating Modes

SetDi_	Typ2Di	DoMode_[1:0]	MODE
0	X	00	DO Mode, High-side
0	X	01	DO Mode, High-side with 2x inrush current for t_{INRUSH} time
0	X	10	DO Mode, Active clamp push-pull
0	X	11	DO Mode, Simple push-pull
1	X	1X	Low-leakage, High-impedance
1	0	0X	DI Mode, Type 1 and 3
1	1	0X	DI Mode, Type 2

Digital Input Operation

Each channel can be configured as a Type 1 and 3, or a Type 2 digital input. However, it is not possible to mix input types as the internal current sink is globally set to either 2.3mA (typ) for Type 1 and 3, or 7mA (typ) for Type 2 inputs.

To configure a channel as an input, use the SPI interface to set the appropriate SetDi_ bit within the SetOUT register to 1. By default, inputs are configured as Type 1 and 3 with bit Typ2Di = 0 in the ConfigDI register. To change the configuration of all input channels to Type 2, set Typ2Di to 1.

To read the level of the DOI input channels, the user can poll the DoiLevel register using the SPI interface and read bits DoiLevel_/VDDOKFault_. Alternatively, the user can monitor the logic pins D1 to D4 directly.

Standard compliant digital inputs are required to support a minimal voltage range from -3V to +30V. In order to allow the DOI_ input voltage to go above the $V_{DD_}$ supply voltage and not be clamped to one diode above the field supply by the high-side body diode, an external pMOS transistor can be placed in series between the field supply and each individual $V_{DD_}$ supply pin, as shown in the *Typical Application Circuits*.

Digital Output Operation

Each DOI_ channel can be configured as a high-side (HS) switch or a push-pull (PP) driver. In digital output high-side mode, the DOI_ output voltage is high when supplied from $V_{DD_}$, and the HighO_ bit is 1 or D_ pin is high with SYNCH high. The DOI_ output is high-impedance when the HighO_ bit is 0 or D_ pin is low with SYNCH high. The high-side driver has 120mΩ (typ) on-resistance at 500mA and 25ºC ambient temperature.

In digital output mode, the DOI_ output state follows the logical OR of the HighO_ bit and the D_ pin when SYNCH is high. If the application only uses the SPI interface to set DOI_ channel states, the D_ pins should be tied low with a pulldown resistor.

Except for simple push-pull mode, the DOI_ voltage can go below PGND, as occurs during inductive load demagnetization. Internal clamping structures limit the negative excursion to ($V_{DD_}$ - V_{CL}). See *Driving Inductive Loads* in the applications information for details. The low-side switch speeds up the discharge of RC loads in push-pull mode.

The driver output pins (DOI_) are monitored in both high-side and push-pull modes and the corresponding logic level can be read out from the DoiLevel register, when the VDDFaultSel bit in the ConfigDI register is 0. The DOI_ threshold voltages in DO modes are the same as in DI modes. When the channels are in DO mode the DOI_ status can be read in the DoiLevel register only, but in DI mode, the DOI_ status can be read in both the DoiLevel register and from the D_ pins.

The MAX14906 has two push-pull modes. Simple push-pull mode uses a push-pull pair in which the DOI voltage switches rail-to-rail inside the $V_{DD_}$-to-GND range even when an inductive load is present. Active-clamp push-pull mode behaves similarly to simple push-pull mode when resistive and capacitive loads are driven; however, the kick-back energy in inductive loads causes the DOI to be clamped at a negative voltage ($V_{DD_}$ - V_{CL}) when the low-side is turned on subsequent to the high-side being on. This causes fast demagnetization of inductive loads.

Reverse Current Protection and Overvoltage Support

To protect the MAX14906 against high-reverse-current flow into the DOI_ pins, an optional external pMOS transistor, as shown in the *Typical Application Circuits*, can be used. In this case, the gate drive pins G1 to G4 must be enabled with the GDrvEn_ bits in the OpnWrEn register.

Driver Enable

When the EN pin is driven low, all DOI_ channels are disabled/three-stated, independent of the SYNCH pin level, the D_ pin levels, or the settings of the HighO_ bits in the SetOUT register.

Load Current Limiting

The maximum load currents of the high-side and low-side switches are actively limited. The current limit of the high-side switch is selectable for four operating ranges: 130mA, 300mA, 600mA, and 1.2A. Use the two CL_ bits in the CurrLim register to select the operating current range for each channel. In push-pull modes, the low-side transistor has a current limit of 150mA (min). If the high-side or low-side transistor is in active current limit, this is indicated as a current-limit fault in the CL1 to CL4 bits in the OvrLdChF register.

An overcurrent or output short-circuit generally results in a rapid temperature rise in the chip. Both the high-side and low-side transistor temperature are continuously monitored. When any channel temperature exceeds 170°C (typ), the DOI_ driver is put into high-impedance (Hi-Z) mode until the temperature falls by the hysteresis amount (15°C typ).

The result of overcurrent on both high-side and low-side switches is indicated through the current limit bits CL1 to CL4 and thermal overload is indicated through the bits OVL1 to OVL4 in the OvrLdChF register.

Inrush Current Mode

The driver inrush current mode enables 2x load current for t_{INRUSH} time. This mode allows faster turn-on of incandescent lamp loads and charging of large capacitive loads. Inrush current can be enabled per-channel using the two DoMode_ bits in the ConfigDO register, while the current limit value and inrush time (t_{INRUSH}) are set per-channel using the two CL_ bits in the CurrLim register. Refer to Table 2.

Table 2. Inrush Current Mode

CL_[1]	CL_[0]	CURRENT LIMIT (min)	INRUSH MODE CURRENT LIMIT (min)	t_{INRUSH} (ms)
0	0	600mA	1.2A	20
0	1	130mA	260mA	50
1	0	300mA	600mA	40
1	1	1.2A	2.4A	10

Chip Thermal Protection

When the chip temperature rises above the thermal shutdown threshold of 150°C (typ), the chip enters thermal shutdown for protection and all DOI_ drivers are turned off until the chip temperature drops below 140°C (typ). The ThrmShutd bit in the GlobalErr register and $\overline{FAULT}$ output are set in this condition. If the chip temperature rises above 165°C, the internal LDO (V_5 regulator) goes into thermal shutdown to prevent damage to the device. In this condition, the ThrmShutd bit and $\overline{FAULT}$ output are already set. The register contents are not lost in thermal shutdown if the V_{DD} supply is present. When the chip temperature falls by the hysteresis amount, the V_5 regulator turns on, and the LED matrix and the DOI_ drivers are restored to normal operation.

Channel Thermal Management

Every channel temperature is constantly monitored. If the temperature of a channel rises above the thermal shutdown threshold of 170°C (typ), that channel is automatically turned off for protection. After the temperature drops by 15°C (typ), the driver is turned on again. When a channel turns off due to thermal shutdown, the per-channel thermal overload bit OVL_ in the OvrLdChF register and the OverLdFault bit in the Interrupt register are set to 1; the $\overline{FAULT}$ pin is asserted low if the OverLdM bit in the Mask register is set to 0.

Overvoltage Lockout

When a $V_{DD_}$ supply voltage exceeds the V_{DD_OVTH} threshold voltage of 43.5V (typ) in digital output mode for a duration longer than 200µs (typ), the high-side and low-side switches are automatically turned off. They remain turned off until $V_{DD_}$ is reduced to below the V_{DD_OVTH} - V_{DD_OVHYST} threshold voltage.

When a $V_{DD_}$ supply voltage exceeds the V_{DD_OVTH} threshold voltage of 43.5V (typ) in digital input mode for a duration longer than 200µs (typ), the VDDOV_ bits in ShtVDDChF register are set and the SupplyErr bit in the Interrupt register is also set.

Power-Up and Undervoltage Lockout

When any of the V_{DD}, V_5, V_L, or V_{INT} supply voltages are under their respective UVLO thresholds, all DOI_ switches are off and the open-wire detection current sources are turned off. V_{INT} is an internally generated supply for the registers and logic circuitry derived from the V_5 or V_{DD} supply.

When the V_{DD} or V_5 supply rises, the internal logic supply V_{INT} exceeds the internal threshold (V_{TUV_INT}). If the V_L supply is also above its UVLO threshold voltage, the $\overline{READY}$ pin becomes passive-low to indicate that the part is ready for communication through the SPI interface.

After power-up, the VDD_UVLO, VDD_Low, VDD_Warn, VINT_UV and V5_UVLO bits in the GlobalErr register are set to 1, and the $\overline{FAULT}$ output is asserted low. These bits and the $\overline{FAULT}$ pin only clear once the GlobalErr register is read. The register contents are lost when the internal register supply (V_{INT}) falls below its undervoltage lockout threshold. The VINT_UV bit indicates that the register contents are in power-on-reset state and can be programmed.

When V_{DD} rises above $V_{DD_UVLO_R}$, in the case of VDDOnThr bit in the Config2 register set to 0, or above $V_{DD_GOOD_R}$, in the case of VDDOnThr bit set to 1, the $\overline{VDDOK}$ pin is asserted low, indicating that the V_{DD} supply is high enough so the DOI_ switches can operate normally. When V_{DD} falls below $V_{DD_WARN_F}$, the VDD_Warn bit is set to 1, but the DOI_ switches continue operating normally. If VddOKM bit in the Mask register is disabled, the $\overline{FAULT}$ pin is also asserted low at the same time that the VDD_Warn bit is set to 1. When V_{DD} falls further below $V_{DD_UVLO_F}$, the VDD_UVLO bit is set and the DOI_ switches are turned off. The $\overline{VDDOK}$ pin is released high when V_{DD} falls below $V_{DD_WARN_F}$, if the VDDOnThr bit is set to 1. Otherwise, the $\overline{VDDOK}$ pin is high when V_{DD} falls below $V_{DD_UVLO_F}$ if the VDDOnThr bit is set to 0. The $\overline{VDDOK}$ pin only monitors the V_{DD} supply thresholds. Refer to Figure 2 and Figure 3 for different V_{DD} UVLO thresholds based on different VDDOnThr bit settings.

The four-channel $V_{DD_}$ supplies are also monitored. When a channel $V_{DD_}$ supply is below its threshold, as defined by the VDDOnThr bit setting in the Config2 register, the per-channel VDDOKFault_ bit in the DoiLevel register is set if the VDDFaultSel bit is set to 1 in the ConfigDI register. The VDDOKFault_ bit is latched and can be read and cleared through the SPI interface.

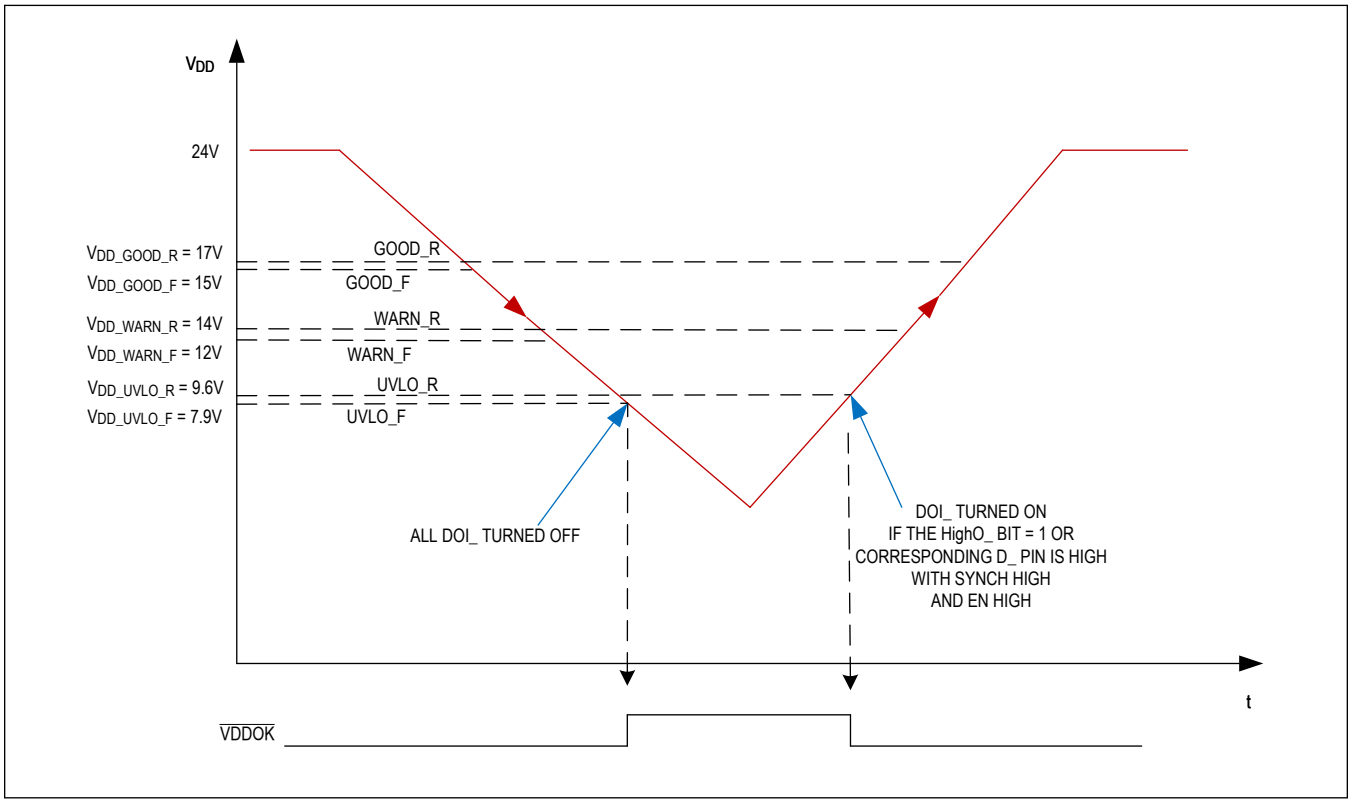


Figure 2. V_{DD} Monitoring with VDDOnThr = 0

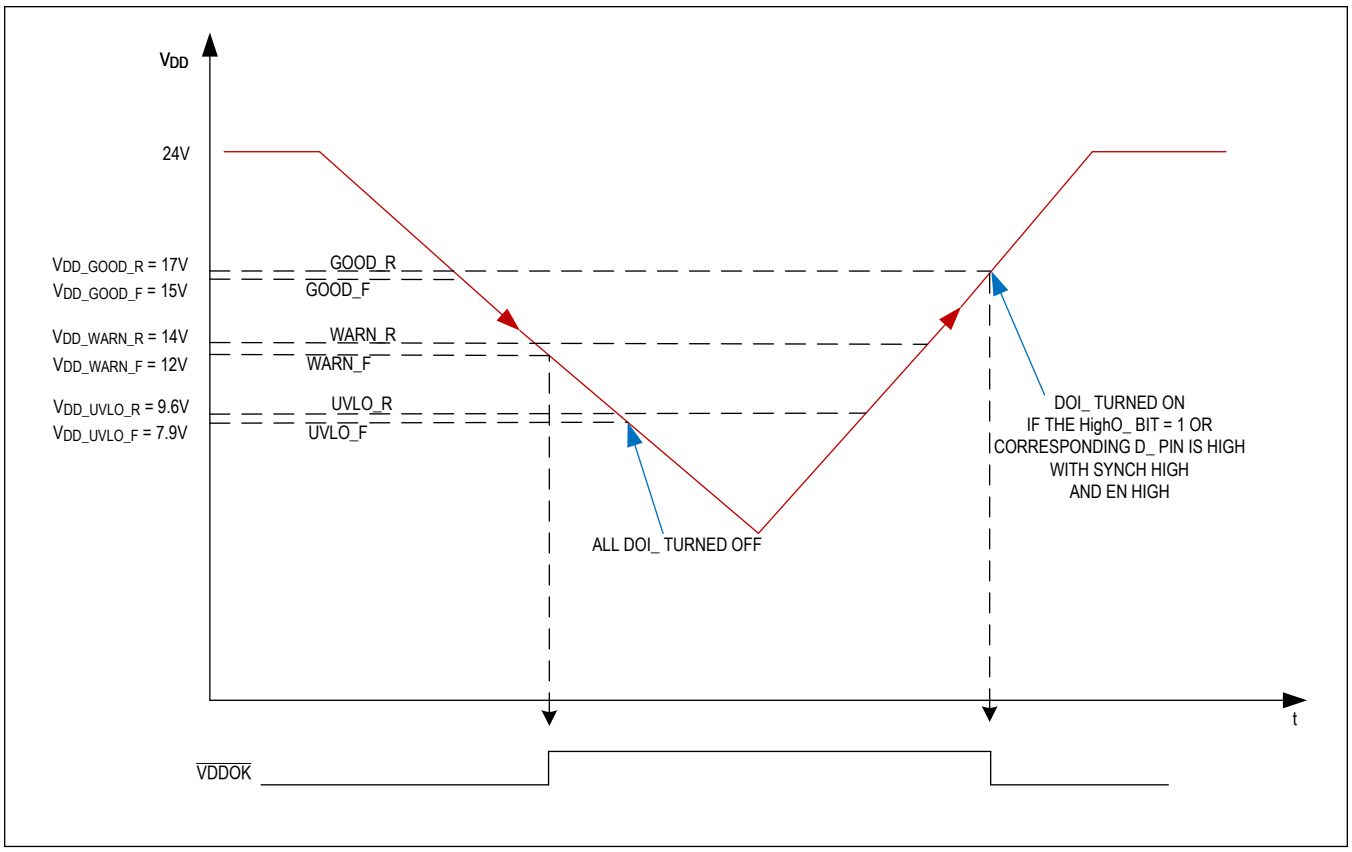


Figure 3. V_{DD} Monitoring with VDDOnThr = 1

Diagnostics

The per-channel diagnostics are listed in Table 3. These diagnostic faults are all enabled in digital output modes, and all faults are disabled (except $V_{DD_}$ OVLO and $\overline{VDDOK}$ faults) in digital input modes. Table 4 summarizes the global diagnostics.

Table 3. Per-Channel Diagnostics

PER-CHANNEL DIAGNOSTICS	ACTIVE IN HS MODE WHEN	ACTIVE IN PP MODE WHEN	ENABLED VIA	$\overline{FAULT}$ PIN INTERRUPT MASKABLE VIA
Thermal Overload	Switch closed	Always active	Always enabled	OverLdM
Current Limit	Switch closed	Always active	Always enabled (*)	CurrLimM
Open-Wire Fault with Switch Off	Switch open	Not active	OWOffEn_ = 1	OWOffM
Short-to-V_{DD}	Switch open	Not active	ShVddEn_ = 1	ShtVddM
Above V_{DD}	Always active	Always active	Always enabled	AboveVDDM
V_{DD} OVLO (**)	Always active	Always active	VDDOVEn_ = 1	SupplyErrM
SafeDemag Fault	Always active	Always active	Always enabled	Not maskable
$\overline{VDDOK}$ Fault (**)	Always active	Always active	VDDFaultSel = 1	SupplyErrM, VDDFaultDis

(*) Fault LEDs only signal faults according to the LEDCurrLim bit in the Config1 register.

(**) Enabled in digital input modes.

Table 4. Global Diagnostics

GLOBAL DIAGNOSTICS	FUNCTION	$\overline{FAULT}$ PIN INTERRUPT MASKABLE VIA
ThrmShutd	Chip thermal shutdown	Not maskable
VINT_UV	Undervoltage on the internal supply for the SPI registers	SupplyErrM
V5_UVLO	V_5 undervoltage	SupplyErrM
VDD_Warn	Below V_{DD_WARN} threshold	VddOKM, SupplyErrM, VDDFaultDis
VDD_Low	Below V_{DD_GOOD} threshold	VddOKM, SupplyErrM, VDDFaultDis
VDD_UVLO	V_{DD} supply in UVLO; all DOI_ switches turned off	SupplyErrM, VDDFaultDis
SPI/CRC Error	CRC error, or SPI clock cycle error, or watchdog error (***)	ComErrM
WDogErr	SYNCH input inactivity or SPI interface inactivity	ComErrM
LossGND	GND is disconnected	SupplyErrM

(***) The ComErr bit in the Interrupt register is the result of a logical OR of the SPI and SYNCH watchdog error (WDogErr), SPI number of clock cycles error, and CRC error.

Diagnostics Filtering

Open-wire detection and short-to-V_{DD} detection in conjunction with reactive loads can take many milliseconds to settle to stable conditions after a change in the high-side switch mode. During this time, diagnostic detection would not generate reliable results. After the DOI_ state switches, a blanking period of 4ms (typ) or 8ms (typ) based on the FilterLong bit in the Config1 register can be selected, during which these diagnostics are not evaluated. After this blanking time, a 4ms (typ) averaging filter is enabled after which the short-to-V_{DD} and open-wire diagnostics are updated as per-channel diagnostics in the OpnWirChF, ShtVDDChF, and the Interrupt registers. If the FLEDSet bit in the Config1 register is 0, the fault LEDs are turned on under the fault conditions, and in the next SPI cycle the diagnostic bits (SHTVDD, OWOffF) can be read from the SDO pin.

When a DOI_ switch changes state, the diagnostics for the previous state is cleared internally. The diagnostic bits in the OvrLdChF, OpnWirChF, and ShtVDDChF registers are cleared if the FLatchEn bit in the Config1 register is set to 0. If FLatchEn = 1, the diagnostic bits are cleared by a SPI read command. The faults in the GlobalErr register, SafeDemagF_ faults and VDDOKFault_ faults are always latched.

For the thermal overload and overcurrent diagnostics detection, a filter time is used (36µs (typ) for overload and 68µs (typ) for overcurrent) and there is no blanking time. To manage cold lamp loads or other heavy loads, an optional blanking time can be activated on thermal overload faults (OVL_). When DOI_ changes state, a dedicated timer masks overload faults for a period up to 300ms (typ). See the OVLBlank bits in the *ConfigDI* register for details. In case of cold lamp loads, per-channel thermal faults (OVL_) can blink on/off many times before reaching a steady-state, to avoid this "lamp blinking," an optional fault stretch function can be enabled to mask the thermal overload faults for a minimum 100ms (typ). See the OVLStretchEn bit in *ConfigDI* register for details.

AboveVDD faults are filtered with a 200µs (typ) debouncer with a 10.7ms (typ) stretch function after the debouncer, while V_{DD} OVLO faults (VDDOV_) is only filtered with a 200µs (typ) debouncer.

Open-Wire Detection with High-Side Switch Off

When an output channel is configured as a high-side switch, the MAX14906 monitors for an open-wire condition when the switch is in an off state. This can be enabled on individual channels using the OwOffEn_ bits in the OpnWrEn register. When the open-wire detection is enabled and the DOI_ switch is off, a current source is enabled, which pulls the DOI_ pins to 6.7V (typ) if there is an open-wire condition. The current source value can be set between 60µA (typ) to 600µA (typ) using OWOffCs[1:0] bits in the Config2 register.

If the DOI_ voltage is above 5V (min), an open-wire fault is indicated and the OWOff_ bits in the OpnWirChF register and the OWOffFault bit in the Interrupt register are set. The I_{DIAG} current source is turned off when open-wire detection is disabled on a channel.

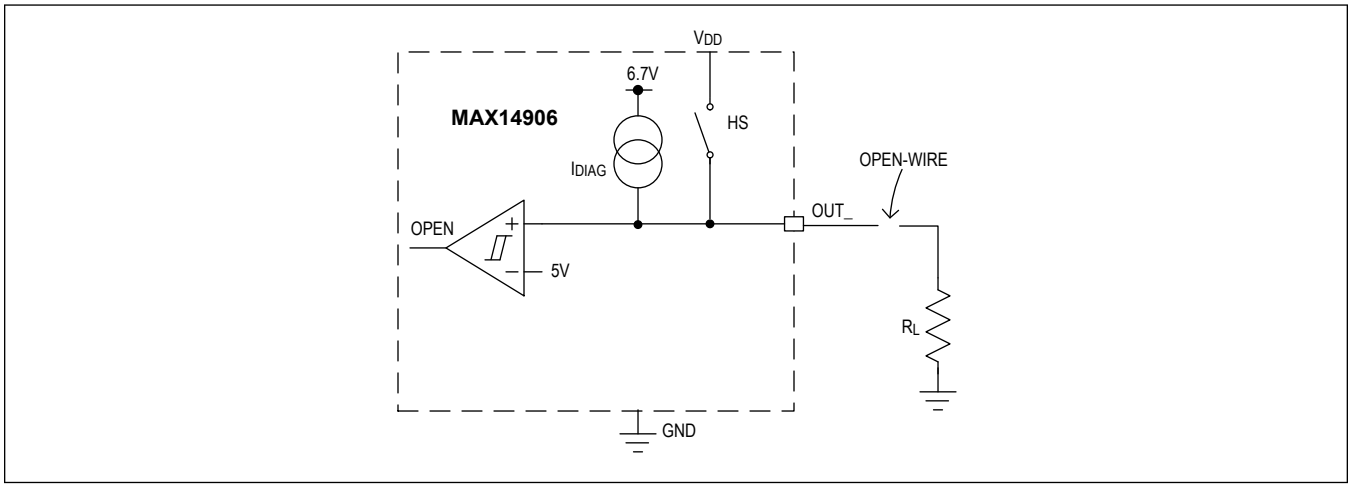


Figure 4. Open-Wire Detection with Switch OFF

Short-to-V_{DD} Detection

When an output channel is configured as a high-side switch, the MAX14906 monitors for a short-to-V_{DD} condition when the switch is in the off state. This can be enabled on individual channels using the ShVddEn_ bits in the ShtVDDEn register. When the short-to-V_{DD} detection is enabled and the DOI_ switch is off, a current source is enabled, which pulls the DOI_ pins to 6.7V (typ). The current source value can be set between 60µA (typ) to 600µA (typ) using OWOffCs[1:0] bits in the Config2 register. If the DOI_ voltage is higher than the threshold voltage selected by the ShtVddThr[1:0] bits in the Config2 register, the ShtVDDFault bit in the Interrupt register and the SHVDD_ bits in the ShtVDDChF register are set, and the $\overline{FAULT}$ output is asserted (if not masked).

The ShtVddThr[1:0] bits select a threshold between 9V (typ) and 14V (typ) when $V_{DD_}$ is above the V_{DD_GOOD} thresholds. For $V_{DD_}$ below 16V (typ), the V_{TH_SHVDD} is always set to 9V, independent of the ShtVddThr[1:0] bits.

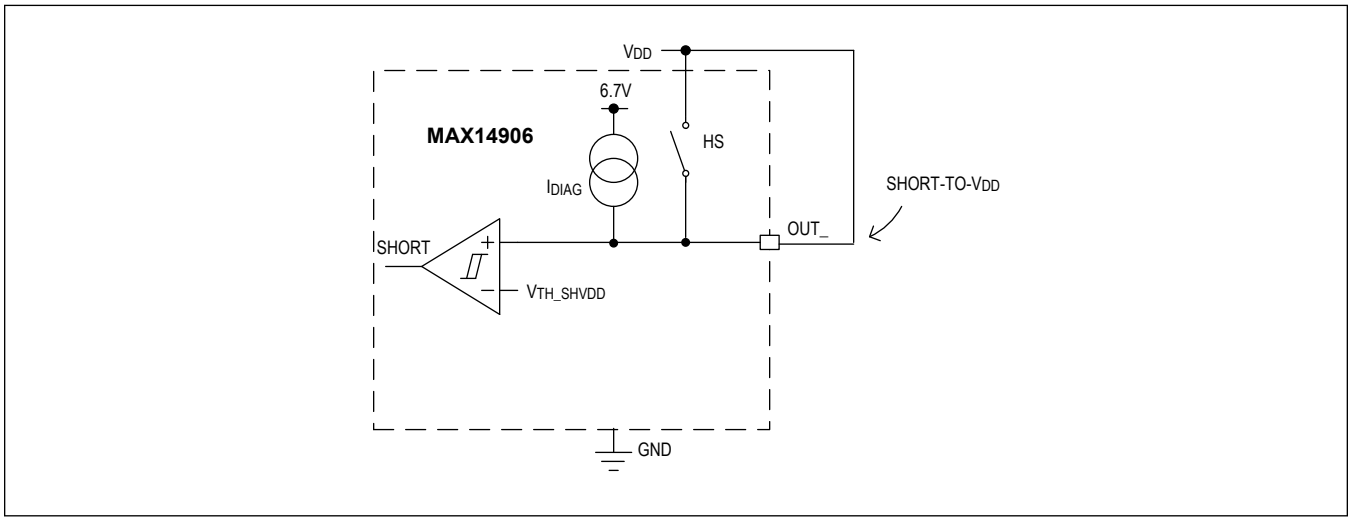


Figure 5. Short-to-V_{DD} Detection

SafeDemag Fault

The SafeDemagF_ bits in the DoiLevel register are always latched (can never be masked), allowing the microcontroller to identify which channel went into SafeDemag condition with the resulting thermal overload of both the high-side and low-side switches.

Above-V_{DD} Fault

The MAX14906 has a comparator to monitor if the DOI_ outputs are higher in voltage than the $V_{DD_}$ supply. If the Above-V_{DD} condition is present after a debounce time of 200µs (typ), the AboveVDD_ fault bits in the OpnWirChF register and the AboveVDDFault bit in the Interrupt register are set.

If an external pMOS transistor is used and enabled, and the AboveVDDProtEn bit in the ConfigDI register is set to 1 when the AboveVDD_ fault is set, the external pMOS transistor is turned off for protection purposes through the G_ pin and the high-side switch is driven off. The AboveVDD_ fault is stretched for 10.7ms (typ) before the high-side switch and the external pMOS transistor are turned back on.

If an external pMOS transistor is not used, the AboveVDD_ faults are latched in the registers, the $\overline{FAULT}$ pin is asserted low (if not masked), and no further action is taken on the DOI_ or G_ pins.

Loss of GND Fault

During a loss of ground event with a large inductive load, the inductor energy might be partially dissipated by the external V_{DD} TVS diode. In order to avoid stress on the TVS diode, the microcontroller or FPGA should turn the high-side switch off when the loss of ground fault is detected and indicated by the LossGND bit in the GlobalErr register. At power-on-reset, the loss of ground bit can be 1 or 0. The microcontroller should ignore this initial setting until after it reads the GlobalErr register to clear this bit for normal operaton.

Watchdog Fault

The MAX14906 has two watchdog timers. One watchdog monitors activity on the SPI interface and the other monitors activity on the SYNCH pin. The SPI watchdog timer is enabled and the timeout period is set through the WDTo[1:0] bits in the Config2 register. If enabled, it monitors and expects activity on the CLK and $\overline{CS}$ input. At least one valid SPI cycle must be detected in the watchdog timeout period. This means that the CLK input must have a multiple of 8 clock cycles during a $\overline{CS}$ low period.

The SYNCH pin watchdog can be enabled through the SynchWDEn bit in the Config2 register if the SPI watchdog timer is disabled (WDTo[1:0] = 00). The SYNCH pin watchdog monitors if the SYNCH pin is stuck low. At least a 1µs (typ) SYNCH high pulse must be present in a watchdog timeout period.

If the watchdog criterion is not met, all DOI_ switches are turned off, the WDogErr bit in the GlobalErr register is set to 1, and the $\overline{FAULT}$ pin is asserted low (if not masked).

Diagnostic Bit Behavior

The per-channel diagnostic bits (OVL_, CL_, OWOff_, AboveVDD_, SHVDD_, VDDOV_) can be configured to be latched or real-time (transparent) using the FLatchEn bit in the Config1 register. When FLatchEn = 1, the diagnostic bit is set to 1 when a fault is detected and remain as 1 even if the fault disappears. A diagnostic bit is only reset to 0 when the cause of the fault has disappeared and the relevant fault register is read. If the cause of the fault has not disappeared, the diagnostic bit remains set as 1.

The SafeDemagF_ and VDDOKFault_ bits are always latched. The fault bits in the Interrupt register (OverLdFault, CurrLim, OWOffFault, AboveVDDFault, ShtVDDFault, and DeMagFault) are the logical OR of the per-channel faults in each of the associated error registers.

$\overline{\text{FAULT}}$ Signaling

The $\overline{\text{FAULT}}$ pin is an open-drain logic output that asserts active-low when a fault condition is detected. The source of faults are the eight bits in the Interrupt register and the global thermal shutdown bit ThrmShutd in the GlobalErr register, covering per-channel faults and global faults. The source of a fault bit to assert the $\overline{\text{FAULT}}$ output can be masked using the Mask register. Refer to Figure 6 for details.

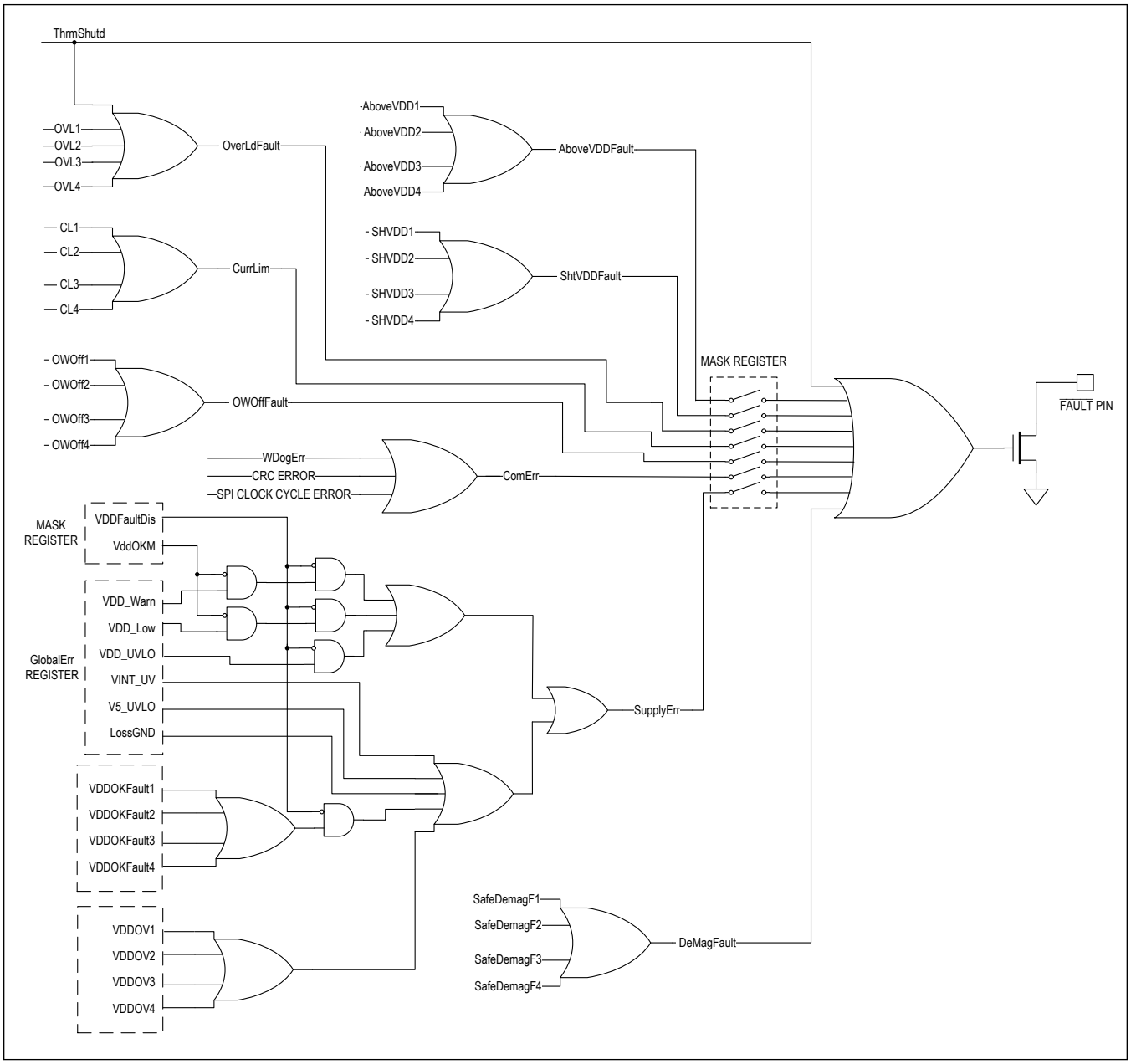


Figure 6. FAULT Interrupt Sources

Logic Interface

The logic interface features flexible logic levels, which allows the MAX14906 to interface with a wide range of logic devices such as microcontrollers or FPGAs. The V_L supply input defines the logic level and can be set in the range between 2.5V and 5.5V.

Synchronization

If SYNCH is low, the DOI_ states do not change in digital output modes, and DoiLevel_ bits and D_ pins do not change in digital input modes. If SYNCH is held high, the DOI_ switches change state immediately (transparent) when a new value is written into the SetOUT register or the D_ pins change in digital output modes. In digital input modes, the DoiLevel_ bits and D_ pins are updated as the DOI_ pins change state.

On the rising edge of SYNCH, the DOI_ channels configured as digital outputs change to a new state, which is a logical OR of the HighO_ bit in the SetOUT register and the D_ pin. On the falling edge of SYNCH, the DOI_ logic values are latched and the DoiLevel_ bits in the DoiLevel register are updated. In digital input modes, the D_ pins are also updated to represent the DOI_ levels.

Table 5. DOI_ Truth Table, Digital Input

MODE	EN	SYNCH	DOI_ CHANNEL PINS (INPUTS)	D_ LOGIC PINS (OUTPUTS)
Digital Input	X	0	24V Field Input	Latched, no change of state
	X	1	24V Field Input	Logic value of DOI_, transparent
	X	Rising edge	24V Field Input	Read DOI_ level and update D_ pin logic value
	X	Falling edge	24V Field Input	DOI_ logic value latched

Table 6. DOI_ Truth Table, Digital Output

MODE	EN	SYNCH	D_ LOGIC PINS (INPUTS)	DOI_ CHANNEL PINS (OUTPUTS)
Digital Output	0	X	X	Hi-Z
	1	0	Logic Input	No change of state
	1	1	Logic Input	Logical OR of HighO_ bit and D_ pin, transparent
	1	Rising edge	Logic Input	Logical OR of HighO_ bit and D_ pin, simultaneous for all DOI_ channels
	1	Falling edge	Logic Input	Latch DOI_

LED Matrix

The 4 x 2 LED driver crossbar matrix drives up to 8 LEDs (4 Status LEDs and 4 Fault LEDs). The LEDs can either be turned on/off by the SetLED register, or controlled by the MAX14906 autonomously to indicate per-channel status and fault conditions depending on the SLEDSet and FLEDSet bits in the Config1 register. Refer to Figure 7.

If controlled autonomously (SLEDSet = 0 or FLEDSet = 0), a channel status LED (SLED) is automatically turned on when the corresponding DOI_ channel is high/on in digital output modes, or the DOI_ digital input is high in digital input modes, and there is not a diagnostic fault condition. In low-leakage high-impedance mode, the status LEDs are always off.

If a diagnostic fault condition is detected on a DOI_ channel, its associated fault LED (FLED) is turned on and its associated status LED (SLED) is automatically turned off. For any DOI_ channel, its SLED and its FLED are never on simultaneously.

When the FLEDSet bit is 0 in digital output mode, all diagnostics that are enabled (SafeDemagF_, SHVDD_, VDDOV_, OWOff_, AboveVDD_, CL_ and OVL_) result in fault LEDs turning on when a fault is detected. Only overcurrent detection can be masked (through the LEDCurrLim bit in the Config1 register) from driving the fault LEDs. If FLEDSet is 0 in digital input mode or low-leakage high-impedance mode, only Global Thermal Shutdown (the ThrmShutd bit in the GlobalErr register) drives the fault LEDs.

If the fault LEDs are controlled autonomously, they are always filtered, and the FLED minimum on-time can be programmed by the FLEDStretch[1:0] bits in the Config1 register. The status LEDs are real-time when controlled autonomously.

The LED matrix is powered through the V_{LED} supply input, which can be in the range of the 3.0V (min) up to the V_{DD} field supply voltage.

For every current limiting resistor (R) each of the four LEDs in a column string is pulsed for 50% of the 1ms (typ) period, so that current only flows through one LED and a resistor at a time. The average current flowing through an LED that is turned on, is

$$I_{LED} = 0.5 \times (V_{LED} - V_F) / R$$

where V_F is the forward voltage of the LED. The resistor value should be chosen according to the LED current and light intensity requirements.

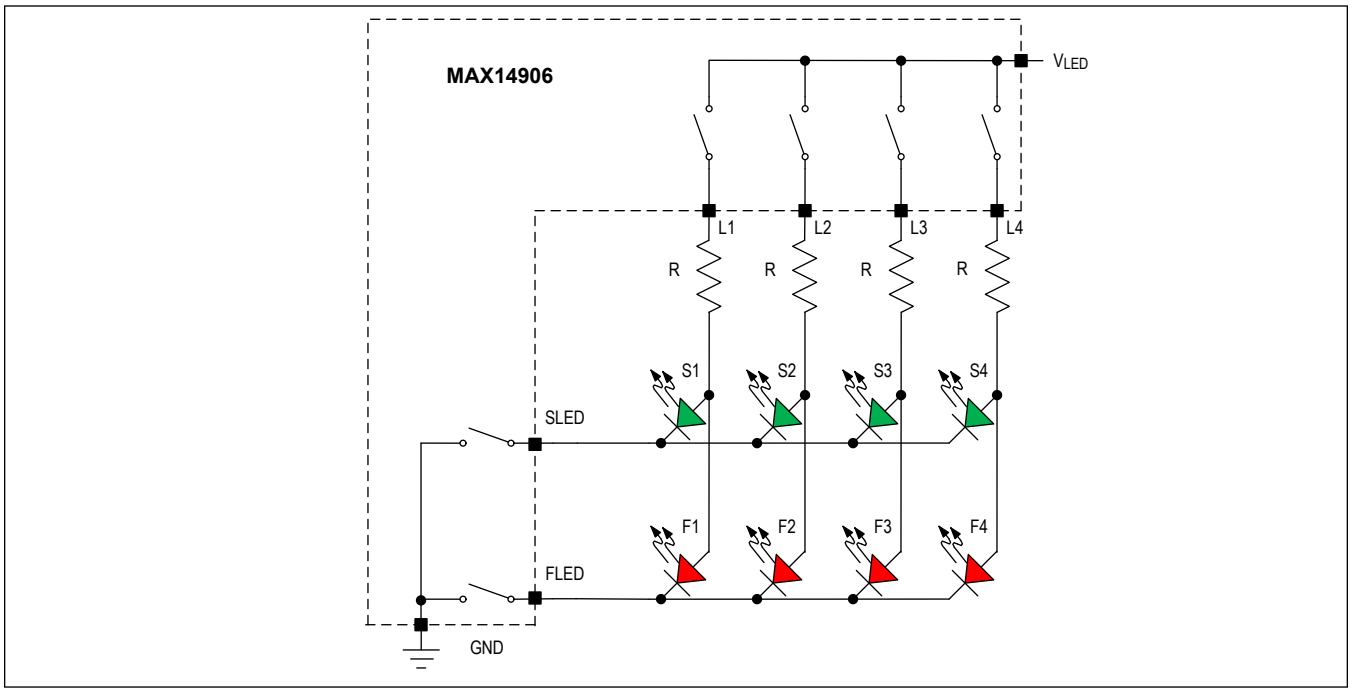


Figure 7. LED Matrix Scheme

Serial Interface

The MAX14906 has a high-speed SPI serial interface. The interface has three logic inputs: clock (CLK), chip select ($\overline{CS}$), serial data-in (SDI), and one output, serial data-out (SDO). The SDO is three-stated when $\overline{CS}$ is high, allowing multiple SPI slave devices to share a common (non-daisy-chained) SPI interface. The maximum SPI clock rate is 10MHz. The SPI interface adheres with clock polarity CPOL = 0 and clock phase CPHA = 0.

The MAX14906 SPI interface supports addressable SPI, which allows direct communication with up to four MAX14906 devices on a shared SPI interface using a single $\overline{CS}$ signal. Addressable SPI supports both single-cycle and burst read and write modes.

Addressable SPI

Each MAX14906 device on the addressable SPI interface is assigned an individual chip address through the logic input pins A1 and A0. Refer to Table 7.

Table 7. SPI Device Address Selection

A1	A0	DEVICE ADDRESS
LOW	LOW	00
LOW	HIGH	01
HIGH	LOW	10
HIGH	HIGH	11

The SPI master addresses a specific device by sending the appropriate A1 and A0 in the first and second bits of the SPI read and write command. The MAX14906 monitors the SPI address in each SPI read and write cycle and responds with SDO appropriately when the address matches the programmed address for that IC. If CRC is enabled, the responding MAX14906 sends its A1 and A0 address bits as part of its SDO data, so the master can check that the command really reached the desired device.

SPI Diagnostic Fault Signaling

In every SPI cycle, the addressed MAX14906 returns six SDO bits within the first eight SPI CLK cycles. These six bits include the global short-to-V_{DD} (SHTVDD), Above-VDD (AbvVDD), open-wire detection in off-state (OWOffF), current limit (OvrCurr), overload (OvldF), as well as a global diagnostic bit (GLOBLF). The global fault bit (GLOBLF) is the logical OR of the ComErr, SupplyErr, and ThrmShutd bits in the Interrupt and GlobalErr registers. These six diagnostic bits allows fast identification of the specific channels in fault or global fault conditions through a minimum of further SPI read cycles.

During a SPI write cycle, the second SDO byte returns eight bits, four DoiLevel bits and four fault bits, one bit associated with each DOI_ channel. Each fault bit (F_) is the logical OR of the per-channel fault bits including SafeDemagF_, VDDOKFault_, CL_, OVL_, OWOff_, AboveVDD_, VDDOV_, and SHVDD_.

SPI Single-Cycle Write

Figure 8 shows the SPI single-cycle write command and Figure 9 shows the SPI single-cycle write command with CRC enabled.

To operate in the SPI single-cycle write mode, the BRST bit is set to 0 and the W bit is set to 1. Bits D[7:0] in the second byte sent by the controller (SDI) are the data to be written into the register selected by bits R[3:0]. The DiLvl_ and F_ bits in the second byte sent by the device (SDO) report the DOI_ channel logic levels and per-channel fault conditions. Bits F1 to F4 are the logical OR of the fault bits including SafeDemagF_, VDDOKFault_, CL_, OVL_, OWOff_, AboveVDD_, VDDOV_, and SHVDD_. If any fault is present in any of the channels, the device immediately reports through the returned SDO data, and further SPI read commands of fault registers can be issued to identify the details.

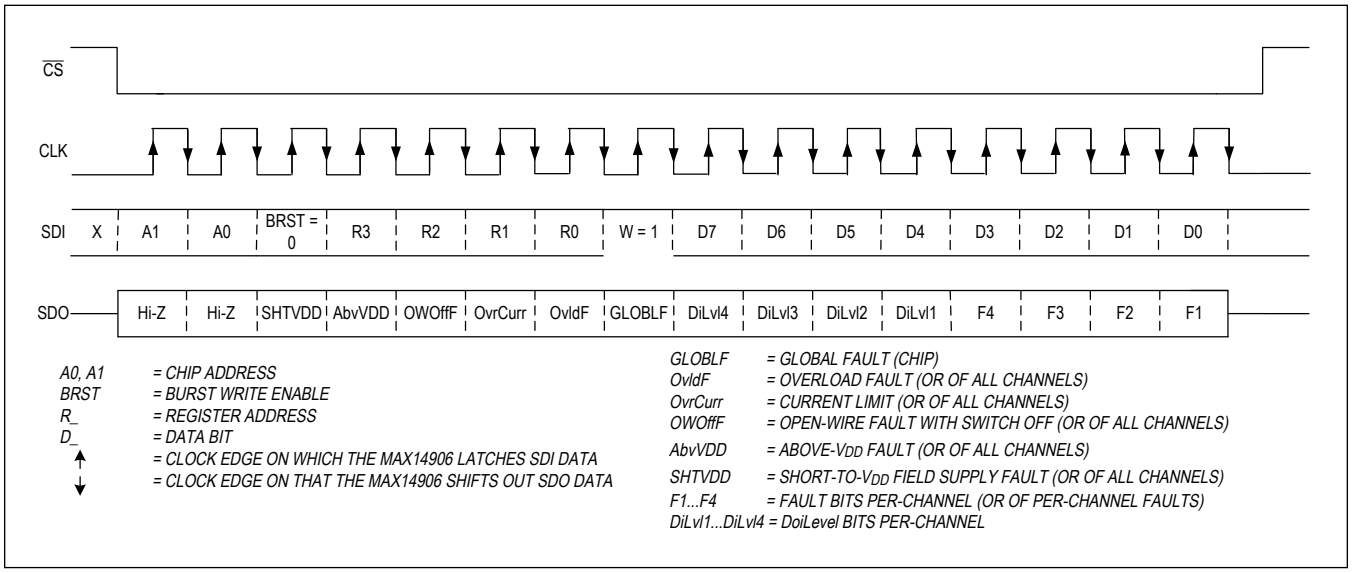


Figure 8. SPI Single-Cycle Write Command

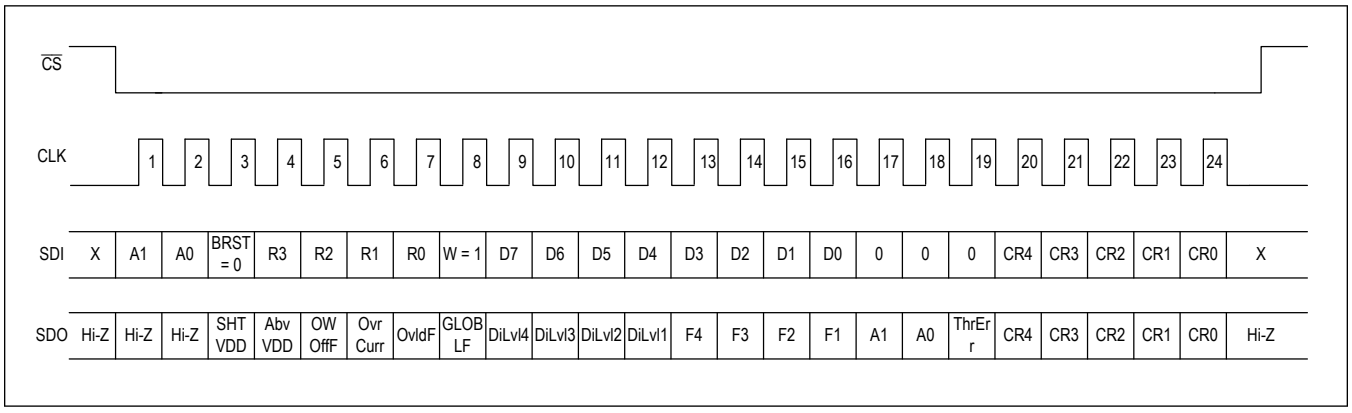


Figure 9. SPI Single-Cycle Write Command with CRC Enabled

SPI Single-Cycle Read

Figure 10 shows the SPI single-cycle read command and Figure 11 shows the SPI single-cycle read command with CRC Enabled.

To operate in the SPI single-cycle read mode, the BRST bit is set to 0 and the R bit is set to 0. Bits D[7:0] in the second byte sent by the device (SDO) are the data read from the register selected by bits R[3:0] in the first byte sent by the controller (SDI).

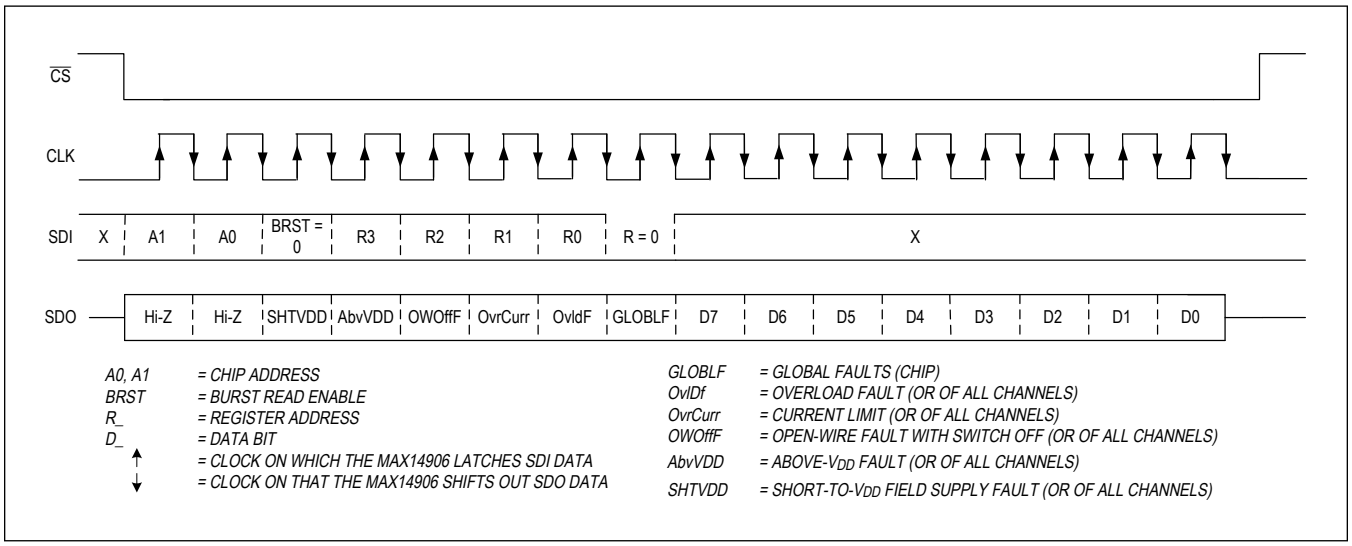


Figure 10. SPI Single-Cycle Read Command

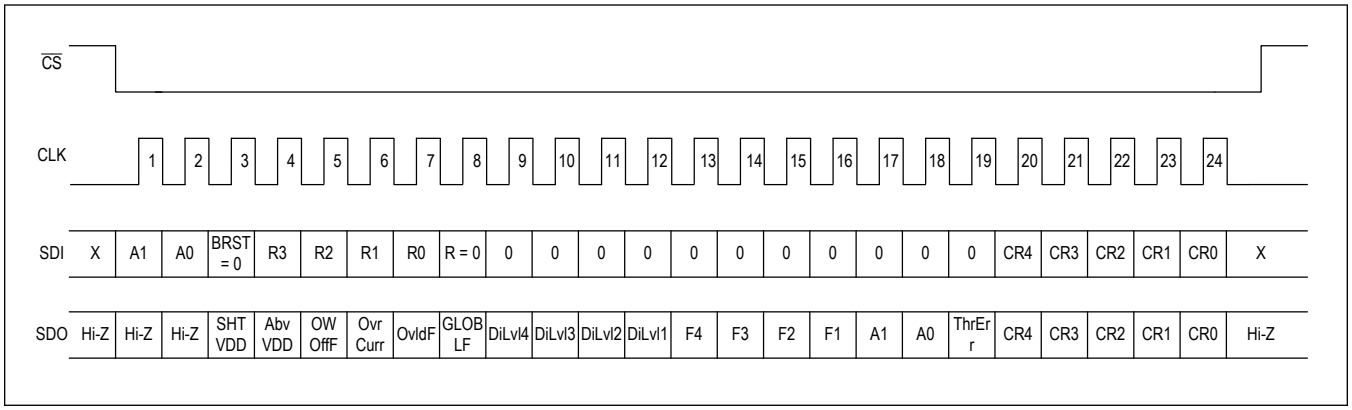


Figure 11. SPI Single-Cycle Read Command with CRC Enabled

SPI Burst Write

SPI burst mode allows using one SPI cycle and one register address to write to multiple consecutive registers and is enabled by setting the BRST bit to 1 in the SDI command byte. Figure 12 and Figure 13 illustrate SPI burst write diagrams. The SPI burst write command supports writing data to the most commonly accessed registers, SetOUT and SetLED.

If BRST = 1, the MAX14906 expects a SPI write cycle writing to both SetOUT and SetLED registers. The chip-select input ($\overline{CS}$) must be held low during the entire burst write cycle. The SPI clock continues clocking throughout the burst cycle. Only the initial register address 0x00 (SetOUT register) is specified using bits R[3:0] in the SDI command byte, followed by two bytes of data, one for the SetOUT register and the other for the SetLED register. The number of CLK cycles is 24 clock cycles if CRC is not used, and 32 clock cycles if CRC is enabled. CRC bits (CR[4:0]) are calculated on all the data sent before the CR[4:0] bits. The burst write cycle ends when the $\overline{CS}$ is driven high.

If the burst write finishes before writing to the two registers completely or if a burst write command attempts to address other registers, a communication error is signaled on the ComErr bit in the Interrupt register.

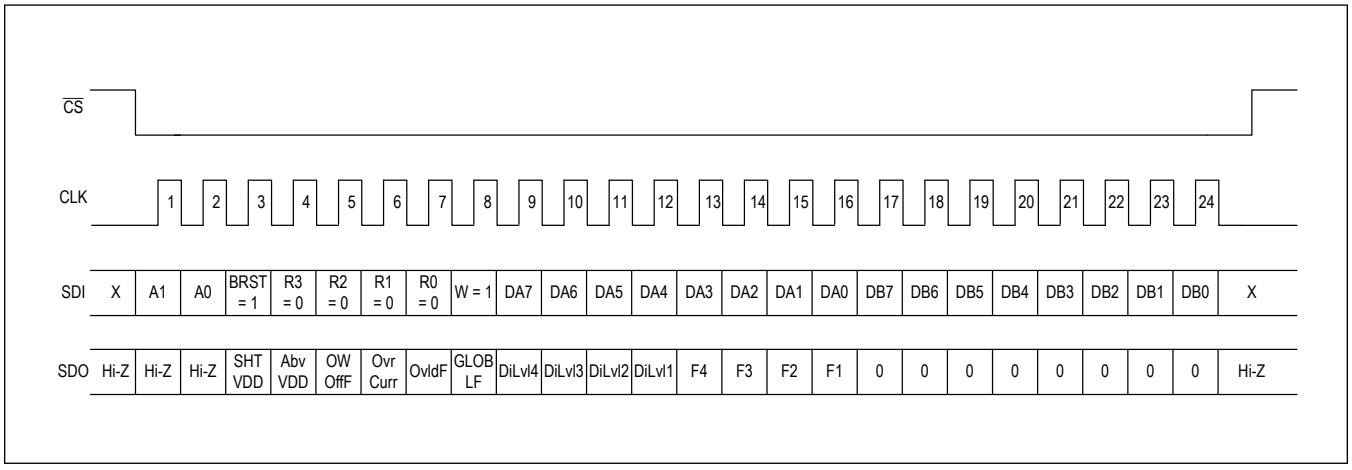


Figure 12. SPI Burst Write without CRC Enabled

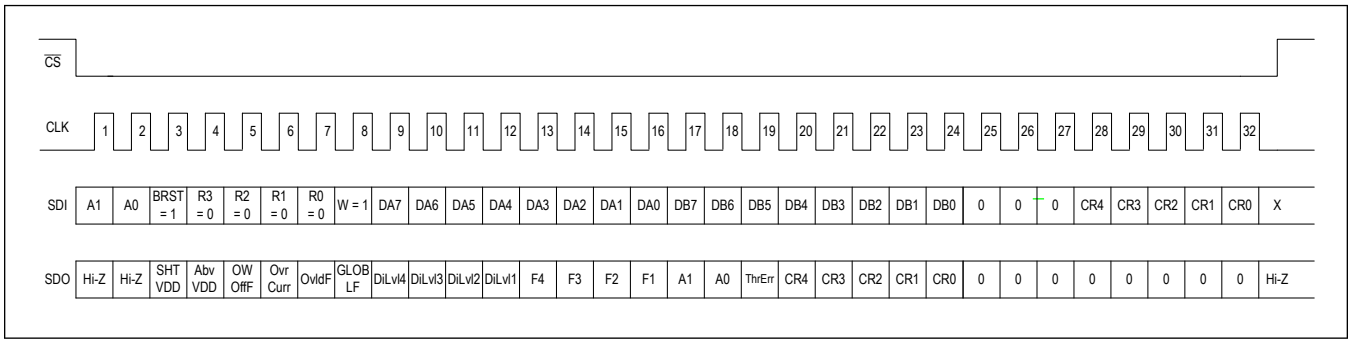


Figure 13. SPI Burst Write with CRC Enabled

SPI Burst Read

Figure 14 and Figure 15 show SPI burst read diagrams.

SPI burst mode allows using one SPI cycle and one register address to read multiple consecutive registers and is enabled by setting the BRST bit to 1 in the SDI command byte. The SPI burst read command supports reading data from the six consecutive diagnostic registers from address 0x02 to 0x07 (DoiLevel, Interrupt, OvrLdChF, OpnWirChF, ShtVDDChF, and GlobalErr registers). Note that this operation must read all six registers completely; otherwise, a communication error is flagged.

The chip-select input ($\overline{CS}$) must be held low during the entire burst read cycle. The SPI clock continues clocking throughout the burst cycle. The initial register address 0x02 (DoiLevel register) is specified using bits R[3:0] in the SDI command byte, and the burst read ends with register 0x07 (GlobalErr) is read. The number of CLK cycles is 56 clock cycles if CRC is not used, and 64 clock cycles if CRC is enabled. During a burst read with CRC enabled, data bits 9 to 59 in the SDI data stream can be a 0 or a 1 (they have no impact on MAX14906 configuration), but these bits are used to calculate the CRC bits (CR[4:0]). CR[4:0] are calculated on all the data sent before the CRC bits. The burst read cycle ends when the $\overline{CS}$ is driven high.

If the burst read command ends before the GlobalErr register has been read or if a burst read command attempts to address other registers, a communication error is signaled on the ComErr bit in the Interrupt register.

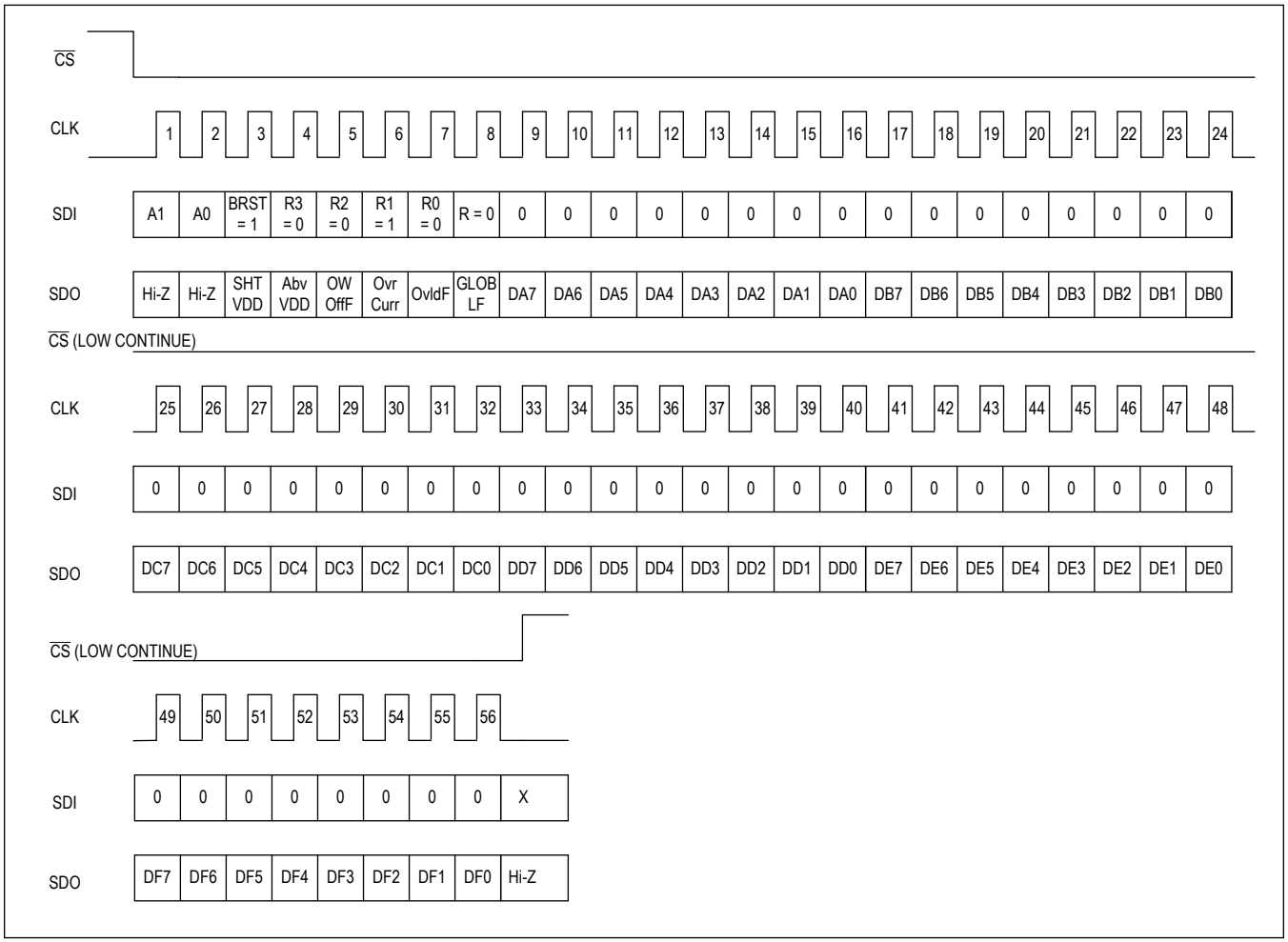


Figure 14. SPI Burst Read without CRC Enabled

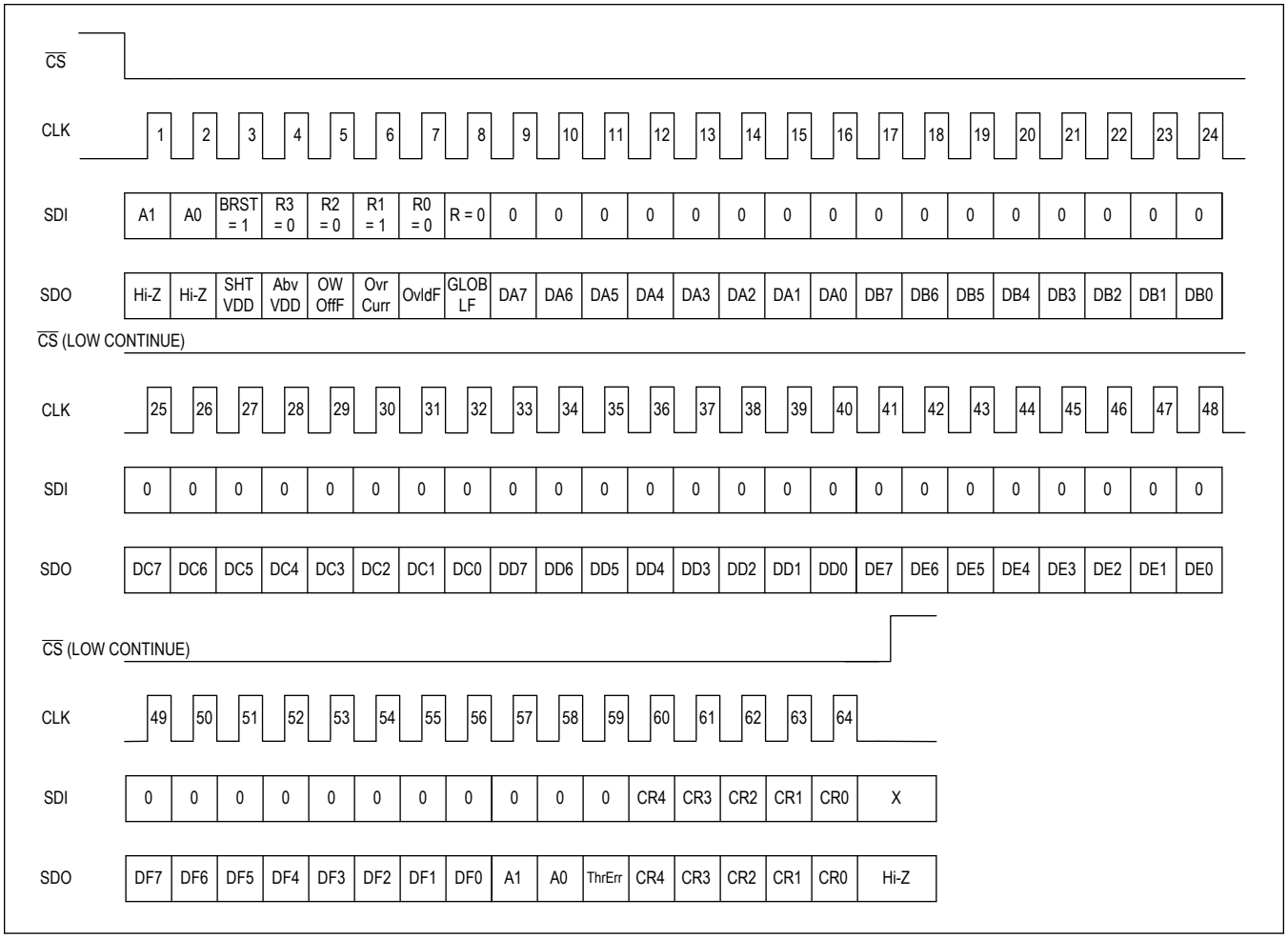


Figure 15. SPI Burst Read with CRC Enabled

CRC Error Detection on the SPI Interface

CRC error detection on the SPI interface can be enabled by setting the CRCEN pin high to detect the data corruption of the SDI and SDO signals. If CRC error detection is enabled, the MAX14906:

1) Performs error detection on the SDI data that it receives from the controller, and

2) Calculates the CRC on the SDO data and appends a check byte at the end of the SDO data stream that it sends to the controller.

This ensures that both the data it receives from the controller and the data it sends to the controller maintains data integrity.

Once enabled, a CRC frame check sequence (FCS) is sent with each SPI command. The 5-bit FCS (CR[4:0]) is based on the generator polynomial $x^5 + x^4 + x^2 + 1$ with CRC starting value = 0b11111. When CRC is enabled, the MAX14906 expects a check byte appended to the SDI data stream that it receives. The check byte format (CR[4:0]) can be seen in Figure 16. See *Application Note 6633* for more details.

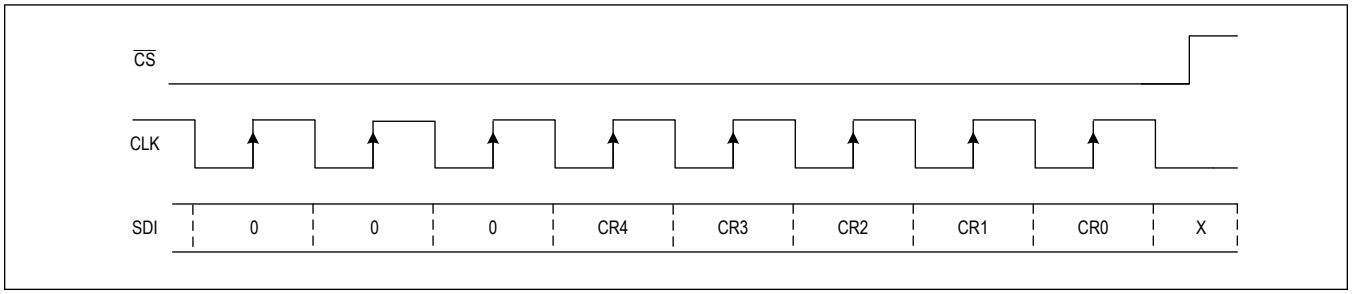


Figure 16. SDI Check Byte Expected from Controller

The 5 FCS bits in the SDI data stream are calculated on all the data bytes plus the three “0s” in the MSBs of the check byte. The CRC is calculated on 16 + 3 bits or up to 56 + 3 bits in case of a burst command. Some bits in the SDI data can be a 0 or 1 as they have no impact on the MAX14906 configuration. However, these bits are used to calculate the CRC so the microcontroller must take these bits into account when calculating the CRC, and this CRC value is appended to the end of the SDI data stream as bits CR[4:0].

The MAX14906 verifies the received FCS, and if no error is detected, the MAX14906 updates the configuration per the SDI data. If a CRC error is detected, the MAX14906 does not change the configuration, but asserts the ComErr bit in the Interrupt register.

The check byte that the MAX14906 appends to the SDO data has the format as shown in Figure 17. The A1 and A0 bits identify the SPI device address of the MAX14906 that returns the SDO data. The ThrErr bit is set when a chip thermal shutdown event occurrs. CR[4:0] are the CRC bits that the MAX14906 calculates based on the SDO data, including the A1, A0, and ThrErr bits. This allows the controller to check for the errors on the SDO data received from the MAX14906.

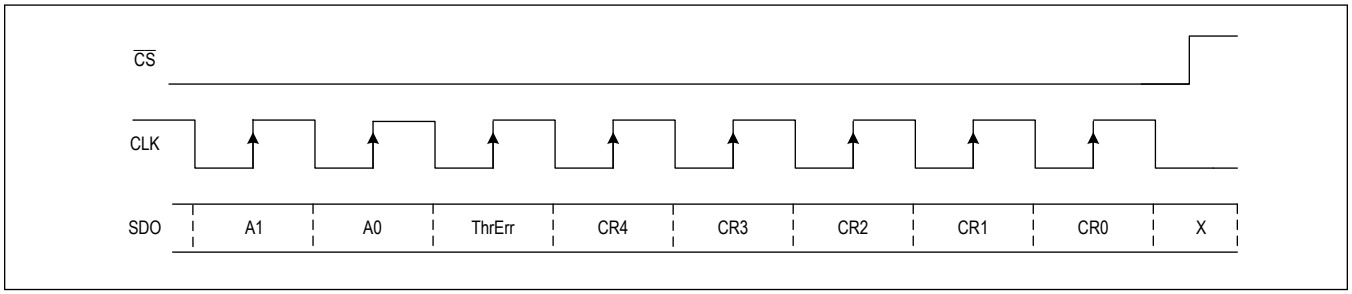


Figure 17. SDO Check Byte Sent by MAX14906

Number of Clock Cycles on the SPI Interface

The MAX14906 verifies that the number of clock cycles in one SPI cycle from the falling edge of $\overline{CS}$ to the rising edge of $\overline{CS}$ is a multiple of 8 with 16 clocks minimum. The expected number of clocks is scaled according to CRCEN pin configuration and burst mode setting. If the number of clock cycles differs from the expected, the SPI command is not executed and a SPI error is signaled through the ComErr bit in the Interrupt register.

Register Map

MAX14906

ADDRESS	RESET	NAME	MSB							LSB
0x00	0x00	SetOUT[7:0]	SetDi4	SetDi3	SetDi2	SetDi1	HighO4	HighO3	HighO2	HighO1
0x01	0x00	SetLED[7:0]	SLED4	SLED3	SLED2	SLED1	FLED4	FLED3	FLED2	FLED1
0x02	0x00	DoiLevel[7:0]	SafeDemagF4	SafeDemagF3	SafeDemagF2	SafeDemagF1	DoiLevel4/ VDDOKFault4	DoiLevel3/ VDDOKFault3	DoiLevel2/ VDDOKFault2	DoiLevel1/ VDDOKFault1
0x03	0x40	Interrupt[7:0]	ComErr	SupplyErr	DeMagFault	ShtVDDFault	AboveVDDFault	OWOffFault	CurrLim	OverLdFault
0x04	0x00	OvrLdChF[7:0]	CL4	CL3	CL2	CL1	OVL4	OVL3	OVL2	OVL1
0x05	0x00	OpnWirChF[7:0]	AboveVDD4	AboveVDD3	AboveVDD2	AboveVDD1	OWOff4	OWOff3	OWOff2	OWOff1
0x06	0x00	ShtVDDChF[7:0]	VDDOV4	VDDOV3	VDDOV2	VDDOV1	SHVDD4	SHVDD3	SHVDD2	SHVDD1
0x07	0x1F	GlobalErr[7:0]	WDogErr	LossGND	ThrmShutd	VDD_UVLO	VDD_Warn	VDD_Low	V5_UVLO	VINT_UV
0x08	0x00	OpnWrEn[7:0]	GDrvEn4	GDrvEn3	GDrvEn2	GDrvEn1	OwOffEn4	OwOffEn3	OwOffEn2	OwOffEn1
0x09	0x00	ShtVDDEn[7:0]	VDDOVEn4	VDDOVEn3	VDDOVEn2	VDDOVEn1	ShVddEn4	ShVddEn3	ShVddEn2	ShVddEn1
0x0A	0x53	Config1[7:0]	LEDCurrLim	FLatchEn	FilterLong	FFilterEn	FLEDStretch[1:0]		SLEDSet	FLEDSet
0x0B	0x00	Config2[7:0]	WDTo[1:0]		OWOffCs[1:0]		ShtVddThr[1:0]		SynchWDEn	VDDOnThr
0x0C	0x08	ConfigDI[7:0]	Typ2Di	Reserved	VDDFaultDis	VDDFaultSel	AboveVDDProtEn	OVLStretchEn	OVLBlank[1:0]	
0x0D	0x00	ConfigDO[7:0]	DoMode4[1:0]		DoMode3[1:0]		DoMode2[1:0]		DoMode1[1:0]	
0x0E	0x00	CurrLim[7:0]	CL4[1:0]		CL3[1:0]		CL2[1:0]		CL1[1:0]	
0x0F	0xBE	Mask[7:0]	ComErrM	SupplyErrM	VddOKM	ShtVddM	AboveVDDM	OWOffM	CurrLimM	OverLdM

Register Details

SetOUT (0x00)

BIT	7	6	5	4	3	2	1	0
Field	SetDi4	SetDi3	SetDi2	SetDi1	HighO4	HighO3	HighO2	HighO1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
SetDi4	7	0: DOI4 Digital Output Mode 1: DOI4 Digital Input Mode See the ConfigDO register for detailed configuration of digital output mode and the Typ2Di bit in the ConfigDI register for digital input mode. See Table 1 for operating mode configurations.
SetDi3	6	0: DOI3 Digital Output Mode 1: DOI3 Digital Input Mode
SetDi2	5	0: DOI2 Digital Output Mode 1: DOI2 Digital Input Mode
SetDi1	4	0: DOI1 Digital Output Mode 1: DOI1 Digital Input Mode
HighO4	3	0: DOI4 if HS mode switch = open, or PP mode driver = GND 1: DOI4 if HS mode switch = closed, or PP mode driver = V_{DD4} HighO_ is used to set the state of DOI_ when configured in DO modes. The logic state of a DOI_ output is a logical OR of the associated D_ input pin and the associated HighO_ bit. In DI modes, the associated HighO_ bit is ignored. In DO modes, the DOI_ output is high-impedance when the associated $V_{DD_}$ falls below the undervoltage-lockout threshold, but the HighO_ bit is not reset. The HighO_ bit is reset when the internal register supply voltage (V_{INT}) is below the V_{TUV_INT} threshold.
HighO3	2	0: DOI3 if HS mode switch = open, or PP mode driver = GND 1: DOI3 if HS mode switch = closed, or PP mode driver = V_{DD3}
HighO2	1	0: DOI2 if HS mode switch = open, or PP mode driver = GND 1: DOI2 if HS mode switch = closed, or PP mode driver = V_{DD2}
HighO1	0	0: DOI1 if HS mode switch = open, or PP mode driver = GND 1: DOI1 if HS mode switch = closed, or PP mode driver = V_{DD1}

SetLED (0x01)

BIT	7	6	5	4	3	2	1	0
Field	SLED4	SLED3	SLED2	SLED1	FLED4	FLED3	FLED2	FLED1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
SLED4	7	0: Turn off SLED4 (Status LED for DOI4) 1: Turn on SLED4 (Status LED for DOI4) The SLEDSet bit in the Config1 register determines the operating mode for this register. If SLEDSet bit = 0, staus LEDs are controlled directly by the MAX14906. If SLEDSet bit = 1, status LEDs are controlled by SLED_ bits.
SLED3	6	0: Turn off SLED3 (Status LED for DOI3) 1: Turn on SLED3 (Status LED for DOI3)
SLED2	5	0: Turn off SLED2 (Status LED for DOI2) 1: Turn on SLED2 (Status LED for DOI2)
SLED1	4	0: Turn off SLED1 (Status LED for DOI1) 1: Turn on SLED1 (Status LED for DOI1)

BITFIELD	BITS	DESCRIPTION
FLED4	3	0: Turn off FLED4 (Fault LED for DOI4) 1: Turn on FLED4 (Fault LED for DOI4) The FLEDSet bit in the Config1 register determines the operating mode for this register. If FLEDSet bit = 0, fault LEDs are controlled directly by the MAX14906. If FLEDSet bit = 1, fault LEDs are controlled by FLED_ bits.
FLED3	2	0: Turn off FLED3 (Fault LED for DOI3) 1: Turn on FLED3 (Fault LED for DOI3)
FLED2	1	0: Turn off FLED2 (Fault LED for DOI2) 1: Turn on FLED2 (Fault LED for DOI2)
FLED1	0	0: Turn off FLED1 (Fault LED for DOI1) 1: Turn on FLED1 (Fault LED for DOI1)

DoiLevel (0x02)

BIT	7	6	5	4	3	2	1	0
Field	SafeDemagF4	SafeDemagF3	SafeDemagF2	SafeDemagF1	DoiLevel4/VDDOKFault4	DoiLevel3/VDDOKFault3	DoiLevel2/VDDOKFault2	DoiLevel1/VDDOKFault1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
SafeDemagF4	7	0: Normal operating conditions 1: Thermal Overload on DOI4 during SafeDemag. This fault is always latched and never masked.
SafeDemagF3	6	0: Normal operating conditions 1: Thermal Overload on DOI3 during SafeDemag. This fault is always latched and never masked.
SafeDemagF2	5	0: Normal operating conditions 1: Thermal Overload on DOI2 during SafeDemag. This fault is always latched and never masked.
SafeDemagF1	4	0: Normal operating conditions 1: Thermal Overload on DOI1 during SafeDemag. This fault is always latched and never masked.
DoiLevel4/ VDDOKFault4	3	Functionality controlled by the VDDFaultSel bit in the ConfigDI register: If VDDFaultSel = 0, reports DOI4 logic level in DI and DO modes. If VDDFaultSel = 1, reports a VDDOK bit fault for the V_{DD4} supply. VDDOKFault_ bits are set when per-channel VDDOK condition is not met ($V_{DD_}$ thresholds are controlled by the VDDOnThr bit in the Config2 register). This fault is always latched. VDDOKFault_ bits affect the SupplyErr fault bit in the Interrupt register if the VDDFaultDis bit in the ConfigDI register is not set. It also asserts the $\overline{FAULT}$ pin if not masked by the SupplyErrM bit in the Mask register.
DoiLevel3/ VDDOKFault3	2	If VDDFaultSel = 0, reports DOI3 logic level in DI and DO modes. If VDDFaultSel = 1, reports a VDDOK bit fault for the V_{DD3} supply.
DoiLevel2/ VDDOKFault2	1	If VDDFaultSel = 0, reports DOI2 logic level in DI and DO modes. If VDDFaultSel = 1, reports a VDDOK bit fault for the V_{DD2} supply.

BITFIELD	BITS	DESCRIPTION
DoiLevel1/ VDDOKFault1	0	If VDDFaultSel = 0, reports DOI1 logic level in DI and DO modes. If VDDFaultSel = 1, reports a VDDOK bit fault for the V_{DD1} supply.

Interrupt (0x03)

BIT	7	6	5	4	3	2	1	0
Field	ComErr	SupplyErr	DeMagFault	ShtVDDFault	AboveVDDFault	OWOffFault	CurrLim	OverLdFault
Reset	0b0	0b1	0b0	0b0	0b0	0b0	0b0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
ComErr	7	0: Normal operating conditions 1: Communication error detected ComErr is the logic OR result of an SPI watchdog error (if enabled), a SYNCH watchdog error (if enabled), an SPI CRC error (if enabled), and a number of SPI clock cycles error.
SupplyErr	6	0: Normal operating conditions 1: Supply error detected SupplyErr is the logical OR result of VDDOV_ bits, VDDOKFault_ faults (if enabled by the VDDFaultDis bit in the ConfigDI register), and the 6 supply error bits (VDD_UVLO, VDD_Warn, VDD_Low, V5_UVLO, VINT_UV, and LossGND) in the GlobalErr register.
DeMagFault	5	0: Normal operating conditions 1: SafeDemag fault detected on any DOI channel Logic OR result of per-channel SafeDemag faults. The per-channel faults can be identfied using the SafeDemagF_ bits in the DoiLevel register.
ShtVDDFault	4	0: Normal operating conditions 1: Short-to-V_{DD} fault detected on any DOI channel Logic OR result of per-channel short-to-V_{DD} faults. The per-channel faults can be identified using SHVDD_ bits in the ShtVDDChF register.
AboveVDDFault	3	0: Normal operating conditions 1: Above-V_{DD} fault detected on any DOI channel Logic OR result of per-channel above-V_{DD} faults. The per-channel faults can be identified using the AboveVDD_ bits in the OpnWirChF register.
OWOffFault	2	0: Normal operating conditions 1: Open-wire fault in off state detected on any DOI channel Logic OR result of per-channel open-wire faults. The per-channel faults can be identified using the OWOff_ bits in the OpnWirChF register.
CurrLim	1	0: Normal operating conditions 1: Overcurrent occured on any DOI channel Logic OR result of per-channel current limit faults. The per-channel faults can be identified using the CL_ bits in the OvrLdChF register.

BITFIELD	BITS	DESCRIPTION
OverLdFault	0	0: Normal operating conditions 1: Thermal overload occured on any DOI channel Logic OR result of per-channel thermal overload faults and the global thermal shutdown bit ThrmShutd. The per-channel faults can be identified using the OVL_ bits in the OvrLdChF register.

OvrLdChF (0x04)

BIT	7	6	5	4	3	2	1	0
Field	CL4	CL3	CL2	CL1	OVL4	OVL3	OVL2	OVL1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
CL4	7	0: Normal operating conditions 1: Current limit detected on DOI4 The FLatchEn bit in the Config1 register determines if this bit is real time (FLatchEn = 0) and cleared when the event disappears, or latched (FLatchEn = 1) and cleared when OvrLdChF register is read AND a current limiting condition is not present.
CL3	6	0: Normal operating conditions 1: Current limit detected on DOI3
CL2	5	0: Normal operating conditions 1: Current limit detected on DOI2
CL1	4	0: Normal operating conditions 1: Current limit detected on DOI1
OVL4	3	0: Normal operating conditions 1: Thermal overload is detected on DOI4 The FLatchEn bit in the Config1 register determines if this bit is real time (FLatchEn = 0) and cleared when the event disappears, or latched (FLatchEn = 1) and cleared when the OvrLdChF register is read AND a thermal overload condition is not present.
OVL3	2	0: Normal operating conditions 1: Thermal overload is detected on DOI3
OVL2	1	0: Normal operating conditions 1: Thermal overload is detected on DOI2
OVL1	0	0: Normal operating conditions 1: Thermal overload is detected on DOI1

OpnWirChF (0x05)

BIT	7	6	5	4	3	2	1	0
Field	AboveVDD4	AboveVDD3	AboveVDD2	AboveVDD1	OWOff4	OWOff3	OWOff2	OWOff1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
AboveVDD4	7	0: Normal operating conditions 1: Above-V_{DD} fault is detected on DOI4 The FLatchEn bit in the Config1 register determines if this bit is real time (FLatchEn = 0) and cleared when the event disappears, or latched (FLatchEn = 1) and cleared when OpnWirChF register is read AND the fault condition is not present. The Above-V_{DD} fault is always stretched by 10.7ms (typ), so once it is detected it is set for at least 10.7ms (typ).
AboveVDD3	6	0: Normal operating conditions 1: Above-V_{DD} fault is detected on DOI3
AboveVDD2	5	0: Normal operating conditions 1: Above-V_{DD} fault is detected on DOI2
AboveVDD1	4	0: Normal operating conditions 1: Above-V_{DD} fault is detected on DOI1
OWOff4	3	0: Normal operating conditions 1: Only active in digital output high-side mode. Open-wire fault is detected on DOI4 when the high-side switch is in the off state The FLatchEn bit in the Config1 register determines if this bit is real time (FLatchEn = 0) and cleared when the event disappears, or latched (FLatchEn = 1) and cleared when the OpnWirChF register is read AND the fault condition is not present.
OWOff3	2	0: Normal operating conditions 1: Only active in digital output high-side mode. Open-wire fault is detected on DOI3 when the high-side switch is in the off state
OWOff2	1	0: Normal operating conditions 1: Only active in digital output high-side mode. Open-wire fault is detected on DOI2 when the high-side switch is in the off state
OWOff1	0	0: Normal operating conditions 1: Only active in digital output high-side mode. Open-wire fault is detected on DOI1 when the high-side switch is in the off state

ShtVDDChF (0x06)

BIT	7	6	5	4	3	2	1	0
Field	VDDOV4	VDDOV3	VDDOV2	VDDOV1	SHVDD4	SHVDD3	SHVDD2	SHVDD1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
VDDOV4	7	0: Normal operating conditions 1: V_{DD4} supply is higher than the V_{DD_OVTH} threshold voltage (43.5V, typ) The FLatchEn bit in the Config1 register determines if this bit is real time (FLatchEn = 0) and cleared when the event disappears, or latched (FLatchEn = 1) and cleared when ShtVDDChF register is read AND the fault condition is not present.
VDDOV3	6	0: Normal operating conditions 1: V_{DD3} supply is higher than the V_{DD_OVTH} threshold voltage (43.5V, typ)

BITFIELD	BITS	DESCRIPTION
VDDOV2	5	0: Normal operating conditions 1: V_{DD2} supply is higher than the V_{DD_OVTH} threshold voltage (43.5V, typ)
VDDOV1	4	0: Normal operating conditions 1: V_{DD1} supply is higher than the V_{DD_OVTH} threshold voltage (43.5V, typ)
SHVDD4	3	0: Normal operating conditions 1: Only active in digital output high-side mode. Short-to-V_{DD} fault is detected on DOI4 when the high-side switch is in the off state. The FLatchEn bit in the Config1 register determines if this bit is real time (FLatchEn = 0) and cleared when the event disappears, or latched (FLatchEn = 1) and cleared when the ShtVDDChF register is read AND the fault condition is not present.
SHVDD3	2	0: Normal operating conditions 1: Only active in digital output high-side mode. Short-to-V_{DD} fault is detected on DOI3 when the high-side switch is in the off state.
SHVDD2	1	0: Normal operating conditions 1: Only active in digital output high-side mode. Short-to-V_{DD} fault is detected on DOI2 when the high-side switch is in the off state.
SHVDD1	0	0: Normal operating conditions 1: Only active in digital output high-side mode. Short-to-V_{DD} fault is detected on DOI1 when the high-side switch is in the off state.

GlobalErr (0x07)

These bits are always latched, and are cleared on read provided that the diagnostic error is no longer valid at the time of reading the register.

BIT	7	6	5	4	3	2	1	0
Field	WDogErr	LossGND	ThrmShutd	VDD_UVLO	VDD_Warn	VDD_Low	V5_UVLO	VINT_UV
Reset	0b0	0b0	0b0	0b1	0b1	0b1	0b1	0b1
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
WDogErr	7	0: Normal operating conditions 1: SPI or SYNCH watchdog timeout is detected This bit takes effect when the SPI or SYNCH watchdog functions are enabled using the WDTo[1:0] and SynchWDEn bits in the Config2 register. This bit is part of the logical OR result of the ComErr bit in the Interrupt register.
LossGND	6	0: Normal operating conditions 1: The MAX14906 detects loss of GND fault At power-on-reset, this bit can be 0 or 1. The microcontroller should ignore this initial setting until after it reads the GlobalErr register to clear this bit for normal operation. This bit is part of the logical OR result of the SupplyErr bit in the Interrupt register.

BITFIELD	BITS	DESCRIPTION
ThrmShutd	5	0: Normal operating conditions 1: The MAX14906 enters thermal shutdown This bit is part of the logical OR result of the OverLdFault bit in the Interrupt register.
VDD_UVLO	4	0: Normal operating conditions 1: V_{DD} supply falls under V_{DD_UVLO} threshold Set after power-on-reset. This bit can be cleared by reading the GlobalErr register when the V_{DD} voltage exceeds the V_{DD_UVLO} threshold. VDD_UVLO is part of the logic OR result of the SupplyErr bit in the Interrupt register if not disabled by the VDDFaultDis bit in the ConfigDI register.
VDD_Warn	3	0: Normal operating conditions 1: V_{DD} supply falls below V_{DD_WARN} threshold Set after power-on-reset. This bit can be cleared by reading the GlobalErr register when the V_{DD} voltage exceeds the V_{DD_WARN} threshold. VDD_Warm is part of the logic OR result of the SupplyErr bit in the Interrupt register if not disabled by the VDDFaultDis bit in the ConfigDI register. It also asserts $\overline{FAULT}$ pin if not masked by the VddOKM bit in the Mask register.
VDD_Low	2	0: Normal operating conditions 1: V_{DD} supply is below V_{DD_GOOD} threshold Set after power-on-reset. This bit can be cleared by reading the GlobalErr register when the V_{DD} voltage exceeds the V_{DD_GOOD} threshold. VDD_Low is part of the logic OR result of the SupplyErr bit in the Interrupt register if not disabled by the VDDFaultDis bit in the ConfigDI register. It also asserts $\overline{FAULT}$ pin if not masked by the VddOKM bit in the Mask register.
V5_UVLO	1	0: Normal operating conditions 1: V_5 voltage input falls under the V_{5_UVLO} threshold Set after power-on-reset. This bit can be cleared by reading the GlobalErr register when the V_5 voltage exceeds the V_{5_UVLO} threshold.
VINT_UV	0	0: Normal operating conditions 1: Set on initial power-up and when the internal supply to the registers falls to a level where the register contents are lost. This indicates that a power-on-reset has occurred and all register contents were reset. This bit can be cleared by reading the GlobalErr register when the internal register supply voltage (V_{INT}) exceeds the V_{TUV_INT} threshold.

OpnWrEn (0x08)

BIT	7	6	5	4	3	2	1	0
Field	GDrvEn4	GDrvEn3	GDrvEn2	GDrvEn1	OwOffEn4	OwOffEn3	OwOffEn2	OwOffEn1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
GDrvEn4	7	0: Disable gate driver on G4 if not used to reduce power consumption 1: Enable gate driver for external pMOS transistor on G4 pin

BITFIELD	BITS	DESCRIPTION
GDrvEn3	6	0: Disable gate driver on G3 if not used to reduce power consumption 1: Enable gate driver for external pMOS transistor on G3 pin
GDrvEn2	5	0: Disable gate driver on G2 if not used to reduce power consumption 1: Enable gate driver for external pMOS transistor on G2 pin
GDrvEn1	4	0: Disable gate driver on G1 if not used to reduce power consumption 1: Enable gate driver for external pMOS transistor on G1 pin
OwOffEn4	3	0: Disable the pullup current source and open-wire detection on DOI4 1: Enable open-wire detection on DOI4 in DO high-side mode, off state
OwOffEn3	2	0: Disable the pullup current source and open-wire detection on DOI3 1: Enable open-wire detection on DOI3 in DO high-side mode, off state
OwOffEn2	1	0: Disable the pullup current source and open-wire detection on DOI2 1: Enable open-wire detection on DOI2 in DO high-side mode, off state
OwOffEn1	0	0: Disable the pullup current source and open-wire detection on DOI1 1: Enable open-wire detection on DOI1 in DO high-side mode, off state

ShtVDDEn (0x09)

BIT	7	6	5	4	3	2	1	0
Field	VDDOVEn4	VDDOVEn3	VDDOVEn2	VDDOVEn1	ShVddEn4	ShVddEn3	ShVddEn2	ShVddEn1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
VDDOVEn4	7	0: Disable V_{DD} OVLO detection on V_{DD4} 1: Enable V_{DD} OVLO detection (43.5V, typ) on V_{DD4}
VDDOVEn3	6	0: Disable V_{DD} OVLO detection on V_{DD3} 1: Enable V_{DD} OVLO detection (43.5V, typ) on V_{DD3}
VDDOVEn2	5	0: Disable V_{DD} OVLO detection on V_{DD2} 1: Enable V_{DD} OVLO detection (43.5V, typ) on V_{DD2}
VDDOVEn1	4	0: Disable V_{DD} OVLO detection on V_{DD1} 1: Enable V_{DD} OVLO detection (43.5V, typ) on V_{DD1}
ShVddEn4	3	0: Disable short-to-V_{DD} detection on DOI4 1: Enable short-to-V_{DD} detection on DOI4
ShVddEn3	2	0: Disable short-to-V_{DD} detection on DOI3 1: Enable short-to-V_{DD} detection on DOI3
ShVddEn2	1	0: Disable short-to-V_{DD} detection on DOI2 1: Enable short-to-V_{DD} detection on DOI2
ShVddEn1	0	0: Disable short-to-V_{DD} detection on DOI1 1: Enable short-to-V_{DD} detection on DOI1

Config1 (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	LEDCurrLim	FLatchEn	FilterLong	FFilterEn	FLEDStretch[1:0]		SLEDSet	FLEDSet
Reset	0b0	0b1	0b0	0b1	0b00		0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
LEDCurrLim	7	If FLEDSet = 0, fault LEDs are controlled by internal FLED logic. LEDCurrLim controls whether fault LEDs signaling current limit faults. 0: Disable fault LEDs (FLEDs) signaling current limit 1: Enable fault LEDs (FLEDs) signaling current limit If FLEDSet = 1, fault LEDs are controlled by SetLED register.
FLatchEn	6	0: Disable latching of diagnostic fault bits in the OvrLdChF, OpnWirChF, and ShtVDDChF registers 1: Enable latching of diagnostic fault bits in the OvrLdChF, OpnWirChF, and ShtVDDChF registers Faults in GlobalErr register are always latched regardless of the FlatchEn bit setting. SafeDemagF_ and VDDOKFault_ faults are always latched too. When the fault LEDs are controlled internally (FLEDSet = 0), the LED on-time is not affected by this bit, but has a minimum on-time defined by the FLEDStrech[1:0] bits. The fault LEDs are turned off when the faults disappear and minimum LED on-time expires as defined by the FLEDStrech[1:0] bits.
FilterLong	5	0: To select regular blanking time (4ms, typ) for diagnostic fault bits, OWOff_ and SHVDD_ 1: To select long blanking time (8ms, typ) for diagnostic fault bits, OWOff_ and SHVDD_ This bit also affects the fault LEDs (FLEDs) on-time when controlled internally (FLEDSet = 0).
FFilterEn	4	0: Disable blanking and filtering of the SHVDD_ and OWOff_ diagnostic bits. In this mode, open-wire and short-to-V_{DD} diagnostics are real-time (only filtered by a 68µs (typ) filter) and any additional filtering is left to application software 1: Enable blanking and filtering of the SHVDD_ and OWOff_ diagnostic bits When the fault LEDs (FLEDs) are controlled internally (FLEDSet = 0), open-wire and short-to-V_{DD} diagnostics always use filtering and cannot be disabled by the FFilterEn bit.
FLEDStretch	3:2	The FLEDStretch bits select the minimum on-time for the fault LEDs (FLEDs) when they are controlled internally (FLEDSet = 0), so the user can visually see short events. 00: Disable minimum fault LED (FLED) on-time 01: Minimum fault LED (FLED) on-time = 1s (typ) 10: Minimum fault LED (FLED) on-time = 2s (typ) 11: Minimum fault LED (FLED) on-time = 3s (typ)
SLEDSet	1	0: All four status LEDs are controlled by the DOI1 to DOI4 status 1: All four status LEDs are controlled by the SLED_ bits in the SetLED register
FLEDSet	0	0: All four fault LEDs are controlled by the DOI1 to DOI4 fault diagnostics 1: All four fault LEDs are controlled by the FLED_ bits in the SetLED register Internal fault diagnostics include (if enabled): SafeDemagF_, SHVDD_, VDDOV_, OWOff_, AboveVDD_, CL_, OVL_, VDDOKFault_.

Config2 (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	WDTo[1:0]		OWOffCs[1:0]		ShtVddThr[1:0]		SynchWDEn	VDDOnThr
Reset	0b00		0b00		0b00		0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
WDTo	7:6	00: Disable SPI Watchdog Status and SPI Watchdog Timeout 01: Enable SPI Watchdog Status, set SPI and SYNCH Watchdog Timeout to 200ms (typ) 10: Enable SPI Watchdog Status, set SPI and SYNCH Watchdog Timeout to 600ms (typ) 11: Enable SPI Watchdog Status, set SPI and SYNCH Watchdog Timeout to 1.2s (typ) When the SPI watchdog is disabled, the SYNCH watchdog is configured by the SynchWDEn bit and the SYNCH watchdog timeout is set to 600ms (typ).
OWOffCs	5:4	The OWOffCs[1:0] bits select the pullup current used for the open-wire and short-to-V_{DD} detection when the switch is in the off state: 00: Set open-wire and short-to-V_{DD} detection current to 60µA (typ) 01: Set open-wire and short-to-V_{DD} detection current to 100µA (typ) 10: Set open-wire and short-to-V_{DD} detection current to 300µA (typ) 11: Set open-wire and short-to-V_{DD} detection current to 600µA (typ)
ShtVddThr	3:2	00: Set threshold voltage for short-to-V_{DD} detection to 9V (typ) 01: Set threshold voltage for short-to-V_{DD} detection to 10V (typ) 10: Set threshold voltage for short-to-V_{DD} detection to 12V (typ) 11: Set threshold voltage for short-to-V_{DD} detection to 14V (typ)
SynchWDEn	1	0: Disable the SYNCH Watchdog Status and Timeout 1: Enable the SYNCH Watchdog Status and Timeout The SYNCH watchdog timeout is defined by the WDTo[1:0] bits if the SPI watchdog is enabled. When WDTo[1:0] = 00 (SPI watchdog disabled), the SYNCH watchdog timeout is 600ms (typ) if enabled.
VDDOnThr	0	0: Disable higher voltage thresholds for V_{DD} and $V_{DD_}$ undervoltage monitoring 1: Enable higher voltage thresholds for V_{DD} and $V_{DD_}$ undervoltage monitoring $\overline{VDDOK}$ pin is asserted low and DOI_ channels automatically turn on when V_{DD} and $V_{DD_}$ rise above the thresholds. See the Power-Up and Undervoltage Lcokout section for details. The VDDOnThr bit affects per-channel VDDOKFault_ bits in the DoiLevel register when VDDFaultSel is set to 1.

ConfigDI (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	Typ2Di	Reserved	VDDFaultDis	VDDFaultSel	AboveVDDProtEn	OVLStretchEn	OVLBlank[1:0]	
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b00	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION
Typ2Di	7	0: Select IEC 61131-2 Type 1 and 3 in digital input mode 1: Select IEC 61131-2 Type 2 in digital input mode
Reserved	6	Reserved. Default value is 0.
VDDFaultDis	5	0: Enable all V_{DD} and $V_{DD_}$ voltage level monitoring faults (VDD_UVLO, VDD_Warn, VDD_Low and VDDOKFault_) to be the source of the logic OR result of the SupplyErr bit in the Interrupt register 1: Mask all V_{DD} and $V_{DD_}$ voltage level monitoring faults (VDD_UVLO, VDD_Warn, VDD_Low and VDDOKFault_) to be the source of the logic OR result of the SupplyErr bit in the Interrupt register
VDDFaultSel	4	0: Bits[3:0] in the DoiLevel register are per-channel DOI_ pin logic level 1: Bits[3:0] in DoiLevel register are per-channel $\overline{VDDOK}$ fault diagnostics for $V_{DD_}$ supply When VDDFaultSel = 0, the per-channel VDDOKFault_ bits are not mapped to the SupplyErr bit in the Interrupt register; hence, VDDOKFault_ bits do not generate an interrupt on the $\overline{FAULT}$ pin.
AboveVDDProtEn	3	0: Disable Above-V_{DD} protection 1: Enable Above-V_{DD} protection. External pMOS transistors on G_ pins are turned-off when Above-V_{DD} fault is detected on DOI_ pins
OVLStretchEn	2	0: Disable a 100ms (typ) minimum delay time to avoid channel thermal overload faults (OVL_ bits in the OvrLdChF register) toggling on and off when turning on a cold incandescent lamp 1: Enable a 100ms (typ) minimum delay time to avoid channel thermal overload faults (OVL_ bits in the OvrLdChF register) toggling on and off when turning on a cold incandescent lamp
OVLBlank	1:0	These bits select the banking time for the OVL_ diagnostic bits in the OvrLdChF register and apply to all DOI_ channels no matter they are on or off. 00: Disable the blanking time for the OVL_ diagnostic bits 01: Set the OVL_ blanking time to 8ms (typ) 10: Set the OVL_ blanking time to 50ms (typ) 11: Set the OVL_ blanking time to 300ms (typ)

ConfigDO (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	DoMode4[1:0]		DoMode3[1:0]		DoMode2[1:0]		DoMode1[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
DoMode4	7:6	The DoMode4[1:0] bits select the digital output operating mode for DOI4. 00: High-side 01: High-side with 2x inrush current for t_{INRUSH} time (see CL4[1:0] bits for details) 10: Active-clamp push-pull 11: Simple push-pull
DoMode3	5:4	The DoMode3[1:0] bits select the digital output operating mode for DOI3. 00: High-side 01: High-side with 2x inrush current for t_{INRUSH} time (see CL3[1:0] bits for details) 10: Active-clamp push-pull 11: Simple push-pull
DoMode2	3:2	The DoMode2[1:0] bits select the digital output operating mode for DOI2. 00: High-side 01: High-side with 2x inrush current for t_{INRUSH} time (see CL2[1:0] bits for details) 10: Active-clamp push-pull 11: Simple push-pull
DoMode1	1:0	The DoMode1[1:0] bits select the digital output operating mode for DOI1. 00: High-side 01: High-side with 2x inrush current for t_{INRUSH} time (see CL1[1:0] bits for details) 10: Active-clamp push-pull 11: Simple push-pull

CurrLim (0x0E)

BIT	7	6	5	4	3	2	1	0
Field	CL4[1:0]		CL3[1:0]		CL2[1:0]		CL1[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
CL4	7:6	The CL4[1:0] bits set the current limit for DOI4 high-side transistor 00: Current Limit = 600mA (typ), t_{INRUSH} = 20ms (typ) 01: Current Limit = 130mA (typ), t_{INRUSH} = 50ms (typ) 10: Current Limit = 300mA (typ), t_{INRUSH} = 40ms (typ) 11: Current Limit = 1.2A (typ), t_{INRUSH} = 10ms (typ)
CL3	5:4	The CL3[1:0] bits set the current limit for DOI3 high-side transistor 00: Current Limit = 600mA (typ), t_{INRUSH} = 20ms (typ) 01: Current Limit = 130mA (typ), t_{INRUSH} = 50ms (typ) 10: Current Limit = 300mA (typ), t_{INRUSH} = 40ms (typ) 11: Current Limit = 1.2A (typ), t_{INRUSH} = 10ms (typ)

BITFIELD	BITS	DESCRIPTION
CL2	3:2	The CL2[1:0] bits set the current limit for DOI2 high-side transistor 00: Current Limit = 600mA (typ), t_{INRUSH} = 20ms (typ) 01: Current Limit = 130mA (typ), t_{INRUSH} = 50ms (typ) 10: Current Limit = 300mA (typ), t_{INRUSH} = 40ms (typ) 11: Current Limit = 1.2A (typ), t_{INRUSH} = 10ms (typ)
CL1	1:0	The CL1[1:0] bits set the current limit for DOI1 high-side transistor 00: Current Limit = 600mA (typ), t_{INRUSH} = 20ms (typ) 01: Current Limit = 130mA (typ), t_{INRUSH} = 50ms (typ) 10: Current Limit = 300mA (typ), t_{INRUSH} = 40ms (typ) 11: Current Limit = 1.2A (typ), t_{INRUSH} = 10ms (typ)

Mask (0x0F)

Disabling the mask (setting the bit = 0) enables the fault source to assert the $\overline{FAULT}$ pin output.

Enabling the mask (setting the bit = 1) disables the fault source to assert the $\overline{FAULT}$ pin output.

BIT	7	6	5	4	3	2	1	0
Field	ComErrM	SupplyErrM	VddOKM	ShtVddM	AboveVDDM	OWOffM	CurrLimM	OverLdM
Reset	0b1	0b0	0b1	0b1	0b1	0b1	0b1	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
ComErrM	7	0: Disable masking of watchdog error and SPI/CRC error bits on the $\overline{FAULT}$ pin 1: Enable masking of watchdog error and SPI/CRC error bits on the $\overline{FAULT}$ pin Independent of this bit setting, the error conditions are flagged using the ComErr bit in the Interrupt register and the GLOBF bit in the SDO data packet.
SupplyErrM	6	0: Disable masking of supply errors on the $\overline{FAULT}$ pin 1: Enable masking of supply errors on the $\overline{FAULT}$ pin Independent of this bit, the error conditions are flagged using the SupplyErr bit in the Interrupt register and the GLOBF bit in the SDO data packet.
VddOKM	5	0: Disable masking of VDD_Low and VDD_Warn errors on the $\overline{FAULT}$ pin 1: Enable masking of VDD_Low and VDD_Warn errors on the $\overline{FAULT}$ pin The SupplyErr bit is always active and not affected by this bit setting. See Figure 6 for details.
ShtVddM	4	0: Disable masking of short-to-V_{DD} error on the $\overline{FAULT}$ pin 1: Enable masking of short-to-V_{DD} error on the $\overline{FAULT}$ pin If the short-to-V_{DD} detection is enabled in the ShtVDDEn register, short-to-V_{DD} conditions are signaled in the SHVDD_ bits in the ShtVDDChF register, and the SHTVDD bit in the SPI SDO data.

BITFIELD	BITS	DESCRIPTION
AboveVDDM	3	0: Disable masking of above-V_{DD} error on the $\overline{FAULT}$ pin 1: Enable masking of above-V_{DD} error on the $\overline{FAULT}$ pin If the above-V_{DD} detection is enabled in the ShtVDDEn register, above-V_{DD} conditions are signaled in the AboveVDD_ bits in the OpnWirChF register, and the AbvVDD bit in the SPI SDO data.
OWOffM	2	0: Disable masking of open-wire in off-state error on the $\overline{FAULT}$ pin 1: Enable masking of open-wire in off-state error on the $\overline{FAULT}$ pin If the open-wire detection in off state is enabled by the OwOffEn_ bits in the OpnWrEn register, the open-wire detection in off state is signaled by the OWOff_ bits in the OpnWirChF register and the OWOffF bit in the SPI SDO data.
CurrLimM	1	0: Disable masking of current limit error on the $\overline{FAULT}$ pin 1: Enable masking of current limit error on the $\overline{FAULT}$ pin Independent of this bit setting, current limit conditions are always signaled by the CL_ bits in the OvrLdChF register and the OvrCurr bit in the SPI SDO data.
OverLdM	0	0: Disable masking of thermal overload error on the $\overline{FAULT}$ pin 1: Enable masking of thermal overload error on the $\overline{FAULT}$ pin Independent of this bit setting, thermal overload faults are always signaled by the OVL_ bits in the OvrLdChF register and the OvldF bit in the SPI SDO data.

Applications Information

Configurable DO/DI

The Typical Application Circuit: *Quad DO/DI with Each Channel Fully IEC 61131-2 Compliant* illustrates a configurable digital-output/digital-input circuit.

The external pMOS transistors protect the MAX14906 from $V_{DD_}$ reverse polarity miswiring on the $V_{DD_}$ supplies. In DI mode, the external pMOS transistor is permanently turned off through the gate output (G_), allowing DOI_ input to be higher than the $V_{DD_}$ supply voltage. When the DOI_ voltage is lower than the $V_{DD_}$ voltage minus one diode drop, the MAX14906 is powered through $V_{DD_}$ through the body diode of the external pMOS transistor.

Power Supply Sequencing

The MAX14906 is flexible, and does not require any specific power-up sequence for its supplies.

At power-up, the default register settings configure the device into digital output high-side mode. Thus, if the D_ logic pins are high at power-up, for example due to pullup resistors, the associated DOI_ outputs switch on if the EN and the SYNCH logic inputs also are high.

To avoid the DOI_ switches turning on at power-up, the following should be considered:

- If the device is operated in serial mode, connect all D_ pins low.
- When operated in pin-control mode, during which the D_ logic pins are used, ensure that either the EN, the SYNCH, or the D_ pins are logic low at power-up.

External V_5 Power

The MAX14906 requires a 5V power supply on V_5 and can be powered either by the internal 5V linear regulator if REGEN is unconnected; or can be powered by an external 5V supply. If powering V_5 from an external regulator, connect REGEN to GND.

Driving Capacitive Loads

When charging and discharging purely capacitive loads with a push-pull driver, the driver dissipates power that is proportional to the switching frequency. The power can be estimated by

$$P_D = C_L \times V_{DD_}^2 \times f$$

where,

C_L = Load capacitance

$V_{DD_}$ = Supply voltage

f = Switching frequency in Hz.

For example, a pure 10nF capacitive load switching at 100kHz with a 24V supply would result in approximately 580mW dissipation in the push-pull driver. Hence the capacitors connected to DOI_ for EMC purposes should be held with as small a capacitance as possible, if high switching rates are expected. Resistance placed in series with the capacitance reduces the power dissipation in the driver.

Driving Inductive Loads

When an inductive load is turned off by opening the high-side switch, the DOI_ pins go to a negative voltage in both high-side and active-clamp push-pull modes. The MAX14906 features an internal active clamp that clamps inductive energy at -55V (typ) relative to $V_{DD_}$, which allows inductive load currents to decay quickly.

The inductive energy is dissipated in the active clamp. If the inductance is large and/or the inductive load current is large, the clamping energy is high. If this dissipation energy is too high, it could cause damage to the IC. The MAX14906 features Maxim's patented SafeDemag technology, allowing unlimited inductive energy to be demagnetized for load currents up to 600mA. Refer to *Application Note 6307* for details. For load currents above 600mA, the inductive clamping

energy must be limited to 0.3 Joule. For higher inductive clamping energies, an external Zener/TVS clamping diode must be used on the DOI_ pin. Ensure that the external TVS/zener clamps at a voltage (V_Z) lower than the internal active clamp (V_{CL}) and that the external zener diode is able to dissipate the clamping energy.

Reverse Current into DOI

If current flows into a DOI_ pin, the device heats up due to the internal current that flows through the device from $V_{DD_}$ to PGND. The internal current is proportional to the reverse input current flowing into DOI_. The allowed reverse current depends on $V_{DD_}$ voltage, the ambient temperature, and the package thermal resistance (θ_{JA}). At an ambient temperature of 25°C, limit the reverse current into a DOI_ pin to 1A at $V_{DD_}$ = 36V and 2A at $V_{DD_}$ = 24V.

To protect the device from reverse currents, connect an external pMOS transistor in series to the $V_{DD_}$ supplies (see the *Typical Application Circuits* for details), and turn on the transistors by setting the GDrvEn_ bits in the OpnWrEn register to high.

The MAX14906 has an above-V_{DD} comparator. After an above-V_{DD} fault is detected and a 200µs (typ) debounce time, the AboveVDD_ bits in the OpnWirChF register are set. When the AboveVDD_ faults are asserted and the device is in digital output mode, the external pMOS transistors are turned off and high-side switches are turned off if the above-V_{DD} protection feature is turned on (AboveVDDProtEn = 1). AboveVDD_ faults are latched and need to be cleared before the high-side switch can be turned on.

When a DOI_ channel is in digital input mode including the high-impedance low-leakage mode, the external pMOS transistor is always off and G_ pin is shorted to $V_{DD_}$. In this case, the current consumption is very low and the channel is supplied through the external pMOS FET body diode.

When the GDrvEn_ bits are 0, the external pMOS transistor gate drivers (G_) are always off to save current consumption. The device is not protected for reverse current. If the above-V_{DD} faults are detected, the AboveVDD_ bits are set after 200µs (typ) debounce time, but no actions are taken on the DOI_ channels.

Surge Protection

Without external protection devices, the DOI_ channels are protected against negative 1kV surges per IEC 61000-4-5 (42Ω/0.5µF). A suppressor/TVS diode should be applied between V_{DD} and GND to clamp positive surge transients on the DOI_ pins. The TVS standoff voltage should be higher than the maximum operating voltage of the equipment while the breakdown voltage should be below 65V.

ESD Protection

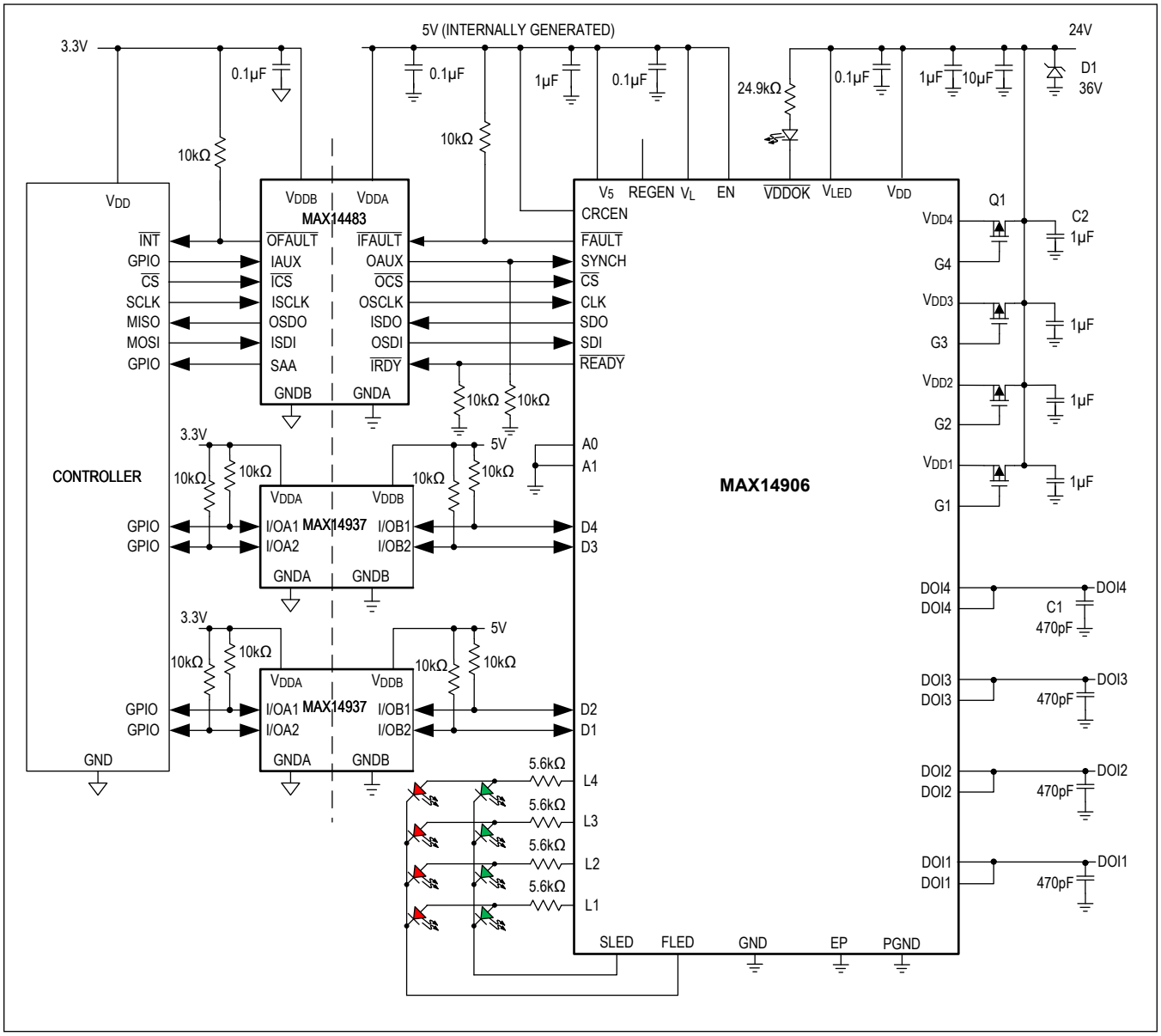
To protect the MAX14906 from an electrostatic discharge (ESD) event per IEC 61000-4-2, an additional 470pF is recommended on each DOI_ to PGND. Also, an additional 1µF bypass capacitor should be placed as close to each $V_{DD_}$ pin as possible.

Table 8. Recommended Components

COMPONENT	DESCRIPTION	REQUIRED/RECOMMENDED/OPTIONAL
C1	470pF, 100V, ceramic capacitor on the DOI_ pins	Required (ESD)
C2	1µF, 100V, ceramic capacitor on the $V_{DD_}$ pins	Required (ESD)
D1	Unidirectional TVS diode (SMBJ36A-E3) on the V_{DD} pin	Required (Surge)
Q1	P-Channel Transistor (NTTFS5116PLTAG) on the $V_{DD_}$ pins	Reverse Current Protection

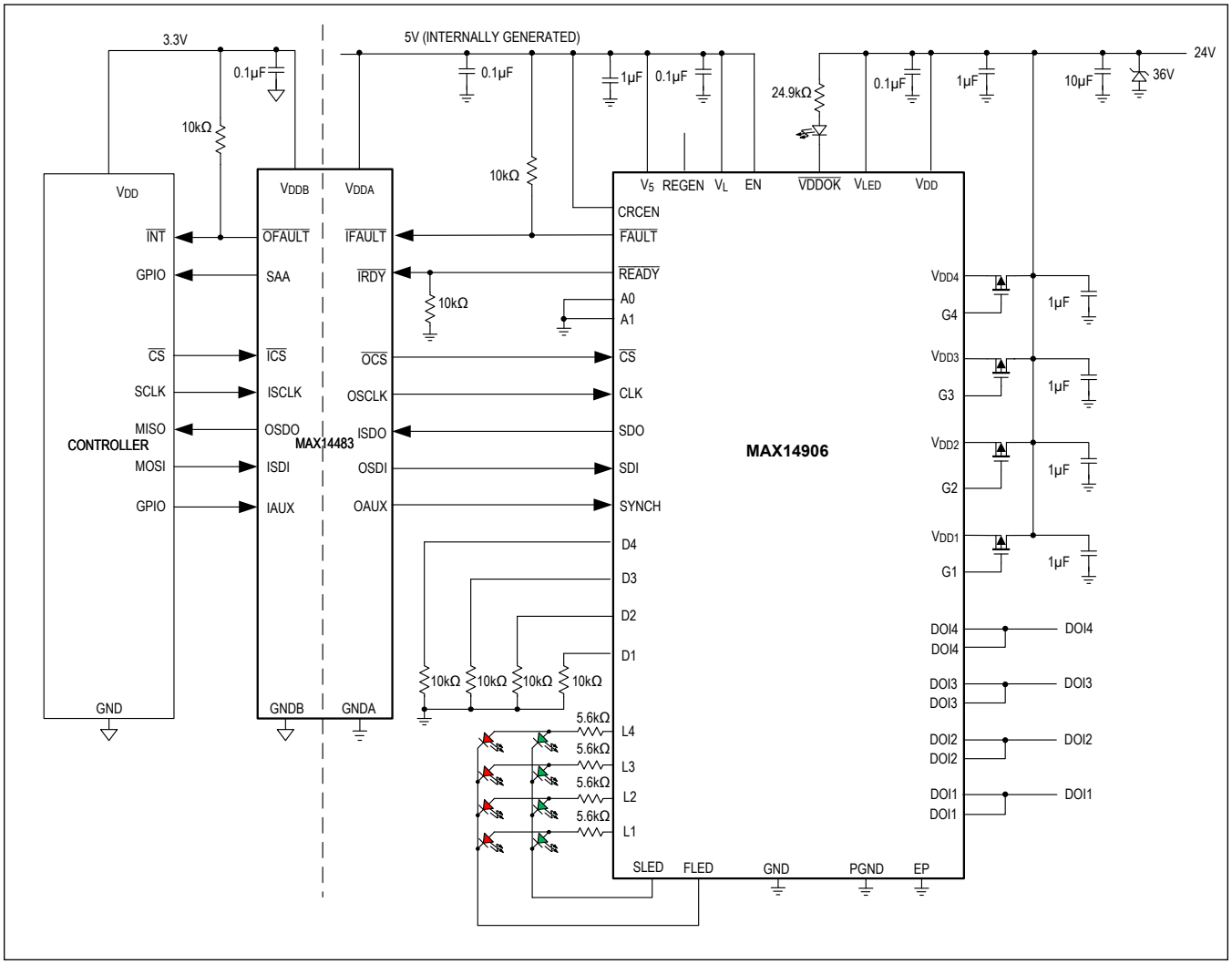
Typical Application Circuit

Quad DO/DI with Each Channel Fully IEC 61131-2 Compliant



Typical Application Circuit (continued)

Quad Isolated Industrial Digital Output, Digital Input



Ordering Information

PART NUMBER	TEMP. RANGE	PIN PACKAGE	LEAD PITCH
MAX14906ATM+	-40°C to +125°C	7 x 7 TQFN-48	0.5mm
MAX14906ATM+T	-40°C to +125°C	7 x 7 TQFN-48	0.5mm

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/20	Initial release	—
1	2/20	Updated the SetOUT (0x00) Register	37

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