MAX1452

Low-Cost Precision Sensor Signal Conditioner

General Description

The MAX1452 is a highly integrated analog-sensor signal processor optimized for industrial and process control applications utilizing resistive element sensors. The MAX1452 provides amplification, calibration, and temperature compensation that enables an overall performance approaching the inherent repeatability of the sensor. The fully analog signal path introduces no quantization noise in the output signal while enabling digitally controlled trimming with the integrated 16-bit DACs. Offset and span are calibrated using 16-bit DACs, allowing sensor products to be truly interchangeable.

The MAX1452 architecture includes a programmable sensor excitation, a 16-step programmable-gain amplifier (PGA), a 768-byte (6144 bits) internal EEPROM, four 16-bit DACs, an uncommitted op amp, and an on-chip temperature sensor. In addition to offset and span compensation, the MAX1452 provides a unique temperature compensation strategy for offset TC and FSOTC that was developed to provide a remarkable degree of flexibility while minimizing testing costs.

The MAX1452 is packaged for the commercial, industrial, and automotive temperature ranges in 16-pin SSOP/TSSOP and 24-pin TQFN packages.

Customization

Maxim can customize the MAX1452 for high-volume dedicated applications. Using our dedicated cell library of more than 2000 sensor-specific functional blocks, Maxim can quickly provide a modified MAX1452 solution. Contact Maxim for further information.

Applications

- Pressure Sensors
- Transducers and Transmitters
- Strain Gauges
- Pressure Calibrators and Controllers
- Resistive Elements Sensors
- Accelerometers
- Humidity Sensors

Outputs Supported

- 4–20mA
- 0 to +5V (Rail-to-Rail)
- +0.5V to +4.5V Ratiometric
- +2.5V to ±2.5V

Benefits and Features

- Single-Chip, Integrated Analog Signal Path Reduces Design Time and Saves Space in a Complete Precision Sensor Solution
  - Provides Amplification, Calibration, and Temperature Compensation
  - Fully Analog Signal Path
  - Accommodates Sensor Output Sensitivities from 4mV/V to 60mV/V
  - Single-Pin Digital Programming
  - No External Trim Components Required
  - 16-Bit Offset and Span Calibration Resolution
  - Supports Both Current and Voltage Bridge Excitation
  - Fast 150µs Step Response
  - On-Chip Uncommitted Op Amp
- On-Chip Lookup Table Supports Multipoint Calibration Temperature Correction Improving System Performance
- Secure-Lock™ Prevents Data Corruption
- Low 2mA Current Consumption Simplifies Power-Supply Design in 4–20mA Applications

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1452CAE+	0°C to +70°C	16 SSOP
MAX1452EAE+	-40°C to +85°C	16 SSOP
MAX1452AAE+	-40°C to +125°C	16 SSOP
MAX1452AUE+	-40°C to +125°C	16 TSSOP
MAX1452ATG+	-40°C to +125°C	24 TQFN-EP*
MAX1452C/D	0°C to +70°C	Dice**

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

***Dice are tested at T_A = +25°C, DC parameters only.*

Detailed Block Diagram and Pin Configurations appear at the end of data sheet.

Secure-Lock is a trademark of Maxim Integrated Products, Inc.

19-1829; Rev 5; 4/15

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Absolute Maximum Ratings

Supply Voltage, V_{DD} to V_{SS}.....-0.3V, +6V
Supply Voltage, V_{DD} to V_{DDF}.....-0.5V to +0.5V
All Other Pins.....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Short-Circuit Duration, FSOTC, OUT, BDR, AMPOUT.....Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin SSOP/TSSOP (derate 8.00mW/°C above +70°C)..640mW
24-Pin TQFN (derate 20.8mW/°C above +70°C).....1.67W

Operating Temperature:
MAX1452CAE+/MAX1452C/D.....0°C to +70°C
MAX1452EAE+.....-40°C to +85°C
MAX1452AAE+.....-40°C to +125°C
MAX1452AUE+.....-40°C to +125°C
MAX1452ATG+.....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = V_{DDF} = +5V, V_{SS} = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS						
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
EEPROM Supply Voltage	V_{DDF}		4.5	5.0	5.5	V
Supply Current	I_{DD}	(Note 1)		2.0	2.5	mA
Maximum EEPROM Erase/ Write Current	I_{DDFW}			30		mA
Maximum EEPROM Read Current	I_{DDFR}			12		mA
Oscillator Frequency	f_{OSC}		0.85	1	1.15	MHz
ANALOG INPUT						
Input Impedance	R_{IN}			1		MI
Input-Referred Offset Tempco		(Notes 2, 3)		P1		µV/°C
Input-Referred Adjustable Offset Range		Offset TC = 0 at minimum gain (Note 4)		P150		mV
Amplifier Gain Nonlinearity		Percent of +4V span, V_{OUT} = +0.5V to 4.5V		0.01		%
Common-Mode Rejection Ratio	CMRR	Specified for common-mode voltages between V_{SS} and V_{DD} (Note 2)		90		dB
Input Referred Adjustable FSO Range		(Note 5)		4 to 60		mV/V
ANALOG OUTPUT						
Differential Signal-Gain Range		Selectable in 16 steps		39 to 234		V/V
Differential Signal Gain		Configuration [5:2] 0000bin	34	39	46	V/V
		Configuration [5:2] 0001bin	47	52	59	
		Configuration [5:2] 0010bin	58	65	74	
		Configuration [5:2] 0100bin	82	91	102	
		Configuration [5:2] 1000bin	133	143	157	
Maximum Output-Voltage Swing		No load from each supply		0.02		V

Electrical Characteristics (continued)

(V_{DD} = V_{DDF} = +5V, V_{SS} = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-Voltage Low		I_{OUT} = 1mA sinking, T_A = T_{MIN} to T_{MAX}		0.100	0.20	V
Output-Voltage High		I_{OUT} = 1mA sourcing, T_A = T_{MIN} to T_{MAX}	4.75	4.87		V
Output Impedance at DC				0.1		Ω
Output Offset Ratio	ΔV_{OUT}/ ΔOffset		0.90	1.05	1.20	V/V
Output Offset TC Ratio	ΔV_{OUT}/ ΔOffset TC		0.9	1	1.2	V/V
Step Response and IC (63% Final Value)				150		µs
Maximum Capacitive Load				1		µF
Output Noise		DC to 1kHz (gain = minimum, source impedance = 5kΩ V_{DDF} filter)		0.5		mV_{RMS}
BRIDGE DRIVE						
Bridge Current	I_{BDR}	R_L = 1.7kΩ	0.1	0.5	2	mA
Current Mirror Ratio	AA	$R_{ISOURCE}$ = internal	10	12	14	A/A
V_{SPAN} Range (Span Code)		T_A = T_{MIN} to T_{MAX}	4000		C000	hex
DIGITAL-TO-ANALOG CONVERTERS						
DAC Resolution				16		Bits
ODAC Bit Weight	ΔV_{OUT}/ ΔCode	DAC reference = V_{DD} = +5.0V		76		µV/bit
OTCDAC Bit Weight	ΔV_{OUT}/ ΔCode	DAC reference = V_{BDR} = +2.5V		38		µV/bit
FSODAC Bit Weight	ΔV_{OUT}/ ΔCode	DAC reference = V_{DD} = +5.0V		76		µV/bit
FSOTCDAC Bit Weight	ΔV_{OUT}/ ΔCode	DAC reference = V_{BDR} = +2.5V		38		µV/bit
COARSE OFFSET DAC						
IRODAC Resolution		Including sign		4		Bits
IRODAC Bit Weight	ΔV_{OUT}/ ΔCode	Input referred, DAC reference = V_{DD} = +5.0V (Note 6)		9		mV/bit
FSOTC BUFFER						
Minimum Output-Voltage Swing		No load			V_{SS} + 0.1	V
Maximum Output-Voltage Swing		No load	V_{DD} - 1.0			V
Current Drive		V_{FSOTC} = +2.5V	-40		+40	µA
INTERNAL RESISTORS						
Current-Source Reference Resistor	R_{ISRC}			75		kΩ

Electrical Characteristics (continued)

(V_{DD} = V_{DDF} = +5V, V_{SS} = 0V, T_A = +25°C, unless otherwise noted.)

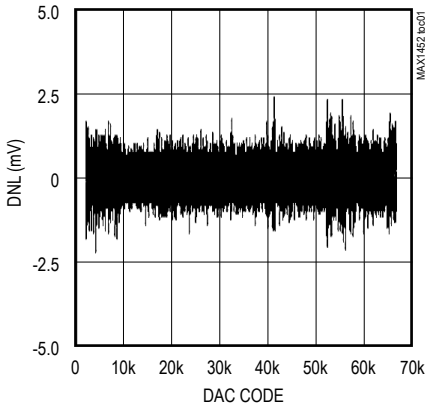
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Source Reference Resistor Temperature Coefficient	ΔR_{ISRC}			1300		ppm/°C
FSOTC Resistor	R_{FTC}			75		kΩ
FSOTC Resistor Temperature Coefficient	ΔR_{FTC}			1300		ppm/°C
TEMPERATURE-TO-DIGITAL CONVERTER						
Temperature ADC Resolution				8		Bits
Offset				P3		LSB
Gain				1.45		°C/bit
Nonlinearity				P0.5		LSB
Lowest Digital Output				00		hex
Highest Digital Output				AF		hex
UNCOMMITTED OP AMP						
Open-Loop Gain		R_L = 100kΩ		90		dB
Input Common-Mode Range			V_{SS}		V_{DD}	V
Output Swing		No load, T_A = T_{MIN} to T_{MAX}	V_{SS} + 0.02		V_{DD} - 0.02	V
Output-Voltage High		1mA source, T_A = T_{MIN} to T_{MAX}	4.85	4.90		V
Output-Voltage Low		1mA sink, T_A = T_{MIN} to T_{MAX}		0.05	0.15	V
Offset		V_{IN+} = +2.5V, unity-gain buffer	-20		+20	mV
Unity-Gain Bandwidth				2		MHz
EEPROM						
Maximum Erase/Write Cycles		(Note 7)		10k		Cycles
Minimum Erase Time		(Note 8)		6		ms
Minimum Write Time				100		µs

Note 1: Excludes sensor or load current.
Note 2: All electronics temperature errors are compensated together with sensors errors.
Note 3: The sensor and the MAX1452 must be at the same temperature during calibration and use.
Note 4: This is the maximum allowable sensor offset.
Note 5: This is the sensor's sensitivity normalized to its drive voltage, assuming a desired full span output of +4V and a bridge voltage range of +1.7V to +4.25V.
Note 6: Bit weight is ratiometric to V_{DD}.
Note 7: Programming of the EEPROM at room temperature is recommended.
Note 8: Allow a minimum of 6ms elapsed time before sending any command.

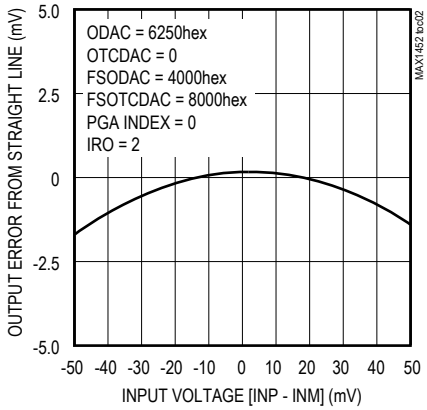
Typical Operating Characteristics

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

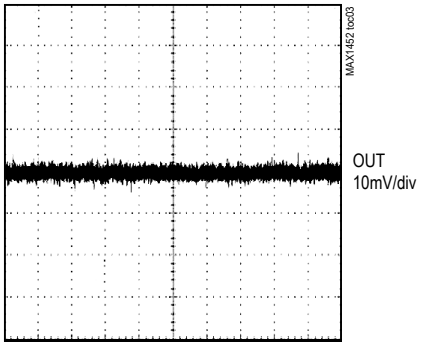
OFFSET DAC DNL



AMPLIFIER GAIN NONLINEARITY



OUTPUT NOISE



Pin Description

PIN		NAME	FUNCTION
SSOP/TSSOP	TQFN-EP		
1	1	ISRC	Bridge Drive Current Mode Setting
2	2	OUT	High ESD and Scan Path Output Signal. May need a 0.1µF capacitor, in noisy environments. OUT may be parallel connected to DIO.
3	3	V_{SS}	Negative Supply Voltage
4	4	INM	Bridge Negative Input. Can be swapped to INP by configuration register.
5	5	BDR	Bridge Drive
6	6	INP	Bridge Positive Input. Can be swapped to INM by configuration register.
7	7	V_{DD}	Positive Supply Voltage. Connect a 0.1µF capacitor from V_{DD} to V_{SS}.
—	8, 9, 13, 16, 20, 22, 23, 24	N.C.	No Connection. Not internally connected; leave unconnected (TQFN package only).
8	10	TEST	Internally Connected. Connect to V_{SS}.

Pin Description (continued)

PIN		NAME	FUNCTION
SSOP/TSSOP	TQFN-EP		
9	11	V_{DDF}	Positive Supply Voltage for EEPROM. Connect a 1µF capacitor from V_{DDF} to V_{SS}. Connect V_{DDF} to V_{DD} or for improved noise performance connect a 30Ω resistor to V_{DD}.
10	12	UNLOCK	Secure-Lock Disable. Allows communication to the device.
11	14	DIO	Digital Input Output. DIO allows communication with the device.
12	15	CLK1M	1MHz Clock Output. The output can be controlled by a configuration bit.
13	17	AMPOUT	Uncommitted Amplifier Output
14	18	AMP-	Uncommitted Amplifier Negative Input
15	19	AMP+	Uncommitted Amplifier Positive Input
16	21	FSOTC	Full Span TC Buffered Output
—	—	EP	Exposed Pad (TQFN Only). Internally connected; connect to V_{SS}.

Detailed Description

The MAX1452 provides amplification, calibration, and temperature compensation to enable an overall performance approaching the inherent repeatability of the sensor. The fully analog signal-path introduces no quantization noise in the output signal while enabling digitally controlled trimming with the integrated 16-bit DACs. Offset and span can be calibrated to within ±0.02% of span.

The MAX1452 architecture includes a programmable sensor excitation, a 16-step programmable-gain amplifier (PGA), a 768-byte (6144 bits) internal EEPROM, four 16-bit DACs, an uncommitted op amp, and an on-chip temperature sensor. The MAX1452 also provides a unique temperature compensation strategy for offset TC and FSOTC that was developed to provide a remarkable degree of flexibility while minimizing testing costs.

The customer can select from one to 114 temperature points to compensate their sensor. This allows the latitude to compensate a sensor with a simple first order linear correction or match an unusual temperature curve. Programming up to 114 independent 16-bit EEPROM locations corrects performance in 1.5°C temperature increments over a range of -40°C to +125°C. For sensors that exhibit a characteristic temperature performance, a select number of calibration points can be used with a number of preset values that define the temperature curve. In cases where the sensor is at a different temperature than the MAX1452, the MAX1452 uses the sensor bridge itself to provide additional temperature correction.

The single pin, serial Digital Input-Output (DIO) communication architecture and the ability to timeshare its activity with the sensor's output signal enables output sensing and calibration programming on a single line by parallel connecting OUT and DIO. The MAX1452 provides a Secure-Lock feature that allows the customer to prevent modification of sensor coefficients and the 52-byte user definable EEPROM data after the sensor has been calibrated. The Secure-Lock feature also provides a hardware override to enable factory rework and recalibration by assertion of logic high on the UNLOCK pin.

The MAX1452 allows complete calibration and sensor verification to be performed at a single test station. Once calibration coefficients have been stored in the MAX1452, the customer can choose to retest in order to verify performance as part of a regular QA audit or to generate final test data on individual sensors.

The MAX1452's low current consumption and the integrated uncommitted op amp enables a 4–20mA output signal format in a sensor that is completely powered from a 2-wire current loop. Frequency response can be user-adjusted to values lower than the 3.2kHz bandwidth by using the uncommitted op amp and simple passive components.

The MAX1452 (Figure 1) provides an analog amplification path for the sensor signal. It also uses an analog architecture for first-order temperature correction. A digitally controlled analog path is then used for nonlinear temperature correction. Calibration and correction is achieved by varying the offset and gain of a programmable-gain-amplifier (PGA) and by varying the sensor bridge excitation current

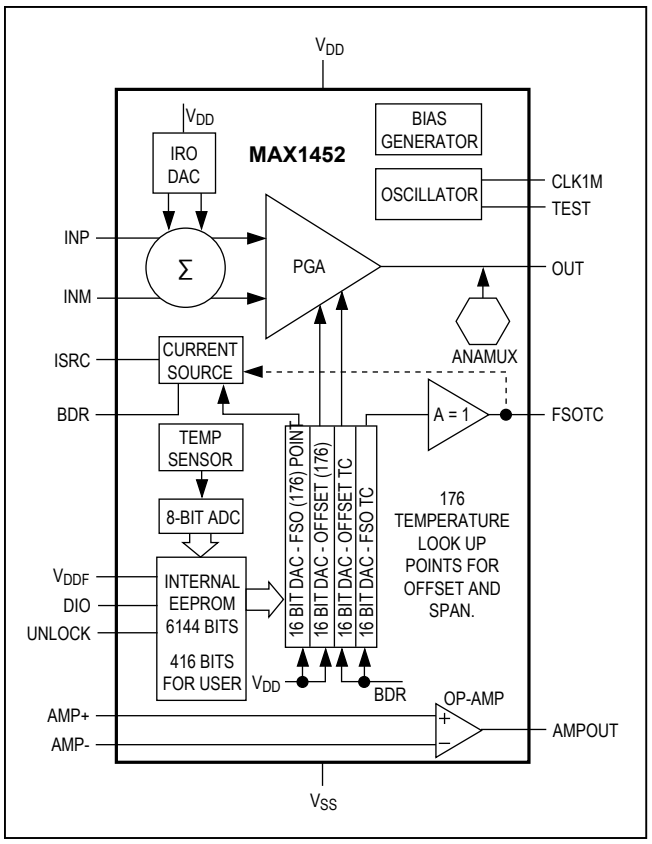


Figure 1. Functional Diagram

or voltage. The PGA utilizes a switched capacitor CMOS technology, with an input-referred offset trimming range of more than ±150mV with an approximate 3µV resolution (16 bits). The PGA provides gain values from 39V/V to 234V/V in 16 steps.

The MAX1452 uses four 16-bit DACs with calibration coefficients stored by the user in an internal 768 x 8 EEPROM (6144 bits). This memory contains the following information, as 16-bit wide words:

- Configuration Register
- Offset Calibration Coefficient Table
- Offset Temperature Coefficient Register
- FSO (Full-Span Output) Calibration Table
- FSO Temperature Error Correction Coefficient Register
- 52 bytes (416 bits) uncommitted for customer programming of manufacturing data (e.g., serial number and date)

Offset Correction

Initial offset correction is accomplished at the input stage of the signal gain amplifiers by a coarse offset setting. Final offset correction occurs through the use of a temperature indexed lookup table with 176 16-bit entries. The on-chip temperature sensor provides a unique 16-bit offset trim value from the table with an indexing resolution of approximately 1.5°C from -40°C to +125°C. Every millisecond, the on-chip temperature sensor provides indexing into the offset lookup table in EEPROM and the resulting value transferred to the offset DAC register. The resulting voltage is fed into a summing junction at the PGA output, compensating the sensor offset with a resolution of ±76µV (±0.0019% FSO). If the offset TC DAC is set to zero then the maximum temperature error is equivalent to one degree of temperature drift of the sensor, given the Offset DAC has corrected the sensor at every 1.5°C. The temperature indexing boundaries are outside of the specified *Absolute Maximum Ratings*. The minimum indexing value is 00hex corresponding to approximately -69°C. All temperatures below this value output the coefficient value at index 00hex. The maximum indexing value is AFhex, which is the highest lookup table entry. All temperatures higher than approximately 184°C output the highest lookup table index value. No indexing wraparound errors are produced.

FSO Correction

Two functional blocks control the FSO gain calibration. First, a coarse gain is set by digitally selecting the gain of the PGA. Second, FSO DAC sets the sensor bridge current or voltage with the digital input obtained from a temperature-indexed reference to the FSO lookup table in EEPROM. FSO correction occurs through the use of a temperature indexed lookup table with 176 16-bit entries. The on-chip temperature sensor provides a unique FSO trim from the table with an indexing resolution approaching one 16-bit value at every 1.5°C from -40°C to +125°C. The temperature indexing boundaries are outside of the specified *Absolute Maximum Ratings*. The minimum indexing value is 00hex corresponding to approximately -69°C. All temperatures below this value output the coefficient value at index 00hex. The maximum indexing value is AFhex, which is the highest lookup table entry. All temperatures higher than approximately 184°C output the highest lookup table index value. No indexing wraparound errors are produced.

Linear and Nonlinear Temperature Compensation

Writing 16-bit calibration coefficients into the offset TC and FSOTC registers compensates first-order temperature errors. The piezoresistive sensor is powered by a current source resulting in a temperature-dependent bridge voltage due to the sensor's temperature resistance coefficient (TCR). The reference inputs of the offset TC DAC and FSOTC DAC are connected to the bridge voltage. The DAC output voltages track the bridge voltage as it varies with temperature, and by varying the offset TC and FSOTC digital code a portion of the bridge voltage, which is temperature dependent, is used to compensate the first-order temperature errors.

The internal feedback resistors (R_{ISRC} and R_{STC}) for FSO temperature compensation are optimized to 75kΩ for silicon piezoresistive sensors. However, since the required feedback resistor values are sensor dependent, external resistors may also be used. The internal resistors selection bit in the configuration register selects between internal and external feedback resistors.

To calculate the required offset TC and FSOTC compensation coefficients, two test-temperatures are needed. After taking at least two measurements at each temperature, calibration software (in a host computer) calculates the correction coefficients and writes them to the internal EEPROM.

With coefficients ranging from 0000hex to FFFFhex and a +5V reference, each DAC has a resolution of 76µV. Two of the DACs (offset TC and FSOTC) utilize the sensor bridge voltage as a reference. Since the sensor bridge voltage is approximately set to +2.5V the FSOTC and offset TC exhibit a step size of less than 38µV.

For high-accuracy applications (errors less than 0.25%), the first-order offset and FSO TC error should be compensated with the offset TC and FSOTC DACs, and the residual higher order terms with the lookup table. The offset and FSO compensation DACs provide unique compensation values for approximately 1.5°C of temperature change as the temperature indexes the address pointer through the coefficient lookup table. Changing the offset does not effect the FSO, however changing the FSO affects the offset due to nature of the bridge. The temperature is measured on both the MAX1452 die and at the bridge sensor. It is recommended to compensate the first-order temperature errors using the bridge sensor temperature.

Typical Ratiometric Operating Circuit

Ratiometric output configuration provides an output that is proportional to the power supply voltage. This output can then be applied to a ratiometric ADC to produce a digital value independent of supply voltage. Ratiometricity is an important consideration for battery-operated instruments and some industrial applications.

The MAX1452 provides a high-performance ratiometric output with a minimum number of external components (Figure 2). These external components include the following:

- One supply bypass capacitor.
- One optional output EMI suppression capacitor.
- Two optional resistors, R_{ISRC} and R_{STC}, for special sensor bridge types.

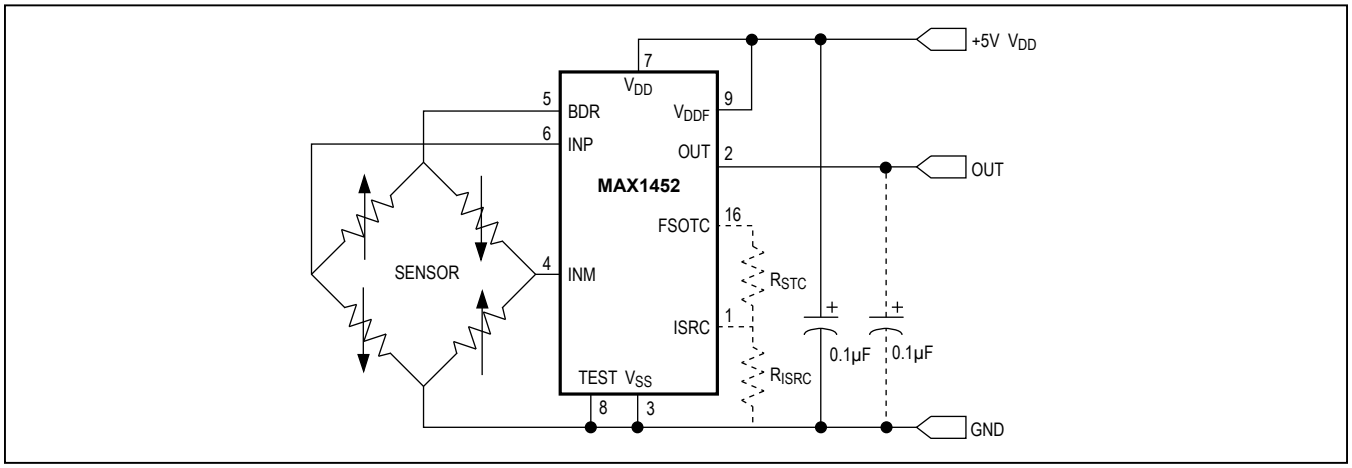


Figure 2. Basic Ratiometric Output Configuration

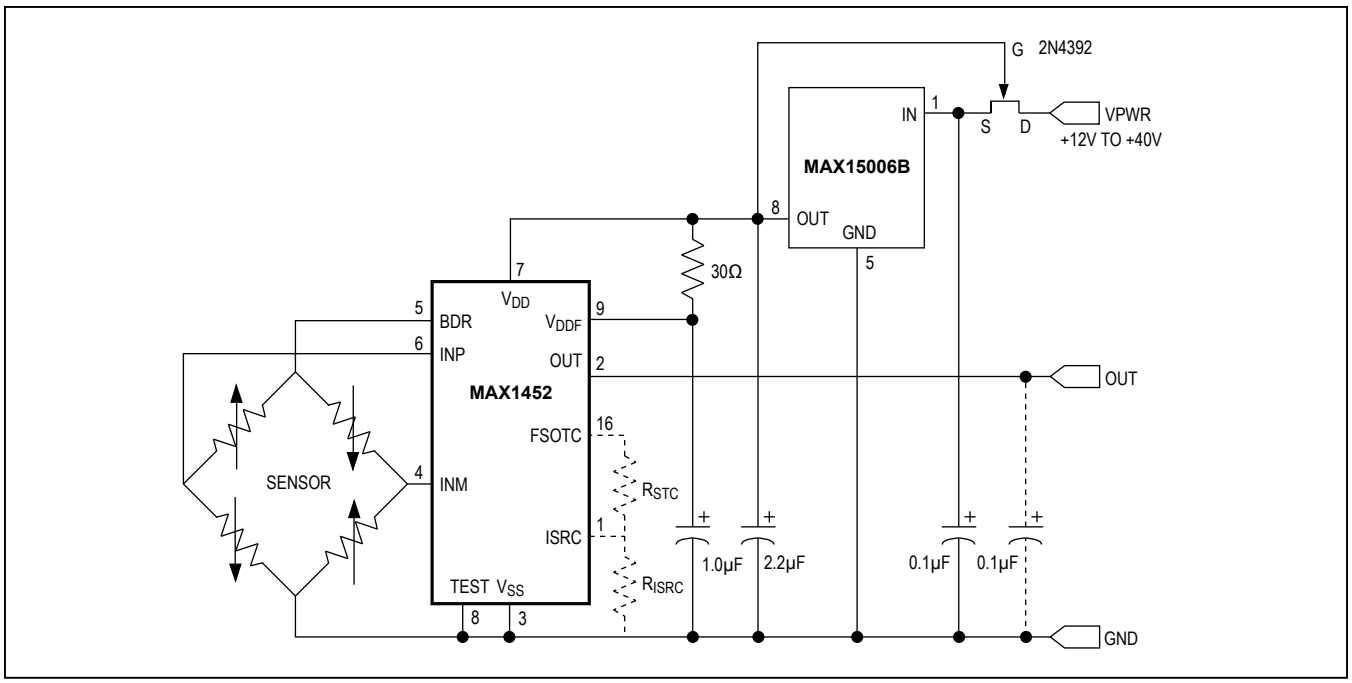


Figure 3. Basic Nonratiometric Output Configuration

Typical Nonratiometric Operating Circuit (12VDC < V_{PWR} < 40VDC)

Nonratiometric output configuration enables the sensor power to vary over a wide range. A high-performance voltage reference, such as the MAX15006B, is incorporated in the circuit to provide a stable supply and reference for MAX1452 operation. A typical example is shown in Figure 3. Nonratiometric operation is valuable when wide ranges of input voltage are to be expected and the system A/D or readout device does not enable ratiometric operation.

Typical 2-Wire, Loop-Powered, 4–20mA Operating Circuit

Process Control systems benefit from a 4–20mA current loop output format for noise immunity, long cable runs, and 2-wire sensor operation. The loop voltages can range from 12VDC to 40VDC and are inherently nonratiometric. The low current consumption of the MAX1452 allows it to operate from loop power with a simple 4–20mA drive circuit efficiently generated using the integrated uncommitted op amp (Figure 4).

Internal Calibration Registers (ICRs)

The MAX1452 has five 16-bit internal calibration registers that are loaded from EEPROM, or loaded from the serial digital interface.

Data can be loaded into the internal calibration registers under three different circumstances.

Normal Operation, Power-On Initialization Sequence

- The MAX1452 has been calibrated, the Secure-Lock byte is set (CL[7:0] = FFhex) and UNLOCK is low.
- Power is applied to the device.
- The power-on-reset functions have completed.
- Registers CONFIG, OTCDAC, and FSOTCDAC are refreshed from EEPROM.
- Registers ODAC, and FSODAC are refreshed from the temperature indexed EEPROM locations.

Normal Operation, Continuous Refresh

- The MAX1452 has been calibrated, the Secure-Lock byte has been set (CL[7:0] = FFhex) and UNLOCK is low.
- Power is applied to the device.
- The power-on-reset functions have completed.
- The temperature index timer reaches a 1ms time period.

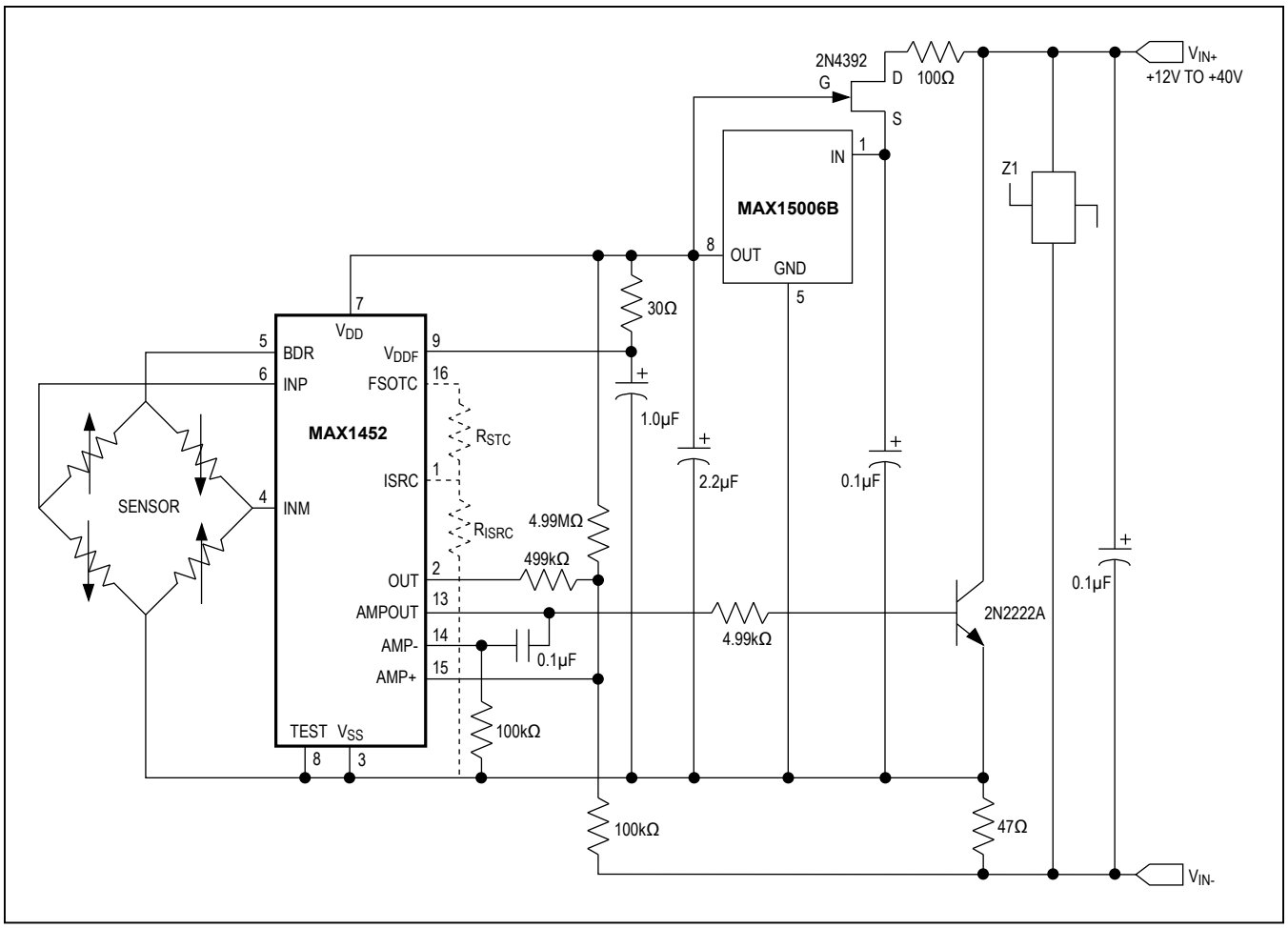


Figure 4. Basic 4–20mA Output, Loop-Powered Configuration

- Registers CONFIG, OTCDAC, and FSOTCDAC are refreshed from EEPROM.
- Registers ODAC and FSODAC are refreshed from the temperature indexed EEPROM locations.

Calibration Operation, Registers Updated by Serial Communications

- The MAX1452 has not had the Secure-Lock byte set (CL[7:0] = 00hex) or UNLOCK is high.
- Power is applied to the device.
- The power-on-reset functions have completed.
- The registers can then be loaded from the serial digital interface by use of serial commands. See the section on *Serial Interface Command Format*.

Internal EEPROM

The internal EEPROM is organized as a 768 by 8-bit memory. It is divided into 12 pages, with 64 bytes per page. Each page can be individually erased. The memory structure is arranged as shown in Table 1. The lookup tables for ODAC and FSODAC are also shown, with the respective temp-index pointer. Note that the ODAC table occupies a continuous segment, from address 000hex to address 15Fhex, whereas the FSODAC table is divided in two parts, from 200hex to 2FFhex, and from 1A0hex to 1FFhex. With the exception of the general-purpose user bytes, all values are 16-bit wide words formed by two adjacent byte locations (high byte and low byte).

The MAX1452 compensates for sensor offset, FSO, and temperature errors by loading the internal calibration registers with the compensation values. These compensation values can be loaded to registers directly through the serial digital interface during calibration or loaded automatically from EEPROM at power-on. In this way the device can be tested and configured during calibration and test and the appropriate compensation values stored

Table 1. EEPROM Memory Address Map

PAGE	LOW-BYTE ADDRESS (hex)	HIGH-BYTE ADDRESS (hex)	TEMP-INDEX[7:0] (hex)	CONTENTS
0	000	001	00	ODAC Lookup Table
	03E	03F	1F	
1	040	041	20	
	07E	07F	3F	
2	080	081	40	
	0BE	0BF	5F	
3	0C0	0C1	60	
	0FE	0FF	7F	
4	100	101	80	
	13E	13F	9F	
5	140	141	A0	
	15E	15F	AF to FF	
	160	161		Configuration
	162	163		Reserved
	164	165		OTCDAC
	166	167		Reserved
	168	169		FSOTCDAC
	16A	16B		Control Location
	16C	16D		52 General-Purpose User Bytes
	17E	17F		
6	180	181		
	19E	19F		
	1A0	1A1	80	FSODAC Lookup Table
	1BE	1BF	8F	
7	1C0	1C1	90	
	1FE	1FF	AF to FF	
8	200	201	00	
	23E	23F	1F	
9	240	241	20	
	27E	27F	3F	
A	280	281	40	
	2BE	2BF	5F	
B	2C0	2C1	60	
	2FE	2FF	7F	

in internal EEPROM. The device auto-loads the registers from EEPROM and be ready for use without further configuration after each power-up. The EEPROM is configured as an 8-bit wide array so each of the 16-bit registers is stored as two 8-bit quantities. The configuration register, FSOTCDAC and OTCDAC registers are loaded from the pre-assigned locations in the EEPROM.

The ODAC and FSODAC are loaded from the EEPROM lookup tables using an index pointer that is a function of temperature. An ADC converts the integrated temperature sensor output to an 8-bit value every 1ms. This digitized value is then transferred into the temp-index register.

The typical transfer function for the temp-index is as follows:

temp-index = 0.6879 Temperature (°C) + 44.0

where temp-index is truncated to an 8-bit integer value. Typical values for the temp-index register are given in Table 6.

Note that the EEPROM is byte wide and the registers that are loaded from EEPROM are 16 bits wide. Thus each index value points to two bytes in the EEPROM.

Maxim programs all EEPROM locations to FFhex with the exception of the oscillator frequency setting and Secure-Lock byte. OSC[2:0] is in the Configuration Register (Table 3). These bits should be maintained at the factory preset values. Programming 00hex in the Secure-Lock byte (CL[7:0] = 00hex), configures the DIO as an asynchronous serial input for calibration and test purposes.

Communication Protocol

The DIO serial interface is used for asynchronous serial data communications between the MAX1452 and a host calibration test system or computer. The MAX1452 automatically detects the baud rate of the host computer when the host transmits the initialization sequence. Baud rates between 4800bps and 38,400bps can be detected and used regardless of the internal oscillator frequency setting. Data format is always 1 start bit, 8 data bits, 1 stop bit and no parity. Communications are only allowed when Secure-Lock is disabled (i.e., CL[7:0] = 00hex) or the UNLOCK pin is held high.

Initialization Sequence

Sending the initialization sequence shown below enables the MAX1452 to establish the baud rate that initializes the serial port. The initialization sequence is one byte transmission of 01hex, as follows:

1111111**0**10000000**1**1111111

The first start bit **0** initiates the baud rate synchronization sequence. The 8 data bits 01hex (LSB first) follow this and then the stop bit, which is indicated above as a **1**, terminates the baud rate synchronization sequence. This initialization sequence on DIO should occur after a period of 1ms after stable power is applied to the device. This allows time for the power-on-reset function to complete and the DIO pin to be configured by Secure-Lock or the UNLOCK pin.

Reinitialization Sequence

The MAX1452 allows for relearning the baud rate. The reinitialization sequence is one byte transmission of FFhex, as follows:

11111111**0**11111111**1**11111111

When a serial reinitialization sequence is received, the receive logic resets itself to its power-up state and waits for the initialization sequence. The initialization sequence must follow the reinitialization sequence in order to re-establish the baud rate.

Serial Interface Command Format

All communication commands into the MAX1452 follow a defined format utilizing an interface register set (IRS). The IRS is an 8-bit command that contains both an interface register set data (IRSD) nibble (4-bit) and an interface register set address (IRSA) nibble (4-bit). All internal calibration registers and EEPROM locations are accessed for read and write through this interface register set. The IRS byte command is structured as follows:

IRS[7:0] = IRSD[3:0], IRSA[3:0]

Where:

- IRSA[3:0] is the 4-bit interface register set address and indicates which register receives the data nibble IRSD[3:0].
- IRSA[0] is the first bit on the serial interface after the start bit.
- IRSD[3:0] is the 4-bit interface register set data.
- IRSD[0] is the fifth bit received on the serial interface after the start bit.

The IRS address decoding is shown in Table 10.

Special Command Sequences

A special command register to internal logic (CRIL[3:0]) causes execution of special command sequences within the MAX1452. These command sequences are listed as CRIL command codes as shown in Table 11.

Write Examples

A 16-bit write to any of the internal calibration registers is performed as follows:

1) Write the 16 data bits to DHR[15:0] using four byte accesses into the interface register set.
2) Write the address of the target internal calibration register to ICRA[3:0].

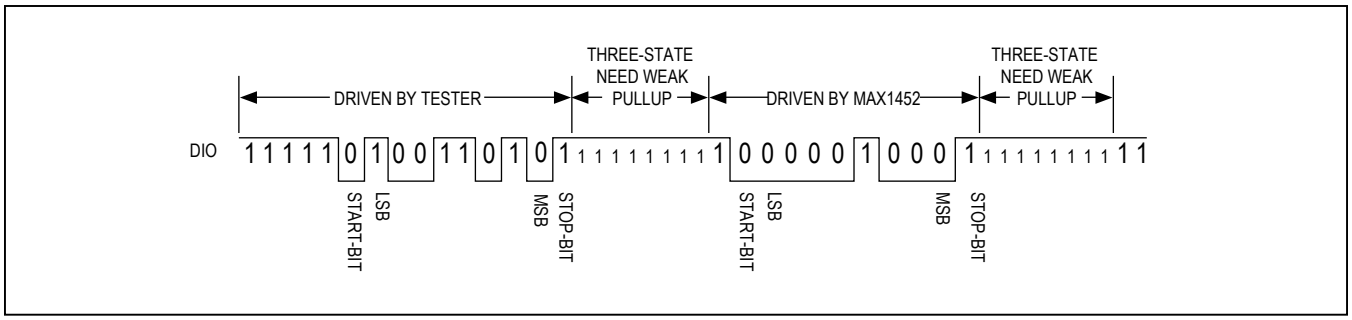


Figure 5. DIO Output Data Format

3) Write the load internal calibration register (LdICR) command to CRIL[3:0].

When a LdICR command is issued to the CRIL register, the calibration register loaded depends on the address in the internal calibration register address (ICRA). Table 12 specifies which calibration register is decoded.

Erasing and Writing the EEPROM

The internal EEPROM needs to be erased (bytes set to FFhex) prior to programming the desired contents. Remember to save the 3 MSBs of byte 161 hex (high byte of the configuration register) and restore it when programming its contents to prevent modification of the trimmed oscillator frequency.

The internal EEPROM can be entirely erased with the ERASE command, or partially erased with the PageErase command (see Table 11, CRIL command). It is necessary to wait 6ms after issuing the ERASE or PageErase command.

After the EEPROM bytes have been erased (value of every byte = FFhex), the user can program its contents, following the procedure below:

1) Write the 8 data bits to DHR[7:0] using two byte accesses into the interface register set.
2) Write the address of the target internal EEPROM location to IEEA[9:0] using three byte accesses into the interface register set.
3) Write the EEPROM write command (EEPW) to CRIL[3:0].

Serial Digital Output

When a RdIRS command is written to CRIL[3:0], DIO is configured as a digital output and the contents of the register designated by IRSP[3:0] are sent out as a byte framed by a start bit and a stop bit.

Once the tester finishes sending the RdIRS command, it must three-state its connection to DIO to allow the MAX1452 to drive the DIO line. The MAX1452 three-states DIO high for 1 byte time and then drive with the start bit in the next bit period followed by the data byte and stop bit. The sequence is shown in Figure 5.

The data returned on a RdIRS command depends on the address in IRSP. Table 13 defines what is returned for the various addresses.

Multiplexed Analog Output

When a RdAlg command is written to CRIL[3:0] the analog signal designated by ALOC[3:0] is asserted on the OUT pin. The duration of the analog signal is determined by ATIM[3:0] after which the pin reverts to three-state. While the analog signal is asserted in the OUT pin, DIO is simultaneously three-stated, enabling a parallel wiring of DIO and OUT. When DIO and OUT are connected in parallel, the host computer or calibration system must three-state its connection to DIO after asserting the stop bit. **Do not load the OUT line when reading internal signals, such as BDR, FSOTC...etc.**

The analog output sequence with DIO and OUT is shown in Figure 6.

The duration of the analog signal is controlled by ATIM[3:0] as given in Table 14.

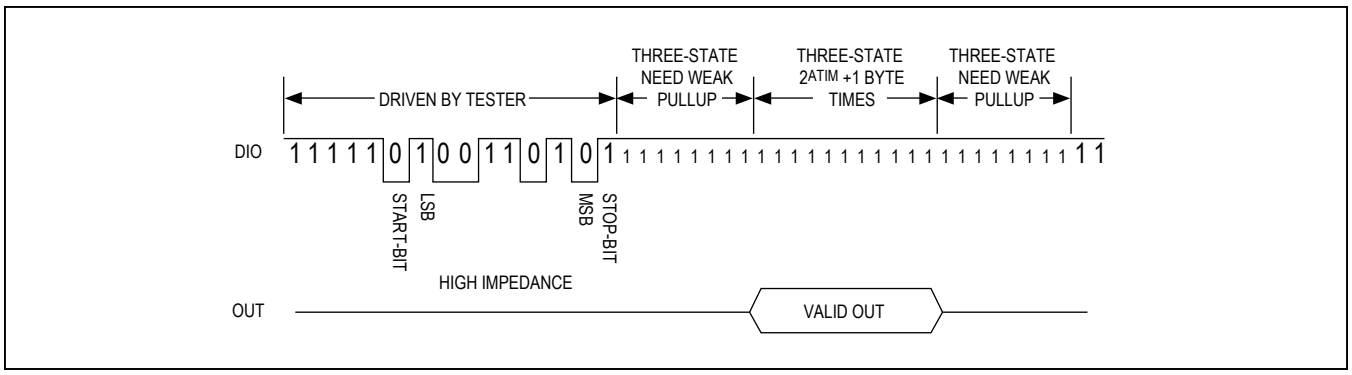


Figure 6. Analog Output Timing

The analog signal driven onto the OUT pin is determined by the value in the ALOC register. The signals are specified in Table 15.

Test System Configuration

The MAX1452 is designed to support an automated production test system with integrated calibration and temperature compensation. Figure 7 shows the implementation concept for a low-cost test system capable of testing many transducer modules connected in parallel. The MAX1452 allows for a high degree of flexibility in system calibration design. This is achieved by use of single-wire digital communication and three-state output nodes. Depending upon specific calibration requirements one may connect all the OUTs in parallel or connect DIO and OUT on each individual module.

Sensor Compensation Overview

Compensation requires an examination of the sensor performance over the operating pressure and temperature range. Use a minimum of two test pressures (e.g., zero and full-span) and two temperatures. More test pressures and temperatures result in greater accuracy. A typical compensation procedure can be summarized as follows:

Set reference temperature (e.g., +25°C):

- Initialize each transducer by loading their respective registers with default coefficients (e.g., based on mean values of offset, FSO and bridge resistance) to prevent overload of the MAX1452.
- Set the initial bridge voltage (with the FSODAC) to half of the supply voltage. Measure the bridge voltage using the BDR or OUT pins, or calculate based on measurements.
- Calibrate the output offset and FSO of the transducer using the ODAC and FSODAC, respectively.
- Store calibration data in the test computer or MAX1452 EEPROM user memory.

Set next test temperature:

- Calibrate offset and FSO using the ODAC and FSODAC, respectively.
- Store calibration data in the test computer or MAX1452 EEPROM user memory.
- Calculate the correction coefficients.
- Download correction coefficients to EEPROM.
- Perform a final test.

Sensor Calibration and Compensation Example

The MAX1452 temperature compensation design corrects both sensor and IC temperature errors. This enables the MAX1452 to provide temperature compensation approaching the inherent repeatability of the sensor. An example of the MAX1452's capabilities is shown in Figure 8.

A repeatable piezoresistive sensor with an initial offset of 16.4mV and a span of 55.8mV was converted into a compensated transducer (utilizing the piezoresistive sensor with the MAX1452) with an offset of 0.5000V and a span of 4.0000V. Nonlinear sensor offset and FSO temperature errors, which were on the order of 20% to 30% FSO, were reduced to under ±0.1% FSO. The following graphs show the output of the uncompensated sensor and the output of the compensated transducer. Six temperature points were used to obtain this result.

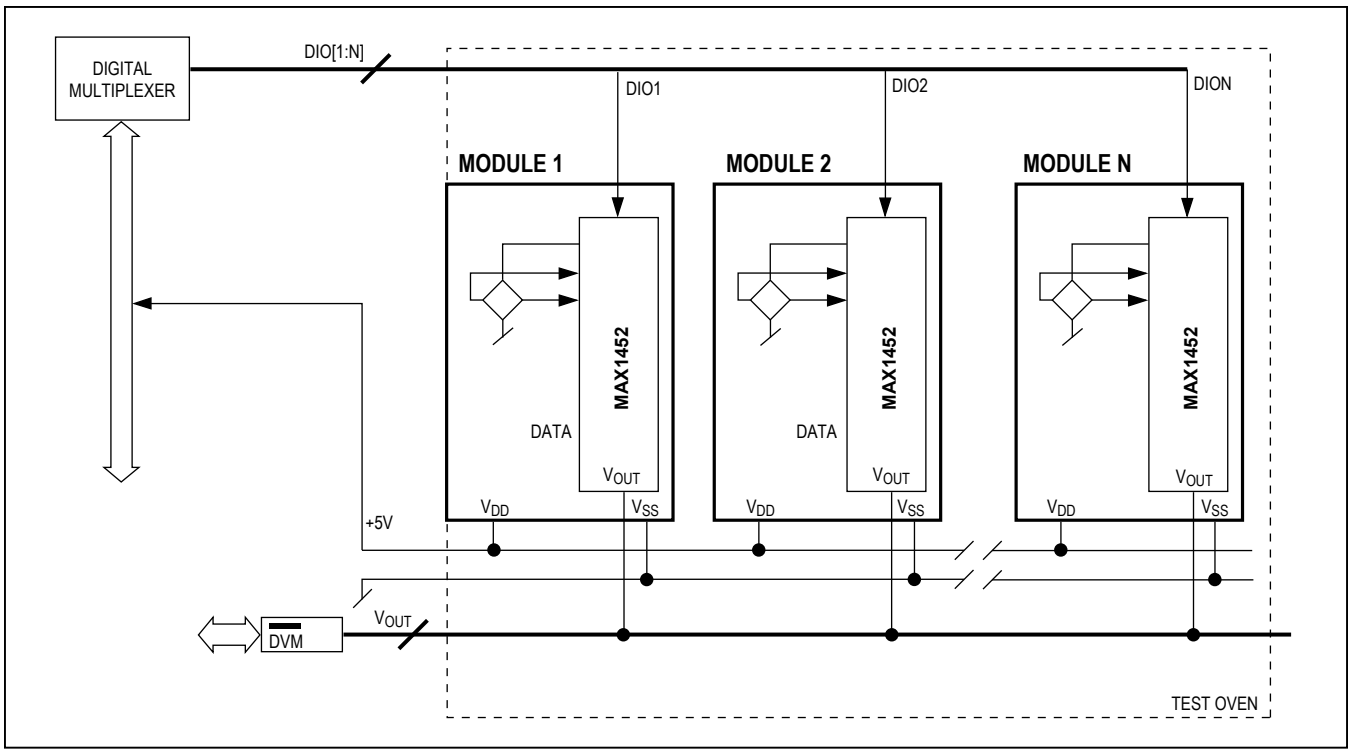


Figure 7. Automated Test System Concept

MAX1452 Evaluation Kit

To expedite the development of MAX1452-based transducers and test systems, Maxim has produced the MAX1452 evaluation kit (EV kit). First-time users of the MAX1452 are strongly encouraged to use this kit.

The EV kit is designed to facilitate manual programming of the MAX1452 with a sensor. It includes the following:

1) **Evaluation Board** with or without a silicon pressure sensor, ready for customer evaluation.
2) **Design/Applications Manual,** which describes in detail the architecture and functionality of the MAX1452. This manual was developed for test engineers familiar with data acquisition of sensor data and provides sensor compensation algorithms and test procedures.
3) **MAX1452 Communication Software,** which enables programming of the MAX1452 from a computer keyboard (IBM compatible), one module at a time.
4) **Interface Adapter,** which allows the connection of the evaluation board to a PC serial port.

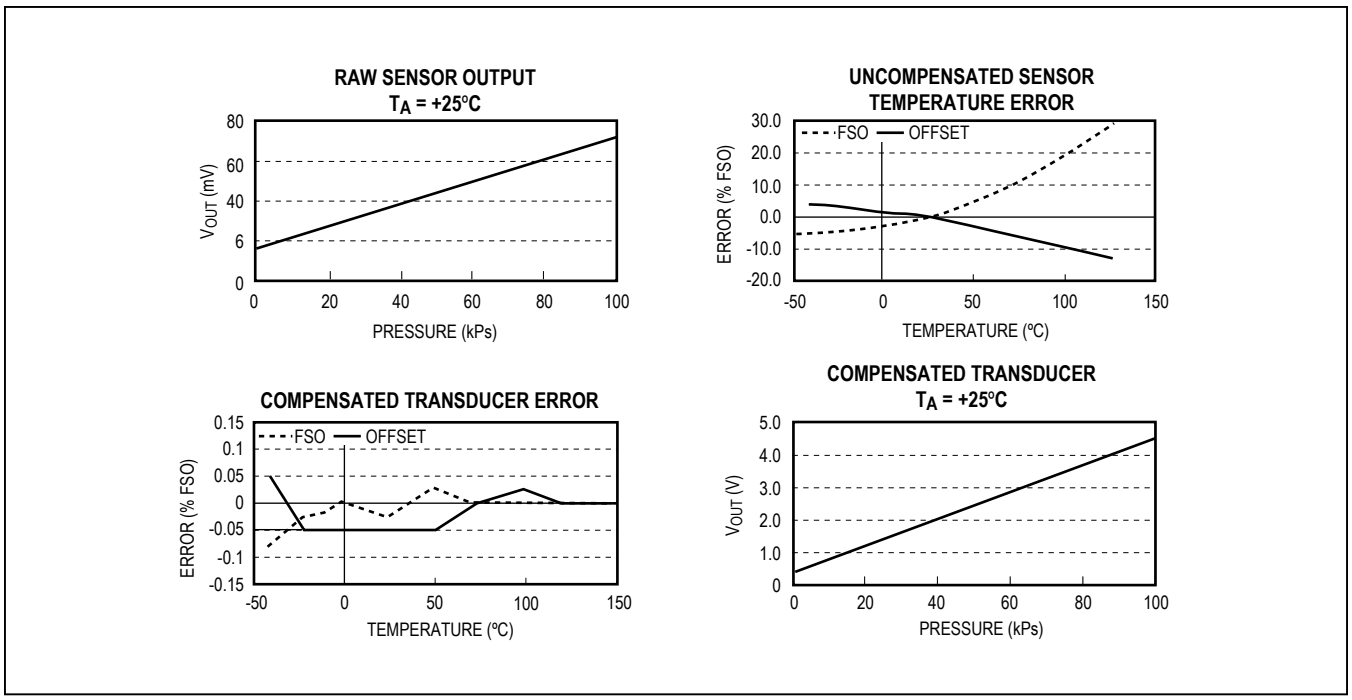


Figure 8. Comparison of an Uncalibrated Sensor and a Calibrated Transducer

Table 2. Registers

REGISTER	DESCRIPTION
CONFIG	Configuration Register
ODAC	Offset DAC Register
OTCDAC	Offset Temperature Coefficient DAC Register
FSODAC	Full Span Output DAC Register
FSOTCDAC	Full Span Output Temperature Coefficient DAC Register

Table 3. Configuration Register (CONFIG[15:0])

FIELD	NAME	DESCRIPTION
15:13	OSC[2:0]	Oscillator frequency setting. **Factory preset, do not change**.
12	R_{EXT}	Logic '1' selects external R_{ISRC} and R_{STC}.
11	CLK1M EN	Logic '1' enables CLK1M output driver.
10	PGA Sign	Logic '1' inverts INM and INP polarity.
9	IRO Sign	Logic '1' for positive input-referred offset (IRO). Logic '0' for negative input-referred offset (IRO).
8:6	IRO[2:0]	Input-referred coarse offset adjustment.
5:2	PGA[3:0]	Programmable gain amplifier setting.
1	ODAC Sign	Logic '1' for positive offset DAC output. Logic '0' for negative offset DAC output.
0	OTCDAC Sign	Logic '1' for positive offset TC DAC output. Logic '0' for negative offset TC DAC output.

Table 4. Input Referred Offset (IRO[2:0])

IRO SIGN, IRO[2:0]	INPUT-REFERRED OFFSET CORRECTION AS % OF V_{DD}	INPUT-REFERRED OFFSET, CORRECTION AT V_{DD} = 5VDC IN mV
1,111	+1.25	+63
1,110	+1.08	+54
1,101	+0.90	+45
1,100	+0.72	+36
1,011	+0.54	+27
1,010	+0.36	+18
1,001	+0.18	+9
1,000	0	0
0,000	0	0
0,001	-0.18	-9
0,010	-0.36	-18
0,011	-0.54	-27
0,100	-0.72	-36
0,101	-0.90	-45
0,110	-1.08	-54
0,111	-1.25	-63

Table 5. PGA Gain Setting (PGA[3:0])

PGA[3:0]	PGA GAIN (V/V)
0000	39
0001	52
0010	65
0011	78
0100	91
0101	104
0110	117
0111	130
1000	143
1001	156
1010	169
1011	182
1100	195
1101	208
1110	221
1111	234

Table 6. Temp-Index Typical Values

TEMPERATURE (°C)	TEMP-INDEX[7:0]	
	DECIMAL	HEXADECIMAL
-40	20	14
25	65	41
85	106	6A
125	134	86

Table 7. Oscillator Frequency Setting

OSC[2:0]	OSCILLATOR FREQUENCY
100	-37.5%
101	-28.1%
110	-18.8%
111	-9.4%
000	1MHz (nominal)
001	+9.4%
010	+18.8%
011	+28.1%

Table 8. EEPROM ODAC and FSODAC Lookup Table Memory Map

TEMP-INDEX[7:0]	EEPROM ADDRESS ODAC LOW BYTE AND HIGH BYTE	EEPROM ADDRESS FSODAC LOW BYTE AND HIGH BYTE
00hex to 7Fhex	000hex and 001hex to 0FEhex and 0FFhex	200hex and 201hex to 2FEhex and 2FFhex
80hex to AFhex	100hex and 101hex to 15Ehex and 15Fhex	1A0hex and 1A1hex to 1FEhex and 1FFhex

Table 9. Control Location (CL[15:0])

FIELD	NAME	DESCRIPTION
15:8	CL[15:8]	Reserved
7:0	CL[7:0]	Control Location. Secure-Lock is activated by setting this to FFhex which disables DIO serial communications and connects OUT to PGA output.

Table 10. IRSA Decoding

IRSA[3:0]	DESCRIPTION
0000	Write IRSD[3:0] to DHR[3:0] (data hold register)
0001	Write IRSD[3:0] to DHR[7:4] (data hold register)
0010	Write IRSD[3:0] to DHR[11:8] (data hold register)
0011	Write IRSD[3:0] to DHR[15:12] (data hold register)
0100	Reserved
0101	Reserved
0110	Write IRSD[3:0] to ICRA[3:0] or IEEA[3:0], (internal calibration register address or internal EEPROM address nibble 0)
0111	Write IRSD[3:0] to IEEA[7:4] (internal EEPROM address, nibble 1)
1000	Write IRSD[3:0] to IRSP[3:0] or IEEA[9:8], (interface register set pointer where IRSP[1:0] is IEEA[9:8])
1001	Write IRSD[3:0] to CRIL[3:0] (command register to internal logic)
1010	Write IRSD[3:0] to ATIM[3:0] (analog timeout value on read)
1011	Write IRSD[3:0] to ALOC[3:0] (analog location)
1100 to 1110	Reserved
1111	Write IRSD[3:0] = 1111bin to relearn the baud rate

Table 11. CRIL Command Codes

CRIL[3:0]	NAME	DESCRIPTION
0000	LdICR	Load internal calibration register at address given in ICRA with data from DHR[15:0].
0001	EEPW	EEPROM write of 8 data bits from DHR[7:0] to address location pointed by IEEA[9:0].
0010	ERASE	Erase all of EEPROM (all bytes equal FFhex).
0011	RdICR	Read internal calibration register as pointed to by ICRA and load data into DHR[15:0].
0100	RdEEP	Read internal EEPROM location and load data into DHR[7:0] pointed by IEEA[9:0].
0101	RdIRS	Read interface register set pointer IRSP[3:0]. See Table 13.
0110	RdAlg	Output the multiplexed analog signal onto OUT. The analog location is specified in ALOC[3:0] (Table 15) and the duration (in byte times) that the signal is asserted onto the pin is specified in ATIM[3:0] (Table 14).
0111	PageErase	Erases the page of the EEPROM as pointed by IEEA[9:6]. There are 64 bytes per page and thus 12 pages in the EEPROM.
1000 to 1111	Reserved	Reserved.

Table 12. ICRA[3:0] Decode

ICRA[3:0]	NAME	DESCRIPTION
0000	CONFIG	Configuration Register
0001	ODAC	Offset DAC Register
0010	OTCDAC	Offset Temperature Coefficient DAC Register
0011	FSODAC	Full Scale Output DAC Register
0100	FSOTCDAC	Full Scale Output Temperature Coefficient DAC Register
0101		Reserved. Do not write to this location (EEPROM test).
0110 to 1111		Reserved. Do not write to this location.

Table 13. IRSP Decode

IRSP[3:0]	RETURNED VALUE
0000	DHR[7:0]
0001	DHR[15:8]
0010	IEEA[7:4], ICRA[3:0] concatenated
0011	CRIL[3:0], IRSP[3:0] concatenated
0100	ALOC[3:0], ATIM[3:0] concatenated
0101	IEEA[7:0] EEPROM address byte
0110	IEED[7:0] EEPROM data byte
0111	TEMP-Index[7:0]
1000	BitClock[7:0]
1001	Reserved. Internal flash test data.
1010-1111	11001010 (CAhex). This can be used to test communication.

Table 14. ATIM Definition

ATIM[3:0]	DURATION OF ANALOG SIGNAL SPECIFIED IN BYTE TIMES (8-BIT TIME)
0000	2^0 + 1 = 2 byte times i.e. (2 x 8)/baud rate
0001	2^1 + 1 = 3 byte times
0010	2^2 + 1 = 5 byte times
0011	2^3 + 1 = 9 byte times
0100	2^4 + 1 = 17 byte times
0101	2^5 + 1 = 33 byte times
0110	2^6 + 1 = 65 byte times
0111	2^7 + 1 = 129 byte times
1000	2^8 + 1 = 257 byte times
1001	2^9 + 1 = 513 byte times
1010	2^{10} + 1 = 1025 byte times
1011	2^{11} + 1 = 2049 byte times
1100	2^{12} + 1 = 4097 byte times
1101	2^{13} + 1 = 8193 byte times
1110	2^{14} + 1 = 16,385 byte times
1111	In this mode OUT is continuous, however DIO accepts commands after 32,769 byte times. Do not parallel connect DIO to OUT.

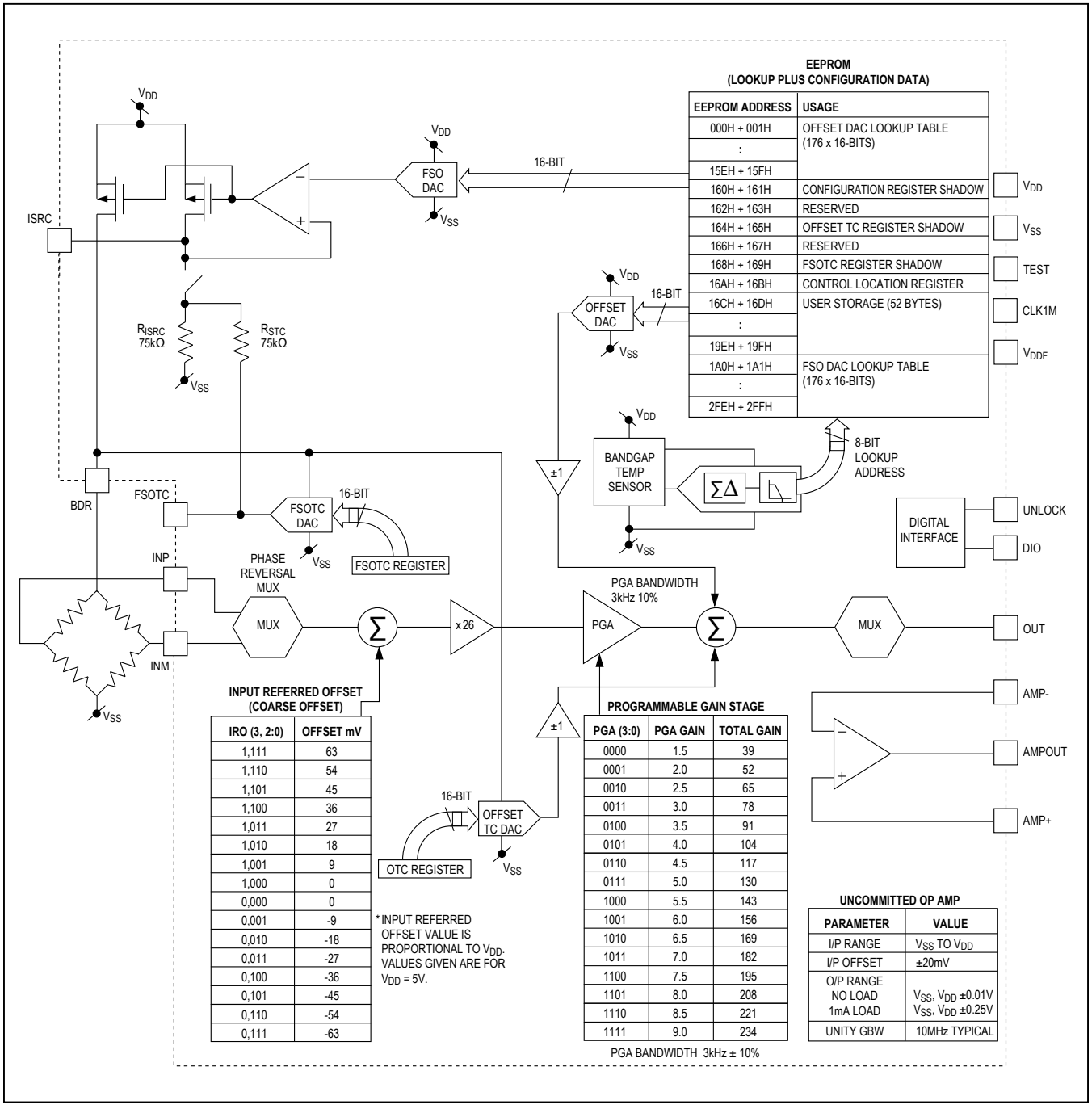
Table 15. ALOC Definition

ALOC[3:0]	ANALOG SIGNAL	DESCRIPTION
0000	OUT	PGA Output
0001	BDR	Bridge Drive
0010	ISRC	Bridge Drive Current Setting
0011	VDD	Internal Positive Supply
0100	VSS	Internal Ground
0101	BIAS5U	Internal Test Node
0110	AGND	Internal Analog Ground. Approximately half of VDD.
0111	FSODAC	Full Scale Output DAC
1000	FSOTCDAC	Full Scale Output TC DAC
1001	ODAC	Offset DAC
1010	OTCDAC	Offset TC DAC
1011	VREF	Bandgap Reference Voltage (nominally 1.25V)
1100	VPTATP	Internal Test Node
1101	VPTATM	Internal Test Node
1110	INP	Sensor's Positive Input
1111	INM	Sensor's Negative Input

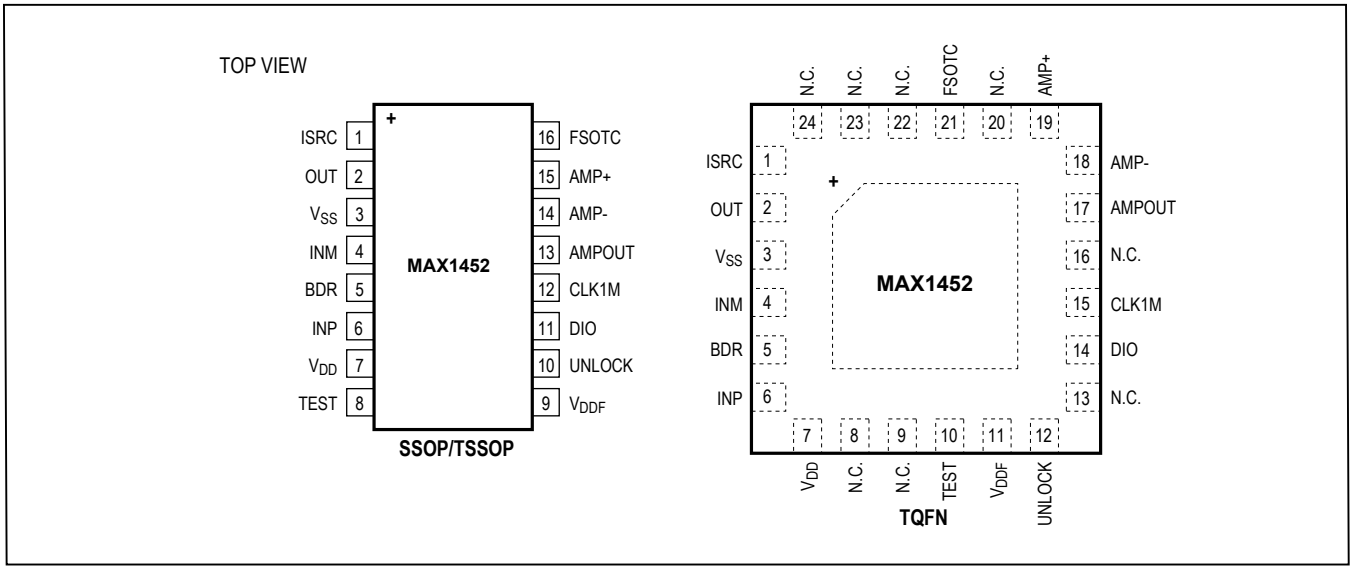
Table 16. Effects of Compensation

TYPICAL UNCOMPENSATED INPUT (SENSOR)	TYPICAL COMPENSATED TRANSDUCER OUTPUT
Offset ..... ±100% FSO FSO ..... 4mV/V to 60mV/V Offset TC ..... 20% FSO Offset TC Nonlinearity ..... 4% FSO FSOTC ..... -20% FSO FSOTC Nonlinearity ..... 5% FSO Temperature Range..... -40°C to +125°C	OUT ..... Ratiometric to V_{DD} at 5.0V Offset at +25°C..... 0.500V ±200µV FSO at +25°C..... 4.000V ±200µV Offset accuracy over temp. range .....±4mV (±0.1% FSO) FSO accuracy over temp. range .....±4mV (±0.1% FSO)

Detailed Block Diagram



Pin Configurations



Chip Information

SUBSTRATE CONNECTED TO: V_{SS}

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 SSOP	A16+2	21-0056	90-0106
16 TSSOP	U16+2	21-0066	90-0117
24 TQFN-EP	T2444+4	21-0139	90-0022

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	4/09	Added TQFN and TSSOP package information, changed packages to lead free, changed all occurrences of ASIC to MAX1452, changed V_{DDF} RC filter values, recommended a more suitable voltage reference for non-ratiometric application circuits, corrected MAX1452 input range, and added typical EEPROM current requirements to EC table, and added gain nonlinearity graph.	1–7, 9, 10, 12, 18, 22, 24
3	11/13	Updated *Package Information* section	24
4	10/14	Deleted automotive reference	8
5	4/15	Updated *Benefits and Features* section	1

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