MAX11040K/MAX11060 24-/16-Bit, 4-Channel, Simultaneous-Sampling, Cascadable, Sigma-Delta ADCs

General Description

The MAX11040K/MAX11060 are 24-/16-bit, 4-channel, simultaneous-sampling, sigma-delta analog-to-digital converters (ADCs). The devices allow simultaneous sampling of as many as 32 channels using a built-in cascade feature to synchronize as many as eight devices. The serial interface of the devices allows reading data from all the cascaded devices using a single command. Four modulators simultaneously convert each fully differential analog input with a programmable data output rate ranging from 0.25ksps to 64ksps. The devices achieve 106dB SNR at 16ksps and 117dB SNR at 1ksps (MAX11040K). The devices operate from a single +3V supply. The differential analog input range is ±2.2V when using the internal reference; an external reference is optional. Each input is overvoltage protected up to ±6V without damage. The devices use an internal crystal oscillator or an external source for clock.

The devices are compatible with SPI, QSPI™, MICROWIRE®, and DSP-compatible 4-wire serial interfaces. An on-board interface logic allows one serial interface (with a single chip select) to control up to eight cascaded devices or 32 simultaneous sampling analog input channels.

The devices are ideally suited for power-management systems. Each channel includes an adjustable sampling phase enabling internal compensation for phase shift due to external dividers, transformers, or filters at the inputs. The output data rate is adjustable with a 0.065% resolution (at 16ksps or below) to track the varying frequency of a periodic input. A $\overline{SYNC}$ input allows periodic alignment of the conversion timing of multiple devices with a remote timing source.

The devices are available in a 38-pin TSSOP package specified over the -40°C to +105°C industrial temperature range.

Applications

- Power-Protection Relay Equipment
- Multiphase Power Systems
- Industrial Data-Acquisition Systems
- Medical Instrumentation

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX11040K.related.

MICROWIRE is a registered trademark of National Semiconductor Corp.

QSPI is a trademark of Motorola, Inc.

Benefits and Features

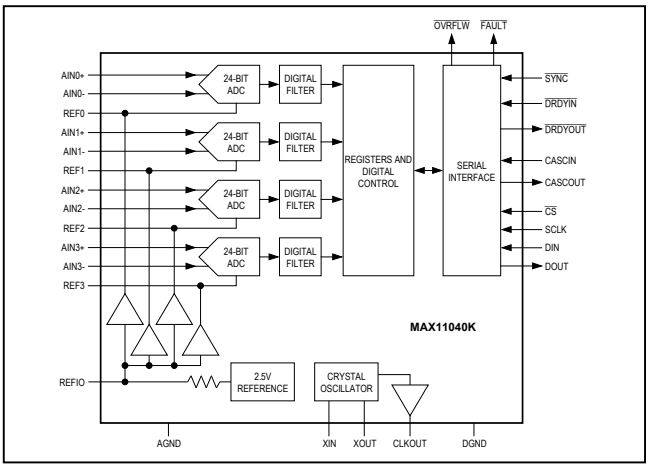
- Feature Set Ideal for Energy Measurement Systems
  - Four Fully Differential Simultaneously Sampled Channels
  - Cascadable for Up to 32 Channels of Simultaneous Sampling
  - Programmable Sampling Phase for Phase Shift Compensation
    - 0 to 333µs in 1.33µs Steps
  - Programmable Output Data Rate with 0.065% Resolution
- Excellent Performance for High-Accuracy Measurement Applications
  - 117dB SNR at 1ksps
  - 106dB SNR at 16ksps
  - 0.25% Error Over a 1000:1 Dynamic Range
  - ±2.2V Full-Scale Input Range
- Single-Supply Operation and Protected Inputs for Design Simplicity and Robustness
  - 3.0V to 3.6V Analog Supply Voltage
  - 2.7V to V_{AVDD} Digital Supply Voltage
  - ±6V Overvoltage Protected Inputs
  - -40°C to +105°C Operating Temperature Range

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX11040KGUU+	-40°C to +105°C	38 TSSOP
MAX11060GUU+	-40°C to +105°C	38 TSSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Functional Diagram



Absolute Maximum Ratings

AVDD to AGND .....-0.3V to +4V
DVDD to DGND.....-0.3V to (V_{AVDD} + 0.3V)
AGND to DGND.....-0.3V to +0.3V
DIN, SCLK, $\overline{CS}$, XIN, $\overline{SYNC}$, $\overline{DRDYIN}$, CASCIN to DGND.....-0.3V to (V_{DVDD} + 0.3V)
DOUT, $\overline{DRDYOUT}$, CASCOUT, CLKOUT, XOUT to DGND.....-0.3V to (V_{DVDD} + 0.3V)
$\overline{FAULT}$, $\overline{OVRFLW}$ to DGND .....-0.3V to +4.0V
AIN_+ to AIN_- .....-6.0V to +6.0V
AIN_ _ to AGND (V_{AVDD} ≥ 3V, V_{DVDD} ≥ 2.7V, FAULTDIS = 0, SHDN = 0, $f_{XIN\ CLOCK}$ ≥ 20MHz).....-6.0V to +6.0V
AIN_ _ to AGND (V_{AVDD} < 3V or V_{DVDD} < 2.7V or FAULTDIS = 1 or SHDN = 1 or $f_{XIN\ CLOCK}$ < 20MHz).....-3.5V to +3.5V
REFIO, REF_ to AGND.....-0.3V to (V_{AVDD} + 0.3V)
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
TSSOP (derated 13.7mW/°C above +70°C).....1096mW
Operating Temperature Range .....-40°C to +105°C
Storage Temperature Range .....-60°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{AVDD} = +3.0V to +3.6V, V_{DVDD} = +2.7V to V_{AVDD}, $f_{XIN\ CLOCK}$ = 24.576MHz, f_{OUT} = 16ksps, V_{REFIO} = +2.5V (external), C_{REFIO} = C_{REF0} = C_{REF1} = C_{REF2} = C_{REF3} = 1µF to AGND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 2)						
Resolution		MAX11040K	24			Bits
		MAX11060	16			
Differential Nonlinearity	DNL	24-bit no missing code (MAX11040K); 16-bit no missing code (MAX11060)		0.1		LSB
Integral Nonlinearity (Note 3)	INL	T_A = +25°C and +105°C (MAX11040K)		0.001	0.004	%FS
		T_A = -40°C (MAX11040K)			0.006	
		MAX11060		0.001		
Offset Error			-1		+1	mV
Gain Error		(Note 4)	-1		+1	%FS
Offset-Error Drift		(Note 5)		0.5		ppm/°C
Gain-Error Drift		(Note 5)		1		ppm/°C
Change in Gain Error vs. f_{OUT}		f_{OUT} = 0.25ksps to 64ksps		< 0.025		% FS
Channel-to-Channel Gain Matching				0.03		% FS
DYNAMIC SPECIFICATIONS (62.5Hz sine-wave input, 2.17V_{P-P})						
Signal-to-Noise Ratio	SNR	(Note 6) (MAX11040K)	103	106		dB
		(Note 6) (MAX11060)		94.5		
Total Harmonic Distortion	THD	T_A = +25°C and +105°C (MAX11040K)			-94	dB
		T_A = -40°C (MAX11040K)			-90	
		MAX11060		-106		
Signal-to-Noise Plus Distortion	SINAD	T_A = +25°C and +105°C (MAX11040K)	93	98		dB
		T_A = -40°C (MAX11040K)	89			
		MAX11060		94		
Spurious-Free Dynamic Range	SFDR	T_A = +25°C and +105°C (MAX11040K)	94	100		dB
		T_A = -40°C (MAX11040K)	89			
		MAX11060		100		
Relative Accuracy (Note 7)		0.1%FS input (MAX11040K)			0.25	%
		6.0%FS input (MAX11040K)			0.005	

Electrical Characteristics (continued)

(V_{AVDD} = +3.0V to +3.6V, V_{DVDD} = +2.7V to V_{AVDD}, $f_{XIN\ CLOCK}$ = 24.576MHz, f_{OUT} = 16ksps, V_{REFIO} = +2.5V (external), C_{REFIO} = C_{REF0} = C_{REF1} = C_{REF2} = C_{REF3} = 1µF to AGND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bandwidth		-3dB		3.4		kHz
Latency		(Note 8)		374		µs
Passband Flatness		From DC to 1.4kHz		< 0.1		dB
Amplitude-Dependent Phase Error		FS vs. 0.1% FS		< 0.01	0.12	Degrees
Channel-to-Channel Phase Matching				0.0001		Degrees
Phase-Error Drift				0.001		Degrees
Channel-to-Channel Isolation				-130		dB
Common-Mode Rejection	CMRR			109		dB
ANALOG INPUTS (AIN_+, AIN_-)						
Differential FS Input Range	V_{IN}	V_{AIN_+} - V_{AIN_-}	-2.2		+2.2	V
Single-Ended Positive Input Range	V_{AIN_+}	Referenced to AGND	-2.2		+2.2	V
Single-Ended Negative Input Range	V_{AIN_-}	Referenced to AGND	-2.2		+2.2	V
Positive Fault Threshold	V_{PFT}	V_{AIN_+} or V_{AIN_-} (Note 9)	2.25		2.65	V
Negative Fault Threshold	V_{NFT}	V_{AIN_+} or V_{AIN_-} (Note 9)	-2.65		-2.25	V
Fault Pin Response Time				2.5		µs
Input Impedance	Z_{IN}	$V_{NFT} \le V_{IN} \le V_{PFT}$		130		kΩ
		$V_{IN} < V_{NFT}$ or $V_{IN} > V_{PFT}$		> 0.5		
DC Leakage Current	I_{IN}	V_{AIN_+} = V_{AIN_-}		±0.01	±1	µA
Input Sampling Rate	f_S	$f_S = f_{XINCLOCK}/8$		3.072		Msps
Input Sampling Capacitance				4.0		pF
INTERNAL REFERENCE						
REFIO Output Voltage	V_{REF}	$T_A = T_{MAX}$	2.4	2.5	2.6	V
REFIO Output Resistance				1		kΩ
REFIO Temp Drift				50		ppm/°C
REFIO Long-Term Stability				200		ppm/ 1000hr
REFIO Output Noise				3		μV_{RMS}
REFIO Power-Supply Rejection	PSRR			75		dB
EXTERNAL REFERENCE						
REFIO Input Voltage	V_{REF}		2.3		2.7	V
REFIO Sink Current				200		µA
REFIO Source Current				200		µA
REFIO Input Capacitance				10		pF
CRYSTAL OSCILLATOR (XIN, XOUT)						
Tested Resonant Frequency		(Note 10)		24.576		MHz
Maximum Crystal ESR				30		Ω
Oscillator Startup Time				< 2		ms
Oscillator Stability		V_{DVDD} = 3.3V, excluding crystal		10		ppm/°C
Maximum Oscillator Load Capacitance				10		pF

Electrical Characteristics (continued)

(V_{AVDD} = +3.0V to +3.6V, V_{DVDD} = +2.7V to V_{AVDD}, $f_{XIN\ CLOCK}$ = 24.576MHz, f_{OUT} = 16ksps, V_{REFIO} = +2.5V (external), C_{REFIO} = C_{REF0} = C_{REF1} = C_{REF2} = C_{REF3} = 1µF to AGND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, $\overline{CS}$, DIN, $\overline{SYNC}$, CASCIN, $\overline{DRDYIN}$, XIN)						
Input Low Voltage	V_{IL}				0.3 x V_{DVDD}	V
Input High Voltage	V_{IH}		0.7 x V_{DVDD}			V
Input Hysteresis	V_{HYS}	V_{DVDD} = 3.0V		100		mV
Input Leakage Current	I_L			±0.01	±1	µA
Input Capacitance	C_{IN}			15		pF
CMOS DIGITAL OUTPUTS (DOUT, CASCOUT, $\overline{DRDYOUT}$, CLKOUT)						
Output Low Voltage	V_{OL}	I_{SINK} = 5mA			0.15 x V_{DVDD}	V
Output High Voltage	V_{OH}	I_{SOURCE} = 1mA	0.85 x V_{DVDD}			V
Three-State Leakage Current	I_{LT}				±1	µA
Three-State Capacitance	C_{OUT}			15		pF
OPEN-DRAIN DIGITAL OUTPUTS ($\overline{OVRFLW}$, $\overline{FAULT}$)						
Output Low Voltage	V_{OL}	I_{SINK} = 5mA			0.15 x V_{DVDD}	V
Output High Voltage	V_{OH}	Internal pullup only	0.85 x V_{DVDD}			V
Internal Pullup Resistance				30		kΩ
POWER REQUIREMENTS						
Analog Supply Voltage	AV_{DD}		3.0		3.6	V
Digital Supply Voltage	DV_{DD}		2.7		V_{AVDD}	V
Analog Supply Current (Note 11)	I_{AVDD}	Normal operation		25	35	mA
		Shutdown and $f_{XINCLOCK}$ = 0Hz		0.1	5	µA
Digital Supply Current (Note 11)	I_{DVDD}	Normal operation		11	15	mA
		Shutdown and $f_{XINCLOCK}$ = 0Hz		0.3		µA
AC Positive-Supply Rejection		V_{AVDD} = 3.3V + 100mV_{P-P} at 1kHz		70		dB
DC Positive-Supply Rejection		V_{AVDD} = V_{DVDD} = 3.0V to 3.6V		75		dB
ESD PROTECTION						
All Pins	ESD	Human Body Model		2.5		kV
TIMING CHARACTERISTICS (Figures 7–10)						
SCLK Clock Period	t_{SCP}		50			ns
SCLK Pulse Width (High and Low)	t_{PW}		20			ns
DIN or $\overline{CS}$ to SCLK Fall Setup	t_{SU}		10			ns
SCLK Fall to DIN Hold	t_{HD}		0			ns
SCLK Rise to $\overline{CS}$ Rise	t_{CSH1}		0			ns

Electrical Characteristics (continued)

(V_{AVDD} = +3.0V to +3.6V, V_{DVDD} = +2.7V to V_{AVDD}, $f_{XIN\ CLOCK}$ = 24.576MHz, f_{OUT} = 16ksps, V_{REFIO} = +2.5V (external), C_{REFIO} = C_{REF0} = C_{REF1} = C_{REF2} = C_{REF3} = 1µF to AGND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

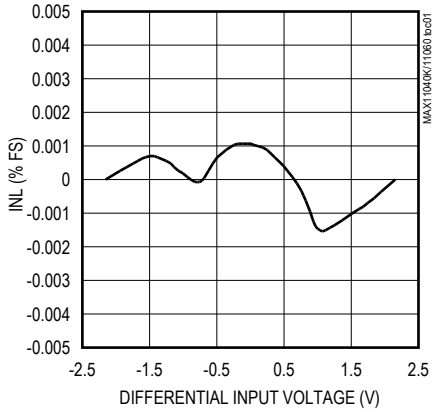
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Rise to DOUT Valid	t_{DOT}	C_{LOAD} = 30pF	1.5	10	16	ns
		C_{LOAD} = 100pF		< 16		
$\overline{CS}$ Fall to DOUT Enable	t_{DOE}	C_{LOAD} = 30pF	0.3		20	ns
$\overline{CS}$ Rise to DOUT Disable	t_{DOD}	C_{LOAD} = 30pF	0.7		16	ns
$\overline{CS}$ Pulse Width	t_{CSW}		16			ns
CASCIN-to-SCLK Rise Setup	t_{SC}		16			ns
SCLK Rise to CASCOUT Valid	t_{COT}	C_{LOAD} = 100pF			20	ns
$\overline{SYNC}$ Pulse Width	t_{SYN}		2			XIN Clock Cycles
XIN Clock Pulse Width	t_{XPW}		16			ns
$\overline{DRDYIN}$ to $\overline{DRDYOUT}$	t_{DRDY}	C_{LOAD} = 30pF			20	ns
XIN Clock to $\overline{DRDYOUT}$ Delay	t_{XDRDY}	$\overline{DRDYIN}$ = DGND			40	ns
XIN Clock Period	t_{XP}		40			ns
XIN Clock to $\overline{SYNC}$ Setup	t_{SS}	(Note 12)	16			ns
$\overline{SYNC}$ to XIN Clock Hold	t_{HS}	(Note 12)	5			ns
XIN-to-CLKOUT Delay	t_{XCD}				40	ns
Power-On Reset Delay		(Note 13)		< 1		ms

Note 1: Devices are production tested at +105°C. Specifications to -40°C are guaranteed by design.
Note 2: Tested at V_{AVDD} = V_{DVDD} = +3.0V.
Note 3: Integral nonlinearity is the deviation of the analog value at any code from its ideal value after the offset and gain errors are removed.
Note 4: Offset nulled.
Note 5: Offset and gain drift defined as change in offset and gain error vs. full scale.
Note 6: Noise measured with AIN_+ = AIN_- = AGND.
Note 7: Relative accuracy is defined as the difference between the actual RMS amplitude and the ideal RMS amplitude of a 62.5Hz sine wave, measured over one cycle at a 16ksps data rate, expressed as a fraction of the ideal RMS amplitude. The relative accuracy specification refers to the maximum error expected over 1 million measurements. Calculated from SNR. Not production tested.
Note 8: Latency is a function of the sampling rate, sample instant delay, and XIN clock.
Note 9: Voltage levels below the positive fault threshold and above the negative fault threshold, relative to AGND on each individual AIN_+ and AIN_- input, do not trigger the analog input protection circuitry.
Note 10: Test performed using RXD MP35.
Note 11: All digital inputs at DGND or DVDD.
Note 12: $\overline{SYNC}$ is captured by the subsequent XIN clock if this specification is violated.
Note 13: Delay from DVDD exceeds 2.0V until digital interface is operational.

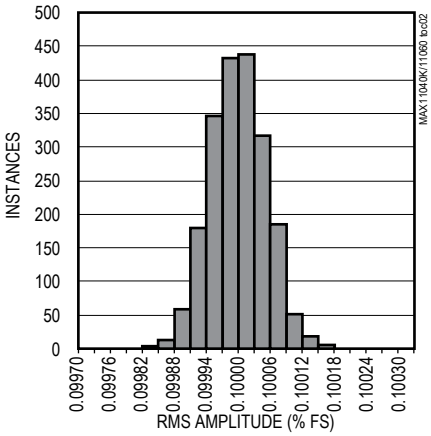
Typical Operating Characteristics (MAX11040K)

(V_{AVDD} = V_{DVDD} = 3.3V, $f_{XIN\ CLOCK}$ = 24.576MHz, f_{OUT} = 16ksps, V_{REFIO} = 2.5V (external), C_{REFIO} = C_{REF0} = C_{REF1} = C_{REF2} = C_{REF3} = 1µF, T_A = +25°C, unless otherwise noted.)

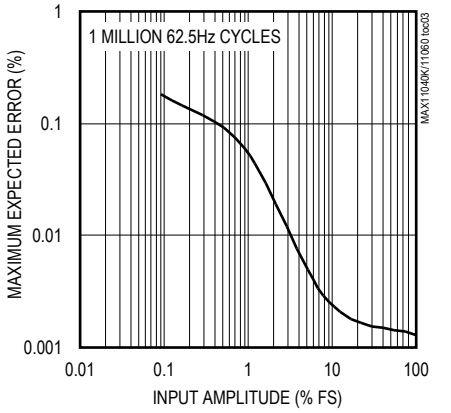
INL vs. DIFFERENTIAL INPUT VOLTAGE



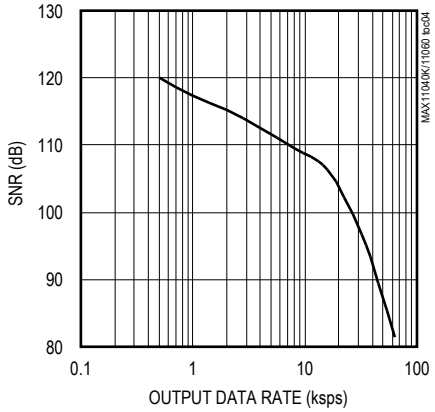
HISTOGRAM OF RMS AMPLITUDE AT 0.1% FS



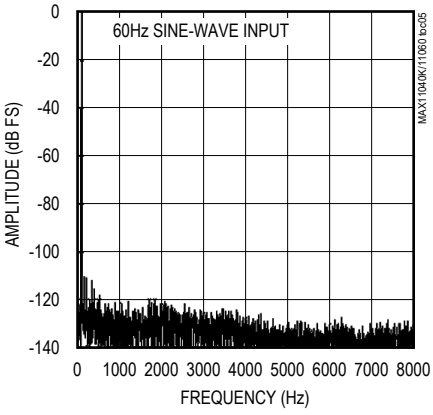
MAXIMUM EXPECTED ERROR OF CALCULATED RMS AMPLITUDE vs. INPUT AMPLITUDE



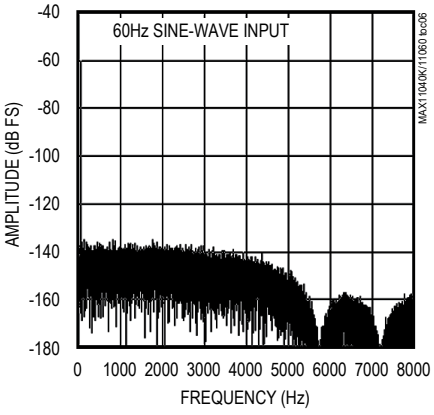
SIGNAL-TO-NOISE RATIO vs. OUTPUT DATA RATE



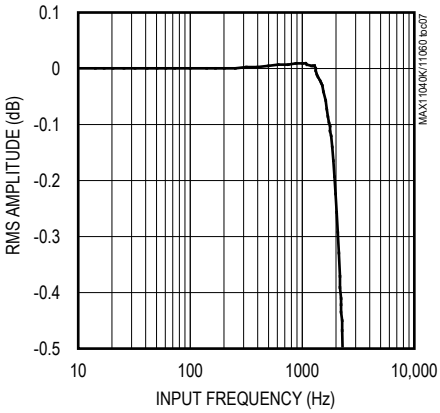
FFT vs. FREQUENCY AT FULL SCALE



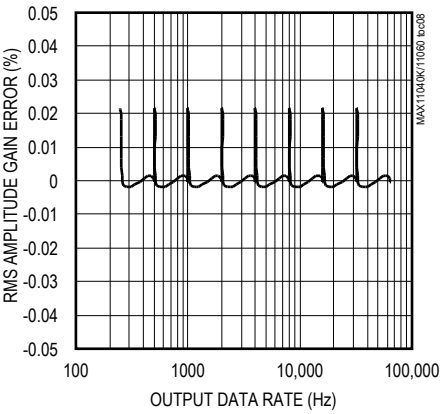
FFT vs. FREQUENCY AT 0.1% FULL SCALE



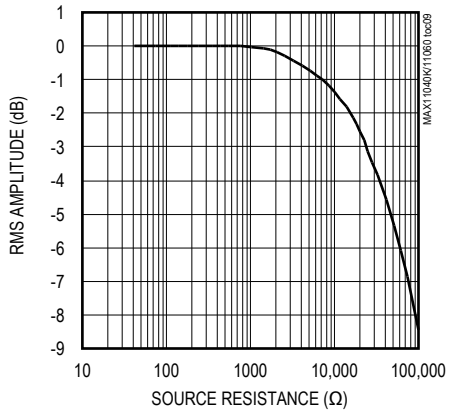
RMS AMPLITUDE vs. INPUT FREQUENCY



RMS AMPLITUDE GAIN ERROR vs. OUTPUT DATA RATE



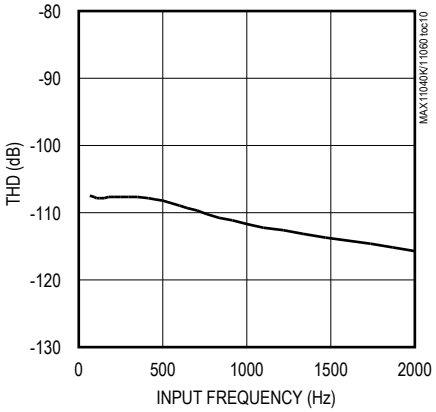
RMS AMPLITUDE vs. SOURCE RESISTANCE



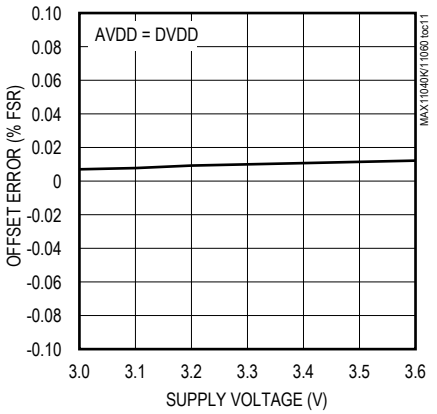
Typical Operating Characteristics (MAX11040K) (continued)

(V_{AVDD} = V_{DVDD} = 3.3V, $f_{XIN\ CLOCK}$ = 24.576MHz, f_{OUT} = 16ksps, V_{REFIO} = 2.5V (external), C_{REFIO} = C_{REF0} = C_{REF1} = C_{REF2} = C_{REF3} = 1µF, T_A = +25°C, unless otherwise noted.)

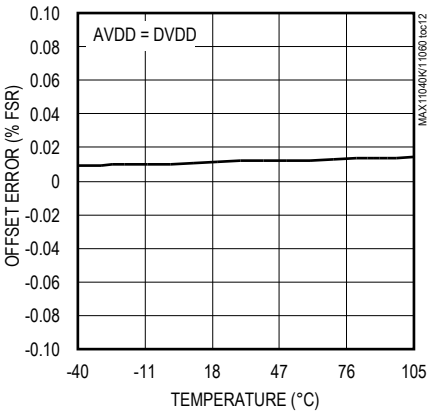
TOTAL HARMONIC DISTORTION vs. INPUT FREQUENCY



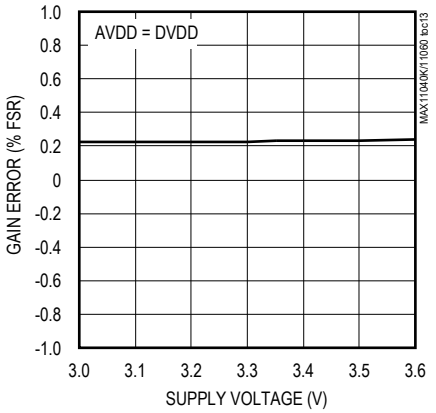
OFFSET ERROR vs. SUPPLY VOLTAGE



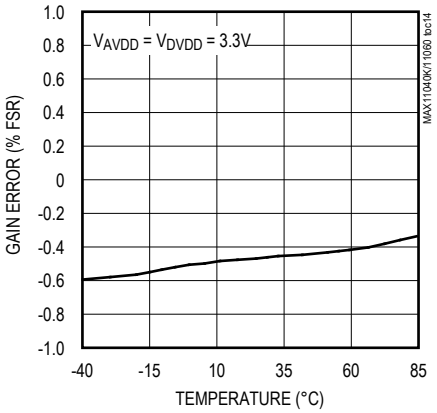
OFFSET ERROR vs. TEMPERATURE



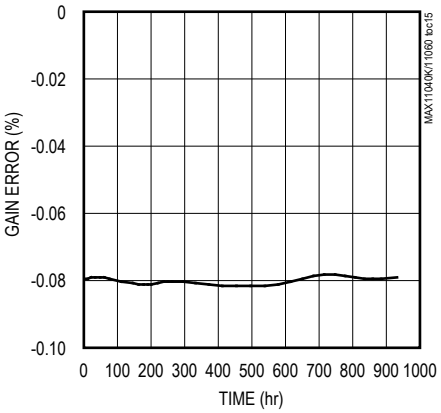
GAIN ERROR vs. SUPPLY VOLTAGE



GAIN ERROR vs. TEMPERATURE



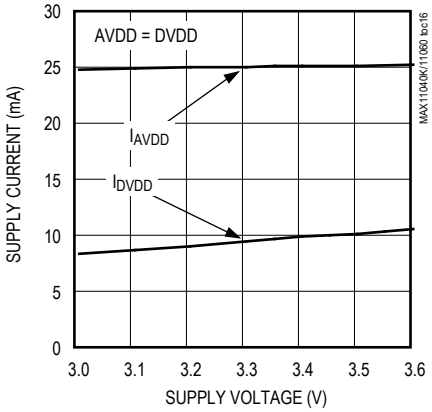
GAIN ERROR DRIFT



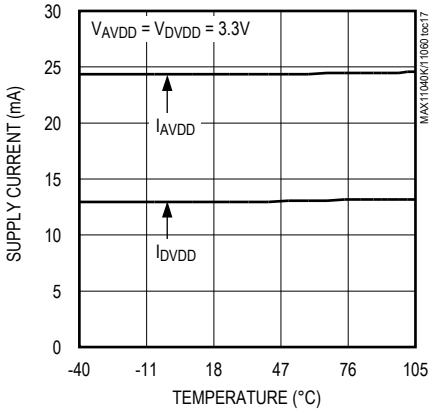
Typical Operating Characteristics (MAX11040K) (continued)

(V_{AVDD} = V_{DVDD} = 3.3V, $f_{XIN\ CLOCK}$ = 24.576MHz, f_{OUT} = 16ksps, V_{REFIO} = 2.5V (external), C_{REFIO} = C_{REF0} = C_{REF1} = C_{REF2} = C_{REF3} = 1µF, T_A = +25°C, unless otherwise noted.)

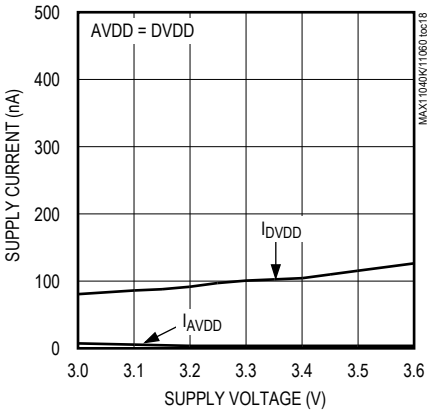
SUPPLY CURRENT vs. SUPPLY VOLTAGE



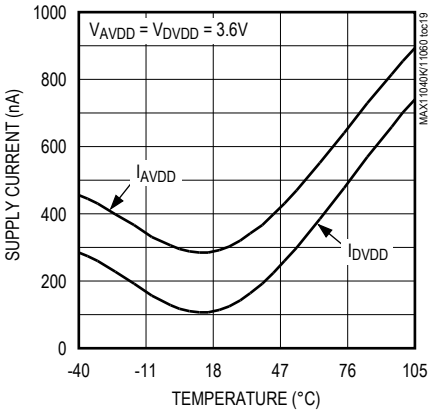
SUPPLY CURRENT vs. TEMPERATURE



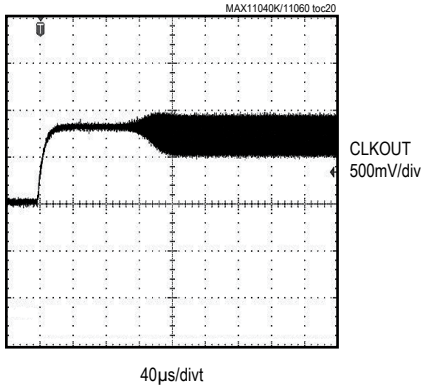
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



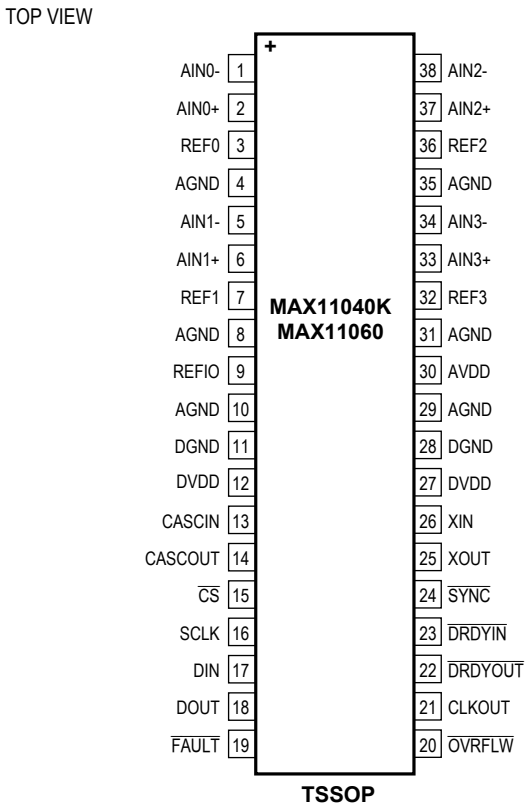
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



CRYSTAL OSCILLATOR STARTUP TIME



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	AIN0-	Negative Analog Input Channel 0
2	AIN0+	Positive Analog Input Channel 0
3	REF0	ADC0 Buffered Reference Voltage. Bypass REF0 with a 1µF capacitor to AGND.
4, 8, 10, 29, 31, 35	AGND	Analog Ground
5	AIN1-	Negative Analog Input Channel 1
6	AIN1+	Positive Analog Input Channel 1
7	REF1	ADC1 Buffered Reference Voltage. Bypass REF1 with a 1µF capacitor to AGND.
9	REFIO	Reference Voltage Output/Input. Reference voltage for analog-to-digital conversion. In internal reference mode, the reference buffer provides a +2.5V nominal output. In external reference mode, overdrive REFIO with an external reference between 2.3V to 2.7V. Bypass REFIO with a 1µF capacitor to AGND.

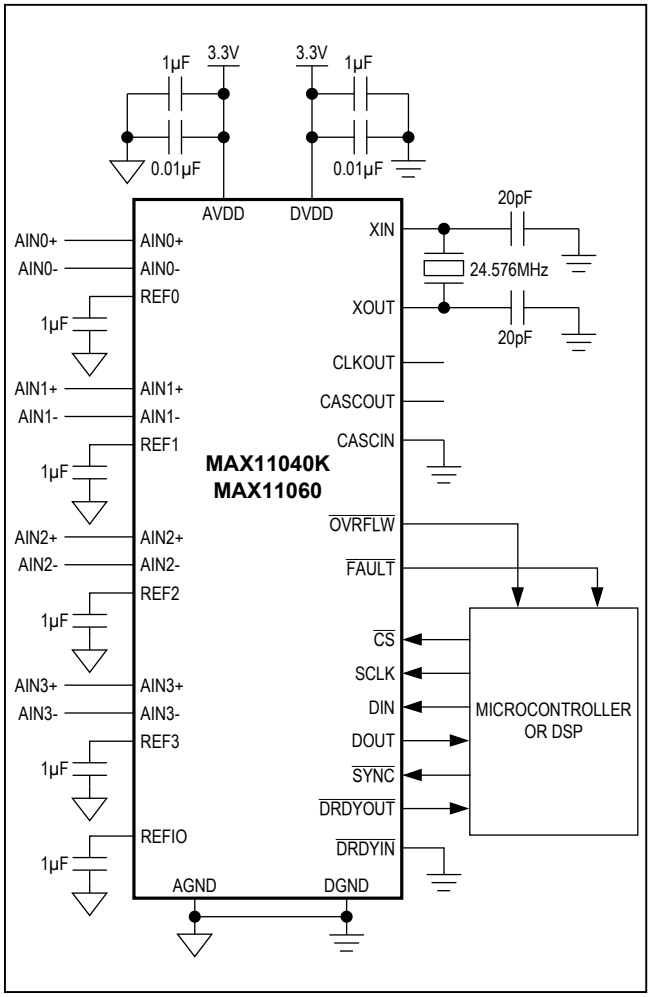
Pin Description (continued)

PIN	NAME	FUNCTION
11, 28	DGND	Digital Ground
12, 27	DVDD	Positive Digital Supply Voltage. Bypass each DVDD to DGND with a 1µF capacitor in parallel with a 0.01µF capacitor as close as possible to the device.
13	CASCIN	Cascade Input. A logic-low on CASCIN while $\overline{CS}$ is a logic-low during the last cycle of a byte signals the device to perform the requested data transfer during subsequent bytes using DIN and DOUT. Once the requested transfer is completed, the part three-states DOUT and ignores DIN until a new command is issued. CASCIN is clocked in at the rising edge of SCLK. Connect CASCIN to DGND when not daisy chaining multiple devices. See the *Multiple Device Connection* section for connection recommendations.
14	CASCOUT	Cascade Output. CASCOUT is driven low during the last cycle of the last byte of a data transfer to signal the next device in the daisy-chain to begin transferring data on the next byte. CASCOUT changes after the rising edge of SCLK. Leave CASCOUT unconnected when not daisy chaining multiple devices. See the *Multiple Device Connection* section.
15	$\overline{CS}$	Active-Low Chip-Select Input. A falling edge on $\overline{CS}$ while CASCIN is a logic-low enables DIN and DOUT for data transfer. A logic-high on $\overline{CS}$ prevents data from being clocked in on DIN and places DOUT in a high-impedance state.
16	SCLK	Serial-Clock Input. Clocks in data at DIN on the falling edge of SCLK and clocks out data at DOUT on the rising edge of SCLK. SCLK must idle high (CPOL = 1).
17	DIN	Serial Data Input. Data at DIN is clocked in on the falling edge of SCLK.
18	DOUT	Serial Data Output. The drive for DOUT is enabled by a falling edge on $\overline{CS}$ while CASCIN is low or by a falling edge on CASCIN while $\overline{CS}$ is low. DOUT is disabled/three-stated when $\overline{CS}$ is high or after the appropriate number of data bytes have been transferred in response to the requested command. Data is clocked out at DOUT on the rising edge of SCLK.
19	$\overline{FAULT}$	Active-Low Overvoltage Fault Indicator Output. $\overline{FAULT}$ goes low when any analog input goes outside the fault threshold range (between V_{PFT} and V_{NFT}). The $\overline{FAULT}$ output is open drain with a 30kΩ internal pullup resistor, allowing wire-NOR functionality. See the *Analog Input Overvoltage and Fault Protection* section.
20	$\overline{OVRFLW}$	Active-Low Channel Data Overflow Output. $\overline{OVRFLW}$ goes low when a conversion result goes outside the voltage range bounded by the positive and negative full scale on one or more of the analog input channels or when $\overline{FAULT}$ goes low. The $\overline{OVRFLW}$ output is open drain with a 30kΩ internal pullup resistor, allowing wire-NOR functionality. See the *Analog Input Overvoltage and Fault Protection* section.
21	CLKOUT	Buffered Clock Output. When the XTALEN bit in the configuration register is 1 and a crystal is installed between XIN and XOUT, CLKOUT provides a buffered version of the internal oscillator's clock. Setting the XTALEN bit to 0 places CLKOUT in a high-impedance state.

Pin Description (continued)

PIN	NAME	FUNCTION
22	$\overline{\text{DRDYOUT}}$	Active-Low Data Ready Output. When $\overline{\text{DRDYIN}}$ = 0, $\overline{\text{DRDYOUT}}$ outputs a logic-low to indicate the availability of a new conversion result. $\overline{\text{DRDYOUT}}$ transitions high at the next $\overline{\text{CS}}$ falling edge or when $\overline{\text{DRDYIN}}$ = 1. See the *Multiple Device Connection* section.
23	$\overline{\text{DRDYIN}}$	Active-Low Data Ready Input. A logic-high at $\overline{\text{DRDYIN}}$ causes $\overline{\text{DRDYOUT}}$ to output a logic-high. When $\overline{\text{DRDYIN}}$ = 0, $\overline{\text{DRDYOUT}}$ outputs a logic-low when a new conversion result is available. See the *Multiple Device Connection* section. Connect $\overline{\text{DRDYIN}}$ to DGND when not daisy chaining multiple devices.
24	$\overline{\text{SYNC}}$	Sampling Synchronization Input. The falling edge of $\overline{\text{SYNC}}$ aligns sampling and output data so that multiple devices sample simultaneously. Synchronize multiple devices running from independent crystals by connecting $\overline{\text{DRDYOUT}}$ of the last device in the chain to the $\overline{\text{SYNC}}$ inputs of all devices in the chain. Connect $\overline{\text{SYNC}}$ to DGND for single device operation. See the *Multiple Device Connection* section.
25	XOUT	Crystal Oscillator Output. Connect a 24.576MHz external crystal or resonator between XIN and XOUT when using the internal oscillator. Leave XOUT unconnected when driving with an external frequency. See the *Crystal Oscillator* section.
26	XIN	Crystal Oscillator/Clock Input. Connect a 24.576MHz external crystal or resonator between XIN and XOUT when using the internal oscillator or drive XIN with an external clock and leave XOUT unconnected. See the *Crystal Oscillator* section.
30	AVDD	Positive Analog Supply Voltage. Bypass to AGND with a 1µF capacitor in parallel with a 0.01µF capacitor as close as possible to the device.
32	REF3	ADC3 Buffered Reference Voltage. Bypass with a 1µF capacitor to AGND.
33	AIN3+	Positive Analog Input Channel 3
34	AIN3-	Negative Analog Input Channel 3
36	REF2	ADC2 Buffered Reference Voltage. Bypass with a 1µF capacitor to AGND.
37	AIN2+	Positive Analog Input Channel 2
38	AIN2-	Negative Analog Input Channel 2

Typical Operating Circuit



Detailed Description

The MAX11040K/MAX11060 are 24-/16-bit, simultaneous-sampling, 4-channel, sigma-delta ADCs including support for synchronized sampling and daisy chaining of the serial interface across multiple (up to eight) devices. The serial interface of the set of synchronized devices behaves as one device. Each channel includes a differential analog input, a sigma-delta modulator, a digital decimation filter, an independent programmable sampling delay, and a buffered reference signal from the internal or an external reference. The device contains an internal crystal oscillator. The output data rate, the effective sample rate of the ADC, is software programmable.

The devices operate from a single 3.0V to 3.6V analog supply and a 2.7V to V_{AVDD} digital supply. The 4-wire serial interface is SPI/QSPI/MICROWIRE and DSP compatible.

ADC Modulator

Each channel of the devices performs analog-to-digital conversion on its input using a dedicated switched-capacitor sigma-delta modulator. The modulator converts the input signal into low-resolution digital data for which the average value represents the digitized signal information at 3.072Msps for a 24.576MHz XIN clock. This data stream is then presented to the digital filter for processing to remove the high-frequency noise that creates a high-resolution 24-/16-bit output data stream.

The input sampling network of the analog input consists of a pair of 4pF capacitors (C_{SAMPLE}), the bottom plates of which are connected to AIN_+ and AIN_- during the track phase and then shorted together during the hold phase (see Figure 1). The internal switches have a total series resistance of 400Ω. Given a 24.576MHz XIN clock, the switching frequency is 3.072MHz. The sampling phase lasts for 120ns.

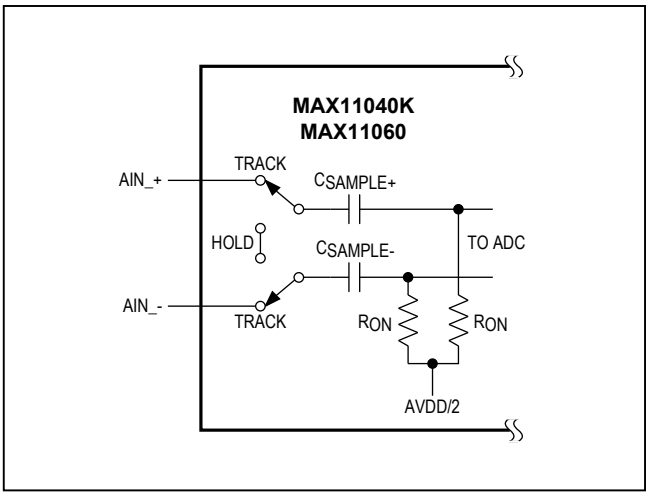


Figure 1. Simplified Track/Hold Stage

Digital Filter

The devices contain an on-chip digital lowpass filter that processes the data stream from each modulator and generates the high-resolution output data. The lowpass filter frequency response is determined by the programmable output data rate. At the nominal 16ksps output data rate, the -3dB bandwidth of the filter is 3.4kHz. The passband flatness is better than ±0.1dB from 0 to 1.74kHz. The notches are located at 5.75kHz and 7.195kHz. These frequencies scale linearly with the output data rate. See Figure 2 and Table 1 for the frequency response at different data rates.

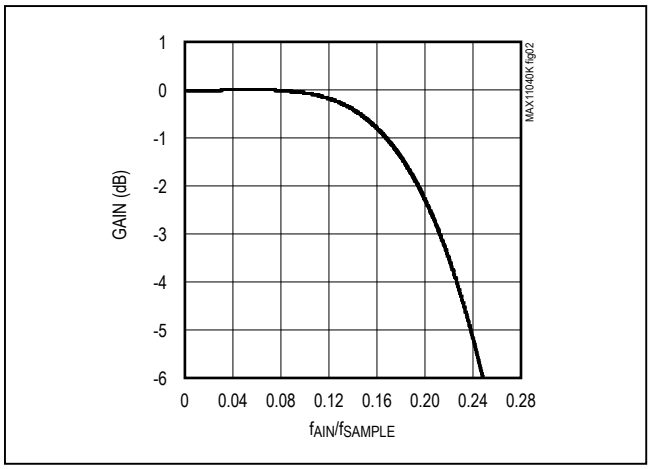


Figure 2. Digital Filter Response

Table 1. Bandwidth vs. Output Data Rate

OUTPUT DATA RATE (ksps)	-3dB BANDWIDTH (kHz)	-0.1dB BANDWIDTH (kHz)
0.5	0.11	0.05
1	0.21	0.11
2	0.42	0.22
4	0.85	0.43
8	1.69	0.87
10	2.11	1.09
12	2.54	1.31
16	**3.38**	**1.74**
32	6.78	3.48
64	13.5	6.96

Since the transfer function of a digital filter is repeatable and predictable, it is possible to correct for frequency-dependent attenuation in downstream software. See the *Compensating for the Rolloff of the Digital Filter in a Typical FFT Analysis* section. The transfer function is defined by the following equation:

$$Gain(f_{AIN}) = \left(\frac{f_{SAMPLE} \times \sin\left(\pi \times \frac{f_{AIN}}{f_{SAMPLE}}\right)}{f_{XINCLOCK} \times \sin\left(\pi \times \frac{f_{AIN}}{f_{XINCLOCK}}\right)} \right)^3 \times (FIR_Gain(f_{AIN}))$$

where:

Gain is the filter gain.

f_{AIN} is the analog input frequency.

f_{SAMPLE} is the programmed output data rate, nominally 16kHz.

$f_{XINCLOCK}$ is the clock frequency at XIN, nominally 24.576MHz.

FIR_Gain (f_{AIN}) is the normalized gain of the FIR filter with the following filter coefficients, as a function of the analog input frequency f_{AIN}. These coefficients are applied at the output data rate:

+ 0.022
- 0.074
- 0.036
+ 0.312
+ 0.552
+ 0.312
- 0.036
- 0.074
+ 0.022

Modulator Clock

The modulator clock is created by dividing the frequency at the XIN input by a factor of 8. The XIN input is driven either directly by an external clock or by the on-chip crystal oscillator.

Crystal Oscillator

The on-chip oscillator requires an external crystal (or resonator) with a 24.576MHz operating frequency connected between XIN and XOUT, as shown in Figure 3. As in any crystal-based oscillator circuit, the oscillator frequency is sensitive to the capacitive load (C_L). C_L is the capacitance that the crystal needs from the oscillator circuit and not the capacitance of the crystal. The input capacitance across XIN and XOUT is 1.5pF.

Choose a crystal with a 24.576MHz oscillation frequency and an ESR less than 30Ω, such as the MP35 from RXD Technologies. See Figure 3 for the block diagram of the crystal oscillator. Set XTALEN = 1 in the configuration register to enable the crystal oscillator. The CLKOUT output provides a buffered version of the clock that is capable of driving eight devices, allowing synchronized operation from a single crystal. See the *Multiple Device Synchronization* section in the *Applications Information* section.

External Clock

To use an external clock, set XTALEN = 0 in the Configuration register and connect an external clock source (20MHz to 25MHz) to XIN. CLKOUT becomes high impedance.

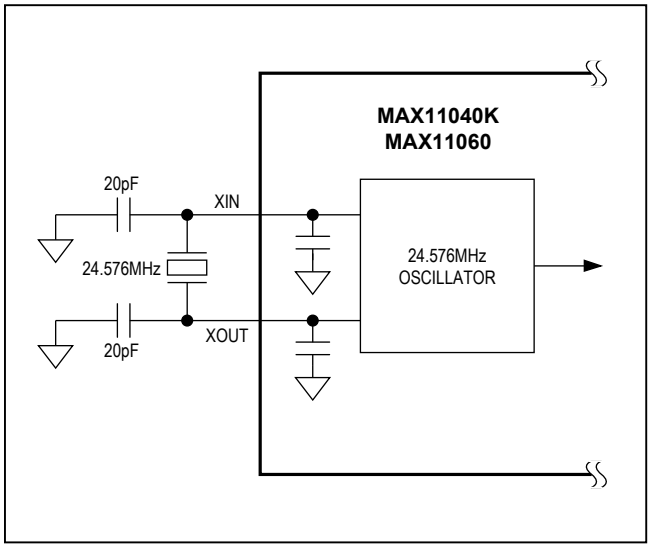


Figure 3. Crystal Oscillator Input

Analog Input Overvoltage and Fault Protection

The full-scale differential input range of the devices is ±0.88V_{REF}. The converter accurately represents any input for which the positive and negative analog inputs are separated by a magnitude of less than 0.88V_{REF}.

The device includes special circuitry that protects it against voltages on the analog inputs up to ±6V. Setting FAULTDIS = 1 disables the protection circuitry.

There are two mechanisms of overvoltage detection and protection: full-scale overflow and overvoltage fault. Full-scale overflow occurs if the magnitude of the applied input voltage on any one or more channels is greater than 0.88V_{REF}. In this case, the digital output is clipped to positive or negative full scale and the $\overline{OVRFLW}$ flag goes low. Overvoltage fault occurs if the magnitude of an applied input voltage on any one or more channels goes outside the fault-detection thresholds. The reaction to an overvoltage fault is dependent on whether the fault-protection circuitry is enabled. If enabled, the input-protection circuits engage and the $\overline{FAULT}$ flag goes low. A full-scale overflow or an overvoltage fault condition on any one channel does not affect the output data for the other channels.

The input protection circuits allow up to ±6V relative to AGND on each input, and up to ±6V differentially between AIN+ and AIN-, without damaging the devices only if the following conditions are satisfied: power is applied, the devices are not in shutdown mode, a clock frequency of at least 20MHz is available at XIN, and FAULTDIS = 0. The analog inputs allow up to ±3.5V relative to AGND when either devices are placed in shutdown mode, the clock stops, or FAULTDIS = 1.

During an overvoltage fault condition, the impedance between AIN_+ and AIN_- reduces to as low as 0.5kΩ.

The output structure and cascading features of $\overline{FAULT}$ and $\overline{OVRFLW}$ are discussed in the *Multiple Device Digital Interface* section.

Analog Input Overflow Detection and Recovery ($\overline{OVRFLW}$)

The $\overline{OVRFLW}$ flag is set based on the ADC conversion result. When the applied voltage on one or more analog inputs goes outside the positive or negative full scale (±0.88V_{REF}), $\overline{OVRFLW}$ asserts after a delay defined by the latency of the converter, coincident with the $\overline{DRDYOUT}$ of the full-scale clamped conversion result (see Figure 4). The specifics of the latency are discussed earlier in the data sheet in the *Latency* section.

When the analog input voltage changes between the ADC full scale and the fault threshold faster than the latency of the converter, $\overline{OVRFLW}$ goes low with the $\overline{FAULT}$ output. $\overline{OVRFLW}$ remains invalid until a valid clock frequency is available at XIN.

Overvoltage-Fault Detection and Recovery ($\overline{FAULT}$)

With overvoltage-fault protection enabled (FAULTDIS = 0), $\overline{FAULT}$ immediately transitions from a high to low when any of the analog inputs go outside the voltage range bounded by the fault-detection thresholds V_{PFT} and V_{NFT}.

Once the analog inputs return back within the fault thresholds, the $\overline{FAULT}$ interrupt output goes high after a delay called the fault-recovery time. The fault-recovery time is:

$$20 \times t_{DOUT} < \text{fault-recovery time} < 25 \times t_{DOUT}$$

where t_{DOUT} is the data output period determined by $f_{XINCLOCK}$ and the selected output data rate.

In the event the analog input voltage changes between the ADC full scale and the fault threshold faster than the latency of the converter, the ADC conversion result prematurely jumps to the full-scale value when a fault is detected (see Detection Discontinuity in Figure 4). During a fault condition and the subsequent fault-recovery time, the ADC conversion result remains at full scale. This creates a discontinuity in the digital conversion result only if the fault recovery time is greater than the latency plus the time that the input changes between the fault threshold and the ADC full scale (see Recovery Discontinuity in Figure 4). Neither of these steps occur if the fault-protection circuitry is disabled (FAULTDIS = 1), or if the input is slow relative to the above descriptions (see Figure 5).

For data rates faster than 32ksps (FSAMPC = 111), the converter output may contain invalid data for up to 188µs after $\overline{FAULT}$ returns high. To prevent this behavior, disable the overvoltage-fault protection by setting the FAULTDIS bit in the configuration register to 1 when using FSAMPC = 111, and limit the analog input swing to ±3.5V.

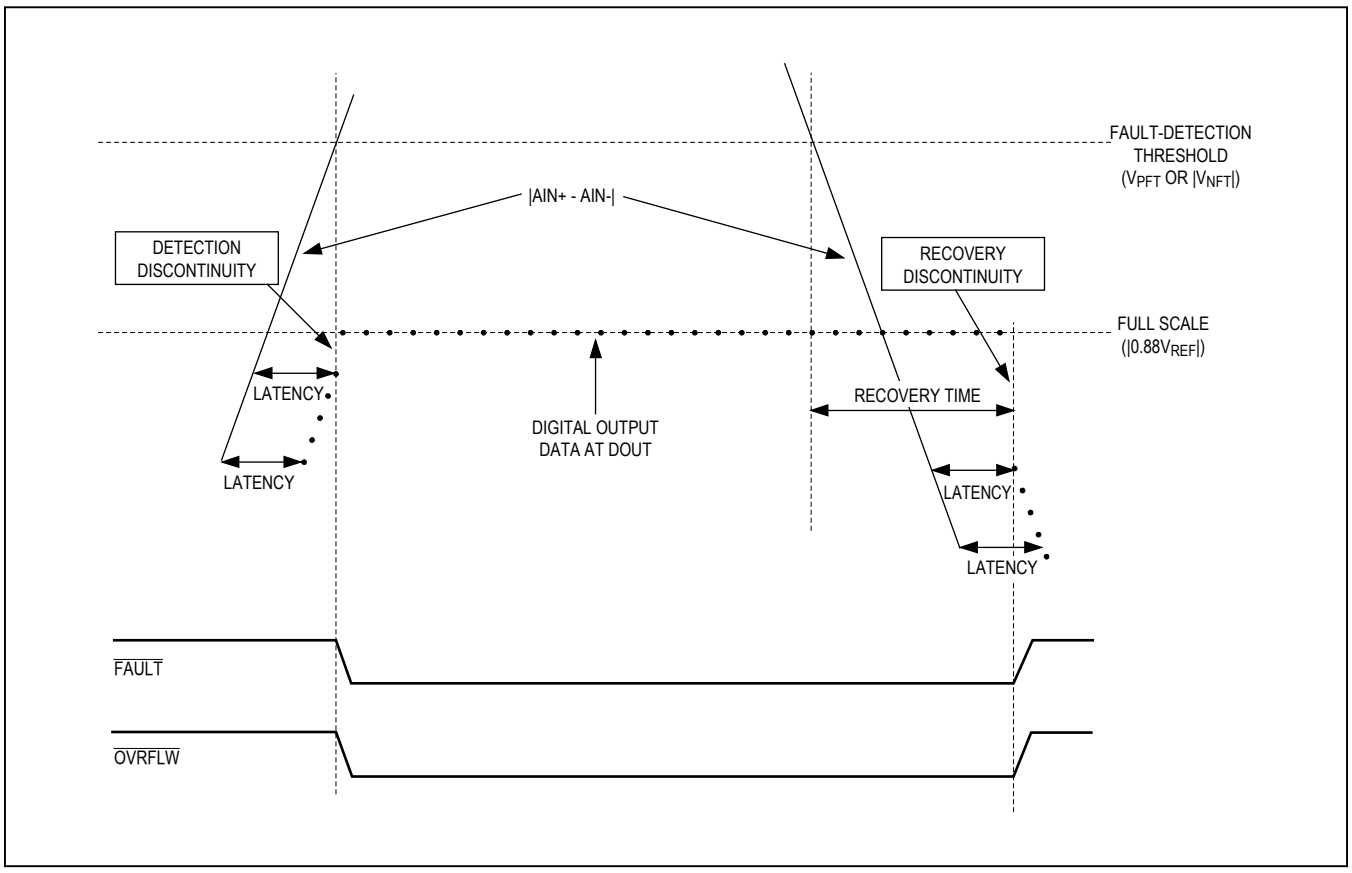


Figure 4. High-Frequency Analog Input Overvoltage Detection and Recovery

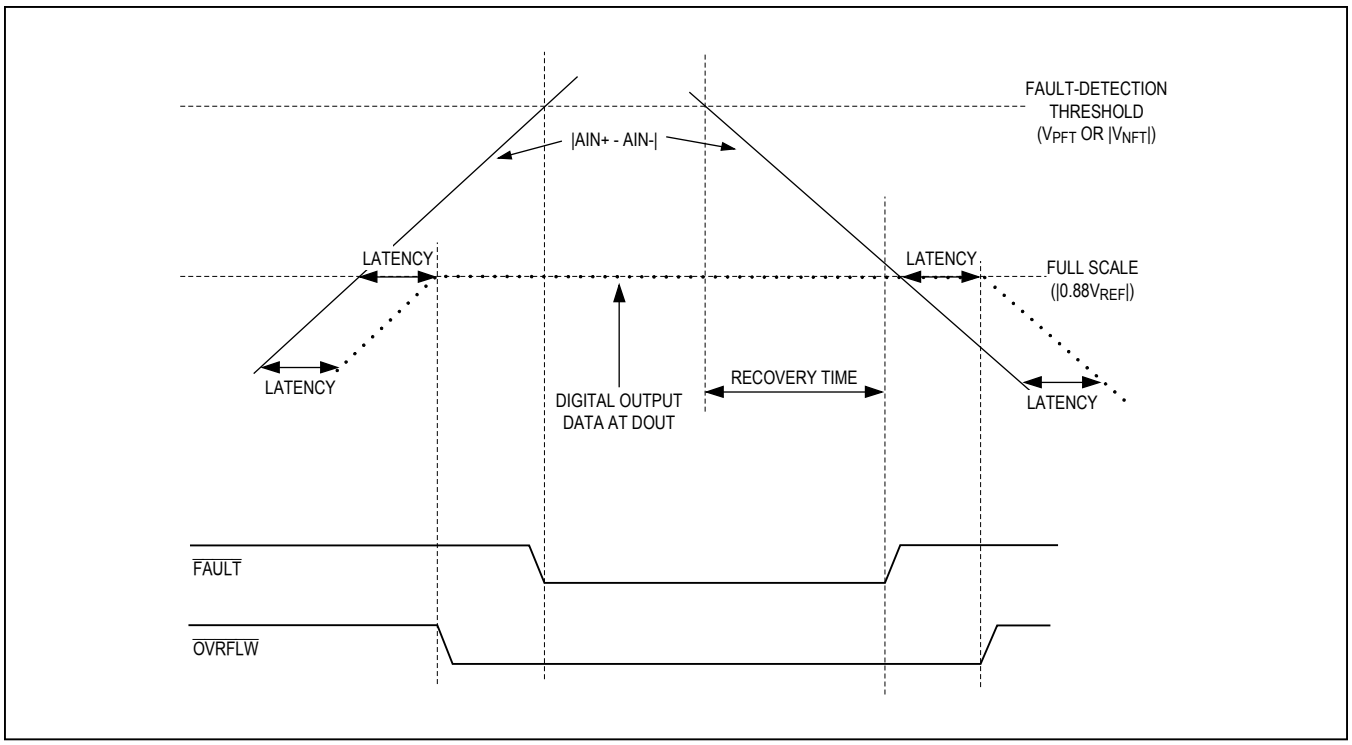


Figure 5. Low-Frequency Analog Input Overvoltage Detection and Recovery

Reference

The devices operate with either a +2.5V internal band-gap reference or an external reference source between +2.3V and +2.7V applied at REFIO. Bypass REFIO and each REF_ to AGND with a 1µF capacitor. The reference voltage sets the positive and negative full-scale voltage according to the following formula:

$$\pm FS = \pm 0.88\ V_{REFIO}$$

The reference voltage at REFIO (external or internal) is individually buffered to generate the reference voltages at REF0 to REF3 (see Figure 6.) These independent buffers minimize the potential for crosstalk between each of the internal ADCs.

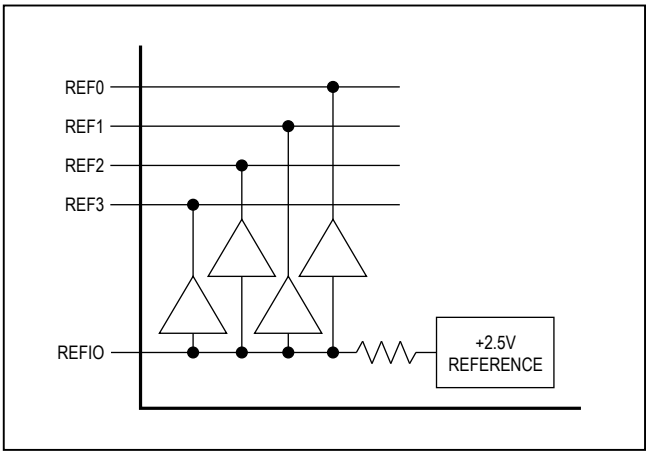


Figure 6. REFIO Input

Serial Interface

The devices' interface is fully compatible with SPI/DSP standard serial interfaces (compatible with SPI modes CPOL = 1, CPHA = 0). The serial interface provides access to four on-chip registers: Sampling Instant Control register (32 bits), Data Rate Control register (16 bits), Configuration register (8 bits), and Data register (96 bits). All serial-interface commands begin with a command byte, which addresses a specific register, followed by data bytes with a data length that depends on the specific register addressed and the number of devices cascaded (see Figures 7, 8, and the *Registers* section).

The serial interface consists of eight signals: $\overline{CS}$, SCLK, DIN, DOUT, CASCIN, CASCOUT, $\overline{DRDYIN}$, and $\overline{DRDYOUT}$. CASCIN, CASCOUT, $\overline{DRDYIN}$, and $\overline{DRDYOUT}$ are used for daisy chaining multiple devices together. See the *Multiple Device Connection* section for details on how to connect CASCIN, CASCOUT, $\overline{DRDYIN}$,

and $\overline{\text{DRDYOUT}}$. For single-device applications, connect CASCIN and $\overline{\text{DRDYIN}}$ to DGND and drive $\overline{\text{CS}}$ low to transfer data in and out of the devices. With $\overline{\text{DRDYIN}}$ low, a falling edge at the data-ready signal output ($\overline{\text{DRDYOUT}}$) indicates that new conversion results are available for reading in the 96-bit data register. A falling edge on SCLK clocks in data at DIN. Data at DOUT changes on the rising edge of SCLK and is valid on the falling edge of SCLK. DIN and DOUT are transferred MSB first. Drive $\overline{\text{CS}}$ high to disable the interface and place DOUT in a high-impedance state.

An interface operation with the devices takes effect on the last rising edge of SCLK. If $\overline{\text{CS}}$ goes high before the complete transfer, the write is ignored. Every data transfer is initiated by the command byte. The command byte consists of an R/$\overline{\text{W}}$ bit and 7 address bits (see Table 2.) Figures 7 and 8 show the timing for read and write operations, respectively.

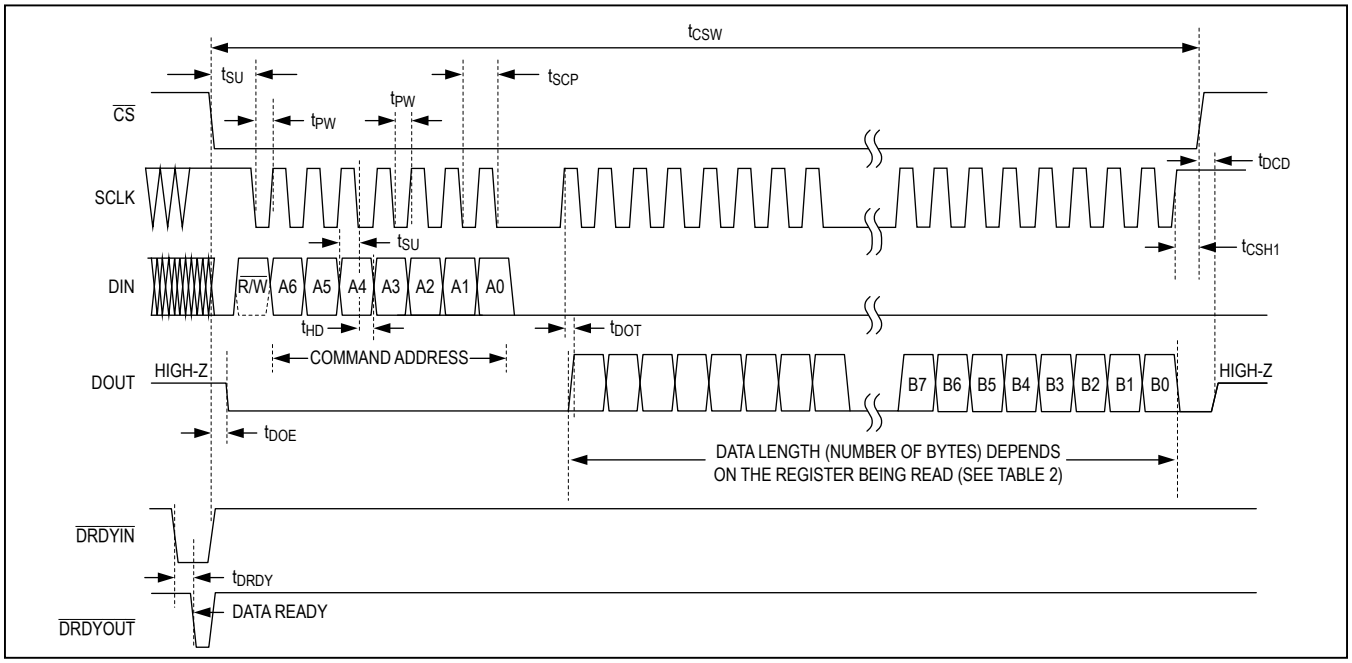


Figure 7. General Read-Operation Timing Diagram

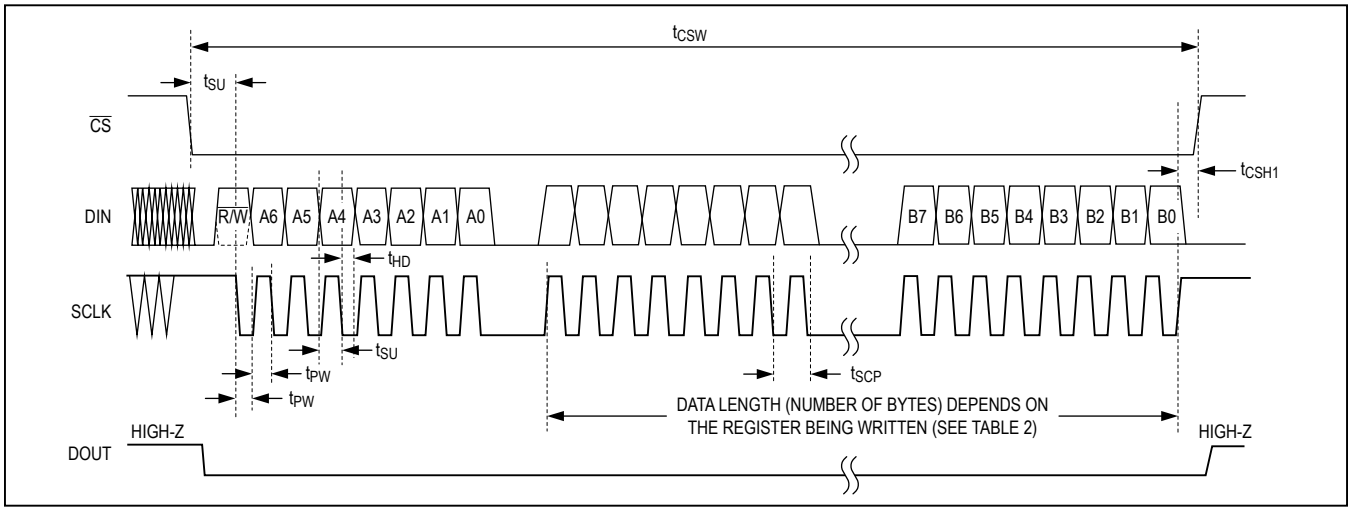


Figure 8. General Write-Operation Timing Diagram

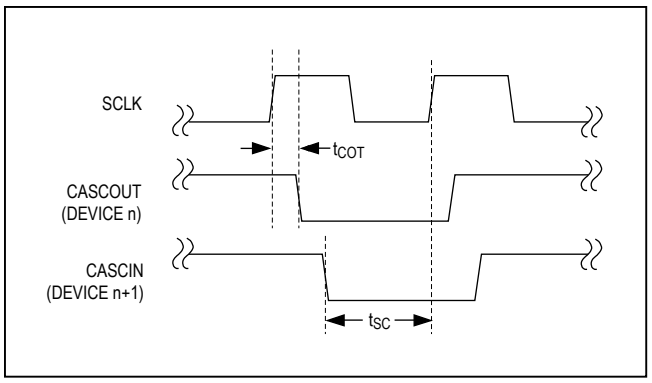


Figure 9. CASCIN and CASCOUT Timing Diagram

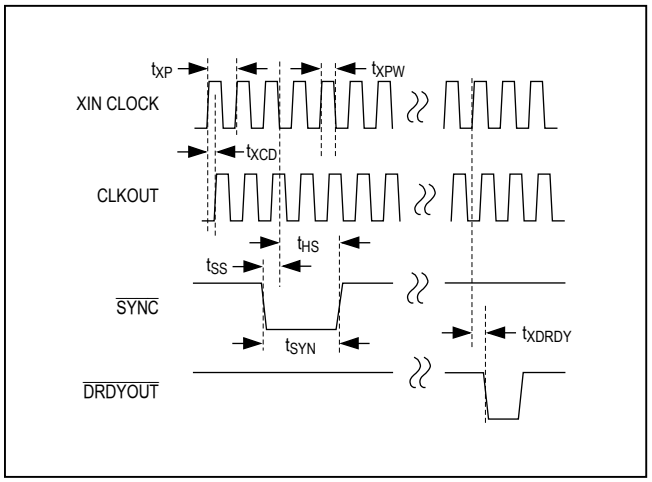


Figure 10. XIN Clock, CLKOUT, SYNC, and DRDYOUT Timing Diagram

Registers

The devices include four registers accessible by 7 command bytes. The command bytes provide read and write access to the Data Rate Control register, the Sampling Instant Control register, and the Configuration register, and read access to the Data register. See Table 2. Figure 9 shows the CASCIN and CASOUT timing diagram. Figure 10 is the XIN clock, CLKOUT, SYNC, and DRDYOUT timing diagram.

Table 2. Command Bytes

R/W	ADDRESS [A6:A0]	DATA LENGTH*	FUNCTION
0	1000000	32 x n** bits	Write Sampling Instant Control Register
1	1000000	32 x n bits	Read Sampling Instant Control Register
0	1010000	16 bits	Write Data-Rate Control Register
1	1010000	16 bits	Read Data-Rate Control Register
0	1100000	8 x n bits	Write Configuration Register
1	1100000	8 x n bits	Read Configuration Register
1	1110000	96 x n bits	Read Data Register

**All data lengths are proportional to the number of cascaded devices except for reads and writes to the Data Rate Control register. When accessing the Data Rate Control register, the data length is fixed at 16 bits. These 16 bits are automatically written to all cascaded devices.*

***n is the total number of cascaded devices.*

Sampling Instant Control Register

By default, the devices sample all 4 input channels simultaneously. To delay the sampling instant on one or more channels, program the appropriate byte in the Sampling Instant Control register. The delay of the actual sampling instant of each individual channel from the default sampling instant (PHI_[7:0] = 0x00) is adjustable between 32 to 819,121 XIN clock cycles, which is 1.3µs to 333µs with $f_{XINCLOCK}$ at 24.576MHz (see Table 3.)

Configuration Register

The Configuration register contains 5 bits that control the functionality of the devices. The default state is 0x00.

The data length of the Configuration register is 8 bits per cascaded device (see Table 4).

Table 3. Sampling Instant Control Register

BIT	NAME	DESCRIPTION
[31:24]	PHI0[7:0]	Channel 0 sample instant adjust. PHI0 delays sampling instant on channel 0 by 32 XIN clock cycles per LSB, up to 8192 cycles total (1.3µs resolution; 333µs range at XIN of 24.576MHz).
[23:16]	PHI1[7:0]	Channel 1 sample instant adjust. PHI1 delays sampling instant on channel 1 by 32 XIN clock cycles per LSB, up to 8192 cycles total (1.3µs resolution; 333µs range at XIN of 24.576MHz).
[15:8]	PHI2[7:0]	Channel 2 sample instant adjust. PHI2 delays sampling instant on channel 2 by 32 XIN clock cycles per LSB, up to 8192 cycles total (1.3µs resolution; 333µs range at XIN of 24.576MHz).
[7:0]	PHI3[7:0]	Channel 3 sample instant adjust. PHI3 delays sampling instant on channel 3 by 32 XIN clock cycles per LSB, up to 8192 cycles total (1.3µs resolution; 333µs range at XIN of 24.576MHz).

Table 4. Configuration Register

BIT	NAME	DESCRIPTION
7	SHDN	Shutdown bit. Set SHDN high to place the device in shutdown mode. In shutdown mode, the internal oscillator, fault circuitry, and internal bandgap reference are turned off. Set SHDN low for normal operation.
6	RST	Reset bit. Set RST high to reset all registers to the default states except for the RST bit, and realign sampling clocks and output data.
5	EN24BIT	Enable 24-bit resolution bit for the MAX11040K. Set EN24BIT high to enable the 24-bit data output. Set EN24BIT low to enable 19-bit data output with device address and channel address tags. Tables 5 and 6 specify the Data register for both states of this bit. Set to 0 for MAX11060.
4	XTALEN	Internal oscillator enable bit. When using the on-chip crystal oscillator as the clock source, set XTALEN high to enable the crystal oscillator and provide a buffered version of the crystal clock at the CLKOUT output. When using an external clock source, set XTALEN low to disable the internal crystal oscillator and three-state the CLKOUT output. Connect the external clock source to the XIN input.
3	FAULTDIS	Overvoltage fault-protection disable bit. Set FAULTDIS high to disable the overvoltage fault-protection circuits. For FAULTDIS = 0, the absolute maximum input range is ±6V. Analog inputs beyond the fault-detection threshold range trip the fault-protection circuits. The output remains clipped for a fault-recovery time (typically < 1.57ms) after the inputs return within the fault-detection threshold range. For FAULTDIS = 1, the absolute maximum input range is only ±3.5V, but there is no fault-recovery delay. See the *Overvoltage Fault Detection and Recovery (FAULT)* section.
2	PDBUF	PDBUF = 1 disables the internal reference buffer. Use this mode when an external reference is used; otherwise, PDBUF should be set to 0 to enable the internal reference buffer.
[1:0]	Reserved	**Must set to 0.**

Data Register

The Data register contains the results of the ADC conversion. The result is reported in two's complement format. The register contains one or two pieces of information, depending on the state of EN24BIT in the Configuration register. When EN24BIT is set to zero, the Data register contains the ADC data truncated to 19 bits, followed by the device and channel addresses (see Table 5). When EN24BIT is set to one, the data contained in the Data register represents the 24-bit conversion (see Table 6). The data length of the Data register is 96 bits for each cascaded device. Figure 11 shows the sequence of the conversion result output of all channels for two cascaded devices. Table 7 is the data register for the MAX11060.

If the results are not read back prior to completion of the next conversion, the data is overwritten.

Table 5. Data Register (EN24BIT = 0) (MAX11040K)

BIT	NAME	DESCRIPTION
[95:77]	CH0DATA[18:0]	Channel 0 19-bit conversion result (two's complement)
[76:74]	IC[2:0]	Device address tag. IC[2:0] starts with 000 for the device nearest the master.
[73:72]	00	Channel 0 address tag = 00
[71:53]	CH1DATA[18:0]	Channel 1 19-bit conversion result (two's complement)
[52:50]	IC[2:0]	Device address tag. IC[2:0] starts with 000 for the device nearest the master.
[49:48]	01	Channel 1 address tag = 01
[47:29]	CH2DATA[18:0]	Channel 2 19-bit conversion result (two's complement)
[28:26]	IC[2:0]	Device address tag. IC[2:0] starts with 000 for the device nearest the master.
[25:24]	10	Channel 2 address tag = 10
[23:5]	CH3DATA[18:0]	Channel 3 19-bit conversion result (two's complement)
[4:2]	IC[2:0]	Device address tag. IC[2:0] starts with 000 for the device nearest the master.
[1:0]	11	Channel 3 address tag = 11

Table 6. Data Register (EN24BIT = 1) (MAX11040K)

BIT	NAME	DESCRIPTION
[95:72]	CH0DATA[23:0]	Channel 0 24-bit conversion result (two's complement)
[71:48]	CH1DATA[23:0]	Channel 1 24-bit conversion result (two's complement)
[47:24]	CH2DATA[23:0]	Channel 2 24-bit conversion result (two's complement)
[23:0]	CH3DATA[23:0]	Channel 3 24-bit conversion result (two's complement)

Table 7. Data Register (MAX11060)

BIT	NAME	DESCRIPTION
[95:80]	CH0DATA[15:0]	Channel 0 16-bit conversion result (two's complement)
[79:77]	000	—
[76:74]	IC[2:0]	Device address tag. IC[2:0] starts with 000 for the device nearest the master.
[73:72]	00	Channel 0 address tag = 00
[71:56]	CH1DATA[15:0]	Channel 1 16-bit conversion result (two's complement)
[55:53]	000	—
[52:50]	IC[2:0]	Device address tag. IC[2:0] starts with 000 for the device nearest the master.
[49:48]	01	Channel 1 address tag = 01
[47:32]	CH2DATA[15:0]	Channel 2 16-bit conversion result (two's complement)

Table 7. Data Register (MAX11060) (continued)

BIT	NAME	DESCRIPTION
[31:29]	000	—
[28:26]	IC[2:0]	Device address tag. IC[2:0] starts with 000 for the device nearest the master.
[25:24]	10	Channel 2 address tag = 10
[23:8]	CH3DATA[15:0]	Channel 3 16-bit conversion result (two's complement)
[7:5]	000	—
[4:2]	IC[2:0]	Device address tag. IC[2:0] starts with 000 for the device nearest the master.
[1:0]	11	Channel 3 address tag = 11

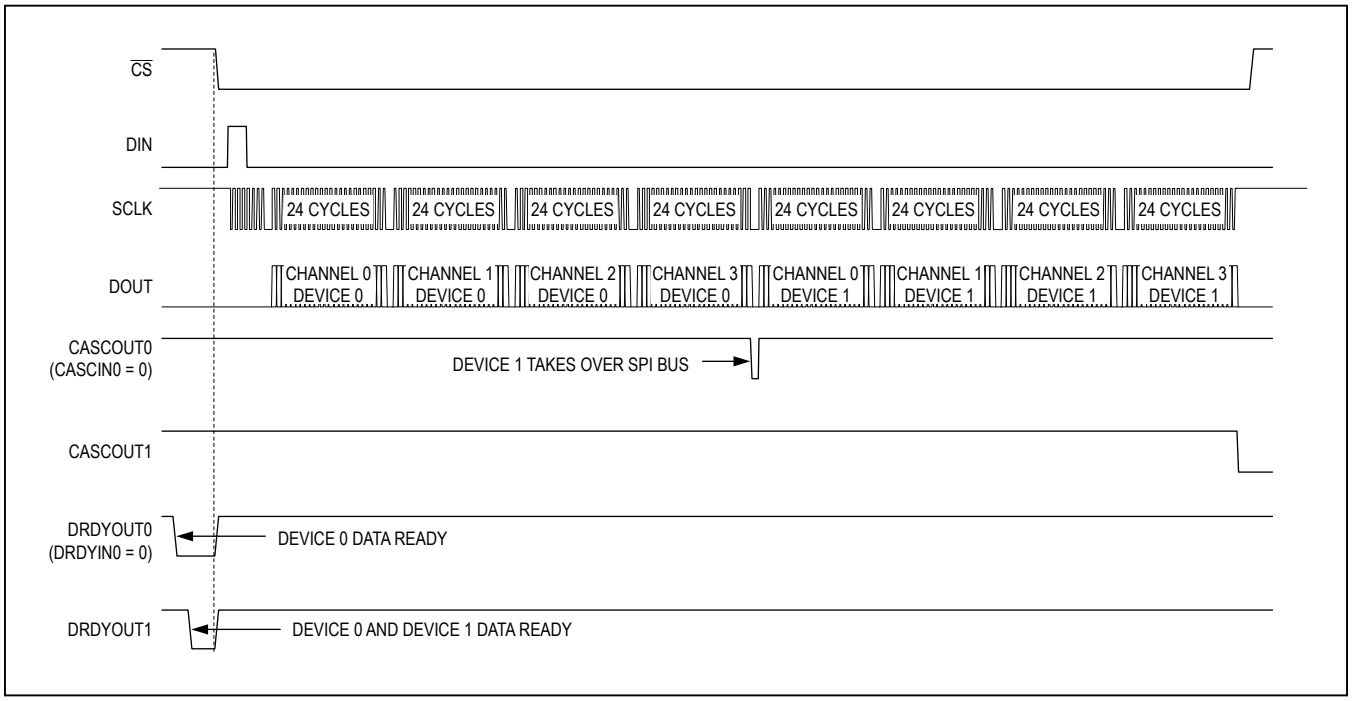


Figure 11. 192-Bit Data Read Operation Diagram for Two Cascaded Devices

Data Rate Control Register

The Data Rate Control register controls the output data period, which corresponds to the output data rate of the ADC. The data period is controlled by both a coarse (FSAMPC[2:0]) and a fine (FSAMPF[10:0]) adjustment (see Table 8).

The final data rate is derived by dividing the XIN clock frequency by a divider value. The divider value is a function of FSAMPC[2:0] and FSAMPF[10:0]:

$$\text{Data Rate} = f_{XINCLOCK}/\text{Divider}$$

$$\text{Divider} = \text{Coarse Cycle Factor} \times 384 + \text{Fine Cycle Factor} \times \text{FSAMPF[10:0]}$$

Note: Fractional results for the divider are rounded down to the nearest integer. Coarse cycle factor and fine cycle factor come from Table 8. The effect of FSAMPF[10:0] in the formula has limitations as noted in the table.

Examples of output data rate vs. FSAMPC[2:0] and FSAMPF[10:0] are shown in Table 9. Table 10 shows typical device performance for various data rate settings.

The data length of the Data-Rate Control register is 16 bits total for writes and reads (see Table 2). Changes to the Data-Rate Control register take effect after 16 conversion periods (Figure 12), i.e., the ADC continues to operate at the old data rate for another 16 periods. Also, the last sample at the old data rate (sample 16 in Figure 12) may contain some noise component and should be discarded. Changes in data rate should be limited to ±5% for correct operation. The data rate register should not be updated more than once every 32 data rate periods.

Note: Write to the data rate register in the time window of 10ns after the rising edge of $\overline{\text{DRDYOUT}}$ and 100ns before the falling edge of $\overline{\text{DRDYOUT}}$.

The digital filter determines the latency. Latency is defined as the time between the effective point in time that a sample is taken and when the resulting digital data is available for reading ($\overline{\text{DRDYOUT}}$ goes low). The latency of the converter is specified by the following equation:

$$\text{Latency} = (5.5 \times t_{DOUT}) + (\text{PHI} \times 1.3\mu s) + 30\mu s$$

where t_{DOUT} is the data output period (inverse of the programmed sample rate) determined by XINCLOCK and the selected output data rate, and PHI is the programmed sampling instant delay for the channel in question (0 ≤ PHI ≤ 255). The latency is approximately 374µs at 16ksps.

Because the two filters operate at different output data rates, a skew builds up between them over the 16 samples that both are in operation. For example, at 30ksps, the minimum data rate step size is 0.125%; so over 16 samples, the difference becomes 2%. This causes the period from sample 16 to sample 17 to be different by this amount.

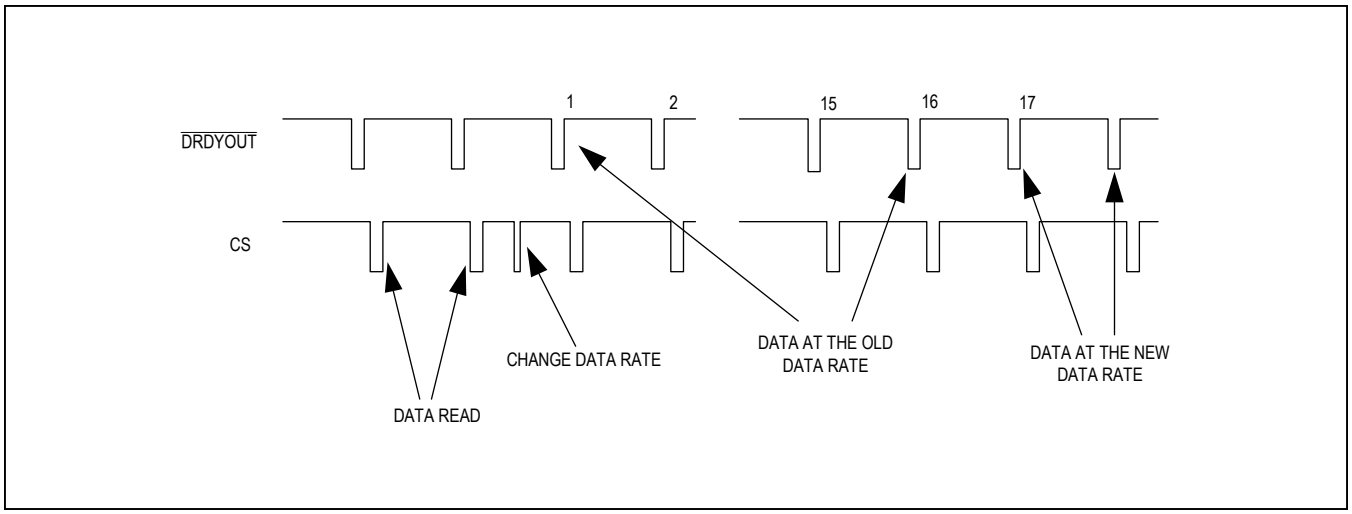


Figure 12. Timing Diagram for a Data-Rate Change

Table 8. Data-Rate Control Register

BITS	NAME	DESCRIPTION		
[15:13]	FSAMPC[2:0]	Output data rate coarse adjust bits. FSAMPC[2:0] sets the coarse cycle factor.		
		FSAMPC	Coarse Cycle Factor	Sample Rate in ksps ($f_{XIN\ CLOCK}$ = 24.576MHz)
		000	4	16
		001	128	0.5
		010	64	1
		011	32	2
		100	16	4
		101	8	8
		110	2	32
		111	1	64
[12:11]	Reserved	Set to 0.		
[10:0]	FSAMPF[10:0]	Output data rate fine adjusts bits. FSAMPF[10:0] increases the output data period by a number of XIN clock cycles. This number is the value of the register times the fine cycle factor. Values of FSAMPF greater than 1535 have no additional effect.		
		FSAMPC	XIN Fine Cycle Factor	
		000	1 cycle	
		001	32 cycles	
		010	16 cycles	
		011	8 cycles	
		100	4 cycles	
		101	2 cycles	
		110	1 cycle	
		111	1 cycle	

Table 9. Examples of Output Data Rate as a Function of FSAMPC[2:0] and FSAMPF[10:0]

FSAMPC[2:0]	FSAMPF[10:0]	OUTPUT DATA RATE (sps)	OUTPUT DATA PERIOD (24.576MHz CLOCK CYCLES)	FSAMPF OUTPUT DATA PERIOD RESOLUTION (24.576MHz CLOCK CYCLES)
001	11xxxxxxxxx	250.1	98272	32
	10111111111	250.1	98272	
	00000000001	499.7	49184	
	00000000000	500.0	49152	
010	11xxxxxxxxx	500.2	49136	16
	10111111111	500.2	49136	
	00000000001	999.3	24592	
	00000000000	1000.0	24576	
011	11xxxxxxxxx	1000.3	24568	8
	10111111111	1000.3	24568	
	00000000001	1998.7	12296	
	00000000000	2000.0	12288	

Table 9. Examples of Output Data Rate as a Function of FSAMPC[2:0] and FSAMPF[10:0] (continued)

FSAMPC[2:0]	FSAMPF[10:0]	OUTPUT DATA RATE (sps)	OUTPUT DATA PERIOD (24.576MHz CLOCK CYCLES)	FSAMPF OUTPUT DATA PERIOD RESOLUTION (24.576MHz CLOCK CYCLES)
100	11xxxxxxxxx	2000.7	12284	4
	10111111111	2000.7	12284	
	00000000001	3997.4	6148	
	00000000000	4000.0	6144	
101	11xxxxxxxxx	4001.3	6142	2
	10111111111	4001.3	6142	
	00000000001	7994.8	3074	
	00000000000	8000.0	3072	
000	11xxxxxxxxx	8002.6	3071	**1**
	10111111111	8002.6	3071	
	00000000001	15990	1537	
	00000000000	**16000**	**1536**	
110	11xxxxxxxxx	16010	1535	1
	1011111111x	16010	1535	
	0000000001x	31958	769	
	0000000000x	32000	768	
111	11xxxxxxxxx	32042	767	1
	101111111xx	32042	767	
	000000001xx	63834	385	
	000000000xx	64000	384	

Table 10. Typical Performance vs. Output Data Rate

OUTPUT DATA RATE (ksps)	-3dB BANDWIDTH (kHz)	-0.1dB BANDWIDTH (kHz)	LATENCY (µs)	FAULT RECOVERY TIME (µs)	SNR OF 24-BIT DATA (dB)	RELATIVE ACCURACY OF 256 DATA POINTS (%)	RELATIVE ACCURACY OF SINGLE CYCLE AT 60Hz (%)
0.5	0.11	0.05	11030	16375	117	0.04	0.23
1	0.21	0.11	5530	8375	115	0.05	0.20
2	0.42	0.22	2780	4375	113	0.06	0.17
4	0.85	0.43	1405	2375	111	0.08	0.16
8	1.69	0.87	718	1375	108	0.11	0.16
10	2.11	1.09	580	1175	107	0.13	0.16
12	2.54	1.31	488	1042	106	0.14	0.16
16	**3.38**	**1.74**	**374**	**875**	**105**	**0.16**	**0.16**
32	6.78	3.48	202	625	97	0.40	0.28
64	13.5	6.96	116	500	81	2.51	1.26

Multiple Device Connection

Daisy chain up to eight devices for applications that require up to 32 simultaneously sampled inputs over a single SPI-/DSP-compatible serial interface with a single chip-select signal, and single interface commands that apply to all devices in the chain. The eight devices effectively operate as one device.

There are two aspects to cascading multiple devices: the digital interface and the mechanism for keeping multiple devices sampling simultaneously.

There are many configurations for connecting multiple devices; one is described in the next section, others are described in the Synchronizing Multiple Devices section within the Applications Information section.

Multiple Device Digital Interface

Figure 13 shows the most common way to daisy chain the digital interface of multiple devices.

SPI bus arbitration is performed using CASCIN and CASCOUT. A falling edge at the CASCIN input of device n, which is driven by the CASCOUT of device n-1, allows device n to take over the SPI bus until all expected data is written or read; at this point, device n pulls its CASCOUT output low. Similarly, CASCOUT of device n drives CASCIN of device n+1. Figures 12 and 14 show read operations, including CASCIN and CASCOUT timings, for two cascaded devices and eight cascaded devices, respectively. The operation described above applies to all register operations except for writes to the Data-Rate Control register. A fixed 16-bit word is written to the Data-Rate Control registers of all devices in the chain, independent of the number of cascaded devices (see Figure 15). Reading from the Data-Rate Control register returns 16 bits per cascaded device.

Connecting the open-drain $\overline{\text{OVRFLW}}$ output of all devices together creates one signal that summarizes the overflow information of all devices. This is also true of the $\overline{\text{FAULT}}$ output. Connecting together these outputs from multiple devices has the effect of a “wire NOR.” Any device that has an active condition on these outputs is allowed to pull the line low.

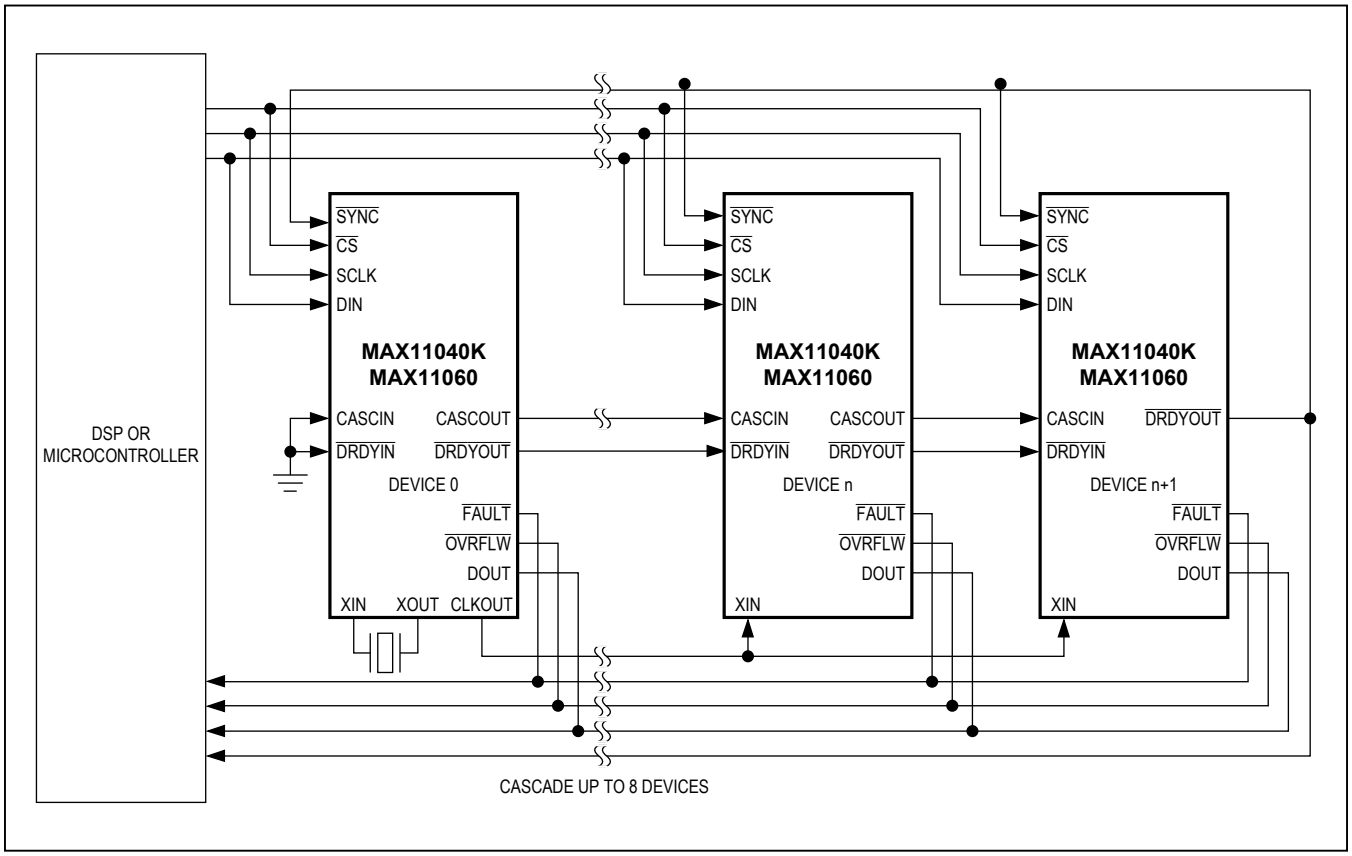


Figure 13. Daisy- Chaining Multiple Devices

To ensure that all devices have their data ready, connect $\overline{DRDYIN}$ of device 0 to ground, and connect $\overline{DRDYIN}$ of device n to the $\overline{DRDYOUT}$ of device n-1 for all devices. $\overline{DRDYOUT}$ does not go low until $\overline{DRDIN}$ is low and the conversion of the device is complete. In this configuration, $\overline{DRDYOUT}$ of the last device goes low only when all devices in the chain have their data ready.

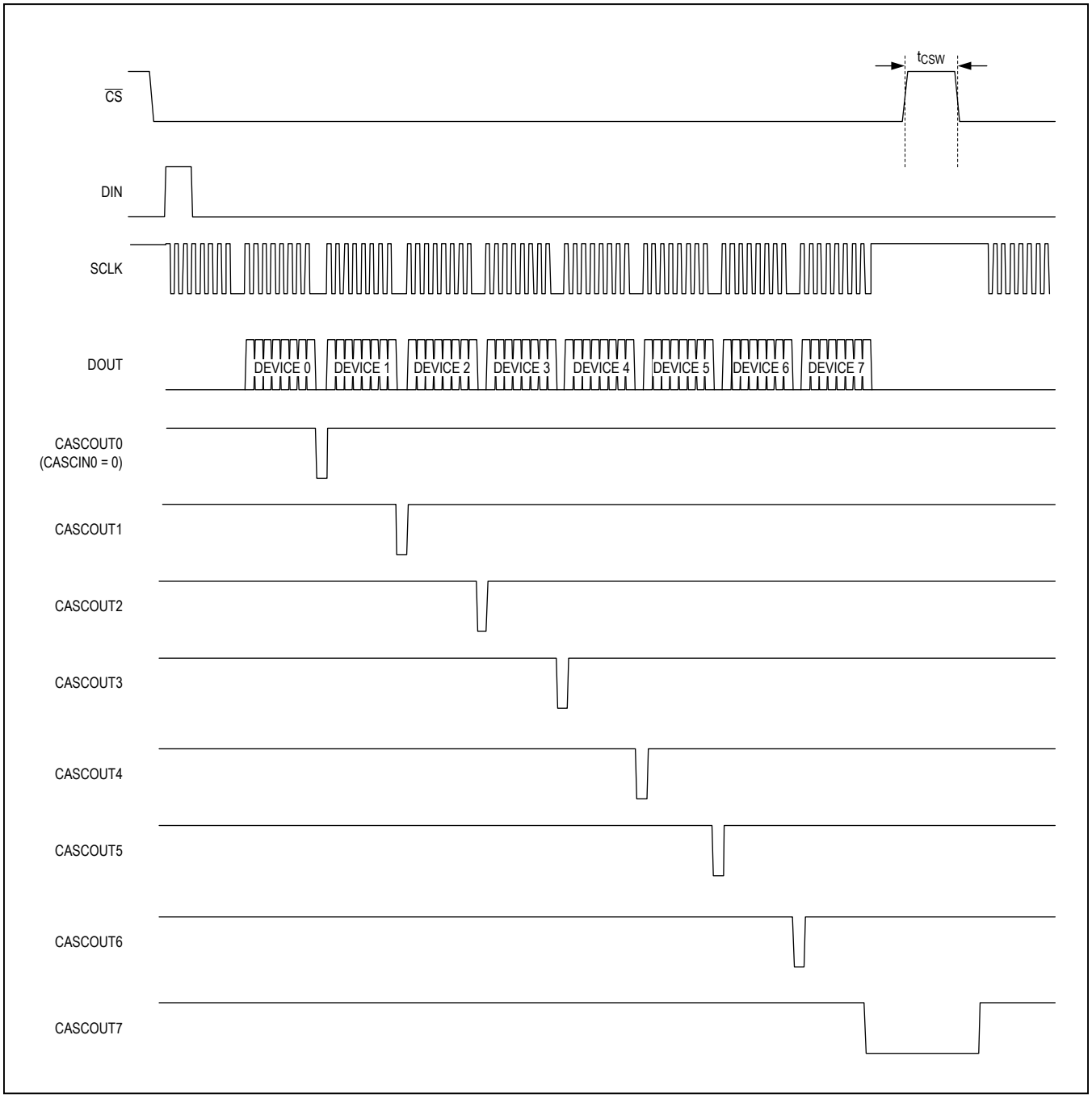


Figure 14. Configuration Register Read Operation Timing Diagram for Eight Cascaded Devices

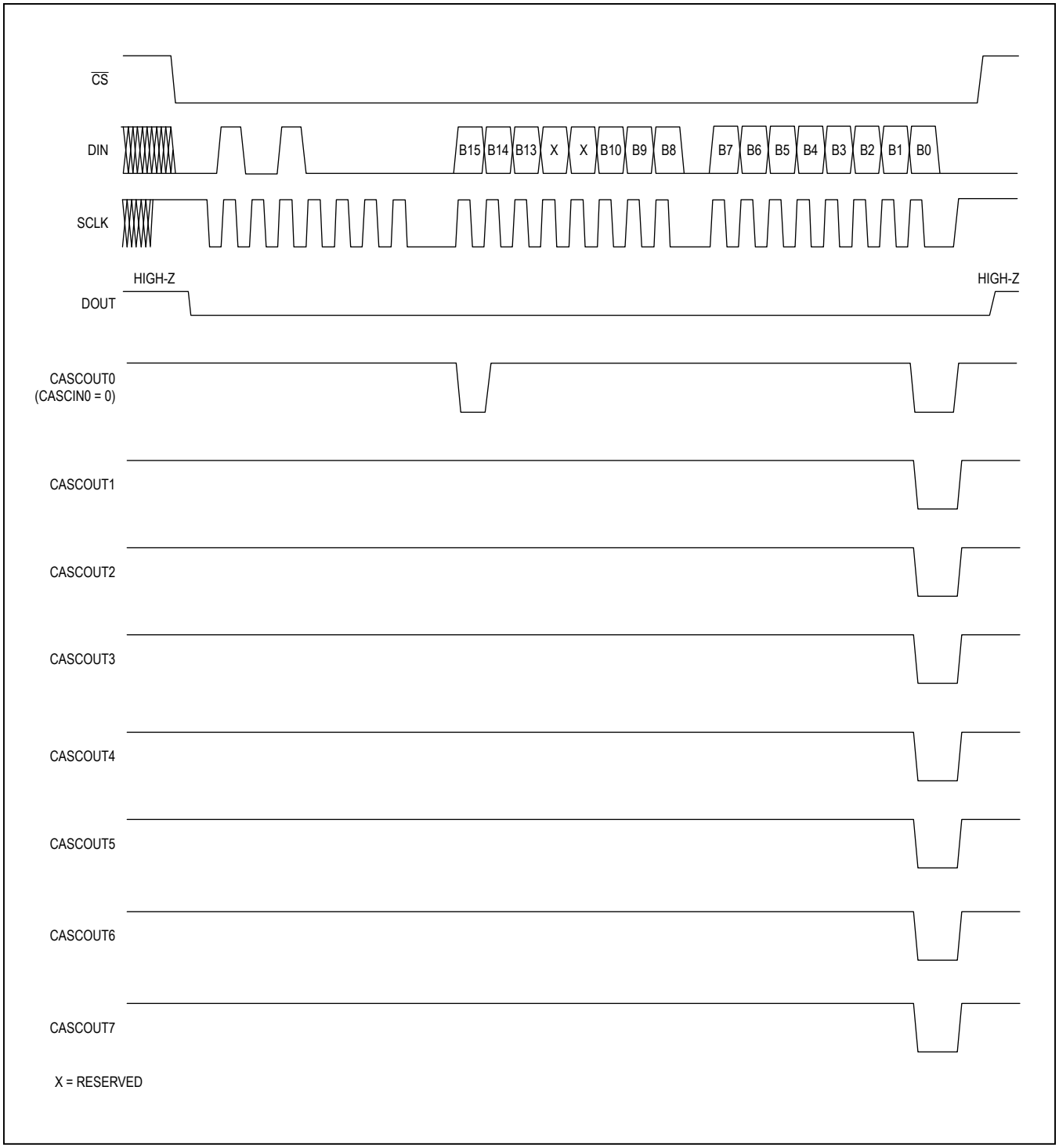


Figure 15. Data Rate Controller Register Write Operation Timing Diagram for Eight Cascaded Devices

$\overline{\text{SYNC}}$ for Simultaneous Sampling with Multiple Devices

The $\overline{\text{SYNC}}$ input permits multiple devices to sample simultaneously. The mismatch between the power-up reset of multiple devices causes the devices to begin conversion at different times. After a falling edge on the $\overline{\text{SYNC}}$ input, the device completes the current conversion and then synchronizes subsequent conversions (see Figure 16).

Upon a $\overline{\text{SYNC}}$ falling edge, the devices measure the time between the $\overline{\text{SYNC}}$ falling edge to the preceding $\overline{\text{DRDYOUT}}$ falling edge, wait until the next $\overline{\text{DRDYOUT}}$ falling edge, then pause the ADC for the measured amount of time. Figure 16 shows an example where the converter is regularly sampling the input and producing a $\overline{\text{DRDYOUT}}$ with a period t_S. The effect of a $\overline{\text{SYNC}}$ falling edge as shown in Figure 16 is described in sequence below:

1) A $\overline{\text{SYNC}}$ falling edge is issued two XIN clock cycles after the $\overline{\text{DRDYOUT}}$ event 2.
2) The converter remembers the two XIN clock cycles, and completes the current sample, issuing $\overline{\text{DRDYOUT}}$ event 3 a period of t_S after $\overline{\text{DRDYOUT}}$ event 2.
3) Then, the converter pauses for the remembered time period, two XIN clock cycles for this example.
4) Correspondingly, $\overline{\text{DRDYOUT}}$ event 4 is issued two XIN cycles later than it would have without the $\overline{\text{SYNC}}$ falling edge.
5) The process continues as normal with $\overline{\text{DRDYOUT}}$ event 5 appearing t_S after $\overline{\text{DRDYOUT}}$ event 4.

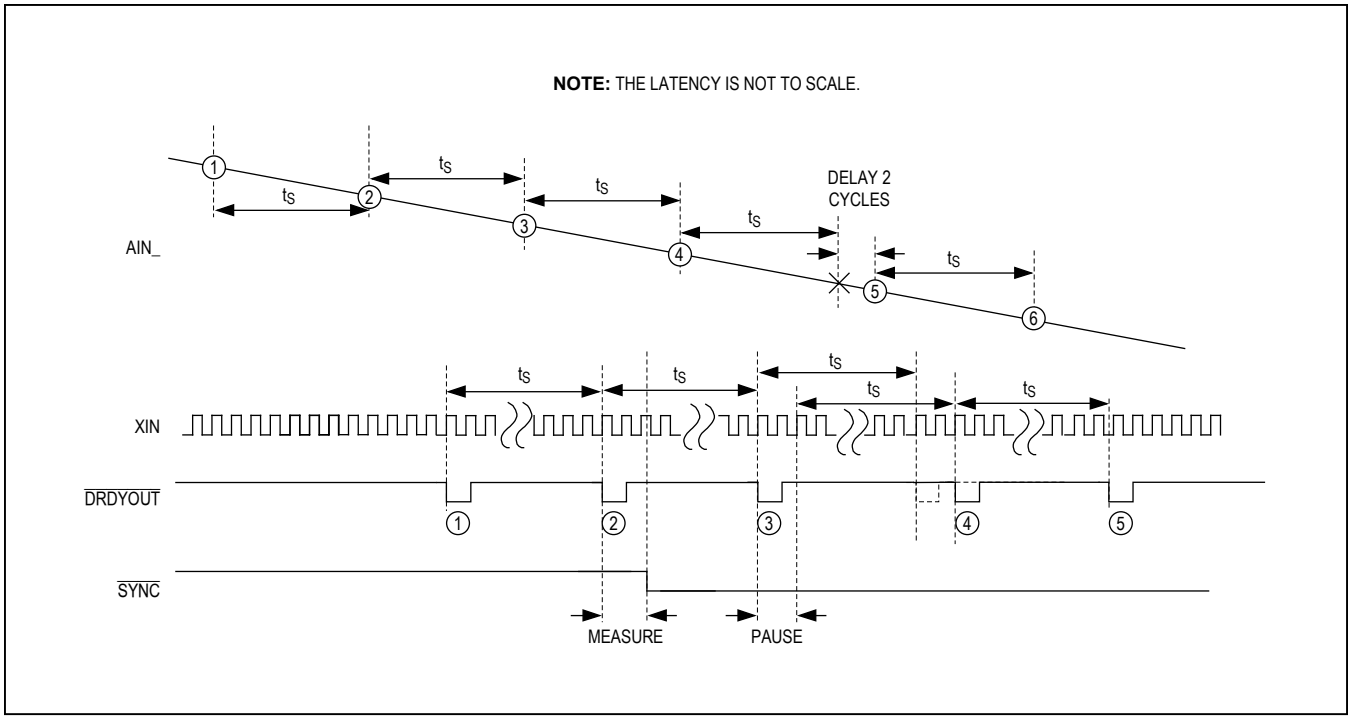


Figure 16. Effect of a $\overline{\text{SYNC}}$ Falling Edge

Referring back to the analog input, since the entire sampling section of the converter also paused for two clock cycles, the sampling point for sample 5 is also paused by two clock cycles, possibly creating a small disturbance at the $\overline{SYNC}$ falling edge. This disturbance is filtered with the digital filter, which makes it less distinct.

If the $\overline{SYNC}$ falling edge occurred during the same XIN clock period as the $\overline{DRDYOUT}$ signal, the disturbance does not affect the periodic timing since the $\overline{SYNC}$ falling edge would demand a pause of zero XIN clock cycles. Hence, connecting the $\overline{DRDYOUT}$ of the last converter to the $\overline{SYNC}$ inputs of many converters, as illustrated in Figure 13, aligns the sampling of the converters on the first $\overline{SYNC}$ falling edge, but does not disturb a regular sampling process for future samples.

See the *Multiple Device Synchronization* section for different ways to use the $\overline{SYNC}$ input.

Transfer Function

Figures 17 shows the bipolar I/O transfer function. Code transitions occur halfway between successive integer LSB values. Output coding is binary, with 1 LSB = (0.88 x V_{REFIO}) x 2/524,288 in 19-bit mode, (0.88 x V_{REFIO}) x 2/16,777,216 in 24-bit mode, and (0.88 x V_{REFIO}) x 2/65536 for the MAX11060.

Power-On Reset

The serial interface, logic, digital filter, and modulator circuits reset to zero at power-up. The power-on reset circuit releases this reset no more than 1ms after V_{DVDD} rises above 2V.

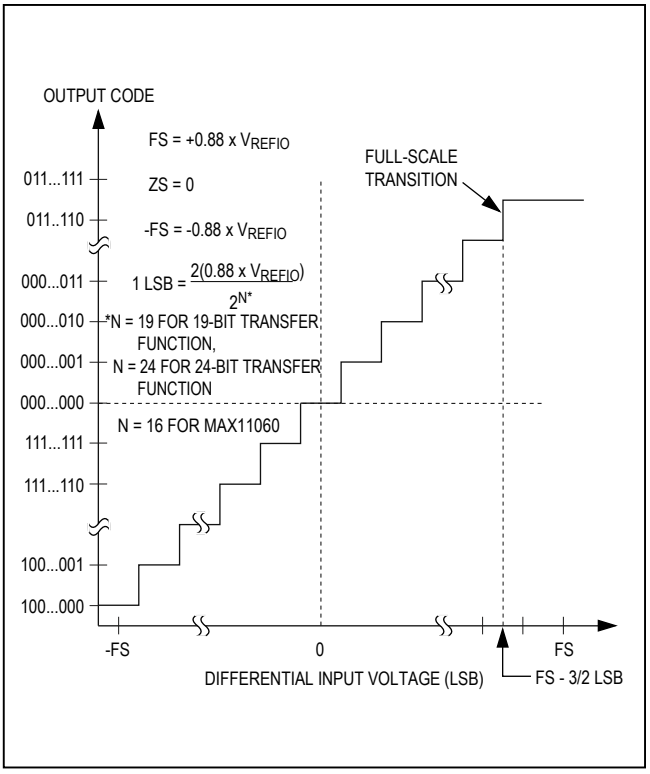


Figure 17. ADC Transfer Function

Applications Information

Multiple Device Synchronization

Synchronizing Multiple Devices Using a Shared XIN Clock Source

To synchronize multiple devices sharing a single XIN clock source, transition the $\overline{SYNC}$ input that is shared by all devices high to low. When an external sync source is not available, connect $\overline{DRDYOUT}$ of the last device to the $\overline{SYNC}$ input of all devices in the chain. The devices ignore any $\overline{SYNC}$ transitions applied during the power-on reset.

Synchronizing Multiple Devices Using Independent XIN Clock Sources

If it is undesirable to connect the XIN clock sources together, due to EMI or other reasons; use $\overline{DRDYIN}$, $\overline{DRDYOUT}$, and $\overline{SYNC}$ to align the conversion timing as shown in Figure 18. This minimizes the effects of drift between the clock sources by resynchronizing after each conversion when $\overline{DRDYOUT}$ transitions low. In this configuration, the maximum correction caused by a $\overline{SYNC}$ edge is one XIN clock cycle.

The resulting sampling rate is determined by the sampling frequency of the device with the slowest clock source, plus the delay through the $\overline{DRDYIN}$ to $\overline{DRDYOUT}$ chain between this slowest device and the end of the chain.

Synchronizing Multiple Devices to an Independent Clock Source

To periodically synchronize multiple devices to an independent timing source, connect the timing source to the $\overline{SYNC}$ inputs of the devices. If minimal jitter is important in the application, program the devices to a frequency slightly slower than the external frequency, such that $\overline{SYNC}$ falling edges only occur a short time after the $\overline{DRDYOUT}$ signals.

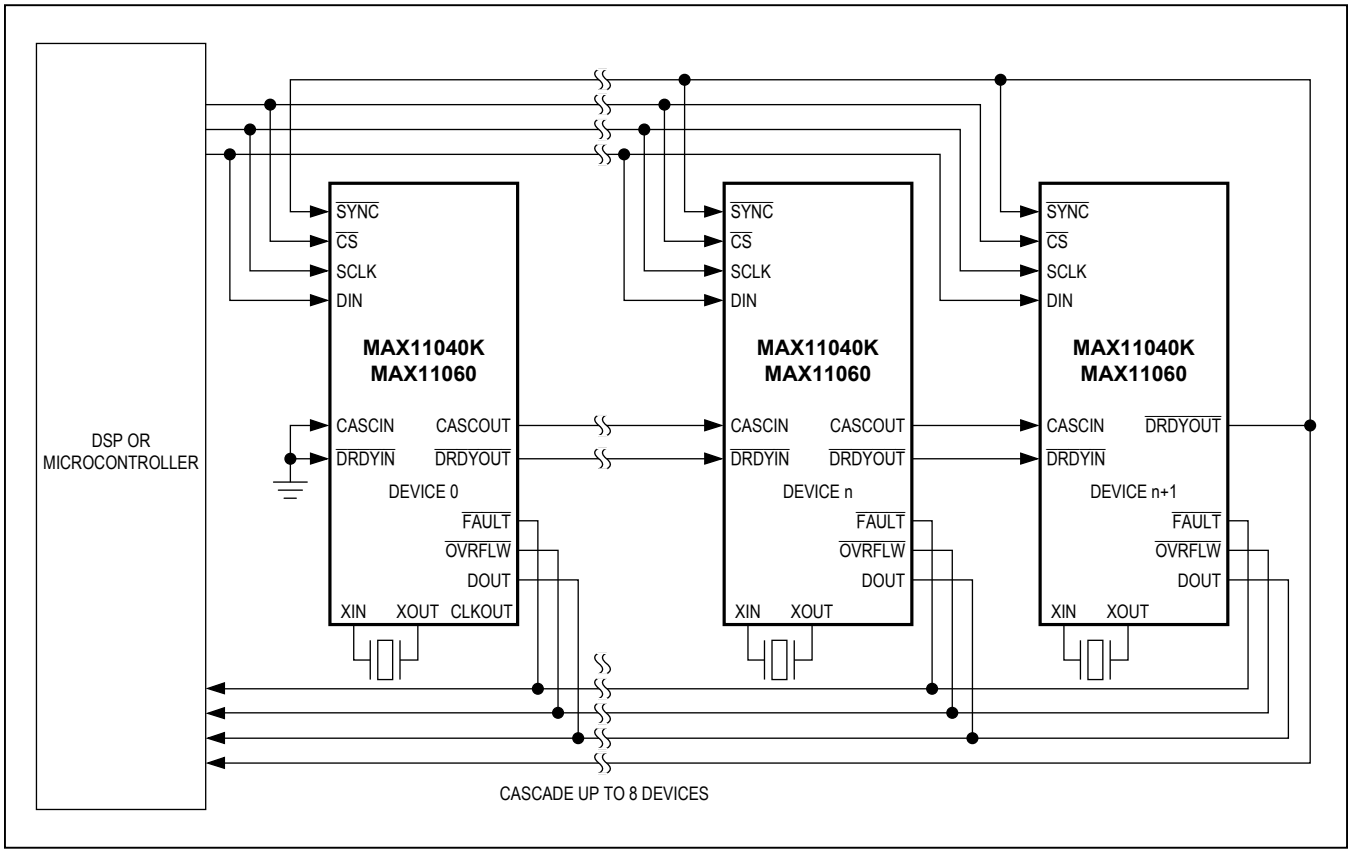


Figure 18. One Crystal per Device and All $\overline{SYNC}$ Inputs Driven by $\overline{DRDYOUT}$ of the Last Device in the Chain

Signal Distortion at $\overline{SYNC}$ Falling Edges

Each $\overline{SYNC}$ falling edge causes a disruption in the digital filter timing proportional to the delay from the previous falling edge of $\overline{DRDYOUT}$ to the falling edge of $\overline{SYNC}$. Any analysis of the output data that assumes a uniform sampling period sees an error proportional to that delay, with a maximum value determined by the maximum derivative of the analog input. Figure 19 shows the effect of this discontinuity at output sample 5.

Assuming a 60Hz ±2.2V sine wave, the maximum possible error on any given sample caused by a $\overline{SYNC}$ falling edge is:

$$V_{ERROR_MAX} = 2.2V \times 2\pi \times 60Hz \times t_{\overline{DRDYOUT}_TO_SYNC}$$
$$= 0.83\mu V/ns \times t_{\overline{DRDYOUT}_TO_SYNC}$$

The delay from $\overline{DRDYOUT}$ to $\overline{SYNC}$ is quantized to within one cycle of the 24.576MHz clock. $\overline{SYNC}$ pulses that are asynchronous to $\overline{DRDYOUT}$ may cause large errors. To eliminate this error, use a single clock source for all devices and avoid disrupting the output data timing with $\overline{SYNC}$ pulses while making high-precision measurements. Alternately, minimize the delay from $\overline{DRDYOUT}$ to $\overline{SYNC}$ to minimize the error.

Example:

Assume $f_{AIN_}$ = 60Hz, f_S = 16ksps, and eight total devices in the chain.

Device 1 has the longest $t_{\overline{DRDYOUT}_TO_\overline{SYNC}}$ delay, therefore the worst-case $\overline{SYNC}$ error.

If device 1 has the fastest XIN clock in the chain, and device 2 has the slowest XIN clock in the chain, and they differ by 0.1%, device 1 completes its conversion as much as 0.1% earlier than device 2. Hence, the delay of device 2 is:

$$0.1\% \times (1/16kHz) = 62.5ns$$

The signal then propagates down the chain at a time delay of nominally 20ns for each device.

The total delay back to the $\overline{SYNC}$ falling edge after going through six additional delays is:

$$t_{DELAY} = 62.5ns + 6 \times 20ns = 182.5ns$$

$$\text{Maximum \% Error} = 2\pi \times f_{IN} \times t_{\overline{DRDYOUT}_TO_\overline{SYNC}} \times 100\% = 2 \times \pi \times 60Hz \times 182.5ns \times 100\% = 0.007\%$$

The above error is relative to the signal level, not to the full scale of the data converter.

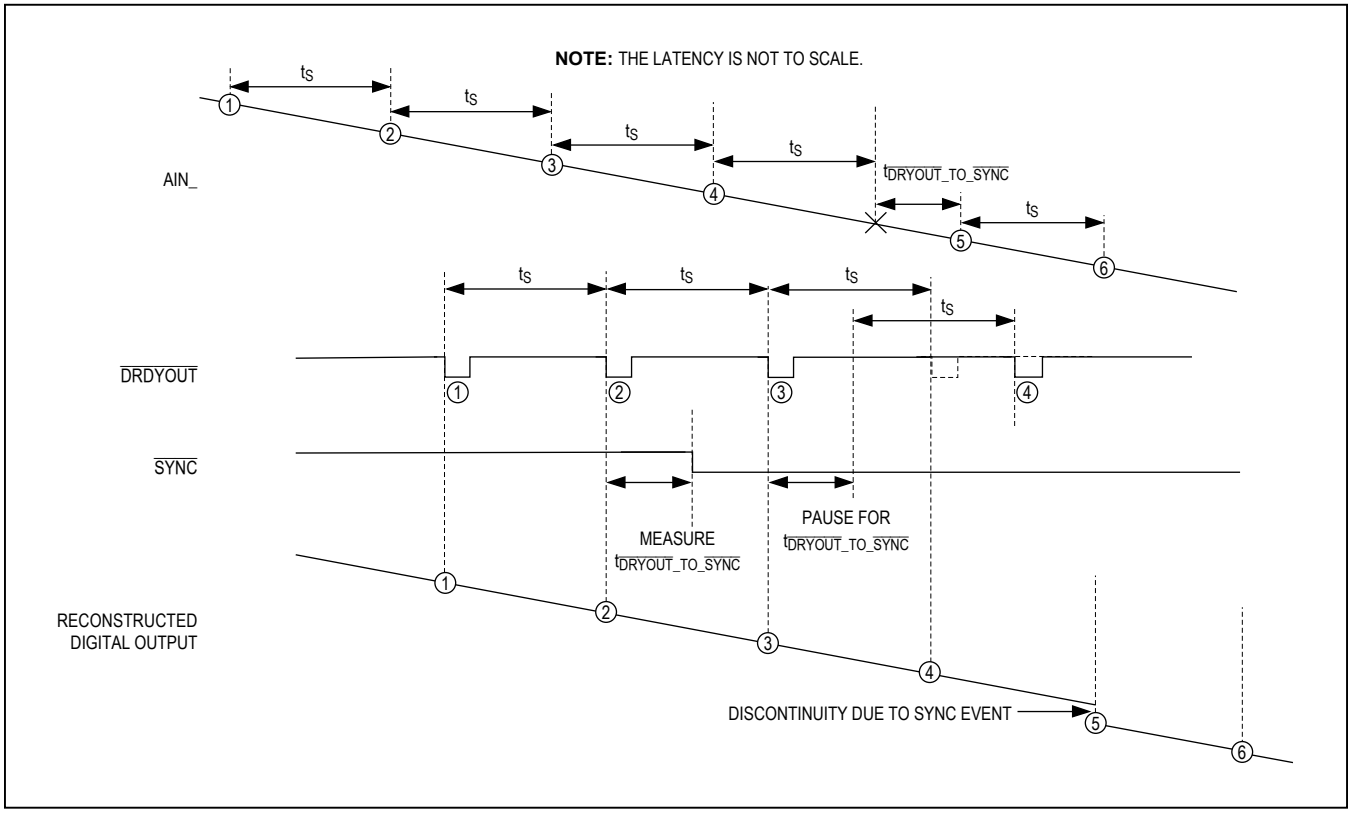


Figure 19. Example of Discontinuity in Reconstructed Digital Output Due to $\overline{SYNC}$ Falling Edge with a Large $\overline{DRDYOUT}$-to-$\overline{SYNC}$ Delay

Source Impedance and Input Sampling Network

The source impedance that drives the analog inputs affects the sampling period.

Low-Impedance Sources

Minimize the source impedance to ensure the input capacitor fully charges during the sampling phase. The required source resistance is defined by the equation below:

$$R_{SOURCE_MAX} < \frac{t_{SAMP}}{K \times C_{SAMP} \times \ln\left(\frac{1}{Error}\right)} - R_{INT}$$

$$= \frac{120ns}{1.5 \times 4pF \times \ln\left(\frac{1}{Error}\right)} - 2600\Omega$$

where K = 1.5 and R_{INT} = 2600Ω.

For example, the required source resistance to achieve 0.1% accuracy is:

$$R_{SOURCE_MAX} < \frac{120ns}{1.5 \times 4pF \times \ln\left(\frac{1}{0.1\%}\right)} - 2600\Omega$$

$$= \frac{120ns}{1.5 \times 4pF \times \ln(1000)} - 2600\Omega$$

$$= \frac{120ns}{1.5 \times 4pF \times 6.91} - 2600\Omega = 294\Omega$$

High-Impedance Sources

If the source impedance is greater than R_{SOURCE_MAX}, as defined in the *Low-Impedance Sources* section, place a 0.1µF bypass capacitor between AIN_+ and AIN_- to provide transient charge. The average switched-capacitor load with a proper bypass capacitor and XIN clock frequency = 24.576MHz is equivalent to a 130kΩ resistor connected between AIN_+ and AIN_-. This resistance is independent of the value of the 0.1µF bypass capacitor. If another XIN clock frequency is chosen, this resistance is directly proportional to the XIN clock period.

Although the addition of a bypass capacitor helps charge the devices' 0 input capacitor, some gain error due to resistive drop across the source resistance still remains. Calculate this gain error using the following equation:

$$\Delta Gain = \frac{R_{SOURCE}}{R_{SOURCE} + R_{LOAD}} = \frac{R_{SOURCE}}{R_{SOURCE} + 130k\Omega}$$

Analog Filtering

The analog filtering requirements in front of the devices are considerably reduced compared to a conventional converter with no on-chip filtering. The internal digital filter has significant rejection of signals higher than the Nyquist frequency of the output data rate that would alias back into the sampled signal.

The internal digital filter does not provide rejection close to the harmonics of the 3.072MHz modulator frequency. For example, assuming an output data rate of 16ksps if the XIN clock is set to 24.576MHz, then the band between 3.0686MHz and 3.0750MHz is not explicitly filtered. Since this unfiltered band is very small compared to its actual frequency, very little broadband noise enters through this mechanism. If focused narrowband noise in this band is present, a simple analog filter can create significant attenuation at this frequency because the ratio of passband-to-stopband frequency is large.

In addition, because the device's common-mode rejection extends out to several 100kHz, the common-mode noise susceptibility in this frequency range is substantially reduced.

Providing additional filtering in some applications ensures that differential noise signals outside the frequency band of interest do not saturate the analog modulator.

The modulator saturates if the input voltage exceeds its full scale (±2.2V). The digital filter does not prevent a large signal in the filter stopband from saturating the modulator. If signals outside the band of interest cause violation of this full scale while accurate conversion of passband signals is desired, then additional analog filtering is required to prevent saturation.

Compensating for the Rolloff of the Digital Filter in Typical FFT Analysis

To calculate FIR_GAIN($f_{AIN_}$):

1) Decide the number of evenly spaced frequencies between DC and the Nyquist frequency of the output data rate at which correction factors are desired, which is usually the same as the FFT result.
2) Create an array with a length that is 2x the number of the desired frequencies. (Again, the result is likely to correlate with the time domain array that is loaded into an FFT algorithm.)
3) Fill this array with the filter coefficients provided in the *Digital Filter* section. Fill the rest of the array with zeros.
4) Take an FFT of this array. The result represents the response of the devices' built-in FIR filter.

To compensate the result of an FFT for the devices' output data:

1) Calculate the inverse (1/x) of the equation provided in the *Digital Filter* section for each frequency in the FFT.
2) Multiply the FFT of the devices' output data by the result of the above step.

Power Supplies

AVDD and DVDD provide power to the devices. The AVDD powers up the analog section, while the DVDD powers up the digital section. The power supply for AVDD and DVDD ranges from +3.0V to +3.6V and 2.7V to V_{AVDD}, respectively. Bypass AVDD to AGND with a 1µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor and bypass DVDD to DGND with a 1µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor. For improved performance, place the bypass capacitors as close as possible to the device.

Layout, Grounding, and Bypassing

The best layout and grounding design always comes from a thorough analysis of the complete system. This includes the signal source's dependence and sensitivity on ground currents, and knowledge of the various currents that could travel through the various potential grounding paths.

Use PCBs with separate analog and digital ground planes. Connect the two ground planes together only at the devices' GND input. Isolate the digital supply from the analog with a low-value resistor (10Ω) or ferrite bead when the analog and digital supplies come from the same source.

Ensure that digital return currents do not pass through the analog ground and that return-current paths are low impedance. A 5mA current flowing through a PCB ground trace impedance of only 0.05Ω creates an error voltage of approximately 250µV.

Ensure that digital and analog signal lines are kept separate. Do not run digital (especially the SCLK and DOUT) lines parallel to any analog lines or under the devices. Lay out the traces in perpendicular directions when a digital line and an analog line cross each other.

Bypass AVDD to the analog ground plane with a 0.1µF capacitor in parallel with a 1µF to 10µF low-ESR capacitor. Keep capacitor leads short for best supply-noise rejection. Bypass REF+ and REF- with a 0.1µF capacitor to GND. Place all bypass capacitors as close as possible to the device for optimum decoupling.

Crystal Layout

Follow these basic layout guidelines when placing a crystal on a PCB with the devices to avoid coupled noise:

1) Place the crystal as close as possible to XIN and XOUT. Keeping the trace lengths between the crystal and inputs as short as possible reduces the probability of noise coupling by reducing the length of the "antennae." Keep the XIN and XOUT lines close to each other to minimize the loop area of the clock lines. Keeping the trace lengths short also decreases the amount of stray capacitance.
2) Keep the crystal solder pads and trace width to XIN and XOUT as small as possible. The larger these bond pads and traces are, the more likely it is that noise will couple from adjacent signals.
3) Place a guard ring (connect to ground) around the crystal to isolate the crystal from noise coupled from adjacent signals.
4) Ensure that no signals on other PCB layers run directly below the crystal or below the traces to XIN and XOUT. The more the crystal is isolated from other signals on the board, the less likely for noise to couple into the crystal.
5) Place a local ground plane on the PCB layer immediately below the crystal guard ring. This helps to isolate the crystal from noise coupling from signals on other PCB layers.

   Note: Keep the ground plane in the vicinity of the crystal only and not on the entire board.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
38 TSSOP	U38+3	21-0081	90-0140

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/11	Initial release of the MAX11040K	—
1	4/11	Initial release of the MAX11060	1
2	11/11	Updated *Absolute Maximum Ratings*	2
3	8/12	Updated the *Multiple Device Digital Interface* and the *Synchronizing Multiple Devices Using a Shared XIN Clock Source* sections and Figure 13	25, 26 29, 30
4	5/15	Revised the *Benefits and Features*, *Electrical Characteristics*, *Data Rate Control Register* section, and Table 10	1, 3, 5, 22, 24

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