MAS9081

- **Dual Band Receiver IC**
- **High Sensitivity**
- **Very Low Power Consumption**
- **Wide Supply Voltage Range**
- **Power Down Control**
- **Control for AGC On**
- **High Selectivity by Crystal Filter**
- **Fast Startup Feature**

DESCRIPTION

The MAS9081 AM-Receiver chip is a highly sensitive, simple to use AM receiver specially intended to receive time signals in the frequency range from 40 kHz to 100 kHz. Only a few external components are required for time signal receiving. The circuit has preamplifier, wide range automatic gain control, demodulator and output comparator built in. The output signal can be processed directly by an additional digital circuitry to extract the data from the received signal. The control for AGC (automatic gain control) can be used to switch AGC on or off if necessary. MAS9081 supports dual band operation by switching between two crystal filters and an additional antenna tuning capacitor.

MAS9081 has differential input and different internal compensation capacitor options for compensating shunt capacitances of different crystals (See ordering information on page 12).

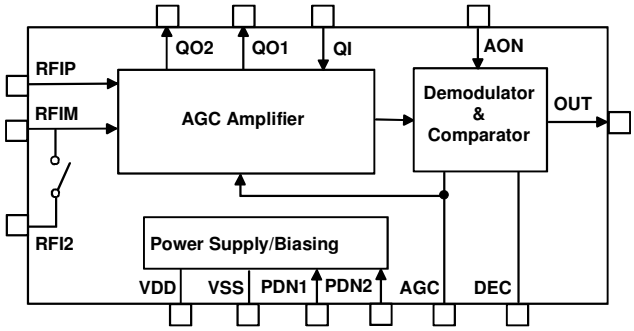
FEATURES

- Dual Band Receiver IC
- Highly Sensitive AM Receiver, 0.4 μV_{RMS} typ.
- Wide Supply Voltage Range from 1.1 V to 5 V
- Very Low Power Consumption
- Power Down Control
- Fast Startup
- Only a Few External Components Necessary
- Control for AGC On
- Wide Frequency Range from 40 kHz to 100 kHz
- High Selectivity by Quartz Crystal Filter

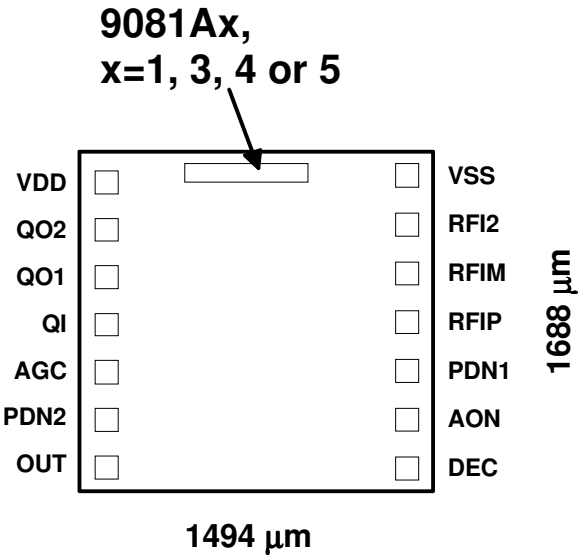
APPLICATIONS

- Dual Band Time Signal Receiver WWVB (USA), JJY (Japan), DCF77 (Germany), MSF (UK), HGB (Switzerland) and BPC (China)

BLOCK DIAGRAM



MAS9081 PAD LAYOUT



DIE size = 1.49 x 1.69 mm; PAD size = 80 x 80 µm

Note: Because the substrate of the die is internally connected to VDD, the die has to be connected to VDD or left floating. Please make sure that VDD is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.

Note: Coordinates are pad center points where origin has been located in bottom-left corner of the silicon die.

Pad Identification	Name	X-coordinate	Y-coordinate	Note
Power Supply Voltage	VDD	174 µm	1452 µm	
Quartz Filter Output for Crystal 2	QO2	174 µm	1247 µm	
Quartz Filter Output for Crystal 1	QO1	174 µm	1043 µm	
Quartz Filter Input for Crystals	QI	174 µm	839 µm	
AGC Capacitor	AGC	174 µm	633 µm	
Power Down/Frequency Selection Input 2	PDN2	174 µm	430 µm	3
Receiver Output	OUT	175 µm	224 µm	1
Demodulator Capacitor	DEC	1318 µm	240 µm	
AGC On Control	AON	1318 µm	444 µm	2
Power Down/Frequency Selection Input 1	PDN1	1318 µm	648 µm	3
Positive Receiver Input	RFIP	1318 µm	853 µm	4
Negative Receiver Input	RFIM	1318 µm	1057 µm	4
Receiver Input 2 (for Antenna Capacitor 2)	RFI2	1318 µm	1262 µm	
Power Supply Ground	VSS	1318 µm	1466 µm	

Notes:
1) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5$ µA
   - at power down the output is pulled to VSS (pull down switch)
2) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up with current < 1 µA which is switched off at power down
3) PDN1 = VDD and PDN2 = VDD means receiver off
   - Fast start-up is triggered when the receiver is after power down controlled to power up
4) Receiver inputs RFIP and RFIM have both 600 kΩ biasing resistances against ground

FREQUENCY SELECTION

The frequency selection and power down control is accomplished via two digital control pins PDN1 and PDN2. The control logic is presented in table 1.

Table 1 Frequency selection and power down control

PDN1	PDN2	RFI2 Switch	Selected Crystal Output	Description
High	High	Open	-	Power down
High	Low	Open	QO1	Frequency 1
Low	High	Closed	QO2	Frequency 2, RFI2 capacitor connected in parallel with antenna
Low	Low	Closed	QO2	Frequency 2, RFI2 capacitor connected in parallel with antenna

The internal antenna tuning capacitor switch (RFI2) and crystal filter output switches (QO1, QO2) are controlled according table 1. See switch in block diagram on page 1.

If frequency 1 is selected the RFI2 switch is open and only crystal output QO1 is active. Antenna frequency is determined by antenna inductor L_{ANT} (see Typical Application on page 5), antenna capacitor C_{ANT1} and parasitic capacitances related to antenna inputs RFI1, RFI2 and RFI3 (see Antenna Tuning Considerations below). Frequency 1 is the higher frequency of two selected frequencies.

If frequency 2 is selected then RFI2 switch is closed to connect C_{ANT2} in parallel with ferrite antenna and tune it to frequency 2. Then only crystal output QO2 is active. Frequency 2 is lower frequency of the two selected frequencies.

It is recommended to switch the device to power down for 50ms before switching to another frequency. This guarantees fast startup in switching to another frequency. The 50ms power down period is used to discharge AGC capacitor and to initialize fast startup conditions.

ANTENNA TUNING CONSIDERATIONS

The ferrite bar antenna having inductance L_{ANT} and parasitic coil capacitance C_{COIL} is tuned to two reception frequencies f_1 and f_2 by parallel capacitors C_{ANT1} and C_{ANT2}. The receiver input stage and internal antenna capacitor switch have capacitances (C_{RFI1}, C_{OFF2}) which affect the resonance frequencies. C_{OFF2} is switch capacitance when switch is open. When the switch is closed this capacitance is shorted by on resistance of the switch and is effectively eliminated. Following relationships can be written into two tuning frequencies.

Frequency f_1 (higher frequency):

$C_{TOT1}=C_{COIL}+C_{ANT1}+C_{RFI1}+C_{OFF2}=C_{COIL}+C_{ANT1}+6.5pF+37pF=C_{COIL}+C_{ANT1}+43.5pF$, $f_1 = \frac{1}{2\pi\sqrt{L_{ANT} \cdot C_{TOT1}}}$

Frequency f_2 (lower frequency):

$C_{TOT2}=C_{COIL}+C_{ANT1}+C_{ANT2}+C_{RFI1}=C_{COIL}+C_{ANT1}+C_{ANT2}+6.5pF$, $f_2 = \frac{1}{2\pi\sqrt{L_{ANT} \cdot C_{TOT2}}}$

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}-V_{SS}		-0.3	6	V
Input Voltage	V_{IN}		V_{SS}-0.3	V_{DD}+0.3	V
Power Dissipation	P_{MAX}			100	mW
Operating Temperature	T_{OP}		-40	+85	°C
Storage Temperature	T_{ST}		-55	+150	°C

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 1.4V, Temperature = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		1.10		5	V
Current Consumption	I_{DD}	VDD=1.4 V, Vin=0 µVrms VDD=1.4 V, Vin=20 mVrms VDD=3.6 V, Vin=0 µVrms VDD=3.6 V, Vin=20 mVrms	 31 27	64 37 67 40	 91 65	µA
Stand-By Current	I_{DDoff}				0.1	µA
Input Frequency Range	f_{IN}		40		100	kHz
Minimum Input Voltage	$V_{IN\ min}$			0.4	1	µVrms
Maximum Input Voltage	$V_{IN\ max}$		20			mVrms
Receiver Input Resistance Receiver Input Capacitance	R_{RFI} C_{RFI}	f=40kHz..77.5 kHz		270 6.5		kΩ pF
RFI2 Switch On Resistance RFI2 Switch Off Resistance RFI2 Switch Off Capacitance	R_{ON2} R_{OFF2} C_{OFF2}	VDD=1.4 V	10	3.8 37		Ω MΩ pF
Input Levels $\|I_{IN}\|$<0.5 µA	V_{IL} V_{IH}		 0.8 V_{DD}		0.2 V_{DD}	V
Output Current V_{OL}<0.2 V_{DD};V_{OH} >0.8 V_{DD}	$\|I_{OUT}\|$		5			µA
Output Pulse	T_{100ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	50		140	ms
	T_{200ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	150		230	ms
	T_{500ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	400	500	600	ms
	T_{800ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	700	800	900	ms
Startup Time	T_{Start}	Fast Start-up, Vin=0.4 µVrms Fast Start-up, Vin=20 mVrms		1.3 3.5		s
Output Delay Time	T_{Delay}			50	100	ms

TYPICAL APPLICATION

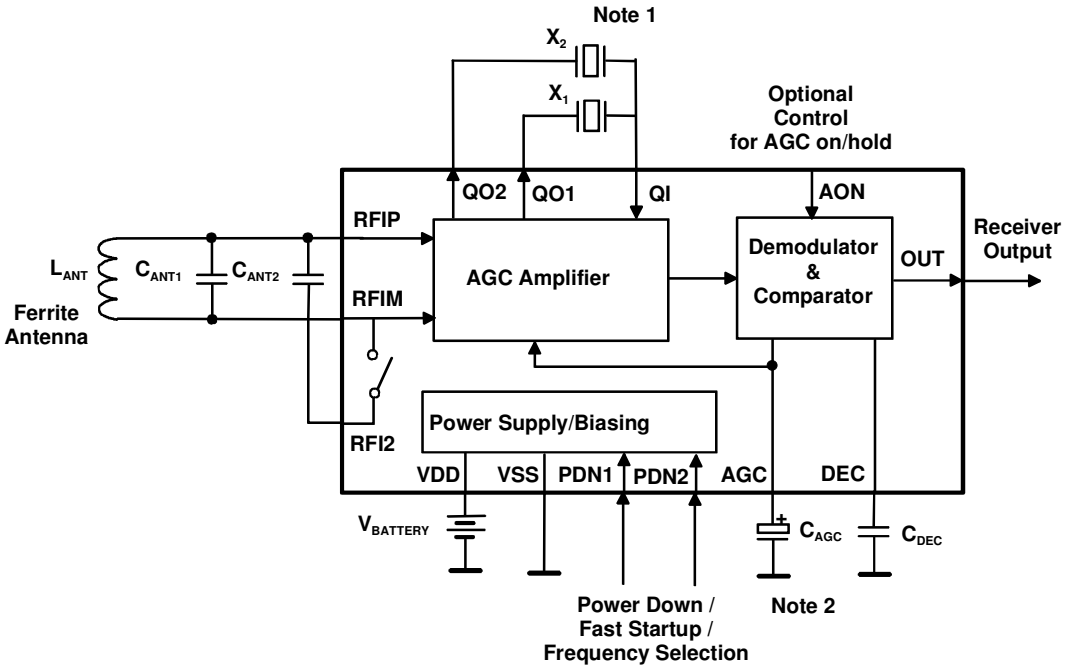


Figure 1 Application circuit of dual band receiver MAS9081

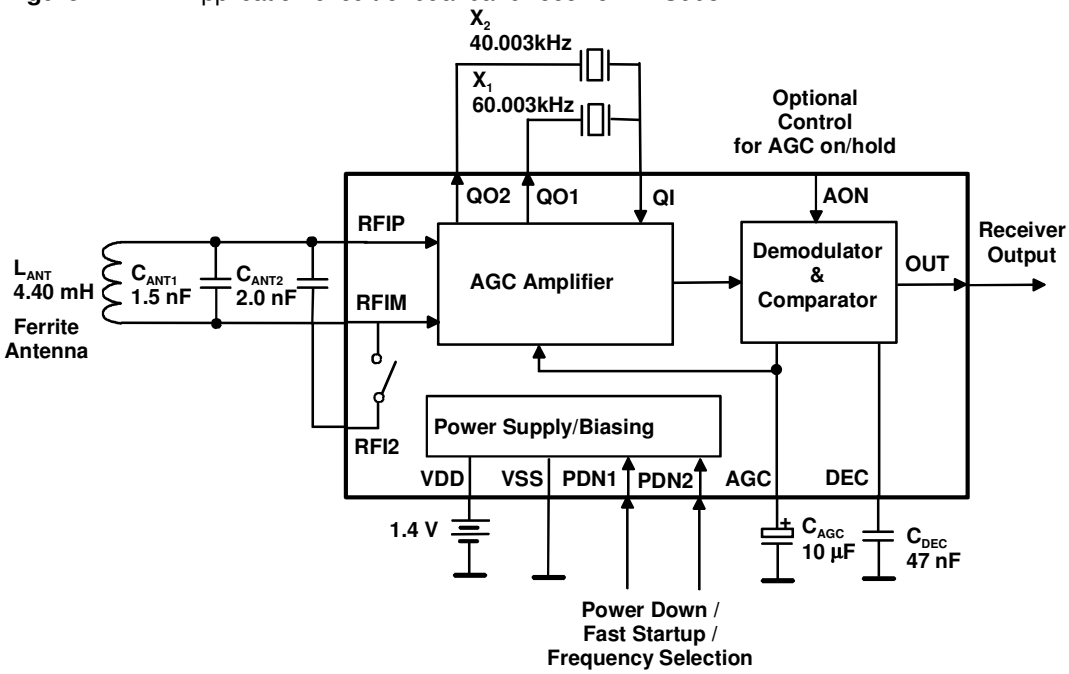


Figure 2 Example circuit of dual band receiver MAS9081 for MSF/WWVB/JJY frequencies

TYPICAL APPLICATION (Continued)

Note 1: Crystals
The crystals as well as ferrite antenna frequencies are chosen according to the time-signal system (Table 2). The crystal shunt capacitance C_0 should be matched as well as possible with the internal shunt capacitance compensation capacitor C_C of MAS9081. See Compensation Capacitance Options on table 3.

Table 2 Time-Signal System Frequencies

Time-Signal System	Location	Antenna Frequency	Recommended Crystal Frequency
DCF77	Germany	77.5 kHz	77.503 kHz
HGB	Switzerland	75 kHz	75.003 kHz
MSF	United Kingdom	60 kHz	60.003 kHz
WWVB	USA	60 kHz	60.003 kHz
JJY	Japan	40 kHz and 60 kHz	40.003 kHz and 60.003 kHz
BPC	China	68.5 kHz	68.505 kHz

Table 3 Compensation Capacitance Options

Device	C_C	Crystal Description
MAS9081A1	0.75 pF	For low C_0 crystal
MAS9081A3	1.25 pF	For high C_0 crystal
MAS9081A4	1.5 pF	For high C_0 crystal
MAS9081A5	3.875 pF	For any crystal (over compensated, requires external capacitors)

It should be noted that grounded crystal package has reduced shunt capacitance. This value is about 85% of floating crystal shunt capacitance. For example crystal with 1pF floating package shunt capacitance can have 0.85pF grounded package shunt capacitance. PCB traces of crystal and external compensation capacitance should be kept at minimum to minimize additional parasitic capacitance which can cause capacitance mismatching.

Highest frequency crystal is connected to crystal output pin 1 (QO1). Lowest frequency crystal is connected to crystal output pin 2 (QO2). The other pin of both crystals is connected to common crystal input pin QI.

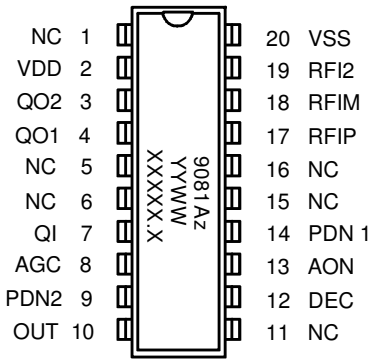
Table 4 below presents some crystal manufacturers having suitable crystals for timesignal receiver application.

Table 4. Crystal Manufacturers and Crystal Types in Alphaphetical Order for Timesignal Receiver Application

Manufacturer	Crystal Type	Dimensions	Web Link
Citizen	CFV-206	ø 2.0 x 6.0	http://www.citizen.co.jp/tokuhan/quartz/
Epson	C-2-Type C-4-Type	ø 1.5 x 5.0 ø 2.0 x 6.0	http://www.epsondevice.com/e/
KDS Daishinku	DT-261	ø 2.0 x 6.0	http://www.kdsj.co.jp/english.html
Microcrystal	MX1V-L2N MX1V-T1K	ø 2.0 x 6.0 ø 2.0 x 8.1	http://www.microcrystal.com/
Seiko Instruments	VTC-120	ø 1.2 x 4.7	http://speed.sii.co.jp/pub/compo/quartz/topE.jsp

Note 2: AGC Capacitor
The AGC and DEC capacitors must have low leakage currents due to very small signal currents through the capacitors. The insulation resistance of these capacitors should be at minimum 100 MΩ. Also probes with at least several 100 MΩ impedance should be used for voltage probing of AGC and DEC pins. DEC capacitor can be low leakage chip capacitor.

MAS9081 SAMPLES IN SBDIL 20 PACKAGE



Top Marking Definitions:
YYWW = Year Week
XXXXX.X = Lot Number
z = Sample Version Number

PIN DESCRIPTION

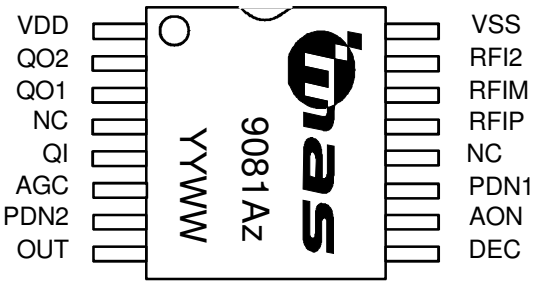
Pin Name	Pin	Type	Function	Note
NC	1			
VDD	2	P	Positive Power Supply	
QO2	3	AO	Quartz Filter Output for Crystal 2	
QO1	4	AO	Quartz Filter Output for Crystal 1	
NC	5			1
NC	6			1
QI	7	AI	Quartz Filter Input for Crystals	
AGC	8	AO	AGC Capacitor	
PDN2	9	DI	Power Down/Frequency Selection Input 2	
OUT	10	DO	Receiver Output	2
NC	11			
DEC	12	AO	Demodulator Capacitor	
AON	13	DI	AGC On Control	3
PDN1	14	DI	Power Down/Frequency Selection Input 1	
NC	15			
NC	16			
RFIP	17	AI	Positive Receiver Input	4
RFIM	18	AI	Negative Receiver Input	4
RFI2	19	AI	Receiver Input 2 (for Antenna Capacitor 2)	
VSS	20	G	Power Supply Ground	

A = Analog, D = Digital, P = Power, G = Ground, I = Input, O = Output, NC = Not Connected

Notes:

1) Pins 5 and 6 between QO and QI must be connected to VSS to eliminate DIL package leadframe parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
2) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5\ \mu A$
   - at power down the output is pulled to VSS (pull down switch)
3) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up with current < 1 µA which is switched off at power down
4) Receiver inputs RFIP and RFIM have both 600 kΩ biasing MOSFET-transistors towards ground

PIN CONFIGURATION & TOP MARKING FOR PLASTIC TSSOP-16 PACKAGE



Top Marking Definitions:
z = Version Number
YYWW = Year Week

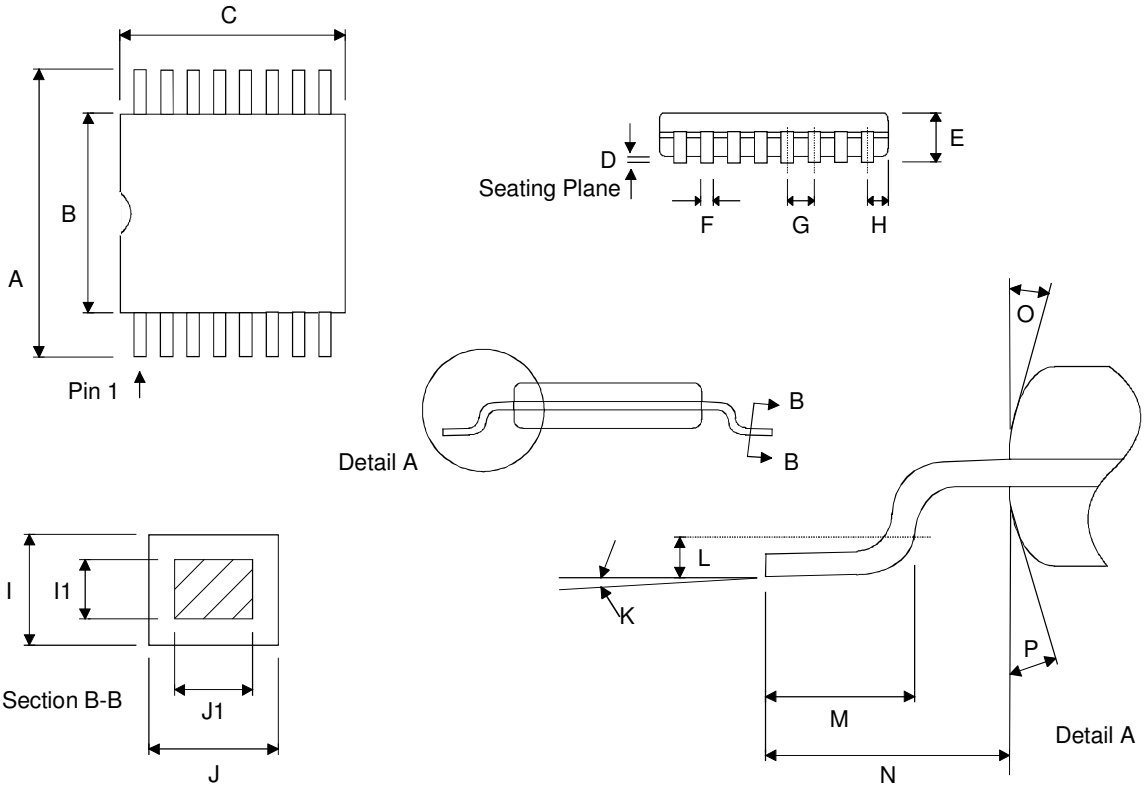
PIN DESCRIPTION

Pin Name	Pin	Type	Function	Note
VDD	1	P	Positive Power Supply	
QO2	2	AO	Quartz Filter Output for Crystal 2	
QO1	3	AO	Quartz Filter Output for Crystal 1	
NC	4			1
QI	5	AI	Quartz Filter Input for Crystal and External Compensation Capacitor	
AGC	6	AO	AGC Capacitor	
PDN2	7	DI	Power Down/Frequency Selection Input 2	
OUT	8	DO	Receiver Output	2
DEC	9	AO	Demodulator Capacitor	
AON	10	DI	AGC On Control	3
PDN1	11	DI	Power Down/Frequency Selection Input 1	
NC	12			
RFIP	13	AI	Positive Receiver Input	4
RFIM	14	AI	Negative Receiver Input	4
RFI2	15	AI	Receiver Input 2 (for Antenna Capacitor 2)	
VSS	16	G	Power Supply Ground	

A = Analog, D = Digital, P = Power, G = Ground, I = Input, O = Output, NC = Not Connected

Notes:
1) Pin 4 between quartz crystal filter pins must be connected to VSS to eliminate package leadframe parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
2) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5\ \mu A$
   - at power down the output is pulled to VSS (pull down switch)
3) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up (to AGC on) with current < 1 µA which is switched off at power down
4) Differential input versions A1..A5 have 600 kΩ biasing MOSFET-transistors towards ground from both receiver inputs RFIP and RFIM. Asymmetric input versions AB..AF have input pin RFIM unconnected.

PACKAGE (TSSOP-16) OUTLINES



Dimension	Min	Max	Unit
A	6.40 BSC		mm
B	4.30	4.50	mm
C	5.00 BSC		mm
D	0.05	0.15	mm
E		1.10	mm
F	0.19	0.30	mm
G	0.65 BSC		mm
H	0.18	0.28	mm
I	0.09	0.20	mm
I1	0.09	0.16	mm
J	0.19	0.30	mm
J1	0.19	0.25	mm
K	0°	8°	
L	0.24	0.26	mm
M (The length of a terminal for soldering to a substrate)	0.50	0.75	mm
N	1.00 REF		mm
O	12°		
P	12°		

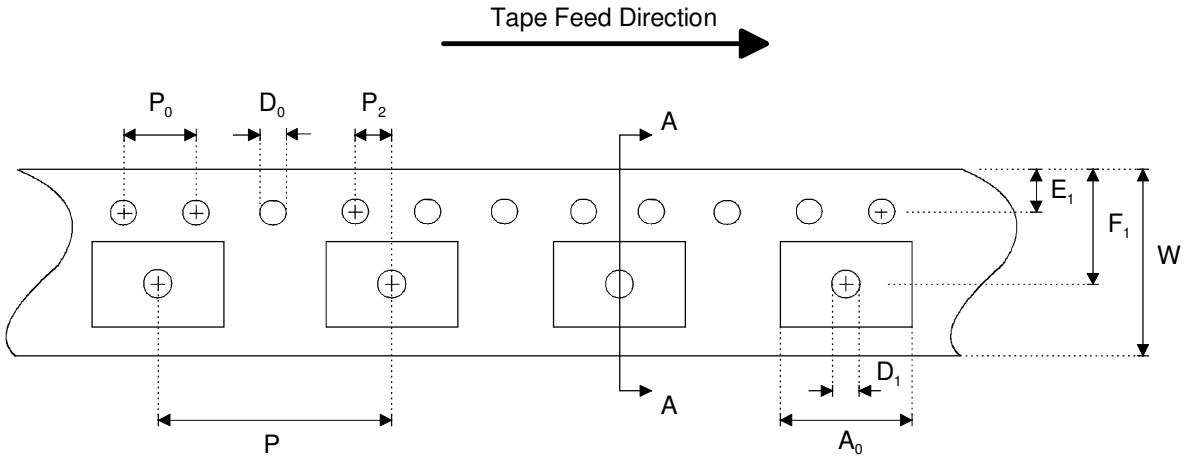
Dimensions do not include mold flash, protrusions, or gate burrs.
All dimensions are in accordance with JEDEC standard MO-153.

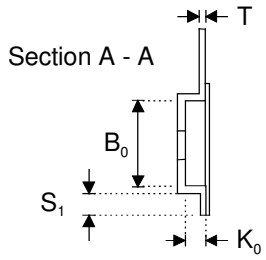
SOLDERING INFORMATION

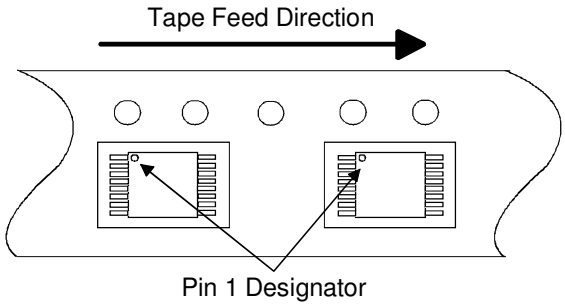
◆ **For Pb-Free, RoHS Compliant TSSOP-16**

Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20
Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in IPC/JEDEC J-STD-020 should not be exceeded. http://www.jedec.org
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 µm, material Matte Tin

EMBOSSED TAPE SPECIFICATIONS

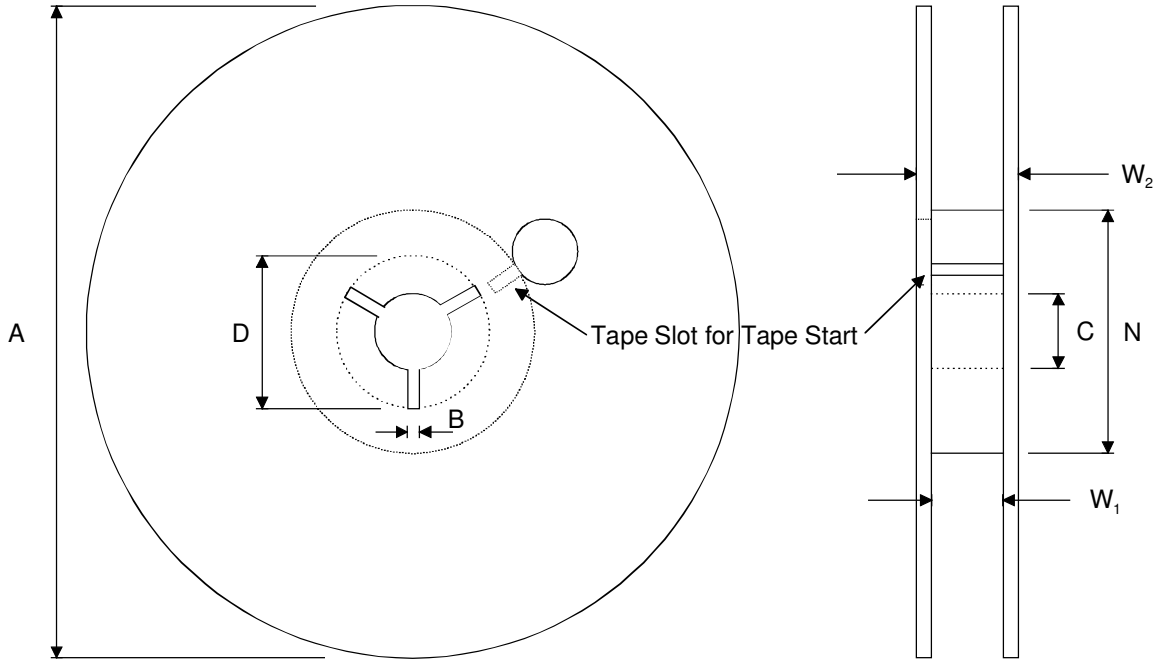






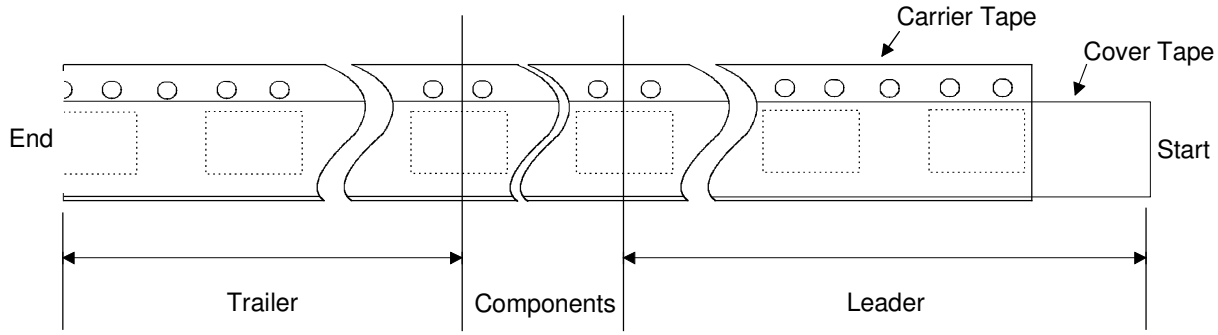
Dimension	Min	Max	Unit
A_0	6.50	6.70	mm
B_0	5.20	5.40	mm
D_0	1.50 +0.10 / -0.00		mm
D_1	1.50		mm
E_1	1.65	1.85	mm
F_1	7.20	7.30	mm
K_0	1.20	1.40	mm
P	11.90	12.10	mm
P_0	4.0		mm
P_2	1.95	2.05	mm
S_1	0.6		mm
T	0.25	0.35	mm
W	11.70	12.30	mm

REEL SPECIFICATIONS



2000 Components on Each Reel

Reel Material: Conductive, Plastic Antistatic or Static Dissipative
Carrier Tape Material: Conductive
Cover Tape Material: Static Dissipative



Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	50		mm
W_1 (measured at hub)	12.4	14.4	mm
W_2 (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm
Weight		1500	g

ORDERING INFORMATION

Product Code	Product	Description	Capacitance Option
MAS9081A1TC00	Dual Band AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 µm.	C_C = 0.75 pF
MAS9081A3TC00	Dual Band AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 µm.	C_C = 1.25 pF
MAS9081A4TC00	Dual Band AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 µm.	C_C = 1.5 pF
MAS9081A5TC00	Dual Band AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 µm.	C_C = 3.875 pF
MAS9081A1UC06	Dual Band AM-Receiver IC with Differential Input	TSSOP-16, Pb-free, RoHS compliant, Tape & Reel	C_C = 0.75 pF

Contact Micro Analog Systems Oy for other wafer thickness options.

LOCAL DISTRIBUTOR

MICRO ANALOG SYSTEMS OY CONTACTS

Micro Analog Systems Oy Kamreerintie 2, P.O. Box 51 FIN-02771 Espoo, FINLAND	Tel. +358 9 80 521 Fax +358 9 805 3213 http://www.mas-oy.com

NOTICE
Micro Analog Systems Oy reserves the right to make changes to the products contained in this data sheet in order to improve the design or performance and to supply the best possible products. Micro Analog Systems Oy assumes no responsibility for the use of any circuits shown in this data sheet, conveys no license under any patent or other rights unless otherwise specified in this data sheet, and makes no claim that the circuits are free from patent infringement. Applications for any devices shown in this data sheet are for illustration only and Micro Analog Systems Oy makes no claim or warranty that such applications will be suitable for the use specified without further testing or modification.