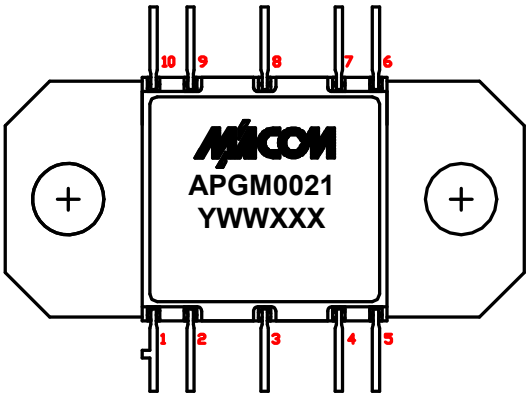
5.0-8.5 GHz 2W Power Amplifier

MAAPGM0021
RO-P-DS-3067 D

Features

- 2 Watt Saturated Output Power Level
- Variable Drain Voltage (4-10V) Operation
- MSAG™ Process
- High Performance Ceramic Bolt Down Package



Primary Applications

- Multiple Band Point-to-Point Radio
- SatCom
- ISM Band

Description

The MAAPGM0021 is a 2-stage 2 W power amplifier with on-chip bias networks in a bolt down ceramic package, allowing easy assembly. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using M/A-COM's GaAs Multifunction Self-Aligned Gate MESFET Process. M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors and multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Pin Number	RF Designator
1	No Connection
2	V_{GG}
3	RF IN
4	V_{GG}
5	No Connection
6	No Connection
7	V_{DD}
8	RF OUT
9	V_{DD}
10	No Connection

Maximum Operating Conditions [1]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	23.0	dBm
Drain Supply Voltage	V_{DD}	+12.0	V
Gate Supply Voltage	V_{GG}	-3.0	V
Quiescent Drain Current (No RF)	I_{DQ}	790	mA
Quiescent DC Power Dissipated (No RF)	P_{DISS}	6.3	W
Junction Temperature	T_J	180	°C
Storage Temperature	T_{STG}	-55 to +150	°C

1. Operation outside of these ranges may reduce product reliability.

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Recommended Operating Conditions

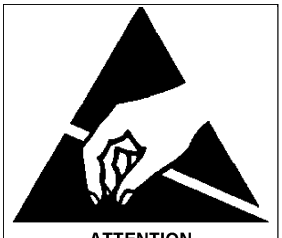
Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	V_{DD}	4.0	8.0	10.0	V
Gate Supply Voltage	V_{GG}	-2.4	-1.7	-1.3	V
Input Power	P_{IN}		18	21.0	dBm
Junction Temperature	T_J			150	°C
Thermal Resistance	Θ_{JC}		14.9		°C/W
MMIC Base Temperature	T_B			Note 2	°C

2. Maximum MMIC Base Temperature = 150°C — Θ_{JC}* V_{DD} * I_{DQ}

Electrical Characteristics: $T_B = 40°C^2$, $Z_0 = 50\ \Omega$, $V_{DD} = 8V$, $I_{DQ} = 600$ mA, $P_{in} = 18$ dBm, $R_G = 121\Omega$

Parameter	Symbol	Minimum	Typical*	Maximum	Units
Bandwidth	f	—	5.0-8.5	—	GHz
Output Power	POUT	31.5	33	—	dBm
Output Power @ 7 GHz	POUT	32	33	34*	dBm
Power Added Efficiency	PAE	—	30	—	%
1-dB Compression Point	P1dB	—	32	—	dBm
Small Signal Gain	G	14	17	—	dB
Small Signal Gain @ 7 GHz	G	17.5	20	22*	dB
Input VSWR	VSWR	—	1.6	2.6	—
Input VSWR @ 7 GHz	VSWR	1.2*	1.4	1.8	—
Output VSWR	VSWR	—	2:1	—	—
Gate Supply Current	I_{GG}	-10	0	10	mA
Gate Supply Current @ 7 GHz	I_{GG}	-10	0	10	mA
Drain Supply Current	I_{DD}	—	0.9	1.2	A
Drain Supply Current @ 7 GHz	I_{DD}	0.6*	0.8	1.0	A
Noise Figure	NF	—	9.5	—	dB
2nd Harmonic	2f	—	-20	—	dBc
3rd Harmonic	3f	—	-45	—	dBc
Output Third Order Intercept	OTOI	—	40	—	dBm
3rd Order Intermodulation Distortion, Single Carrier Level = 23 dBm	IM3	—	-10	—	dBm
5th Order Intermodulation Distortion, Single Carrier Level = 23 dBm	IM5	—	-25	—	dBm

3. Adjust V_{GG} between –2.4 to-1.3 to achieve indicated I_{DQ}. **4. *Not screened—shown to indicate range of expected values.**



ATTENTION
Static-Sensitive Devices
Handling Precautions Required

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{GG} = -1.7 V, V_{DD}= 0 V.
2. Ramp V_{DD} to desired voltage, typically 8 V.
3. Adjust V_{GG} to set I_{DQ}, (approxmately @ –1.7V).
4. Set RF input.

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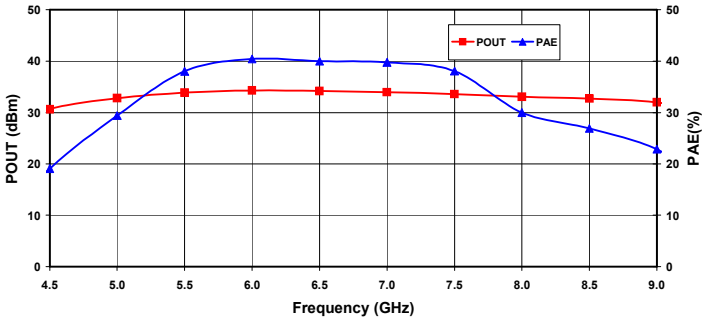


Figure 1. Output Power and Power Added Efficiency vs. Frequency
at V_{DD} = 8V and P_{in} = 18 dBm

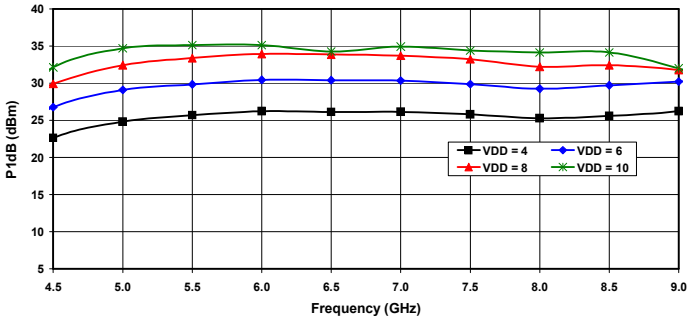


Figure 2. 1dB Compression Point vs. Drain Voltage

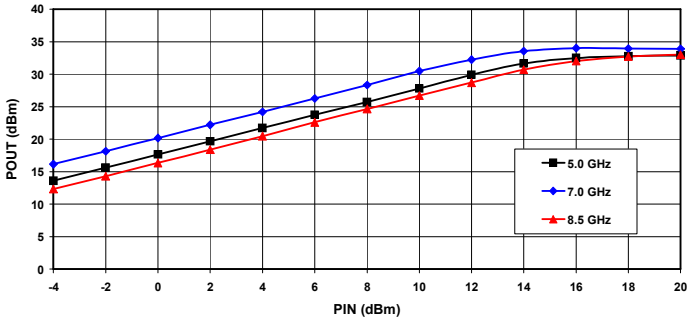


Figure 3. Output Power vs. Input Power
at V_{DD} = 8V

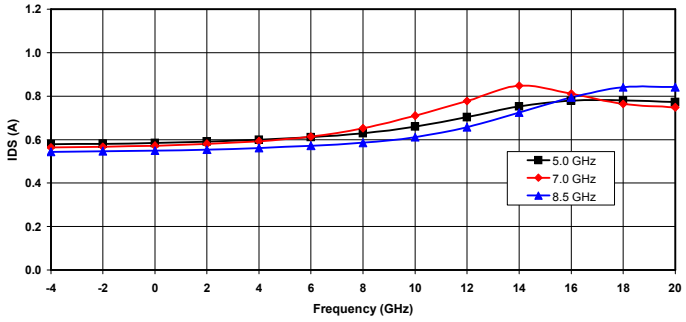


Figure 4. Drain Current vs. Input Power
at V_{DD} = 8V

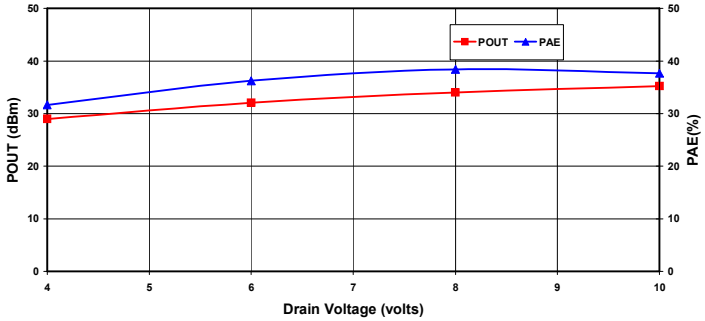


Figure 5. Saturated Output Power and Power Added Efficiency vs. Drain Voltage
at f_o = 7 GHz

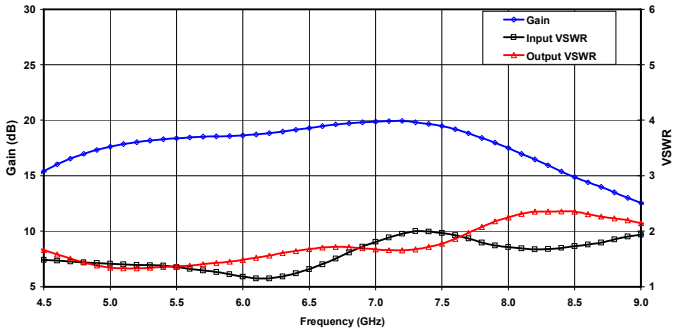


Figure 6. Small Signal Gain and VSWR vs. Frequency at VDD = 8V.

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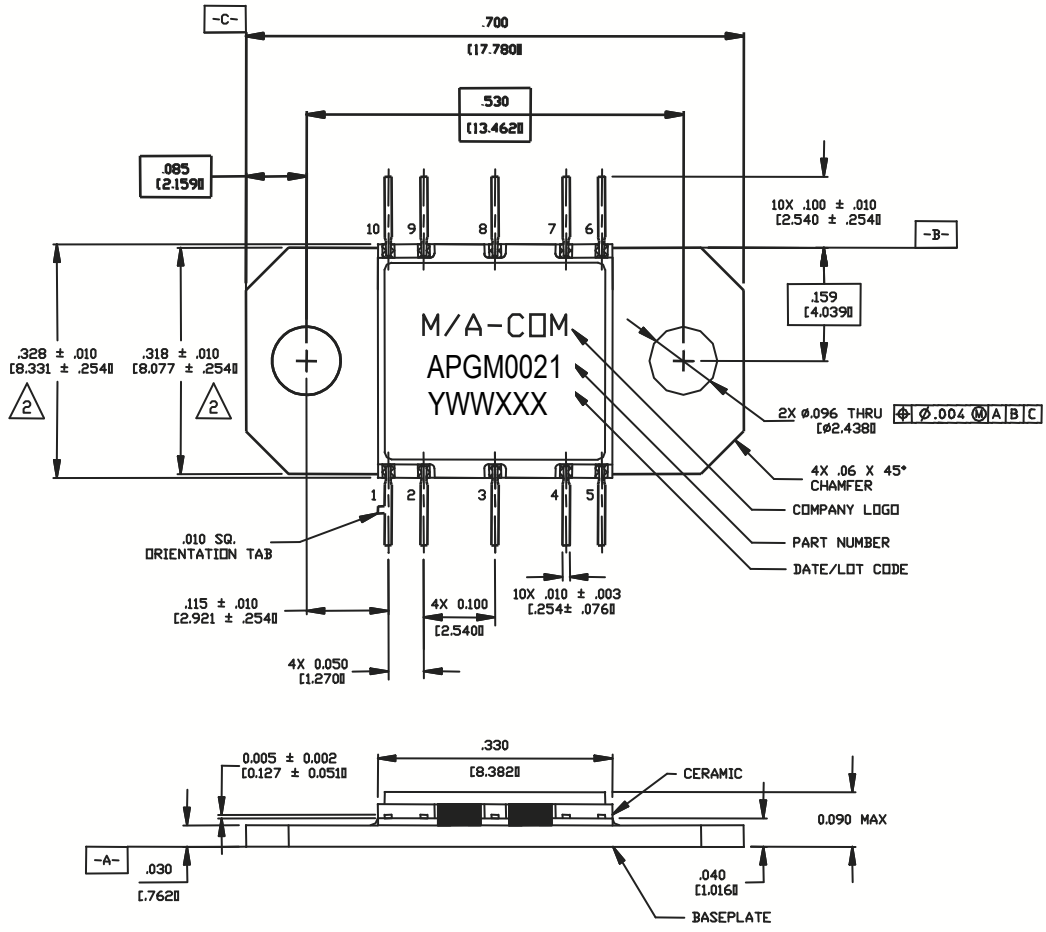


Figure 6. CR-15 Package Dimensions

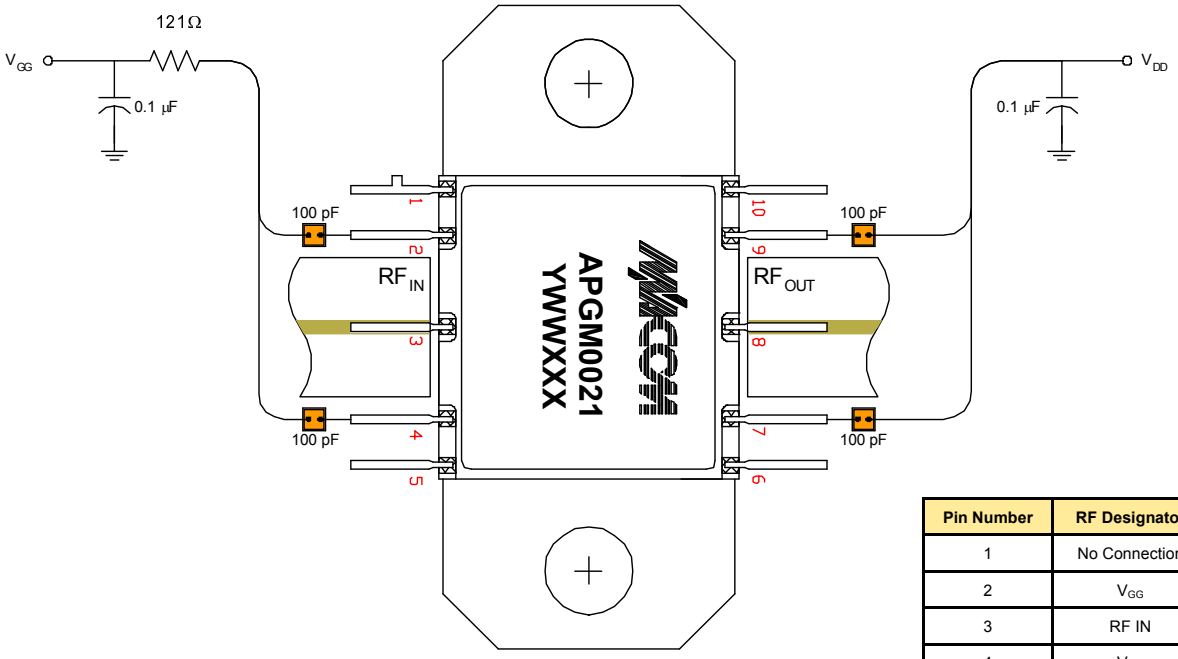
The CR-15 is a high frequency, low thermal resistance package. The package consists of a cofired ceramic construction with a copper-tungsten base and iron-nickel-cobalt leads. The finish consists of electrolytic gold over nickel plate.

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Figure 7. Recommended Bias Configuration



Pin Number	RF Designator
1	No Connection
2	V_{GG}
3	RF IN
4	V_{GG}
5	No Connection
6	No Connection
7	V_{DD}
8	RF OUT
9	V_{DD}
10	No Connection

Assembly Instructions:

This flange mount style package provides a robust interface between a highly integrated GaAs MMIC device and a circuit board which may be assembled using conventional surface mount techniques. A thin shim made of a thermally and electrically conductive, ductile material should be used prior to installation of the CR-15 to improve the thermal and electrical performance of the package to housing interface. Refer to **M/A-COM Application Note #M567*** for more information .

For applications where surface mount components are to be installed after the CR-15 installation, this package will not be damaged when subjected to typical convection or IR oven reflow profiles. Refer to **M/A-COM Application Note #M538*** for maximum allowable reflow time and temperature. Alternatively, the package leads may be individually soldered. Whether an iron or hot gas soldering equipment is used, care should be taken to insure that the temperature is well controlled and electric static discharge (ESD) safe.

* Application Notes can be found by going to the Site Search Page on M/A-COM's web page (http://www.macom.com/search/search.jsp) and searching for the required Application Note.

Biasing Notes:

- The 100pF bypass capacitors must be placed as close to the V_{GG} and V_{DD} pins as possible (recommended < 100 mils).
- A negative bias must be applied to V_{GG} before applying a positive bias to V_{DD} to prevent damage to the amplifier.

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