MAAD-007080

Digital Attenuator
50.0 dB, 6-Bit, TTL Driver, DC-2.4 GHz

Rev. V5

Features

- Attenuation: 1 dB Steps to 50 dB
- Single Positive Supply
- Contains Internal DC to DC Converter
- Low DC Power Consumption
- Small Footprint, JEDEC Package
- Integral TTL Driver
- 50 ohm Impedance
- Lead-Free CSP-1 Package
- 100% Matte Tin Plating over Copper
- Halogen-Free “Green” Mold Compound
- 260°C Reflow Compatible
- RoHS* Compliant Version of AT90-1106

Description

The MAAD-007080 is a GaAs FET 6-bit digital attenuator with integral TTL driver. Step size is 1 dB providing a 50 dB total attenuation range. This device is in a PQFN plastic surface mount package. MAAD-007080 is ideally suited for use where accuracy, fast speed, very low power consumption and low costs are required.

For dual supply designs without switching noise, use MAAD-007082-000100.

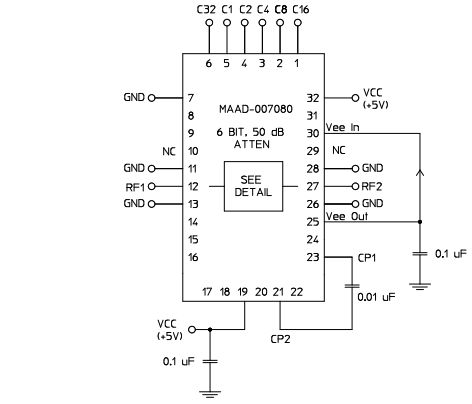
Ordering Information

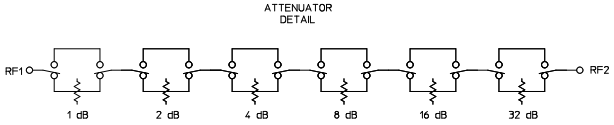
Part Number	Package
MAAD-007080-00100	Bulk Packaging
MAAD-007080-001TR	1000 piece reel
MAAD-0007080-001TB	Sample Test Board

Note: Reference Application Note M513 for reel size information.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

Functional Schematic





Pin Configuration[1]

Pin No.	Function	Pin No.	Function
1	C16	17	NC
2	C8	18	NC
3	C4	19	+Vcc
4	C2	20	NC
5	C1	21	Cp
6	C32	22	NC
7	GND	23	Cp
8	NC	24	NC
9	NC	25	-Vee[3]
10	NC[2]	26	GND
11	GND	27	RF2
12	RF1	28	GND
13	GND	29	NC[2]
14	NC	30	-Vee[3]
15	NC	31	NC
16	NC	32	+Vcc

1. The exposed pad centered on the package bottom must be connected to RF and DC ground. (For PQFN Packages)
2. Pins 10 & 29 must be isolated
3. -Vee is produced internally and requires a .1µF cap to GND. Generated noise is typical of switching DC-DC Converters.

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Digital Attenuator
50.0 dB, 6-Bit, TTL Driver, DC-2.4 GHz

Rev. V5

Electrical Specifications: T_A = 25°C, Z_0 = 50 Ω

Parameter	Test Conditions	Frequency	Units	Min	Typ	Max
Insertion Loss	—	DC - 2.4 GHz	dB	—	5.5	6.0
Attenuation Accuracy	Individual Bits 1-2-4-8-16-32 dB Any Combination of Bits 1 to 50 dB	DC - 2.4 GHz DC - 2.4 GHz	dB	±(.3 +5% of atten setting) ±(.5 +8% of atten setting)		
VSWR	Full Range	DC - 2.4 GHz	Ratio	—	1.8:1	2:1
Switching Speed	50% Cntl to 90%/10% RF 10% to 90% or 90% to 10%	—	ns	—	75 20	—
1 dB Compression	—	50 MHz 0.5 - 2.4 GHz	dBm	—	+21 +24	—
Input IP_3	Two-tone inputs up to +5 dBm	50 MHz 0.5-2.4 GHz	dB	—	+35 +48	—
Vcc	—	—	V	4.75	5.0	5.25
V_{IL} V_{IH}	LOW-level input voltage HIGH-level input voltage	—	V	0.0 2.0	—	0.8 5.0
Iin (Input Leakage Current)	Vin = V_{CC} or GND	—	µA	-1.0	—	1.0
Icc[4]	Vcc min to max, Logic "0" or "1"	—	mA	—	6	10
Turn-on Current[5]	For guaranteed start-up	—	mA	—	—	125
ΔIcc (Additional Supply Current Per TTL Input Pin)	V_{CC} = Max, Vcntrl = V_{CC} - 2.1 V		mA	—	—	1.0
Switching Noise	Generated from DC-DC Converter with recommended capacitors	3.5 MHz	dBm	—	-93	—
Thermal Resistance θjc	—	—	°C/W	—	15	—

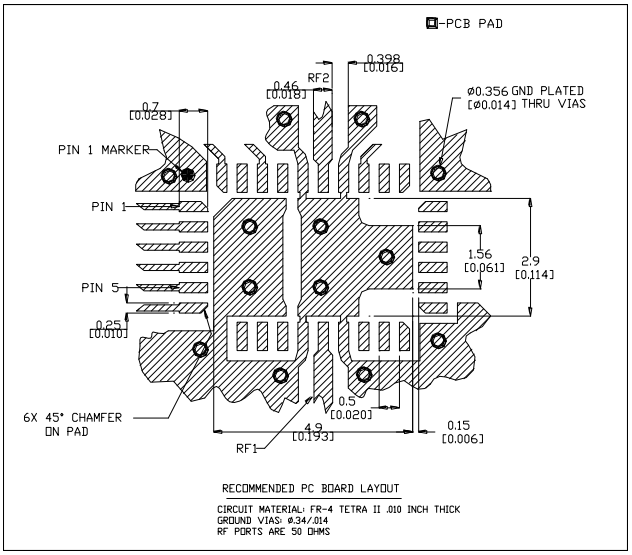
4. During turn-on, the device requires an initial "Turn-on Current". Once operational, Icc will drop to the specified levels.
5. The DC-DC converter is guaranteed to start in 100 µs as long as the power supplies can provide a minimum of 100 mA "Turn-on Current".

Absolute Maximum Ratings[6,7]

Parameter	Absolute Maximum
Input Power 0.05 GHz 0.5 - 2.4 GHz	 +27 dBm +34 dBm
V_{CC}	-0.5V ≤ V_{CC} ≤ +6.0V
Vin[8]	-0.5V ≤ Vin ≤ V_{CC} + 0.5V
Operating Temperature	-40ºC to +85ºC
Storage Temperature	-65ºC to +125ºC

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.
8. Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

Recommended PCB Configuration[9]



9. Application Note S2083 is available at www.macom.com.

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Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Moisture Sensitivity

The MSL rating for this part is defined as Level 2 per IPC/JEDEC J-STD-020. Parts shall be stored and/or baked as required for MSL Level 2 parts.

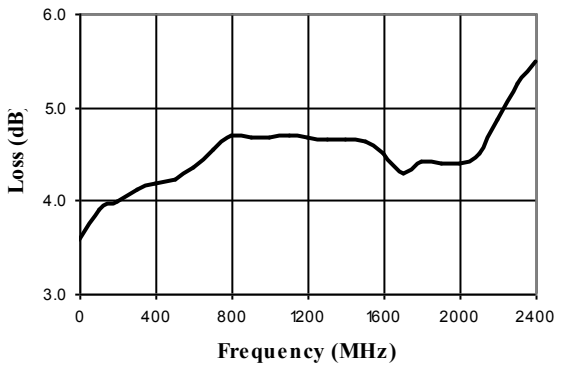
Truth Table (Digital Attenuator)

C32	C16	C8	C4	C2	C1	Attenuation
0	0	0	0	0	0	Loss, Reference
0	0	0	0	0	1	1.0 dB
0	0	0	0	1	0	2.0 dB
0	0	0	1	0	0	4.0 dB
0	0	1	0	0	0	8.0 dB
0	1	0	0	0	0	16.0 dB
1	0	0	0	0	0	32.0 dB
1	1	0	0	1	0	50.0 dB

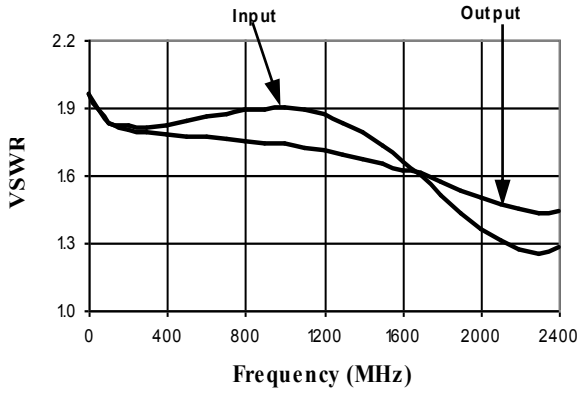
0 = TTL Low; 1 = TTL High

Typical Performance Curves

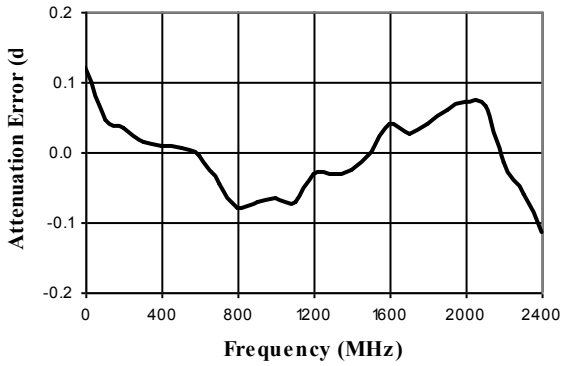
Insertion Loss



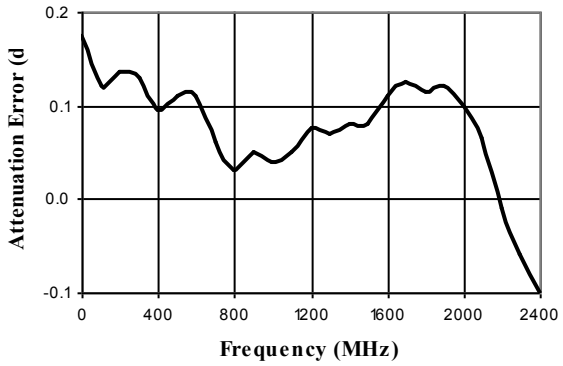
VSWR @ Insertion Loss



Attenuation Error, 1 dB Bit



Attenuation Error, 2 dB Bit



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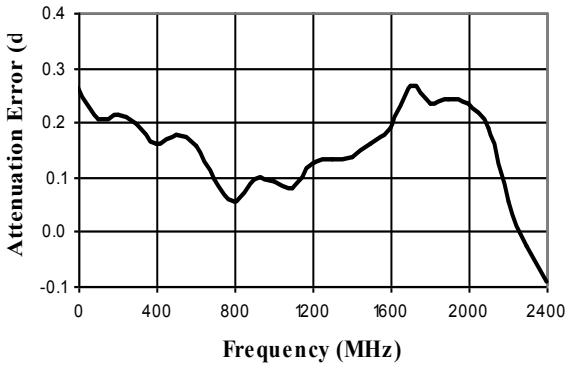
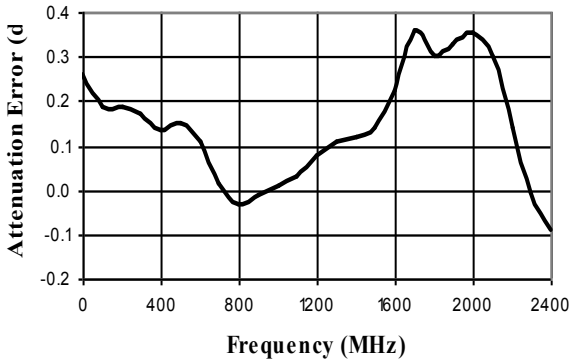
Typical Performance Curves

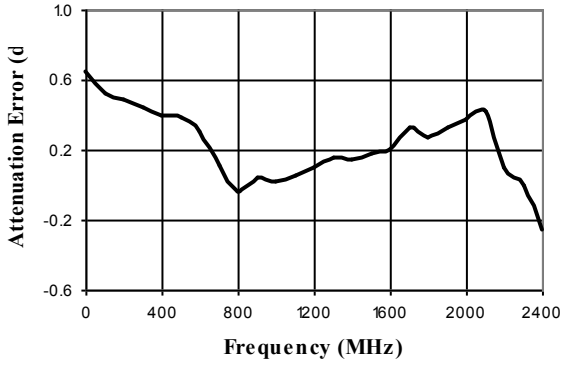
Attenuation Error, 4 dB Bit



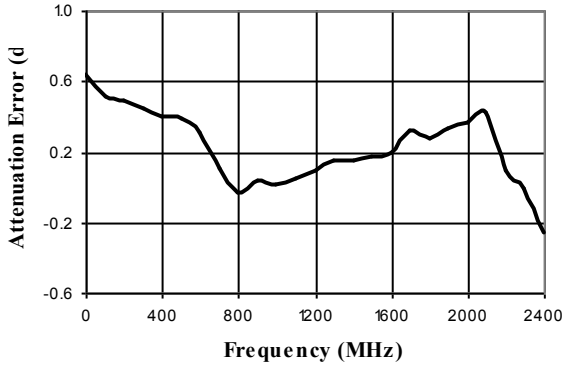
Attenuation Error, 8 dB Bit



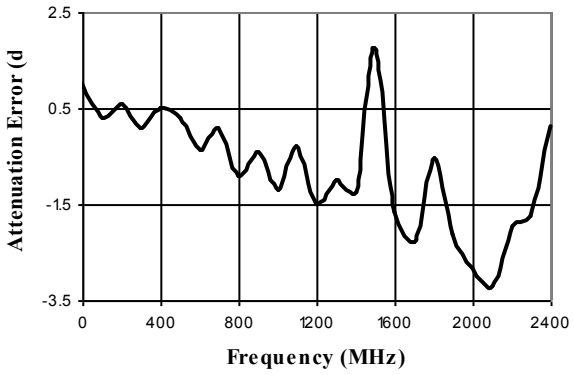
Attenuation Error, 16 dB Bit



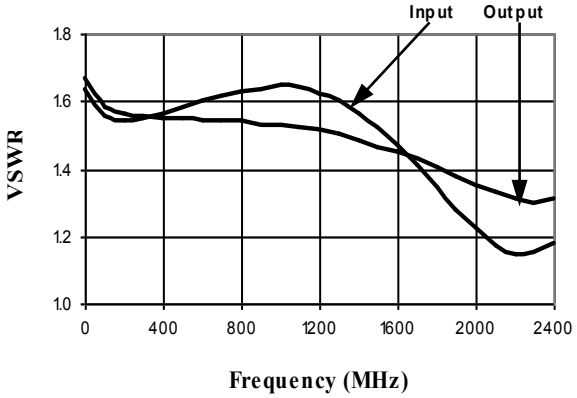
Attenuation Error, 32 dB Bit



Attenuation Error, Max. Attenuation



VSWR, 1 dB Bit



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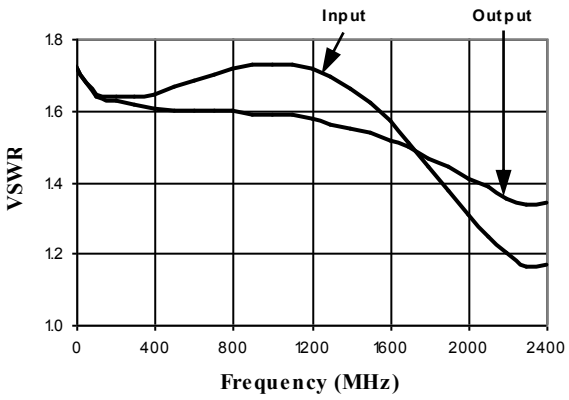
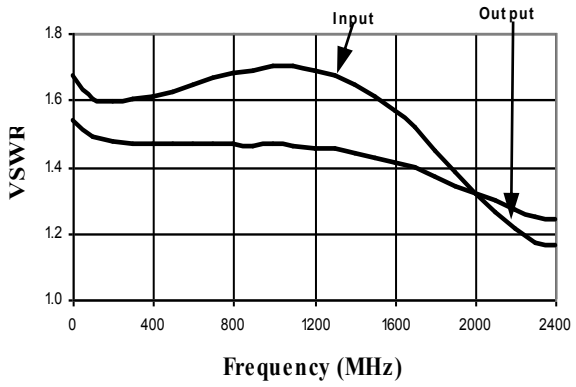
Typical Performance Curves

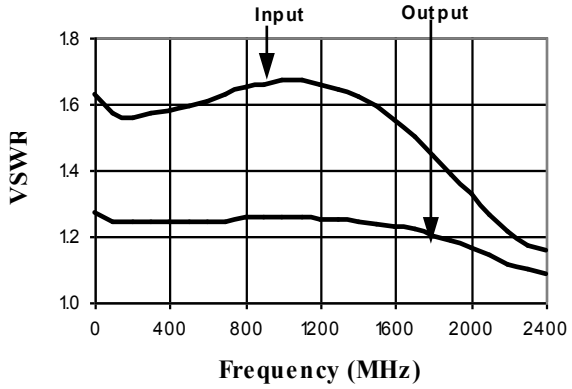
VSWR, 2 dB Bit



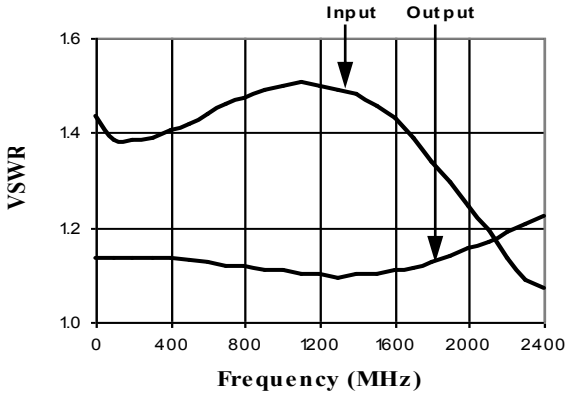
VSWR, 4 dB BIt



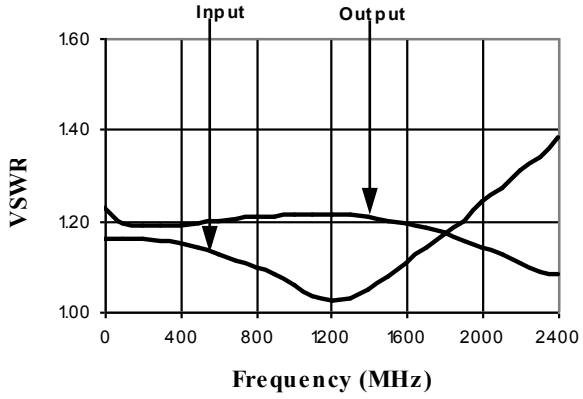
VSWR, 8 dB Bit



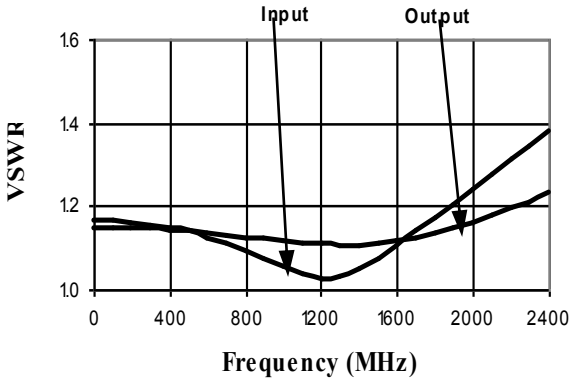
VSWR, 16 dB Bit



VSWR, 32 dB Bit



VSWR, Maximum attenuation



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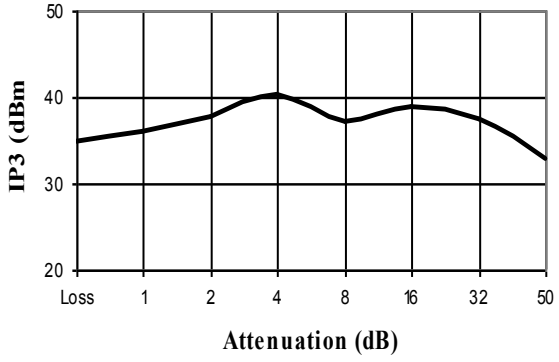
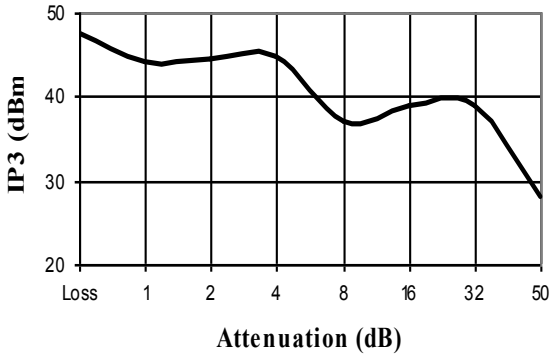
Typical Performance Curves

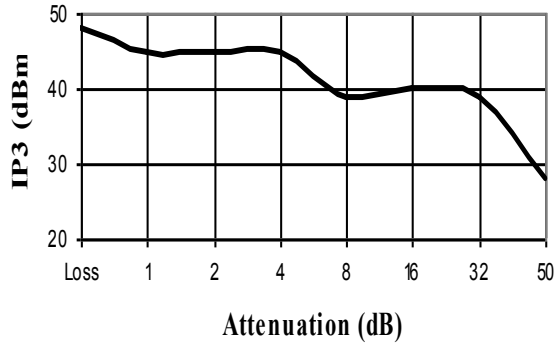
Maximum IP3 over Temperature Range and Attenuation @ 50 MHz



Maximum IP3 over Temperature Range and Attenuation @ 950 MHz



Maximum IP3 over Temperature Range and Attenuation @ 1900 MHz



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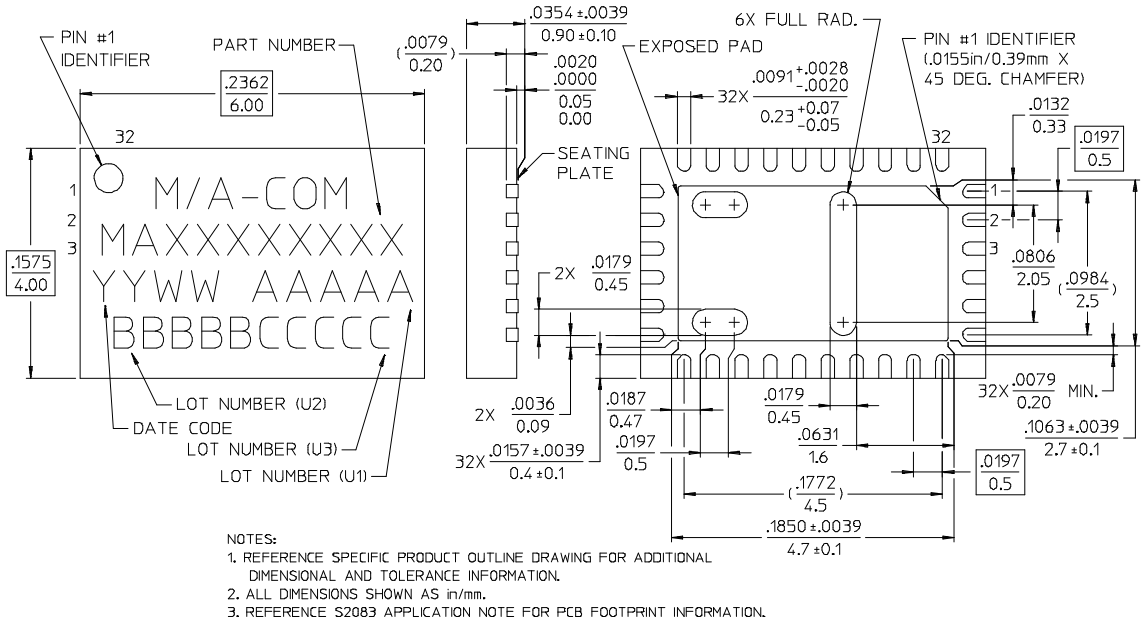
CSP-1, Lead-Free 4 x 6 mm, 32-lead PQFN†



† Reference Application Note M538 for lead-free solder reflow recommendations.

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