M95320 M95320-W M95320-R
M95640 M95640-W M95640-R

32 Kbit and 64 Kbit Serial SPI bus EEPROMs with high speed clock

Feature summary

- Compatible with SPI Bus Serial Interface (Positive Clock SPI Modes)
- Single Supply Voltage:
  - 4.5 to 5.5V for M95320 and M95640
  - 2.5 to 5.5V for M95320-W and M95320-W
  - 1.8 to 5.5V for M95320-R and M95640-R
- 10MHz, 5MHz or 2MHz clock rates
- 5ms or 10ms Write Time
- Status Register
- Hardware Protection of the Status Register
- Byte and Page Write (up to 32 Bytes)
- Self-Timed Programming Cycle
- Adjustable Size Read-Only EEPROM Area
- Enhanced ESD Protection
- More than 1 million Write cycles
- More than 40-Year Data Retention
- Packages
  - ECOPACK® (RoHS compliant)



SO8 (MN)
150 mil width



TSSOP8 (DW)
169 mil width



MLP8 (MB)
2x3 mm

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1 Summary description

These electrically erasable programmable memory (EEPROM) devices are accessed by a high speed SPI-compatible bus.

The M95320, M95320-W and M95320-R are 32Kbit devices organized as 4096 x 8 bits. The M95640, M95640-W and M95640-R are 64Kbit devices organized as 8192 x 8 bits.

The device is accessed by a simple serial interface that is SPI-compatible. The bus signals are C, D and Q, as shown in *Table 1* and *Figure 1*.

The device is selected when Chip Select ($\overline{S}$) is taken Low. Communications with the device can be interrupted using Hold ($\overline{HOLD}$).

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages.
ECOPACK® packages are Lead-free and RoHS compliant.

ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

Figure 1. Logic diagram

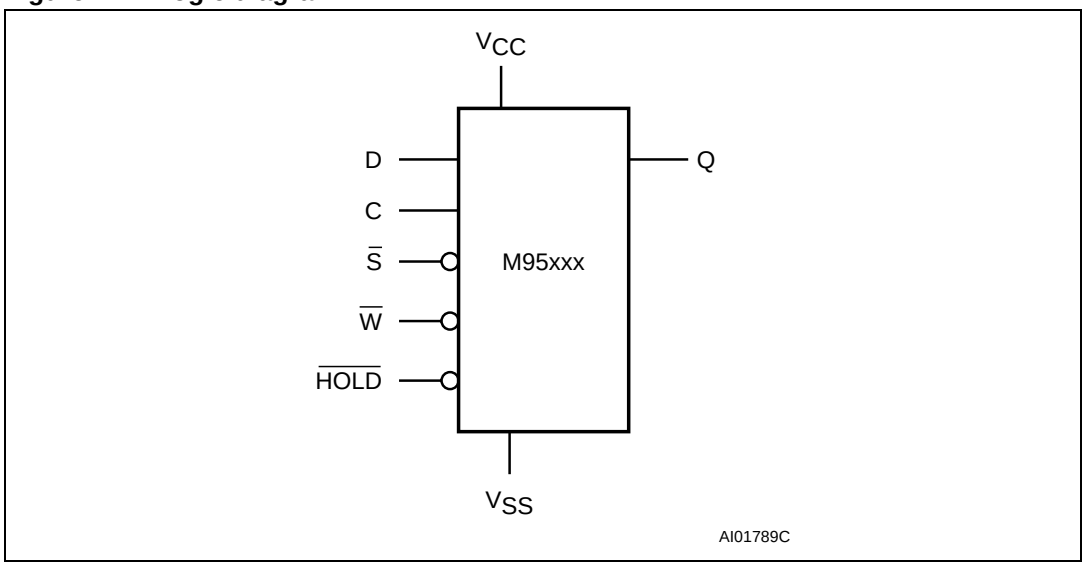
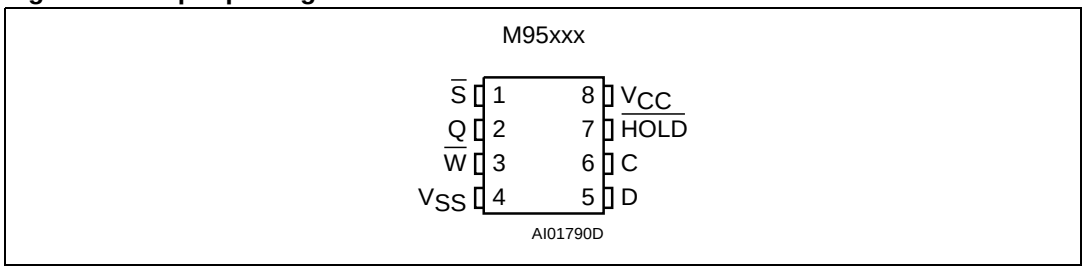


Figure 2. 8 pin package connections



1. See *Package mechanical* section for package dimensions and how to identify pin-1.

Table 1. Signal names

C	Serial Clock
D	Serial data Input
Q	Serial data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

2 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals must be held High or Low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in *Table 13* to *Table 17*). These signals are described next.

2.0.1 Serial Data Output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

2.0.2 Serial Data Input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

2.0.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

2.0.4 Chip Select ($\overline{S}$)

When this input signal is High, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Write cycle is in progress, the device will be in the Standby Power mode. Driving Chip Select ($\overline{S}$) Low selects the device, placing it in the Active Power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.0.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven Low.

2.0.6 Write Protect ($\overline{W}$)

The main purpose of this input signal is to freeze the size of the area of memory that is protected against Write instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

This pin must be driven either High or Low, and must be stable during all write operations.

3 Connecting to the SPI bus

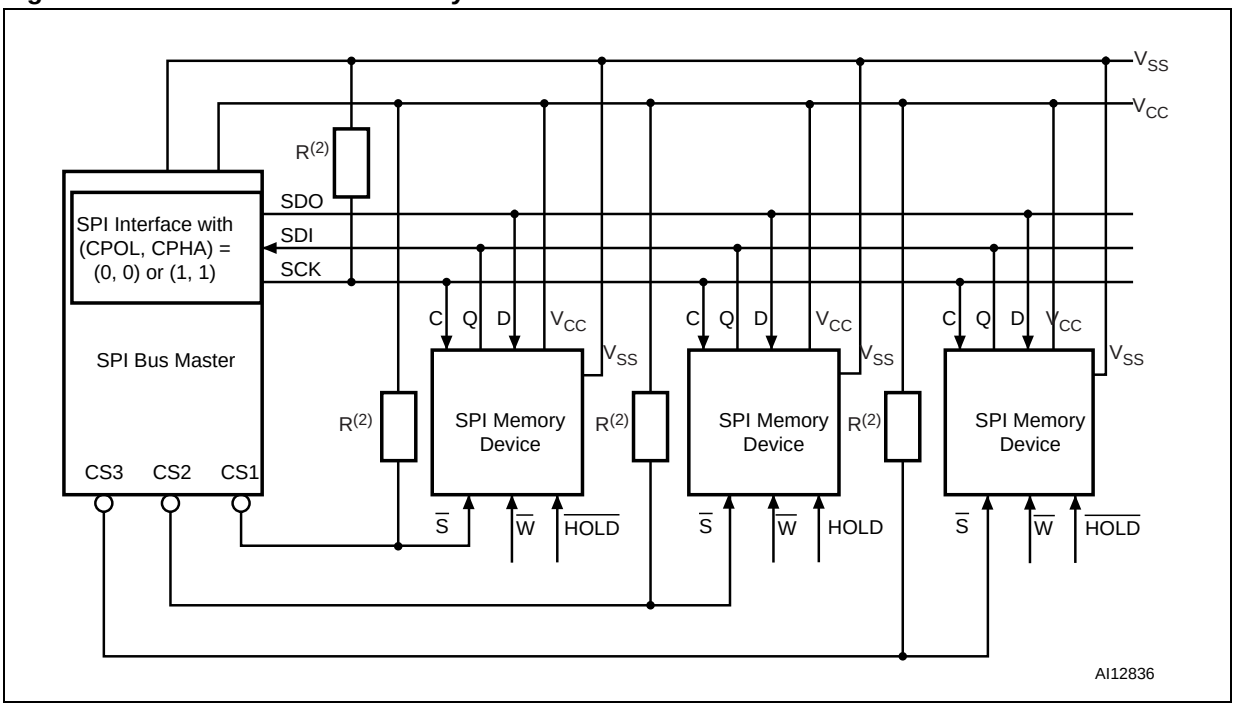
These devices are fully compatible with the SPI protocol.

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ($\overline{S}$) goes Low.

All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 3 shows three devices, connected to an MCU, on a SPI bus. Only one device is selected at a time, so only one device drives the Serial Data Output (Q) line at a time, all the others being high impedance.

Figure 3. Bus master and memory devices on the SPI bus



1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, High or Low as appropriate.
2. These pull-up resistors, R, ensure that the memory devices are not selected if the Bus Master leaves the $\overline{S}$ line in the high-impedance state. As the Bus Master may enter a state where all inputs/outputs are in high impedance at the same time (e.g.: when the Bus Master is reset), the clock line (C) must be connected to an external pull-down resistor so that, when all inputs/outputs become high impedance, $\overline{S}$ is pulled High while C is pulled Low (thus ensuring that $\overline{S}$ and C do not become High at the same time, and so, that the t_{SHCH} requirement is met).

3.1 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

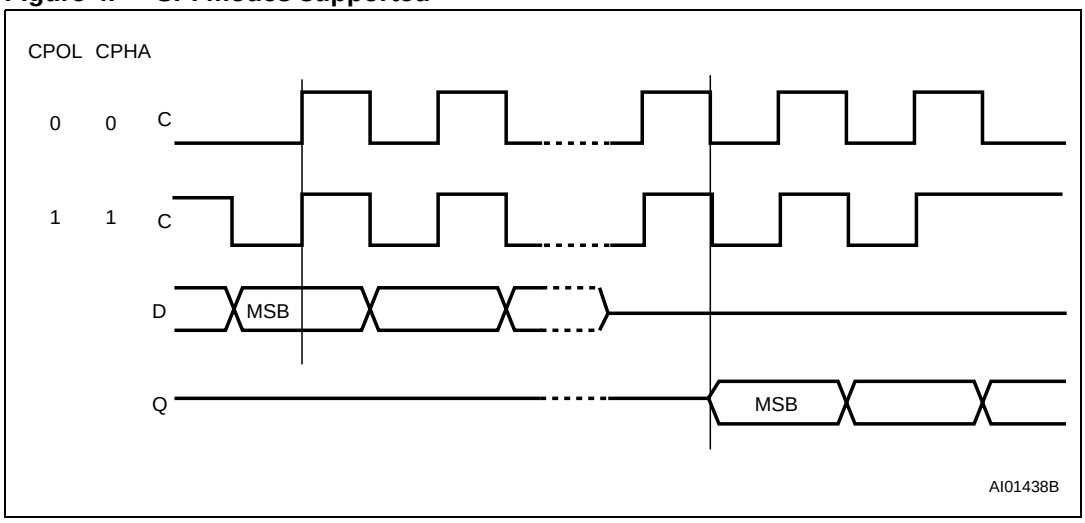
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 4*, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 4. SPI modes supported



4 Operating features

4.1 Supply voltage (V_{CC})

4.1.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Table 8.). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10nF to 100nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

4.1.2 Power-up conditions

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}. During this time, the Chip Select ($\overline{S}$) is not allowed to float but must follow the V_{CC} voltage, therefore the $\overline{S}$ line should be connected to V_{CC} via a suitable pull-up resistor.

In addition, the Chip Select ($\overline{S}$) input offers a built-in safety feature, as the $\overline{S}$ input is edge sensitive as well as level sensitive: after Power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been High, prior to going Low to start the first operation.

The V_{CC} rise time must not be faster than 1V/µs.

4.1.3 Internal device Reset

In order to prevent inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included. At Power-up (continuous rise of V_{CC}), the device will not respond to any instruction until V_{CC} has reached the Power On Reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in Tables XX).

When V_{CC} has passed the POR threshold, the device is reset and in the following state:

- Standby Power mode
- deselected (at next Power-up, a falling edge is required on Chip Select ($\overline{S}$) before any instructions can be started).
- not in the Hold Condition

Status Register state:

- the Write Enable Latch (WEL) is reset to 0
- Write In Progress (WIP) is reset to 0. The SRWD, BP1 and BP0 bits of the Status Register are in the same state as when the power was last removed (they are non-volatile bits).

4.1.4 Power-down

At Power-down (continuous decrease of V_{CC}), as soon as V_{CC} drops from the normal operating voltage to below the Power On Reset threshold voltage, the device stops responding to any instruction sent to it.

During Power-down, the device must be deselected and in Standby Power mode (that is there should be no internal Write cycle in progress). Chip Select ($\overline{S}$) should be allowed to follow the voltage applied on V_{CC}.

4.2 Active Power and Standby Power modes

When Chip Select ($\overline{S}$) is Low, the device is selected, and in the Active Power mode. The device consumes I_{CC}, as specified in *Table 13* to *Table 17*.

When Chip Select ($\overline{S}$) is High, the device is deselected. If an Erase/Write cycle is not currently in progress, the device then goes in to the Standby Power mode, and the device consumption drops to I_{CC1}.

4.2.1 Hold condition

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) Low.

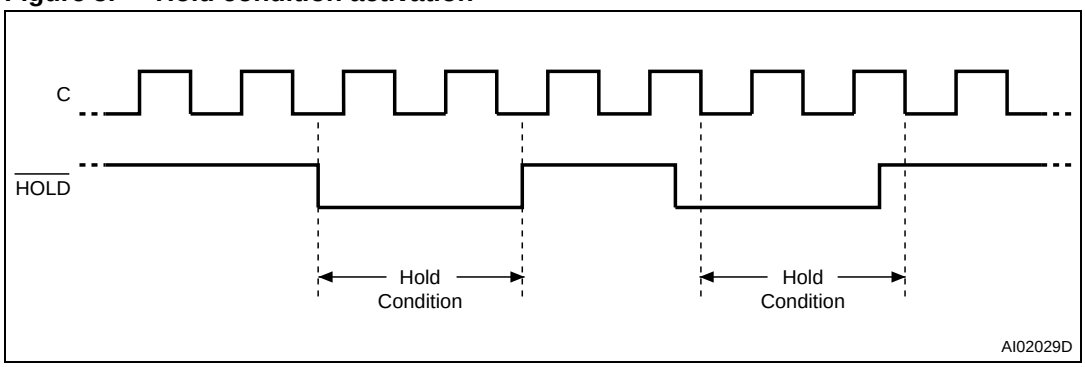
Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold ($\overline{HOLD}$) signal is driven Low at the same time as Serial Clock (C) already being Low (as shown in *Figure 5*).

The Hold condition ends when the Hold ($\overline{HOLD}$) signal is driven High at the same time as Serial Clock (C) already being Low.

Figure 5 also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (C) being Low.

Figure 5. Hold condition activation



4.3 Status Register

Figure 6 shows the position of the Status Register in the control logic of the device. The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See *Section 6.3: Read Status Register (RDSR)* for a detailed description of the Status Register bits.

4.4 Data protection and protocol control

Non-volatile memory devices can be used in environments that are particularly noisy, and within applications that could experience problems if memory bytes are corrupted. Consequently, the device features the following data protection mechanisms:

- Write and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Write (WRITE) instruction completion
- The Block Protect (BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect ($\overline{W}$) signal allows the Block Protect (BP1, BP0) bits to be protected. This is the Hardware Protected Mode (HPM).

For any instruction to be accepted, and executed, Chip Select ($\overline{S}$) must be driven High after the rising edge of Serial Clock (C) for the last bit of the instruction, and before the next rising edge of Serial Clock (C).

Two points need to be noted in the previous sentence:

- The ‘last bit of the instruction’ can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except for Read Status Register (RDSR) and Read (READ) instructions).
- The ‘next rising edge of Serial Clock (C)’ might (or might not) be the next bus transaction for some other device on the SPI bus.

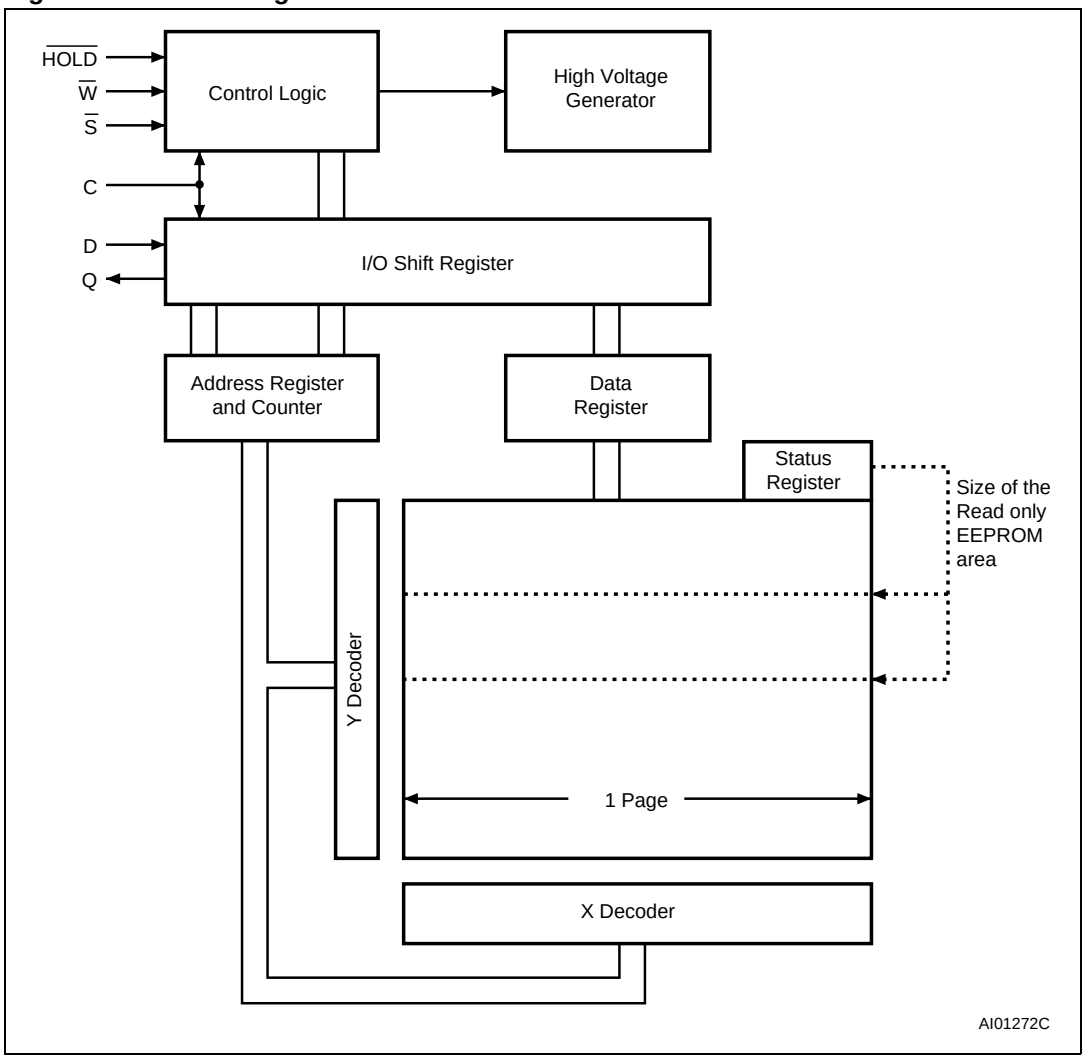
Table 2. Write-Protected block size

Status Register Bits		Protected Block	Array Addresses Protected	
BP1	BP0		M95640, M95640-W, M95640-R, M95640-S	M95320, M95320-W, M95320-R, M95320-S
0	0	none	none	none
0	1	Upper quarter	1800h - 1FFFh	0C00h - 0FFFh
1	0	Upper half	1000h - 1FFFh	0800h - 0FFFh
1	1	Whole memory	0000h - 1FFFh	0000h - 0FFFh

5 Memory organization

The memory is organized as shown in *Figure 6*.

Figure 6. Block diagram



6 Instructions

Each instruction starts with a single-byte code, as summarized in *Table 3*.

If an invalid instruction is sent (one not contained in <Blue>Table 3.), the device automatically deselects itself.

Table 3. Instruction set

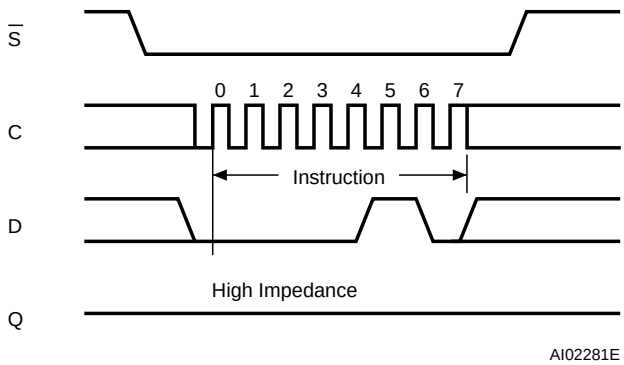
Instruction	Description	Instruction Format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010

6.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.

As shown in *Figure 7*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven Low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven High.

Figure 7. Write Enable (WREN) sequence



6.2 Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

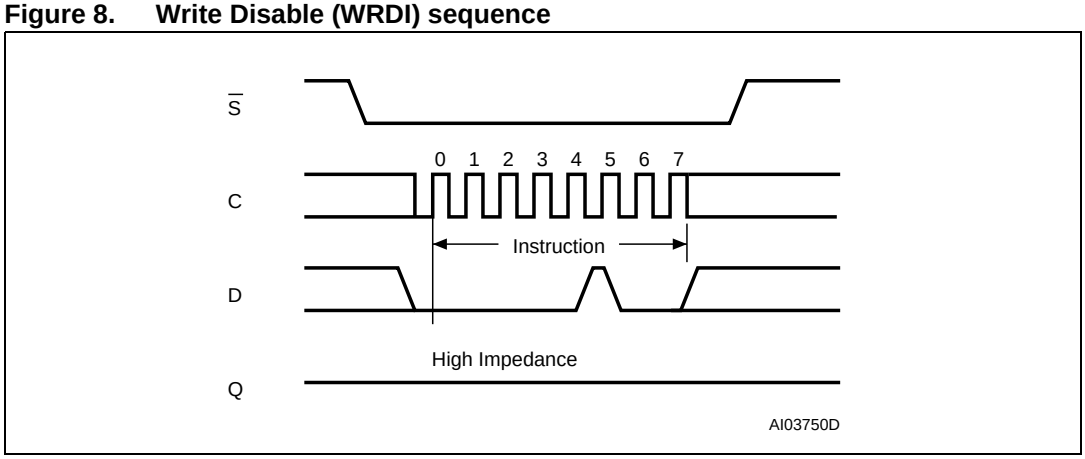
As shown in *Figure 8*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven Low, and the bits of the instruction byte are shifted in, on Serial Data Input (D).

The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven High.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion.

Figure 8. Write Disable (WRDI) sequence



6.3 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Write or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in *Figure 9*.

The Status Register format is shown in *Table 4* and the status and control bits of the Status Register are as follows:

6.3.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

6.3.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write or Write Status Register instruction is accepted.

6.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in *Table 4*) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

6.3.4 SRWD bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect ($\overline{W}$) is driven Low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Table 4. Status Register format

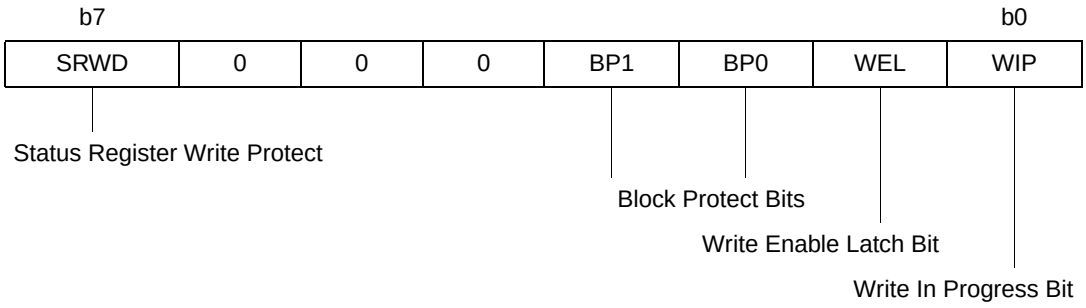
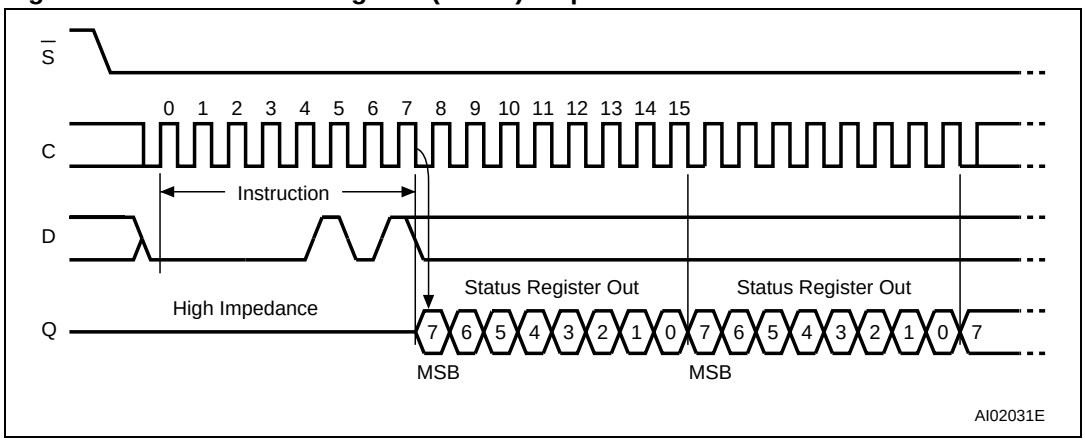


Figure 9. Read Status Register (RDSR) sequence



6.4 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code and the data byte on Serial Data Input (D).

The instruction sequence is shown in *Figure 10*.

The Write Status Register (WRSR) instruction has no effect on b6, b5, b4, b1 and b0 of the Status Register. b6, b5 and b4 are always read as 0.

Chip Select ($\overline{S}$) must be driven High after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in *Table 4*.

The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Write Disable (SRWD) bit in accordance with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

The contents of the Status Register Write Disable (SRWD) and Block Protect (BP1, BP0) bits are frozen at their current values from just before the start of the execution of Write Status Register (WRSR) instruction. The new, updated, values take effect at the moment of completion of the execution of Write Status Register (WRSR) instruction.

Table 5. Protection modes

$\overline{W}$ Signal	SRWD Bit	Mode	Write Protection of the Status Register	Memory Content	
				Protected Area(1)	Unprotected Area(1)
1	0	Software Protected (SPM)	Status Register is Writable (if the WREN instruction has set the WEL bit) The values in the BP1 and BP0 bits can be changed	Write Protected	Ready to accept Write instructions
0	0				
1	1				
0	1	Hardware Protected (HPM)	Status Register is Hardware write protected The values in the BP1 and BP0 bits cannot be changed	Write Protected	Ready to accept Write instructions

1. As defined by the values in the Block Protect (BP1, BP0) bits of the Status Register, as shown in *Table 2*.

The protection features of the device are summarized in *Table 2*.

When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless of the whether Write Protect ($\overline{W}$) is driven High or Low.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to 1, two cases need to be considered, depending on the state of Write Protect ($\overline{W}$):

- If Write Protect ($\overline{W}$) is driven High, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction.
- If Write Protect ($\overline{W}$) is driven Low, it is *not* possible to write to the Status Register *even* if the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM) by the Block Protect (BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

Regardless of the order of the two events, the Hardware Protected Mode (HPM) can be entered:

- by setting the Status Register Write Disable (SRWD) bit after driving Write Protect ($\overline{W}$) Low
- or by driving Write Protect ($\overline{W}$) Low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit the Hardware Protected Mode (HPM) once entered is to pull Write Protect ($\overline{W}$) High.

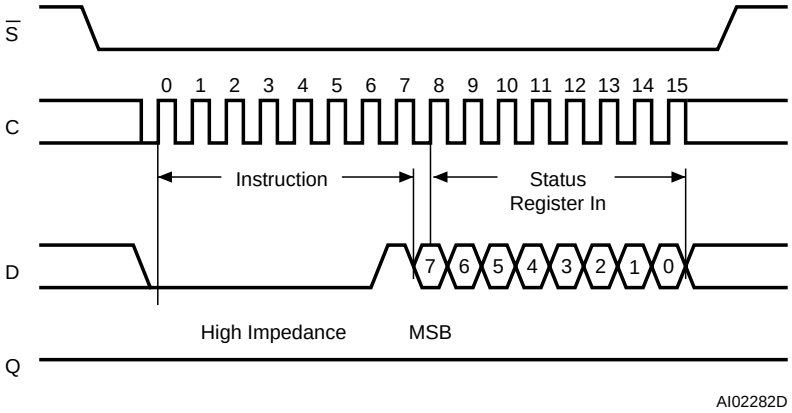
If Write Protect ($\overline{W}$) is permanently tied High, the Hardware Protected Mode (HPM) can never be activated, and only the Software Protected Mode (SPM), using the Block Protect (BP1, BP0) bits of the Status Register, can be used.

Table 6. Address range bits(1)

Device	32 Kbit Devices	64 Kbit Devices
Address Bits	A12-A0	A11-A0

1. b15 to b13 are Don't Care on the 64 Kbit devices.
b15 to b12 are Don't Care on the 32 Kbit devices.

Figure 10. Write Status Register (WRSR) sequence



6.5 Read from Memory Array (READ)

As shown in *Figure 11*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven Low. The bits of the instruction byte and address bytes are then shifted in, on Serial Data Input (D). The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

If Chip Select ($\overline{S}$) continues to be driven Low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

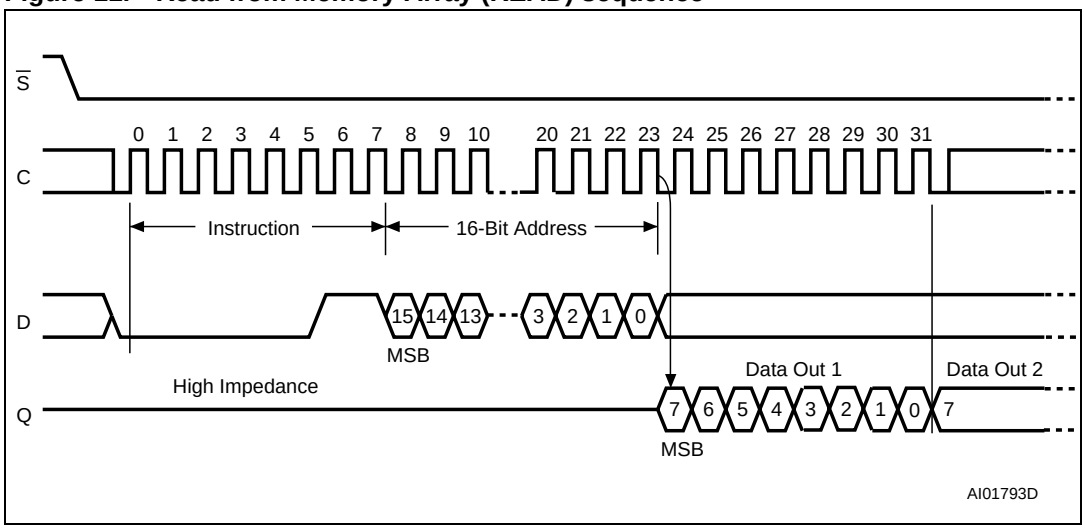
When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) High. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Figure 11. Read from Memory Array (READ) sequence



1. Depending on the memory size, as shown in *Table 6*, the most significant address bits are Don't Care.

6.6 Write to Memory Array (WRITE)

As shown in *Figure 12*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven Low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data Input (D).

The instruction is terminated by driving Chip Select ($\overline{S}$) High at a byte boundary of the input data. In the case of *Figure 12*, this occurs after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. The self-timed Write cycle starts, and continues for a period t_{WC} (as specified in *Table 18* to *Table 22*), at the end of which the Write in Progress (WIP) bit is reset to 0.

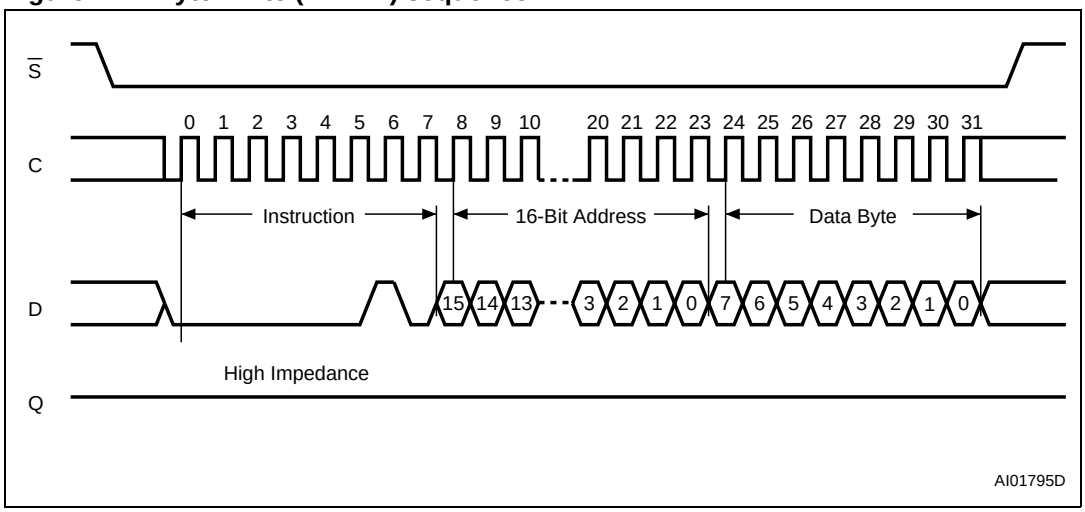
If, though, Chip Select ($\overline{S}$) continues to be driven Low, as shown in *Figure 13*, the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal Write cycle.

Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the number of data bytes sent to the device exceeds the page boundary, the internal address counter rolls over to the beginning of the page, and the previous data there are overwritten with the incoming data. (The page size of these devices is 32 bytes).

The instruction is not accepted, and is not executed, under the following conditions:

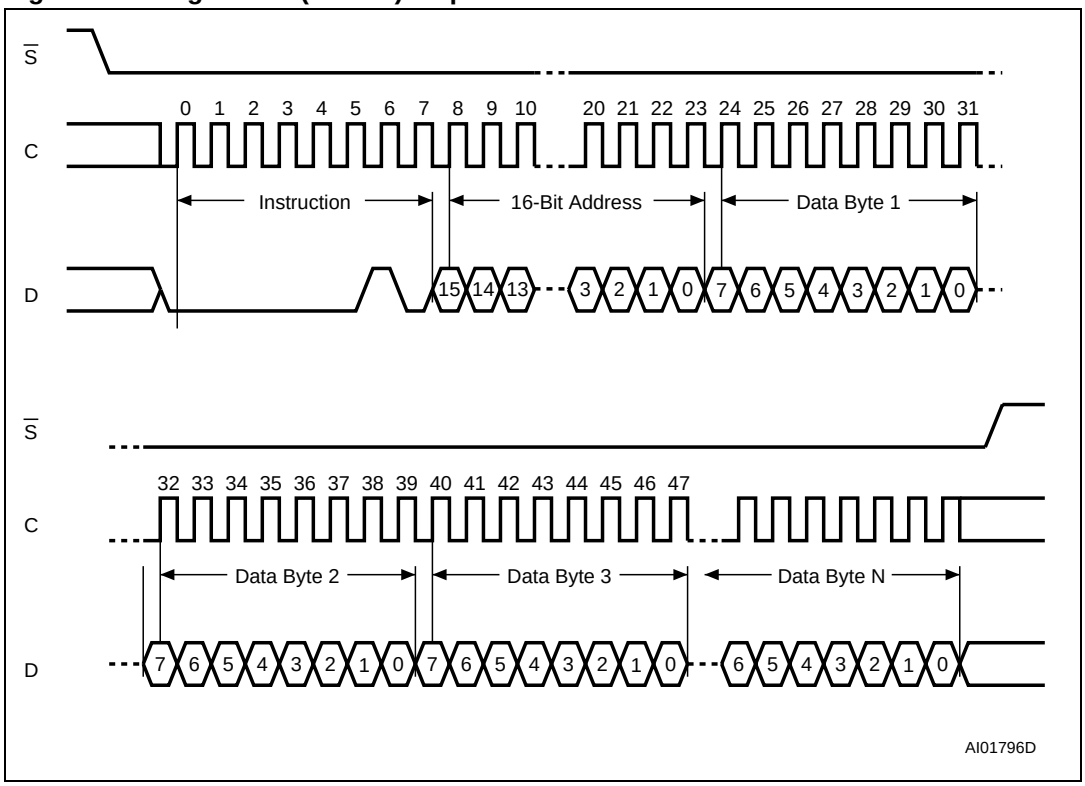
- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- if a Write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven High, at a byte boundary (after the eighth bit, b0, of the last data byte that has been latched in)
- if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

Figure 12. Byte Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 6*, the most significant address bits are Don't Care.

Figure 13. Page Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 6*, the most significant address bits are Don't Care.

7 Power-up and delivery state

7.1 Power-up state

After Power-up, the device is in the following state:

- Standby Power mode
- deselected (after Power-up, a falling edge is required on Chip Select ($\overline{S}$) before any instructions can be started).
- not in the Hold Condition
- the Write Enable Latch (WEL) is reset to 0
- Write In Progress (WIP) is reset to 0

The SRWD, BP1 and BP0 bits of the Status Register are unchanged from the previous power-down (they are non-volatile bits).

7.2 Initial delivery state

The device is delivered with the memory array set at all 1s (FFh). The Status Register Write Disable (SRWD) and Block Protect (BP1 and BP0) bits are initialized to 0.

8 Maximum rating

Stressing the device outside the ratings listed in *Table 7* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the Operating sections of this specification, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 7. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	–65	150	°C
T_A	Ambient operating temperature	–40	130	°C
T_{LEAD}	Lead Temperature during Soldering	See note (1)		°C
V_O	Output Voltage	–0.50	V_{CC}+0.6	V
V_I	Input Voltage	–0.50	6.5	V
V_{CC}	Supply Voltage	–0.50	6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)(2)	–4000	4000	V

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU
2. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114A, C1=100pF, R1=1500Ω, R2=500Ω)

9 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 8. Operating conditions (M95320 and M95640)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
T_A	Ambient Operating Temperature (Device Grade 6)	–40	85	°C
	Ambient Operating Temperature (Device Grade 3)	–40	125	°C

Table 9. Operating conditions (M95320-W and M95640-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.5	5.5	V
T_A	Ambient Operating Temperature (Device Grade 6)	–40	85	°C
	Ambient Operating Temperature (Device Grade 3)	–40	125	°C

Table 10. Operating conditions (M95320-R and M95640-R)

Symbol	Parameter	Min.(1)	Max. (1)	Unit
V_{CC}	Supply Voltage	1.8	5.5	V
T_A	Ambient Operating Temperature	–40	85	°C

1. This product is under development. For more information, please contact your nearest ST sales office.

Table 11. AC measurement conditions(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_L	Load Capacitance		30		pF
	Input Rise and Fall Times			50	ns
	Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$			V
	Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$			V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 14. AC measurement I/O waveform

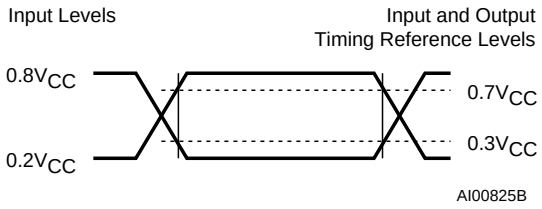


Table 12. Capacitance(1)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{OUT}	Output Capacitance (Q)	V_{OUT} = 0V		8	pF
C_{IN}	Input Capacitance (D)	V_{IN} = 0V		8	pF
	Input Capacitance (other pins)	V_{IN} = 0V		6	pF

1. Sampled only, not 100% tested, at T_A=25°C and a frequency of 5MHz.

Table 13. DC characteristics (M95320 and M95640, device grade 6)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply Current	C = 0.1V_{CC}/0.9V_{CC} at 10MHz, V_{CC} = 5V, Q = open		5	mA
I_{CC1}	Supply Current (Standby)	$\overline{S} = V_{CC}$, V_{CC} = 5V, $V_{IN} = V_{SS}$ or V_{CC}		2	µA
V_{IL}	Input Low Voltage		–0.45	0.3V_{CC}	V
V_{IH}	Input High Voltage		0.7V_{CC}	V_{CC}+1	V
V_{OL}(1)	Output Low Voltage	I_{OL} = 2 mA, V_{CC} = 5V		0.4	V
V_{OH}(1)	Output High Voltage	I_{OH} = –2 mA, V_{CC} = 5V	0.8V_{CC}		V

1. For all 5V range devices, the device meets the output requirements for both TTL and CMOS standards.

Table 14. DC characteristics (M95320 and M95640, device grade 3)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply Current	C = 0.1V_{CC}/0.9V_{CC} at 5MHz, V_{CC} = 5V, Q = open		4	mA
I_{CC1}	Supply Current (Standby)	$\overline{S} = V_{CC}$, V_{CC} = 5V, $V_{IN} = V_{SS}$ or V_{CC}		5	µA
V_{IL}	Input Low Voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}(1)	Output Low Voltage	I_{OL} = 2mA, V_{CC} = 5V		0.4	V
V_{OH}(1)	Output High Voltage	I_{OH} = –2mA, V_{CC} = 5V	0.8 V_{CC}		V

1. For all 5V range devices, the device meets the output requirements for both TTL and CMOS standards.

Table 15. DC characteristics (M95320-W and M95640-W, device grade 6)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply Current	C = $0.1V_{CC}/0.9V_{CC}$ at 5MHz, V_{CC} = 2.5V, Q = open		3	mA
I_{CC1}	Supply Current (Standby)	$\overline{S} = V_{CC}$, V_{CC} = 2.5V $V_{IN} = V_{SS}$ or V_{CC}		1	µA
V_{IL}	Input Low Voltage		–0.45	$0.3V_{CC}$	V
V_{IH}	Input High Voltage		$0.7V_{CC}$	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 1.5mA, V_{CC} = 2.5V or I_{OL} = 2mA, V_{CC} = 5.5V		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.4mA, V_{CC} = 2.5V or I_{OH} = –2mA, V_{CC} = 5.5V	$0.8V_{CC}$		V

Table 16. DC characteristics (M95320-W and M95640-W, device grade 3)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply Current	C = $0.1V_{CC}/0.9V_{CC}$ at 5MHz, V_{CC} = 2.5V, Q = open		3	mA
I_{CC1}	Supply Current (Standby)	$\overline{S} = V_{CC}$, V_{CC} = 2.5V, $V_{IN} = V_{SS}$ or V_{CC}		2	µA
V_{IL}	Input Low Voltage		–0.45	$0.3V_{CC}$	V
V_{IH}	Input High Voltage		$0.7V_{CC}$	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 1.5mA, V_{CC} = 2.5V		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.4mA, V_{CC} = 2.5V	$0.8V_{CC}$		V

Table 17. DC characteristics (M95320-R and M95640-R)

Symbol	Parameter	Test Condition	Min.(1)	Max.(1)	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{CC}		± 1	µA
I_{LO}	Output Leakage Current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 1	µA
I_{CC}	Supply Current	C = $0.1V_{CC}/0.9V_{CC}$ at max clock frequency, $1.8V < V_{CC} = 2.5V$, Q = open		3	mA
I_{CC1}	Supply Current (Standby)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}, $1.8V < V_{CC} = 2.5V$		1	µA
V_{IL}	Input Low Voltage		–0.45	$0.3\ V_{CC}$	V
V_{IH}	Input High Voltage		$0.7\ V_{CC}$	$V_{CC}+1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 0.15$ mA, $V_{CC} = 1.8$ V		0.3	V
V_{OH}	Output High Voltage	$I_{OH} = –0.1$ mA, $V_{CC} = 1.8$ V	$0.8\ V_{CC}$		V

1. This product is under qualification. For more information, please contact your nearest ST sales office.

Table 18. AC characteristics (M95320 and M95640, device grade 6)

Test conditions specified in *Table 11* and *Table 8*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock Frequency	D.C.	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	15		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	15		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	40		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	25		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	15		ns
t_{CH}(1)	t_{CLH}	Clock High Time	40		ns
t_{CL}(1)	t_{CLL}	Clock Low Time	40		ns
t_{CLCH}(2)	t_{RC}	Clock Rise Time		1	µs
t_{CHCL}(2)	t_{FC}	Clock Fall Time		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	15		ns
t_{CHDX}	t_{DH}	Data In Hold Time	15		ns
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	15		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	20		ns
t_{CLHL}		Clock Low Set-up Time before $\overline{HOLD}$ Active	0		ns
t_{CLHH}		Clock Low Set-up Time before $\overline{HOLD}$ not Active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output Disable Time		25	ns
t_{CLQV}	t_V	Clock Low to Output Valid		25	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		ns
t_{QLQH}(2)	t_{RO}	Output Rise Time		20	ns
t_{QHQL}(2)	t_{FO}	Output Fall Time		20	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ High to Output Valid		25	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		25	ns
t_W	t_{WC}	Write Time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Value guaranteed by characterization, not 100% tested in production.

Table 19. AC characteristics (M95320 and M95640, device grade 3)

Test conditions specified in *Table 11* and *Table 8*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock Frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		ns
t_{CH}(1)	t_{CLH}	Clock High Time	90		ns
t_{CL}(1)	t_{CLL}	Clock Low Time	90		ns
t_{CLCH}(2)	t_{RC}	Clock Rise Time		1	µs
t_{CHCL}(2)	t_{FC}	Clock Fall Time		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		ns
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	70		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	40		ns
t_{CLHL}		Clock Low Set-up Time before $\overline{HOLD}$ Active	0		ns
t_{CLHH}		Clock Low Set-up Time before $\overline{HOLD}$ not Active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output Disable Time		100	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		ns
t_{QLQH}(2)	t_{RO}	Output Rise Time		50	ns
t_{QHQL}(2)	t_{FO}	Output Fall Time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ High to Output Valid		50	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100	ns
t_W	t_{WC}	Write Time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Value guaranteed by characterization, not 100% tested in production.

Table 20. AC characteristics (M95320-W and M95640-W, device grade 6)

Test conditions specified in *Table 11* and *Table 9*							
Symbol	**Alt.**	**Parameter**	**Current Product Version(1)**		**New Product Version(2)**		**Unit**
			Min.	**Max.**	**Min.**	**Max.**	
f_C	f_{SCK}	Clock Frequency	D.C.	5	D.C.	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	90		30		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	90		30		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		40		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		30		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		30		ns
t_{CH}(3)	t_{CLH}	Clock High Time	90		42		ns
t_{CL}(3)	t_{CLL}	Clock Low Time	90		40		ns
t_{CLCH}(4)	t_{RC}	Clock Rise Time		1		2	µs
t_{CHCL}(4)	t_{FC}	Clock Fall Time		1		2	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		10		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		10		ns
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	70		30		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	40		30		ns
t_{CLHL}		Clock Low Set-up Time before $\overline{HOLD}$ Active	0		0		ns
t_{CLHH}		Clock Low Set-up Time before $\overline{HOLD}$ not Active	0		0		ns
t_{SHQZ}(4)	t_{DIS}	Output Disable Time		100		40	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60		40	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH}(4)	t_{RO}	Output Rise Time		50		40	ns
t_{QHQL}(4)	t_{FO}	Output Fall Time		50		40	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ High to Output Valid		50		40	ns
t_{HLQZ}(4)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100		40	ns
t_W	t_{WC}	Write Time		5		5	ms

1. Current product version is identified by Process Identification letter ‘V’.
2. New product version is identified by Process Identification letter ‘P’. Please contact your nearest ST sales office for details (PCN MPG-NVM/05/1315 and PCN MPG-NVM/05/1191)
3. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
4. Value guaranteed by characterization, not 100% tested in production.

Table 21. AC characteristics (M95320-W and M95640-W, device grade 3)

Test conditions specified in *Table 11* and *Table 9*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock Frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		ns
t_{CH}(1)	t_{CLH}	Clock High Time	90		ns
t_{CL}(1)	t_{CLL}	Clock Low Time	90		ns
t_{CLCH}(2)	t_{RC}	Clock Rise Time		1	µs
t_{CHCL}(2)	t_{FC}	Clock Fall Time		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		ns
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	70		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	40		ns
t_{CLHL}		Clock Low Set-up Time before $\overline{HOLD}$ Active	0		ns
t_{CLHH}		Clock Low Set-up Time before $\overline{HOLD}$ not Active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output Disable Time		100	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		ns
t_{QLQH}(2)	t_{RO}	Output Rise Time		50	ns
t_{QHQL}(2)	t_{FO}	Output Fall Time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ High to Output Valid		50	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100	ns
t_W	t_{WC}	Write Time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Value guaranteed by characterization, not 100% tested in production.

Table 22. AC characteristics (M95320-R)

Test conditions specified in *Table 11* and *Table 10*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock Frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	60		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	60		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	90		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	60		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	60		ns
t_{CH}(1)	t_{CLH}	Clock High Time	90		ns
t_{CL}(1)	t_{CLL}	Clock Low Time	90		ns
t_{CLCH}(2)	t_{RC}	Clock Rise Time		2	µs
t_{CHCL}(2)	t_{FC}	Clock Fall Time		2	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		ns
t_{CHDX}	t_{DH}	Data In Hold Time	20		ns
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	60		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	60		ns
t_{CLHL}		Clock Low Set-up Time before $\overline{HOLD}$ Active	0		0
t_{CLHH}		Clock Low Set-up Time before $\overline{HOLD}$ not Active	0		0
t_{SHQZ}(2)	t_{DIS}	Output Disable Time		80	ns
t_{CLQV}	t_V	Clock Low to Output Valid		80	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		ns
t_{QLQH}(2)	t_{RO}	Output Rise Time		80	ns
t_{QHQL}(2)	t_{FO}	Output Fall Time		80	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ High to Output Valid		80	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		80	ns
t_W	t_{WC}	Write Time		10	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Value guaranteed by characterization, not 100% tested in production.

Table 23. AC characteristics (M95640-R)

Test conditions specified in *Table 11* and *Table 9*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock Frequency	D.C.	2	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	150		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	150		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	200		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	150		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	150		ns
t_{CH}(1)	t_{CLH}	Clock High Time	200		ns
t_{CL}(3)	t_{CLL}	Clock Low Time	200		ns
t_{CLCH}(2)	t_{RC}	Clock Rise Time		2	µs
t_{CHCL}(4)	t_{FC}	Clock Fall Time		2	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	50		ns
t_{CHDX}	t_{DH}	Data In Hold Time	50		ns
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	150		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	150		ns
t_{CLHL}		Clock Low Set-up Time before $\overline{HOLD}$ Active	0		0
t_{CLHH}		Clock Low Set-up Time before $\overline{HOLD}$ not Active	0		0
t_{SHQZ}(4)	t_{DIS}	Output Disable Time		200	ns
t_{CLQV}	t_V	Clock Low to Output Valid		200	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		ns
t_{QLQH}(4)	t_{RO}	Output Rise Time		200	ns
t_{QHQL}(4)	t_{FO}	Output Fall Time		200	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ High to Output Valid		200	ns
t_{HLQZ}(4)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		200	ns
t_W	t_{WC}	Write Time		10	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Value guaranteed by characterization, not 100% tested in production.

Figure 15. Serial Input timing

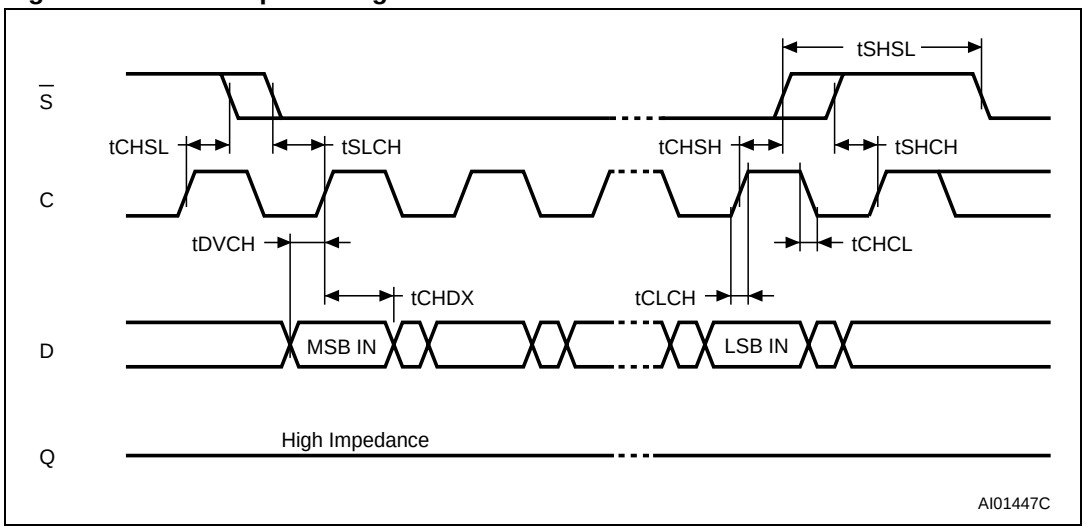


Figure 16. Hold timing

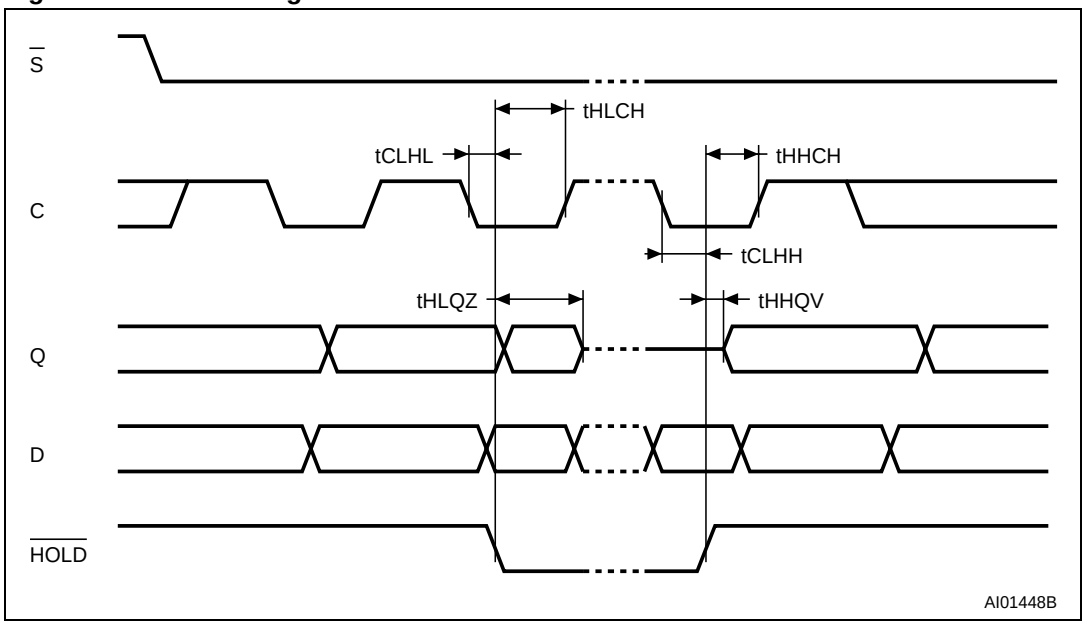
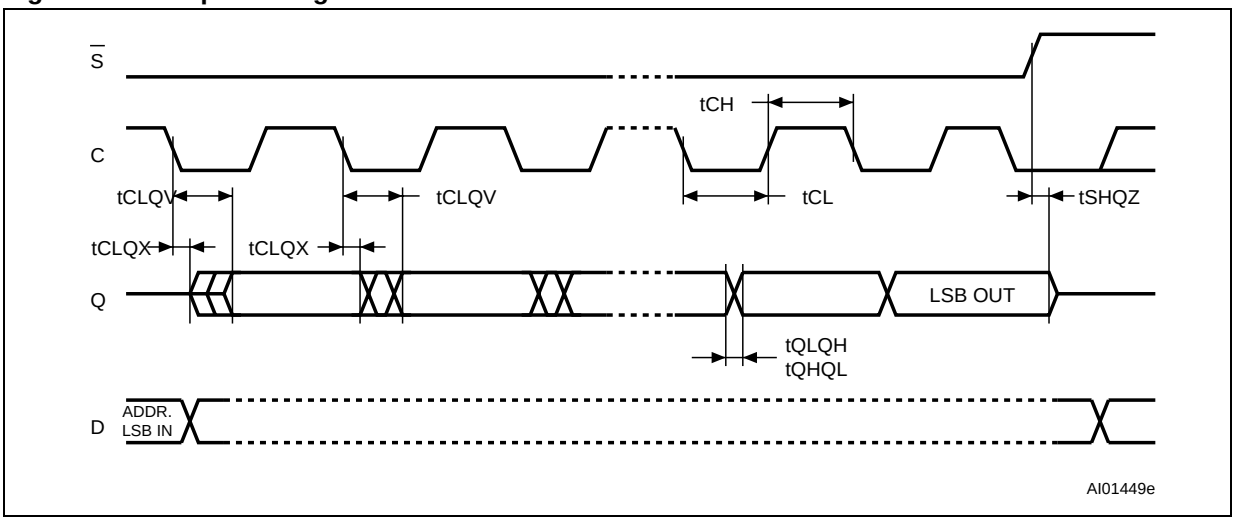
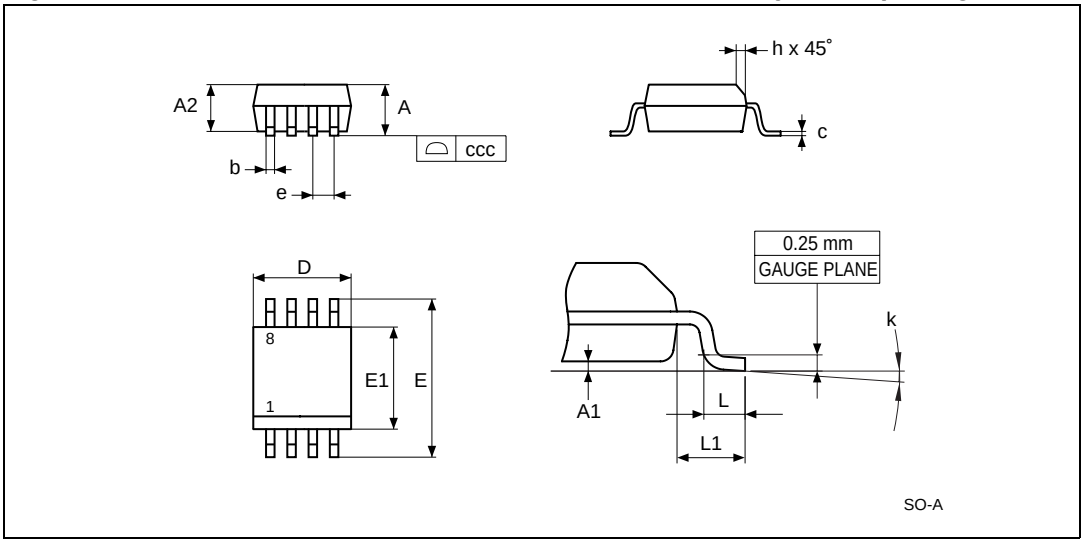


Figure 17. Output timing



10 Package mechanical

Figure 18. SO8N – 8 lead Plastic Small Outline, 150 mils body width, package outline

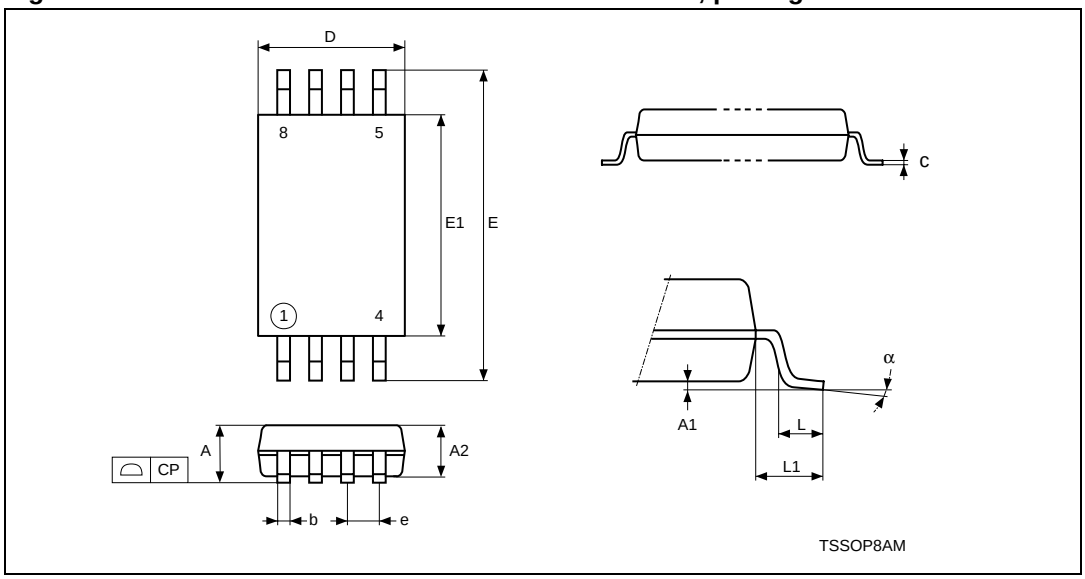


1. Drawing is not to scale.

Table 24. SO8N – 8 lead Plastic Small Outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2		1.25			0.049	
b		0.28	0.48		0.011	0.019
c		0.17	0.23		0.007	0.009
ccc			0.10			0.004
D	4.90	4.80	5.00	0.193	0.189	0.197
E	6.00	5.80	6.20	0.236	0.228	0.244
E1	3.90	3.80	4.00	0.154	0.150	0.157
e	1.27	–	–	0.050	–	–
h		0.25	0.50		0.010	0.020
k		0°	8°		0°	8°
L		0.40	1.27		0.016	0.050
L1	1.04			0.041		

Figure 19. TSSOP8 – 8 lead Thin Shrink Small Outline, package outline

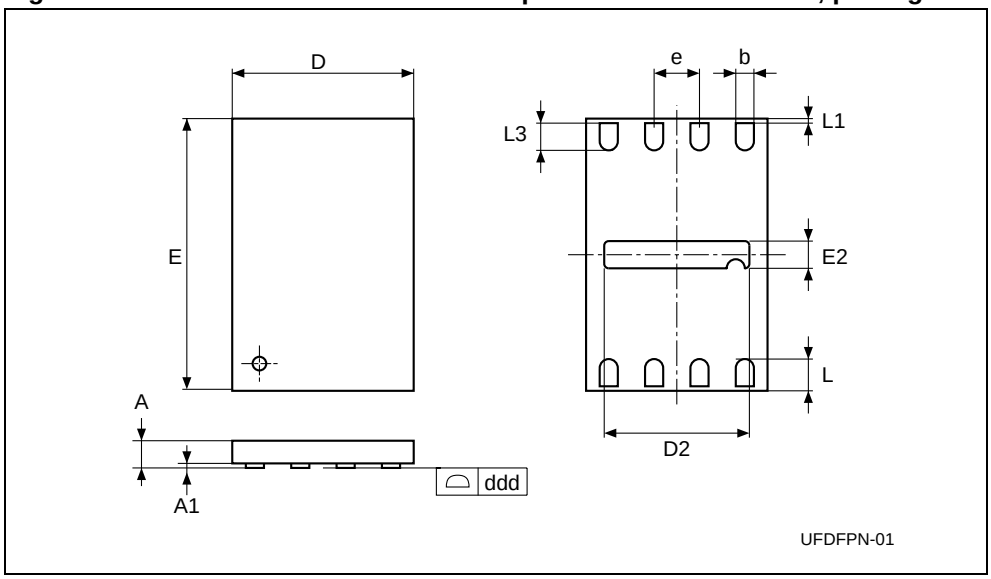


1. Drawing is not to scale.

Table 25. TSSOP8 – 8 lead Thin Shrink Small Outline, package mechanical data

Symbol	millimeters			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

Figure 20. MLP8 - 8-lead Ultra thin Fine pitch Dual Flat No Lead, package outline



1. Drawing is not to scale.

Table 26. MLP8 - 8-lead Ultra thin Fine pitch Dual Flat No Lead, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.55	0.50	0.60	0.022	0.020	0.024
A1		0.00	0.05		0.000	0.002
b	0.25	0.20	0.30	0.010	0.008	0.012
D	2.00			0.079		
D2		1.55	1.65		0.061	0.065
ddd			0.05			0.002
E	3.00			0.118		
E2		0.15	0.25		0.006	0.010
e	0.50	–	–	0.020	–	–
L	0.45	0.40	0.50	0.018	0.016	0.020
L1			0.15			0.006
L3		0.30			0.012	
N	8			8		

11 Part numbering

Table 27. Ordering information scheme

Example: M95640 – W MN 6 T P /B

Device Type

M95 = SPI serial access EEPROM

Device Function

640 = 64 Kbit (8192 x 8)

320 = 32 Kbit (4096 x 8)

Operating Voltage

blank = V_{CC} = 4.5 to 5.5V

W = V_{CC} = 2.5 to 5.5V

R = V_{CC} = 1.8 to 5.5V

Package

MN = SO8 (150 mil width)

DW = TSSOP8 (169 mil width)

MB = MLP8 (2x3 mm)

Device Grade

6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow

3 = Device tested with High Reliability Certified Flow[1] Automotive temperature range (–40 to 125 °C)

Option

blank = Standard Packing

T = Tape and Reel Packing

Plating Technology

blank = Standard SnPb plating

P or G = ECOPACK (RoHS compliant)

Process letter[2]

/B = DP26% Rsst

/P = DP26% Chartered

1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The High Reliability Certified Flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
2. The Process letter only concerns Grade-3 devices.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

The category of second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

12 Revision history

Table 28. Document revision history

Date	Revision	Changes
13-Jul-2000	1.2	Human Body Model meets JEDEC std (Table 2). Minor adjustments on pp 1,11,15. New clause on p7. Addition of TSSOP8 package on pp 1, 2, Ordering Info, Mechanical Data
16-Mar-2001	1.3	Test condition added I_{LI} and I_{LO}, and specification of t_{DLDH} and t_{DHDL} removed. t_{CLCH}, t_{CHCL}, t_{DLDH} and t_{DHDL} changed to 50ns for the -V range. “-V” Voltage range changed to “2.7V to 3.6V” throughout. Maximum lead soldering time and temperature conditions updated. Instruction sequence illustrations updated. “Bus Master and Memory Devices on the SPI bus” illustration updated. Package Mechanical data updated
19-Jul-2001	1.4	M95160 and M95080 devices removed to their own data sheet
06-Dec-2001	1.5	Endurance increased to 1M write/erase cycles Instruction sequence illustrations updated
18-Dec-2001	2.0	Document reformatted using the new template. No parameters changed.
08-Feb-2002	2.1	Announcement made of planned upgrade to 10MHz clock for the 5V, –40 to 85°C, range. Endurance set to 100K write/erase cycles
18-Dec-2002	2.2	10MHz, 5MHz, 2MHz clock; 5ms, 10ms Write Time; 100K, 1M erase/write cycles distinguished on front page, and in the DC and AC Characteristics tables
26-Mar-2003	2.3	Process indentification letter corrected in footnote to AC Characteristics table for temp. range 3
26-Jun-2003	2.4	-S voltage range upgraded by removing it and inserting -R voltage range in its place
15-Oct-2003	3.0	Table of contents, and Pb-free options added. V_{IL}(min) improved to -0.45V
21-Nov-2003	3.1	V_I(min) and V_O(min) corrected (improved) to -0.45V
28-Jan-2004	4.0	TSSOP8 connections added to DIP and SO connections

Table 28. Document revision history (continued)

Date	Revision	Changes
24-May-2005	5.0	M95320-S and M95640-S root part numbers (1.65 to 5.5V Supply) and related characteristics added. 20MHz Clock rate added.TSSOP14 package removed and MLP8 package added. Description of *Power On Reset: VCC Lock-Out Write Protect* updated. Product List summary table added. Absolute Maximum Ratings for V_{IO}(min) and V_{CC}(min) improved. Soldering temperature information clarified for RoHS compliant devices. Device Grade 3 clarified, with reference to HRCF and automotive environments. AEC-Q100-002 compliance. t_{CHHL}(min) and t_{CHHH}(min) is t_{CH} for products under “S” process. t_{HHQX} corrected to t_{HHQV}. *Figure 16: Hold timing* updated.
07-Jul-2006	6	Document converted to new ST template. Packages are ECOPACK® compliant. PDIP package removed. SO8N package specifications updated (see *Table 24* and *Figure 18*). M95640-S and M95320-S part numbers removed (*DC and AC parameters* updated accordingly). *How to identify previous, current and new products by the Process identification letter* Table removed. *Figure 4: SPI modes supported* updated and *Note 2* added. First three paragraphs of *Section 4: Operating features* replaced by *Section 4.1: Supply voltage (V_{CC})*. T_A added to *Table 7: Absolute maximum ratings*. I_{CC} and I_{CC1} updated in *Table 13*, *Table 14*, *Table 15* and *Table 17*. V_{OL} and V_{OH} updated in *Table 15*. I_{CC} updated in *Table 16*. Data in *Table 17* is no longer preliminary. t_{CH} updated in *Table 20*. *Table 23: AC characteristics (M95640-R)* added. Timing line of t_{SHQZ} modified in *Figure 17: Output timing*. *Process letter* added to *Table 27: Ordering information scheme*, Note 2 removed. Note 2 removed from *Figure 2*.

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