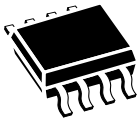
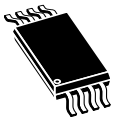
M95256-DRE

256-Kbit serial SPI bus EEPROM - 105 °C Operation

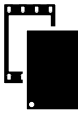
Datasheet - production data



SO8 (MN)
150 mil width



TSSOP8 (DW)
169 mil width



WFDFPN8 (MF)
2 x 3 mm

Features

- Compatible with the Serial Peripheral Interface (SPI) bus
- Memory array
  - 256 Kbit (32 Kbytes) of EEPROM
  - Page size: 64 bytes
  - Write protection by block: 1/4, 1/2 or whole memory
  - Additional Write lockable Page (Identification page)
- Extended temperature and voltage range
  - Up to 105 °C (V_{CC} from 1.8 V to 5.5 V)
- High speed clock frequency
  - 20 MHz for $V_{CC} \geq 4.5$ V
  - 10 MHz for $V_{CC} \geq 2.5$ V
  - 5 MHz for $V_{CC} \geq 1.8$ V
- Schmitt trigger inputs for noise filtering
- Short Write cycle time
  - Byte Write within 4 ms
  - Page Write within 4 ms
- Write cycle endurance
  - 4 million Write cycles at 25 °C
  - 1.2 million Write cycles at 85 °C
  - 900 k Write cycles at 105 °C
- Data retention
  - more than 50 years at 105 °C
  - 200 years at 55 °C
- ESD Protection (Human Body Model)
  - 4000 V
- Packages
  - RoHS-compliant and halogen-free (ECOPACK2®)

This is information on a product in full production. www.st.com

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1 Description

The M95256-DRE is a 256-Kbit serial EEPROM device operating up to 105 °C. The M95256-DRE is compliant with the level of reliability defined by the AEC-Q100 grade 2.

The device is accessed by a simple serial SPI compatible interface running up to 20 MHz.

The memory array is based on advanced true EEPROM technology (Electrically Erasable PROgrammable Memory). The M95256-DRE is a byte-alterable memory (32768 × 8 bits) organized as 512 pages of 64 bytes in which the data integrity is significantly improved with an embedded Error Correction Code logic.

The M95256-DRE offers an additional Identification Page (64 bytes) in which the ST device identification can be read. This page can also be used to store sensitive application parameters which can be later permanently locked in read-only mode.

Figure 1. Logic diagram

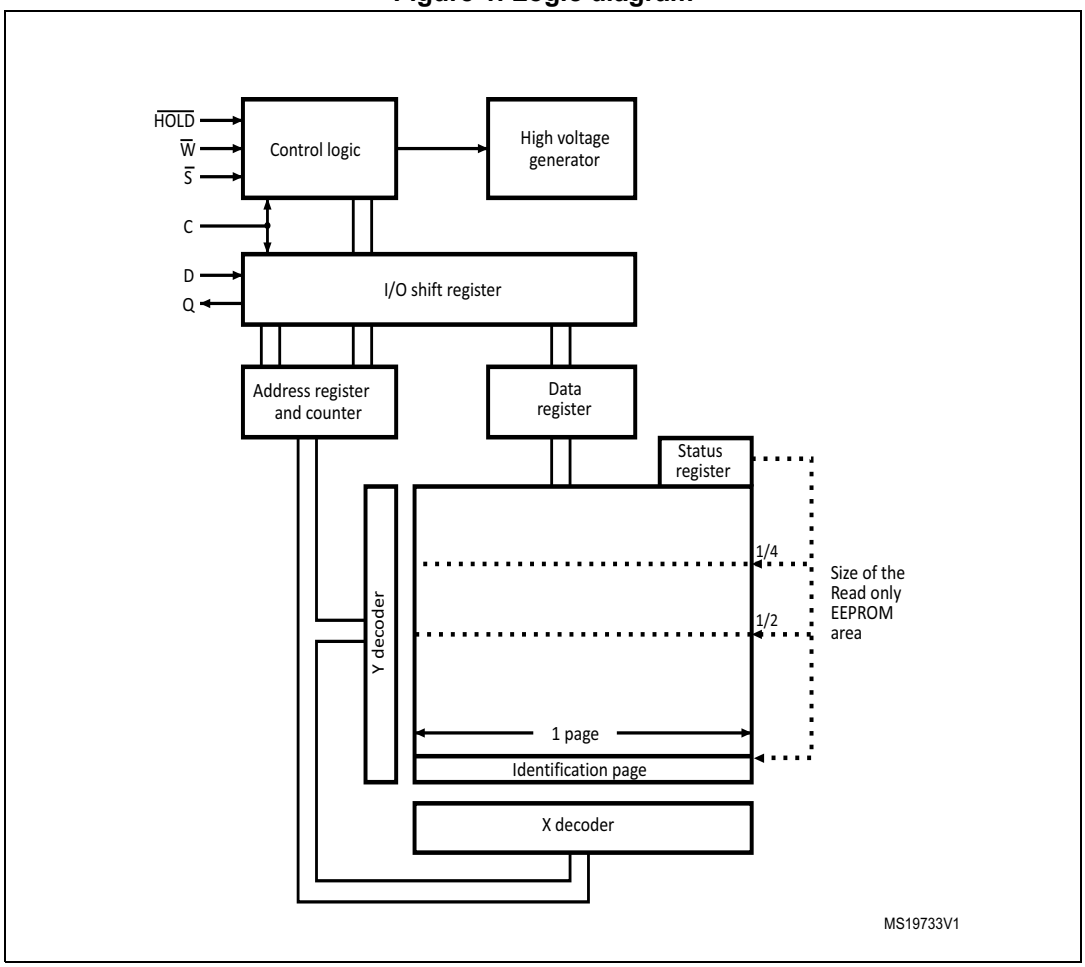
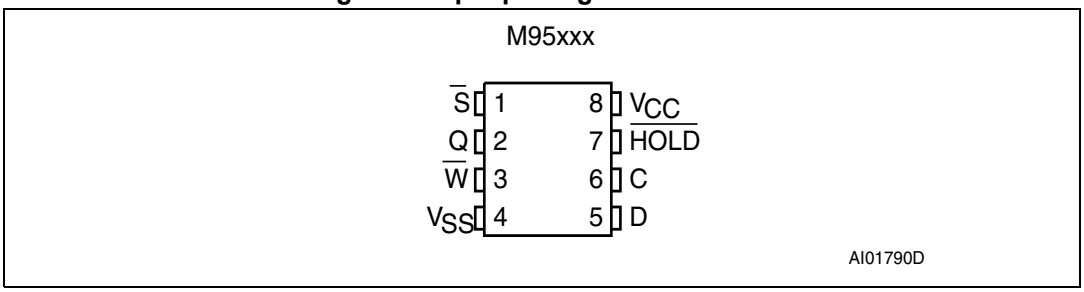


Figure 2. 8-pin package connections



1. See *Package mechanical data* section for package dimensions and how to identify pin-1.

Table 1. Signal names

Signal name	Description
C	Serial Clock
D	Serial data input
Q	Serial data output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply voltage
V_{SS}	Ground

2 Signal description

All input signals must be held high or low (according to voltages of V_{IH} or V_{IL}, as specified in *Table 12*). These signals are described below.

2.1 Serial Data output (Q)

This output signal is used to transfer data serially out of the device during a Read operation. Data is shifted out on the falling edge of Serial Clock (C), most significant bit (MSB) first. In all other cases, the Serial Data output is in high impedance.

2.2 Serial Data input (D)

This input signal is used to transfer data serially into the device. D input receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C), most significant bit (MSB) first.

2.3 Serial Clock (C)

This input signal allows to synchronize the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

Driving Chip Select ($\overline{S}$) low selects the device in order to start communication. Driving Chip Select ($\overline{S}$) high deselects the device and Serial Data output (Q) enters the high impedance state.

2.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

2.6 Write Protect ($\overline{W}$)

This pin is used to write-protect the Status Register.

2.7 V_{SS} ground

V_{SS} is the reference for all signals, including the V_{CC} supply voltage.

2.8 V_{CC} supply voltage

V_{CC} is the supply voltage pin. Refer to *Section 3.1: Active power and Standby power modes* and to *Section 5.1: Supply voltage (V_{CC})*.

3 Operating features

3.1 Active power and Standby power modes

When Chip Select ($\overline{S}$) is low, the device is selected and in the Active power mode.

When Chip Select ($\overline{S}$) is high, the device is deselected. If a Write cycle is not currently in progress, the device then goes in to the Standby power mode, and the device consumption drops to I_{CC1}, as specified in *Table 12*.

3.2 SPI modes

The device can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

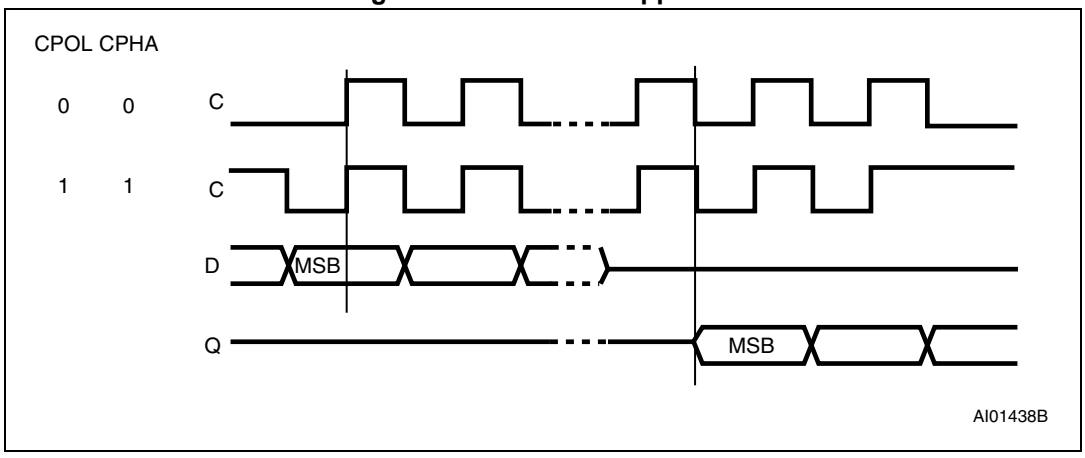
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 3*, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 3. SPI modes supported

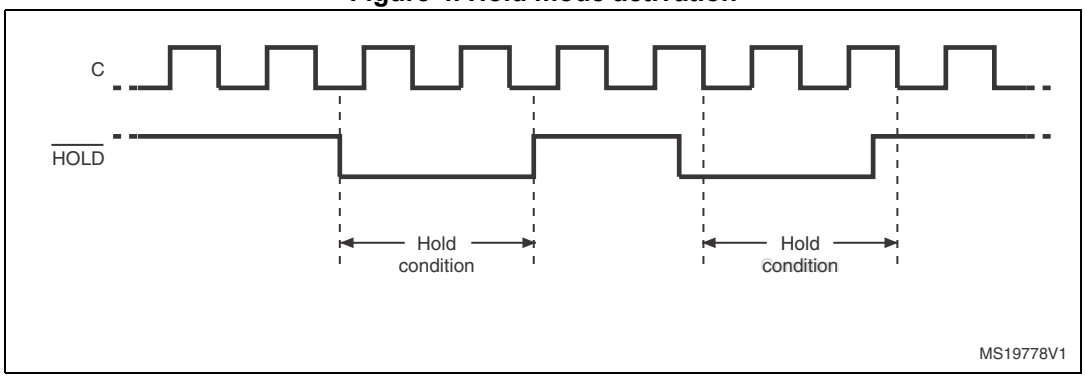


3.3 Hold mode

The Hold ($\overline{\text{HOLD}}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

The Hold mode starts when the Hold ($\overline{\text{HOLD}}$) signal is driven low and the Serial Clock (C) is low (as shown in *Figure 4*). During the Hold mode, the Serial Data output (Q) is high impedance, and the signals present on Serial Data input (D) and Serial Clock (C) are not decoded. The Hold mode ends when the Hold ($\overline{\text{HOLD}}$) signal is driven high and the Serial Clock (C) is or becomes low.

Figure 4. Hold mode activation



Deselecting the device while it is in Hold mode resets the paused communication.

3.4 Protocol control and data protection

3.4.1 Protocol control

The Chip Select ($\overline{\text{S}}$) input offers a built-in safety feature, as the $\overline{\text{S}}$ input is edge-sensitive as well as level-sensitive: after power-up, the device is not selected until a falling edge has first been detected on Chip Select ($\overline{\text{S}}$). This ensures that Chip Select ($\overline{\text{S}}$) must have been high prior to going low, in order to start the first operation.

For Write commands (WRITE, WRSR, WRID, LID) to be accepted and executed:

- the Write Enable Latch (WEL) bit must be set by a Write Enable (WREN) instruction
- a falling edge and a low state on Chip Select ($\overline{\text{S}}$) during the whole command must be decoded
- instruction, address and input data must be sent as multiple of eight bits
- the command must include at least one data byte
- Chip Select ($\overline{\text{S}}$) must be driven high exactly after a data byte boundary

Write command can be discarded at any time by a rising edge on Chip Select ($\overline{\text{S}}$) outside of a byte boundary.

To execute Read commands (READ, RDSR, RDID, RDLS), the device must decode:

- a falling edge and a low level on Chip Select ($\overline{\text{S}}$) during the whole command
- instruction and address as multiples of eight bits (bytes)

From this step, data bits are shifted out until the rising edge on Chip Select ($\overline{\text{S}}$).

3.4.2 Status Register and data protection

The Status Register format is shown in *Table 2* and the status and control bits of the Status Register are as follows:

Table 2. Status Register format

b7	b6	b5	b4	b3	b2	b1	b0
SRWD	0	0	0	BP1	BP0	WEL	WIP

Status Register Write Protect

Block Protect bits

Write Enable Latch bit

Write In Progress bit

Note: Bits b6, b5, b4 are always read as 0.

WIP bit

The WIP bit (Write In Progress) is a read-only flag that indicates the Ready/Busy state of the device. When a Write command (WRITE, WRSR, WRID, LID) has been decoded and a Write cycle (t_W) is in progress, the device is busy and the WIP bit is set to 1. When WIP=0, the device is ready to decode a new command.

During a Write cycle, reading continuously the WIP bit allows to detect when the device becomes ready (WIP=0) to decode a new command.

WEL bit

The WEL bit (Write Enable Latch) bit is a flag that indicates the status of the internal Write Enable Latch. When WEL is set to 1, the Write instructions (WRITE, WRSR, WRID, LID) are executed; when WEL is set to 0, any decoded Write instruction is not executed.

The WEL bit is set to 1 with the WREN instruction. The WEL bit is reset to 0 after the following events:

- Write Disable (WRDI) instruction completion
- Write instructions (WRITE, WRSR, WRID, LID) completion including the write cycle time t_W
- Power-up

BP1, BP0 bits

The Block Protect bits (BP1, BP0) are non-volatile. BP1,BP0 bits define the size of the memory block to be protected against write instructions, as defined in *Table 2*. These bits are written with the Write Status Register (WRSR) instruction, provided that the Status Register is not protected (refer to "*SRWD bit and W input signal*", *on page 13*).

Table 3. Write-protected block size

Status Register bits		Protected block	Protected array addresses
BP1	BP0		
0	0	None	None
0	1	Upper quarter	6000h-7FFFh
1	0	Upper half	4000h-7FFFh
1	1	Whole memory	0000h - 7FFFh plus Identification page

SRWD bit and $\overline{W}$ input signal

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect pin ($\overline{W}$) signal. When the SRWD bit is written to 0, it is possible to write the Status Register, regardless of whether the pin Write Protect ($\overline{W}$) is driven high or low.

When the SRWD bit is written to 1, two cases have to be considered, depending on the state of the $\overline{W}$ input pin:

- Case 1: if pin $\overline{W}$ is driven high, it is possible to write the Status Register.
- Case 2: if pin $\overline{W}$ is driven low, it is not possible to write the Status Register (WRSR is discarded) and therefore SRWD,BP1,BP0 bits cannot be changed (the size of the protected memory block defined by BP1,BP0 bits is frozen).

Case 2 can be entered in either sequence:

- Writing SRWD bit to 1 after driving pin $\overline{W}$ low, or
- Driving pin $\overline{W}$ low after writing SRWD bit to 1.

The only way to exit Case 2 is to pull pin $\overline{W}$ high.

Note: if pin $\overline{W}$ is permanently tied high, the Status Register cannot be write-protected.

The protection features of the device are summarized in *Table 4*.

Table 4. Protection modes

SRWD bit	$\overline{W}$ signal	Status
0	X	Status Register is writable.
1	1	
1	0	Status Register is write-protected.

3.5 Identification page

The M95256-DRE offers an Identification page (64 bytes) in addition to the 256 Kbit memory. The Identification page contains two fields:

- Device identification: the three first bytes are programmed by STMicroelectronics with the Device identification code, as shown in *Table 5*.
- Application parameters: the bytes after the Device identification code are available for application specific data.

Note: If the end application does not need to read the Device identification code, this field can be overwritten and used to store application-specific data. Once the application-specific data are written in the Identification page, the whole Identification page should be permanently locked in Read-only mode.

The Read, Write, Lock Identification Page instructions are detailed in *Section 4: Instructions*.

Table 5. Device identification bytes

Address in Identification page	Content	Value
00h	ST Manufacturer code	20h
01h	SPI Family code	00h
02h	Memory Density code	0Fh (256 Kbit)

4 Instructions

Each command is composed of bytes (MSBit transmitted first), initiated with the instruction byte, as summarized in *Table 6*.

If an invalid instruction is sent (one not contained in *Table 6*), the device automatically enters a Wait state until deselected.

Table 6. Instruction set

Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010
RDID	Read Identification Page	1000 0011
WRID	Write Identification Page	1000 0010
RDLS	Reads the Identification Page lock status.	1000 0011
LID	Locks the Identification page in read-only mode.	1000 0010

For read and write commands to memory array and Identification Page, the address is defined by two bytes as explained in *Table 7*.

Table 7. Significant bits within the two address bytes(1)(2)

Instructions	MSB Address byte								LSB Address byte							
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
READ or WRITE	x	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RDID or WRID	0	0	0	0	0	0	0	0	0	0	A5	A4	A3	A2	A1	A0
RDLS or LID	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

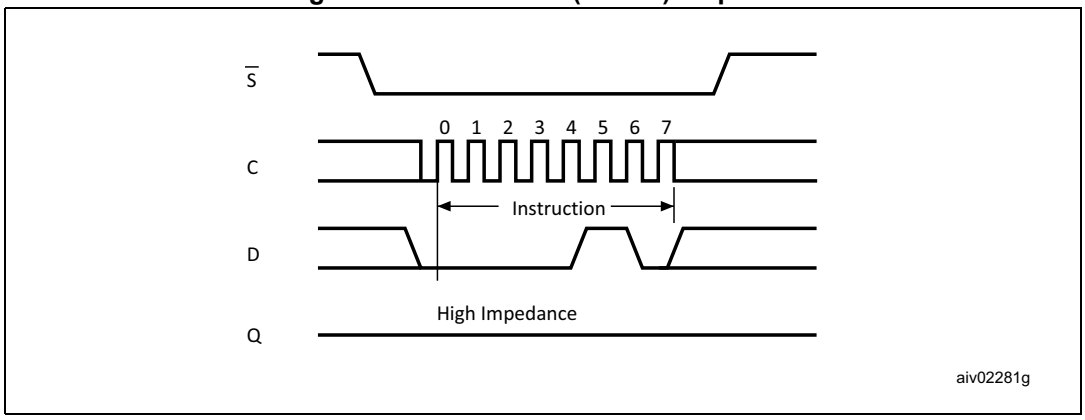
1. A: Significant address bit.
2. x: bit is Don't Care.

4.1 Write Enable (WREN)

The WREN instruction must be decoded by the device before a write instruction (WRITE, WRSR, WRID or LID).

As shown in *Figure 5*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, the bits of the instruction byte are shifted in (MSB first) on Serial Data Input (D) after what the Chip Select ($\overline{S}$) input is driven high and the WEL bit is set (Status Register bit).

Figure 5. Write Enable (WREN) sequence



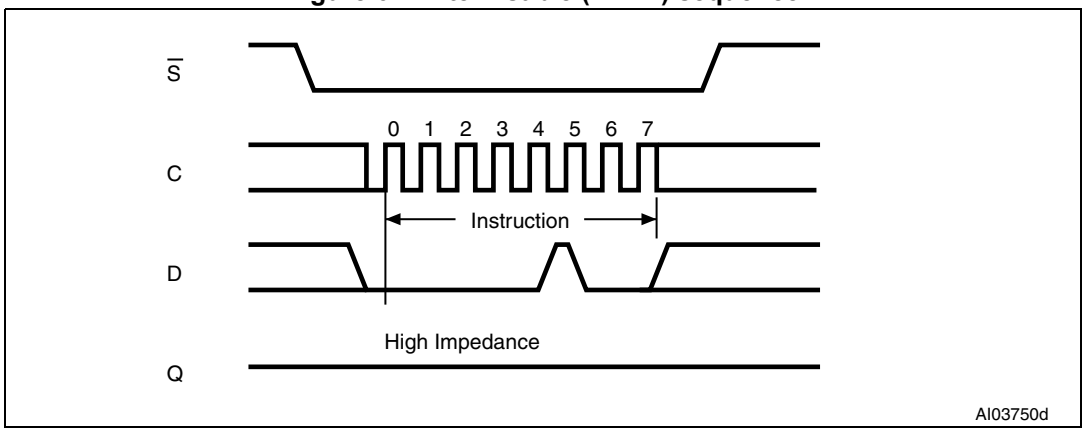
4.2 Write Disable (WRDI)

One way of resetting the WEL bit (in the Status Register) is to send a Write Disable instruction to the device.

As shown in *Figure 6*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in (MSB first), on Serial Data Input (D), after what the Chip Select ($\overline{S}$) input is driven high and the WEL bit is reset (Status Register bit).

If a Write cycle is currently in progress, the WRDI instruction is decoded and executed and the WEL bit is reset to 0 with no effect on the ongoing Write cycle.

Figure 6. Write Disable (WRDI) sequence



4.3 Read Status Register (RDSR)

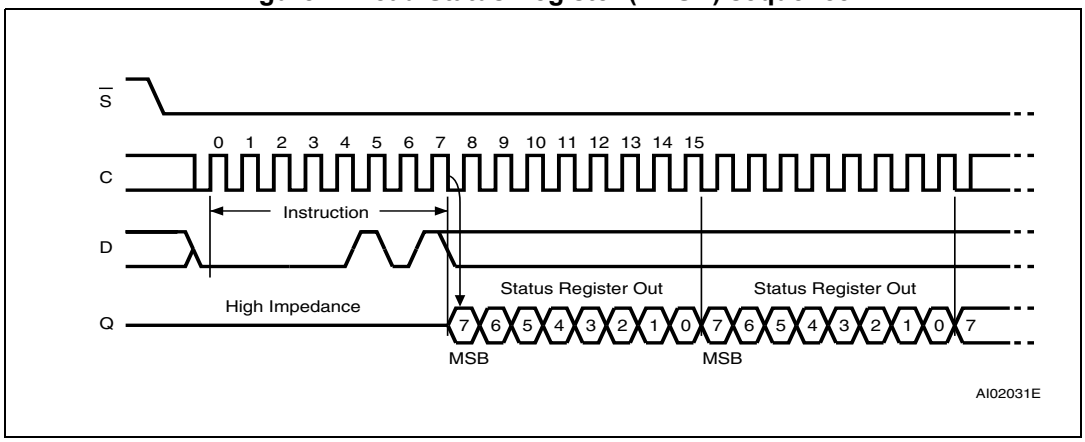
The Read Status Register (RDSR) instruction is used to read the content of the Status Register.

As shown in *Figure 7*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte are shifted in (MSB first) on Serial Data Input (D), the Status Register content is then shifted out (MSB first) on Serial Data Output (Q).

If Chip Select ($\overline{S}$) continues to be driven low, the Status Register content is continuously shifted out.

The Status Register can always be read, even if a Write cycle (t_W) is in progress. The Status Register functionality is detailed in *Section 3.4.2: Status Register and data protection*.

Figure 7. Read Status Register (RDSR) sequence



4.4 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed.

The Write Status Register (WRSR) instruction is entered (MSB first) by driving Chip Select ($\overline{S}$) low, sending the instruction code followed by the data byte on Serial Data input (D), and driving the Chip Select ($\overline{S}$) signal high.

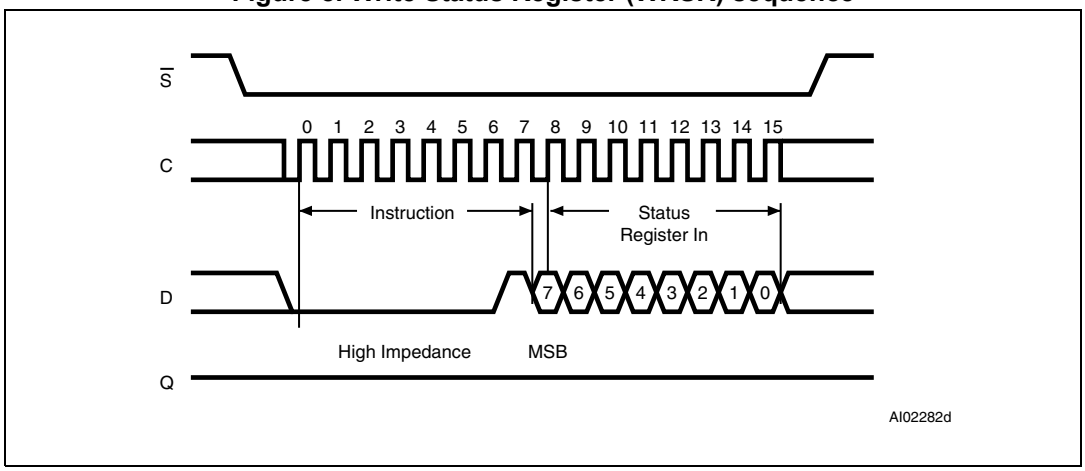
The contents of the SRWD and BP1, BP0 bits are updated after the completion of the WRSR instruction, including the Write cycle (t_W).

The Write Status Register (WRSR) instruction has no effect on the b6, b5, b4, b1 and b0 bits in the Status Register (see *Table 2: Status Register format*).

The Status Register functionality is detailed in *Section 3.4.2: Status Register and data protection*.

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Figure 8. Write Status Register (WRSR) sequence



4.5 Read from Memory Array (READ)

The READ instruction is used to read the content of the memory.

As shown in *Figure 9*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low.

The bits of the instruction byte and address bytes are shifted in (MSB first) on Serial Data Input (D) and the addressed data byte is then shifted out (MSB first) on Serial Data Output (Q). The first addressed byte can be any byte within any page.

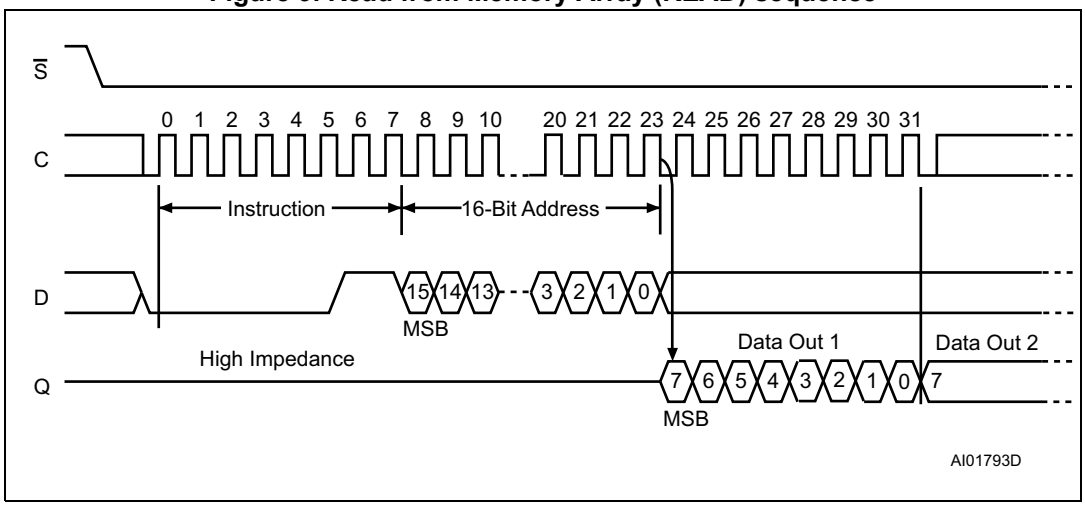
If Chip Select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented, and the next byte of data is shifted out. The whole memory can therefore be read with a single READ instruction.

When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) high at any time when the data bits are shifted out on Serial Data Output (Q).

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Figure 9. Read from Memory Array (READ) sequence



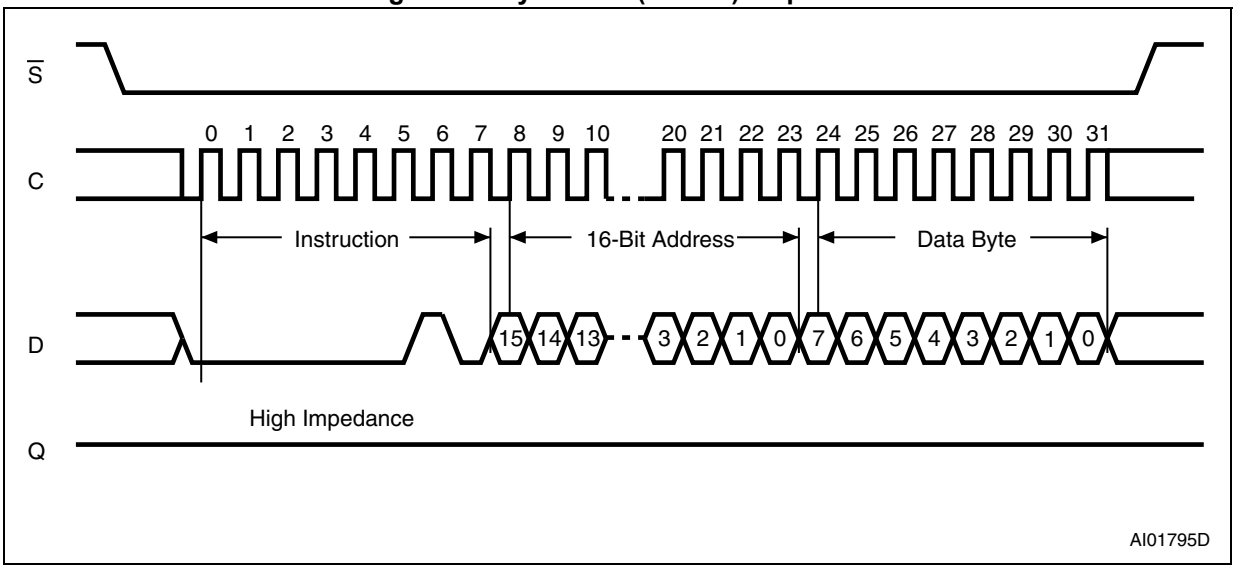
1. Depending on the memory size, as shown in *Table 7*, the most significant address bits are Don't Care.

4.6 Write to Memory Array (WRITE)

The WRITE instruction is used to write new data in the memory.

As shown in *Figure 10*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte, address bytes, and at least one data byte are then shifted in (MSB first), on Serial Data Input (D). The instruction is terminated by driving Chip Select ($\overline{S}$) high at a data byte boundary. *Figure 10* shows a single byte write.

Figure 10. Byte Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 7*, the most significant address bits are Don't Care.

A Page write is used to write several bytes inside a page, with a single internal Write cycle.

For a Page write, Chip Select ($\overline{S}$) has to remain low, as shown in *Figure 11*, so that the next data bytes are shifted in. Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the address counter exceeds the page boundary (the page size is 64 bytes), the internal address pointer rolls over to the beginning of the same page where next data bytes will be written. If more than 64 bytes are received, only the last 64 bytes are written.

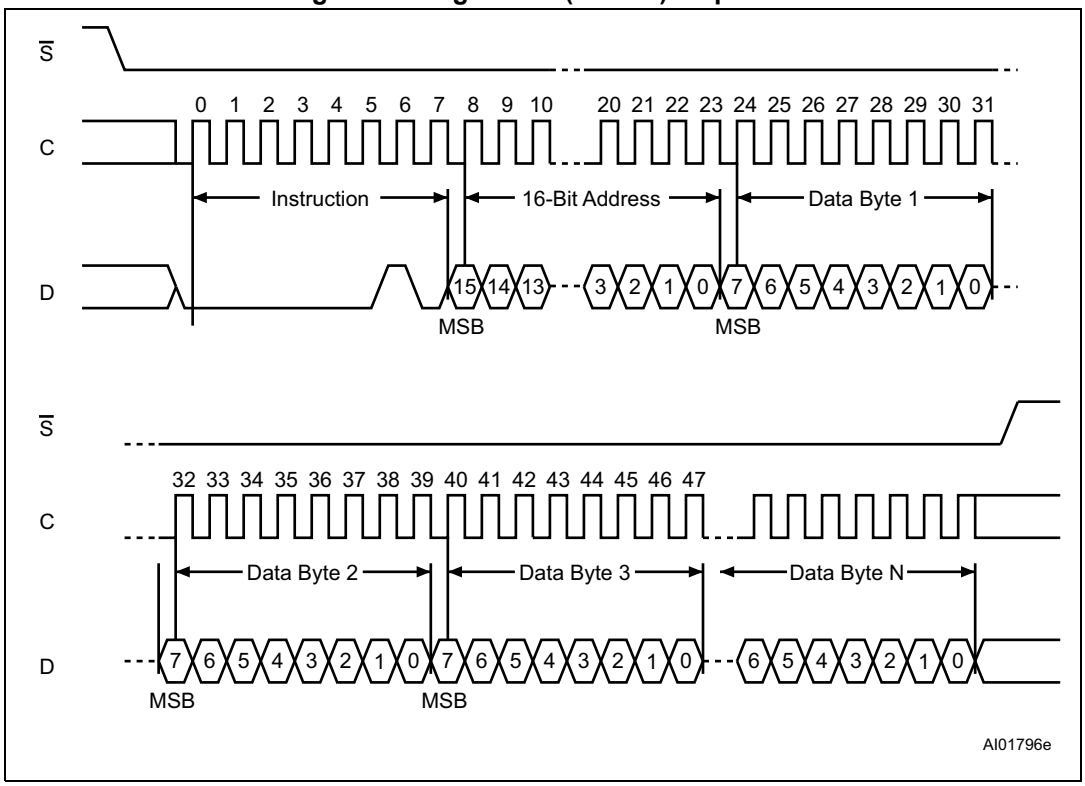
For both Byte write and Page write, the self-timed Write cycle starts from the rising edge of Chip Select ($\overline{S}$), and continues for a period t_W (as specified in *Table 13*).

The instruction is discarded, and is not executed, under the following conditions:

- if a Write cycle is already in progress
- if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits
- if one of the conditions defined in *Section 3.4.1* is not satisfied

Note: The self-timed Write cycle t_W is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)]. An erased bit is read as "0" and a programmed bit is read as "1".

Figure 11. Page Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 7*, the most significant address bits are Don't Care.

4.7 Read Identification Page (RDID)

The Read Identification Page instruction is used to read the Identification Page (additional page of 64 bytes which can be written and later permanently locked in Read-only mode).

The Chip Select ($\overline{S}$) signal is first driven low, the bits of the instruction byte and address bytes are then shifted in (MSB first) on Serial Data input (D). Address bit A10 must be 0 and the other upper address bits are Don't Care (it might be easier to define these bits as 0, as shown in *Table 7*). The data byte pointed to by the lower address bits [A5:A0] is shifted out (MSB first) on Serial Data output (Q).

The first byte addressed can be any byte within the identification page.

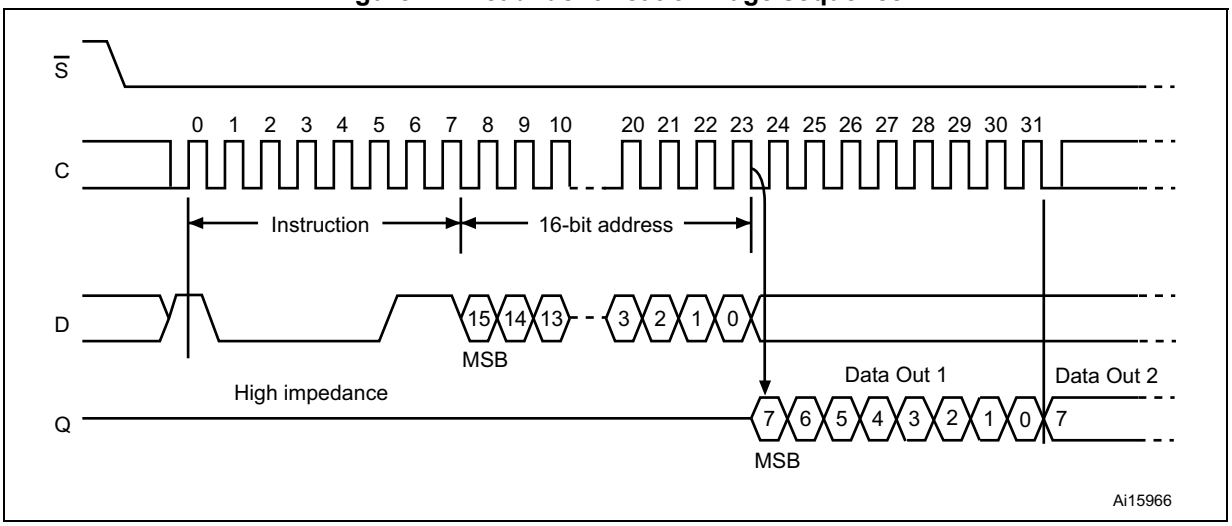
If Chip Select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented and the byte of data at the new address is shifted out.

Note that there is no roll over feature in the Identification Page. The address of bytes to read must not exceed the page boundary.

The read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time when the data bits are shifted out.

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Figure 12. Read Identification Page sequence



The first three bytes of the Identification page offer information about the device itself. Please refer to *Section 3.5: Identification page* for more information.

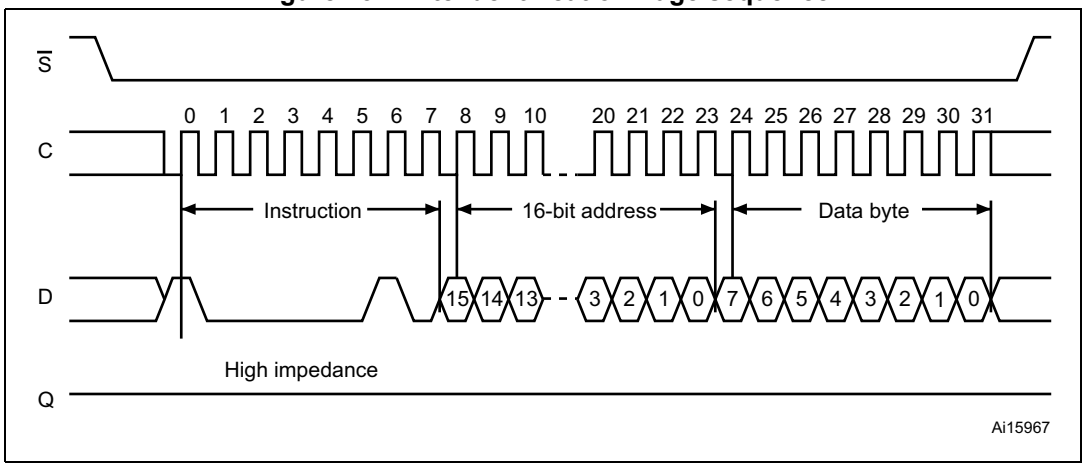
4.8 Write Identification Page (WRID)

The Write Identification Page instruction is used to write the Identification Page (additional page of 64 bytes which can also be permanently locked in Read-only mode).

The Chip Select signal ($\overline{S}$) is first driven low, and then the bits of the instruction byte, address bytes, and at least one data byte are shifted in (MSB first) on Serial Data input (D). Address bit A10 must be 0 and the other upper address bits are Don't Care (it might be easier to define these bits as 0, as shown in *Table 7*). The lower address bits [A5:A0] define the byte address inside the identification page.

The self-timed Write cycle starts from the rising edge of Chip Select ($\overline{S}$), and continues for a period t_W (as specified in *Table 13*).

Figure 13. Write Identification Page sequence



Note: The first three bytes of the Identification page offer the Device Identification code (Please refer to Section 3.5: Identification page for more information). Using the WRID command on these first three bytes overwrites the Device Identification code.

The instruction is discarded, and is not executed, under the following conditions:

- If a Write cycle is already in progress
- If the Block Protect bits (BP1,BP0) = (1,1)
- If one of the conditions defined in *Section 3.4.1: Protocol control* is not satisfied.

4.9 Read Lock Status (RDLS)

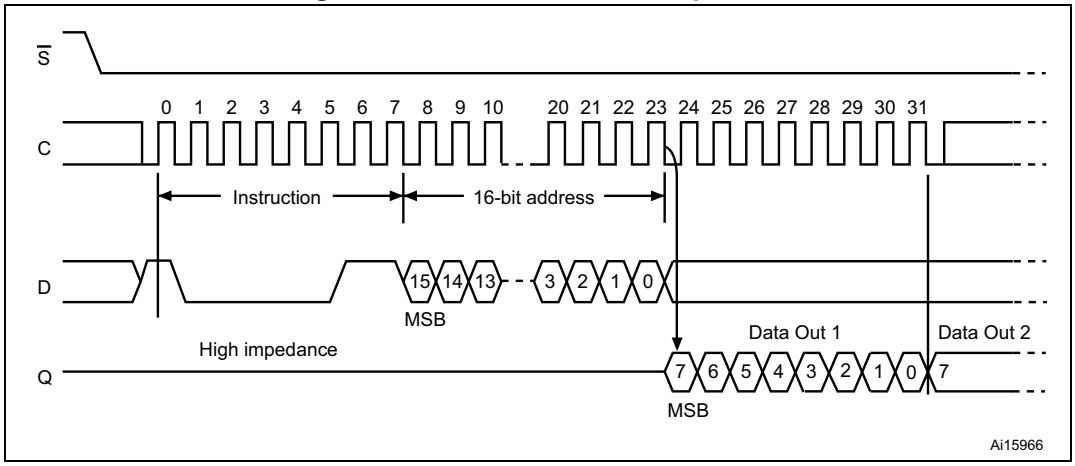
The Read Lock Status instruction is used to read the lock status.

To send this instruction to the device, Chip Select ($\overline{S}$) first has to be driven low. The bits of the instruction byte and address bytes are then shifted in (MSB first) on Serial Data input (D). Address bit A10 must be 1; all other address bits are Don't Care (it might be easier to define these bits as 0, as shown in *Table 7*). The Lock bit is the LSB (Least Significant Bit) of the byte read on Serial Data output (Q). It is at '1' when the lock is active and at '0' when the lock is not active. If Chip Select ($\overline{S}$) continues to be driven low, the same data byte is shifted out.

The read cycle is terminated by driving Chip Select ($\overline{S}$) high. The instruction sequence is shown in *Figure 14*.

The Read Lock Status instruction is not accepted and not executed if a Write cycle is currently in progress.

Figure 14. Read Lock Status sequence

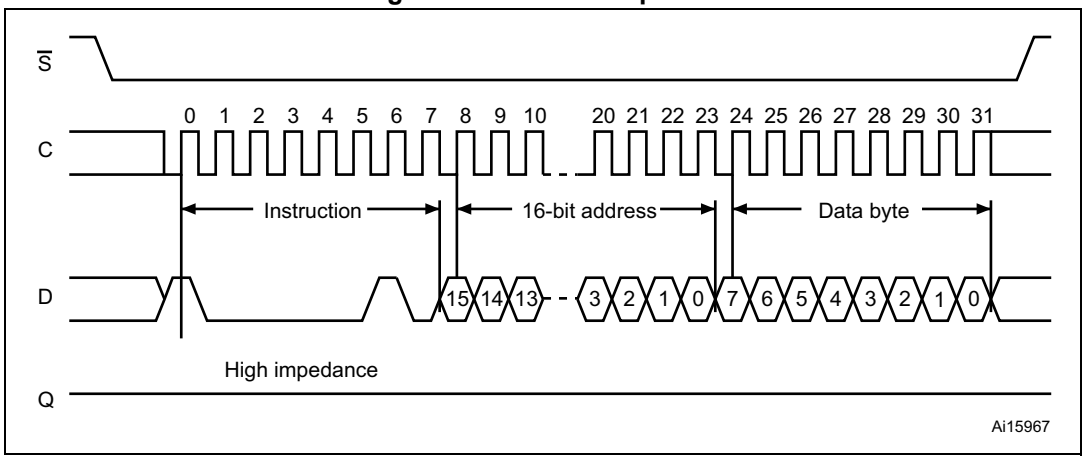


4.10 Lock Identification Page (LID)

The Lock Identification Page (LID) command is used to permanently lock the Identification Page in Read-only mode.

The LID instruction is issued by driving Chip Select (S) low, sending (MSB first) the instruction code, the address and a data byte on Serial Data input (D), and driving Chip Select (S) high. In the address sent, A10 must be equal to 1. All other address bits are Don't Care (it might be easier to define these bits as 0, as shown in *Table 7*). The data byte sent must be equal to the binary value xxxx xx1x, where x = Don't Care. The LID instruction is terminated by driving Chip Select (S) high at a data byte boundary, otherwise, the instruction is not executed.

Figure 15. Lock ID sequence



Driving Chip Select ($\overline{S}$) high at a byte boundary of the input data triggers the self-timed Write cycle which duration is t_W (specified in *Table 13*). The instruction sequence is shown in *Figure 15*.

The instruction is discarded, and is not executed, under the following conditions:

- If a Write cycle is already in progress
- If the Block Protect bits (BP1,BP0) = (1,1)
- If one of the conditions defined in *Section 3.4.1: Protocol control* is not satisfied.

5 Application design recommendations

5.1 Supply voltage (V_{CC})

5.1.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [$V_{CC(min)}$, $V_{CC(max)}$] range must be applied (see *Table 10* and *Table 11*).

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal Write cycle (t_W). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

5.1.2 Power-up conditions

When the power supply is turned on, V_{CC} continuously rises from V_{SS} to V_{CC}. During this time, the Chip Select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage. It is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor (see *Figure 16*).

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in *Table 12*.

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} reaches the internal threshold voltage (this threshold is defined in the DC characteristics *Table 12* as VRES).

When V_{CC} passes over the POR threshold, the device is reset and in the following state:

- in the Standby power mode
- deselected
- Status register values:
  - Write Enable Latch (WEL) bit is reset to 0.
  - Write In Progress (WIP) bit is reset to 0.
  - SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits).
- not in the Hold condition

As soon as the V_{CC} voltage has reached a stable value within [V_{CC}(min), V_{CC}(max)] range, the device is ready for operation.

5.1.3 Power-down

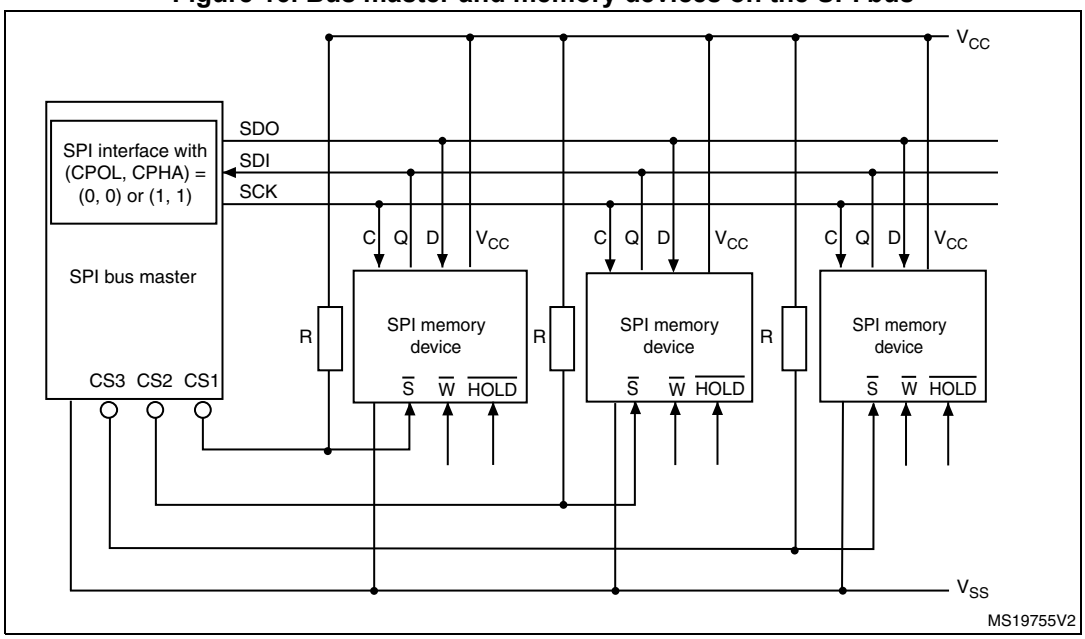
During power-down (continuous decrease in the V_{CC} supply voltage below the minimum V_{CC} operating voltage defined in *Table 12*), the device must be:

- deselected (Chip Select ($\overline{S}$) should be allowed to follow the voltage applied on V_{CC}),
- in Standby power mode (there should not be any internal Write cycle in progress).

5.2 Implementing devices on SPI bus

Figure 16 shows an example of three devices, connected to the SPI bus master. Only one device is selected at a time, so that only the selected device drives the Serial Data output (Q) line. All the other devices outputs are then in high impedance.

Figure 16. Bus master and memory devices on the SPI bus



1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals must be driven high or low as appropriate.

A pull-up resistor connected on each /$\overline{S}$ input (represented in *Figure 16*) ensures that each device is not selected if the bus master leaves the /$\overline{S}$ line in the high impedance state.

5.3 Cycling with Error Correction Code (ECC)

The Error Correction Code (ECC) is an internal logic function which is transparent for the SPI communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes[a]. Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group[a]. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the 4 bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value defined in *Table 9: Cycling performance by groups of 4 bytes*.

Example1: maximum cycling limit reached with 1 million cycles per byte

Each byte of a group can be equally cycled 1 million times (at 25 °C) so that the group cycling budget is 4 million cycles.

Example2: maximum cycling limit reached with unequal byte cycling

Inside a group, byte0 can be cycled 2 million times, byte1 can be cycled 1 million times, byte2 and byte3 can be cycled 500,000 times, so that the group cycling budget is 4 million cycles.

a. A group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer.

6 Delivery state

The device is delivered with:

- the memory array set to all 1s (each byte = FFh),
- Status register: bit SRWD =0, BP1 =0 and BP0 =0,
- Identification page: the first three bytes define the Device identification code (value defined in *Table 5*). The content of the following bytes is Don't Care.

7 Absolute maximum ratings

Stressing the device outside the ratings listed in *Table 8* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage temperature	–65	150	°C
T_{AMR}	Ambient operating temperature	–40	150	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_O	Voltage on Q pin	–0.50	V_{CC}+0.6	V
V_I	Input voltage	–0.50	6.5	V
I_{OL}	DC output current (Q = 0)	-	5	mA
I_{OH}	DC output current (Q = 1)	-	5	mA
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic pulse (Human Body Model)(2)	-	4000	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb-free assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions of Hazardous Substances (RoHS directive 2011/65/EU of July 2011).
2. Positive and negative pulses applied on pin pairs, in accordance with AEC-Q100-002 (compliant with ANSI/ESDA/JEDEC JS-001-2012, C1=100 pF, R1=1500 Ω, R2=500 Ω)

8 DC and AC parameters

This section summarizes the operating conditions and the DC/AC characteristics of the device.

Table 9. Cycling performance by groups of 4 bytes

Symbol	Parameter	Test condition	Min.	Max.	Unit
Ncycle	Write cycle endurance(1)	$T_A \leq 25$ °C, 1.8 V < V_{CC} < 5.5 V	-	4,000,000	Write cycle(2)
		T_A = 85 °C, 1.8 V < V_{CC} < 5.5 V	-	1,200,000	
		T_A = 105 °C, 1.8 V < V_{CC} < 5.5 V	-	900,000	

1. The Write cycle endurance is defined for groups of four data bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer, or for the status register byte (refer also to *Section 5.3: Cycling with Error Correction Code (ECC)*). The Write cycle endurance is defined by characterization and qualification.
2. A Write cycle is executed when either a Page Write, a Byte Write, a WRSR, a WRID or an LID instruction is decoded. When using the Byte Write, the Page Write or the WRID, refer also to *Section 5.3: Cycling with Error Correction Code (ECC)*.

Table 10. Operating conditions (voltage range R, temperature range 8)

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage	-	1.8	5.5	V
T_A	Ambient operating temperature	-	–40	105	°C
f_C	Operating clock frequency	$V_{CC} \geq 2.5$ V, capacitive load on Q pin ≤100pF	-	10	MHz
		$V_{CC} \geq 1.8$ V, capacitive load on Q pin ≤100pF	-	5	

Table 11. Operating conditions (voltage range R, temperature range 8) for high-speed communications

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage	-	4.5	5.5	V
T_A	Ambient operating temperature	-	–40	85	°C
f_C	Operating clock frequency	$V_{CC} \geq 4.5$ V, capacitive load on Q pin ≤ 60 pF	-	20	MHz

Table 12. DC characteristics (voltage range R, temperature range 8)

Symbol	Parameter	Test conditions (in addition to conditions specified in *Table 10*)	Min.	Max.	Unit
C_{OUT}(1)	Output capacitance (Q)	V_{OUT} = 0 V	-	8	pF
C_{IN}(1)	Input capacitance	V_{IN} = 0 V	-	6	
I_{LI}	Input leakage current	V_{IN} = V_{SS} or V_{CC}	-	2	µA
I_{LO}	Output leakage current	$\overline{S}$ = V_{CC}, V_{OUT} = V_{SS} or V_{CC}	-	3	
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V, C = 0.1 V_{CC}/0.9 V_{CC}, Q = open, f_C = 5 MHz	-	2	mA
		V_{CC} = 2.5 V, C = 0.1 V_{CC}/0.9 V_{CC}, Q = open, f_C = 10 MHz	-	2	
		V_{CC} = 5.5 V, f_C = 20 MHz(2) C = 0.1 V_{CC}/0.9 V_{CC}, Q = open	-	5	
I_{CC0}(3)	Supply current (Write)	1.8 V ≤ V_{CC} < 5.5 V during t_W, $\overline{S}$ = V_{CC}	-	2(1)	mA
I_{CC1}	Supply current (Standby mode)	t° = 25 °C, V_{CC} = 1.8 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	1	µA
		t° = 25 °C, V_{CC} = 2.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	2	
		t° = 25 °C, V_{CC} = 5.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	3	
		t° = 105 °C, V_{CC} = 1.8 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	5	
		t° = 105 °C, V_{CC} = 2.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	5	
		t° = 105 °C, V_{CC} = 5.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	10	
V_{IL}	Input low voltage	1.8 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
		2.5 V ≤ V_{CC} < 5.5 V	–0.45	0.3 V_{CC}	
V_{IH}	Input high voltage	1.8 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+ 1	V
		2.5 V ≤ V_{CC} < 5.5 V	0.7 V_{CC}	V_{CC}+ 1	
V_{OL}	Output low voltage	V_{CC} = 1.8 V, I_{OL} = 1 mA	-	0.3	V
		V_{CC} ≥ 2.5 V, I_{OL} = 2 mA	-	0.4	
V_{OH}	Output high voltage	V_{CC} = 1.8 V, I_{OH} = 1 mA	0.8 V_{CC}	-	V
		V_{CC} ≥ 2.5 V, I_{OH} = -2 mA	0.8 V_{CC}	-	
V_{RES}(1)	Internal reset threshold voltage	-	0.5	1.5	V

1. Characterized only, not 100% tested.
2. When –40 °C < t° < 85 °C.
3. Average value during the Write cycle (t_W).

Table 13. AC characteristics

Symbol	Alt.	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
			Test conditions specified in *Table 10*		Test conditions specified in *Table 10*		Test conditions specified in *Table 11*		
f_C	f_{SCK}	Clock frequency	-	5	-	10	-	20	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	60	-	30	-	15	-	ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	60	-	30	-	15	-	
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	90	-	40	-	20	-	
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	60	-	30	-	15	-	
t_{CHSL}		$\overline{S}$ not active hold time	60	-	30	-	15	-	
t_{CH}(1)	t_{CLH}	Clock high time	80	-	40	-	20	-	
t_{CL}(1)	t_{CLL}	Clock low time	80	-	40	-	20	-	
t_{CLCH}(2)	t_{RC}	Clock rise time	-	2	-	2	-	2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time	-	2	-	2	-	2	
t_{DVCH}	t_{DSU}	Data in setup time	20	-	10	-	5	-	ns
t_{CHDX}	t_{DH}	Data in hold time	20	-	10	-	10	-	
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	60	-	30	-	15	-	
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	60	-	30	-	15	-	
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0	-	0	-	0	-	
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0	-	0	-	0	-	
t_{SHQZ}(2)	t_{DIS}	Output disable time	-	80	-	40	-	20	
t_{CLQV}(3)	t_V	Clock low to output valid	-	80	-	40	-	20	
t_{CLQX}	t_{HO}	Output hold time	0	-	0	-	0	-	
t_{QLQH}(2)	t_{RO}	Output rise time	-	20	-	20	-	20	
t_{QHQL}(2)	t_{FO}	Output fall time	-	20	-	20	-	20	
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid	-	80	-	40	-	20	
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z	-	80	-	40	-	20	
t_W	t_{WC}	Write time	-	4	-	4	-	4	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Value guaranteed by characterization, not 100% tested in production.
3. t_{CLQV} must be compatible with t_{CL} (clock low time): if t_{SU} is the Read setup time of the SPI bus master, t_{CL} must be equal to (or greater than) $t_{CLQV}+t_{SU}$.

Figure 17. AC measurement I/O waveform

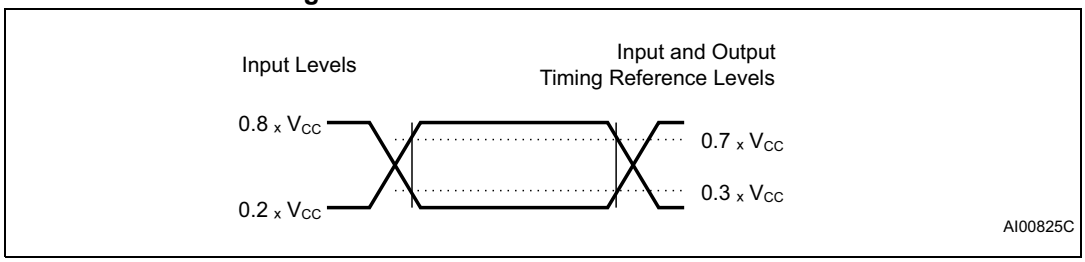


Figure 18. Serial input timing

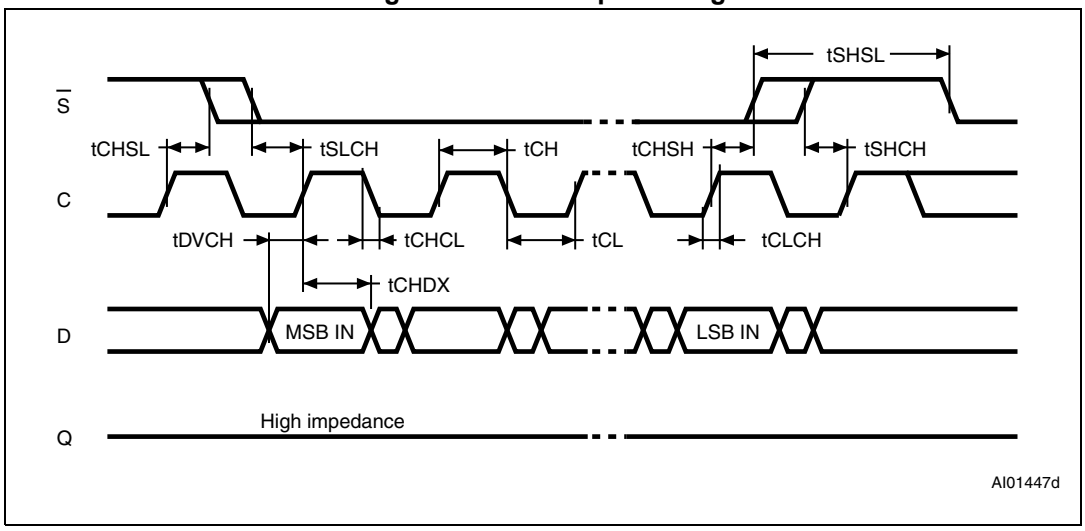


Figure 19. Hold timing

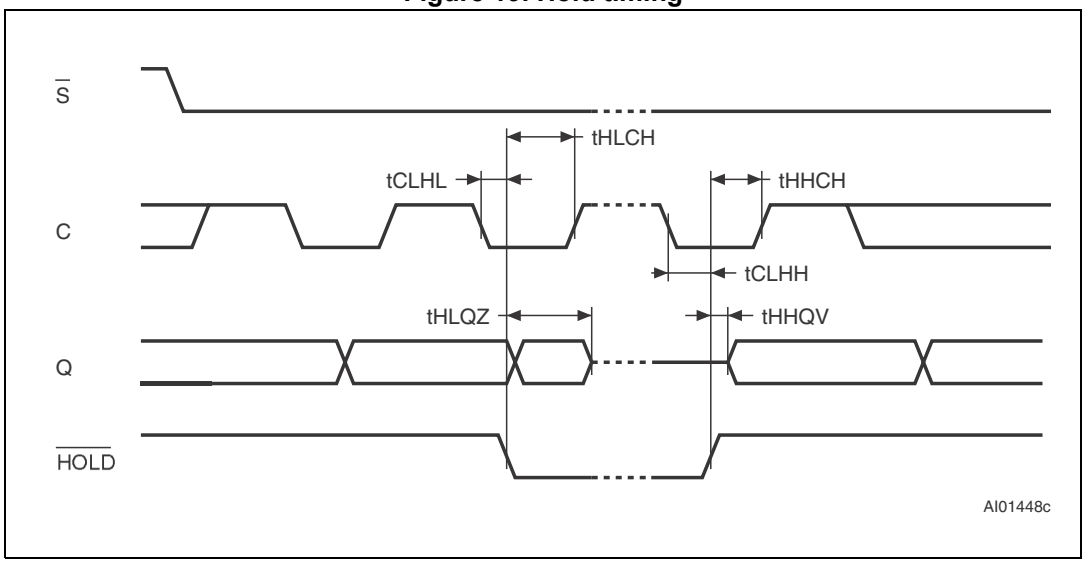
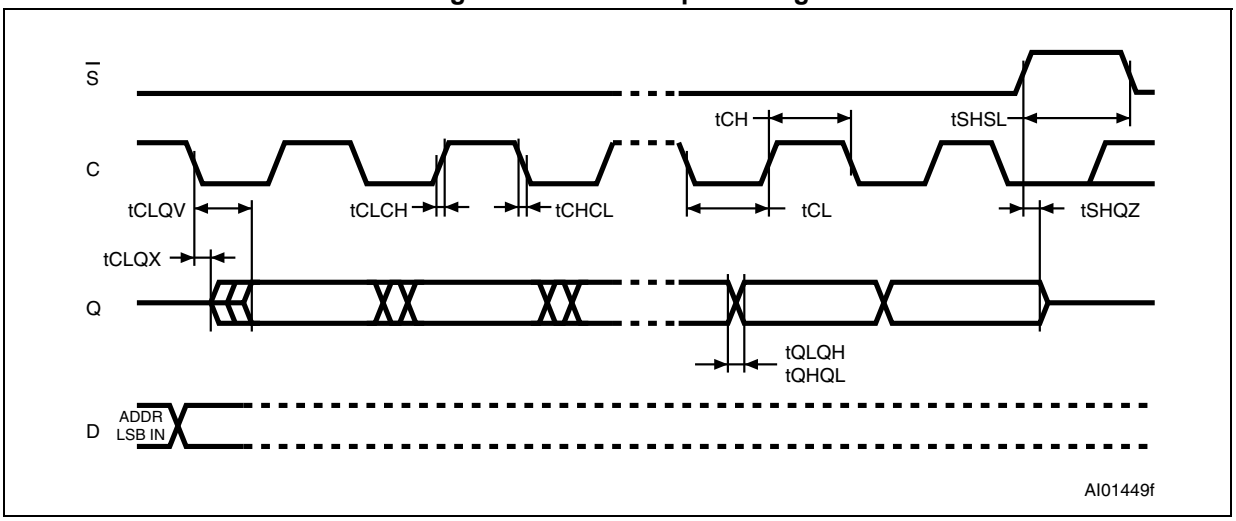


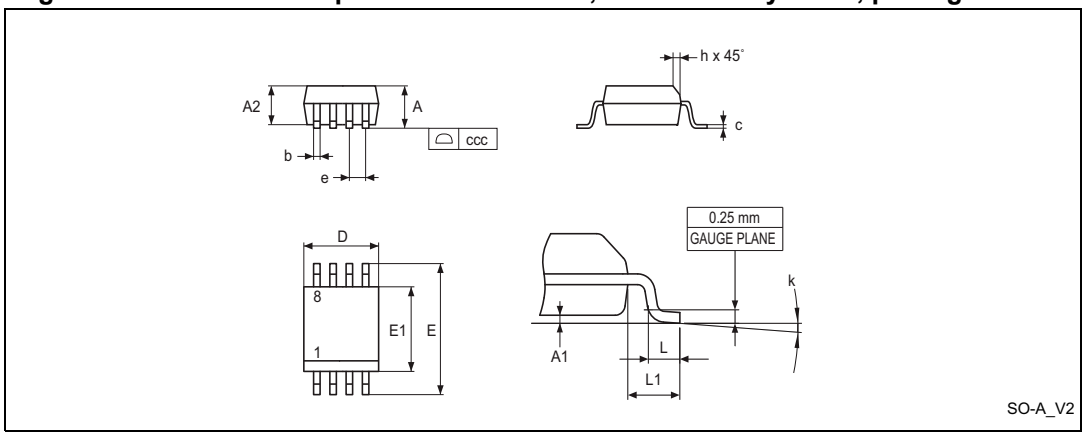
Figure 20. Serial output timing



9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 21. SO8N – 8-lead plastic small outline, 150 mils body width, package outline



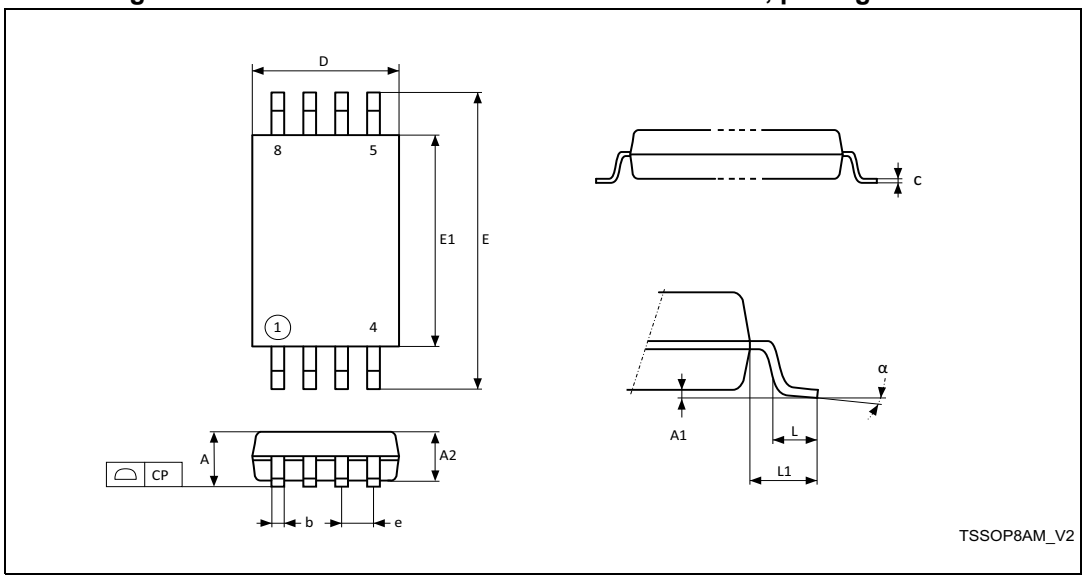
1. Drawing is not to scale.

Table 14. SO8N – 8-lead plastic small outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	-	-	1.75	-	-	0.0689
A1	-	0.10	0.25	-	0.0039	0.0098
A2	-	1.25	-	-	0.0492	-
b	-	0.28	0.48	-	0.011	0.0189
c	-	0.17	0.23	-	0.0067	0.0091
ccc	-	-	0.10	-	-	0.0039
D	4.90	4.80	5.00	0.1929	0.189	0.1969
E	6.00	5.80	6.20	0.2362	0.2283	0.2441
E1	3.90	3.80	4.00	0.1535	0.1496	0.1575
e	1.27	-	-	0.05	-	-
h	-	0.25	0.50	-	0.0098	0.0197
k	-	0°	8°	-	0°	8°
L	-	0.40	1.27	-	0.0157	0.05
L1	1.04	-	-	0.0409	-	-

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 22. TSSOP8 – 8-lead thin shrink small outline, package outline



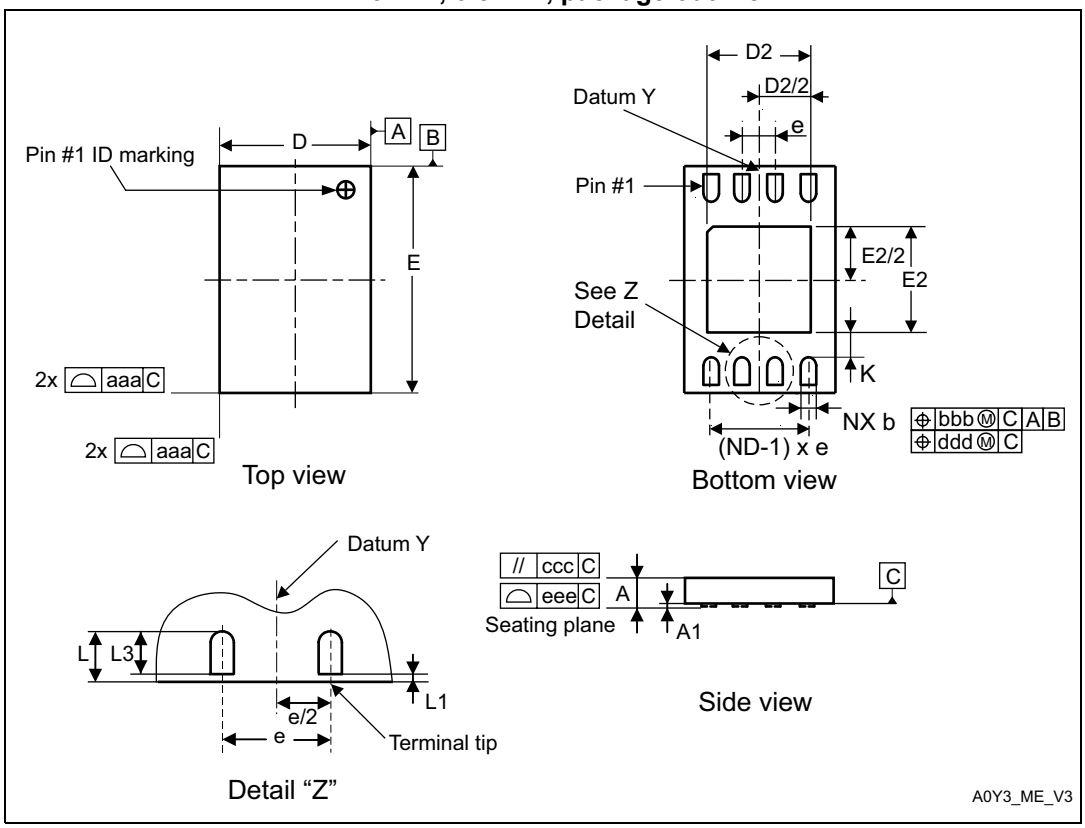
1. Drawing is not to scale.

Table 15. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	-	-	1.200	-	-	0.0472
A1	-	0.050	0.150	-	0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b	-	0.190	0.300	-	0.0075	0.0118
c	-	0.090	0.200	-	0.0035	0.0079
CP	-	-	0.100	-	-	0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	-	-	0.0256	-	-
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000	-	-	0.0394	-	-
α	-	0°	8°	-	0°	8°

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 23. WFDFPN8 (MLP8) – 8-lead very thin fine pitch dual flat package no lead 2 x 3 mm, 0.5 mm, package outline



1. Drawing is not to scale.
2. *The central pad (the area E2 by D2 in the above illustration) must be either connected to Vss or left floating (not connected) in the end application.*

Table 16. WFDFPN8 (MLP8) – 8-lead very thin fine pitch dual flat package no lead 2 x 3 mm, 0.5 mm pitch, mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.700	0.750	0.800	0.0276	0.0295	0.0315
A1	0.025	0.045	0.065	0.0010	0.0018	0.0026
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
D	1.900	2.000	2.100	0.0748	0.0787	0.0827
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.500	-	-	0.0197	-
L1	-	-	0.150	-	-	0.0059
L3	0.300	-	-	0.0118	-	-
D2	1.050	-	1.650	0.0413	-	0.0650
E2	1.050	-	1.450	0.0413	-	0.0571
K	0.400	-	-	0.0157	-	-
L	0.300	-	0.500	0.0118	-	0.0197
NX[2]	8					
ND[3]	4					
aaa	0.150			0.0059		
bbb	0.100			0.0039		
ccc	0.100			0.0039		
ddd	0.050			0.0020		
eee[4]	0.080			0.0031		

1. Values in inches are converted from mm and rounded to four decimal digits.
2. NX is the number of terminals.
3. ND is the number of terminals on “D” sides.
4. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

10 Part numbering

Table 17. Ordering information scheme

Example: M95256 -D R DW 8 T P /K

Device type

M95 = SPI serial access EEPROM

Device function

256-D = 256 Kbit (32 Kbytes) plus Identification Page

Operating voltage

R = V_{CC} = 1.8 to 5.5 V

Package(1)

MN = SO8 (150 mils width)

DW = TSSOP8 (169 mils width)

MF = WFDFPN8 (2 x 3 mm)

Device grade

8 = – 40 to 105 °C.

Option

blank = Tube packing

T = Tape and reel packing

Plating technology

P or G = ECOPACK2®

Process letter

/K = Manufacturing technology code

1. All packages are ECOPACK2® (RoHS compliant and free of brominated, chlorinated and antimony-oxide flame retardants).

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Engineering samples

Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

11 Revision history

Table 18. Document revision history

Date	Revision	Changes
09-Feb-2015	1	Initial release.

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