Keysight Technologies
M8085A MIPI Receiver Test Solutions

Data Sheet
Version 1.0

KEYSIGHT TECHNOLOGIES
Unlocking Measurement Insights

Introduction

The M8085A is a software plug-in for M8070A Bit Error Ratio Test system software within the M8000 series of BER test solutions. The M8085A software plug-in controls an M8190A or M8195A Arbitrary Waveform Generator (AWG) to create C-PHY and D-PHY standard conformant test signals. Depending on the provisions for error detection implemented in the DUT receiver (RX) the plug-in provides the option to connect to your DUT built-in receiver via the so-called IBERReader interface, which is based on a user provided DLL, to read the bit error counter and display the result in the M8085A user interface.

Key benefits

- Fast characterization of digital C-PHY and D-PHY receivers through easy test signal generation
- Editor enabling set-up of all PHY-parameters in application terms
- Reliable and automated calibration of signal parameters
- Complete and conformant RX test procedures for single lane enabling automated, unattended test
- Can be operated manually or through program control via customer or N5990A Keysight test sequencer

Mobile applications, challenges for testing C-PHY and D-PHY receivers and solutions

While modern mobile products are undoubtedly designed for high speed data transmission and processing (e.g. HD camera or video applications), they are even so undoubtedly often in a mode where this high speed data capabilities are not needed and they preferably are operating in a mode consuming less to nearly no power at all in order to extend battery life. Mobile standards are designed accordingly featuring such power saving modes.

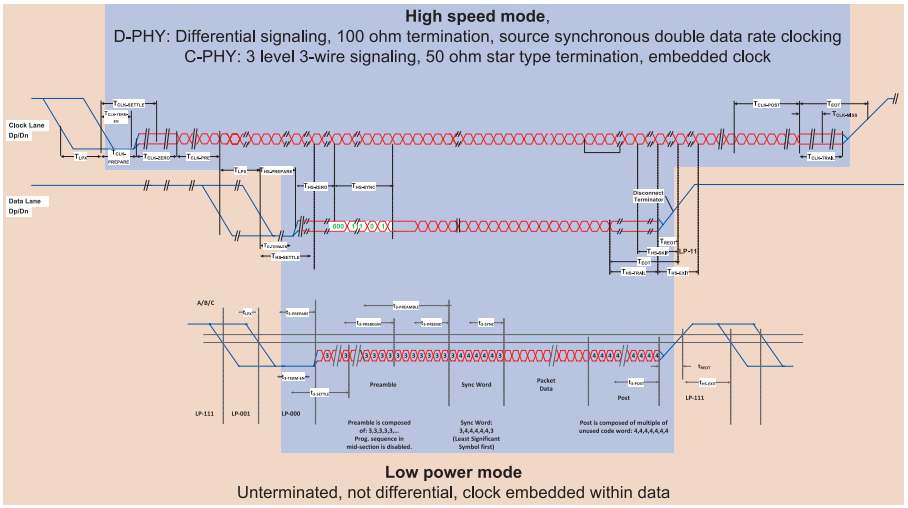

Figure 1. Timing Diagram of C-PHY and D-PHY showing transitions from Low Power Mode to High Speed Mode and back

As depicted in Figure 1 above, the PHY-Layer standards D-PHY and C-PHY, which support the applications CSI (for camera) and DSI (for Display), use different signaling (levels and data formats) in Low Power (LP) and High Speed (HS) mode. The LP modes for these PHYs are more or less identical. However, while D-PHY uses differential NRZ format for HS-data transmission, C-PHY was brought up allowing transmission of 2.28 bits/symbol utilizing non-differential data format requiring 3-wires , 3-level transmission with a star-type resistive termination and a 16/7 bit encoding.

Essentials of the C-PHY Standard

An example for a lane configuration and the 3-level / 3 wire signaling is shown below in Figure 2a and 2b

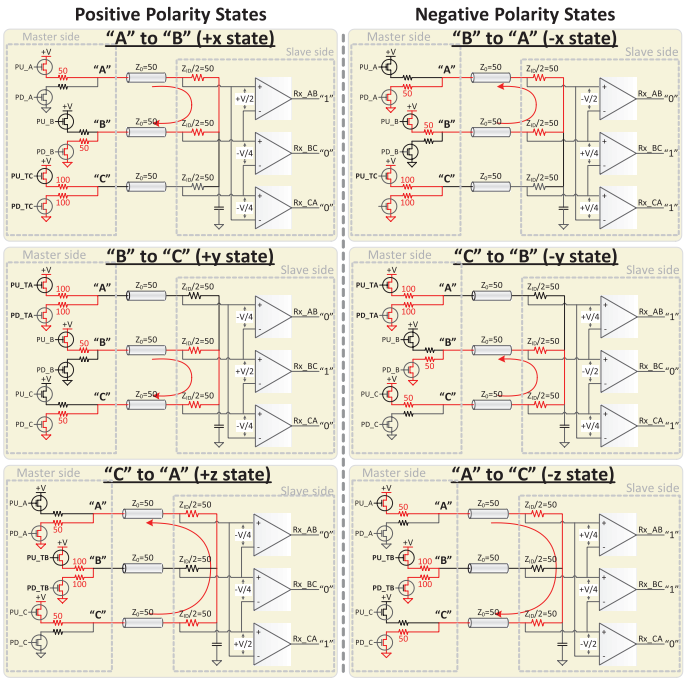

Figure 2a. C-PHY block diagram for a single lane

Coding rules and possible wire states:

- 27 possible wires states
- 6 allowed wire states (+x -x, +y, -y, +z, -z)only those states with different voltage on each wire
- From one symbol to the next symbol only 5 wire states are possible, because a transition is required for clock recovery (CR)
- Theoretical coding gain: log2(5) = 2.32
- Practically usable gain is 2.28 by sending 16 bits in 7 symbols

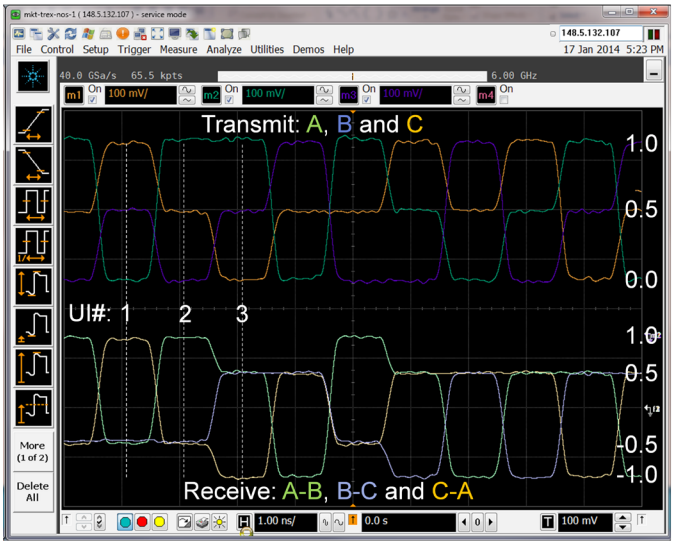

Figure 2b. All six possible wire states and HS data signal on A, B and C wires and differential signals as seen by the three differential receivers

It is obvious that the generation of the necessary test patterns is a real challenge. Traditional BERTs using NRZ pattern format cannot generate such 3-level signals required for C-PHY HS-mode not to mention 5-level signals when also including LP-mode. AWGs can generate any signal; however, customers may not want to deal with the necessary generation of the waveform (vector) files.

MIPI Receiver Test Solutions

The next level of integration

The M8000 Series of BER test solutions for digital RX characterization with its modular AXI-HW architecture and its Plug In SW-concept allows composing the required BERT consisting of Pattern Generator (PG) and Error Detector (ED) building blocks using a Keysight M819x AWG as PG and the M8070A System Software. The M8070A SW furthermore hosts the application specific test automation SW Plug In M8085A as depicted below in Figure 4 below, which hosts the IBERReader interface providing the connection to the error detector that needs to be provided by the DUT.

The functionality is visualized in the (SW-) block diagram

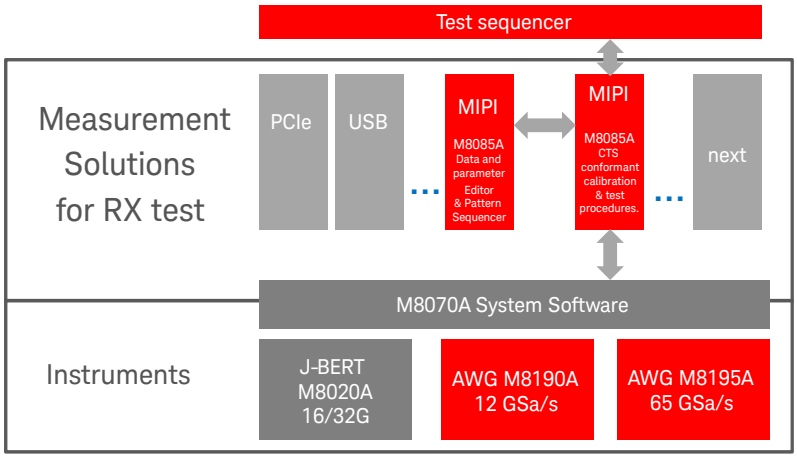

Figure 3. Architecture of application specific solutions within the M8000 System

Building blocks of a complete RX test

An RX test is used to determine an RX's capability to properly detect the digital signal content, even for worst-case impaired input signals. For this testing

- A Bit Error Ratio Tester's (BERT) Pattern Generator (BERT PG) is used to emulate a system's TX plus channel thus generating a data signal containing the impairments to be expected at the RX input when it is operating in a target system.
- This signal has to be calibrated according to the specification / conformance test suite (CTS)
- The RX is set into test mode and the input of the RX under test is stimulated with the calibrated test signal
- Proper detection of the digital content is monitored in a suitable fashion to determine performance according to target BER

These tasks are depicted in the functional block diagram Figure 4 below. The functionality is delivered by separate SW blocks allowing the user to tailor the solution according to his needs.

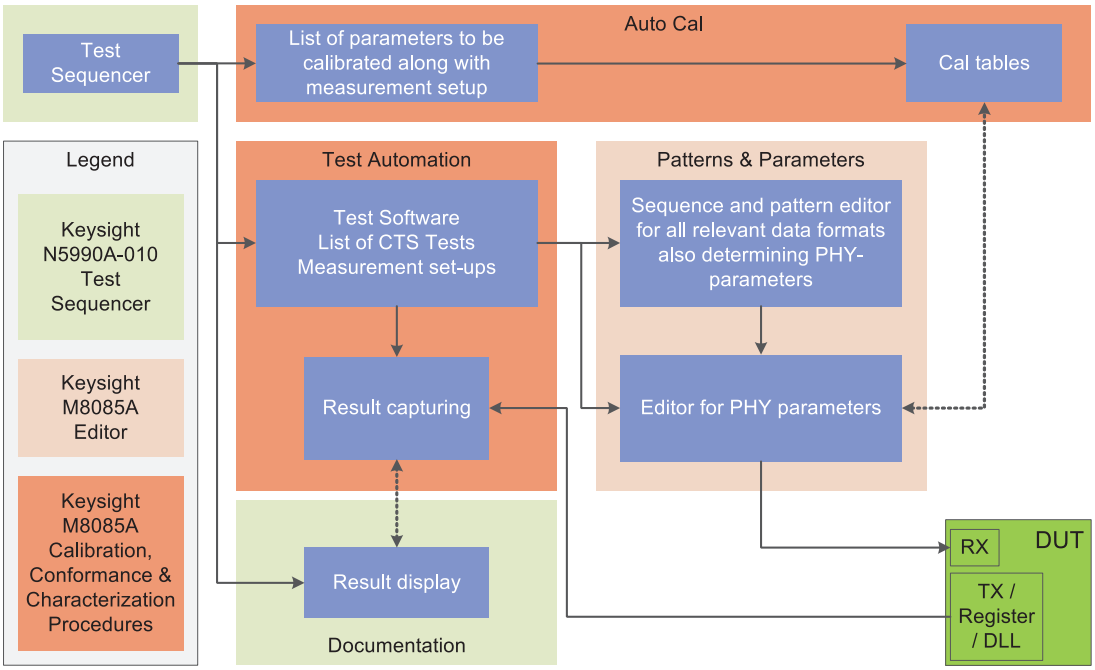

Figure 4. Building blocks of an RX Test and Related SW Products using Plug Ins for the M8000 System SW M8070A

1. Editors allow direct setup of PHY parameters and data content (local from GUI or remote under program control via SCPI commands)
2. Automated calibration, conformance and characterization procedures can be started individually from GUI or a remote program
3. In case the customer does not want to generate his own remote control program or use his own test sequencer the test sequencer from the Keysight N5990A Test Automation Software Platform provides complete automated control of all the calibration and tests.

M8085A Product Options

The M8085A addresses mobile applications. Options Cxy and Dxy are addressing C-PHY and D-PHY standard respectively. The SW is available as a perpetual, Transportable (options CT1, DT1, CTA and DTA) or Network (options CN1, DN1, CNA and DNA) license.

P/N	Option	Description	Comments
M8085A	-CT1	MIPI C-PHY Editor for M819xA AWG, Transportable, Perpetual License	
	-CN1	MIPI C-PHY Editor for M819xA AWG, Network/Floating, Perpetual License	
	-CTA	MIPI C-PHY Calibration, Conformance and Characterization Procedures for M819xA AWG, transportable, perpetual License	
	-CNA	MIPI C-PHY Calibration, Conformance and Characterization Procedures for M819xA AWG, Network/Floating, Perpetual License	

P/N	Option	Description	Comments
M8085A	-DT1	MIPI D-PHY Editor for M819xA AWG, Transportable, Perpetual License	
	-DN1	MIPI D-PHY Editor for M819xA AWG, Network/Floating, Perpetual License	
	-DTA	MIPI D-PHY Calibration, Conformance and Characterization Procedures for M819xA AWG, transportable, perpetual License	
	-DNA	MIPI D-PHY Calibration, Conformance and Characterization Procedures for M819xA AWG, Network/Floating, Perpetual License	

Both the C-PHY and the D-PHY are both used for camera (CSI) and Display (DSI) applications. Both can appear as single- or multilane-applications. Which SW option and which HW generator module is required for which flavor is listed below:

Addressable numbers of C-PHY D-PHY lanes	Usable HW modules	Applicable SW options
1	M8190A, M8195A, rev.2	CT1, DT1, CTA, DTA, CN1, DN1, CNA, DNA
1,2,4 (D(PHY), 1,3,4 (C-PHY)	M8195A, rev.2	CT1, DT1, CTA, DTA, CN1, DN1, CNA, DNA

Standards are continuously improved addressing evolving needs e.g. for higher bandwidth (BW) and/ or lower power etc.
The table below shows, which options address which standard / CTS revisions.

Standard	Addressed Standard / CTS-Revisions	Applicable SW options
D-PHY	Up to 1.2	Dx1, DxA
C-PHY	Up to 1.0	Cx1, CxA

Benefits

Key features of the M8085A editor options

As already mentioned above, the generators used for C-PHY and D-PHY applications are of the AWG-type. These instruments generate their output signal from a vector memory that contains the digitized waveform information. Usually the waveform vectors have to be generated by the user utilizing waveform synthesis tools such as MATLAB or equivalent. With the M8085A editor SW options, these instruments can be operated from the familiar user interface which the M8070A SW provides for the J-BERT M8020A - with the addition of application specific parameters as shown below in Figures 5 to 7 for the C-PHY application.

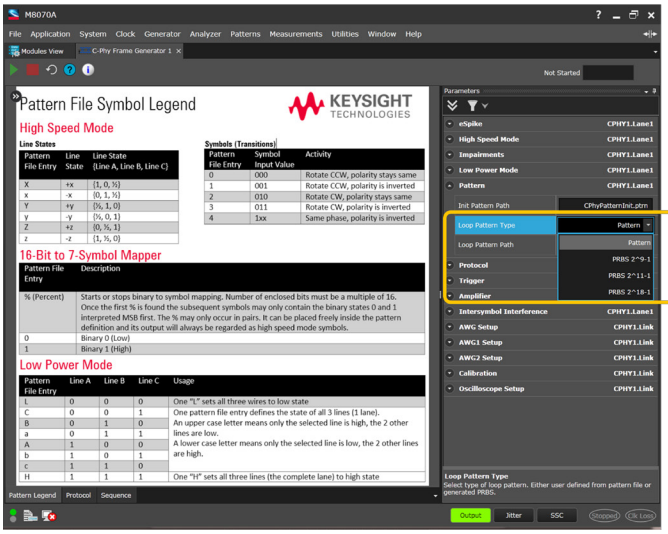

Figure 5 C-PHY editor showing GUI for Data set-up

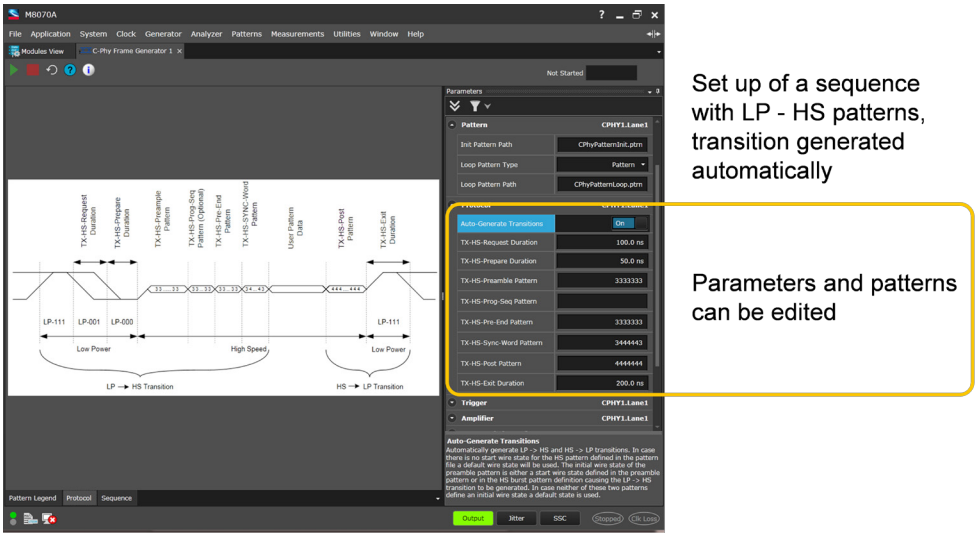

Figure 6. C-PHY editor showing GUI for LP-HS transition

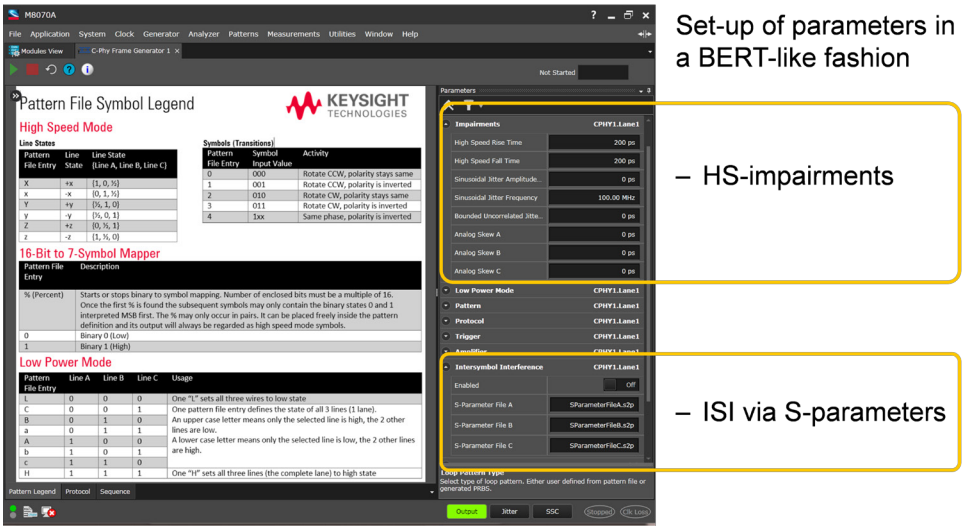

Figure 7. C-PHY editor showing GUI for set-up of PHY parameters (HS)

Key features of the M8085A calibration and test procedure options

A prerequisite for any RX test is to stimulate the RX with well-calibrated test signals. As the test set-ups often differ from those used to perform the factory calibration of the generators and influence the parameter values it is necessary to do an in-situ calibration. The Conformance Test Suites (CTS) for both C-PHY and D-PHY specify the different test set-ups and by this indirectly also the calibration procedures.

Furthermore they contain quite a few tests to verify the conformance or characterize the margins of the respective HS and LP RXs, as well as tests verifying proper behavior during mode transitions. To unburden the user from having to study the CTS and maybe the specification itself and translate the insights into test set-ups and calibration and test procedures, Keysight provides the M8085A options CTA /CNA and DTA / DNA containing these calibration, test and characterization procedures.

Below it is listed which tests are addressed by the above mentioned SW options.

List of tests C-PHY provided by options CTA and CNA	
CTS SECTION 2: RX TIMERS AND ELECTRICAL TOLERANCES	
GROUP 1: LP-RX VOLTAGE AND TIMING REQUIREMENTS	
– Test 2.1.1 – LP-RX Logic 1 Input Voltage (VIH)	√
– Test 2.1.2 – LP-RX Logic 0 Input Voltage, Non-ULP State (VIL)	√
– Test 2.1.3 – LP-RX Input Hysteresis (VHYST)	√
– Test 2.1.4 – LP-RX Minimum Pulse Width Response (TMIN-RX)	√
– Test 2.1.5 – LP-RX Input Pulse Rejection (eSPIKE)	√
GROUP 2: LP-RX BEHAVIORAL REQUIREMENTS	
– Test 2.2.1 – LP-RX Initialization period (TINIT)	√
– Test 2.2.2 – ULPS Exit: LP-RX TWAKEUP Timer Value	√
– Test 2.2.3 – LP-RX Invalid/Aborted Escape Mode Entry	√
– Test 2.2.4 – LP-RX Invalid/Aborted Escape Mode Command	√
– Test 2.2.5 – LP-RX Escape Mode, Ignoring of Post-Trigger-Command Extra Bits	√
– Test 2.2.6 – LP-RX Escape Mode Unsupported/Unassigned Commands	√
GROUP 3: HS-RX VOLTAGE AND JITTER TOLERANCE REQUIREMENTS	
– Test 2.3.1 – HS-RX Amplitude Tolerance (VCPRX(DC), VIHHS, VILHS)	√
– Test 2.3.2 – HS-RX Differential Input High/Low Thresholds (VIDTH, VIDTL)	√
– Test 2.3.3 – HS-RX Jitter Tolerance	√
GROUP 4: HS-RX TIMER REQUIREMENTS	
– Test 2.4.1 – HS-RX T3-TERM-EN Duration	√
– Test 2.4.2 – HS-RX T3-PREPARE Tolerance	√
– Test 2.4.3 – HS-RX T3-PREBEGIN Tolerance	√
– Test 2.4.4 – HS-RX T3-PROGSEQ Tolerance	√
– Test 2.4.5 – HS-RX T3-POST Tolerance	√

List of tests D-PHY options DTA and DNA	
CTS SECTION 2: RX TIMERS AND ELECTRICAL TOLERANCES	
GROUP 1: LP-RX VOLTAGE AND TIMING REQUIREMENTS	
– Test 2.1.1 – LP-RX Logic 1 Input Voltage (VIH)	√
– Test 2.1.2 – LP-RX Logic 0 Input Voltage, Non-ULP State (VIL)	√
– Test 2.1.3 – LP-RX Logic 0 Input Voltage, ULP State (VIL-ULPS)	√
– Test 2.1.4 – LP-RX Input Hysteresis (VHYST)	√
– Test 2.1.5 – LP-RX Minimum Pulse Width Response (TMIN-RX)	√
– Test 2.1.6 – LP-RX Input Pulse Rejection (eSPIKE)	√
– Test 2.1.7 – LP-RX Interference Tolerance (VINT and fINT)	√
– Test 2.1.8 – LP-CD Logic Contention Thresholds (VIHCD and VILCD)	√
GROUP 2: LP-RX BEHAVIORAL REQUIREMENTS	
– Test 2.2.1 – LP-RX Initialization period (TINIT)	√
– Test 2.2.2 – ULPS Exit: LP-RX TWAKEUP Timer Value	√
– Test 2.2.3 – Clock Lane LP-RX Invalid/Aborted ULPS Entry	√
– Test 2.2.4 – Data Lane LP-RX Invalid/Aborted Escape Mode Entry	√
– Test 2.2.5 – Data Lane LP-RX Invalid/Aborted Escape Mode Command	√
– Test 2.2.6 – Data Lane LP-RX Escape Mode Invalid Exit (INFORMATIVE)	√
– Test 2.2.7 – Data Lane LP-RX Escape Mode, Ignoring of Post-Trigger-Command Extra Bits	√
– Test 2.2.8 – Data Lane LP-RX Escape Mode Unsupported/Unassigned Commands	√
GROUP 3: HS-RX VOLTAGE AND SETUP/HOLD REQUIREMENTS	
– Test 2.3.1 – HS-RX Common Mode Voltage Tolerance (VCMRX(DC))	√
– Test 2.3.2 – HS-RX Differential Input High Threshold (VIDTH)	√
– Test 2.3.3 – HS-RX Differential Input Low Threshold (VIDTL)	√
– Test 2.3.4 – HS-RX Single-Ended Input High Voltage (VIHHS)	√
– Test 2.3.5 – HS-RX Single-Ended Input Low Voltage (VILHS)	√
– Test 2.3.6 – HS-RX Common-Mode Interference 50MHz - 450MHz (ΔVCMRX(LF))	√
– Test 2.3.7 – HS-RX Common-Mode Interference Beyond 450MHz (ΔVCMRX(HF))	√
– Test 2.3.8 – HS-RX Setup/Hold and Jitter Tolerance	√
GROUP 4: HS-RX TIMER REQUIREMENTS	
– Test 2.4.1 – Data Lane HS-RX TD-TERM-EN Value	√
– Test 2.4.2 – Data Lane HS-RX THS-PREPARE + THS-ZERO Tolerance	√
– Test 2.4.3 – Data Lane HS-RX THS-SETTLE Value	√
– Test 2.4.4 – Data Lane HS-RX THS-TRAIL Tolerance	√
– Test 2.4.5 – Data Lane HS-RX THS-SKIP Value	√
– Test 2.4.6 – Clock Lane HS-RX TCLK-TERM-EN Value	√
– Test 2.4.7 – Clock Lane HS-RX TCLK-PREPARE + TCLK-ZERO Tolerance	√
– Test 2.4.8 – Clock Lane HS-RX TCLK-SETTLE Value	√
– Test 2.4.9 – Clock Lane HS-RX TCLK-TRAIL Tolerance	√
– Test 2.4.10 – Clock Lane HS-RX TCLK-MISS Value	√
– Test 2.4.11 – Clock Lane HS-RX TCLK-PRE and TCLK-POST Tolerance	√

Performing calibration and tests automatically

Figure 8 below shows how the M8085A-CTA C-PHY or M8085A-DTA D-PHY calibration procedure guides the user through the connections of the oscilloscope with the AWG and the DUT. The result of the automated calibration is displayed in graphical form as well as with numerical values listed in a table.

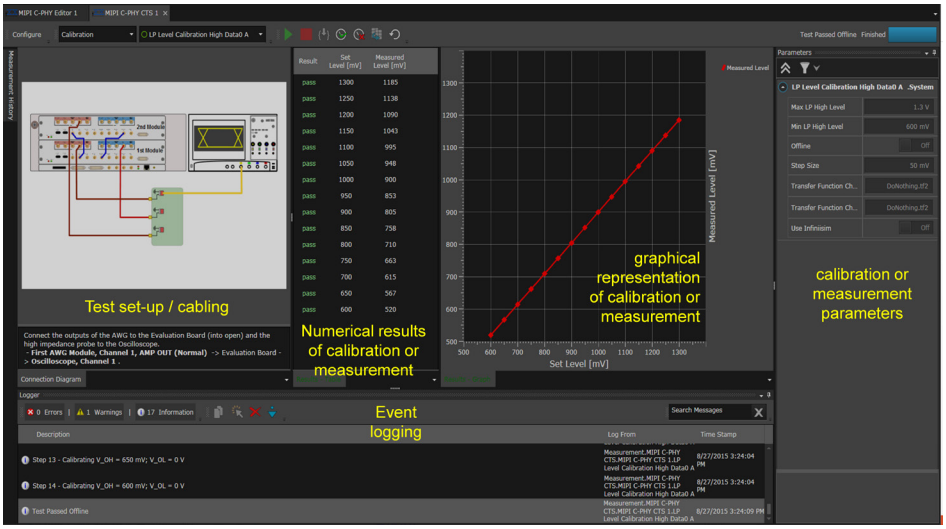

Figure 8. GUI of M8085A option CTA / CNA, Calibration and test routines for C-PHY

Ordering a MIPI RX C-PHY Test Configuration

Complete n-Lane C-PHY Setup (HS, LP, and transitions, full compliance) using M8195A rev2 modules					
Number of C-PHY lanes			**1**	**3**	**4**
Product	**Option**	**Description**	**Quantity**		
M8195A	M8195A-BU1	AXIe Chassis: 5-slot with Integrated System Module plus Embedded Controller: Quad Core, 8GB RAM, 160 SSD, 2 GB/s	1	1	1
M8195A	M8195A-004	Arbitrary Waveform Generator, 4 Channels, 65 GSa/s	1	3	4
M8195A	M8195A-002	Arbitrary Waveform Generator, 2 Channels, 65 GSa/s	0	0	0
M8195A	M8195A-001	Arbitrary Waveform Generator, 1 Channel, 65 GSa/s	0	0	0
M8195A	M8195A-16G	Upgrade to 16 GSa Memory	1	3	4
M8195A	M8195A-SEQ	Sequencer	1	3	4
M8197A	N/A	Synchcronisation module for the M8195A	0	1	1
M8195A	R-50C-011-5	Calibration Assurance Plan - Return to Keysight - 5 years	0	0	0
M8195A	R-51B-001-5Z	Warranty Assurance Plan - Return to Keysight - 5 years	0	0	0
M8070A	M8070A-0TP	System Software for M8000 Series of BER Test Solutions, Transportable, Perpetual License	1	1	1
M8070A	M8070A-0NP	System Software for M8000 Series of BER Test Solutions, Network License	0	0	0
M8070A	M8070A-1TP	Device Control Interface	1	1	1
M8195A	M8195A-810	Matched Cable Pair for M8195A AWG, 2.92 mm	0	0	0
M8085A	M8085A-CT1	MIPI C-PHY Editor for M819xA AWG, Transportable, Perpetual License	1	1	1
M8085A	M8085A-CTA	MIPI C-PHY Calibration, Conformance and Characterization Procedures for M819xA AWG, transportable, perpetual License	1	1	1
M8085A	M8085A-CN1	MIPI C-PHY Editor for M819xA AWG, Network License	0	0	0
M8085A	M8085A-CNA	MIPI C-PHY Calibration, Conformance and Characterization Procedures for M819xA AWG, Network License	0	0	0
N5990A	N5990A-010	Bitifeye Test sequencer for M8085A Cxx options	1	1	1
Complete 1-Lane C-PHY Setup (HS, LP, and transitions, full compliance) using M8190A modules					
M8190A	M8190A-BU1	Bundle 1 consisting of M9505A AXIe Chassis w/ 5 slots and M9536A Embedded PC Controller	1	N/A	N/A
M8190A	M8190A-001	Arbitrary Waveform Generator 1 Channel	1	N/A	N/A
M8190A	M8190A-002	Arbitrary Waveform Generator 2 Channel	1	N/A	N/A
M8190A	M8190A-02G	Upgrade from 128Msa to 2GSa Memory/Channel	3	N/A	N/A
M8190A	M8190A-12G	12GSa/s with 12 bit resolution	2	N/A	N/A
M8190A	M8190A-14B	14 Bit resolution at 8GSa/s	0	N/A	N/A
M8190A	M8190A-AMP	Additional AC and DC Amplifier	2	N/A	N/A
M8190A	M8190A-SEQ	Sequencer	2	N/A	N/A
M8192A	N/A	Synchronization module for the M8190A	1	N/A	N/A
M8070A	M8070A-0TP	System Software for M8000 Series of BER Test Solutions, Transportable, Perpetual License	1	N/A	N/A
M8070A	M8070A-0NP	System Software for M8000 Series of BER Test Solutions, Network License	0	N/A	N/A
M8070A	M8070A-1TP	Device Control Interface	1	N/A	N/A
M8085A	M8085A-CT1	MIPI C-PHY Editor for M819xA AWG, Transportable, Perpetual License	1	N/A	N/A
M8085A	M8085A-CTA	MIPI C-PHY Calibration, Conformance and Characterization Procedures for M819xA AWG, transportable, perpetual License	1	N/A	N/A
M8085A	M8085A-CN1	MIPI C-PHY Editor for M819xA AWG, Network License	0	N/A	N/A
M8085A	M8085A-CNA	MIPI C-PHY Calibration, Conformance and Characterization Procedures for M819xA AWG, Network License	0	N/A	N/A
N5990A	N5990A-010	Bitifeye Test sequencer for M8085A Cxx options	1	N/A	N/A

Ordering a MIPI D-PHY RX Test Configuration

Complete n-Lane D-PHY Setup (HS, LP, and transitions, full compliance) using M8195A rev2 modules					
Number of D-PHY lanes			**1**	**2**	**4**
Product	**Option**	**Description**	**Quantity**		
M8195A	M8195A-BU1	AXIe Chassis: 5-slot with Integrated System Module plus Embedded Controller: Quad Core, 8GB RAM, 160 SSD, 2 GB/s	1	1	1
M8195A	M8195A-004	Arbitrary Waveform Generator, 4 Channels, 65 GSa/s	1	1	2
M8195A	M8195A-002	Arbitrary Waveform Generator, 2 Channels, 65 GSa/s	0	1	1
M8195A	M8195A-001	Arbitrary Waveform Generator, 1 Channel, 65 GSa/s	0	0	0
M8195A	M8195A-16G	Upgrade to 16 GSa Memory	1	2	3
M8195A	M8195A-SEQ	Sequencer	1	2	3
M8197A	N/A	AWG synchcronisation module	0	1	1
M8195A	R-50C-011-5	Calibration Assurance Plan - Return to Keysight - 5 years	0	0	0
M8195A	R-51B-001-5Z	Warranty Assurance Plan - Return to Keysight - 5 years	0	0	0
M8070A	M8070A-0TP	System Software for M8000 Series of BER Test Solutions, Transportable, Perpetual License	1	1	1
M8070A	M8070A-0NP	System Software for M8000 Series of BER Test Solutions, Network License	0	0	0
M8070A	M8070A-1TP	Device Control Interface	1	1	1
M8195A	M8195A-810	Matched Cable Pair for M8195A AWG, 2.92 mm	0	0	0
M8085A	M8085A-DT1	MIPI D-PHY Editor for M819xA AWG, Transportable, Perpetual License	1	1	1
M8085A	M8085A-DTA	MIPI D-PHY Calibration, Conformance and Characterization Procedures for M819xA AWG, transportable, perpetual License	1	1	1
M8085A	M8085A-DN1	MIPI D-PHY Editor for M819xA AWG, Network License	0	0	0
M8085A	M8085A-DNA	MIPI D-PHY Calibration, Conformance and Characterization Procedures for M819xA AWG, Network License	0	0	0
N5990A	N5990A-010	Bitifeye Test sequencer for M8085A Cxx options	1	1	1
Complete 1-Lane D-PHY Setup (HS, LP, and transitions, full compliance) using M8190A modules					
M8190A	M8190A-BU1	Bundle 1 consisting of M9505A AXIe Chassis w/ 5 slots and M9536A Embedded PC Controller	1	N/A	N/A
M8190A	M8190A-001	Arbitrary Waveform Generator 1 Channel	0	N/A	N/A
M8190A	M8190A-002	Arbitrary Waveform Generator 2 Channel	2	N/A	N/A
M8190A	M8190A-02G	Upgrade from 128Msa to 2GSa Memory/Channel	4	N/A	N/A
M8190A	M8190A-12G	12GSa/s with 12 bit resolution	2	N/A	N/A
M8190A	M8190A-14B	14 Bit resolution at 8GSa/s	0	N/A	N/A
M8190A	M8190A-AMP	Additional AC and DC Amplifier	2	N/A	N/A
M8190A	M8190A-SEQ	Sequencer	2	N/A	N/A
M8192A	N/A	Synchronization module for the M8190A	1	N/A	N/A
M8070A	M8070A-0TP	System Software for M8000 Series of BER Test Solutions, Transportable, Perpetual License	1	N/A	N/A
M8070A	M8070A-0NP	System Software for M8000 Series of BER Test Solutions, Network License	0	N/A	N/A
M8070A	M8070A-1TP	Device Control Interface	1	N/A	N/A
M8085A	M8085A-DT1	MIPI D-PHY Editor for M819xA AWG, Transportable, Perpetual License	1	1	1
M8085A	M8085A-DTA	MIPI D-PHY Calibration, Conformance and Characterization Procedures for M819xA AWG, transportable, perpetual License	1	1	1
M8085A	M8085A-DN1	MIPI D-PHY Editor for M819xA AWG, Network License	0	0	0
M8085A	M8085A-DNA	MIPI D-PHY Calibration, Conformance and Characterization Procedures for M819xA AWG, Network License	0	0	0
N5990A	N5990A-010	Bitifeye Test sequencer for M8085A Cxx options	1	N/A	N/A

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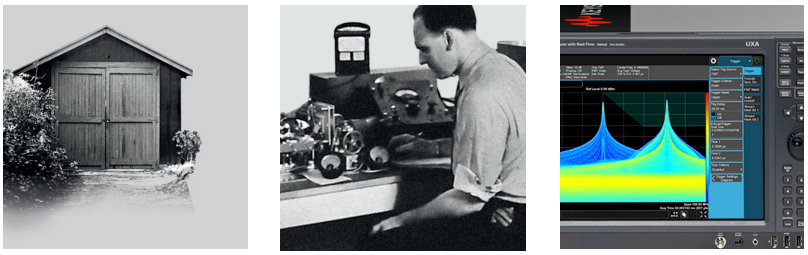

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