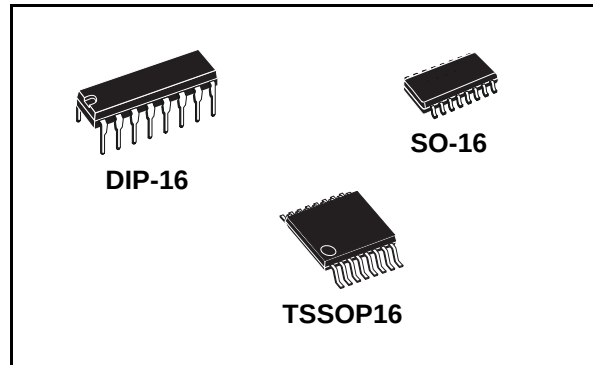


8-bit PISO shift register

Features

- High speed:
 - $t_{PD} = 15 \text{ ns}$ (typ.) at $V_{CC} = 6 \text{ V}$
- Low power dissipation:
 - $I_{CC} = 4 \mu\text{A}$ (max.) at $T_A = 25 \text{ }^\circ\text{C}$
- High noise immunity:
 - $V_{NIH} = V_{NIL} = 28 \% V_{CC}$ (Min.)
- Symmetrical output impedance:
 - $|I_{OH}| = I_{OL} = 4 \text{ mA}$ (min)
- Balanced propagation delays:
 - $t_{PLH} \cong t_{PHL}$
- Wide operating voltage range:
 - $V_{CC} \text{ (opr)} = 2 \text{ V to } 6 \text{ V}$
- Pin and function compatible with 74 series 165



Description

The M74HC165 is a high speed CMOS 8-bit PISO (parallel-in-serial-out) shift register fabricated with silicon gate C²MOS technology. This device contains eight clocked master slave RS flip-flops connected as a shift register, with auxiliary gating to provide overriding asynchronous parallel entry. The parallel data enter when the shift/load input is low and can change while shift/load is low, provided that the recommended set-up and hold times are observed. For clocked operation, shift/load must be high. The two clock inputs perform identically: one can be used as a clock inhibit by applying a high signal, to allow this operation clocking is accomplished through a 2-input nor gate. To avoid double clocking, however, the inhibit signal should only go high while the clock is high. Otherwise the rising inhibit signal causes the same response as rising clock edge. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Table 1. Device summary

Order code	Package	Packaging
M74HC165B1R	DIP-16	Tube
M74HC165RM13TR	SO-16	Tape and reel
M74HC165TTR	TSSOP16	Tape and reel

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1 Logic symbols and I/O equivalent circuit

Figure 1. IEC logic symbols

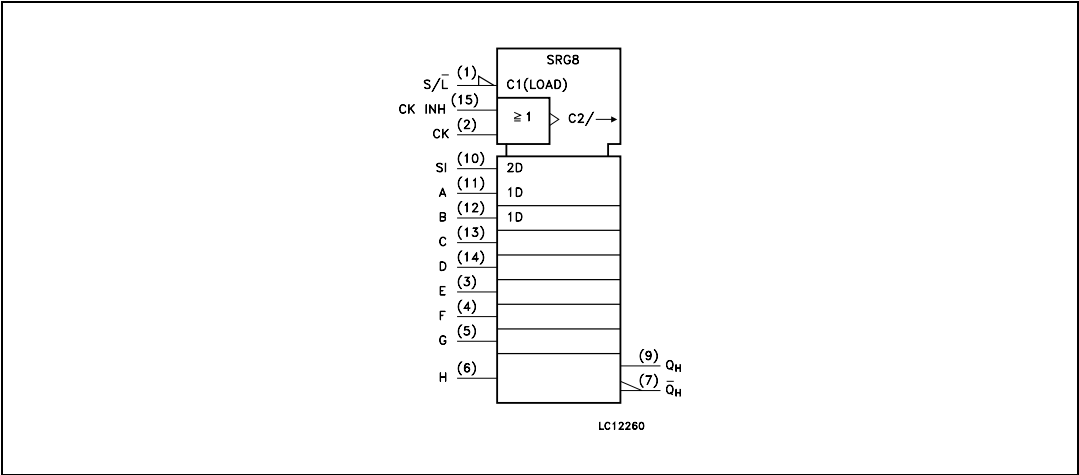
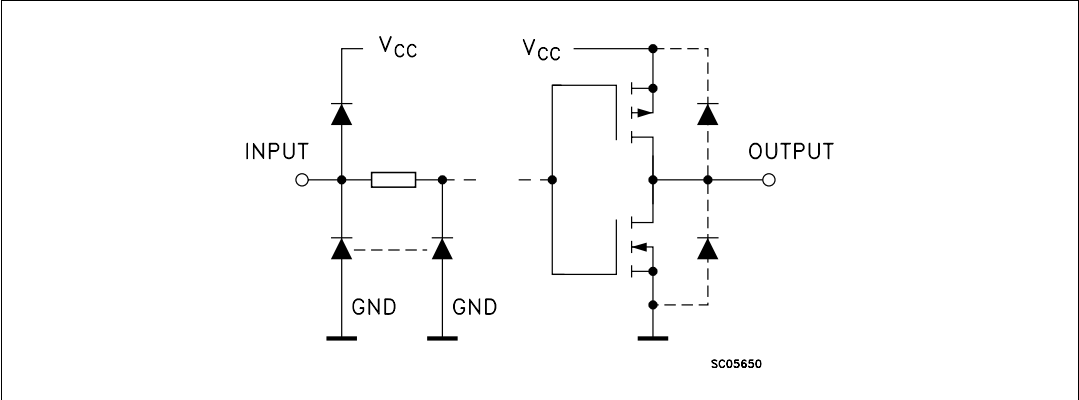


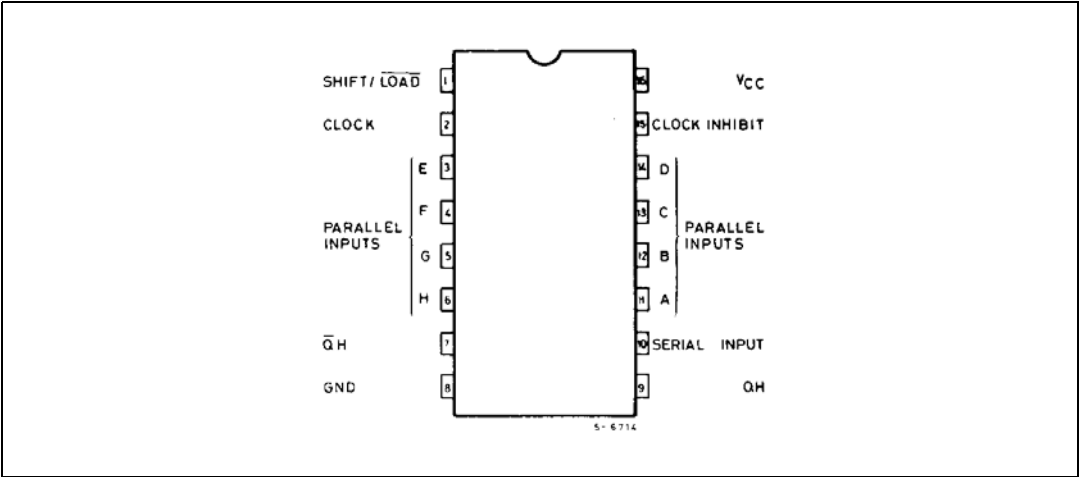
Figure 2. Input and output equivalent circuit



2 Pin settings

2.1 Pin connection

Figure 3. Pin connection (top through view)



2.2 Pin description

Table 2. Pin description

Pin number	Symbol	Name and function
1	SHIFT/LOAD	Data inputs
2	CLOCK	Clock input (low to high, edge triggered)
7	$\overline{QH}$	Complementary output
9	QH	Serial output
10	SI	Serial input
11, 12, 13, 14, 3, 4, 5, 6	A to H	Parallel data inputs
15	CLOCK INH	Clock inhibit
8	GND	Ground (0 V)
16	V_{CC}	Positive supply voltage

3 Logic states

3.1 Truth table

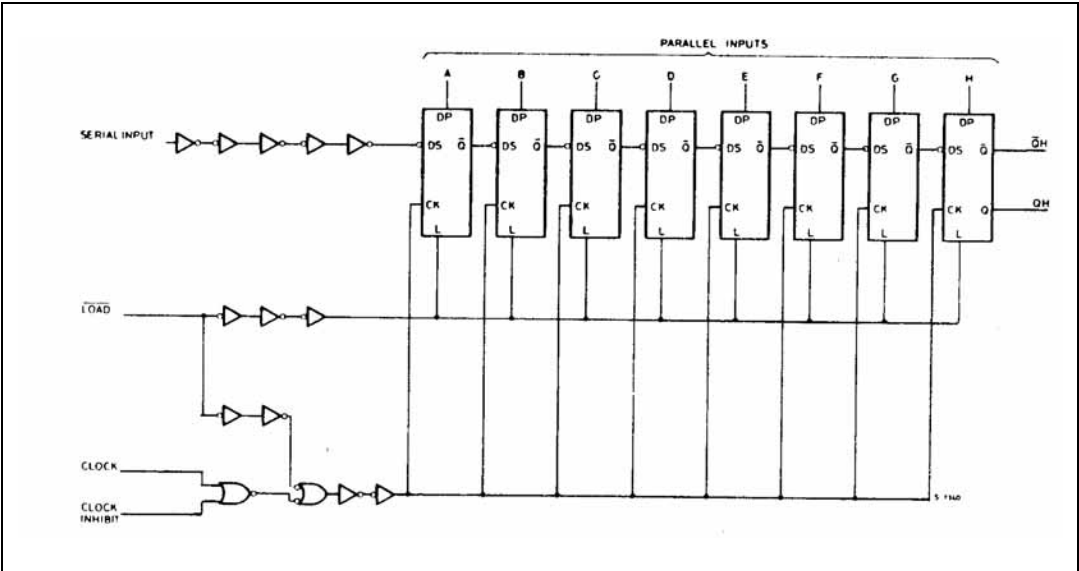
Table 3. Truth table

Inputs					Internal outputs		Outputs
Shift /Load	Clock INH	Clock	SI	A.....H	QA	QB	QH
L	X	X	X	a.....h	a	b	h
H	L		H	X	H	QAn	QGn
H	L		L	X	L	QAn	QGn
H		L	H	X	H	QAn	QGn
H		L	L	X	L	QAn	QGn
H	X	H	X	X	No change		
H	H	X	X	X	No change		

Note: a.....h : the level of steady input voltage at inputs a through respectively QAn - QGn : the level of QA - QG, respectively. Before the most recent transition of the clock.

3.2 Logic diagram

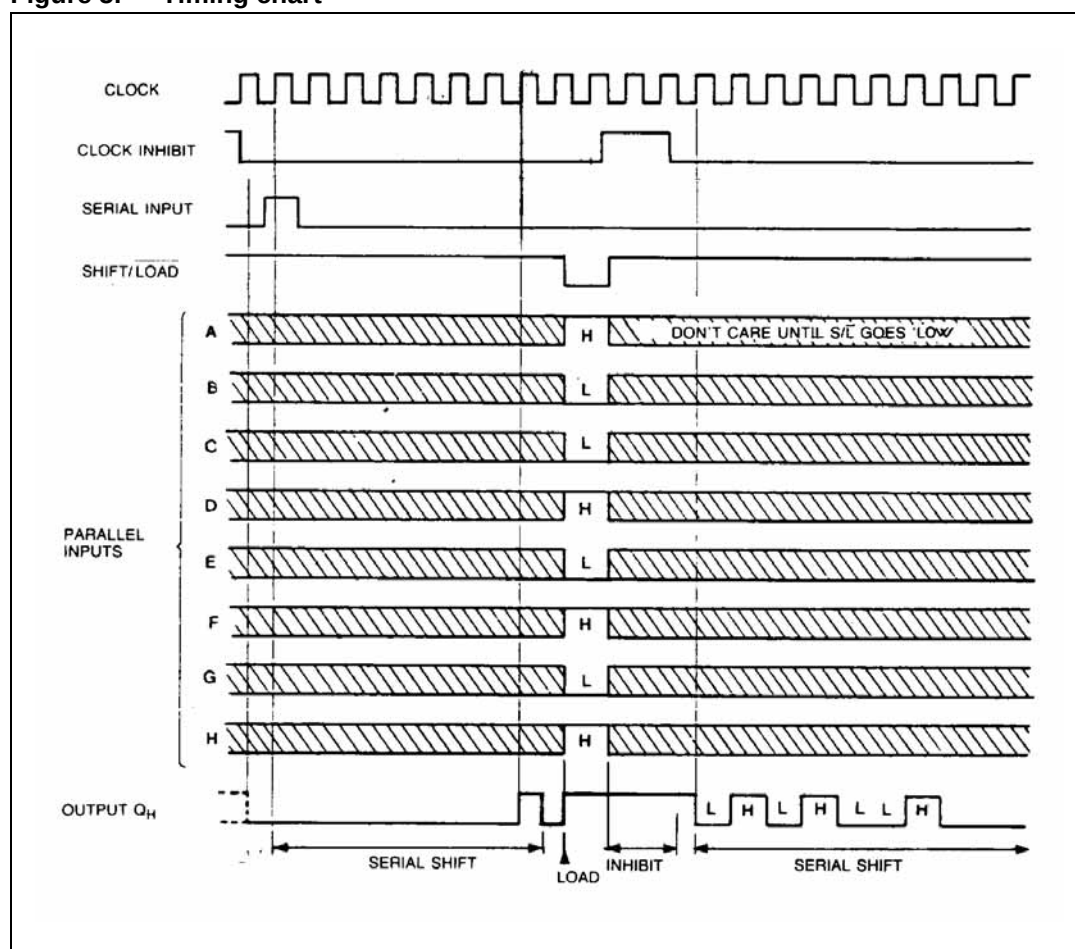
Figure 4. Logic diagram



Note: This logic diagram has not to be used to estimate propagation delays

3.3 Timing chart

Figure 5. Timing chart



4 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. these are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. exposure to absolute maximum rating conditions for extended periods may affect device reliability. refer also to the STMicroelectronics sure program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +7	V
V_I	DC input voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC output voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC input diode current	± 20	mA
I_{OK}	DC output diode current	± 20	mA
I_O	DC output current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	± 50	mA
P_D	Power dissipation	500 ⁽¹⁾	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	300	°C

1. (*) 500 mW at 65 °C; derate to 300 mW by 10 mW/°C from 65°C to 85°C

4.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbols	Parameter		Value	Unit
V _{CC}	Supply voltage		2 to 6	V
V _I	Input voltage		0 to V _{CC}	V
V _O	Output voltage		0 to V _{CC}	V
T _{op}	Operating temperature		-55 to 125	°C
t _r , t _f	Input rise and fall time	V _{CC} = 2.0 V	0 to 1000	ns
		V _{CC} = 4.5 V	0 to 500	ns
		V _{CC} = 6.0 V	0 to 400	ns

5 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test condition		Value								Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C			
				Min	Typ	Max	Min	Max	Min	Max		
V _{IH}	High level input voltage	2.0		1.5			1.5		1.5		V	
		4.5		3.15			3.15		3.15			
		6.0		4.2			4.2		4.2			
V _{IL}	Low level input voltage	2.0				0.5		0.5		0.5	V	
		4.5				1.35		1.35		1.35		
		6.0				1.8		1.8		1.8		
V _{OH}	High level output voltage	2.0	I _O = -20 μA	1.9	2.0		1.9		1.9		V	
		4.5	I _O = -20 μA	4.4	4.5		4.4		4.4			
		6.0	I _O = -20 μA	5.9	6.0		5.9		5.9			
		4.5	I _O = -4.0 mA	4.18	4.31		4.13		4.10			
		6.0	I _O = -5.2 mA	5.68	5.8		5.63		5.60			
V _{OL}	Low level output voltage	2.0	I _O = 20 μA		0.0	0.1		0.1		0.1	V	
		4.5	I _O = 20 μA		0.0	0.1		0.1		0.1		
		6.0	I _O = 20 μA		0.0	0.1		0.1		0.1		
		4.5	I _O = 4.0 mA		0.17	0.26		0.33		0.40		
		6.0	I _O = 5.2 mA		0.18	0.26		0.33		0.40		
I _I	Input leakage current	6.0	V _I = V _{CC} or GND			±0.1		±1		±1	μA	
I _{CC}	Quiescent supply current	6.0	V _I = V _{CC} or GND			4		40		80	μA	

Table 7. AC electrical characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	Test condition		Value							Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min	Typ	Max	Min	Max	Min	Max	
t _{TLH} t _{THL}	Output transition time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t _{PLH} t _{PHL}	Propagation delay time (CLOCK - QH, $\overline{QH}$)	2.0			55	150		190		225	ns
		4.5			18	30		38		45	
		6.0			15	26		33		38	
t _{PLH} t _{PHL}	Propagation delay time (SHIFT/ $\overline{LOAD}$ - QH, $\overline{QH}$)	2.0			65	165		205	250		ns
		4.5			21	33		41		50	
		6.0			18	28		35		43	
t _{PLH} t _{PHL}	Propagation delay time (H - QH, $\overline{QH}$)	2.0			52	135		170		205	ns
		4.5			17	27		34		41	
		6.0			14	23		29		35	
f _{MAX}	Maximum clock frequency	2.0		7.4	15		6.0		4.8		MHz
		4.5		37	60		30		24		
		6.0		44	71		35		28		
t _{W(H)} t _{W(L)}	Minimum pulse width (CLOCK)	2.0			24	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
t _{W(L)}	Minimum pulse width (SHIFT/ $\overline{LOAD}$)	2.0			32	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t _s	Minimum set-up time (PI - SHIFT/ $\overline{LOAD}$) (SI - CLOCK) (SHIFT/ $\overline{LOAD}$ - CK)	2.0			24	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
t _h	Minimum hold time (PI - SHIFT/ $\overline{LOAD}$) (SI - CLOCK) (SHIFT/ $\overline{LOAD}$ - CK)	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t _{REM}	Minimum removal time (CLOCK - CK INH)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	

Table 8. Capacitive characteristics

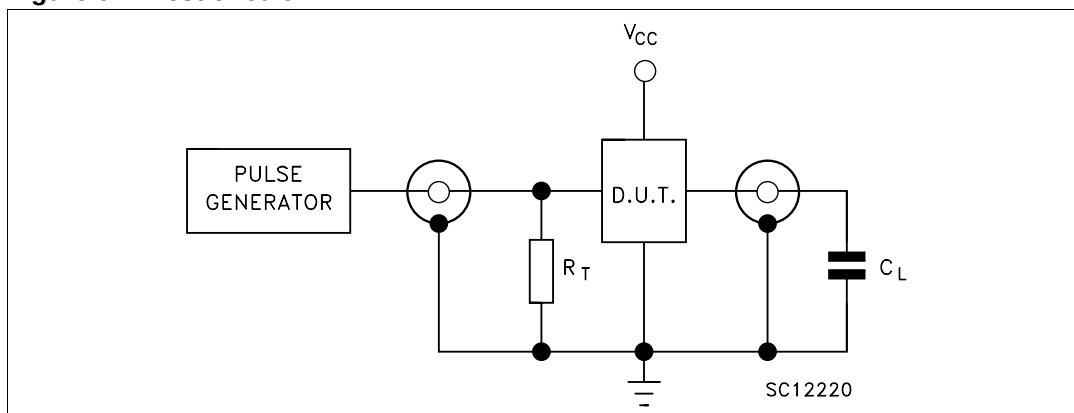
Symbol	Parameter	Test condition		Value						Unit	
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		-55 to 125 °C		
				Min	Typ	Max	Min	Max	Min		Max
C _{IN}	Input capacitance	5.0			5	10		10		10	pF
C _{PD}	Power dissipation capacitance ⁽¹⁾	5.0			55						pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$$

6 Test circuit

Figure 6. Test circuit



$C_L = 50 \text{ pF}$ or equivalent (includes jig and probe capacitance)

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

7 Waveforms

Figure 7. Serial mode propagation delay ($f = 1\text{ MHz}$; 50% duty cycle)

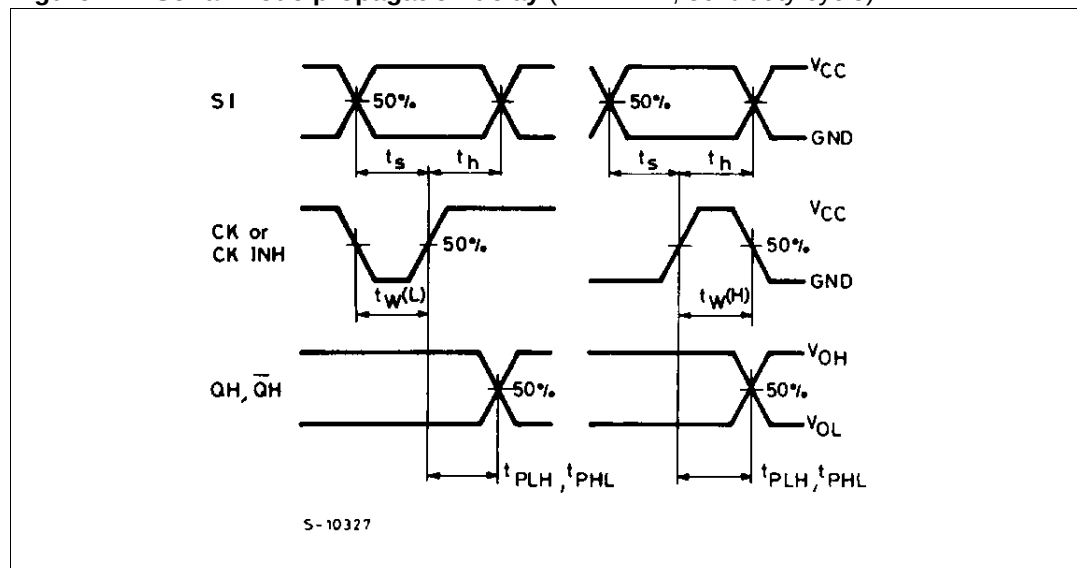


Figure 8. Parallel mode propagation delay ($f = 1\text{ MHz}$; 50% duty cycle)

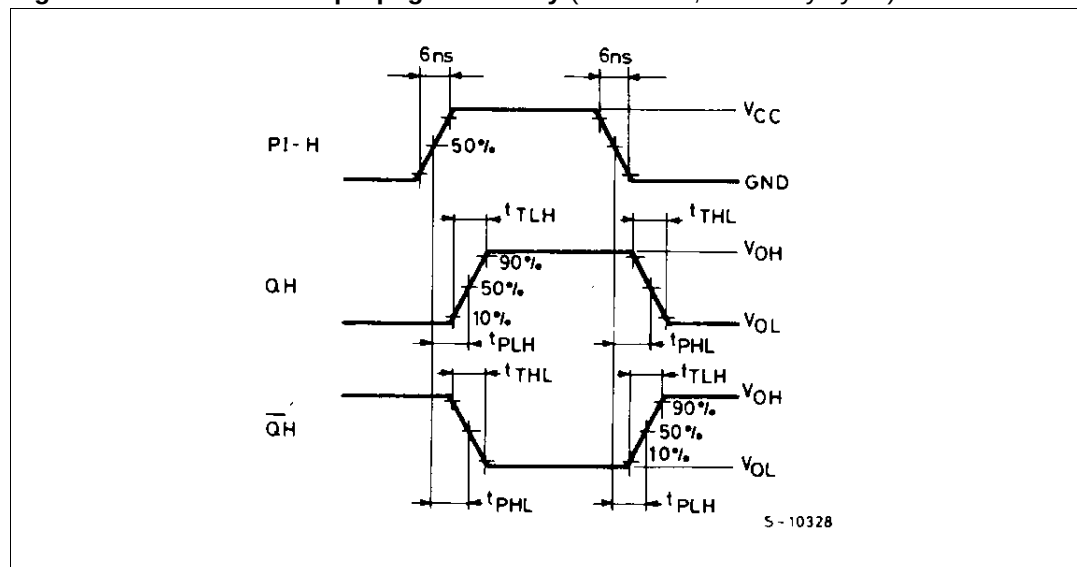


Figure 9. Minimum pulse width ($S/\bar{L}$), propagation delay times
($f = 1\text{ MHz}$; 50% duty cycle)

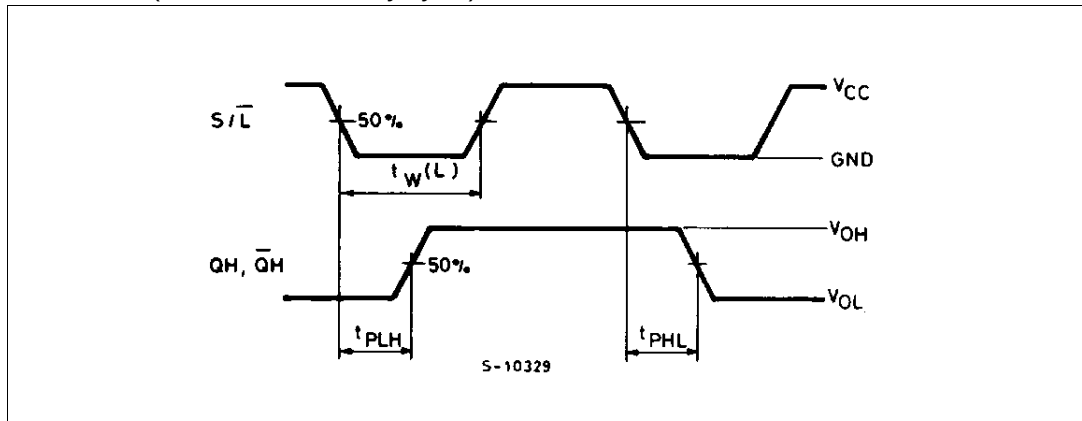


Figure 10. Setup and hold time (PI to $S/\bar{L}$) ($f = 1\text{ MHz}$; 50% duty cycle)

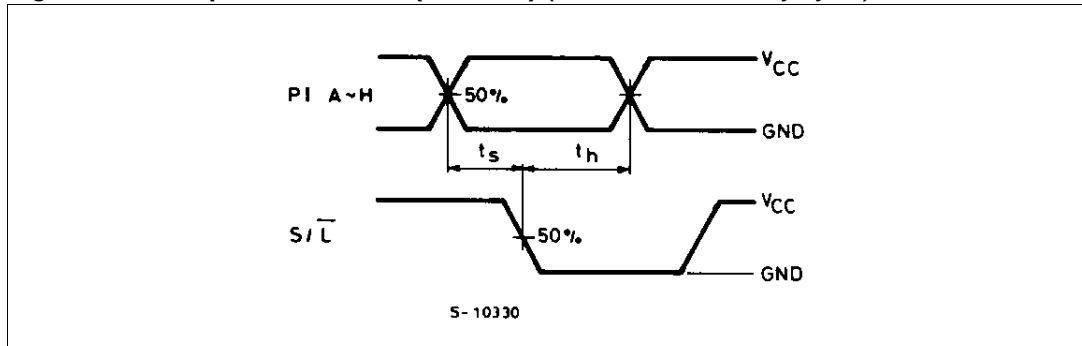
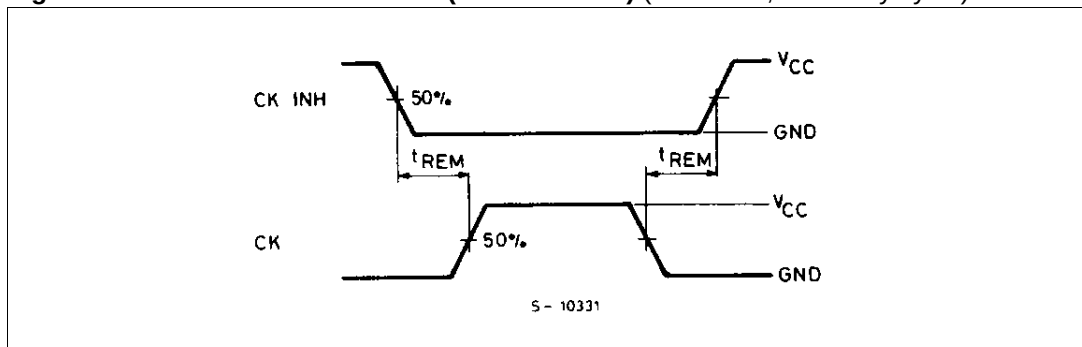
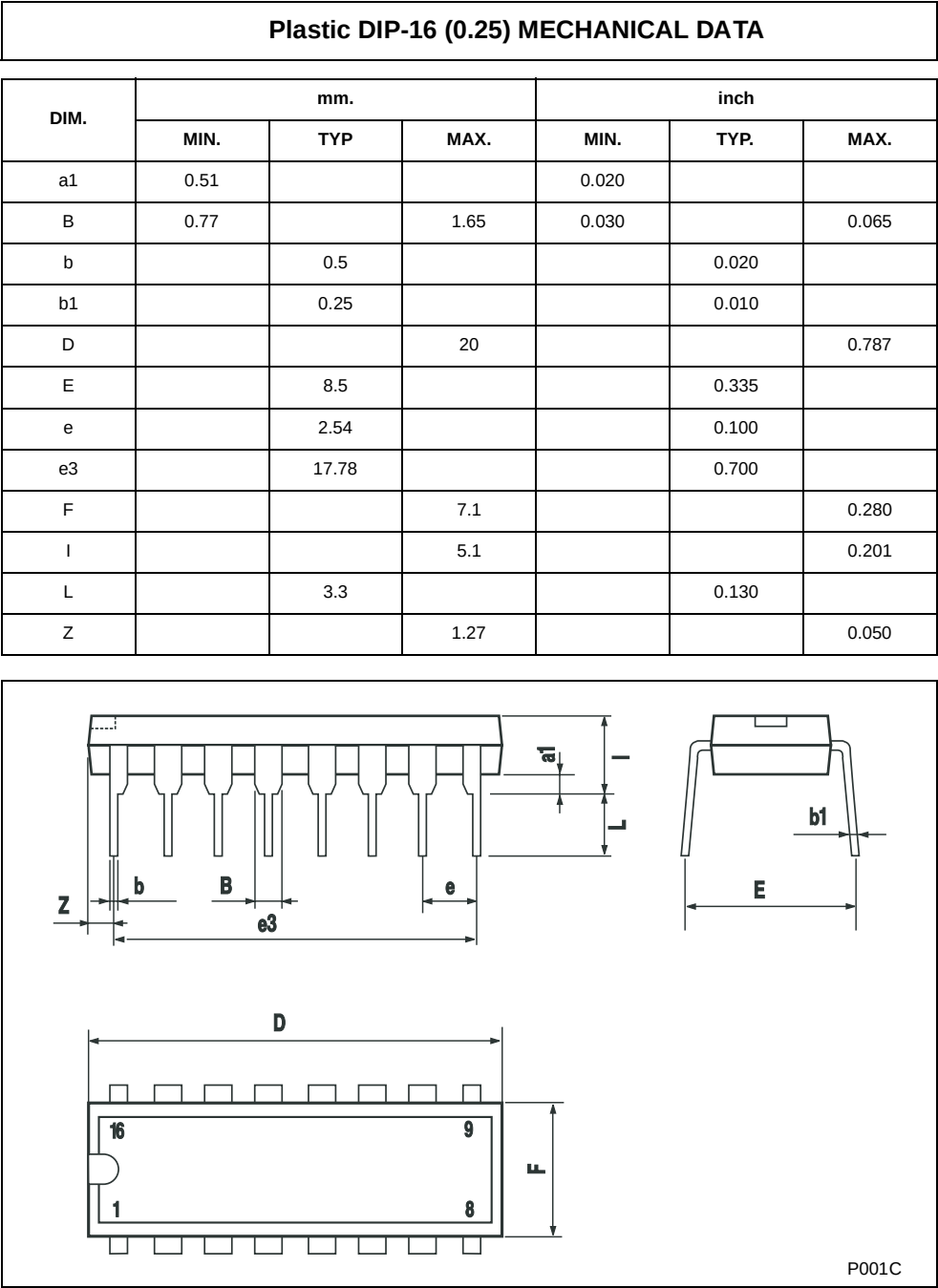


Figure 11. Minimum removal time ($CK\ INH$ to CK) ($f = 1\text{ MHz}$; 50% duty cycle)



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

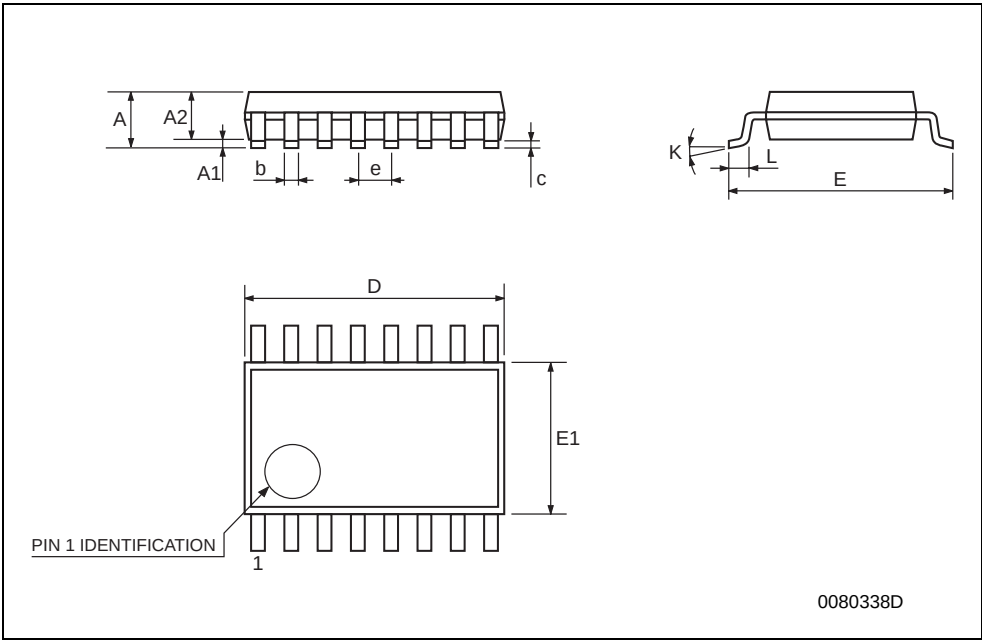


SO-16 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					

The diagram illustrates the mechanical specifications of the SO-16 package through three views: top, side, and end. The top view shows a rectangular package with pins on all four sides, with dimensions D (total width), E (pin pitch), and F (pin length). Pin numbers 1, 8, 9, and 16 are indicated at the corners. The side view shows the package height A, pin height a1, and pin width b1. The end view shows the package width b, pin pitch e, and total pin length e3. A detail view of the pin shows the lead length L, pin width G, and the 45-degree lead angle c1. The package is identified by the code 0016020D.

TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Tape & Reel SO-16 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.45		6.65	0.254		0.262
Bo	10.3		10.5	0.406		0.414
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

The mechanical drawing illustrates the M74HC165 package in three views: top, side, and detail. The top view shows a circular package with a central pin 1 indicator. Dimensions A (overall diameter), D (pin diameter), and C (pin pitch) are indicated. The side view shows the package height with dimensions N (total height) and T (lead height). The detail view shows the lead profile with dimensions Bo (lead width), Ko (lead thickness), Ao (lead spacing), Po (lead pitch), and P (lead width). A note at the bottom right states: 'Note: Drawing not in scale'.

Tape & Reel SSOP16 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.4		8.6	0.331		0.339
Bo	6.7		6.9	0.264		0.272
Ko	2.9		3.1	0.114		0.122
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

The diagram illustrates the mechanical specifications of the SSOP16 package. It includes three views: a top view showing the circular package body with diameter A and a central pin diameter D; a side view showing the package height N, lead thickness T, and lead length C; and a detail view of the lead profile showing dimensions Bo (lead thickness), Ko (lead width), Ao (lead pitch), Po (lead spacing), and P (lead width). The drawing is not to scale.

Note: Drawing not in scale

9 Revision history

Table 9. Document revision history

Date	Revision	Changes
9-Jul-2001	3	Final release.
21-Mar-2007	4	The document has been reformatted, updated Table 2: Pin description on page 4
26-May-2008	5	Removed: M74HC165M1R order code. Minor changes in the text. Added: SO-16 and TSSOP16 tape and reel specifications.

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