GENERAL DESCRIPTION



The M672 is a Voltage Controlled SAW Oscillator (VCSO) with a selectable output frequency divider. The output frequency can be pin-selected to be either the VCSO fundamental frequency (Fvcso) or a fraction of Fvcso ($^1/_8$, $^1/_4$, or $^1/_2$ depending on frequency and order code). Available center fundamental frequencies for the VCSO are between 125 and 700MHz. Divided Fvcso frequencies are in the 60 to 175MHz range. The M672 SAW (surface acoustic wave) VCO is a high Q frequency source for low-jitter clock generation. It is well suited for phase-locked loop implementations, clock and data recovery circuits, and other timing applications in telecom and optical fiber networking systems (e.g., SONET/SDH).

FEATURES

- **Selectable divider chooses one of two output frequencies; the Fvcso or its divided output frequency**
- **Low phase jitter 0.2ps rms typical (50kHz to 80MHz)**
- **Differential 3.3V LVPECL output**
- **Single 3.3V power supply**
- **Small 5 x 7.5mm SMT (surface mount) package**

PIN ASSIGNMENT (5 x 7.5mm SMT)

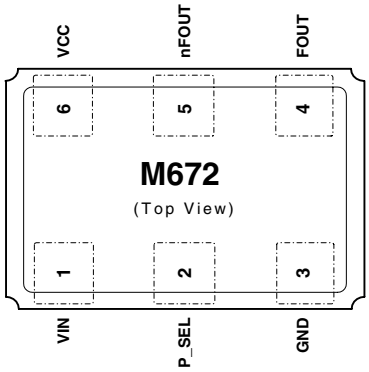


Figure 1: Pin Assignment

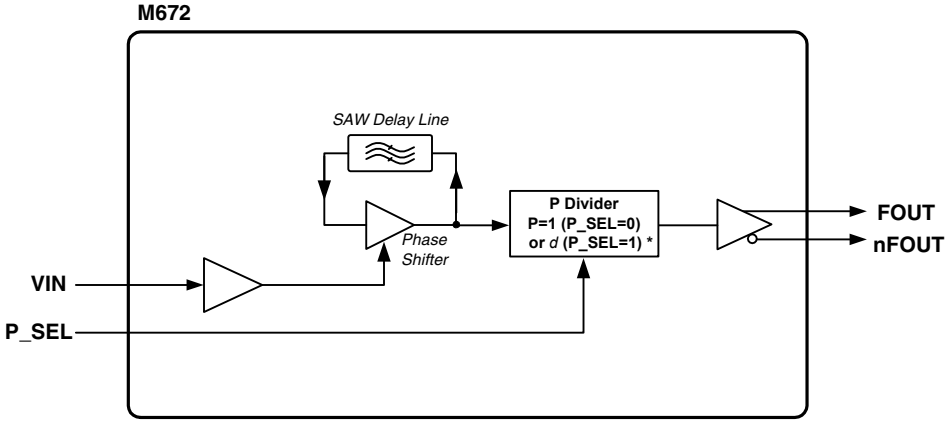
Sample of Available Output Frequencies

VCSO Center Fundamental Frequency[1] (MHz)	Corresponding P Divider[1]	Output Frequency Selections (MHz)
622.0800	4	622.0800, 155.5200
622.0800	8	622.0800, 77.7600
311.0400	2	311.0400, 155.5200
155.5200	2	155.5200, 77.7600

Table 1: Sample of Available Output Frequencies

Note 1: Specify VCSO center frequency and valid corresponding P divider value at time of order. See Ordering Information on pg. 4.

BLOCK DIAGRAM



* The P divider value *d* (4, 8, or 2) is specified as part of the order number (format is M672-*d*-*xx*).

Figure 2: Block Diagram

PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1	VIN	Input		Frequency control input.
2	P_SEL	Input	Internal pull-up resistor[1]	P Divider selection: Logic 0 selects P=1, so that Fout = Fvcso. Logic 1 selects P=*d*, so that Fout = 1/*d* Fvcso.[2]
3	GND	Ground		Power supply ground connection.
4 5	FOUT nFOUT	Output	No internal terminator	Clock output pair. Differential LVPECL.
6	VCC	Power		Power supply connection, connect to +3.3V.

Table 2: Pin Descriptions

Note 1: See “P Select Pull-up” in Table 5, DC Characteristics on pg. 3.

Note 2: The P divider value *d* (4, 8, or 2) is specified as part of the order number. Format is M672-d-xx. See Ordering Information on pg. 4.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_I	Inputs	-0.5 to V_{CC} +0.5	V
V_O	Outputs	-0.5 to V_{CC} +0.5	V
V_{CC}	Power Supply Voltage	4.6	V
T_S	Storage Temperature	-55 to +125	°C

Table 3: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Positive Supply Voltage	2.97	3.3	3.63	V
T_A	Ambient Operating Temperature	-40	25	+85	°C

Table 4: Recommended Conditions of Operation

PARAMETER MEASUREMENT INFORMATION

Output Rise and Fall Time

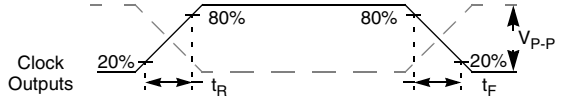


Figure 3: Output Rise and Fall Time

Output Duty Cycle

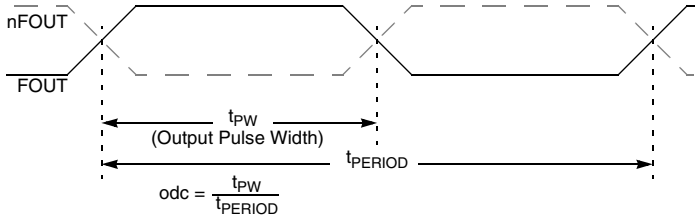


Figure 4: Output Duty Cycle

ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, V_{CC} = 3.3 Volts ± 10%, T_A = 0 to 85 °C, Fvcso = 622.08, 311.04, or 155.52 MHz, Outputs terminated into 180Ω to ground

	Symbol	Parameter	Pin	Min	Typ	Max	Unit
Power Supply	V_{CC}	Positive Supply Voltage	VCC	2.97	3.3	3.63	V
	I_{CC}	Power Supply Current			85	125	mA
Control Voltage	V_{IN}	Input Control Voltage Range	VIN	0		3.3	V
		V_{IN} Input Impedence			100		kΩ
P Select Pull-up[1]	V_{IH}	Input High Voltage	P_SEL	2		V_{CC} + 0.3	V
	V_{IL}	Input Low Voltage		-0.3		0.8	V
	I_{IH}	Input High Current				5	µA
	I_{IL}	Input Low Current		-150			µA
	R_{pullup}	Internal Pull-up Resistor			51		kΩ
Differential Outputs	V_{OH}	Output High Voltage	FOUT, nFOUT	V_{CC} - 0.98		V_{CC} - 0.75	V
	V_{OL}	Output Low Voltage		V_{CC} - 1.95		V_{CC} - 1.63	V
	V_{P-P}	Peak to Peak Output Voltage[2]		0.450	0.625	0.85	V_{P-P}
	I_{OUT}	Output Current				20	mA

Table 5: DC Characteristics

Note 1: Internally pulled up to Logic 1 (Fout = $^1/_d$ Fvcso) if left unselected.
Note 2: Single-ended measurement. See Figure 3, Output Rise and Fall Time, on pg. 2.

AC Characteristics

Unless stated otherwise, V_{CC} = 3.3 Volts ± 10%, T_A = 0 to 85 °C, Fvcso = 622.08, 311.04, or 155.52 MHz, Outputs terminated into 180Ω to ground

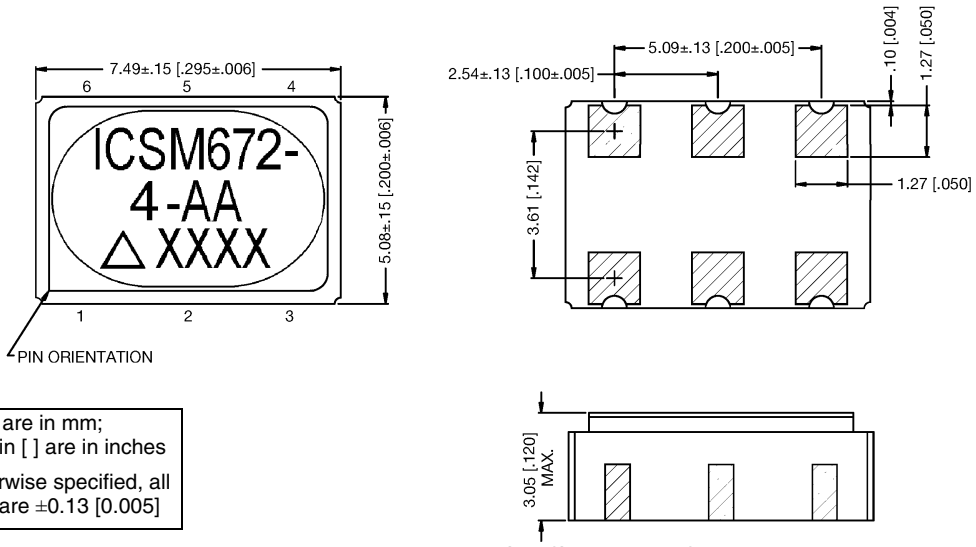
	Symbol	Parameter		Min	Typ	Max	Unit	Notes
Control Voltage	V_{IN}	Modulation Bandwidth	VIN		500		kHz	
Output	F_{OUT}	Output Frequency Range		60		700	MHz	
	APR	Absolute (Guaranteed) Pull-Range [1]		±100			ppm	
	f_{STAB}	Frequency Stability			100		ppm p-p	At any givin V_{IN}
	L_{IN}	Tuning Linearity			6		%	V_{IN} = 0.3 to 3.0V Best fit straight line
	K_{VCO}	VCO Gain @622.08MHz			400		ppm/V	V_{IN} = 0.3 to 3.0V
		Non-harmonic Spurious		-50	-77		dBc	
	Φn	SSB (single sideband) Phase Noise, offset from carrier @622.08MHz	100Hz Offset		-48		dBc/Hz	
			1kHz Offset		-75		dBc/Hz	
			10kHz Offset		-99		dBc/Hz	
			100kHz Offset		-124		dBc/Hz	
			1MHz Offset		-142		dBc/Hz	
	J(t)	Jitter (rms) @622.08MHz	12kHz to 20MHz		0.30		ps rms	
			50kHz to 80MHz		0.18		ps rms	
	odc	Output Duty Cycle [2]		45		55	%	
	t_R	Output Rise Time [2] for FOUT, nFOUT			275	425	ps	20% to 80%
	t_F	Output Fall Time [2] for FOUT, nFOUT			275	425	ps	20% to 80%

Table 6: AC Characteristics

Note 1: Also fully meets ±50 ppm minimum pull-range specification that is commonly required.
Note 2: See Parameter Measurement Information on pg. 2.

DEVICE PACKAGE - 5 x 7.5mm SMT (Surface Mount) Package

Mechanical Dimensions:



Dimensions are in mm;
dimensions in [ ] are in inches

Unless otherwise specified, all dimensions are ±0.13 [0.005]

Figure 5: Device Package - 5 x 7.5mm SMT (Surface Mount) Package

ORDERING INFORMATION

Part Numbering Scheme

Part Number: **M672-d-xx**

Device Number

P Divider Value
See Table 7 at right for valid "d " values for particular frequency order codes.

VCSO Output Frequency Order Code
See Table 7 at right for valid frequency order codes.

Consult ICS for other frequencies and order codes.

Figure 6: Part Numbering Scheme

Standard Output Frequencies & Order Codes

VCSO Center Fundamental Frequency (MHz)	Divided Frequency	P Divider	Order Part #
622.0800	155.5200	4	**M672-4-AA**
622.0800	77.7600	8	**M672-8-AA**
311.0400	155.5200	2	**M672-2-AZ**
155.5200	77.7600	2	**M672-2-BA**

Table 7: Standard Output Frequencies & Order Codes

Consult ICS for the availability of other frequencies

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