M66256FP

5120 × 8-Bit Line Memory (FIFO)

REJ03F0250-0200
Rev.2.00
Sep 14, 2007

Description

The M66256FP is a high-speed line memory with a FIFO (First In First Out) structure of 5120-word × 8-bit configuration which uses high-performance silicon gate CMOS process technology.

It has separate clock, enable and reset signals for write and read, and is most suitable as a buffer memory between devices with different data processing throughput.

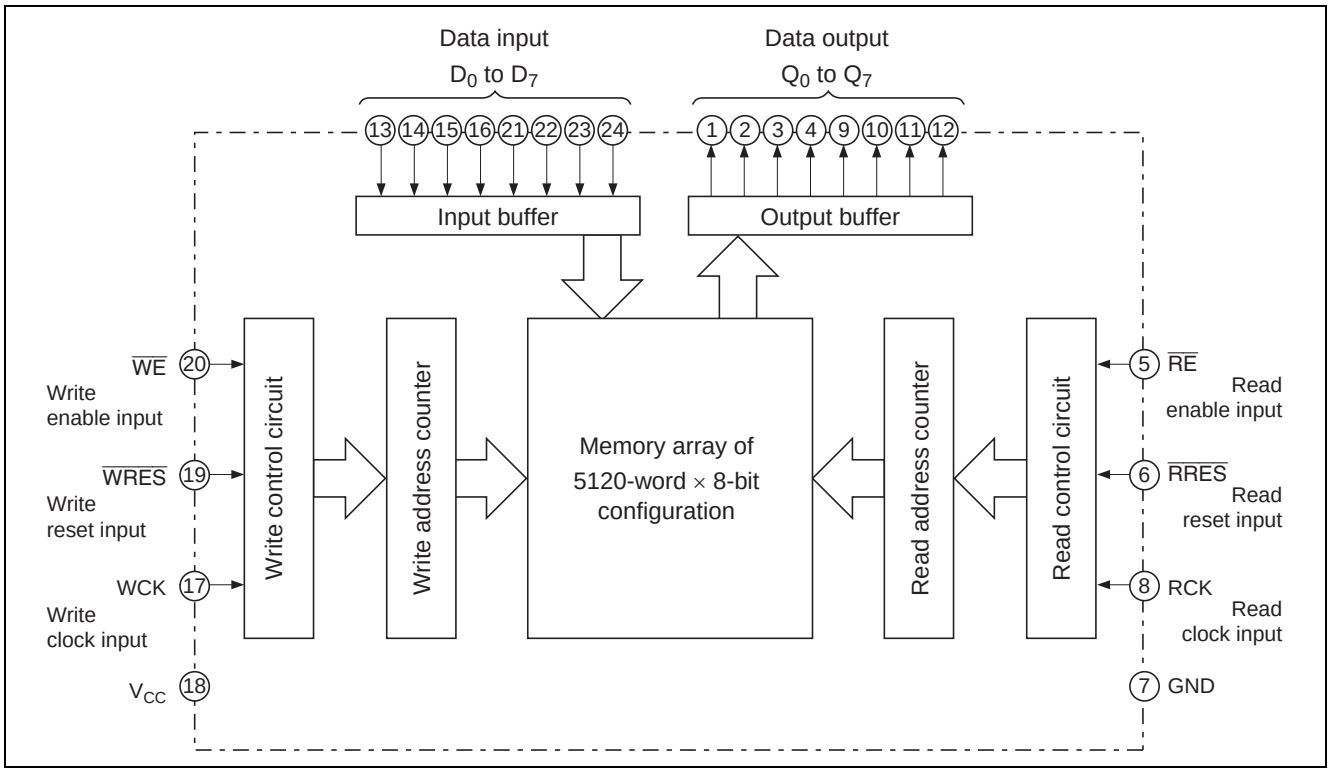
Features

- Memory configuration: 5120 words × 8 bits (dynamic memory)
- High-speed cycle: 25 ns (Min)
- High-speed access: 18 ns (Max)
- Output hold: 3 ns (Min)
- Fully independent, asynchronous write and read operations
- Variable length delay bit
- Output: 3 states

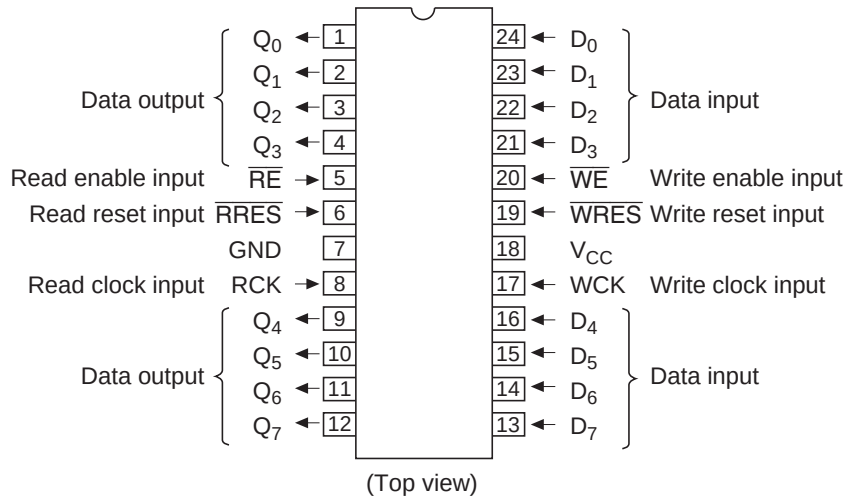
Application

Digital photocopiers, high-speed facsimile, laser beam printers.

Block Diagram



Pin Arrangement



Outline: 24P2U-A

Absolute Maximum Ratings

(Ta = 0 to 70°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to +7.0	V	A value based on GND pin
Input voltage	V_I	–0.5 to V_{CC} + 0.5	V	
Output voltage	V_O	–0.5 to V_{CC} + 0.5	V	
Power dissipation	Pd	440	mW	Ta = 25°C
Storage temperature	Tstg	–65 to 150	°C	

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5	5.5	V
Supply voltage	GND	—	0	—	V
Operating ambient temperature	Topr	0	—	70	°C

Electrical Characteristics

(Ta = 0 to 70°C, V_{CC} = 5 V ± 10%, GND = 0 V)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
"H" input voltage	V_{IH}	2.0	—	—	V		
"L" input voltage	V_{IL}	—	—	0.8	V		
"H" output voltage	V_{OH}	V_{CC} – 0.8	—	—	V	I_{OH} = –4 mA	
"L" output voltage	V_{OL}	—	—	0.55	V	I_{OL} = 4 mA	
"H" input current	I_{IH}	—	—	1.0	µA	$V_I = V_{CC}$	$\overline{WE}$, $\overline{WRES}$, WCK, $\overline{RE}$, $\overline{RRES}$, RCK, D_0 to D_7
"L" input current	I_{IL}	—	—	–1.0	µA	V_I = GND	$\overline{WE}$, $\overline{WRES}$, WCK, $\overline{RE}$, $\overline{RRES}$, RCK, D_0 to D_7
Off state "H" output current	I_{OZH}	—	—	5.0	µA	$V_O = V_{CC}$	
Off state "L" output current	I_{OZL}	—	—	–5.0	µA	V_O = GND	
Operating mean current dissipation	I_{CC}	—	—	80	mA	$V_I = V_{CC}$, GND, Output open t_{WCK}, t_{RCK} = 25 ns	
Input capacitance	C_I	—	—	10	pF	f = 1 MHz	
Off state output capacitance	C_O	—	—	15	pF	f = 1 MHz	

Function

When write enable input $\overline{WE}$ is "L", the contents of data inputs D_0 to D_7 are written into memory in synchronization with rise edge of write clock input WCK. At this time, the write address counter is also incremented simultaneously.

The write function given below are also performed in synchronization with rise edge of WCK.

When $\overline{WE}$ is "H", a write operation to memory is inhibited and the write address counter is stopped.

When write reset input $\overline{WRES}$ is "L", the write address counter is initialized.

When read enable input $\overline{RE}$ is "L", the contents of memory are output to data outputs Q_0 to Q_7 in synchronization with rise edge of read clock input RCK. At this time, the read address counter is also incremented simultaneously.

The read functions given below are also performed in synchronization with rise edge of RCK.

When $\overline{RE}$ is "H", a read operation from memory is inhibited and the read address counter is stopped. The outputs are in the high impedance state.

When read reset input $\overline{RRES}$ is "L", the read address counter is initialized.

Switching Characteristics

($Ta = 0$ to 70°C, $V_{CC} = 5\ V \pm 10\%$, GND = 0 V)

Item	Symbol	Min	Typ	Max	Unit
Access time	t_{AC}	—	—	18	ns
Output hold time	t_{OH}	3	—	—	ns
Output enable time	t_{OEN}	3	—	18	ns
Output disable time	t_{ODIS}	3	—	18	ns

Timing Conditions

($Ta = 0$ to 70°C, $V_{CC} = 5\ V \pm 10\%$, GND = 0 V, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit
Write clock (WCK) cycle	t_{WCK}	25	—	—	ns
Write clock (WCK) "H" pulse width	t_{WCKH}	11	—	—	ns
Write clock (WCK) "L" pulse width	t_{WCKL}	11	—	—	ns
Read clock (RCK) cycle	t_{RCK}	25	—	—	ns
Read clock (RCK) "H" pulse width	t_{RCKH}	11	—	—	ns
Read clock (RCK) "L" pulse width	t_{RCKL}	11	—	—	ns
Input data setup time to WCK	t_{DS}	7	—	—	ns
Input data hold time to WCK	t_{DH}	3	—	—	ns
Reset setup time to WCK or RCK	t_{RESS}	7	—	—	ns
Reset hold time to WCK or RCK	t_{RESH}	3	—	—	ns
Reset nonselect setup time to WCK or RCK	t_{NRESS}	7	—	—	ns
Reset nonselect hold time to WCK or RCK	t_{NRESH}	3	—	—	ns
$\overline{WE}$ setup time to WCK	t_{WES}	7	—	—	ns
$\overline{WE}$ hold time to WCK	t_{WEH}	3	—	—	ns
$\overline{WE}$ nonselect setup time to WCK	t_{NWES}	7	—	—	ns
$\overline{WE}$ nonselect hold time to WCK	t_{NWEH}	3	—	—	ns
$\overline{RE}$ setup time to RCK	t_{RES}	7	—	—	ns
$\overline{RE}$ hold time to RCK	t_{REH}	3	—	—	ns
$\overline{RE}$ nonselect setup time to RCK	t_{NRES}	7	—	—	ns
$\overline{RE}$ nonselect hold time to RCK	t_{NREH}	3	—	—	ns
Input pulse rise/fall time	tr, tf	—	—	20	ns
Data hold time*	t_H	—	—	20	ms

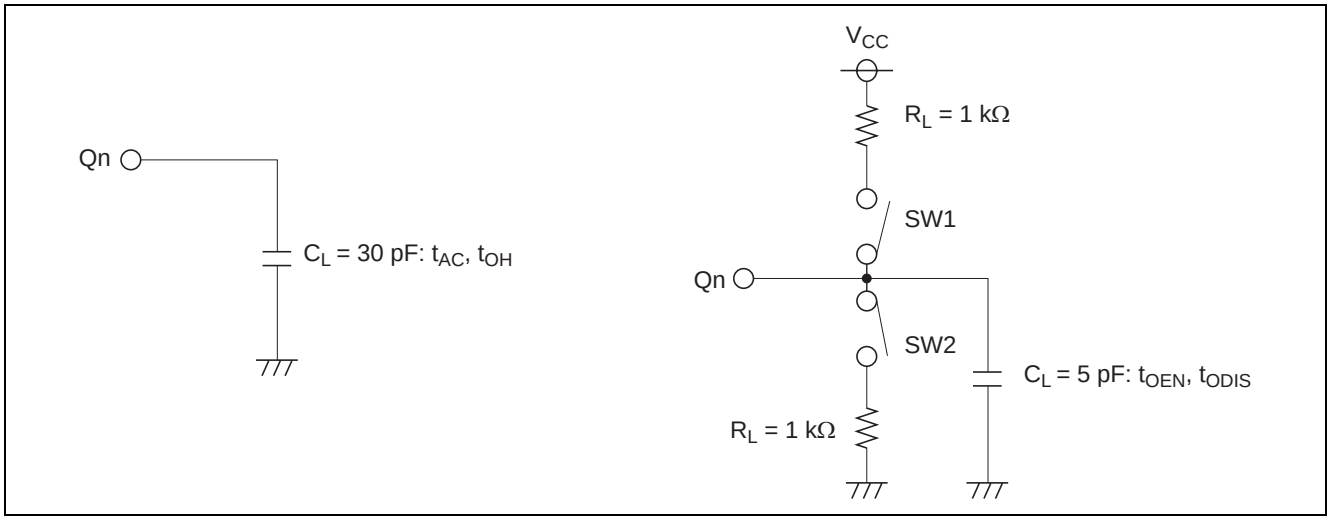
Notes: Perform reset operation after turning on power supply.

* For 1-line access, the following should be satisfied:

$\overline{WE}$ "H" level period ≤ 20 ms − 5120 t_{WCK} − $\overline{WRES}$ "L" level period

$\overline{RE}$ "H" level period ≤ 20 ms − 5120 t_{RCK} − $\overline{RRES}$ "L" level period

Test Circuit



Input pulse level: 0 to 3V

Input pulse rise/fall time: 3 ns

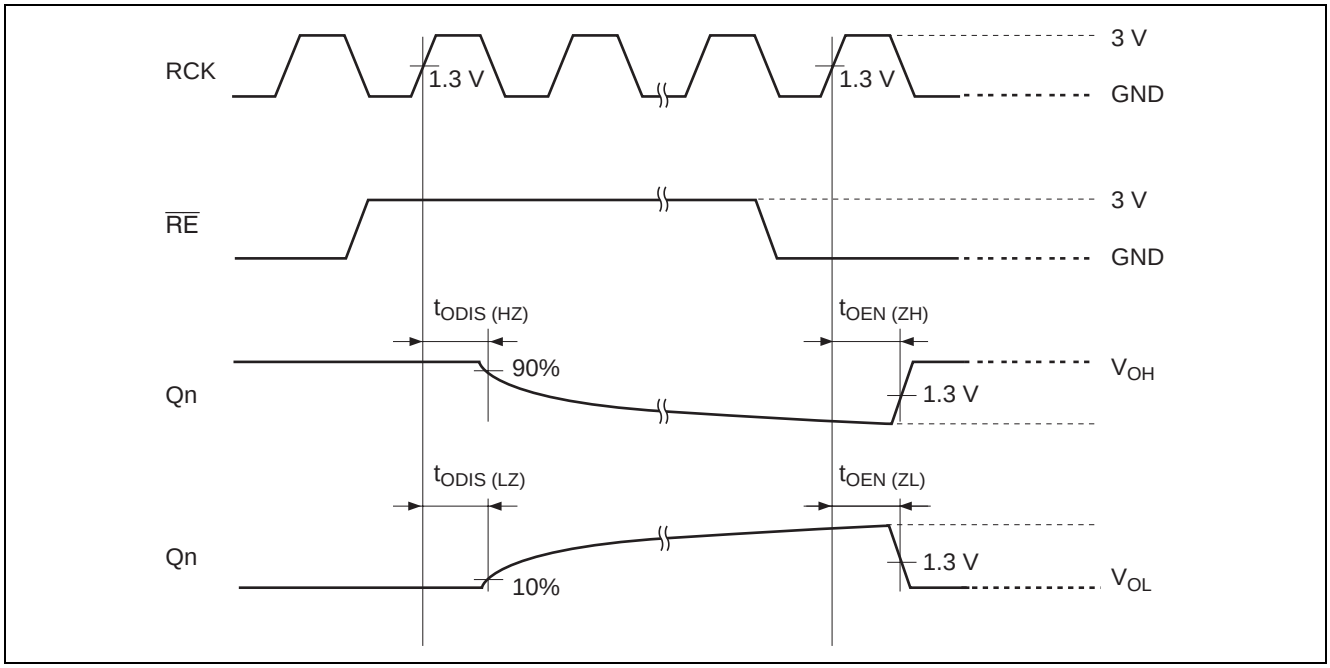
Decision voltage input: 1.3 V

Decision voltage output: 1.3 V (However, $t_{ODIS\ (LZ)}$ is 10% of output amplitude and $t_{ODIS\ (HZ)}$ is 90% of that for decision)

The load capacitance C_L includes the floating capacitance of connection and the input capacitance of probe.

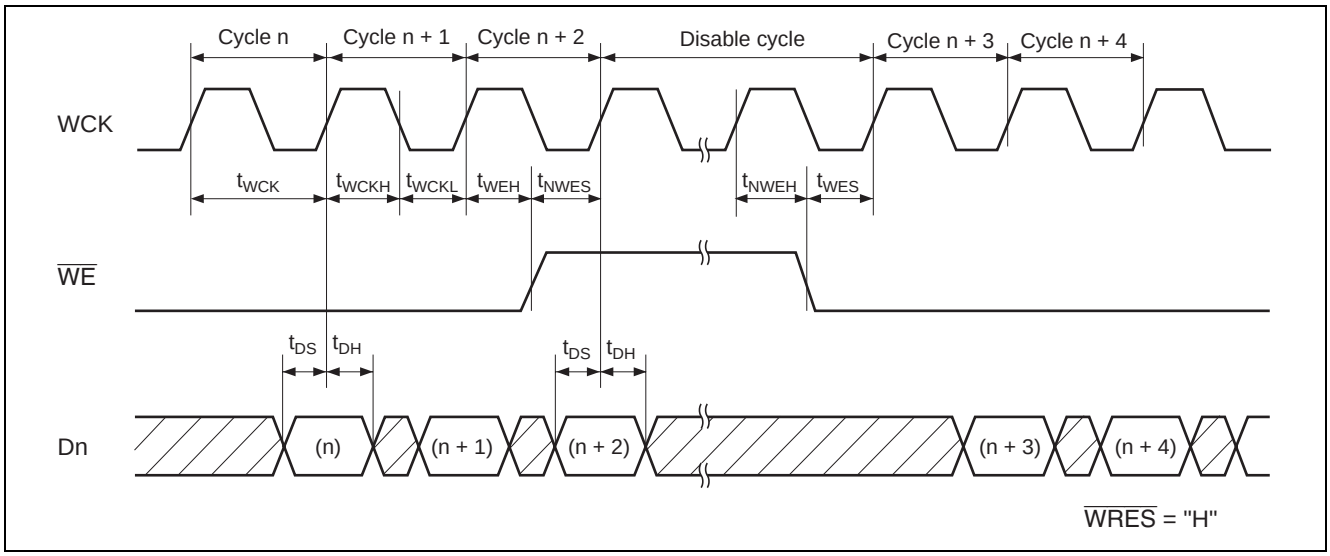
Parameter	SW1	SW2
$t_{ODIS\ (LZ)}$	Closed	Open
$t_{ODIS\ (HZ)}$	Open	Closed
$t_{OEN\ (ZL)}$	Closed	Open
$t_{OEN\ (ZH)}$	Open	Closed

t_{ODIS}/t_{OEN} Test Condition

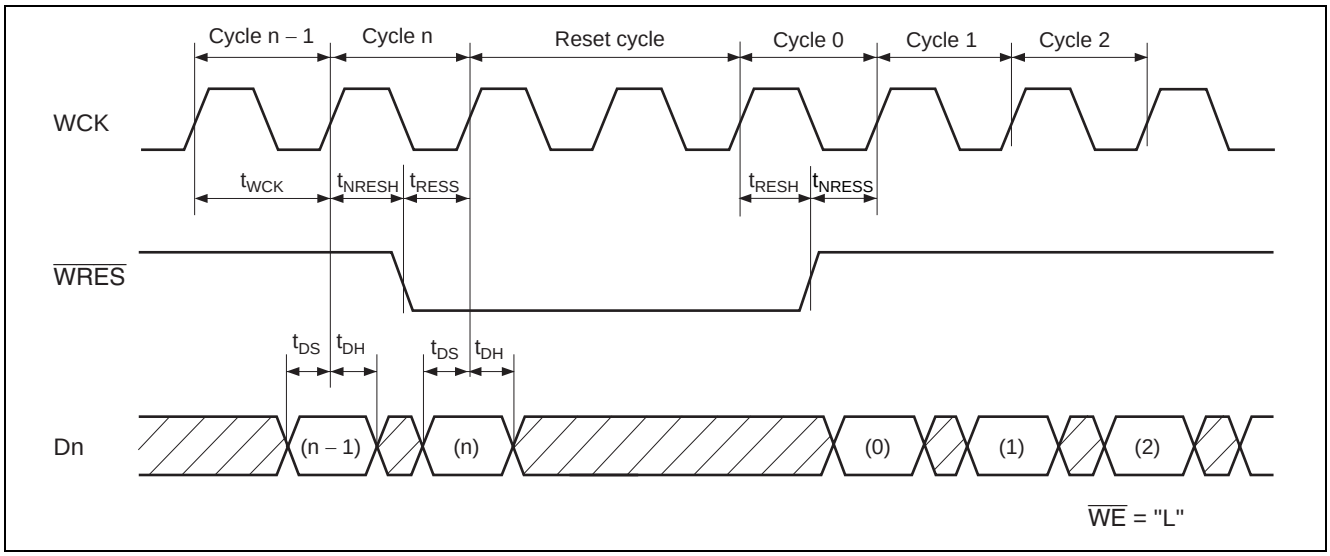


Operating Timing

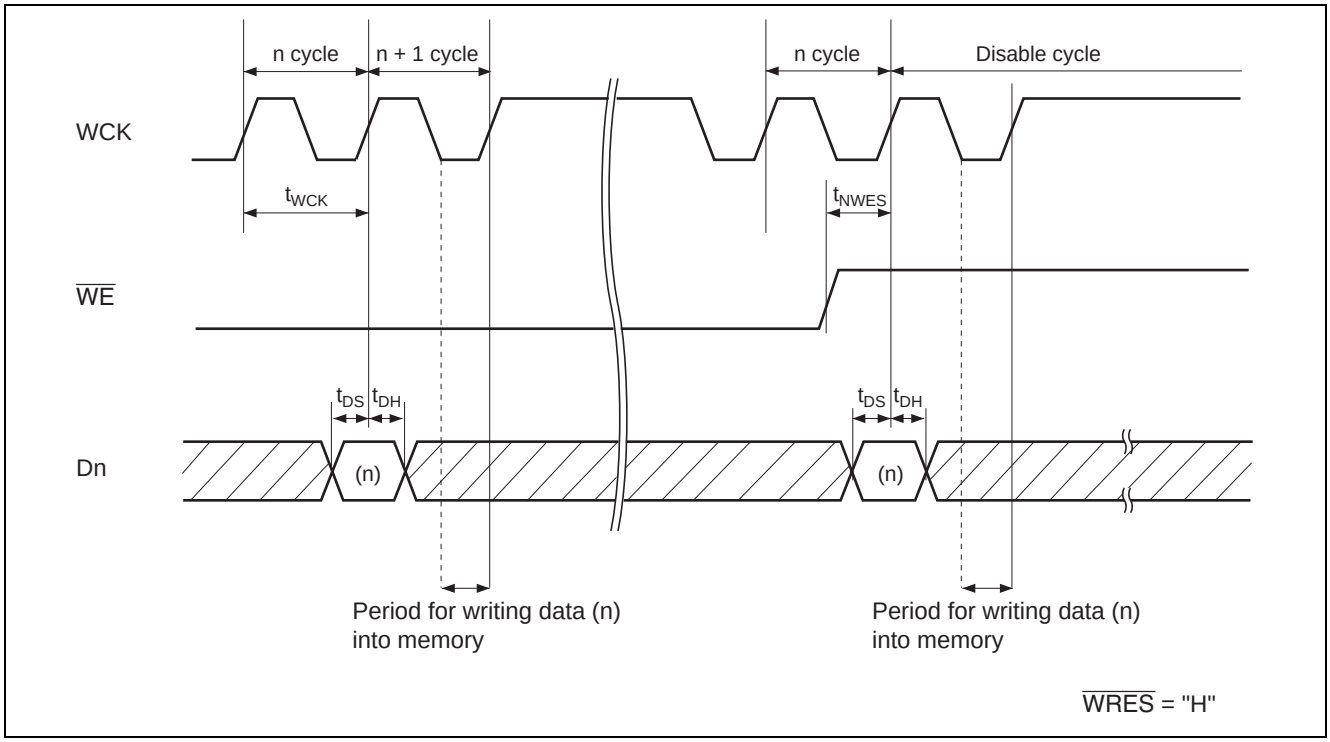
Write Cycle



Write Reset Cycle



Matters that Needs Attention when WCK Stops

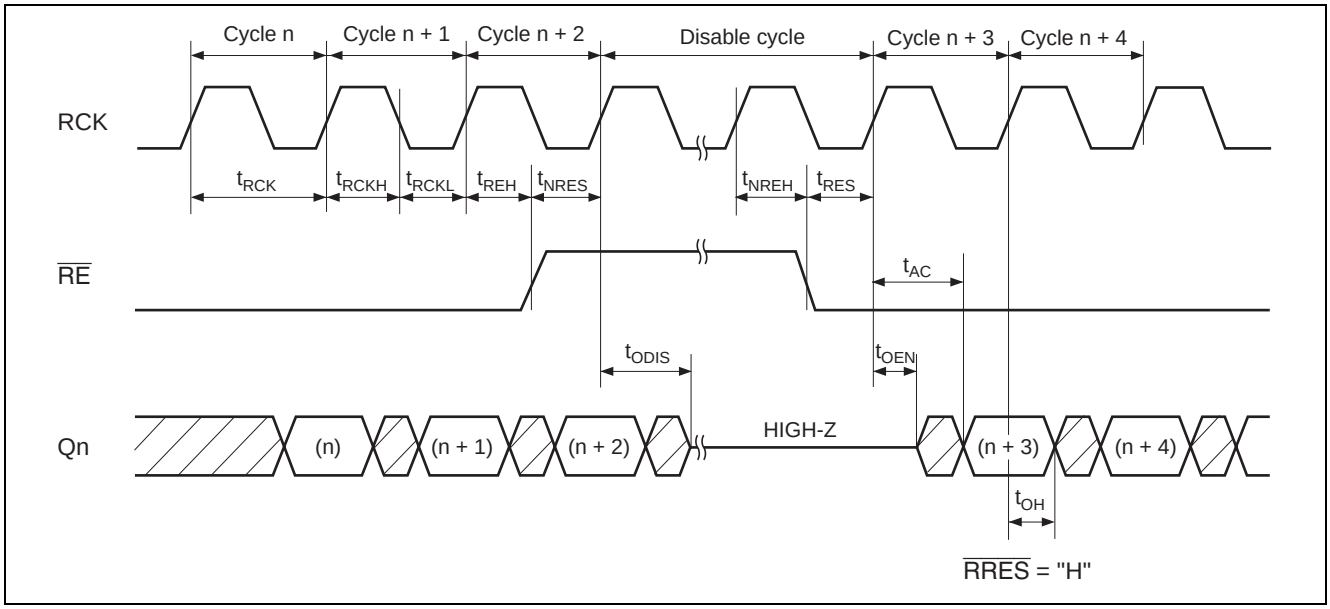


Input data of n cycle is read at the rising edge after WCK of n cycle and writing operation starts in the WCK low-level period of n + 1 cycle. The writing operation is complete at the falling edge after n + 1 cycle.

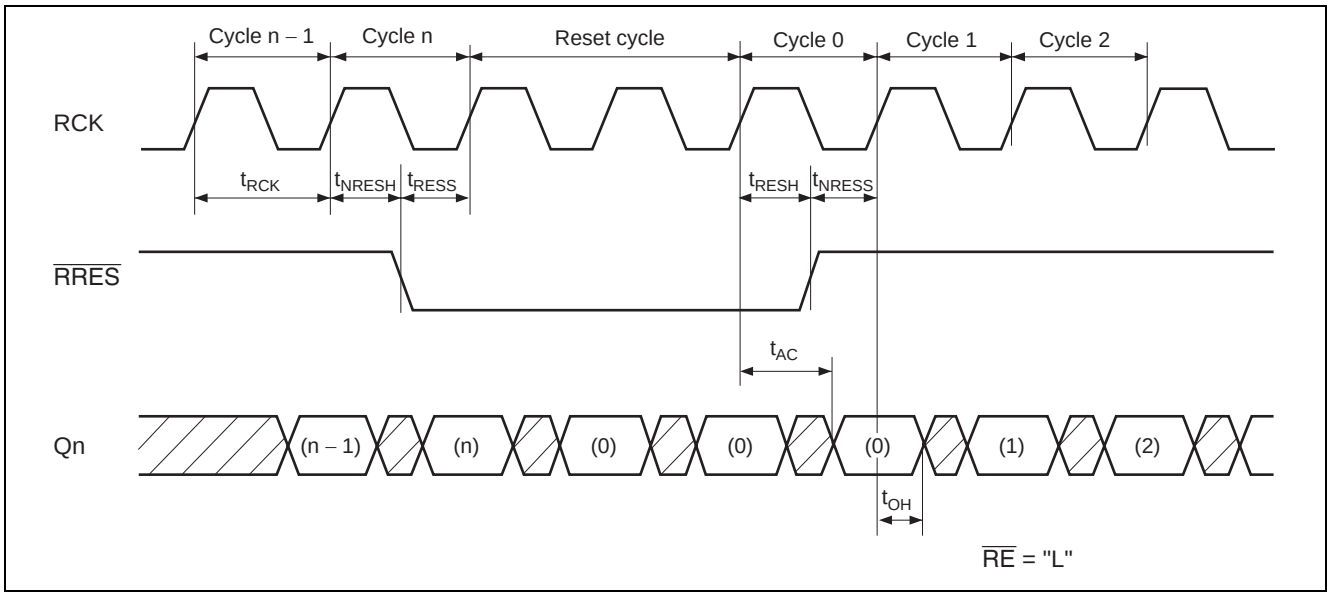
To stop reading write data at n cycle, enter WCK before the rising edge after n + 1 cycle.

When the cycle next to n cycle is a disable cycle, WCK for a cycle requires to be entered after the disable cycle as well.

Read Cycle



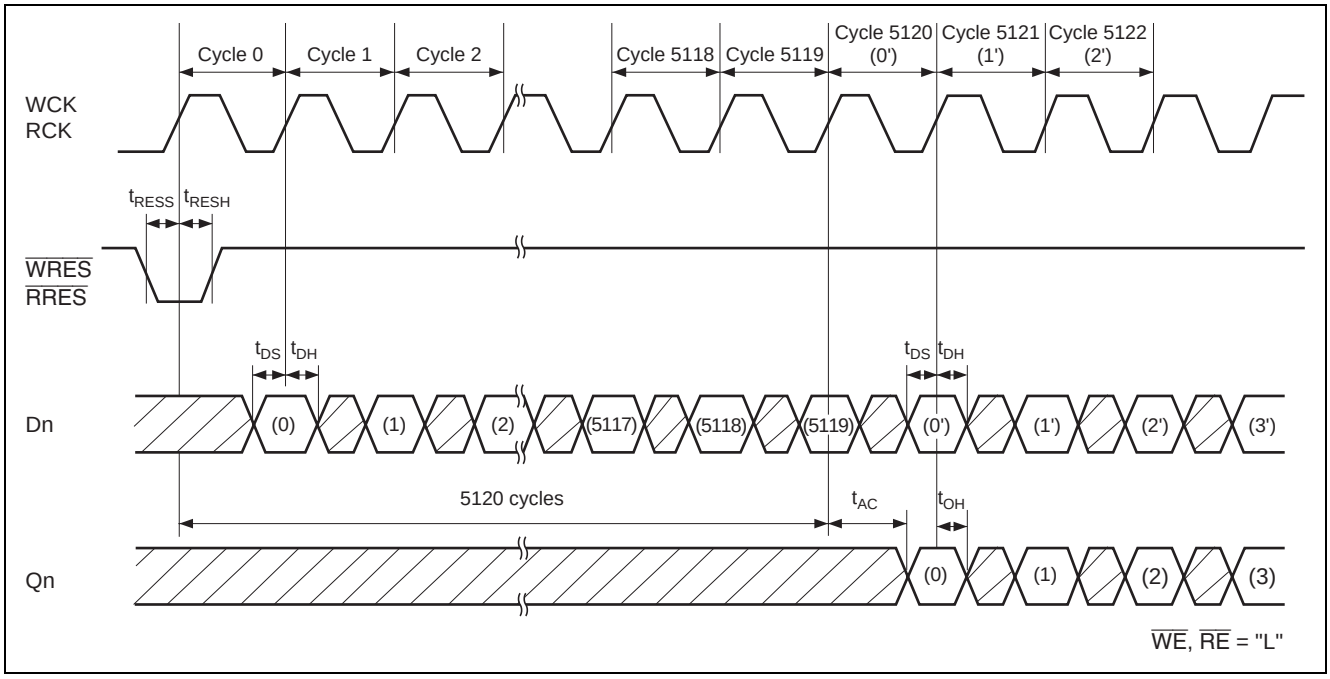
Read Reset Cycle



Variable Length Delay Bits

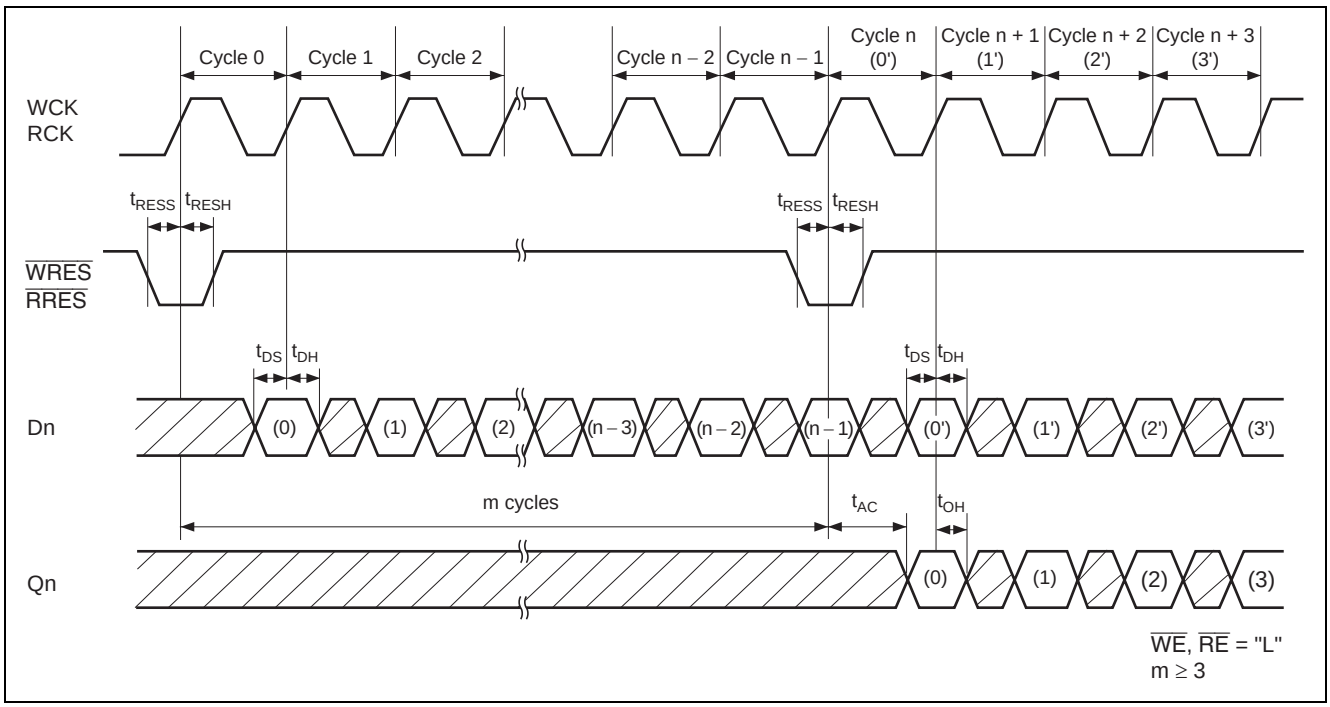
1-line (5120 Bits) Delay

A write input data is written into memory at the second rise edge of WCK in the cycle, and a read output data is output from memory at the first rise edge of RCK in the cycle, so that 1-line delay can be made easily.



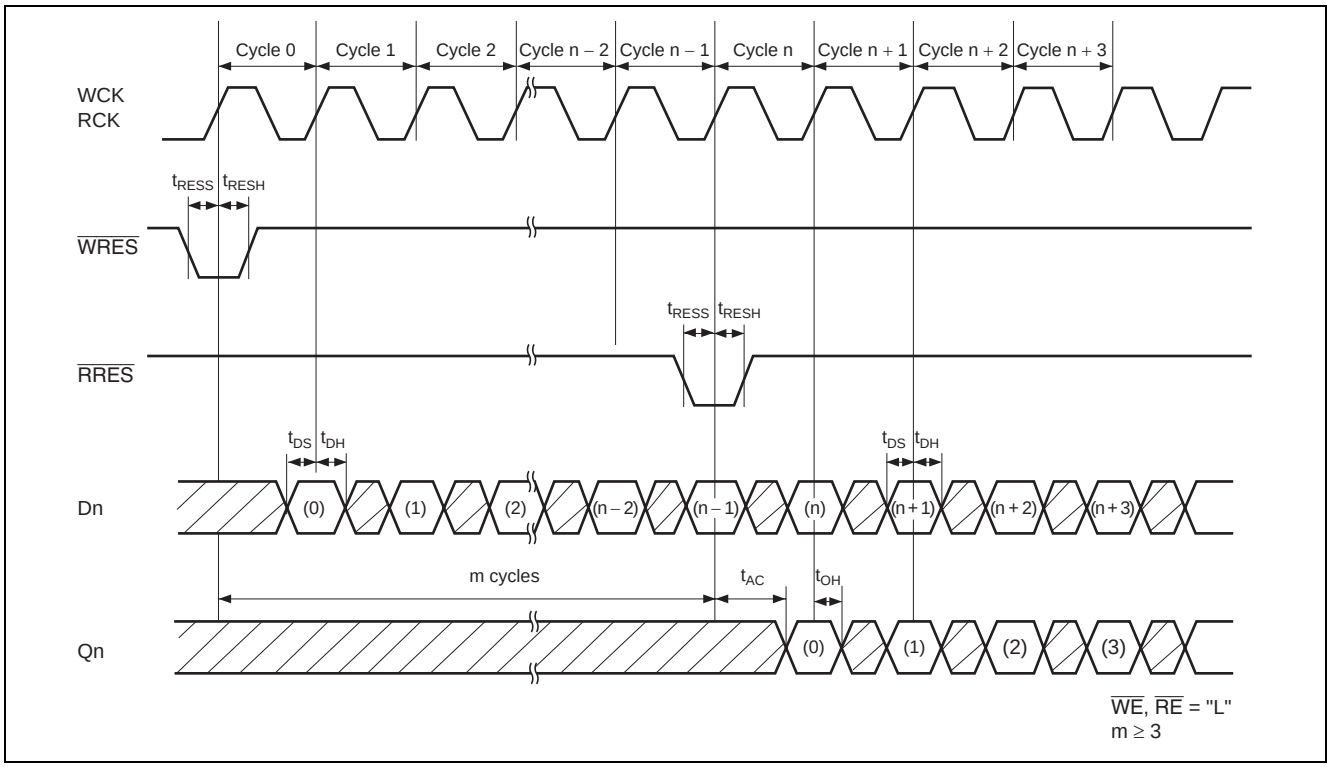
N-bit Delay Bit

(Making a reset at a cycle corresponding to delay length)



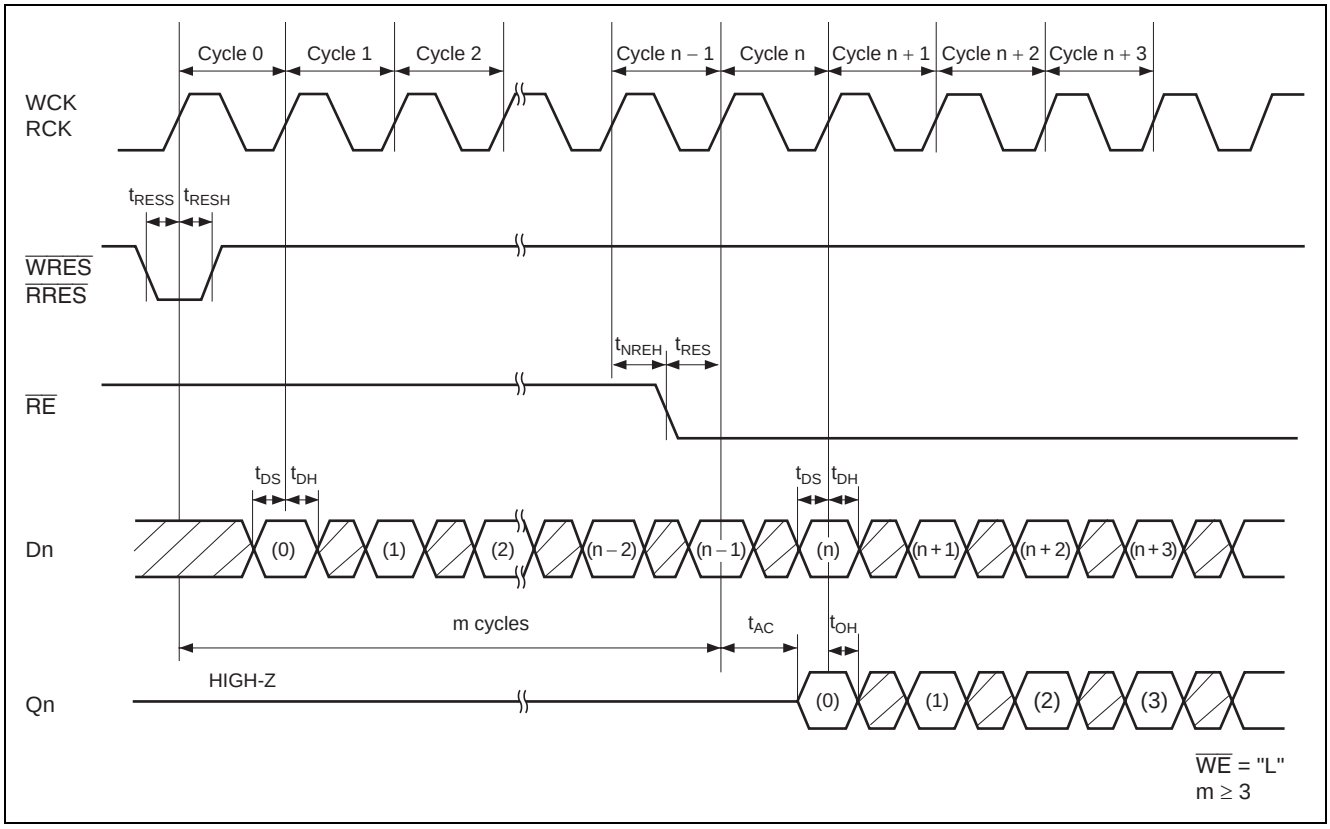
N-bit Delay 2

(Sliding $\overline{WRES}$ and $\overline{RRES}$ at a cycle corresponding to delay length)



N-bit Delay 3

(Disabling $\overline{RE}$ at a cycle corresponding to delay length)

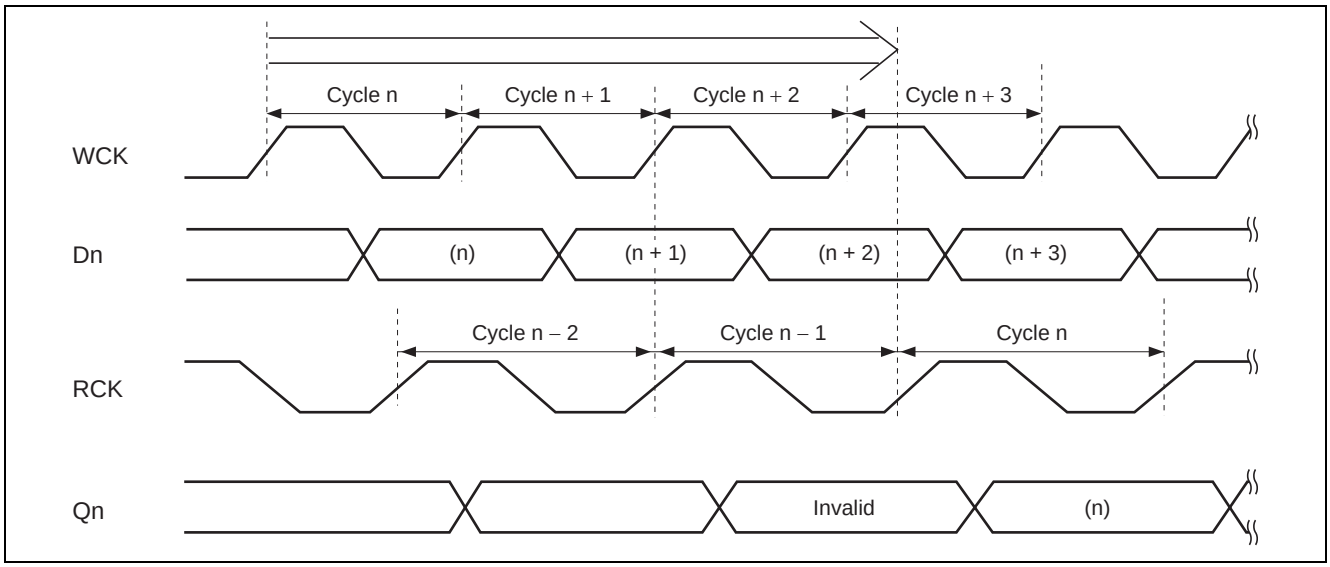


Shortest Read of Data "n" Written in Cycle n

(Cycle n – 1 on read side should be started after end of cycle n + 1 on write side)

When the start of cycle n – 1 on read side is earlier than the end of cycle n + 1 on write side, output Qn of cycle n becomes invalid.

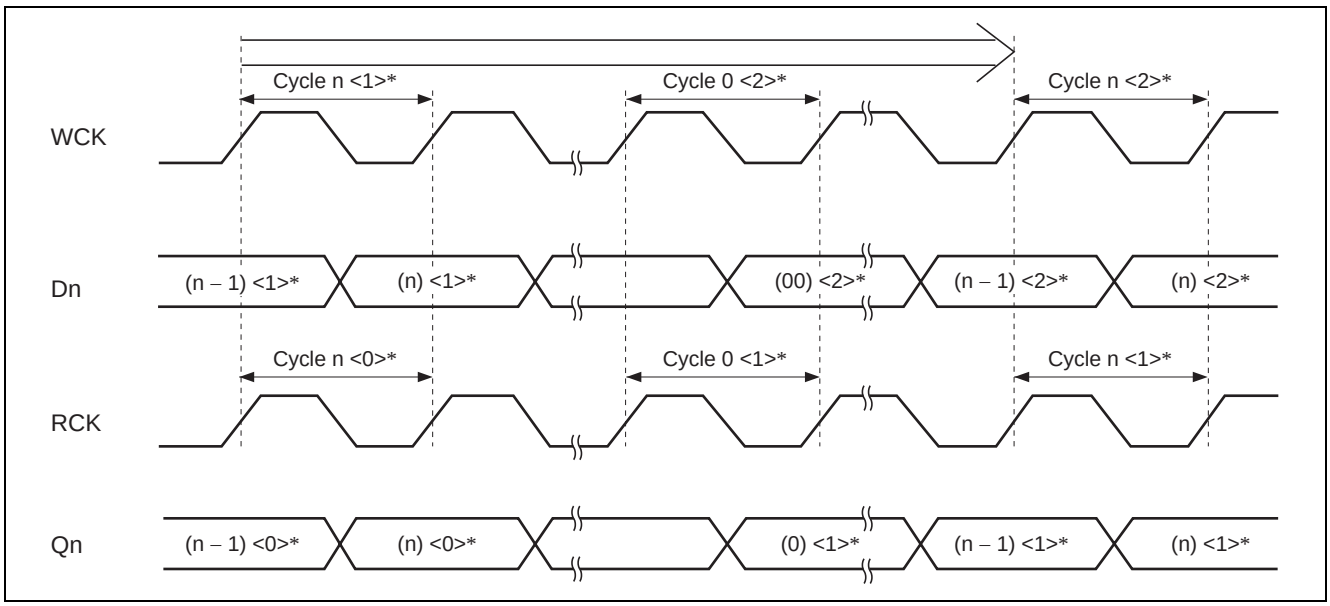
In the figure shown below, the read of cycle n – 1 is invalid.



Longest Read of Data "n" Written in Cycle n: 1-line Delay

(Cycle n <1>* on read side should be started when cycle n <2>* on write is started)

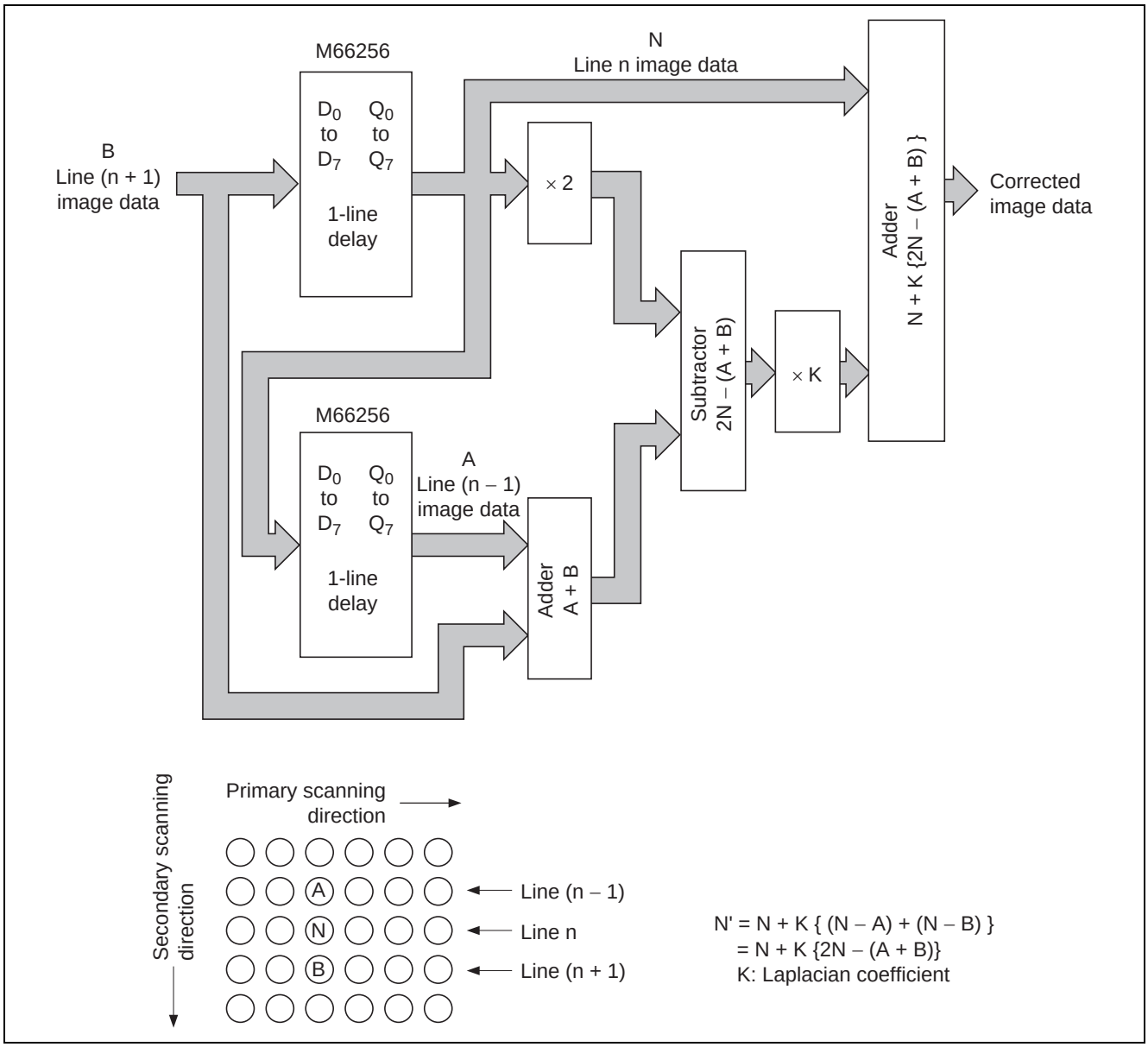
Output Qn of n cycle <1>* can be read until the start of reading side n cycle <1>* and the start of writing side n cycle <2>* overlap each other.



Note: <0>*, <1>* and <2>* indicates a line value.

Application Example

Laplacian Filter Circuit for Correction of Resolution in the Secondary Scanning Direction

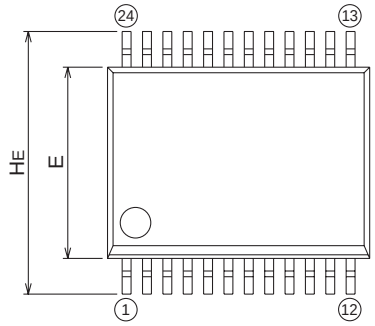


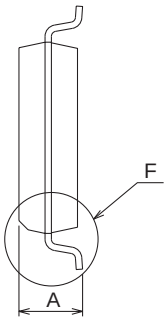
Package Dimensions

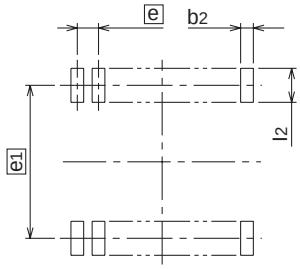
24P2U-A

Plastic 24pin 375mil SSOP

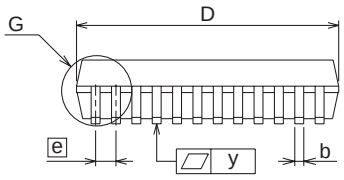
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP24-P-375-0.80	—	0.4	Cu Alloy

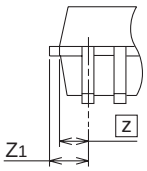




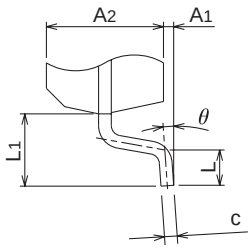


Recommended Mount Pad





Detail G



Detail F

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.65
A1	0.1	0.2	0.3
A2	—	2.3	—
b	0.3	0.35	0.45
c	0.23	0.25	0.3
D	10.2	10.3	10.4
E	7.4	7.5	7.6
e	—	0.8	—
HE	10.0	10.3	10.6
L	0.5	0.7	0.9
L1	—	1.4	—
z	—	0.75	—
Z1	—	—	0.9
y	—	—	0.1
θ	0°	—	8°
b2	—	0.5	—
e1	—	9.53	—
l2	1.27	—	—

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