M62260FP

CS / BS CONVERTER DRIVER IC

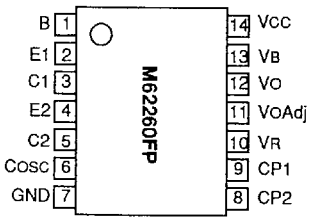
DESCRIPTION

M62260FP is developed to be a 2-channel HEMT driver.

Capable of simplifying the peripheral circuits, this IC permits compact unitized design.

Incorporating in itself two power sources, +8V with high stability and great current capacity and –3.2V with simple construction, and the protective circuit designed to be actuated in the event of output overload or short, the IC has no restrictions to its applications.

PIN CONFIGURATION (TOP VIEW)



Outline 14P2P-A

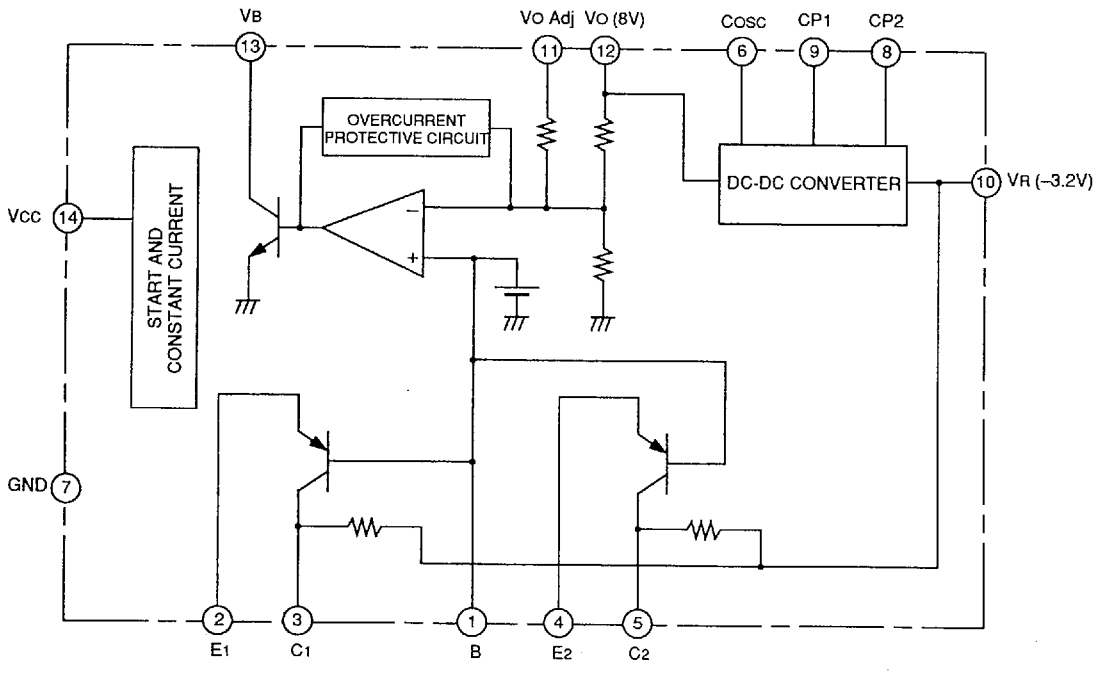
FEATURES

- Sole connection of small-capacity power transistors permits the construction of a power source system, and therefore it is possible to produce low-cost sets with a small number of parts.
- The "L" shape protective circuit used as the over-current limiting circuit prevents heat generation and destruction in the event of output short.
- Since the high-precision +8V power source is arranged as predrive, sole connection of external transistors permits current output in the magnitude of h_{FE} times 30 mA.
  (when h_{FE}=50, the resulting maximum current is 1.5 A.)
  Since the power source can serve as a low dropout power source as well, even low line voltage such as a minimum of Vo + 0.5V provides normal operation.
- The package is small with 14 pins.
- The use of voltage adjustment terminals permits external adjustment of output voltage.

APPLICATION

CS and BS converters and the like

BLOCK DIAGRAM



EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
①	B	HEMT driving PNP transistor base output(reference voltage output)
②	E1	HEMT driving PNP transistor emitter output 1
③	C1	HEMT driving gate bias output 1
④	E2	HEMT driving PNP transistor emitter output 2
⑤	C2	HEMT driving gate bias output 2
⑥	Cosc	DC-DC converter oscillation circuit capacitor connection terminal
⑦	GND	GND terminal
⑧	CP2	Charge pump capacitor connection terminal
⑨	CP1	Charge pump capacitor connection terminal
⑩	V_R	Negative output voltage terminal
⑪	V_{OADJ}	Positive and negative output voltage adjustment terminal
⑫	V_O	Positive output voltage terminal
⑬	V_B	External transistor base drive terminal
⑭	V_{CC}	Power supply terminal

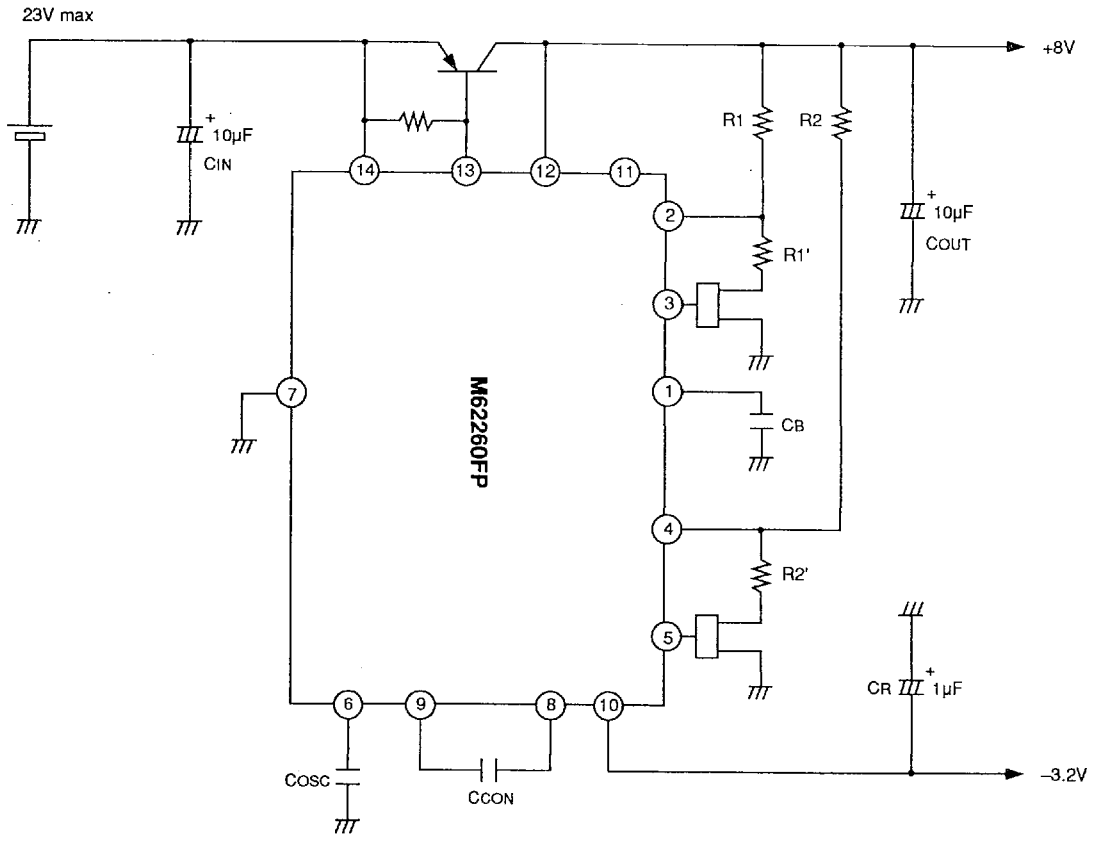
ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		23	V
P_d	Power dissipation		550	mW
K_θ	Thermal derating	Ta>=25°C	5.5	mW/°C
T_{opr}	Operating termperature		−30~+85	°C
T_{stg}	Storage temperature		−55~+125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		V_O+0.5		22	V
I_{CC}	Circuit current			10	15	mA
I_{Bmax}	MAXIMUM Bias current		10	30		mA
V_O	Positive output voltage	In steady state (V_{OAdj} : open)	7.6	8.0	8.4	V
		V_{OAdj}-Vo terminal short	4.75	5.0	5.25	
V_R	Negative output voltage	In steady state (V_{OAdj} : open)	−4.0	−3.2	−2.4	V
		V_{OAdj}-Vo terminal short	−2.5	−2.0	−1.5	
V1	Reference voltage		2.38	2.5	2.62	V
I BSC	Positive output short bias current			1		mA
Reg-in	Positive output input regulation	V_{CC}=8.5V~22V		0.02		%/V
Reg-lo	Positive output load regulation	I_O=10mA~100mA		20		mV
VoN	Positive output noise voltage	BPF:10Hz~100kHz,I_O=100mA		170	300	μVrms
R.R	Positive output ripple removal ratio		40	60		dBm
$\Delta V_O/\Delta T$	Positive output voltage temperature coefficient			0.02		%/T
⊖ Reg-lo	Negative output load regulation	I_R=−0.5mA~−3mA		0.6	0.9	V
$\Delta V_R/\Delta T$	Negative output voltage temperature coefficient			0.02		%/T
ΔV_R	Negative output ripple voltage	I_R=0		20	30	mV
ΔV_O	Positive output clock leak voltage	I_L=0		10	20	mV

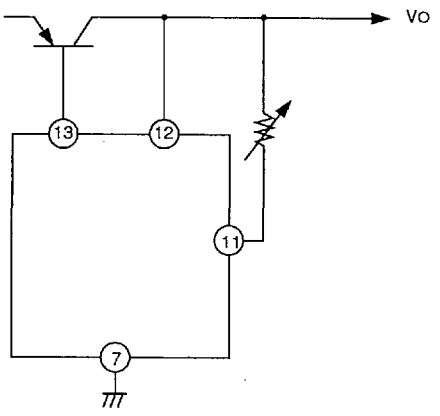
APPLICATION EXAMPLE



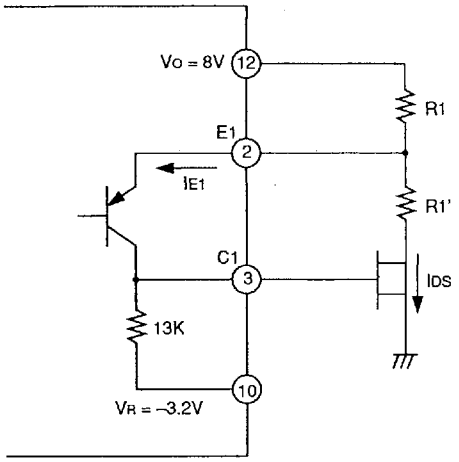
* R1' and R2' are required for VDS adjustment.

V_{OAdj} terminal (pin ⑪)

This terminal is the adjustment terminal for V_O, V_R.
Insertion of an adjustment resistor between pins ⑪, ⑫, as shown in the diagram at right, permits adjustment in the range of $5V \leqq V_O \leqq 8V$.
(When pins ⑪, ⑫ are shorted, V_O=5V)
V_R changes according to V_O setting.
$V_R = -0.4V_O$ (V)



HEMT BIAS CIRCUIT

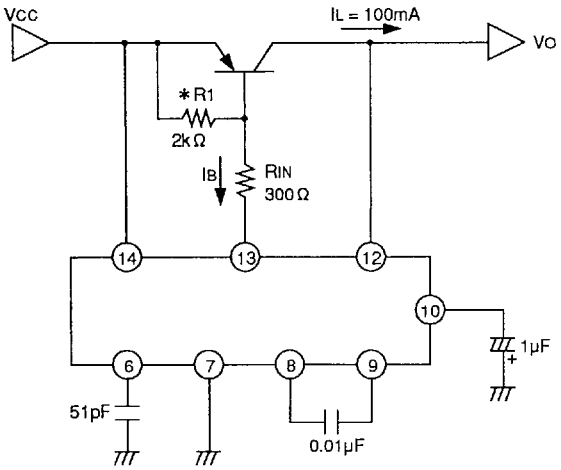


- R1=(VO – VB + VBE) / (IDS + IE1), R1' = (VB + VBE – VDS) / IDS
  (VO = 8V, VB = 2.5V, VBE = 0.7V, IDS = 10mA, VDS = 2V, IE1 = 0.23mA)
  R1 = (8V – 2.5V + 0.7V) / (10mA + 0.23mA)
  =4.8V/10.23mA
  R1 ≒ 470Ω

  R1' = (2.5V + 0.7V – 2V) /10mA
  =1.2V/10mA
  R1' ≒ 120Ω

  VGS = IE1•13K –3.2V
  =2.99V –3.2V
  VGS = –0.21V
  R1 ≒ 470Ω, R1' ≒ 120Ω, VGS = –0.21V

Example application to limit the maximum bias current.



* R1 should be between 700Ω ~6kΩ

When the input voltage (VCC) is lower than the set output voltage (VO), approx. 30 ~ 45mA bias current flows through pin ⑬ of the IC (see the bias current-line voltage characteristics diagram).

Insertion of a resistor, RIN, as needed such as when the bias current need be limited, permits limiting the bias current (see Fig. 1 for the line voltage dependence of the input resistance, RIN and the limited current.)

In this applied circuit, the current flowing through pin ⑬ is limited to approx. 20 mA when the line voltage (VO) is 8V.

Fig. 2 presents the bias current vs. line voltage characteristics of this applied circuit.

MAXIMUM BIAS CURRENT LIMITING (IBM)

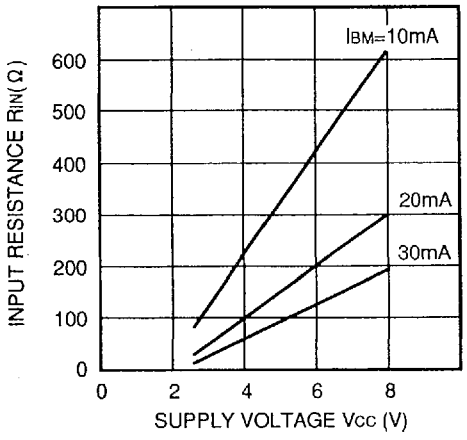


Fig. 1

BIAS CURRENT VS. LINE VOLTAGE

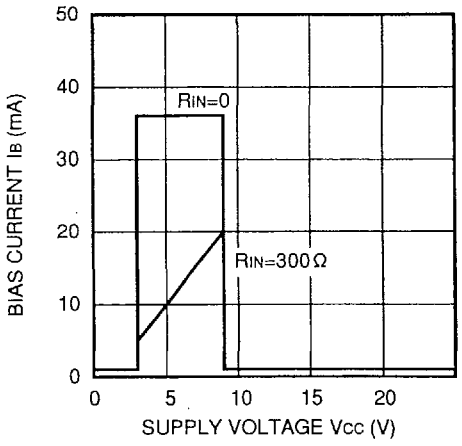


Fig. 2

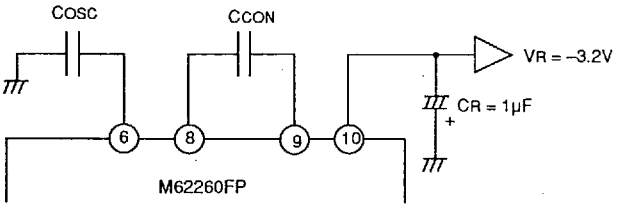
- DC-DC converter oscillation frequency setting equation.

$$f = \frac{1}{26 \times 10^{3} \cdot C_{OSC} + 1 \times 10^{-6}} \text{ [Hz]}$$

- Setting on the capacitors (C_{OSC}, C_{CON}) to produce negative power source (V_R).

〈Example C_{OSC}-C_{CON} ratio〉

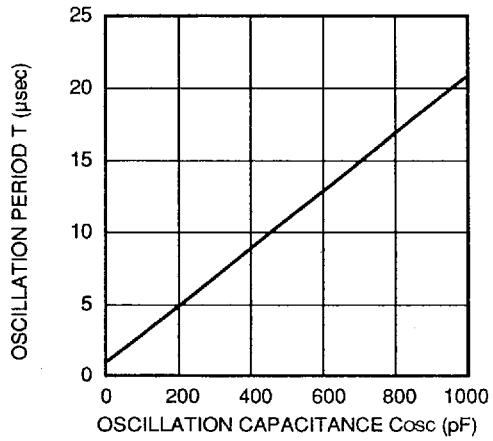
C_{OSC} (PF)	C_{CON} (μF)	f (kHz)
500	0.1	90
100	0.022	333
50	0.01	500



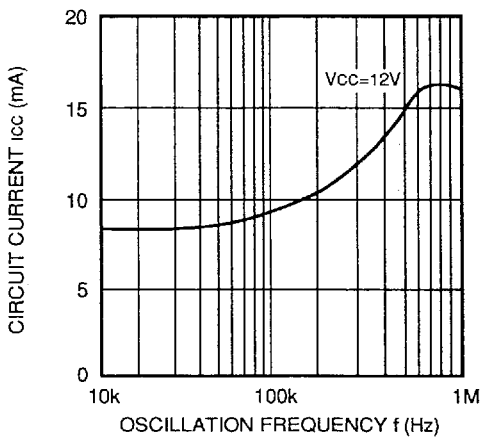
SET THE C_{OSC}-C_{CON} RATIO TO 1: 200 OR GREATER.

TYPICAL CHARACTERISTICS

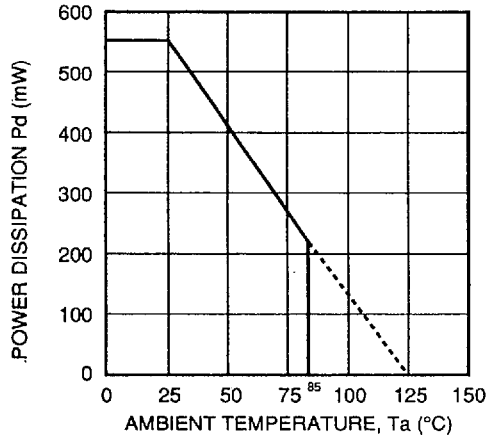
OSCILLATION PERIOD VS. OSCILLATION CAPACITANCE



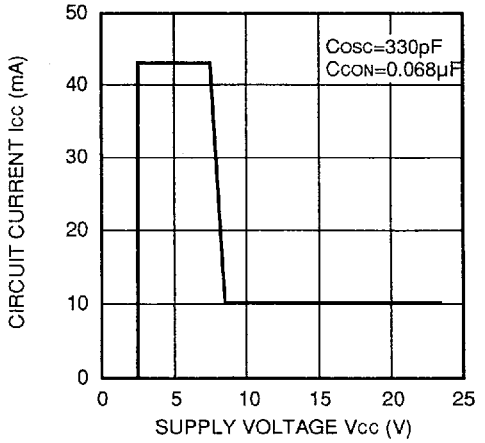
CIRCUIT CURRENT VS. OSCILLATION FREQUENCY



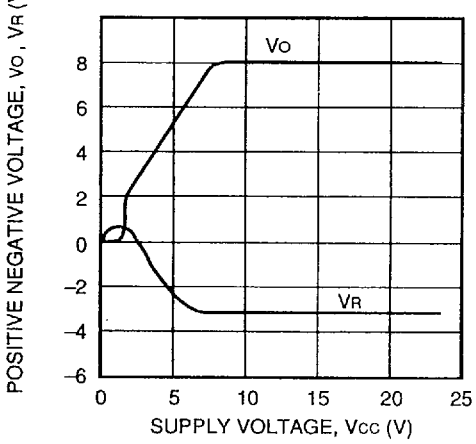
THERMAL DERATING



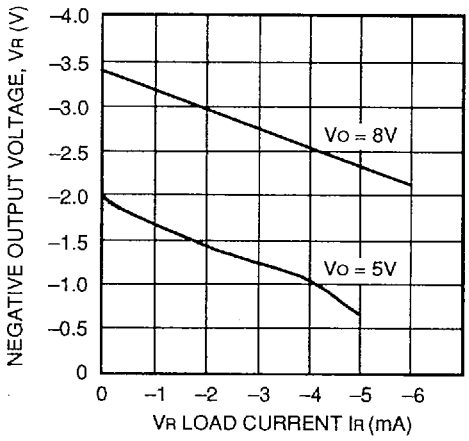
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



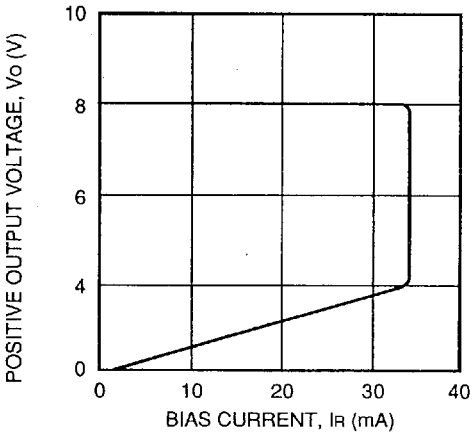
POSITIVE NEGATIVE OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



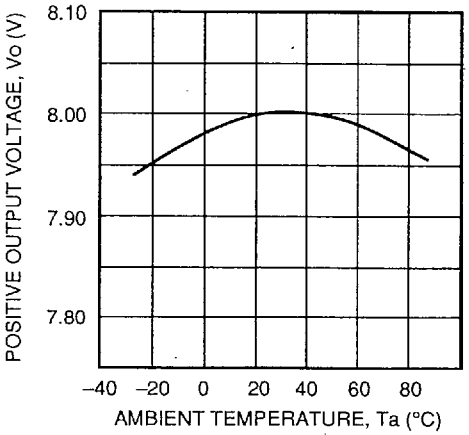
NEGATIVE OUTPUT VOLTAGE VS. NEGATIVE CURRENT



POSITIVE OUTPUT VOLTAGE VS. BIAS CURRENT



POSITIVE OUTPUT VOLTAGE VS. AMBIENT TEMPERATURE



PIN ① POTENTIAL VS. AMBIENT TEMPERATURE

