M61006FP

DISTANCE DETECTION SIGNAL PROCESSING FOR 3 V SUPPLY VOLTAGE

REJ03F0039-0100Z
Rev.1.0
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Description

M61006FP is a semiconductor integrated circuit including distance detection signal processing circuit for 3 V supply voltage. This device transforms each optical inflow current I1 and I2 from PSD SENSOR into the voltage, and integrates the output after doing calculation corresponds to I1 / (I1+I2), and outputs it as the voltage data.

Features

- Wide supply voltage range: Vcc = 2.2 to 5.5 V
- Including clamp level switching circuit
  (It is possible to set a clamp level to 15 points with outside control.)
- Including infinity discrimination function
  (clamp on detection function)
- Including POWER ON RESET function
- Including simple temperature detection function
  (It is possible to correct temperature with transmitting this output to the microcomputer.)

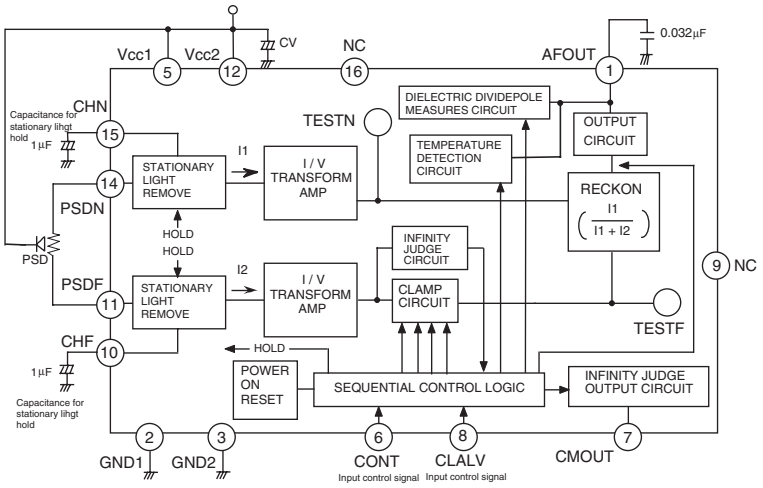
Application

- Auto focus control for a camera, short distance sensor, etc.

Recommended Operating Condition

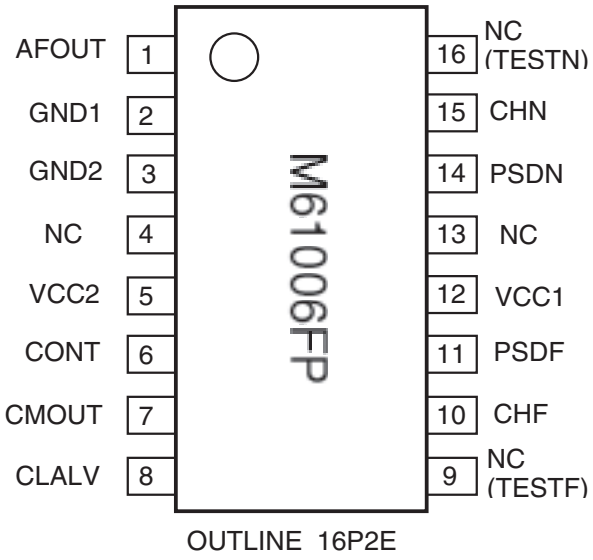
- Supply voltage range …… 2.2 V to 5.5 V
- Rated supply voltage …… 3.0 V

Block Diagram



Note: Pin9, 16 is avail only for engineering sample.

Pin Configuration (Top View)



OUTLINE 16P2E

Note: Pin9,16 is available only for engineeing sample.
Vcc, GND1: small signalanalog line
Vcc, GND2: analog line or control line

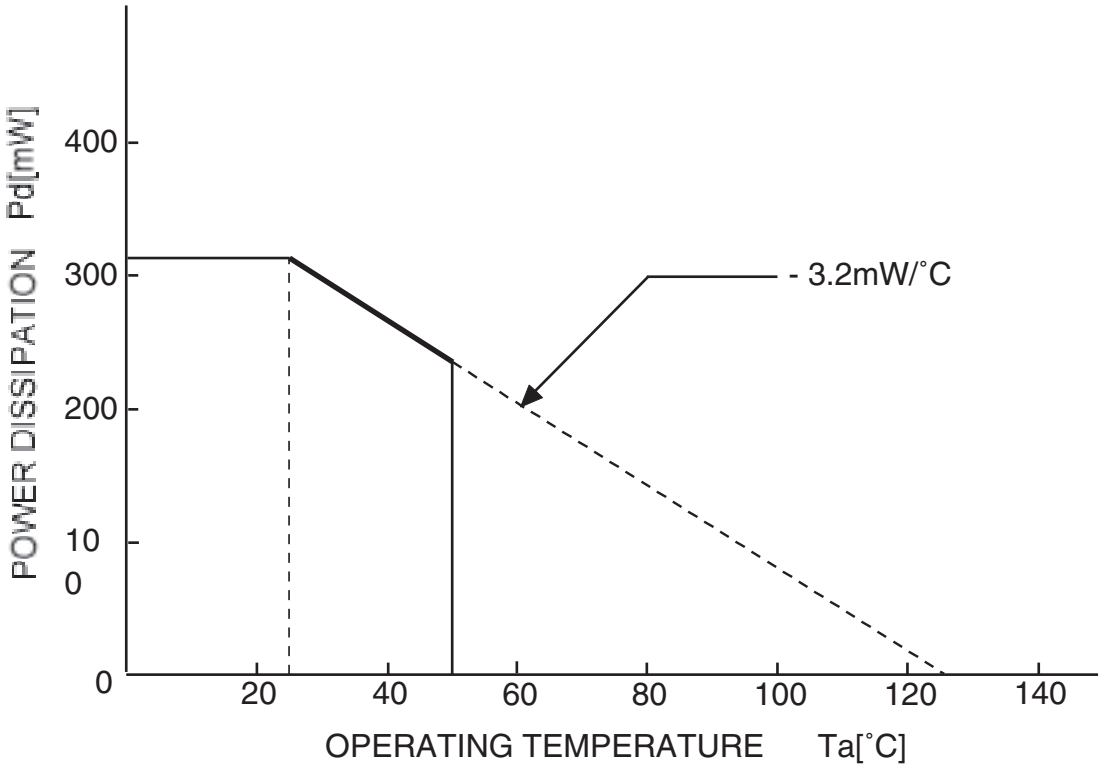
Absolute Maximum Ratings

(Ta = 25°C unless otherwise noted)

Parameter	Symbol	Rating	Unit	Remark
Supply voltage	V_{CC}	7.0	V	Note1
Power dissipation	Pd	320	mW	Ta = 25°C
Thermal derating	Kθ	–3.2	mW / °C	Ta ≥ 25°C
Pin supply voltage	V_{IF}	7.0	V	Pin 6, 7, 8
Another terminal	VI / O	0 to V_{CC}+0.3	V	Note2
Output inflow current	Icmout	0.5	mA	NPN open collector
Operating temperature	Topr	–10 to 50	°C	
Storage temperature	Tstg	–40 to 125	°C	

Notes: 1. As a principle, do not provide a supply voltage reversely.
2. As a principle, do not provide the terminals with the voltage over supply voltage or under ground voltage.

Thermal Derating Curve



Electrical Characteristics - 1

(Ta = 25°C)

Classi-ficatin	Parameter	Symbol	Test conditions	Limits			Unit	V_{CC} (V)	Note
				Min	Typ	Max			
	Operating supply voltage range	VCC		2.2	3.0	5.5	V	3.0	
Consum-ing Current	Usual consuming current	ICC1		—	3.9	5.1	mA		*6
	Rapid charge consuming current 1	ICC2	AFOUT rapid charge consuming current VAFOUT = 0 V	—	9.5	12.5	mA		*1 *6
	Rapid charge consuming current 2	ICC3	CH rapid charge consuming current	—	10.5	13.7	mA		*1 *6
CONT pin	CONT "H" input voltage	VCOH		1.1	—	7.0	V		
	CONT "L" input voltage	VCOL		0	—	0.3	V		
	CONT "H" input current	ICOH	VIH = 5.5 V	—	—	1.0	µA		*6
	CONT "L" input current	ICOL	VIL = 0 V	–84	–64	–44	µA		
CLALV pin	CLALV "H" input voltage	VCLH		1.1	—	7.0	V		
	CLALV "L" input voltage	VCLL		0	—	0.3	V		
	CLALV "H" input current	ICLH	VIH = 5.5 V	—	—	1.0	µA		*6
	CLALV "L" input current	ICLL	VIL = 0 V	–84	–64	–44	µA		
HOLD C	CH rapid charge current	ICHQC	IPSD = 5 µA VCH = 0 V	–2000	–1000	–500	µA		
	CH stationary charge current	ICHC	VCH = 0 V	–33	–22	–11	µA		
	CH stationary discharge current	ICHD	VCH = 1.5 V	11	22	33	µA		
Integra-tion circuit	AFOUT reset current	I_{RAFOUT}	VAFOUT = 0.5 V	600	1200	2400	µA		
	AFOUT integrating off current	$I_{OFFAFOUT}$	VAFOUT = 0.5 V	—	—	1.0	µA		*6
	AFOUT integrating current (maximum integration current)	$I_{INTAFOUT}$	VAFOUT = 0.5 V VCHF = 2.0 V, VCHN = 0 V	–13.0	–10.0	–7.0	µA		
	Distance measurement integration current stability	ΔI_{INT}		—	3.0	6.0	%		*2 *6
	AFOUT temperature revision integration current	I_tAFOUT	VAFOUT = 0.5 V	–6.5	–5.0	–3.5	µA		
	The stability of temperature integration current	ΔIt		—	3.0	6.0	%		*2 *6
	Dynamic rage of AFOUT pin	D_{AFOUT}		—	—	2.7 (V_{CC}0.3)	V		*7

Electrical Characteristics - 2

(Ta = 25°C)

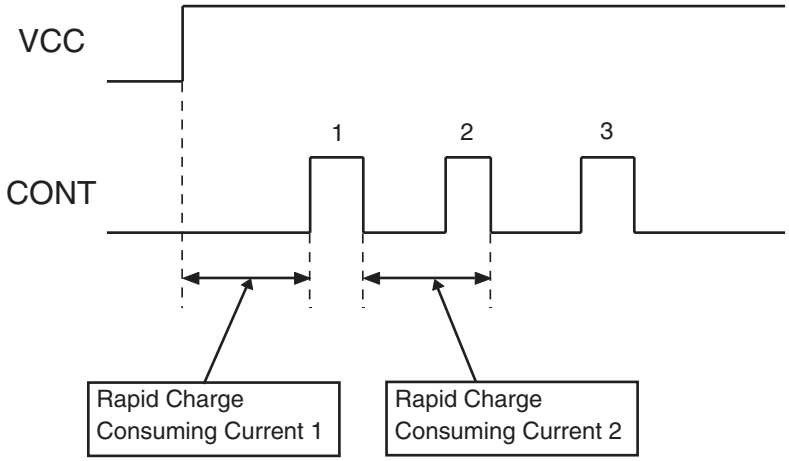
Classification	Parameter	Symbol	Test conditions	Limits			Unit	V_{CC} (V)	Note
				Min	Typ	Max			
AF Input Condition1	AF output voltage (9:1) -1	D (9:1) - 1	Near side 9: far side 1 IP = 100 nA	1.26	1.81	2.36	V	3.0	*3
	AF output voltage (6:4) -1	D (6:4) - 1	Near side 6: far side 4 IP = 100 nA	0.83	1.19	1.55	V		*3
	AF output voltage (3:7) -1	D (3:7) - 1	Near side 3: far side 7 IP = 100 nA	0.41	0.59	0.77	V		*3
	AF slope - 1	ΔAF - 1		0.85	1.22	1.59	V		*3
	AF linearity - 1	LAF - 1		0.875	0.975	1.075	—		*3
AF input condition2	AFoutput time (9:1) - 2	D (9:1) - 2	Near side 9: Far side1 IP = 50 nA	1.26	1.81	2.36	V		*3
	AFoutput time (6:4) - 2	D (6:4) - 2	Near side 6: Far side4 IP = 50 nA	0.83	1.19	1.55	V		*3
	AFoutput time (3:7) - 2	D (3:7) - 2	Near side 3: Far side7 IP = 50 nA	0.41	0.59	0.77	V		*3
	AF slope - 2	ΔAF - 2		0.85	1.22	1.59	V		*3
	AF linearity - 2	LAF - 2		0.875	0.975	1.075	—		*3
AF input condition3	AFoutput time (9:1) - 3	D (9:1) - 3	Near side 9: Far side1 IP = 50 nA	1.26	1.81	2.36	V		*3
	AFoutput time (6:4) - 3	D (6:4) - 3	Near side 6: Far side4 IP = 50 nA	0.83	1.19	1.55	V		*3
	AFoutput time (3:7) - 3	D (3:7) - 3	Near side 3: Far side7 IP = 50 nA	0.41	0.59	0.77	V		*3
	AF slope - 3	ΔAF - 3		0.85	1.22	1.59	μA		*3
	AF linearity - 3	LAF - 3		0.875	0.975	1.075	V		*3
AF input condition 1 to 2	AFoutput time (9:1) - 3	D (9:1) - 3	Near side 9: Far side1 (condition 1 to 3)	–0.022	—	0.022	—		*3
	AFoutput time (6:4) - 3	D (6:4) - 3	Near side 6: Far side4 (condition 1 to 3)	–0.022	—	0.022	—		*3
	AFoutput time (3:7) - 3	D (3:7) - 3	Near side 3: Far side7 (condition 1 to 3)	–0.022	—	0.022	—		*3

Electrical Characteristics - 3

(Ta = 25°C)

Classification	Parameter	Symbol	Test conditions	Limits			Unit	V_{CC} (V)	Note
				Min	Typ	Max			
Clamp determination	CMOUT leak current	ICMOUTH	VCMOUT = 5.5 V	—	—	1.0	µA	3.0	*6
	CMOUT saturation current	VCMOUTL	ICMOUT = 500 µA	—	—	0.3	V		*6
SENSOR	Signal ray maximum current	ΔINF		—	—	3.0	µA		*4 *8
	Capacity of the current to extract stationary rays	IPSD		—	—	30	µA		*4 *8
	Clamp level	ICLAM	The change values about TYP current (Design target value)	–50	—	50	%		
Clout for measurement rays	Nch Response speed of Circuit for measurement rays	ΔT_{TESTN}		—	—	26	µsec		*5 *6
	Fch Response speed of Circuit for measurement rays	ΔT_{TESTF}		—	—	26	µsec		*5 *6

*1 Rapid charge consuming current 1 and 2 are measured with the following conditions:



- Rapid charge consuming current 1
  = (Rapid charge current for integration capacitance AFOUT dielectric absorption) + (Usual consuming current)
- Rapid charge consuming current 2
  = (mainly Rapid charge current for hold capacitance CHN, CHF) + (Usual consuming current)

Shorten hold capacitance CHN, CHF pin, integration capacitance AFOUT pin and GND at measurement rapid charge consuming current 1 and hold capacitance CHN, CHF pin and GND at measurement rapid charge consuming current 2 to leave rapid charge current on stationary. But in practical uses it runs as the follows:

- Rapid charge current for hold capacitance CHN, CHF:
  Use in a constant current charge. The current remain consuming in IC after completing charge.
- Rapid charge current for integration capacitance AFOUT dielectric absourption:
  Transition current. It flows until completing charge.

*2 Charging rate of distance measurement integration current and temperature integration current when the voltage of AFOUT changes.

$$\Delta I_{AFOUT}1 = \left(1 - \frac{\text{distance measurement current (at AFOUT = 0.5V)}}{\text{distance measurement current (at AFOUT = VCC-0.3V)}} \right) / \text{(VCC-0.3V-0.5V)} \times 100\%$$

$$\Delta I_{AFOUT}2 = \left(1 - \frac{\text{distance measurement current (at AFOUT = 0V)}}{\text{distance measurement current (at AFOUT = VCC-0.3V)}} \right) / \text{(VCC-0.3V-0.5V)} \times 100\%$$

*3 Set a current output from PHOTOCUPPLER to following input conditions, and input the varied resistance ratio. AF slope, linearity is calculated with following equations by measuring AFOUT output voltage.

Input condition1: I_{PSD} (Stationary light current) = 0 I1:I2 = 100 nA
Input condition2: I_{PSD} (Stationary light current) = 0 I1:I2 = 50 nA
Input condition3: I_{PSD} (Stationary light current) = 10 μA I1:I2 = 100 nA

D (9:1)·····The AFOUT output voltage at input with I1:I2 = 9:1
D (6:4)·····The AFOUT output voltage at input with I1:I2 = 6:4
D (3:7)·····The AFOUT output voltage at input with I1:I2 = 3:7
AF slope: ΔAF = D (9:1) – D (3:7)
AF linearity: L (AF) = (D (9:1) - (6:4)) / (D (6:4) - (3:7))
PSD quite resistance: 120 kΩ

*4 Input current of one side channel without saturating stationary light remove circuit and I / V transform amplifier circuit.

*5 Confirm not to change the output data at measuring AF input condition (1 to 4), when you shorten intervals between stationary ray hold and distance measurement integration beginning to MIN 26 μS.

*6 The value in this item is less than “max” value at any cases.

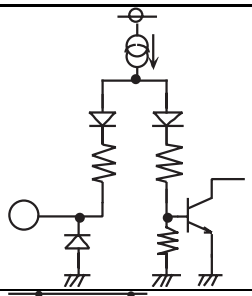
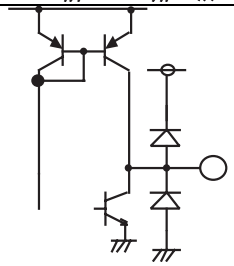
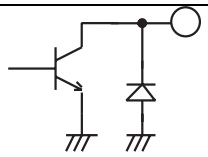
*7 Set AFOUT capacity, distance measurement integration time, and the number of integration under max value, because the “max” value in this item indicates a maximum of IC dynamic range.

*8 Establish optional system to be input current to IC less than standard value, because this item’s value indicates maximum input current to IC.

Interface Table

(Vcc = 3.0 V, Ta = 25°C)

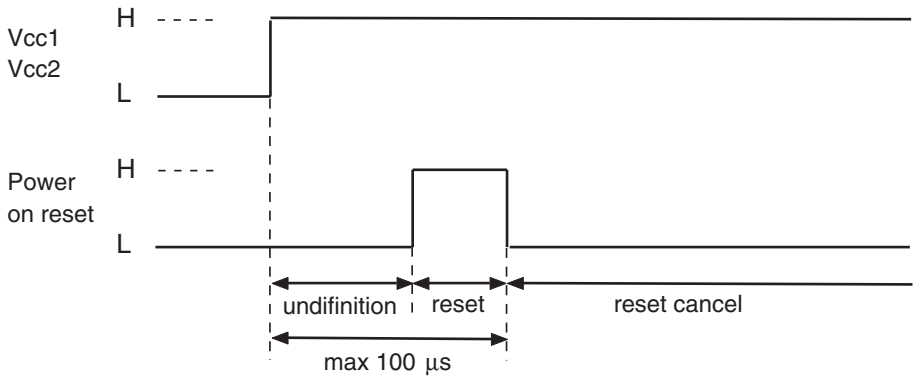
AF – IC side

Pin name	Circuit diagram	Parameter	Limits Min	Typ	Max	Unit	Test conditions and note
CONT CLALV		"H" input voltage	1.1	—	7.0	V	
		"L" input voltage	0	—	0.3		
		"H" input voltage	—	—	1.0	µA	VH = 5.5 V
		"L" input voltage	–84	–64	–44		VF = 0 V
AFOUT		"H" input voltage	—	—	Vcc –0.3	V	
		"L" input voltage	0	—	0.3		
		Integration OFF current	—	—	1.0	µA	VF = 0.5 V
		Integration ON current (Ratio10:0)	–13	–10	–7		VF = 0.5 V
CMOUT		"L" output voltage	—	—	0.3	V	IOL = 500 µA
		"H" leak current	—	—	1.0	µA	VIN = 5.5 V

Controls

(1) V_{CC} (Vcc1+Vcc2)

The power on reset circuit with a built in IC work by this pin turned on, and the whole IC including a part of logic circuit is done reset. Also the workings of power on reset circuit complete by less than 100 µS from rise edge of VCC1, 2 (VCC1, VCC2 greater than 2.2 V).



Note: Regard as rising supply voltage in establishing the timing if uses of this IC is in connecting large capacitance with supply pin.

(2) CLALV:

Do reset the whole IC including the clamp level set and the part of logic. This IC include D / A converter for 4 bits, and it is possible to establish clamp level to 15 points by clock input after cancel of reset (including none clamp). And also, the whole IC including parts of logic is reset by 15th clump level setting pulse (at intervals of 16 click after this clamp)

Values of each bit current are established as the right side. The number of input clock and clamp level are as follows.

bit	Set up current (Typ.)
1	0.130nA
2	0.260nA
3	0.520nA
4	1.040nA

Clock value	Clamp level(Typ.)
0	None clamp
1	0.130 nA
2	0.260 nA
3	0.390 nA
4	0.520 nA
5	0.650 nA
6	0.780 nA
7	0.910 nA
8	1.040 nA
9	1.170 nA
10	1.300 nA
11	1.430 nA

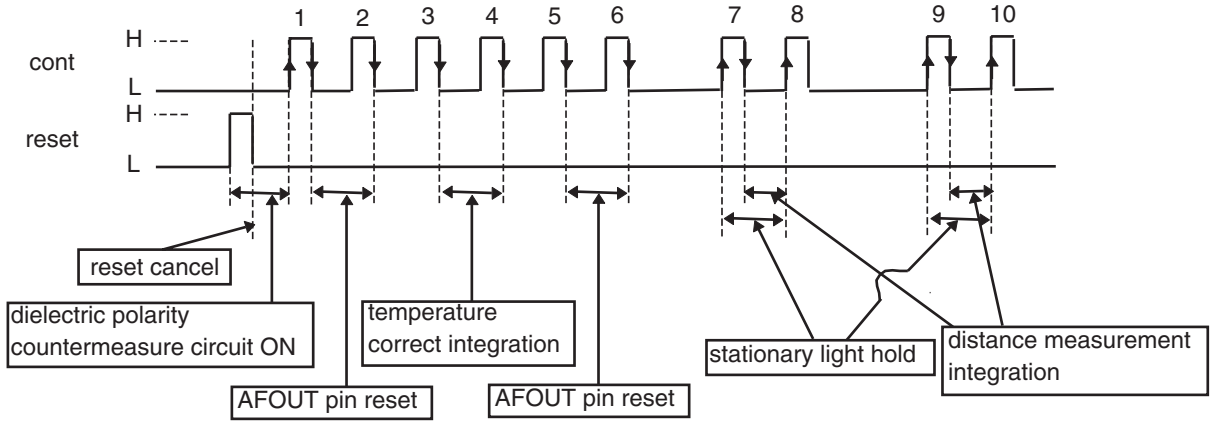
Clock value	Clamp level(Typ.)
12	1.560 nA
13	1.690 nA
14	1.820 nA
15	None clamp,Logic reset
16	0.130 nA
17	0.260 nA
18	0.390 nA
19	0.520 nA
20	0.650 nA
⋮	⋮
⋮	⋮
⋮	⋮

Clamp level is established with fall edge of input clock. It repeats the same value after 15 clock.

(3) CONT:

By the clock input of the this terminal after canceling the IC reset, it begin to control the whole IC as following function without establishing clamp level. And it repeat to switch over stationary hold and distance measurement integration current after 7th clock

a) ON / OFF of dielectric polarity countermeasure circuit integration capacitance
b) ON / OFF of CH rapid charge
c) ON / OFF of AFOUT pin reset
d) ON / OFF of temperature correct integration
e) ON / OFF of stationary light hold
f) ON / OFF of distance measurement integration



a. The dielectric polarty contermeasure of integlation capacitance:

The dielectric polarity contermeasure circuit of integration capacitance run between reset and rise edge of first CONT pin.

b. CH rapid charge:

After reset cancel, CH capacitance is charged rapidy between the fall edge of first clock and second ones.

c. AFOUT pin reset:

After reset cannel, accumulated chage at capacitance added to AFOUT pin is removed between the fall clock edges of 1 to 2 and 5 to 6.

d. Temperrature correct integlation:

After reset cannel, temperature correct integration is carried out betweeen the fall edge of 3rd clock and 4th clock. This voltage of temperature corrent integration mentioned above is maintained at AFOUT pin. This voltage is currected temperature (including time charge correct of AFOUT pin added capacotance) as compared with base voltage estabilished previously.

e. Stationaly light hold:

After 7th clock from reset cuncel (from 7th clock rise to 8th clock rise), stationary light hold is carried out over and over.

f. Distance measurement integration:

After 7th clock from reset cancel (from 7th clock fall to 8th clock rise), distance measurement integration is carried out over and over.

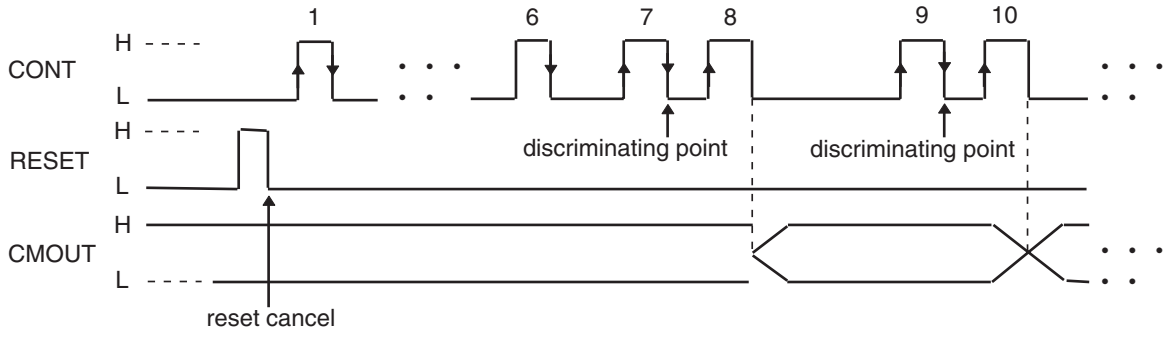
(4) AFOUT:

After reset cancel, the voltage is outputted at intervals of temperature correct integration and distance measurement integration from about 0 V to above a D range of this pin. The output is carried out linearly by integration current or integration time.

(5) CMOUT:

After the CONT pin input 7th clock fall from reset cancel, the signal current at PSDF side is distinguished from the clamp level in terms of the values. The result is outputted at each discrimination as the follows.

And after the CONT pin input 7th clock fall, the discrimination is carried out with the beginning of distance measurement start. After reset cancel, until CONT pin input 8th clock "H" is further outputted.

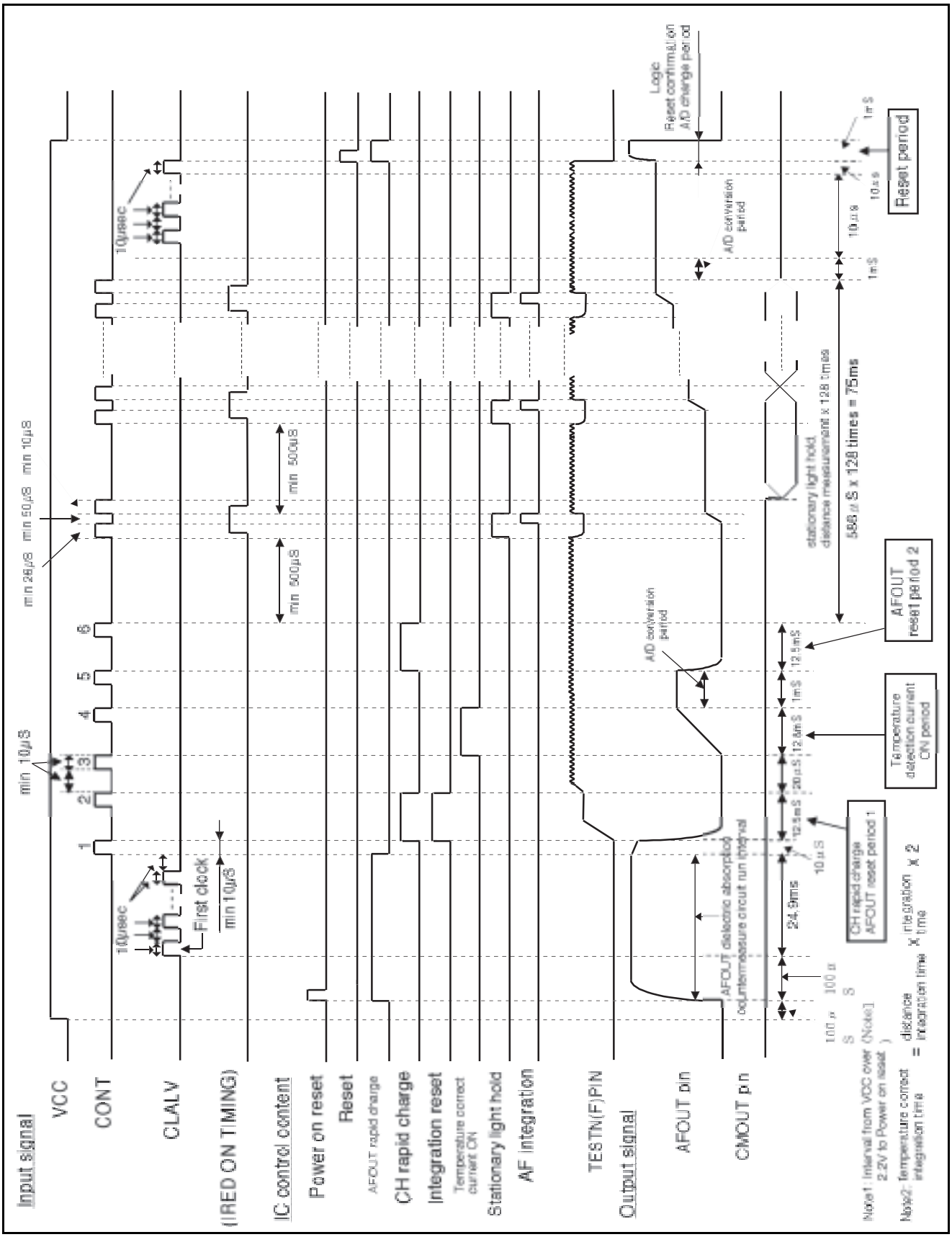


PSDF side signal current	CMOUT output
Greater than clamp level	H
Less than clamp level	L

Notes: 1. It is necessary to contact a control signal for IRED with the control signal mentioned above.

2. Connect NC terminals (4, 9, 12, 16 pin) to Vcc1 terminal or GND.

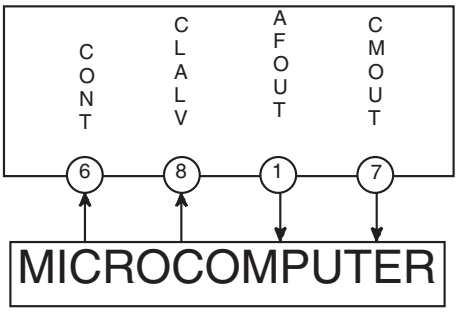
Sequential Time Chart Example



Mask Option

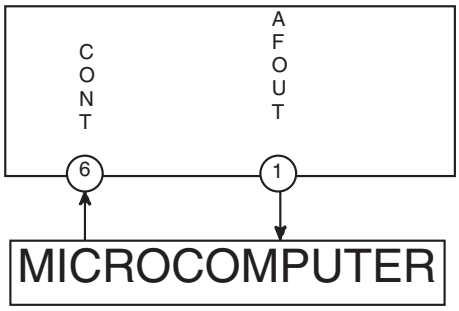
1) Control terminal variation

① Full spec (typical)



This type uses CONT,CLALV,AFOUT ,CMOUT terminal as I/F terminal to the microcomputer.
This is the typical type at M61006FP.

② Most simplified type



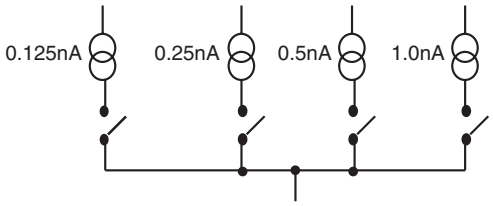
This type does not connect CLALV,CMOUT terminals to the microcomputer.
When above mentioned terminals are not connected to the microcomputer without changing mask,connect each terminal to the ground. In this case,clamp level becomes 0 And Power on reset in IC is used as reset.

③ Explanation of the terminal that can be simplified.

(a) CLALV ・・・・・ In the typical type,15 ways clamp levels can be set by the outside control,but also the terminal can be simplified by mask option as follows.

(I) Clamp level fixation ・・・・・・ Selects 1 point from 15 steps of clamp level and fixes it.

(II) Clamp level 2 step changeover ・・・・ Selects 2 points from clamp level and switches it by changing CLALV terminal HIGH/LOW. However,as selecting 2 points, there is a following constraint.



Fixes 3 parts of 4 switches corresponds to each bit in figure to ON or OFF.controls another part by CLALV terminal .

(b) CMOUT ・・・・・ When an infinity decision function shouldn't be necessary, it is possible that a CMOUT terminal is removed.

Package Dimensions

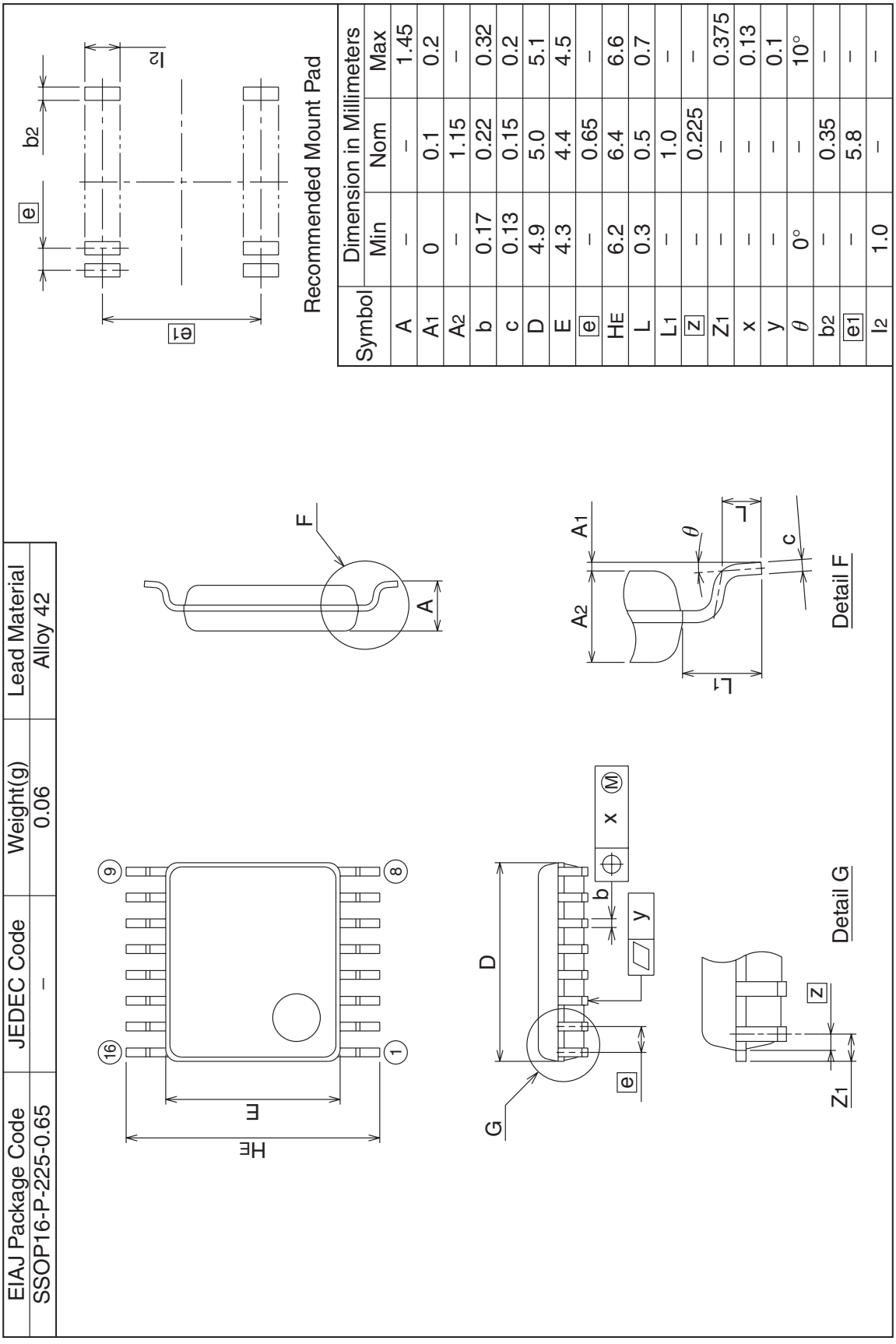
Plastic 16pin 225mil SSOP

16P2E-A

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP16-P-225-0.65	–	0.06	Alloy 42

Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.45
A_1	0	0.1	0.2
A_2	–	1.15	–
b	0.17	0.22	0.32
c	0.13	0.15	0.2
D	4.9	5.0	5.1
E	4.3	4.4	4.5
e	–	0.65	–
H_E	6.2	6.4	6.6
L	0.3	0.5	0.7
L_1	–	1.0	–
z	–	0.225	–
Z_1	–	–	0.375
x	–	–	0.13
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.35	–
e_1	–	5.8	–
l_2	1.0	–	–



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