KEYBOARD ENCODER (JIS CODE STANDARD PRODUCT)

DESCRIPTION

The M58609-04P, S is a keybord encoder for reed switches of terminal equipment. It is fabricated using P-channel aluminum-gate MOS technology and is packaged in a 40-pin DIL package. It contains a 3168-bit mask-programmable read-only memory, and the 8-bit codes specified in JIS C-6220-1969 "Codes for Information Interchange" are stored in the ROM. The output consists of an 8-bit code and a parity bit. The address is selected by the 8-bit and 11-bit ring counters.

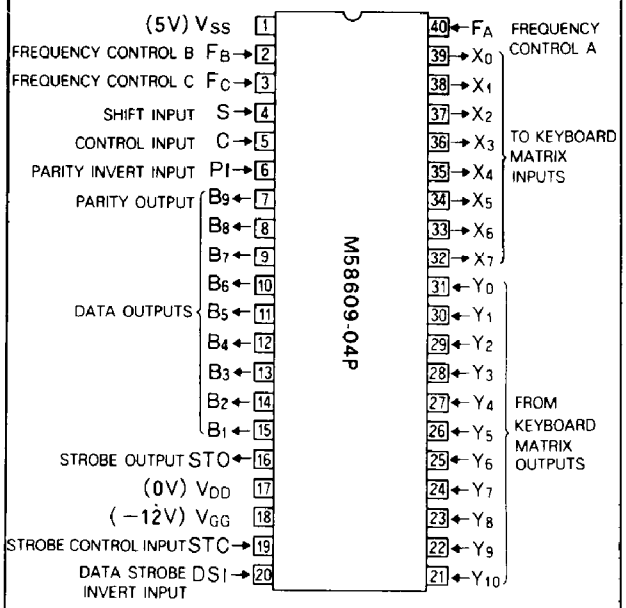
FEATURES

- TTL/DTL-compatible (except X, Y terminals)
- Two-key rollover operation
- Self-contained clock generator circuit
- Strobe delay circuit for eliminating key contact bounce
- External control for output polarity (positive or negative logic)
- External control for selecting odd or even parity

APPLICATION

- Encoder for full-keyboard terminal equipment

PIN CONFIGURATION (TOP VIEW)



Outline 40P1 (M58609-04P)
40S1 (M58609-04S)

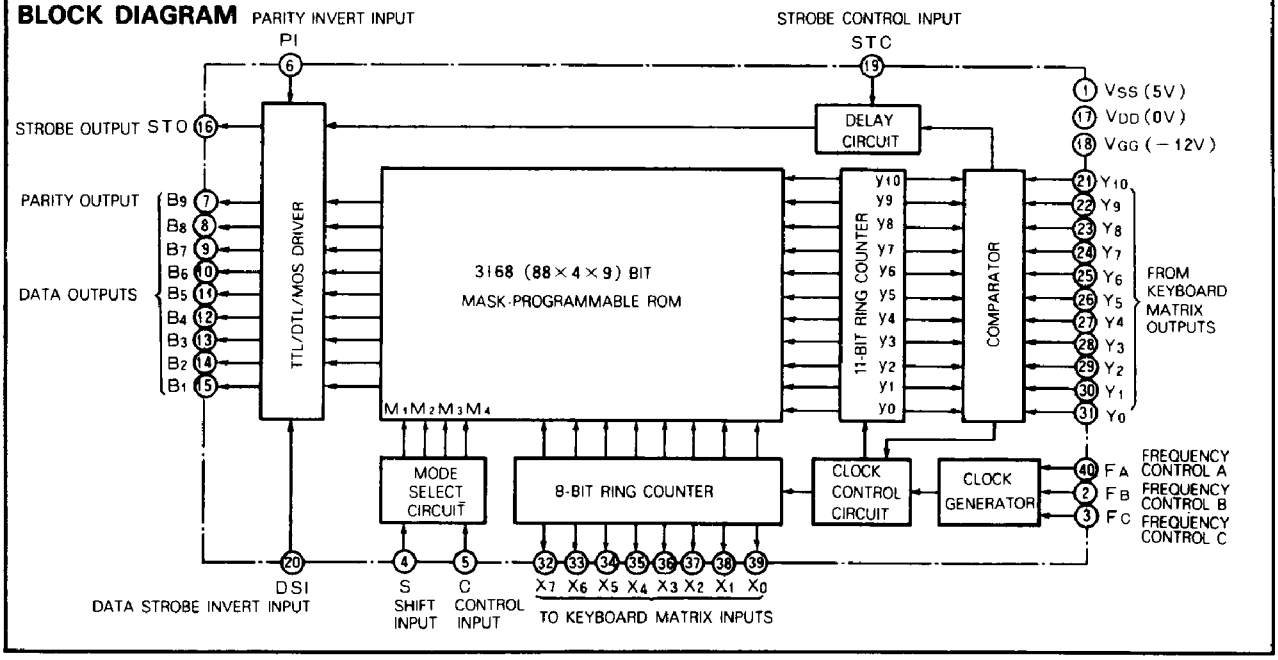
FUNCTION

Outputs (X_0~X_7) of the 8-bit ring counter and inputs (Y_0~Y_{10}) of the 11-bit comparator are wired to the keyboard to form an 8×11 (88-cross points) switch matrix.

When the key connected with X_i and Y_j is depressed, a path is formed between them. When the level of Y_j matches that of X_i, which comes from the 8-bit ring counter, the comparator generates a coincidence signal for clock control and delay circuit. This clock control stops the clock signals to the ring counter and data outputs (B_1~B_9) stabilizing the selected 9-bit code. The stabilization is indicated by a valid signal on the strobe output. A strobe output signal is generated at the time set by the externally controlled delay circuit which receives the coincidence signal. Data outputs and strobe output remain stable until the key is released.

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BLOCK DIAGRAM



M58609-04P, S

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FUNCTION (Data Output and Parity Output)

The relationships between B_1~B_8 in the code table and B_1 ~B_8 in data outputs are shown in Table 1, and those between the parity output B_9 and the parity bit, in Table 2. The parity bit in the table is defined as a '0' when the number of '1's in the code B_1~B_8 is odd and a '1' when it is even.

Mode selection is shown in Table 3.

Table 1 Relationship between code table and data outputs

B_1 ~ B_8 Code table	Data strobe invert input DSI	Data output B_1 ~ B_8	Logic
1	L	H	Positive logic
1	H	L	Negative logic
0	L	L	Positive logic
0	H	H	Negative logic

Table 2 Parity output

Parity bit	Parity invert input PI	Parity output B_9
1	L	H
1	H	L
0	L	L
0	H	H

Table 3 Mode selection

Shift input S	Control input C	Selected mode
L	L	1
H	L	2
L	H	3
H	H	4

CODE TABLE (JIS C-6220-1969)

NUMBER OF BITS										0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
										0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
										0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
										0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
B_9*	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	ROW / COL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PARITY BIT					0	0	0	0	0	NUL	DLE	SP	0	@	P	`						—	タ	ミ	
					0	0	0	1	1	SOH		!	1	A	Q					。	ア	チ	ム		
					0	0	1	0	2	STX		"	2	B	R					「	イ	ツ	メ		
					0	0	1	1	3	ETX		#	3	C	S					」	ウ	テ	モ		
					0	1	0	0	4	EOT		$	4	D	T					、	エ	ト	ヤ		
					0	1	0	1	5	ENQ	NAK	%	5	E	U					・	オ	ナ	ユ		
					0	1	1	0	6	ACK	SYN	&	6	F	V					ヲ	カ	ニ	ヨ		
					0	1	1	1	7	BEL	ETB	'	7	G	W					ァ	キ	ヌ	ラ		
					1	0	0	0	8	BS	CAN	(	8	H	X					ィ	ク	ネ	リ		
					1	0	0	1	9	HT	EM	)	9	I	Y					ゥ	ケ	ノ	ル		
					1	0	1	0	10	LF	SUB	*	:	J	Z					ェ	コ	ハ	レ		
					1	0	1	1	11	VT	ESC	+	;	K	[		{			ォ	サ	ヒ	ロ		
					1	1	0	0	12	FF		,	<	L	¥		|			ャ	シ	フ	ワ		
					1	1	0	1	13	CR		-	=	M	]		}			ュ	ス	ヘ	ン		
					1	1	1	0	14	SO		.	>	N	^		~			ョ	セ	ホ	゛		
					1	1	1	1	15	SI		/	?	O	_		DEL			ッ	ソ	マ	゜		

* B_9 is an odd parity bit for the 8-bit code (B_1 ~ B_8)

Note 1 : A '1' or '0' in the code table indicates that the output level goes high for '1' and low for '0' when input DSI and PI are low-level.

CODE ARRANGEMENT TABLE

Yi \ Xi	Mode	X0	X1	X2	X3	X4	X5	X6	X7
Y0	1	NUL	DLE	^	0	;	L	O	9
	2	NUL	DLE	ー	NUL	+	NUL	NUL	)
	3	NUL	DLE	ヘ	ワ	レ	リ	ラ	ヨ
	4	NUL	DLE	NUL	ヲ	NUL	NUL	NUL	ョ
Y1	1	SOH	6	0	ー	／	K	I	8
	2	SOH	6	0	＝	?	NUL	NUL	(
	3	SOH	6	0	ホ	メ	ノ	ニ	ユ
	4	SOH	6	0	NUL	・	NUL	NUL	ュ
Y2	1	STX	7	1	P	．	J	U	7
	2	STX	7	1	NUL	>	NUL	NUL	'
	3	STX	7	1	セ	ル	マ	ナ	ヤ
	4	STX	7	1	NUL	｡	NUL	NUL	ャ
Y3	1	ETX	8	2	「	，	H	Y	6
	2	ETX	8	2	｜	<	NUL	NUL	&
	3	ETX	8	2	°	ネ	ク	ン	オ
	4	ETX	8	2	｢	､	NUL	NUL	ォ
Y4	1	EOT	9	3	¥	M	G	T	5
	2	EOT	9	3	｜	NUL	NUL	NUL	%
	3	EOT	9	3	ー	モ	キ	カ	エ
	4	EOT	9	3	NUL	NUL	NUL	NUL	ェ
Y5	1	ENQ	NAK	4	BS	N	F	R	4
	2	ENQ	NAK	4	BS	NUL	NUL	NUL	$
	3	ENQ	NAK	4	BS	ミ	ハ	ス	ウ
	4	ENQ	NAK	4	BS	NUL	NUL	NUL	ゥ
Y6	1	ACK	SYN	5	NUL	B	D	E	3
	2	ACK	SYN	5	_	NUL	NUL	NUL	#
	3	ACK	SYN	5	口	コ	シ	イ	ア
	4	ACK	SYN	5	NUL	NUL	NUL	ィ	ァ
Y7	1	BEL	ETB	+	｝	V	S	W	2
	2	BEL	ETB	+	｜	NUL	NUL	NUL	"
	3	BEL	ETB	+	ム	ヒ	ト	テ	フ
	4	BEL	ETB	+	｣	NUL	NUL	NUL	NUL
Y8	1	=	CAN	SP	CR	C	A	Q	!
	2	=	CAN	SP	CR	NUL	NUL	NUL	!
	3	=	CAN	SP	CR	ソ	チ	タ	ヌ
	4	=	CAN	SP	CR	NUL	NUL	NUL	NUL
Y9	1	SO	EM	·	LF	X	FF	HT	@
	2	SO	EM	·	LF	NUL	FF	HT	`
	3	SO	EM	·	LF	サ	FF	HT	｀
	4	SO	EM	·	LF	NUL	FF	HT	NUL
Y10	1	SI	SUB	−	DEL	Z	ESC	VT	:
	2	SI	SUB	−	DEL	NUL	ESC	VT	*
	3	SI	SUB	−	DEL	ツ	ESC	VT	ケ
	4	SI	SUB	−	DEL	ッ	ESC	VT	NUL

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SYMBOLOGY

Symbol	Code name	Col/Row in code table	X/Y/Mode in code arrangement table
SP	Space	2 / 0	2/8/1 ~ 4
!	Exclamation mark	2 / 1	7/8/2
"	Quotation mark, umlaut	2 / 2	7/7/2
#	Number sign	2 / 3	7/6/2
$	Dollar sign	2 / 4	7/5/2
%	Percentage	2 / 5	7/4/2
&	Ampersand	2 / 6	7/3/2
'	Apostrophe, acute accent	2 / 7	7/2/2
(	Left parenthesis	2 / 8	7/1/2
)	Right parenthesis	2 / 9	7/0/2
*	Asterisk, multiplication sign	2 / 10	7/10/2
+	Positive sign, plus sign	2 / 11	2/7/1 ~ 4, 4/0/2
,	Comma	2 / 12	4/3/1
−	Negative sign, subtraction sign	2 / 13	2/10/1 ~ 4, 3/1/1
.	Period	2 / 14	2/9/1 ~ 4, 4/2/1
/	Slash, virgule, division sign, per	2 / 15	4/1/1
:	Colon	3 / 10	7/10/1
;	Semicolon	3 / 11	4/0/1
<	Less than sign	3 / 12	4/3/2
=	Equal sign	3 / 13	0/8/1 ~ 4, 3/1/2
>	Greater than sign	3 / 14	4/2/2

Symbol	Code name	Col/Row in code table	X/Y/Mode in code arrangement table
?	Question mark	3 / 15	4/1/2
@	At mark	4 / 0	7/9/1
{	Left bracket	5 / 11	3/3/1
¥	Yen sign	5 / 12	3/4/1
}	Right bracket	5 / 13	3/7/1
^	Circumflex accent	5 / 14	2/0/1
_	Underline	5 / 15	3/6/2
`	Grave accent	6 / 0	7/9/2
{	Left brace	7 / 11	3/3/2
|	Separate sign, logical add sign	7 / 12	3/4/2
}	Right brace	7 / 13	3/7/2
~	Overline, logical not sign	7 / 14	2/0/2
｡	Japanese period	10 / 1	4/2/4
｢	Japanese initial quotation mark	10 / 2	3/3/4
｣	Japanese final quotation mark	10 / 3	3/7/4
､	Japanese comma	10 / 4	4/3/4
・	Middle dot	10 / 5	4/1/4
ー	Long vowel mark	11 / 0	3/4/3
゛	Voiced consonant mark	13 / 14	7/9/3
゜	Semi-voiced consonant mark	13 / 15	3/3/3

KEYBOARD ENCODER (JIS CODE STANDARD PRODUCT)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{GG}	Supply voltage	With respect to V_{SS}	0.3~−20	V
V_{DD}	Supply voltage		0.3~−20	V
V_I	Input voltage		0.3~−20	V
Topr	Operating free-air temperature range		−20~75	°C
Tstg	Storage temperature range		−40~125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20~75°C, unless otherwise noted)

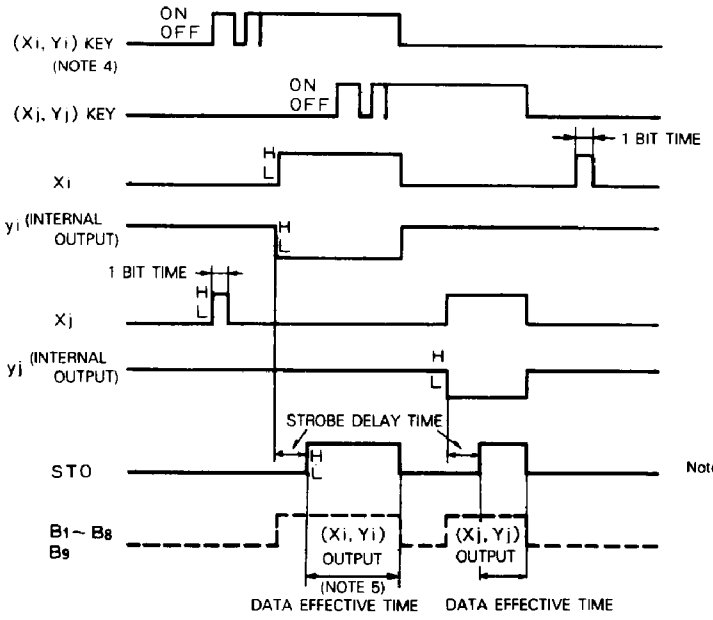
	Parameter	Limits			Unit
		Min	Nom	Max	
V_{GG}	Supply voltage	−11	−12	−13	V
V_{DD}	Supply voltage		0		V
V_{SS}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{SS}−1			V
V_{IL}	Low-level input voltage			0.8	V
$f_{(\phi)}$	Clock frequency	20	50	100	kHz
$t_{D(STO)}$	Strobe delay time		1.5		ms
R_{OFF}	Switch off resistance	10			MΩ
R_{ON}	Switch on resistance			300	Ω

ELECTRICAL CHARACTERISTICS (Ta = −20~75°C, V_{GG} = −12±1V, V_{SS} = 5±0.5V, V_{DD} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{OH(B_1,STO)}$	High-level output voltage, B_1~B_9 and STO	I_{OH} = −100μA	V_{SS}−1			V
$V_{OH(X_i)}$	High-level output voltage, X_0~X_7	I_{OH} = −100μA	V_{SS}−1.3			V
$V_{OL(B_1,STO)}$	Low-level output voltage, B_1~B_9 and STO	I_{OL} = 1.6mA			0.4	V
$V_{OL(X_i)}$	Low-level output voltage, X_0~X_7	I_{OL} = 1μA			−3	V
R_I	Input resistance, S. C. DSI and PI	V_I = −12V	1			MΩ
Pd	Power dissipation	Ta = 25°C		70	200	mW
C_I	Input capacitance	V_I = 0V, f = 1MHz, Ta = 25°C			15	pF

Note 2 : Current flowing into an IC is positive; out is negative.

TIMING DIAGRAM



Note 3 : DSI = "L"

4 : (Xi, Yi) KEY indicates the key switch that is located at the cross point of Xi and Yi of the keyboard matrix.

5 : (Xi, Yi) OUTPUT indicates the code output of the key that is selected by the (Xi, Yi) KEY.

FUNCTION TABLES

Data (B_1 ~ B_9) Invert

DSI (Pin ⑳)	Code table (B_1 ~ B_9)	Data output (B_1 ~ B_9)
H	1	L
L	1	H
H	0	H
L	0	L

Strobe (STO) Invert

DSI (Pin ⑳)	Internal strobe (Note 3)	STO (Pin ⑯)
H	H	L
L	H	H
H	L	H
L	L	L

Parity (B_9) Invert

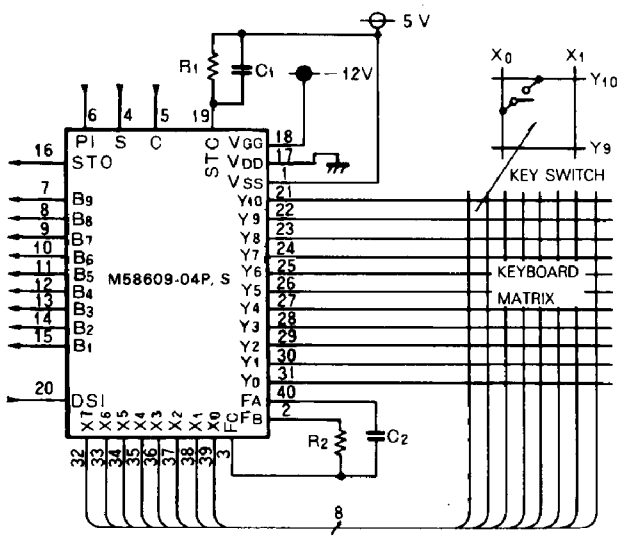
PI (Pin ⑤)	Code table (B_9)	B_9 (Pin ⑦)
H	1	L
L	1	H
H	0	H
L	0	L

Mode Select

S (Pin ④)	C (Pin ⑤)	Mode
L	L	M1
H	L	M2
L	H	M3
H	H	M4

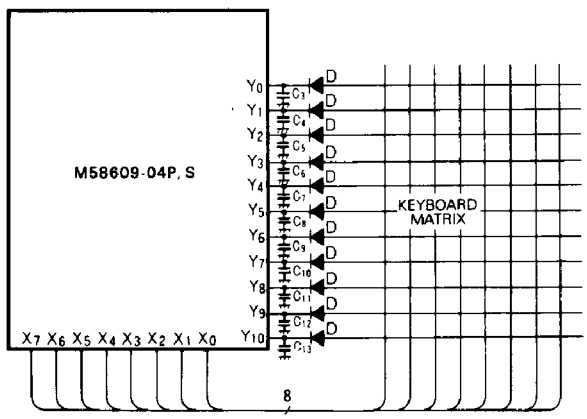
Note 6 : The internal signal of the strobe output (STO) becomes high-level when the strobe signal is generated.

TYPICAL APPLICATION CIRCUIT



Note 7 : $R_1 = 1.5M\Omega$, $C_1 = 0.001\mu F$ provides approximately 1.5ms delay time.
8 : $R_2 = 75k\Omega$, $C_2 = 50pF$ provides approximately 50kHz clock frequency.

Fig. 1 Measures against coupling



Insert diodes and capacitors (C_3 ~ C_{13} should be approx. 50 ~ 100pF) between the keyboard matrix and the Y inputs.

Cautions in Use

1. Coupling at the Keyboard Matrix

Depending on the capacitance of the keyboard matrix wiring, depressing one key while another is depressed gives rise to capacitance coupling, which may result in repetition of the strobe output, the same condition that would occur if a single key were depressed twice. In this case, proceed as shown in Fig. 1.

2. N-Key Rollover

This device is for 2-key rollover; when 3 or more keys are depressed simultaneously, code output is indeterminate.

3. Maximum Chatter Times

1. With Key Off (t_{KOFF})

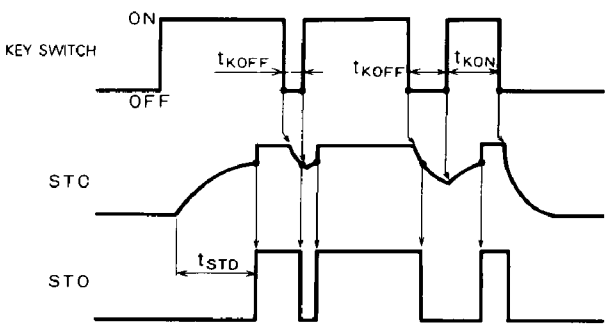
t_{KOFF} is defined as the maximum time that, when a key is turned on but because of faulty contact, etc. the key input signal chatters, the chattering can be disregarded. This may vary according to ambient temperature, power supply conditions, etc., but is approximately 100ns.

2. With Key On (t_{KON})

Conversely, t_{KON} is the maximum time that, when a key is turned off, but the input signal chatters, the chattering condition can be disregarded.

when $t_{KOFF} \leqq 1/f_\phi$ $t_{KON} \leqq 100ns$
when $t_{KOFF} > 1/f_\phi$ $t_{KON} \leqq t_{STD} + t_{SC}$
where: f_ϕ = clock frequency
t_{STD} = strobe delay time
t_{SC} = scanning time

Fig. 2 Timing diagram for maximum chatter time

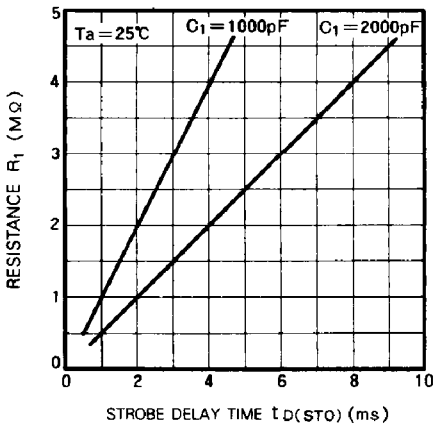


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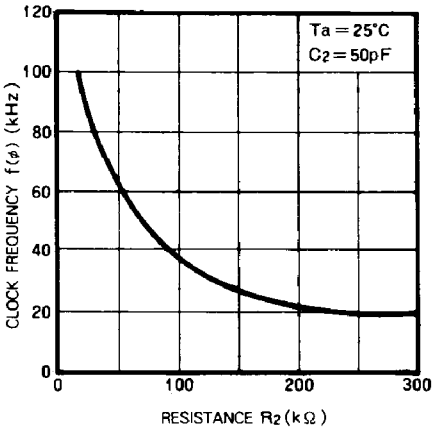
KEYBOARD ENCODER (JIS CODE STANDARD PRODUCT)

TYPICAL CHARACTERISTICS (V_{GG} = −12V, V_{DD} = 0 V, V_{SS} = 5 V)

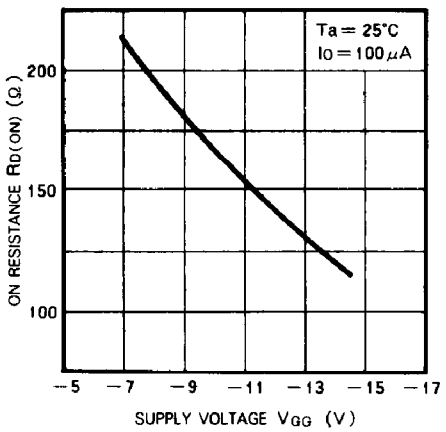
RESISTANCE VS. STROBE DELAY TIME



CLOCK FREQUENCY VS. RESISTANCE



ON RESISTANCE OF OUTPUT DRIVER VS. POWER SUPPLY VOLTAGE



POWER DISSIPATION VS. AMBIENT TEMPERATURE

