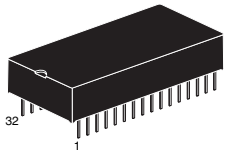
M48Z512BV

3.3 V, 4 Mbit (512 K x 8 bit) ZEROPOWER® SRAM

Features

- Integrated, ultra-low power SRAM, power-fail control circuit, and battery
- Conventional SRAM operation; unlimited WRITE cycles
- 10 years of data retention in the absence of power
- Automatic power-fail chip deselect and WRITE protection
- 3.0 to 3.6 V operation
  - 2.9 V power-fail deselect
- Pin and function compatible with JEDEC standard 512 K x 8 SRAMs
- PMDIP32 is an ECOPACK® package
- For 5 V applications, refer to the M48Z512A



PMDIP32 (PM) module

Description

The M48Z512BV ZEROPOWER® RAM is a non-volatile, 4,194,304-bit static RAM organized as 524,288 words by 8 bits. The devices combine an internal lithium battery, a CMOS SRAM and a control circuit in a plastic, 32-pin DIP module.

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1 Device overview

Figure 1. Logic diagram

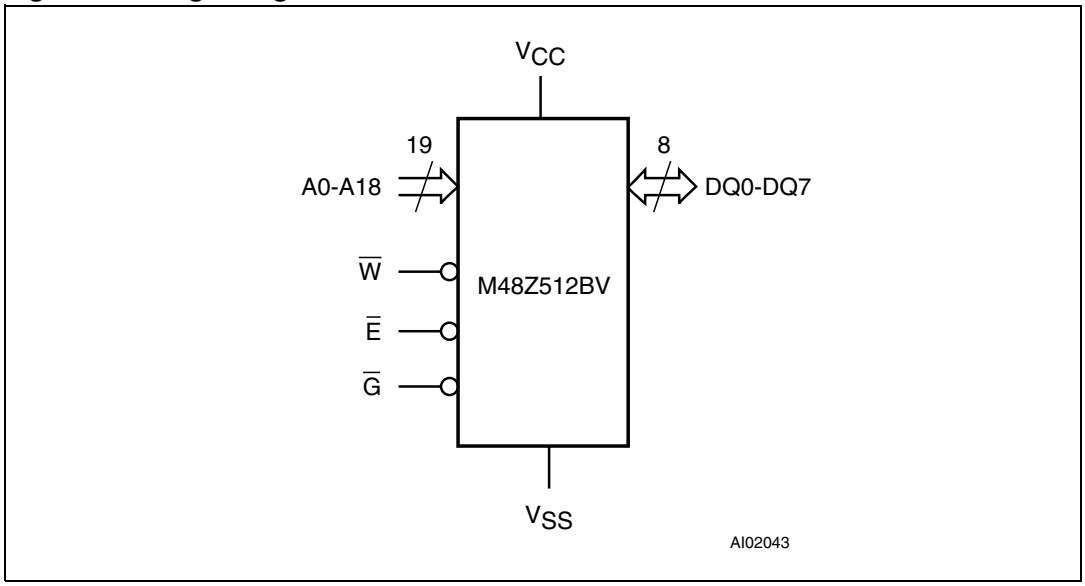


Table 1. Signal names

A0-A18	Address inputs
DQ0-DQ7	Data inputs/outputs
$\overline{E}$	Chip enable input
$\overline{G}$	Output enable input
$\overline{W}$	WRITE enable input
V_{CC}	Supply voltage
V_{SS}	Ground

Figure 2. DIP connections

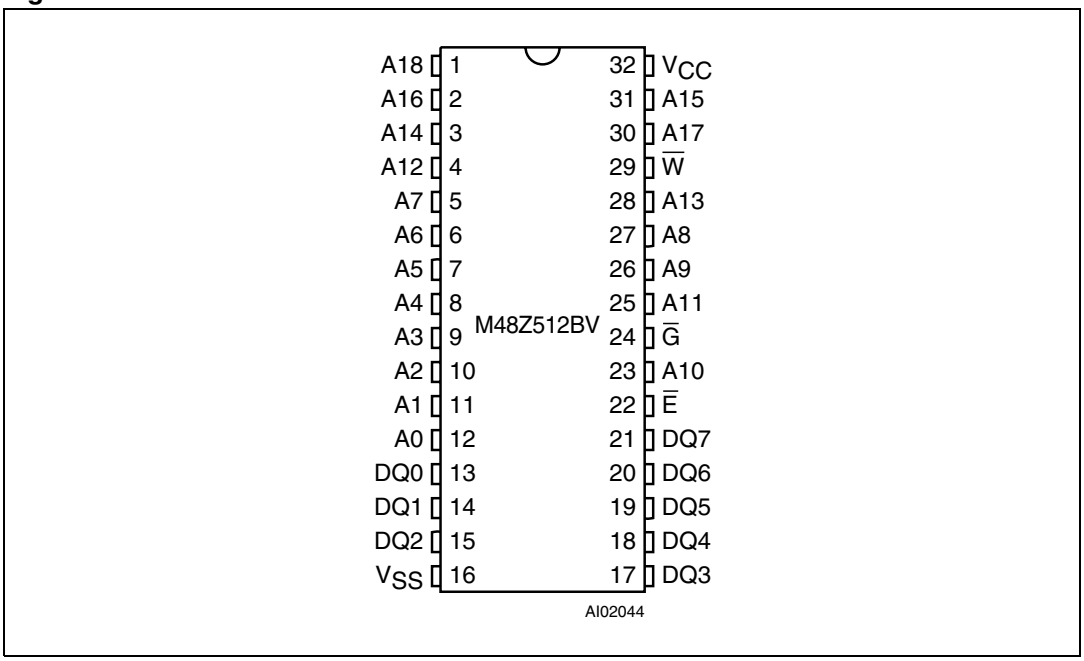
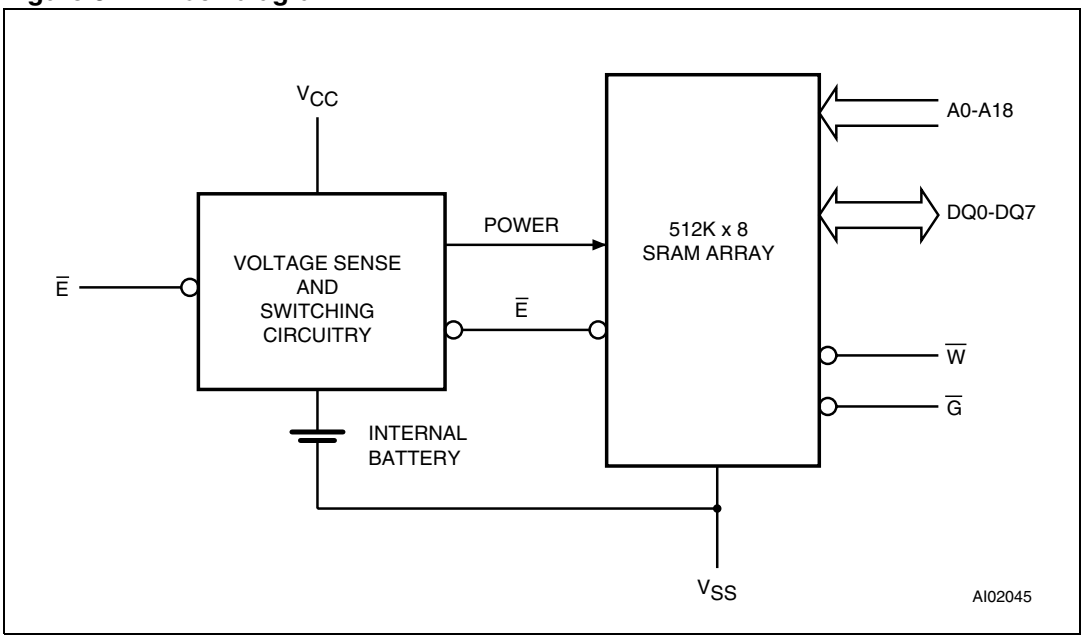


Figure 3. Block diagram



2 Operating modes

The M48Z512BV also has its own power-fail detect circuit. The control circuitry constantly monitors the single V_{CC} supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit WRITE protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below the switchover voltage (V_{SO}), the control circuitry connects the battery which maintains data until valid power returns.

The ZEROPOWER® RAM replaces industry standard SRAMs. It provides the nonvolatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed.

Table 2. Operating modes(1)

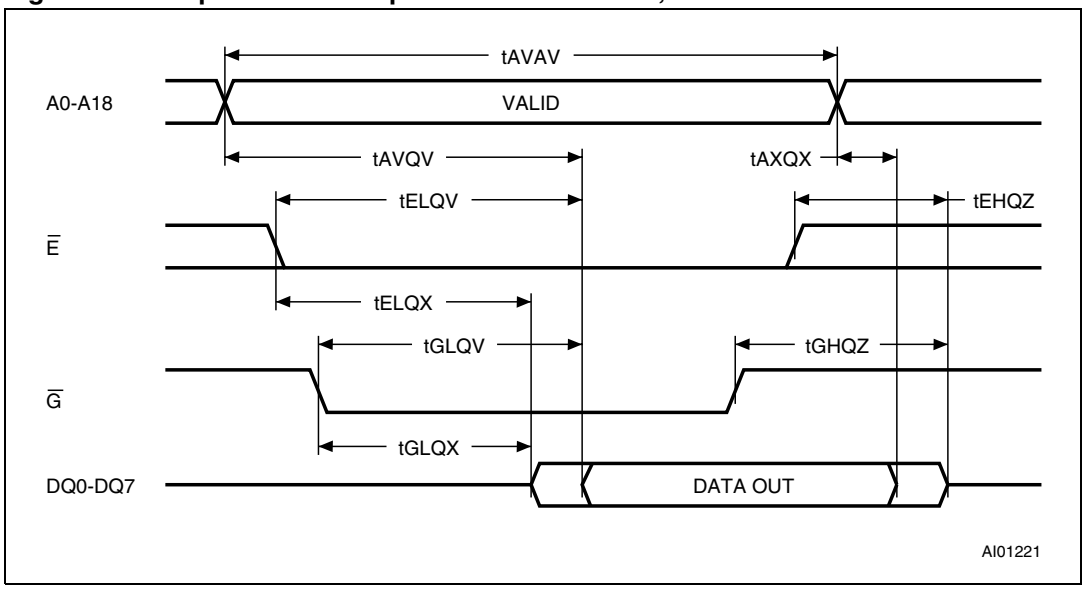
Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	3.0 to 3.6 V	V_{IH}	X	X	High Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)(2)	X	X	X	High Z	CMOS standby
Deselect	$\leq V_{SO}$(2)	X	X	X	High Z	Battery backup mode

1. See *Table 10 on page 16* for details.
2. X = V_{IH} or V_{IL}; V_{SO} = battery backup switchover voltage.

2.1 READ mode

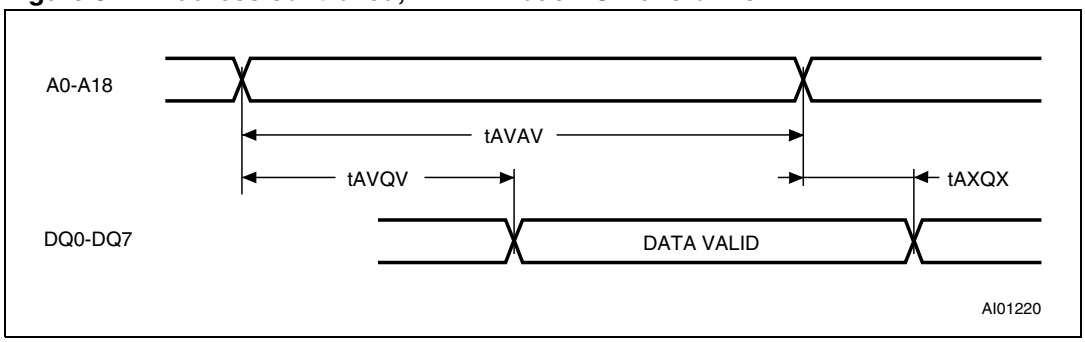
The M48Z512BV is in the READ mode whenever $\overline{W}$ (WRITE enable) is high and $\overline{E}$ (chip enable) is low. The device architecture allows ripple-through access of data from eight of 4,194,304 locations in the static storage array. Thus, the unique address specified by the 19 address inputs defines which one of the 524,288 bytes of data is to be accessed. Valid data will be available at the data I/O pins within address access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ (chip enable) and $\overline{G}$ (output enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of chip enable access time (t_{ELQV}) or output enable access time (t_{GLQV}). The state of the eight three-state data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the address inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for output data hold time (t_{AXQX}) but will go indeterminate until the next address access.

Figure 4. Chip enable or output enable controlled, READ mode AC waveforms



1. WRITE enable ($\overline{W}$) = high.

Figure 5. Address controlled, READ mode AC waveforms



1. Chip enable ($\overline{E}$) and output enable ($\overline{G}$) = low, WRITE enable ($\overline{W}$) = high.

Table 3. READ mode AC characteristics

Symbol	Parameter[1]	Min	Max	Unit
t_{AVAV}	READ cycle time	85		ns
t_{AVQV}	Address valid to output valid		85	ns
t_{ELQV}	Chip enable low to output valid		85	ns
t_{GLQV}	Output enable low to output valid		45	ns
t_{ELQX}[2]	Chip enable low to output transition	5		ns
t_{GLQX}[2]	Output enable low to output transition	5		ns
t_{EHQZ}[2]	Chip enable high to output Hi-Z		35	ns
t_{GHQZ}[2]	Output enable high to output Hi-Z		25	ns
t_{AXQX}	Address transition to output transition	5		ns

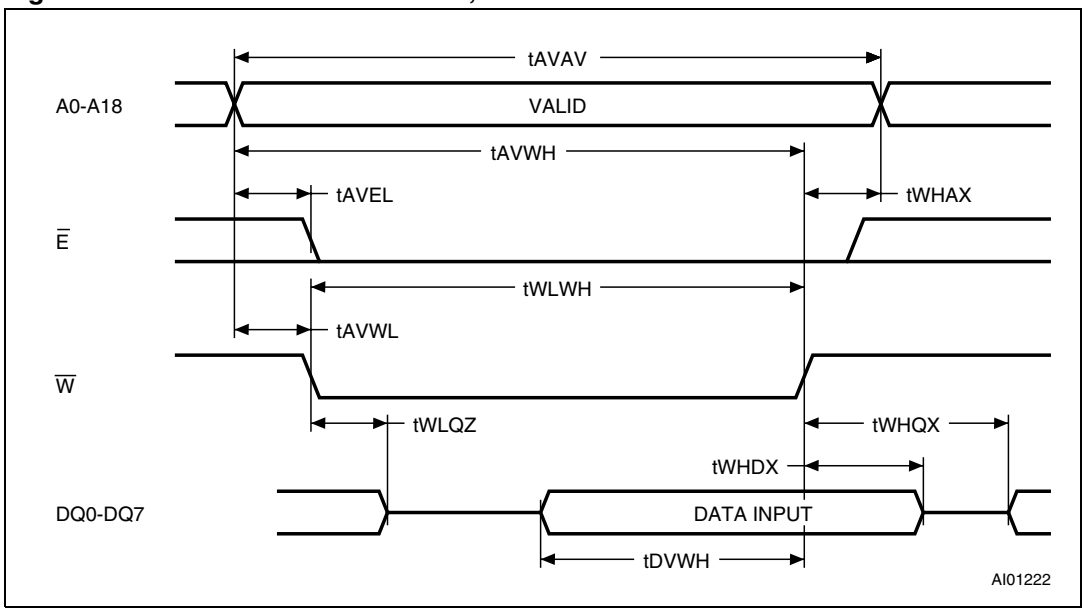
1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6 V (except where noted).
2. C_L = 5 pF.

2.2 WRITE mode

The M48Z512BV is in the WRITE mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$.

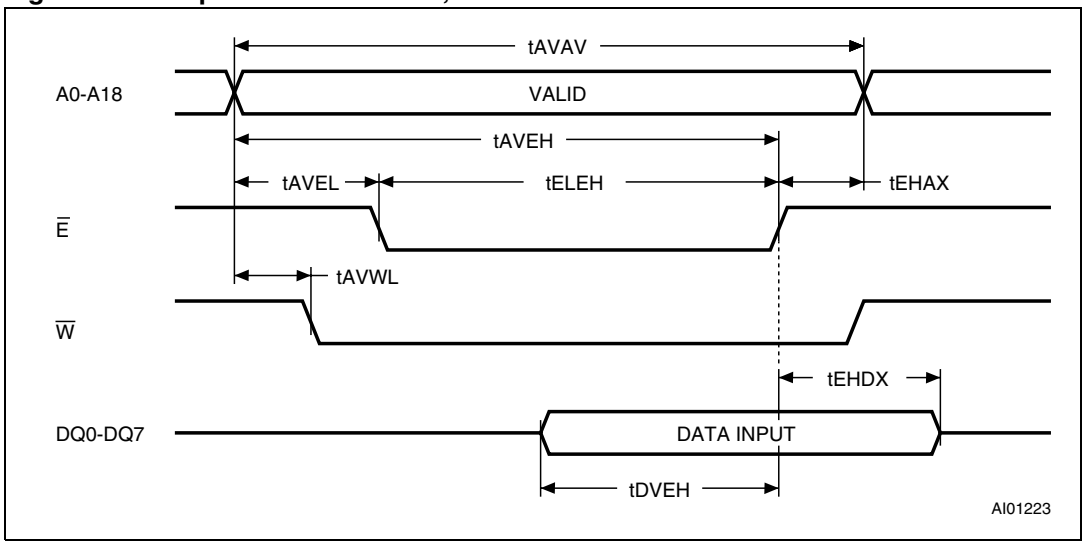
The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVEH} or t_{DVWH} prior to the end of WRITE and remain valid for t_{EHDX} or t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 6. WRITE enable controlled, WRITE AC waveforms



1. Output enable ($\overline{G}$) = high.

Figure 7. Chip enable controlled, WRITE AC waveforms



1. Output enable ($\overline{G}$) = high.

Table 4. WRITE mode AC characteristics

Symbol	Parameter[1]	Min	Max	Unit
t_{AVAV}	WRITE cycle time	85		ns
t_{AVWL}	Address valid to WRITE enable low	0		ns
t_{AVEL}	Address valid to chip enable low	0		ns
t_{WLWH}	WRITE enable pulse width	65		ns
t_{ELEH}	Chip enable low to chip enable high	75		ns
t_{WHAX}	WRITE enable high to address transition	5		ns
t_{EHAX}	Chip enable high to address transition	15		ns
t_{DVWH}	Input valid to WRITE enable high	35		ns
t_{DVEH}	Input valid to chip enable high	35		ns
t_{WHDX}	WRITE enable high to input transition	0		ns
t_{EHDX}	Chip enable high to input transition	10		ns
t_{WLQZ}[2][3]	WRITE enable low to output Hi-Z		30	ns
t_{AVWH}	Address valid to WRITE enable high	75		ns
t_{AVEH}	Address valid to chip enable high	75		ns
t_{WHQX}[2][3]	WRITE enable high to output transition	5		ns

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6 V (except where noted).
2. C_L = 5 pF.
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

2.3 Data retention mode

With valid V_{CC} applied, the M48Z512BV operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, WRITE protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as “don't care.”

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, WRITE protection takes place. When V_{CC} drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data.

The internal coin cell will maintain data in the M48Z512BV after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. WRITE protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

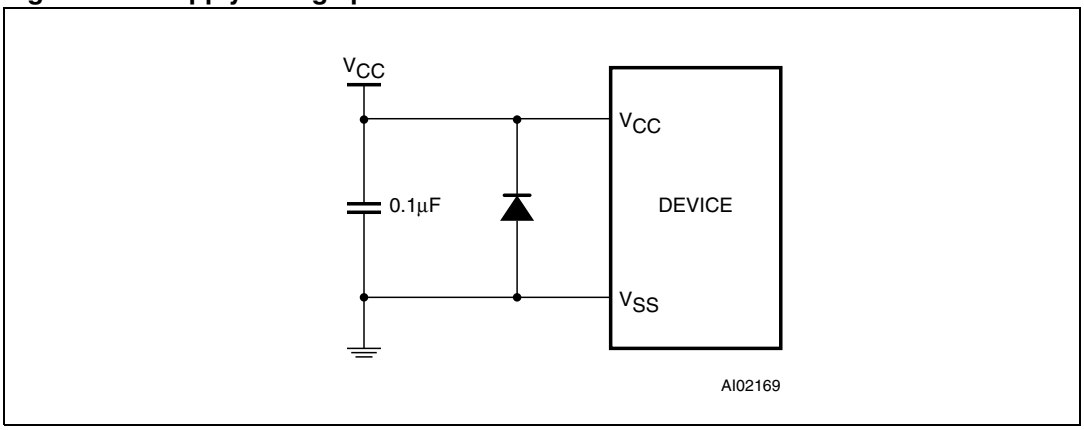
For more information on battery storage life refer to the application note AN1012.

2.4 V_{CC} noise and negative going transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1 µF (see *Figure 8*) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, ST recommends connecting a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). (Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface-mount).

Figure 8. Supply voltage protection



3 Maximum ratings

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_A	Ambient operating temperature	0 to 70	°C
T_{STG}	Storage temperature (V_{CC} off)	–40 to 85	°C
T_{BIAS}	Temperature under bias	0 to 70	°C
T_{SLD} (1)	Lead solder temperature for 10 seconds	260	°C
V_{IO}	Input or output voltages	–0.3 to 4.6	V
V_{CC}	Supply voltage	–0.3 to 4.6	V
I_O	Output current	20	mA
P_D	Power dissipation	1	W

1. For DIP package: soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds). No preheating above 150°C, or direct exposure to IR reflow (or IR preheat) allowed, to avoid damaging the Lithium battery.

Caution: *Negative undershoots below –0.3 V are not allowed on any pin while in the battery backup mode.*

4 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the dc and ac characteristics of the device. The parameters in the following dc and ac characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 6. Operating and AC measurement conditions(1)

Parameter	Value	Unit
Supply voltage (V_{CC})	3.0 to 3.6	V
Ambient operating temperature (T_A)	0 to 70	°C
Load capacitance (C_L)	50	pF
Input rise and fall times	≤ 5	ns
Input pulse voltages	0 to 3	V
Input and output timing ref. voltages	1.5	V

1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 9. AC measurement load circuit

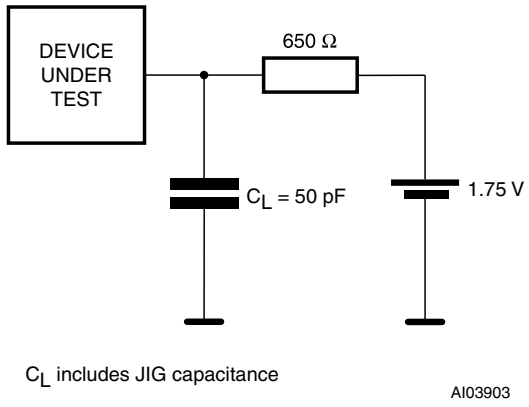


Table 7. Capacitance

Symbol	Parameter(1)(2)	Min	Max	Unit
C_{IN}	Input capacitance		10	pF
C_{IO}(3)	Input/output capacitance		10	pF

1. Effective capacitance measured with power supply at 3.3 V; sampled only, not 100% tested.
2. Outputs deselected.
3. At 25°C.

Table 8. DC characteristics

Sym	Parameter	Test condition(1)	Min	Max	Unit
I_{LI}(2)	Input leakage current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}(2)	Output leakage current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC}	Supply current	$\overline{E} = V_{IL}$ outputs open		50	mA
I_{CC1}	Supply current (standby) TTL	$\overline{E} = V_{IH}$		4	mA
I_{CC2}	Supply current (standby) CMOS	$\overline{E} \ge V_{CC} - 0.2V$		3	mA
V_{IL}	Input low voltage		–0.3	0.6	V
V_{IH}	Input high voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output high voltage	I_{OH} = –1mA	2.2		V

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6 V (except where noted).
2. Outputs deselected.

Table 9. Power down/up AC characteristics

Symbol	Parameter[1]	Min	Typ	Max	Unit
t_F	V_{CC} fall time, V_{PFD} to V_{SS}	150			µs
t_R	V_{CC} rise time, V_{SS} to V_{PFD}	150			µs
t_{WP}	WRITE protect time		25		µs
t_{ER}	$\overline{E}$ recovery time	70		140	ms

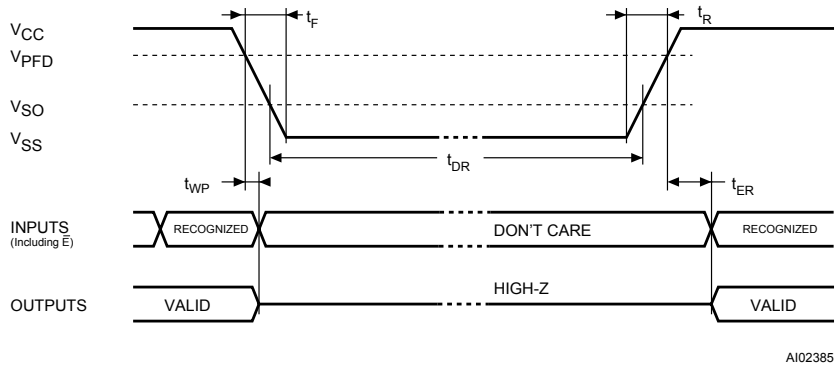
1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6 V (except where noted).

Table 10. Power down/up trip points DC characteristics

Symbol	Parameter[1][2]	Min	Typ	Max	Unit
V_{PFD}	Power-fail deselect voltage	2.8	2.9	3.0	V
V_{SO}	Battery backup switchover voltage		2.4		V
t_{DR}[3]	Expected data retention time	10			Years

1. All voltages referenced to V_{SS}.
2. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6 V (except where noted).
3. At 25°C, V_{CC} = 0 V.

Figure 10. Power down/up mode AC waveforms

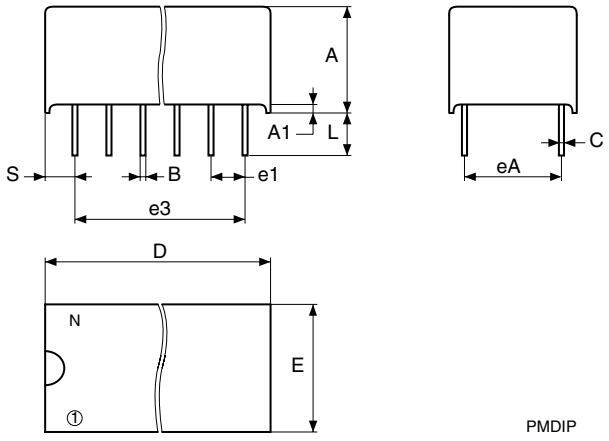


5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at: www.st.com.

Figure 11. PMDIP32 – 32-pin plastic DIP module, package outline



1. Drawing is not to scale.

Table 11. PMDIP32 – 32-pin plastic DIP module, package mechanical data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		9.27	9.52		0.365	0.375
A1		0.38			0.015	
B		0.43	0.59		0.017	0.023
C		0.20	0.33		0.008	0.013
D		42.42	43.18		1.670	1.700
E		18.03	18.80		0.710	0.740
e1		2.29	2.79		0.090	0.110
e3	38.10			1.50		
eA		14.99	16.00		0.590	0.630
L		3.05	3.81		0.120	0.150
S		1.91	2.79		0.075	0.110
N	32			32		

6 Part numbering

Table 12. Ordering information scheme

Example: M48Z 512BV –85 PM 1

Device type

M48Z

Supply voltage and WRITE protect voltage

512BV: V_{CC} = 3.0 to 3.6 V; V_{PFD} = 2.8 to 3.0 V

Speed

–85 = 85 ns

Package

PM = PMDIP32

Temperature range

1 = 0 to 70°C

Shipping method

blank = ECOPACK® package, tubes

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

7 Revision history

Table 13. Document revision history

Date	Revision	Changes
15-Aug-2008	1	Initial release

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