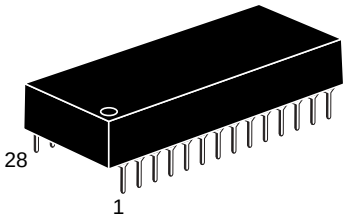
# M48T35AY
# M48T35AV

## 5.0 or 3.3V, 256 Kbit (32 Kb x8) TIMEKEEPER® SRAM

## FEATURES SUMMARY

- INTEGRATED, ULTRA LOW POWER SRAM, REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT AND BATTERY
- BYTEWIDE™ RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES, AND SECONDS
- BATTERY LOW FLAG ($\overline{BOK}$)
- FREQUENCY TEST OUTPUT FOR REAL TIME CLOCK
- AUTOMATIC POWER-FAIL CHIP DESELECT AND WRITE PROTECTION
- WRITE PROTECT VOLTAGES
  ($V_{PFD}$ = Power-fail Deselect Voltage):
  - M48T35AY: $V_{CC}$ = 4.5 to 5.5V
    $4.2V \leq V_{PFD} \leq 4.5V$
  - M48T35AV: $V_{CC}$ = 3.0 to 3.6V
    $2.7V \leq V_{PFD} \leq 3.0V$
- SELF-CONTAINED BATTERY AND CRYSTAL IN THE CAPHAT™ DIP PACKAGE
- SOIC PACKAGE PROVIDES DIRECT CONNECTION FOR A SNAPHAT® HOUSING CONTAINING THE BATTERY AND CRYSTAL
- SNAPHAT® HOUSING (BATTERY AND CRYSTAL) IS REPLACEABLE
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 32Kb x8 SRAMs

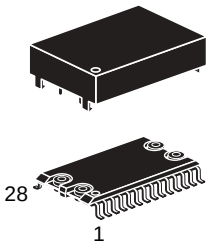
**Figure 1. 28-pin, PCDIP CAPHAT™ Package**




PCDIP28 (PC)
Battery/Crystal
CAPHAT

**Figure 2. 28-pin SOIC Package**

SNAPHAT (SH)
Battery/Crystal




SOH28 (MH)

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## SUMMARY DESCRIPTION

The M48T35AY/V TIMEKEEPER® RAM is a 32Kb x 8 non-volatile static RAM and real time clock. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory and real time clock solution.

The M48T35AY/V is a non-volatile pin and function equivalent to any JEDEC standard 32Kb x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed.

The 28-pin, 600mil DIP CAPHAT™ houses the M48T35AY/V silicon with a quartz crystal and a long-life lithium button cell in a single package.

The 28-pin, 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT® housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SOIC and battery/crystal packages are shipped separately in plastic anti-static tubes or in Tape & Reel form.

For the 28-lead SOIC, the battery/crystal package (e.g. SNAPHAT) part number is “M4T28-BR12SH” (see Table 17., page 23).

**Figure 3. Logic Diagram**

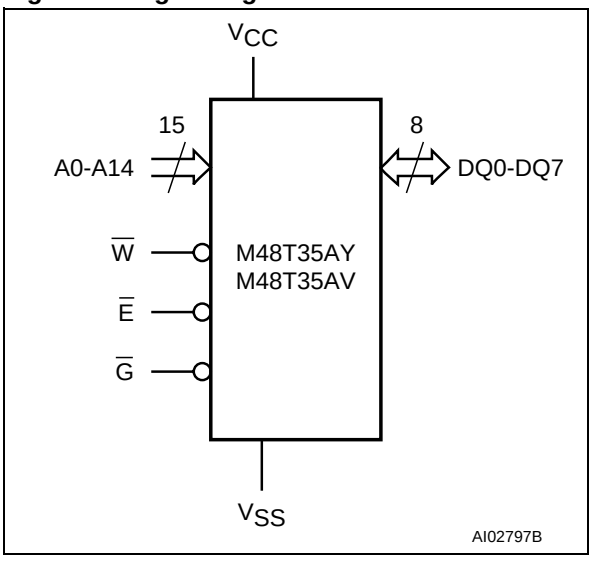



**Table 1. Signal Names**

| | |
|---|---|
| A0-A14 | Address Inputs |
| DQ0-DQ7 | Data Inputs / Outputs |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| $\overline{W}$ | WRITE Enable |
| $V_{CC}$ | Supply Voltage |
| $V_{SS}$ | Ground |

**Figure 4. DIP Connections**

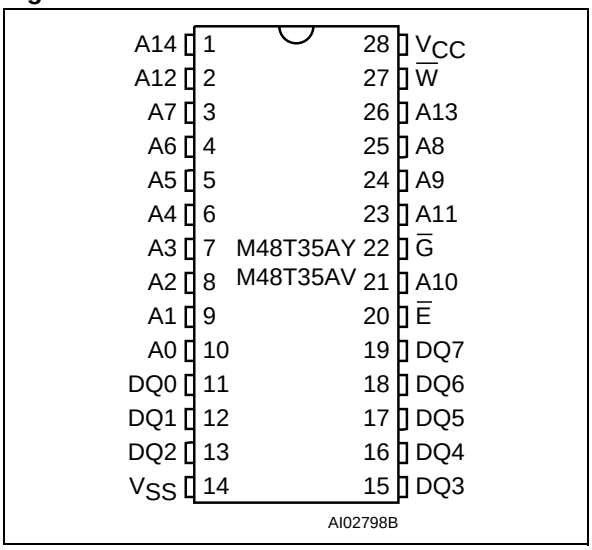



**Figure 5. SOIC Connections**

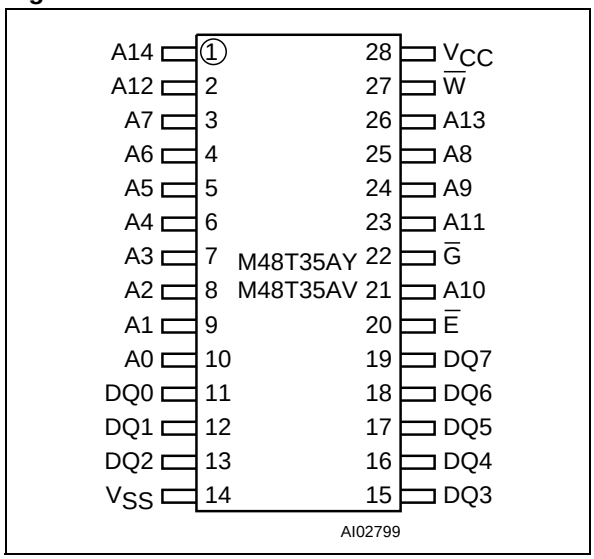
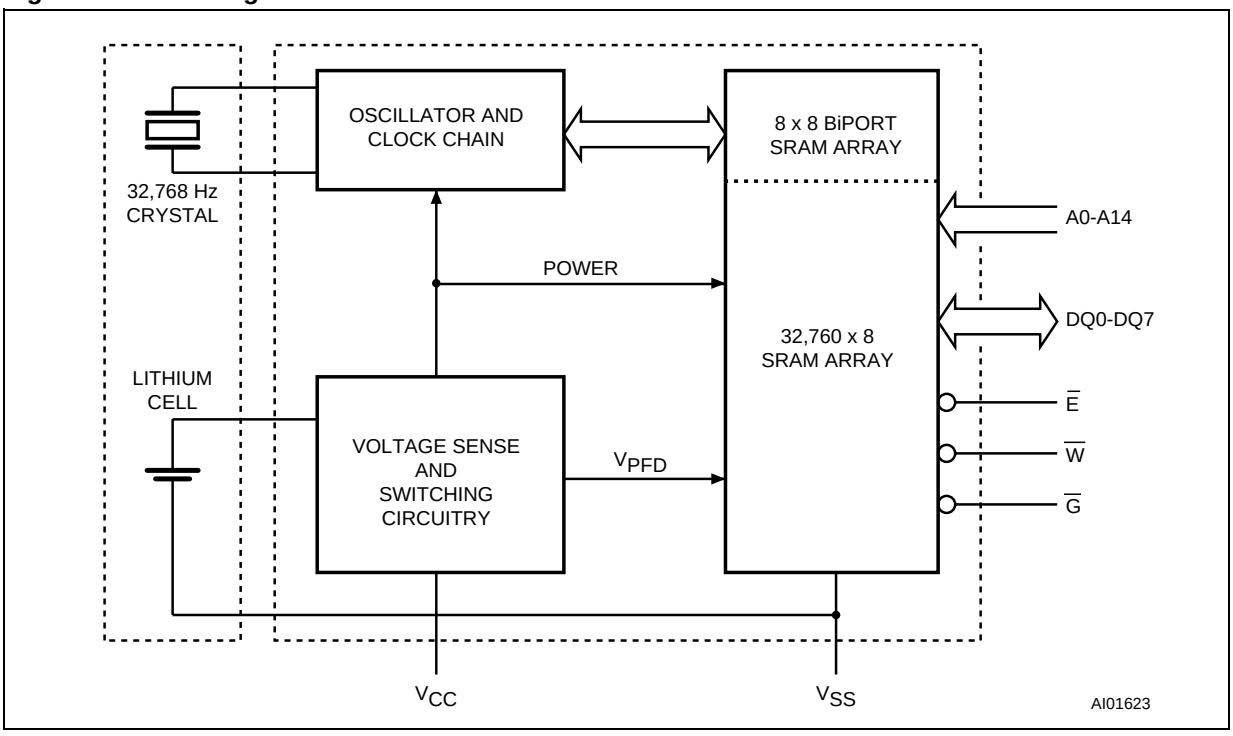



**Figure 6. Block Diagram**



## OPERATION MODES

As Figure 6., page 5 shows, the static memory array and the quartz controlled clock oscillator of the M48T35AY/V are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 7FF8h-7FFFh.

The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year - valid until 2100), 30, and 31 day months are made automatically. Byte 7FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ READ/WRITE memory cells. The M48T35AY/V includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T35AY/V also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 3V supply for an out of tolerance condition. When $V_{CC}$ is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low $V_{CC}$. As $V_{CC}$ falls below the Battery Back-up Switchover Voltage ($V_{SO}$), the control circuitry connects the battery which maintains data and clock operation until valid power returns.

**Table 2. Operating Modes**

| Mode | $V_{CC}$ | $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | DQ0-DQ7 | Power |
|---|---|---|---|---|---|---|
| Deselect | 4.5 to 5.5V or 3.0 to 3.6V | $V_{IH}$ | X | X | High Z | Standby |
| WRITE | | $V_{IL}$ | X | $V_{IL}$ | $D_{IN}$ | Active |
| READ | | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ | Active |
| READ | | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | High Z | Active |
| Deselect | $V_{SO}$ to $V_{PFD}$ (min)(1) | X | X | X | High Z | CMOS Standby |
| Deselect | $\leq V_{SO}$(1) | X | X | X | High Z | Battery Back-up Mode |

Note: X = $V_{IH}$ or $V_{IL}$; $V_{SO}$ = Battery Back-up Switchover Voltage.

1. See Table 11., page 18 for details.

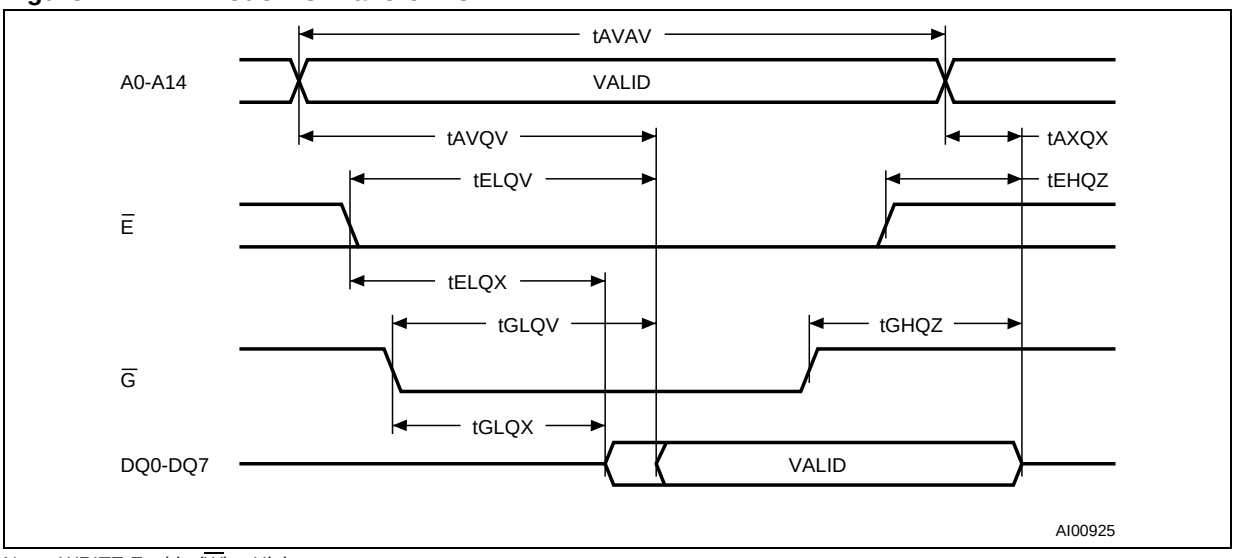
### READ Mode

The M48T35AY/V is in the READ Mode whenever W (WRITE Enable) is high and E (Chip Enable) is low. The unique address specified by the 15 address inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within Address Access time ($t_{AVQV}$) after the last address input signal is stable, providing that the E and G access times are also satisfied.

If the E and G access times are not met, valid data will be available after the latter of the Chip Enable Access time ($t_{ELQV}$) or Output Enable Access time ($t_{GLQV}$).

The state of the eight three-state Data I/O signals is controlled by E and G. If the outputs are activated before $t_{AVQV}$, the data lines will be driven to an indeterminate state until $t_{AVQV}$. If the Address Inputs are changed while E and G remain active, output data will remain valid for Output Data Hold time ($t_{AXQX}$) but will go indeterminate until the next Address Access.

**Figure 7. READ Mode AC Waveforms**




Note: WRITE Enable (W) = High.

**Table 3. READ Mode AC Characteristics**

| Symbol | Parameter[1] | M48T35AY | | M48T35AV | | Unit |
|---|---|---|---|---|---|---|
| | | –70 | | –100 | | |
| | | Min | Max | Min | Max | |
| $t_{AVAV}$ | READ Cycle Time | 70 | | 100 | | ns |
| $t_{AVQV}$ | Address Valid to Output Valid | | 70 | | 100 | ns |
| $t_{ELQV}$ | Chip Enable Low to Output Valid | | 70 | | 100 | ns |
| $t_{GLQV}$ | Output Enable Low to Output Valid | | 35 | | 50 | ns |
| $t_{ELQX}$[2] | Chip Enable Low to Output Transition | 5 | | 10 | | ns |
| $t_{GLQX}$[2] | Output Enable Low to Output Transition | 5 | | 5 | | ns |
| $t_{EHQZ}$[2] | Chip Enable High to Output Hi-Z | | 25 | | 50 | ns |
| $t_{GHQZ}$[2] | Output Enable High to Output Hi-Z | | 25 | | 40 | ns |
| $t_{AXQX}$ | Address Transition to Output Transition | 10 | | 10 | | ns |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C or –40 to 85°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. $C_L$ = 5pF.

### WRITE Mode

The M48T35AY/V is in the WRITE Mode whenever $\overline{W}$ and $\overline{E}$ are low. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of $t_{EHAX}$ from Chip Enable or $t_{WHAX}$ from WRITE Enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid $t_{DVWH}$ prior to the end of WRITE and remain valid for $t_{WHDX}$ afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; however, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs $t_{WLQZ}$ after $\overline{W}$ falls.

**Figure 8. WRITE Enable Controlled, WRITE Mode AC Waveform**

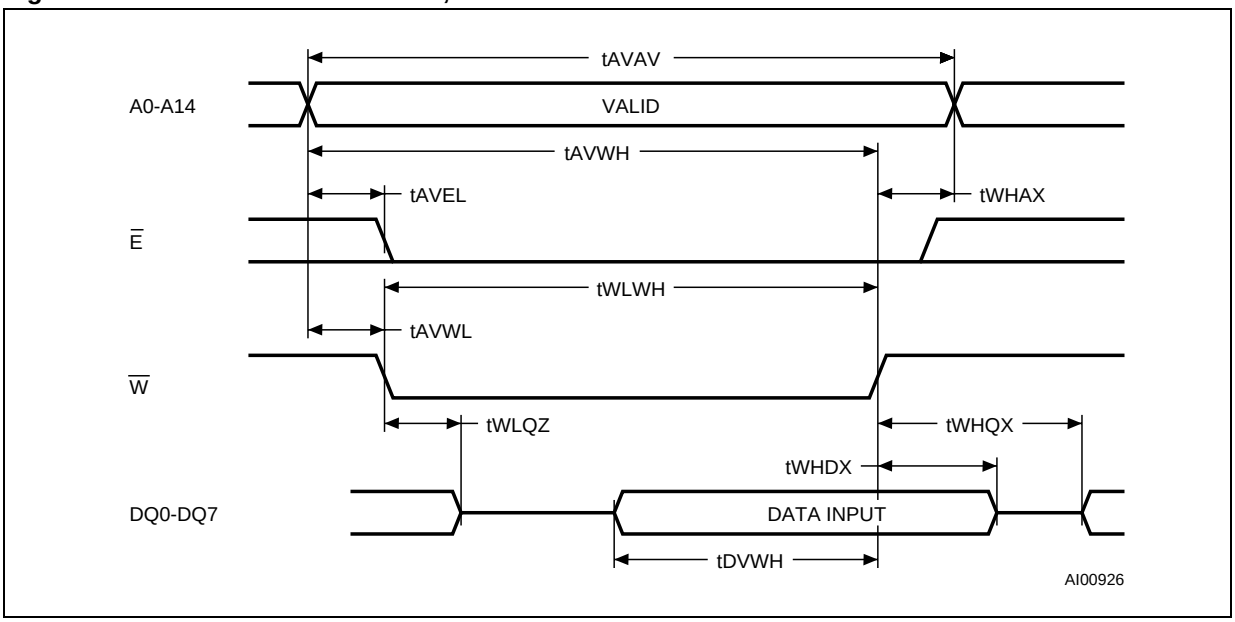



**Figure 9. Chip Enable Controlled, WRITE Mode AC Waveforms**

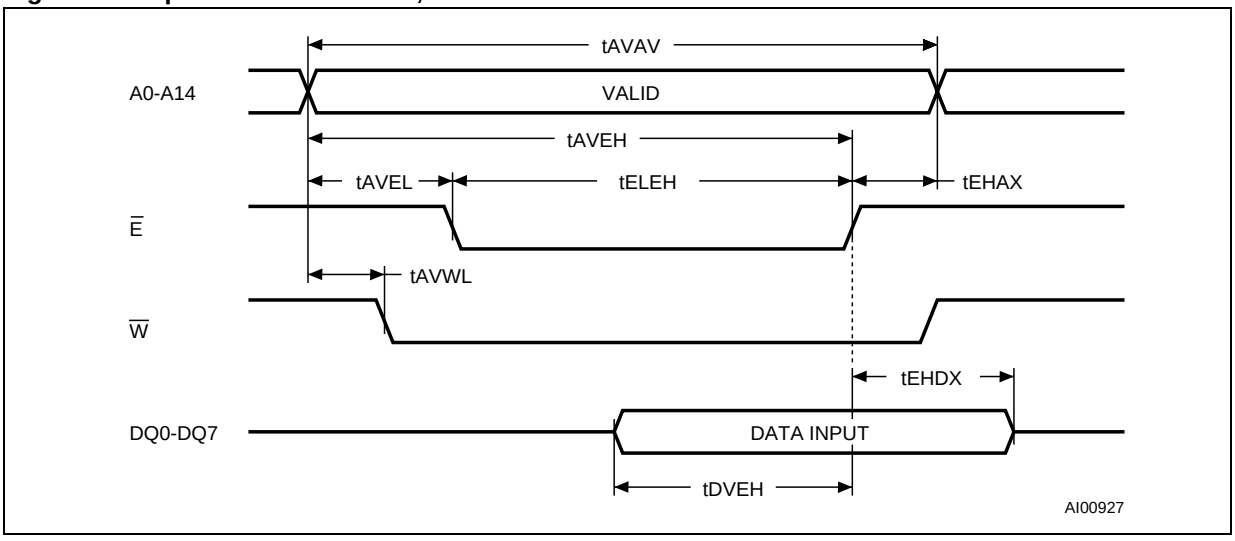


**Table 4. WRITE Mode AC Characteristics**

| Symbol | Parameter[1] | M48T35AY | | M48T35AV | | Unit |
|---|---|---|---|---|---|---|
| | | –70 | | –100 | | |
| | | Min | Max | Min | Max | |
| $t_{AVAV}$ | WRITE Cycle Time | 70 | | 100 | | ns |
| $t_{AVWL}$ | Address Valid to WRITE Enable Low | 0 | | 0 | | ns |
| $t_{AVEL}$ | Address Valid to Chip Enable Low | 0 | | 0 | | ns |
| $t_{WLWH}$ | WRITE Enable Pulse Width | 50 | | 80 | | ns |
| $t_{ELEH}$ | Chip Enable Low to Chip Enable High | 55 | | 80 | | ns |
| $t_{WHAX}$ | WRITE Enable High to Address Transition | 0 | | 10 | | ns |
| $t_{EHAX}$ | Chip Enable High to Address Transition | 0 | | 10 | | ns |
| $t_{DVWH}$ | Input Valid to WRITE Enable High | 30 | | 50 | | ns |
| $t_{DVEH}$ | Input Valid to Chip Enable High | 30 | | 50 | | ns |
| $t_{WHDX}$ | WRITE Enable High to Input Transition | 5 | | 5 | | ns |
| $t_{EHDX}$ | Chip Enable High to Input Transition | 5 | | 5 | | ns |
| $t_{WLQZ}$[2,3] | WRITE Enable Low to Output Hi-Z | | 25 | | 50 | ns |
| $t_{AVWH}$ | Address Valid to WRITE Enable High | 60 | | 80 | | ns |
| $t_{AVEH}$ | Address Valid to Chip Enable High | 60 | | 80 | | ns |
| $t_{WHQX}$[2,3] | WRITE Enable High to Output Transition | 5 | | 10 | | ns |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C or –40 to 85°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. $C_L$ = 5pF.
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

### Data Retention Mode

With valid $V_{CC}$ applied, the M48T35AY/V operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when $V_{CC}$ falls within the $V_{PFD}$ (max), VPFD (min) window (see Figure 15, Table 10, and Table 11., page 18). All outputs become high impedance, and all inputs are treated as “don't care.”

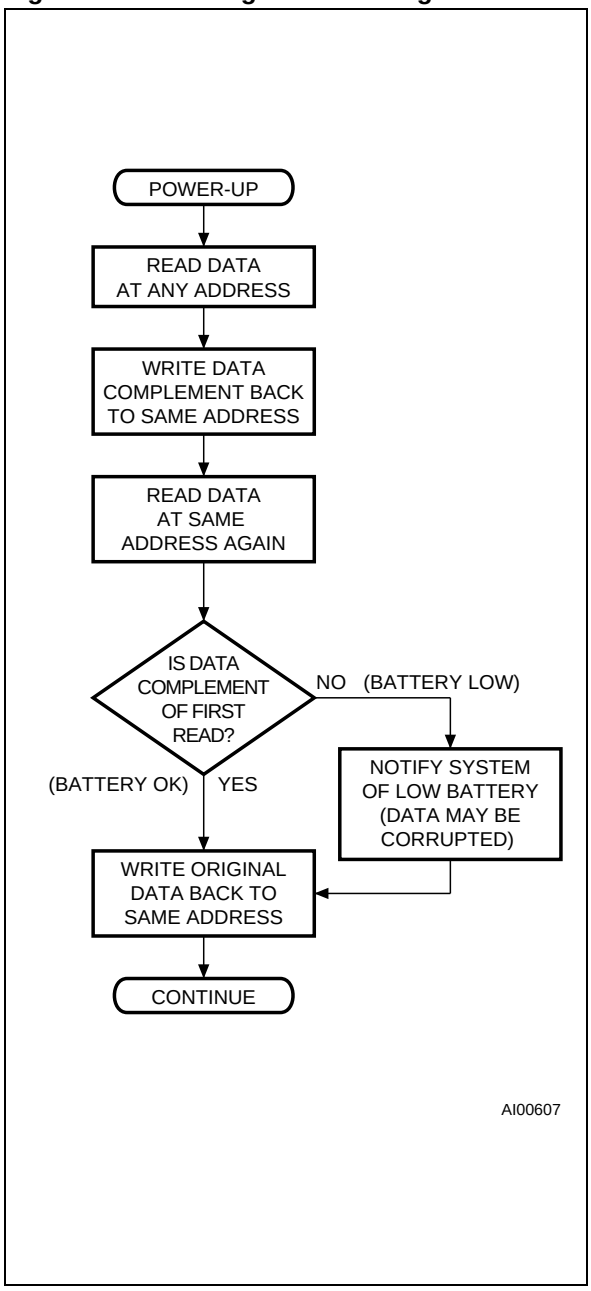
**Note:** A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below $V_{PFD}$ (min), the user can be assured the memory will be in a write protected state, provided the $V_{CC}$ fall time is not less than $t_F$. The M48T35AY/V may respond to transient noise spikes on $V_{CC}$ that reach into the deselect window during the time the device is sampling $V_{CC}$. Therefore, decoupling of the power supply lines is recommended.

When $V_{CC}$ drops below $V_{SO}$, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T35AY/V for an accumulated period of at least 7 years when $V_{CC}$ is less than $V_{SO}$. As system power returns and $V_{CC}$ rises above $V_{SO}$, the battery is disconnected and the power supply is switched to external $V_{CC}$. Write protection continues until $V_{CC}$ reaches $V_{PFD}$ (min) plus $t_{rec}$ (min). $\overline{E}$ should be kept high as $V_{CC}$ rises past $V_{PFD}$ (min) to prevent inadvertent WRITE cycles prior to processor stabilization. Normal RAM operation can resume $t_{rec}$ after $V_{CC}$ exceeds $V_{PFD}$ (max).

Also, as $V_{CC}$ rises, the battery voltage is checked. If the voltage is less than approximately 2.5V, an internal Battery Not OK (BOK) flag will be set. The BOK flag can be checked after power up. If the BOK flag is set, the first WRITE attempted will be blocked. The flag is automatically cleared after the first WRITE, and normal RAM operation resumes. Figure 10 illustrates how a BOK check routine could be structured.

For more information on Battery Storage Life refer to the Application Note AN1012.

**Figure 10. Checking the $\overline{\text{BOK}}$ Flag Status**



## CLOCK OPERATIONS

### Reading the Clock

Updates to the TIMEKEEPER® registers (see Table 5) should be halted before clock data is read to prevent reading data in transition. The BiPORT™ TIMEKEEPER cells in the RAM array are only data registers and not the actual clock counters, so updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ Bit, D6 in the Control Register 7FF8h. As long as a '1' remains in that position, updating is halted.

After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0.'

### Setting the Clock

Bit D7 of the Control Register 7FF8h is the WRITE Bit. Setting the WRITE Bit to a '1,' like the READ Bit, halts updates to the TIMEKEEPER® registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 5). Resetting the WRITE Bit to a '0' then transfers the values of all time registers 7FF9h-7FFFh to the actual TIMEKEEPER counters and allows normal operation to resume. The FT Bit and the bits marked as '0' in Table 5 must be written to '0' to allow for normal TIMEKEEPER and RAM operation. After the WRITE Bit is reset, the next clock update will occur within one second.

See the Application Note AN923, "TIMEKEEPER® Rolling Into the 21st Century" for information on Century Rollover.

### Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP Bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T35AY/V is shipped from STMicroelectronics with the STOP Bit set to a '1.' When reset to a '0,' the M48T35AY/V oscillator starts within 1 second.

**Table 5. Register Map**

| Address | Data | | | | | | | | Function/Range BCD Format | |
|---|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 7FFFh | 10 Years | | | | Year | | | | Year | 00-99 |
| 7FFEh | 0 | 0 | 0 | 10 M. | Month | | | | Month | 01-12 |
| 7FFDh | 0 | 0 | 10 Date | | Date | | | | Date | 01-31 |
| 7FFCh | 0 | FT | CEB | CB | 0 | Day | | | Century/Day | 00-01/01-07 |
| 7FFBh | 0 | 0 | 10 Hours | | Hours | | | | Hours | 00-23 |
| 7FFAh | 0 | 10 Minutes | | | Minutes | | | | Minutes | 00-59 |
| 7FF9h | ST | 10 Seconds | | | Seconds | | | | Seconds | 00-59 |
| 7FF8h | W | R | S | Calibration | | | | | Control | |

Keys: S = SIGN Bit
FT = FREQUENCY TEST Bit (Must be set to '0' upon power for normal operation)
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to '0'
CEB = Century Enable Bit
CB = Century Bit

Note: When CEB is set to '1,' CB will toggle from '0' to '1' or from '1' to '0' at the turn of the century (dependent upon the initial value set). When CEB is set to '0,' CB will not toggle. The WRITE Bit does not need to be set to write to CEB.

### Calibrating the Clock

The M48T35AY/V is driven by a quartz-controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed 35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about ±1.53 minutes per month. With the calibration bits properly set, the accuracy of each M48T35AY/V improves to better than +1/–2 ppm at 25°C.

The oscillation rate of any crystal changes with temperature (see Figure 11., page 13). Most clock chips compensate for crystal frequency and temperature shift error with cumbersome “trim” capacitors. The M48T35AY/V design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in Figure 12., page 13. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration Byte occupies the five lower order bits (D4-D0) in the Control Register 7FF8h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is the Sign Bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration Byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48T35AY/V may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) Bit, the seventh-most significant bit in the Day Register is set to a '1,' and D7 of the Seconds Register is a '0' (Oscillator Running), DQ0 will toggle at 512 Hz during a READ of the Seconds Register. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (WR001010) to be loaded into the Calibration Byte for correction.

**Note:** Setting or changing the Calibration Byte does not affect the Frequency Test output frequency.

The FT Bit MUST be reset to '0' for normal clock operations to resume. The FT Bit is automatically Reset on power-down.

For more information on calibration, see Application Note AN934, “TIMEKEEPER® Calibration.”

### Century Bit

Bit D5 and D4 of Clock Register 7FFCh contain the CENTURY ENABLE Bit (CEB) and the CENTURY Bit (CB). Setting CEB to a '1' will cause CB to toggle, either from a '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle.

**Note:** The WRITE Bit must be set in order to write to the CENTURY Bit.

**Figure 11. Crystal Accuracy Across Temperature**

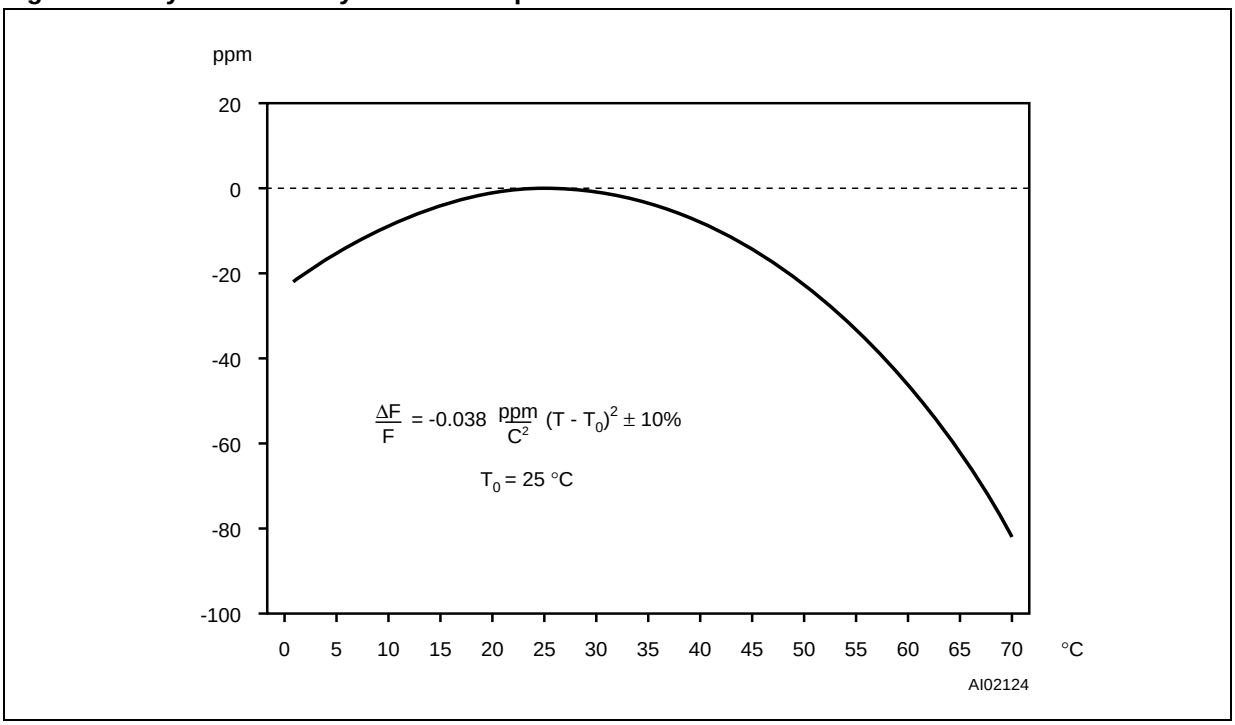
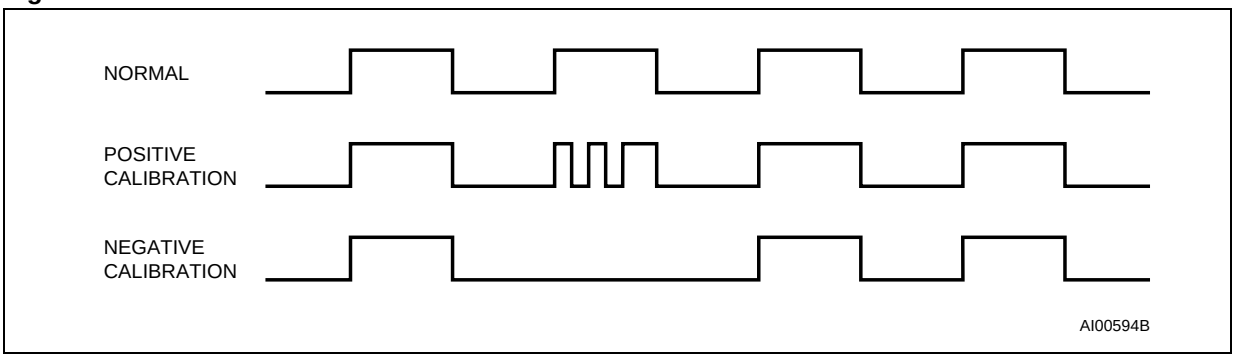



**Figure 12. Clock Calibration**

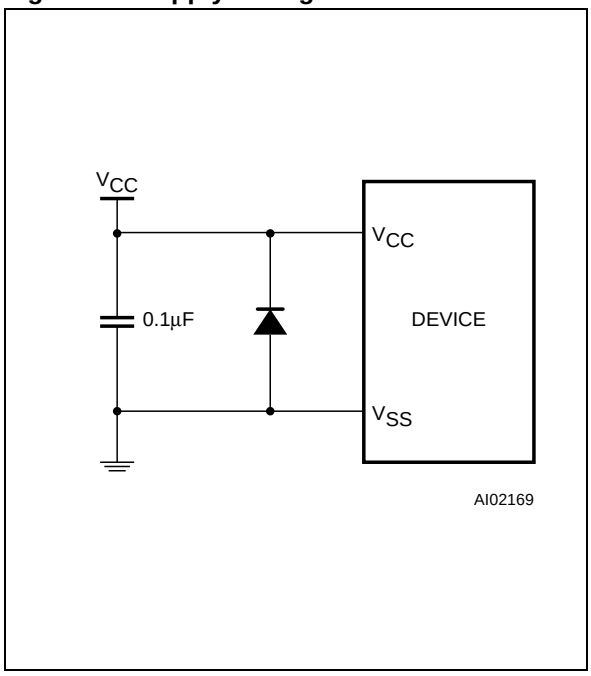


### $V_{CC}$ Noise And Negative Going Transients

$I_{CC}$ transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the $V_{CC}$ bus. These transients can be reduced if capacitors are used to store energy which stabilizes the $V_{CC}$ bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A bypass capacitor value of 0.1µF (as shown in Figure 13) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on $V_{CC}$ that drive it to values below $V_{SS}$ by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a schottky diode from $V_{CC}$ to $V_{SS}$ (cathode connected to $V_{CC}$, anode to $V_{SS}$). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

**Figure 13. Supply Voltage Protection**



## MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 6. Absolute Maximum Ratings**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | Grade 1 | 0 to 70 | °C |
| | | Grade 6 | –40 to 85 | °C |
| $T_{STG}$ | Storage Temperature ($V_{CC}$ Off, Oscillator Off) | | –40 to 85 | °C |
| $T_{SLD}$(1,2,3) | Lead Solder Temperature for 10 seconds | | 260 | °C |
| $V_{IO}$ | Input or Output Voltages | M48T35AY | –0.3 to 7 | V |
| | | M48T35AV | –0.3 to 4.6 | V |
| $V_{CC}$ | Supply Voltage | M48T35AY | –0.3 to 7 | V |
| | | M48T35AV | –0.3 to 4.6 | V |
| $I_O$ | Output Current | | 20 | mA |
| $P_D$ | Power Dissipation | | 1 | W |

Note: 1. For DIP package: Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).
2. For SO package, standard (SnPb) lead finish: Reflow at peak temperature of 225°C (total thermal budget not to exceed 180°C for between 90 to 150 seconds).
3. For SO package, Lead-free (Pb-free) lead finish: Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

***CAUTION:*** *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*
***CAUTION:*** *Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.*

## DC AND AC PARAMETERS

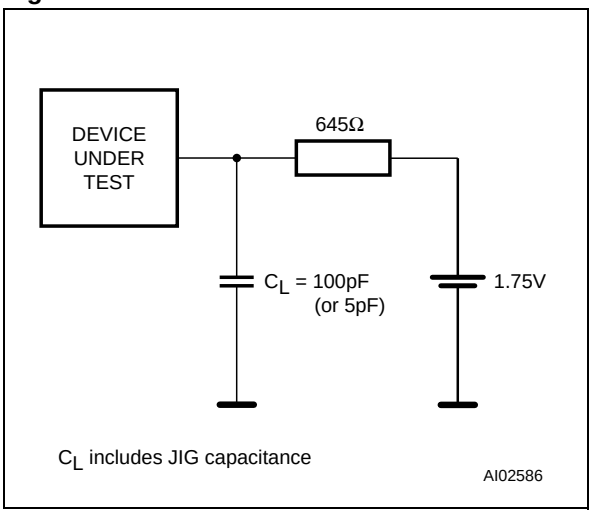
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

**Table 7. Operating and AC Measurement Conditions**

| Parameter | | M48T35AY | M48T35AV | Unit |
|---|---|---|---|---|
| Supply Voltage ($V_{CC}$) | | 4.5 to 5.5 | 3.0 to 3.6 | V |
| Ambient Operating Temperature ($T_A$) | Grade 1 | 0 to 70 | 0 to 70 | °C |
| | Grade 6 | –40 to 85 | –40 to 85 | |
| Load Capacitance ($C_L$) | | 100 | 50 | pF |
| Input Rise and Fall Times | | ≤ 5 | ≤ 5 | ns |
| Input Pulse Voltages | | 0 to 3 | 0 to 3 | V |
| Input and Output Timing Ref. Voltages | | 1.5 | 1.5 | V |

Note: Output Hi-Z is defined as the point where data is no longer driven.

**Figure 14. AC Measurement Load Circuit**




Note: 50pF for M48T35AV.

**Table 8. Capacitance**

| Symbol | Parameter[1,2] | Min | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 10 | pF |
| $C_{OUT}$[3] | Output Capacitance | | 10 | pF |

Note: 1. Effective capacitance measured with power supply at 5V; sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs deselected.

**Table 9. DC Characteristics**

| Symbol | Parameter | Test Condition(1) | M48T35AY | | M48T35AV | | Unit |
|---|---|---|---|---|---|---|---|
| | | | –70 | | –100 | | |
| | | | Min | Max | Min | Max | |
| $I_{LI}$ | Input Leakage Current | $0V \le V_{IN} \le V_{CC}$ | | ±1 | | ±1 | µA |
| $I_{LO}$(2) | Output Leakage Current | $0V \le V_{OUT} \le V_{CC}$ | | ±1 | | ±1 | µA |
| $I_{CC}$ | Supply Current | Outputs open | | 50 | | 30 | mA |
| $I_{CC1}$ | Supply Current (Standby) TTL | $\overline{E} = V_{IH}$ | | 3 | | 2 | mA |
| $I_{CC2}$ | Supply Current (Standby) CMOS | $\overline{E} = V_{CC} - 0.2V$ | | 3 | | 2 | mA |
| $V_{IL}$(3) | Input Low Voltage | | –0.3 | 0.8 | –0.3 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.2 | $V_{CC}$ + 0.3 | 2.2 | $V_{CC}$ + 0.3 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | 0.4 | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –1mA | 2.4 | | 2.4 | | V |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C or –40 to 85°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. Outputs deselected.
3. Negative spikes of –1V allowed for up to 10ns once per Cycle.

**Figure 15. Power Down/Up Mode AC Waveforms**

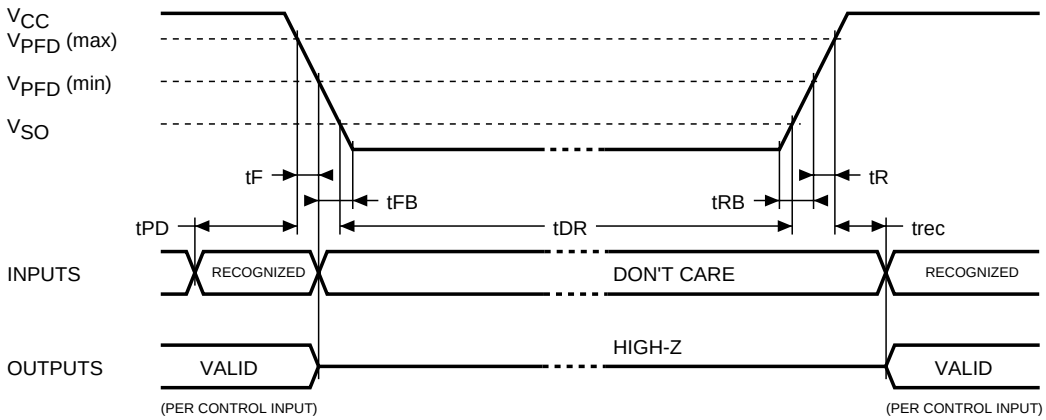



**Table 10. Power Down/Up AC Characteristics**

| Symbol | Parameter[1] | | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{PD}$ | $\overline{E}$ or $\overline{W}$ at $V_{IH}$ before Power Down | | 0 | | µs |
| $t_F$[2] | $V_{PFD}$ (max) to $V_{PFD}$ (min) $V_{CC}$ Fall Time | | 300 | | µs |
| $t_{FB}$[3] | $V_{PFD}$ (min) to $V_{SS}$ $V_{CC}$ Fall Time | M48T35AY | 10 | | µs |
| | | M48T35AV | 150 | | µs |
| $t_R$ | $V_{PFD}$ (min) to $V_{PFD}$ (max) $V_{CC}$ Rise Time | | 10 | | µs |
| $t_{RB}$ | $V_{SS}$ to $V_{PFD}$ (min) $V_{CC}$ Rise Time | | 1 | | µs |
| $t_{rec}$[4] | $V_{PFD}$ (max) to Inputs Recognized | | 40 | 200 | ms |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C or –40 to 85°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. $V_{PFD}$ (max) to $V_{PFD}$ (min) fall time of less than $t_F$ may result in deselection/write protection not occurring until 200µs after $V_{CC}$ passes $V_{PFD}$ (min).
3. $V_{PFD}$ (min) to $V_{SS}$ fall time of less than $t_{FB}$ may cause corruption of RAM data.
4. $t_{rec}$ (min) = 20ms for industrial temperature Grade 6 device.

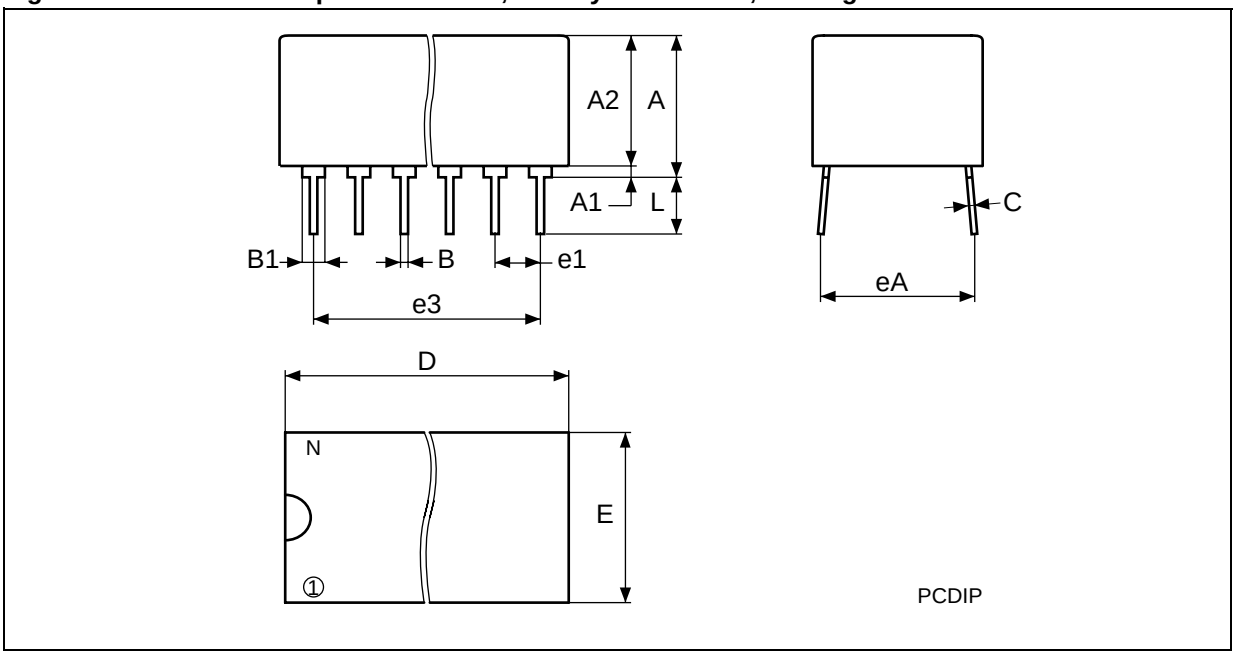
**Table 11. Power Down/Up Trip Points DC Characteristics**

| Symbol | Parameter[1,2] | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PFD}$ | Power-fail Deselect Voltage | M48T35AY | 4.2 | 4.35 | 4.5 | V |
| | | M48T35AV | 2.7 | 2.9 | 3.0 | V |
| $V_{SO}$ | Battery Back-up Switchover Voltage | M48T35AY | | 3.0 | | V |
| | | M48T35AV | | $V_{PFD}$ –100mV | | V |
| $t_{DR}$[5] | Expected Data Retention Time | Grade 1 | 10[3] | | | YEARS |
| | | Grade 6 | 10[4] | | | YEARS |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C or –40 to 85°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. All voltages referenced to $V_{SS}$.
3. CAPHAT and M4T32-BR12SH1 SNAPHAT only, M4T28-BR12SH1 SNAPHAT top $t_{DR}$ = 7 years (typ).
4. Using larger M4T32-BR12SH6 SNAPHAT top (recommended for Industrial Temperature Range - Grade 6 device).
5. At 25°C, $V_{CC}$ = 0V.

## PACKAGE MECHANICAL INFORMATION

**Figure 16. PCDIP28 – 28-pin Plastic DIP, battery CAPHAT™, Package Outline**

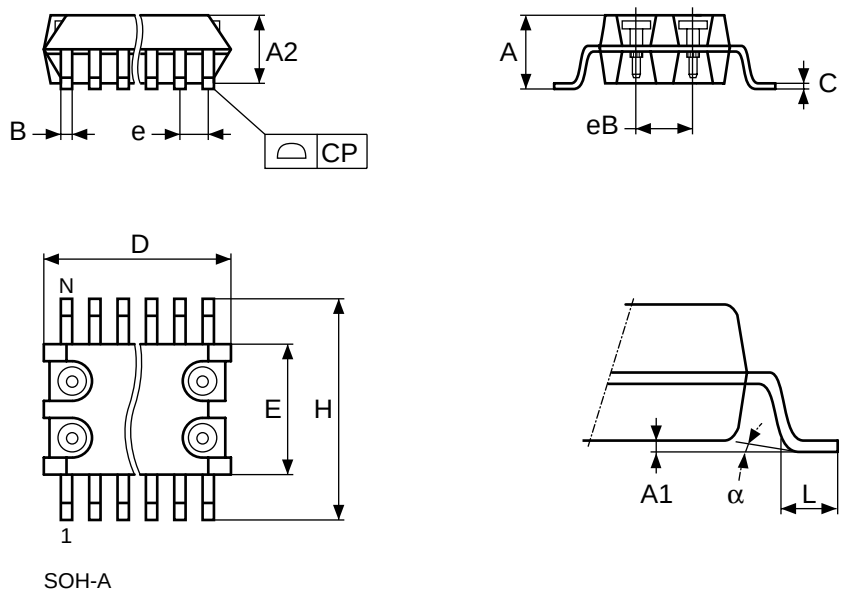



Note: Drawing is not to scale.

**Table 12. PCDIP28 – 28-pin Plastic DIP, battery CAPHAT™, Package Mechanical Data**

| Symb | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 8.89 | 9.65 | | 0.350 | 0.380 |
| A1 | | 0.38 | 0.76 | | 0.015 | 0.030 |
| A2 | | 8.38 | 8.89 | | 0.330 | 0.350 |
| B | | 0.38 | 0.53 | | 0.015 | 0.021 |
| B1 | | 1.14 | 1.78 | | 0.045 | 0.070 |
| C | | 0.20 | 0.31 | | 0.008 | 0.012 |
| D | | 39.37 | 39.88 | | 1.550 | 1.570 |
| E | | 17.83 | 18.34 | | 0.702 | 0.722 |
| e1 | | 2.29 | 2.79 | | 0.090 | 0.110 |
| e3 | | 29.72 | 36.32 | | 1.170 | 1.430 |
| eA | | 15.24 | 16.00 | | 0.600 | 0.630 |
| L | | 3.05 | 3.81 | | 0.120 | 0.150 |
| N | 28 | | | 28 | | |

**Figure 17. SOH28 – 28-lead Plastic Small Outline, 4-socket battery SNAPHAT, Package Outline**

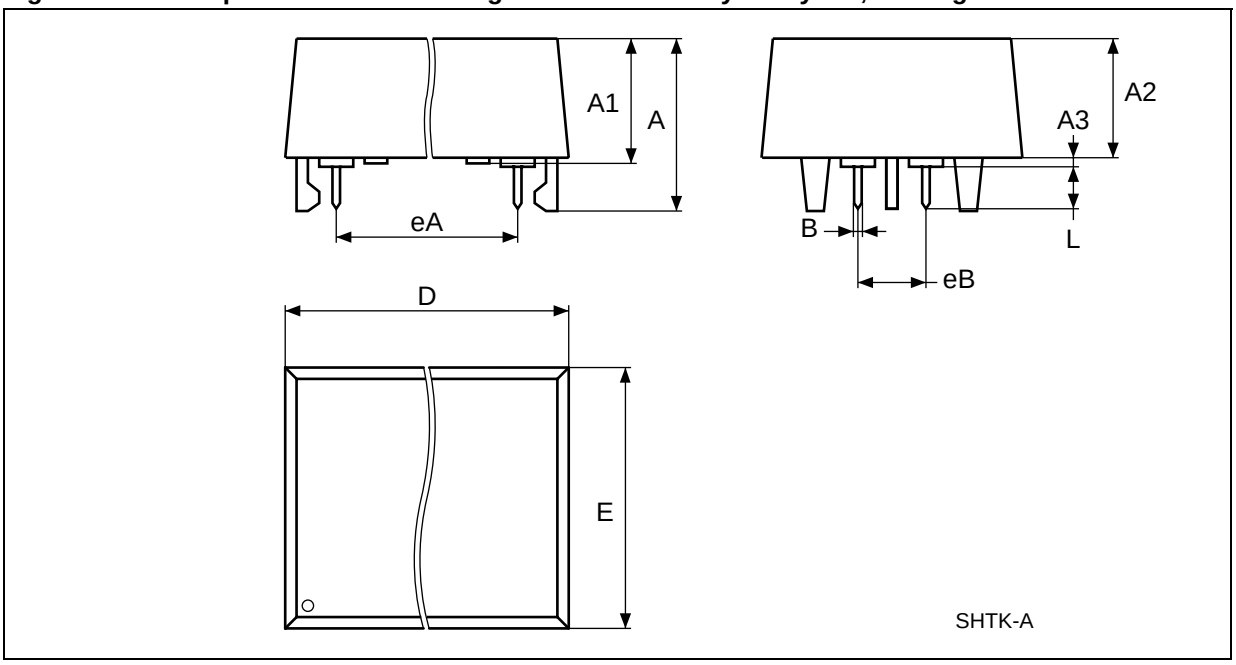



Note: Drawing is not to scale.

**Table 13. SOH28 – 28-lead Plastic Small Outline, 4-socket battery SNAPHAT, Pack. Mech. Data**

| Symb | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 3.05 | | | 0.120 |
| A1 | | 0.05 | 0.36 | | 0.002 | 0.014 |
| A2 | | 2.34 | 2.69 | | 0.092 | 0.106 |
| B | | 0.36 | 0.51 | | 0.014 | 0.020 |
| C | | 0.15 | 0.32 | | 0.006 | 0.012 |
| D | | 17.71 | 18.49 | | 0.697 | 0.728 |
| E | | 8.23 | 8.89 | | 0.324 | 0.350 |
| e | 1.27 | – | – | 0.050 | – | – |
| eB | | 3.20 | 3.61 | | 0.126 | 0.142 |
| H | | 11.51 | 12.70 | | 0.453 | 0.500 |
| L | | 0.41 | 1.27 | | 0.016 | 0.050 |
| α | | 0° | 8° | | 0° | 8° |
| N | | 28 | | | 28 | |
| CP | | | 0.10 | | | 0.004 |

**Figure 18. SH – 4-pin SNAPHAT Housing for 48mAh Battery & Crystal, Package Outline**

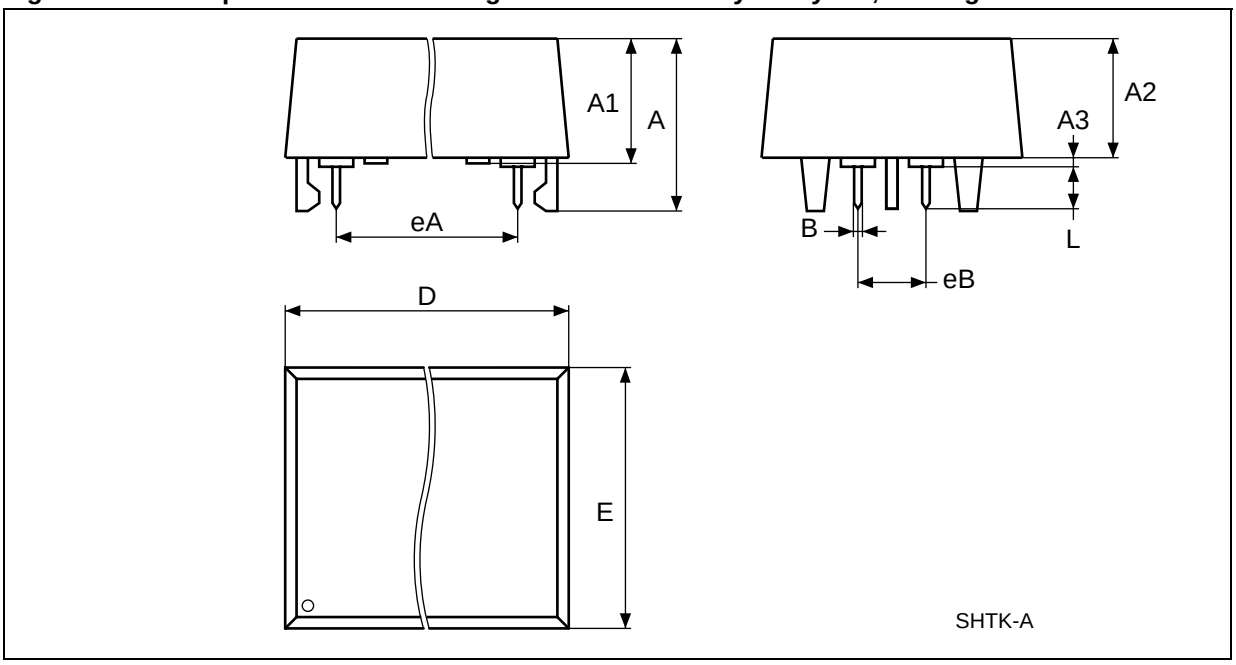



Note: Drawing is not to scale.

**Table 14. SH – 4-pin SNAPHAT Housing for 48mAh Battery & Crystal, Package Mech. Data**

| Symb | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 9.78 | | | 0.385 |
| A1 | | 6.73 | 7.24 | | 0.265 | 0.285 |
| A2 | | 6.48 | 6.99 | | 0.255 | 0.275 |
| A3 | | | 0.38 | | | 0.015 |
| B | | 0.46 | 0.56 | | 0.018 | 0.022 |
| D | | 21.21 | 21.84 | | 0.835 | 0.860 |
| E | | 14.22 | 14.99 | | 0.560 | 0.590 |
| eA | | 15.55 | 15.95 | | 0.612 | 0.628 |
| eB | | 3.20 | 3.61 | | 0.126 | 0.142 |
| L | | 2.03 | 2.29 | | 0.080 | 0.090 |

**Figure 19. SH – 4-pin SNAPHAT Housing for 120mAh Battery & Crystal, Package Outline**




Note: Drawing is not to scale.

**Table 15. SH – 4-pin SNAPHAT Housing for 120mAh Battery & Crystal, Package Mech. Data**

| Symb | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 10.54 | | | 0.415 |
| A1 | | 8.00 | 8.51 | | 0.315 | 0.335 |
| A2 | | 7.24 | 8.00 | | 0.285 | 0.315 |
| A3 | | | 0.38 | | | 0.015 |
| B | | 0.46 | 0.56 | | 0.018 | 0.022 |
| D | | 21.21 | 21.84 | | 0.835 | 0.860 |
| E | | 17.27 | 18.03 | | 0.680 | 0.710 |
| eA | | 15.55 | 15.95 | | 0.612 | 0.628 |
| eB | | 3.20 | 3.61 | | 0.126 | 0.142 |
| L | | 2.03 | 2.29 | | 0.080 | 0.090 |

# PART NUMBERING

### Table 16. Ordering Information Scheme

Example: M48T 35AY –70 MH 1 E

**Device Type**

M48T

**Supply Voltage and Write Protect Voltage**

35AY = $V_{CC}$ = 4.5 to 5.5V; $V_{PFD}$ = 4.2 to 4.5V

35AV = $V_{CC}$ = 3.0 to 3.6V; $V_{PFD}$ = 2.7 to 3.0V

**Speed**

–70 = 70ns (35AY)

–10 = 100ns (35AV)

**Package**

PC = PCDIP28

MH(1) = SOH28

**Temperature Range**

1 = 0 to 70°C

6 = –40 to 85°C(2)

**Shipping Method**

**For SOH28:**

blank = Tubes (Not for New Design - Use E)

E = Lead-free Package (ECOPACK®), Tubes

F = Lead-free Package (ECOPACK®), Tape & Reel

TR = Tape & Reel (Not for New Design - Use F)

**For PCDIP28:**

blank = Tubes

Note: 1. The SOIC package (SOH28) requires the SNAPHAT® battery package which is ordered separately under the part number "M4TXX-BR12SH" in plastic tube or "M4TXX-BR12SHTR" in Tape & Reel form (see Table 17).

2. Available in SOIC package only.

**Caution**: Do not place the SNAPHAT battery package "M4TXX-BR12SH" in conductive foam as it will drain the lithium button-cell battery.

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

### Table 17. SNAPHAT Battery Table

| Part Number | Description | Package |
|---|---|---|
| M4T28-BR12SH | Lithium Battery (48mAh) SNAPHAT | SH |
| M4T32-BR12SH | Lithium Battery (120mAh) SNAPHAT | SH |

# REVISION HISTORY

**Table 18. Document Revision History**

| Date | Rev. # | Revision Details |
|---|---|---|
| November 1999 | 1.0 | First Issue |
| 21-Apr-00 | 2.0 | From Preliminary Data to Data Sheet |
| 29-May-00 | 2.1 | $t_{FB}$ change (Table 10) |
| 20-Jul-01 | 3.0 | Reformatted; temp./voltage info. added to tables (Table 8, 9, 3, 4, 10, 11); add Century Bit text |
| 20-May-02 | 3.1 | Modify reflow time and temperature footnotes (Table 6) |
| 31-Mar-03 | 4.0 | v2.2 template applied; data retention condition updated (Table 11) |
| 01-Apr-04 | 5.0 | Reformatted; updated with Lead-free package information (Table 6, 16) |

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