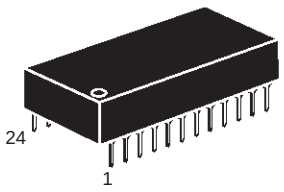
M48T02
M48T12

16 Kbit (2Kb x8) TIMEKEEPER® SRAM

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK and POWER-FAIL CONTROL CIRCUIT
- BYTEWIDE™ RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES and SECONDS
- TYPICAL CLOCK ACCURACY of ± 1 MINUTE a MONTH, AT 25°C
- SOFTWARE CONTROLLED CLOCK CALIBRATION for HIGH ACCURACY APPLICATIONS
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGES (V_{PFD} = Power-fail Deselect Voltage):
  - M48T02: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48T12: 4.2V ≤ V_{PFD} ≤ 4.5V
- SELF-CONTAINED BATTERY and CRYSTAL in the CAPHAT DIP PACKAGE
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 2Kb x8 SRAMs



PCDIP24 (PC)
Battery/Crystal CAPHAT

DESCRIPTION

The M48T02/12 TIMEKEEPER® RAM is a 2Kb x8 non-volatile static RAM and real time clock which is pin and functional compatible with the DS1642.

A special 24 pin 600mil DIP CAPHAT™ package houses the M48T02/12 silicon with a quartz crystal and a long life lithium button cell to form a highly integrated battery backed-up memory and real time clock solution.

Table 1. Signal Names

A0-A10	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

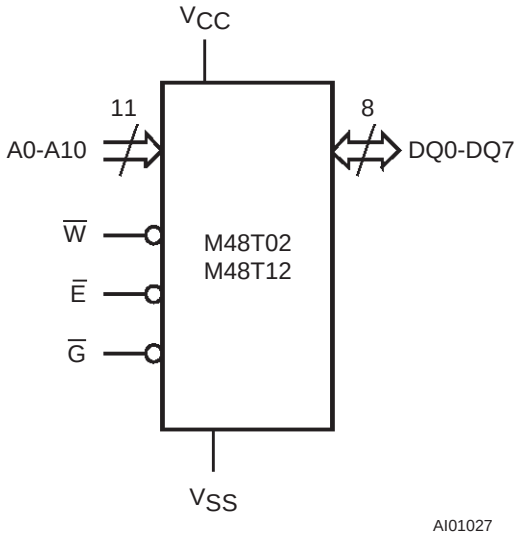


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
T_{SLD} (2)	Lead Solder Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Notes: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.

2. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

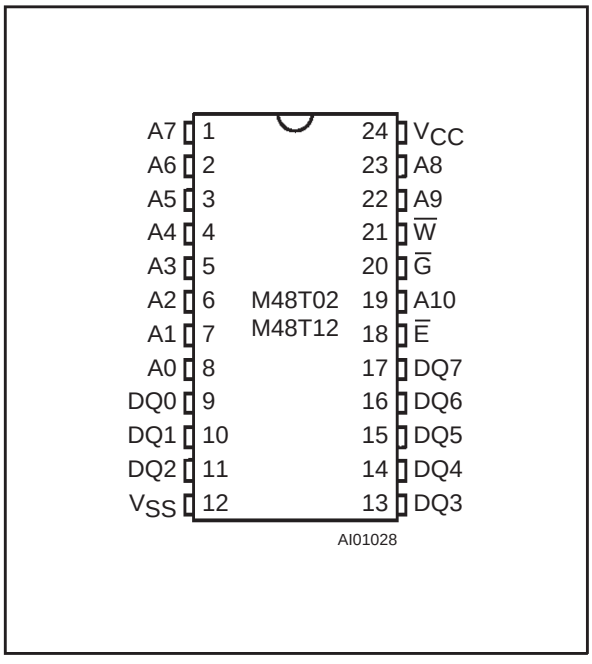
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	High Z	Battery Back-up Mode

Notes: X = V_{IH} or V_{IL}; V_{SO} = Battery Back-up Switchover Voltage.

Figure 2. DIP Pin Connections



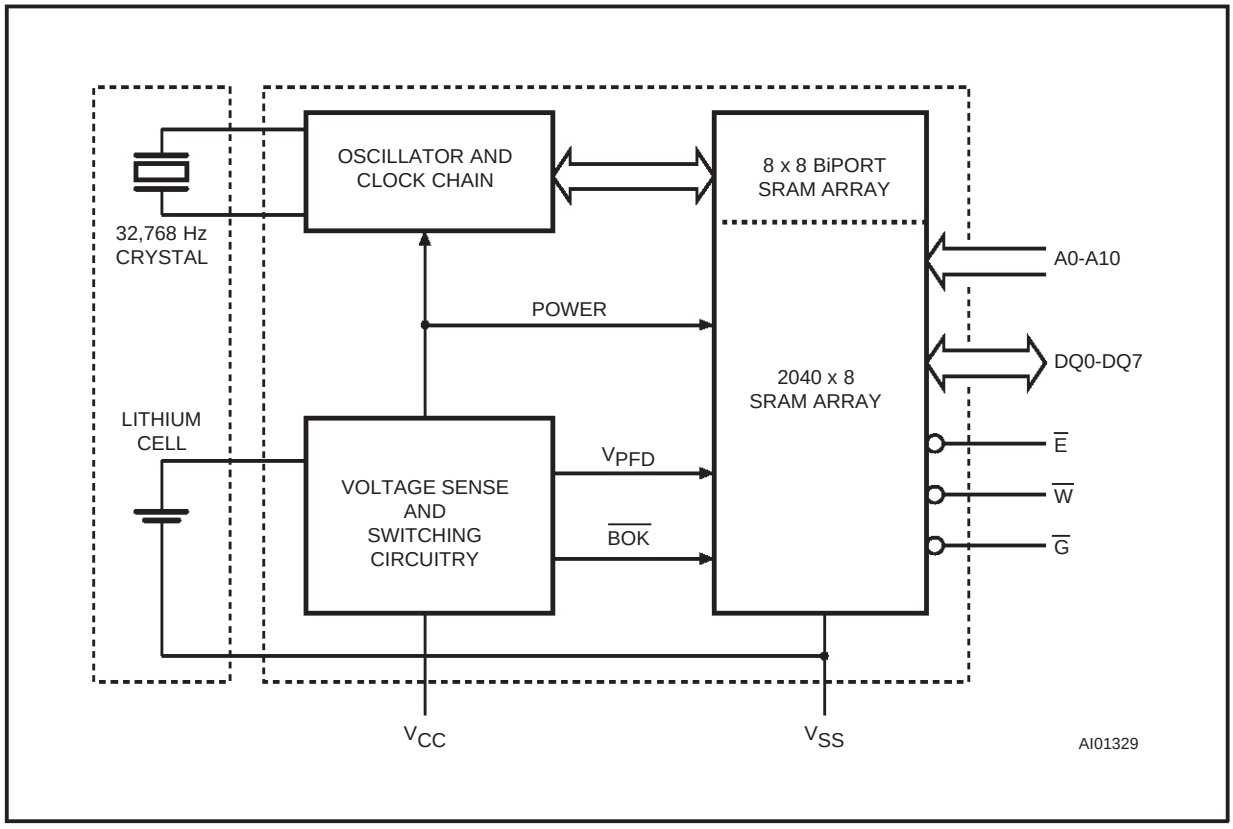
DESCRIPTION (cont'd)

The M48T02/12 button cell has sufficient capacity and storage life to maintain data and clock functionality for an accumulated time period of at least 10 years in the absence of power over the operating temperature range.

The M48T02/12 is a non-volatile pin and function equivalent to any JEDEC standard 2Kb x8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

As Figure 3 shows, the static memory array and the quartz controlled clock oscillator of the M48T02/12 are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE clock information in the bytes with addresses 7F8h-7FFh. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically.

Figure 3. Block Diagram



Byte 7F8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells. The M48T02/12 includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T02/12 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

Table 4. AC Measurement Conditions

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0V to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

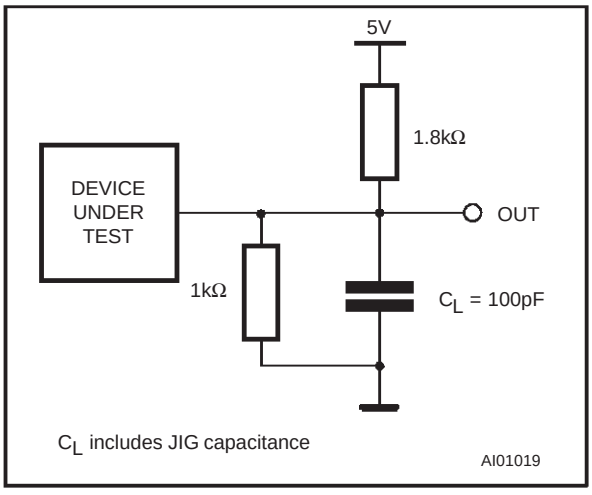


Table 5. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} (2)	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Outputs deselected.

Table 6. DC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} (1)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		80	mA
I_{CC1} (2)	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		3	mA
I_{CC2} (2)	Supply Current (Standby) CMOS	$\overline{E}$ = V_{CC} – 0.2V		3	mA
V_{IL} (3)	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Notes: 1. Outputs Deselected.
2. Measured with Control Bits set as follows: R = '1'; W, ST, KS, FT = '0'.

Table 7. Power Down/Up Trip Points DC Characteristics (1)
(T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48T02)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48T12)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} (2)	Expected Data Retention Time	10			YEARS

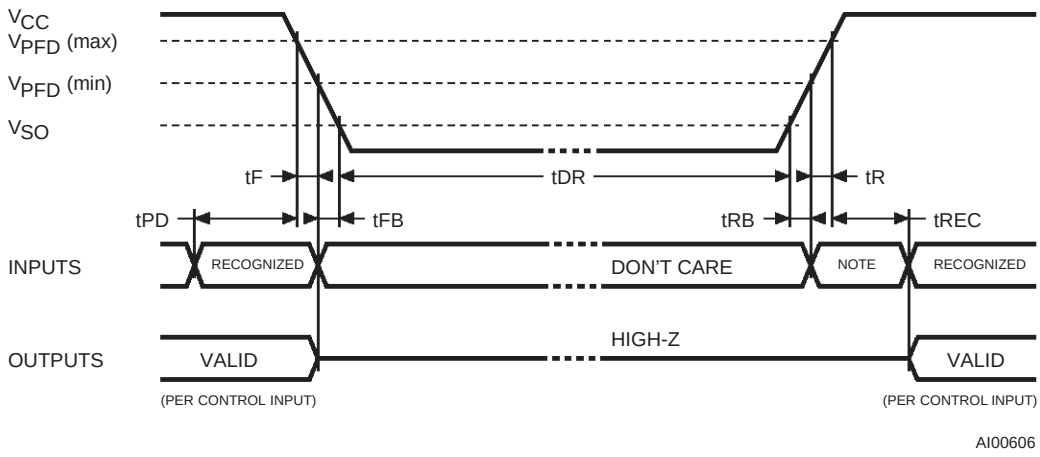
Notes: 1. All voltages referenced to V_{SS}.
2. At 25°C.

Table 8. Power Down/Up Mode AC Characteristics
(T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up		2	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 50 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

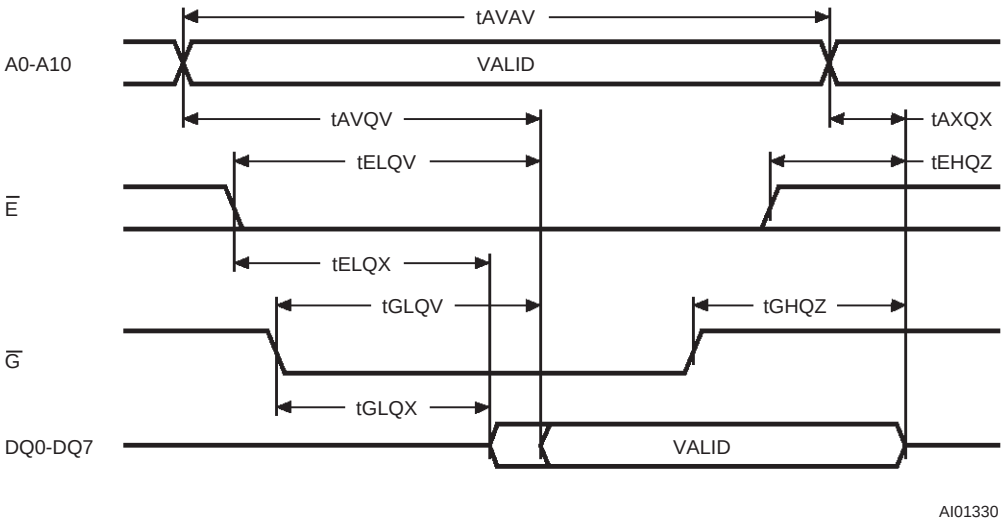


Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PFD}(min). Some systems may perform inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begin. Even though a power on reset is being applied to the processor, a reset condition may not occur until after the system clock is running.

Table 9. Read Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48T02 / M48T12						Unit
		-70		-150		-200		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	70		150		200		ns
t_{AVQV}	Address Valid to Output Valid		70		150		200	ns
t_{ELQV}	Chip Enable Low to Output Valid		70		150		200	ns
t_{GLQV}	Output Enable Low to Output Valid		35		75		80	ns
t_{ELQX}	Chip Enable Low to Output Transition	5		10		10		ns
t_{GLQX}	Output Enable Low to Output Transition	5		5		5		ns
t_{EHQZ}	Chip Enable High to Output Hi-Z		25		35		40	ns
t_{GHQZ}	Output Enable High to Output Hi-Z		25		35		40	ns
t_{AXQX}	Address Transition to Output Transition	10		5		5		ns

Figure 6. Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High.

Table 10. Write Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48T02 / M48T12						Unit
		-70		-150		-200		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	70		150		200		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{WLWH}	Write Enable Pulse Width	50		90		120		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	55		90		120		ns
t_{WHAX}	Write Enable High to Address Transition	0		10		10		ns
t_{EHAX}	Chip Enable High to Address Transition	0		10		10		ns
t_{DVWH}	Input Valid to Write Enable High	30		40		60		ns
t_{DVEH}	Input Valid to Chip Enable High	30		40		60		ns
t_{WHDX}	Write Enable High to Input Transition	5		5		5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		5		5		ns
t_{WLQZ}	Write Enable Low to Output Hi-Z		25		50		60	ns
t_{AVWH}	Address Valid to Write Enable High	60		120		140		ns
t_{AVEH}	Address Valid to Chip Enable High	60		120		140		ns
t_{WHQX}	Write Enable High to Output Transition	5		10		10		ns

READ MODE

The M48T02/12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs defines which one of the 2,048 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within Address Access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access time (t_{ELQV}) or Output Enable Access time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for Output Data Hold time (t_{AXQX}) but will go indeterminate until the next Address Access.

WRITE MODE

The M48T02/12 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 7. Write Enable Controlled, Write AC Waveforms

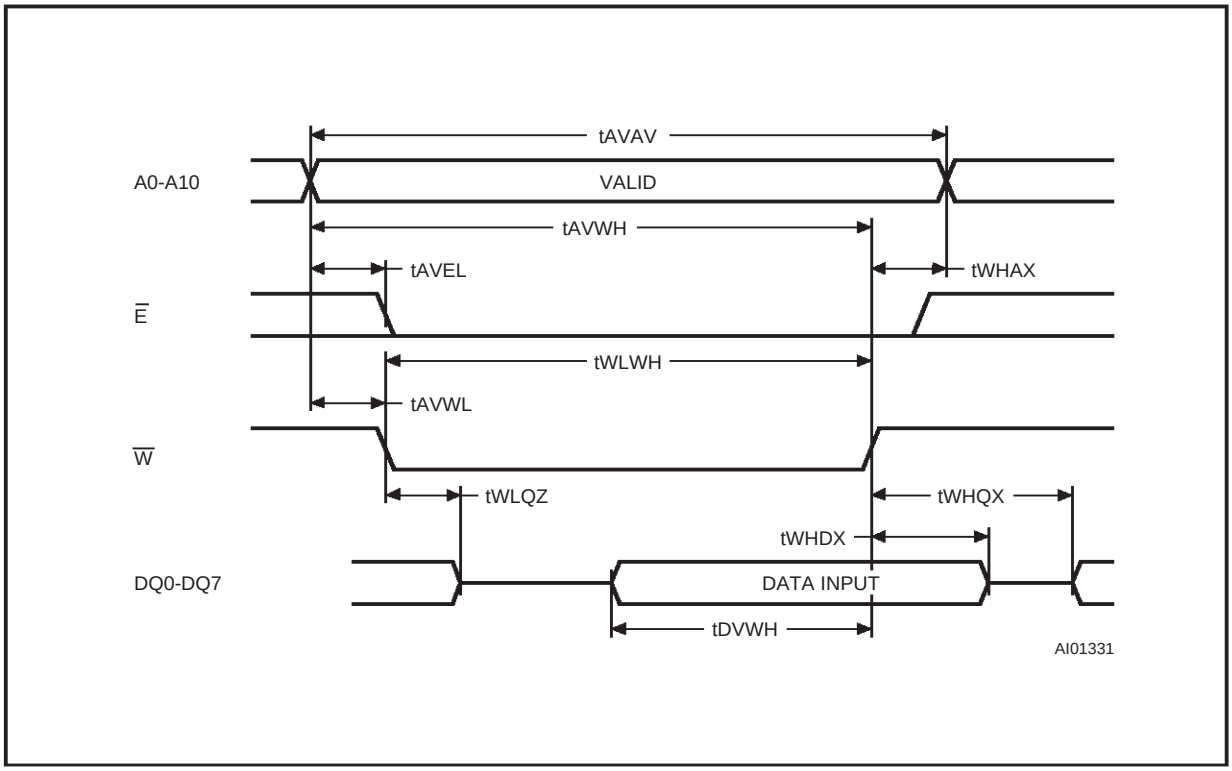
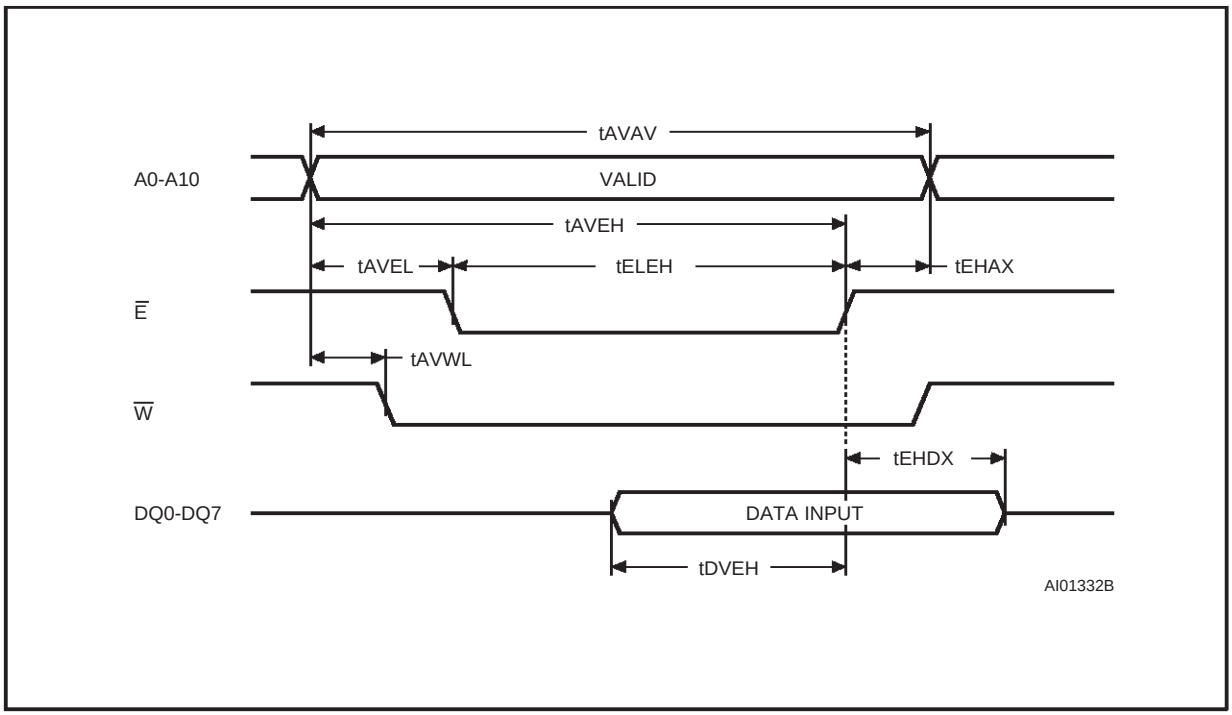


Figure 8. Chip Enable Controlled, Write AC Waveforms



DATA RETENTION MODE

With valid V_{CC} applied, the M48T02/12 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T02/12 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises, the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 9 illustrates how a $\overline{BOK}$ check routine could be structured.

For more information on a Battery Storage Life refer to the Application Note AN1012.

CLOCK OPERATIONS

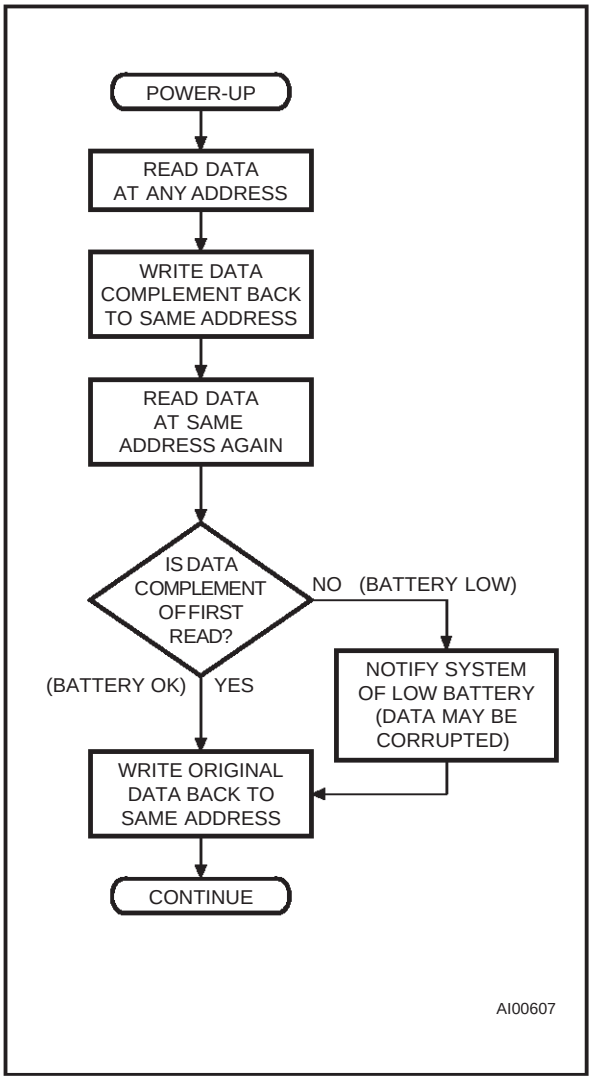
Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, the seventh bit in the control register. As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the read bit is reset to a '0'.

Figure 9. Checking the $\overline{BOK}$ Flag Status



Setting the Clock

The eighth bit of the control register is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 10). Resetting the WRITE bit to a '0' then transfers the values of all time registers (7F9h-7FFh) to the actual TIMEKEEPER counters and allows normal operation to resume. The FT bit and the bits marked as '0' in Table 10 must be written to '0' to allow for normal TIMEKEEPER and RAM operation.

See the Application Note AN923 "TIMEKEEPER rolling into the 21st century" for more information on Century Rollover.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T02/12 is shipped from STMicroelectronics with the STOP bit set to a '1'. When reset to a '0', the M48T02/12 oscillator starts within 1 second.

Calibrating the Clock

The M48T02/12 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. A typical M48T02/12 is accurate within ±1 minute per month at 25°C without calibration. The devices are tested not to exceed ± 35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. The oscillation rate of any crystal changes with temperature (see Figure 10). Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M48T02/12 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in Figure 11. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened or lengthened by 128 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48T02/12 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte.

Table 11. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
7FFh	10 Years				Year				Year	00-99
7FEh	0	0	0	10 M.	Month				Month	01-12
7FDh	0	0	10 Date		Date				Date	01-31
7FCh	0	FT	0	0	0	Day			Day	01-07
7FBh	0	0	10 Hours		Hours				Hour	00-23
7FAh	0	10 Minutes			Minutes				Minutes	00-59
7F9h	ST	10 Seconds			Seconds				Seconds	00-59
7F8h	W	R	S	Calibration					Control	

Keys: S = SIGN Bit
FT = FREQUENCY TEST Bit (Set to '0' for normal clock operation)
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to '0'

Figure 10. Crystal Accuracy Across Temperature

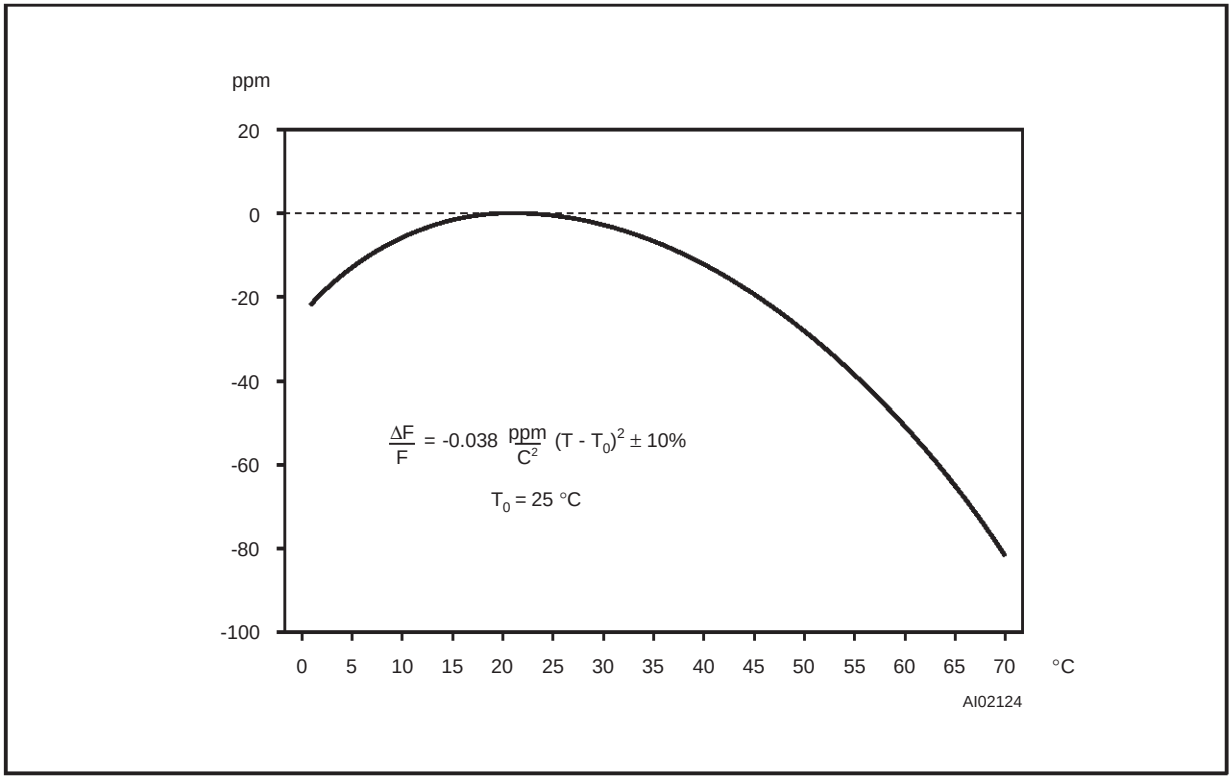
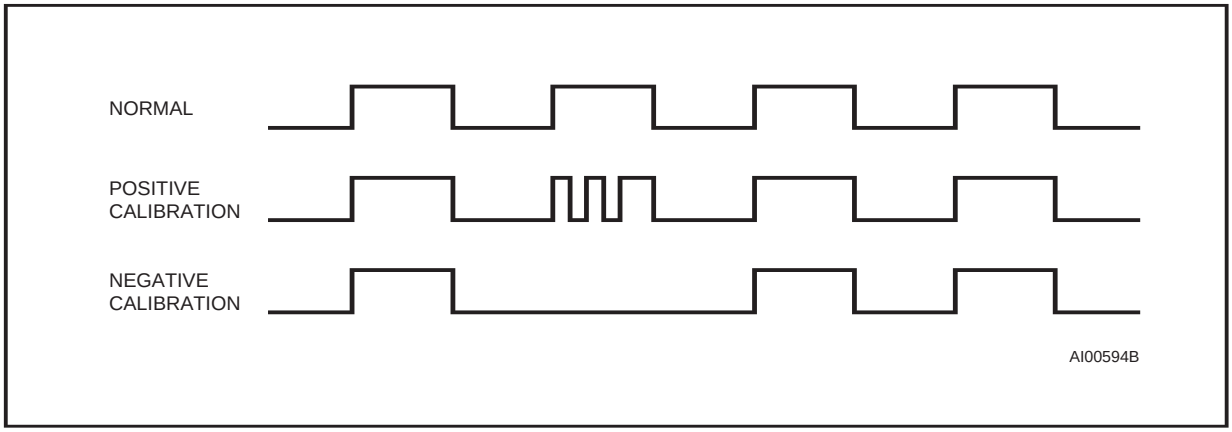


Figure 11. Clock Calibration



CLOCK OPERATION (cont'd)

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day Register, is set to a '1', and the oscillator is running at 32,768 Hz, the LSB (DQ0) of the Seconds Register will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 ppm oscillator frequency error, requiring a -10(WR001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency. The device must be selected and address 7F9h must be held constant when reading the 512 Hz on DQ0.

The FT bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds Register is monitored by holding the M48T02/12 in an extended read of the Seconds Register, without having the Read bit set. The FT bit MUST be reset to '0' for normal clock operations to resume.

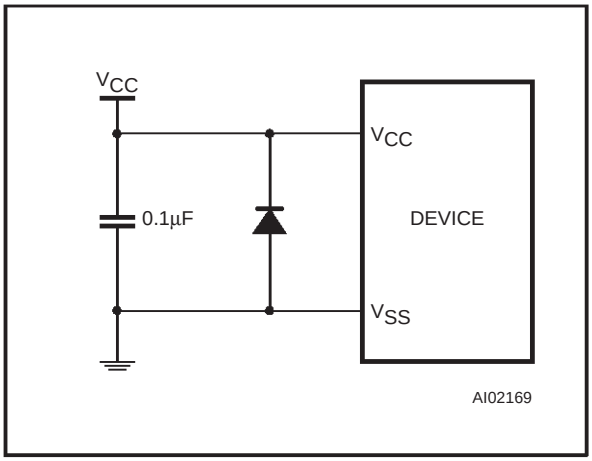
For more information on calibration, see the Application Note AN924 "TIMEKEEPER Calibration".

POWER SUPPLY DECOUPLING and UNDERSHOOT PROTECTION

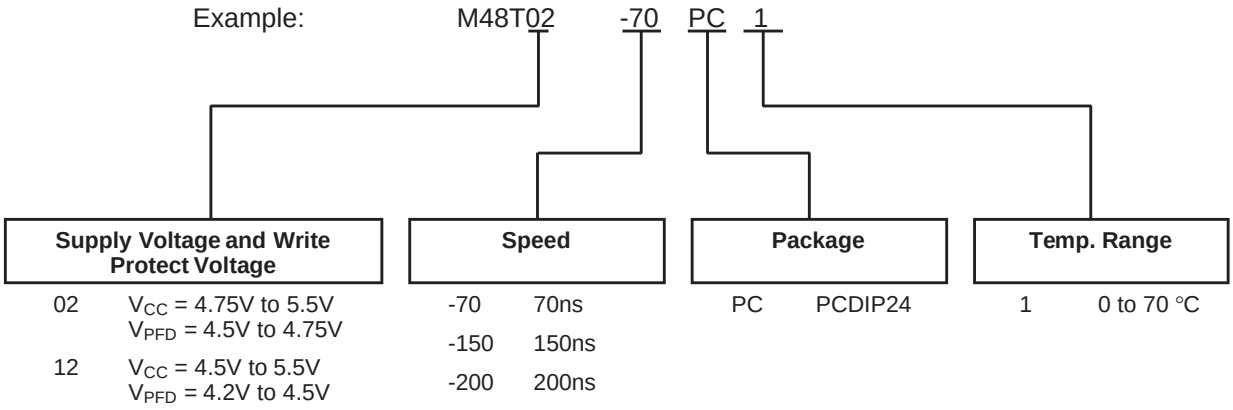
I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy, which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A bypass capacitor value of 0.1µF (as shown in Figure 12) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one Volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommeded to connect a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 12. Supply Voltage Protection



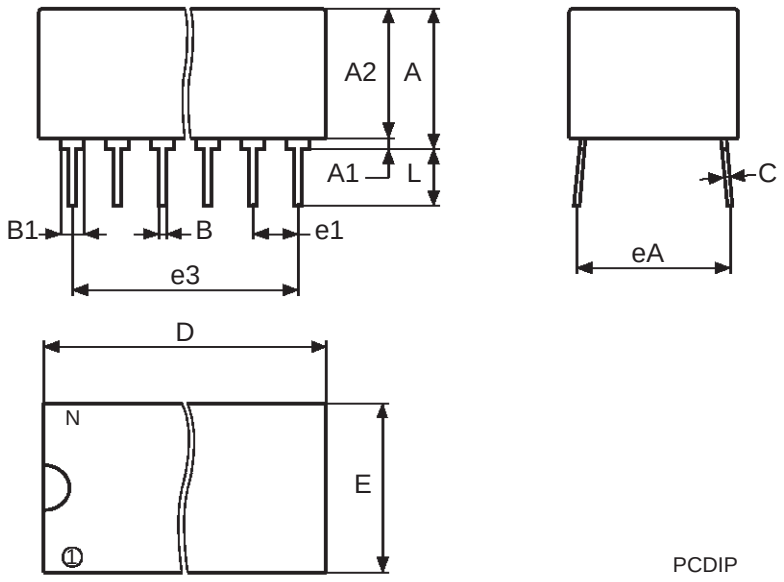
ORDERING INFORMATION SCHEME



For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PCDIP24 - 24 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		34.29	34.80		1.350	1.370
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		25.15	30.73		0.990	1.210
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	24			24		



PCDIP

Drawing is not to scale.

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