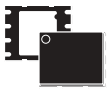
# M45PE80

## 8 Mbit, Low Voltage, Page-Erasable Serial Flash Memory With Byte-Alterability and a 25 MHz SPI Bus Interface

### FEATURES SUMMARY

- 8Mbit of Page-Erasable Flash Memory
- Page Write (up to 256 Bytes) in 11ms (typical)
- Page Program (up to 256 Bytes) in 1.2ms (typical)
- Page Erase (256 Bytes) in 10ms (typical)
- Sector Erase (512 Kbit)
- 2.7 to 3.6V Single Supply Voltage
- SPI Bus Compatible Serial Interface
- 25MHz Clock Rate (maximum)
- Deep Power-down Mode 1µA (typical)
- Electronic Signature
  - JEDEC Standard Two-Byte Signature (4014h)
- More than 100,000 Write Cycles
- More than 20 Year Data Retention

**Figure 1. Packages**



VDFPN8 (MP)
6x5mm (MLP8)



SO16 (MF)
300 mil width

# TABLE OF CONTENTS

**FEATURES SUMMARY . . . 1**
Figure 1. Packages . . . 1
**SUMMARY DESCRIPTION . . . 5**
Figure 2. Logic Diagram . . . 5
Table 1. Signal Names . . . 5
Figure 3. VDFPN Connections . . . 5
Figure 4. SO Connections . . . 5
**SIGNAL DESCRIPTION . . . 6**
Serial Data Output (Q) . . . 6
Serial Data Input (D) . . . 6
Serial Clock (C) . . . 6
Chip Select (S) . . . 6
Reset ($\overline{\text{Reset}}$) . . . 6
Write Protect (W) . . . 6
**SPI MODES . . . 7**
Figure 5. Bus Master and Memory Devices on the SPI Bus . . . 7
Figure 6. SPI Modes Supported . . . 7
**OPERATING FEATURES . . . 8**
**Sharing the Overhead of Modifying Data . . . 8**
**An Easy Way to Modify Data . . . 8**
**A Fast Way to Modify Data . . . 8**
**Polling During a Write, Program or Erase Cycle . . . 8**
**Reset . . . 8**
**Active Power, Stand-by Power and Deep Power-Down Modes . . . 8**
**Status Register . . . 9**
WIP bit . . . 9
WEL bit . . . 9
Table 2. Status Register Format . . . 9
**Protection Modes . . . 9**
**MEMORY ORGANIZATION . . . 10**
Table 3. Memory Organization . . . 10
Figure 7. Block Diagram . . . 11
**INSTRUCTIONS . . . 12**
Table 4. Instruction Set . . . 12
**Write Enable (WREN) . . . 13**
Figure 8. Write Enable (WREN) Instruction Sequence . . . 13
**Write Disable (WRDI) . . . 13**

Figure 9. Write Disable (WRDI) Instruction Sequence . . . . . 13
**Read Identification (RDID) . . . . . 14**
Table 5. Read Identification (RDID) Data-Out Sequence . . . . . 14
Figure 10.Read Identification (RDID) Instruction Sequence and Data-Out Sequence . . . . . 14
**Read Status Register (RDSR) . . . . . 15**
WIP bit . . . . . 15
WEL bit . . . . . 15
Figure 11.Read Status Register (RDSR) Instruction Sequence and Data-Out Sequence . . . . . 15
**Read Data Bytes (READ). . . . . 16**
Figure 12.Read Data Bytes (READ) Instruction Sequence and Data-Out Sequence . . . . . 16
**Read Data Bytes at Higher Speed (FAST_READ) . . . . . 17**
Figure 13.Read Data Bytes at Higher Speed (FAST_READ) Instruction Sequence and Data-Out Sequence 17
**Page Write (PW) . . . . . 18**
Figure 14.Page Write (PW) Instruction Sequence. . . . . 18
**Page Program (PP) . . . . . 19**
Figure 15.Page Program (PP) Instruction Sequence . . . . . 19
**Page Erase (PE) . . . . . 20**
Figure 16.Page Erase (PE) Instruction Sequence. . . . . 20
**Sector Erase (SE) . . . . . 21**
Figure 17.Sector Erase (SE) Instruction Sequence. . . . . 21
**Deep Power-down (DP) . . . . . 22**
Figure 18.Deep Power-down (DP) Instruction Sequence . . . . . 22
**Release from Deep Power-down (RDP) . . . . . 23**
Figure 19.Release from Deep Power-down (RDP) Instruction Sequence. . . . . 23

**POWER-UP AND POWER-DOWN . . . . . 24**
Figure 20.Power-up Timing . . . . . 24
Table 6. Power-Up Timing and VWI Threshold . . . . . 25

**INITIAL DELIVERY STATE. . . . . 25**

**MAXIMUM RATING. . . . . 26**
Table 7. Absolute Maximum Ratings. . . . . 26

**DC AND AC PARAMETERS. . . . . 27**
Table 8. Operating Conditions . . . . . 27
Table 9. AC Measurement Conditions. . . . . 27
Figure 21.AC Measurement I/O Waveform . . . . . 27
Table 10. Capacitance. . . . . 27
Table 11. DC Characteristics. . . . . 28
Table 12. AC Characteristics . . . . . 29
Figure 22.Serial Input Timing . . . . . 30
Figure 23.Write Protect Setup and Hold Timing . . . . . 30
Figure 24.Output Timing . . . . . 31
Figure 25.Reset AC Waveforms . . . . . 31

**PACKAGE MECHANICAL . . . . . 32**

Figure 26.MLP8, 8-lead Very thin Dual Flat Package No lead, 6x5mm, Package Outline . . . . . 32
Table 13. MLP8, 8-lead Very thin Dual Flat Package No lead, 6x5mm, Package Mechanical Data 32
Figure 27.SO16 wide – 16-lead Plastic Small Outline, 300 mils body width, Package Outline . . . . 33
Table 14. SO16 wide – 16-lead Plastic Small Outline, 300 mils body width, Mechanical Data . . . . 33

**PART NUMBERING . . . . . 34**

Table 15. Ordering Information Scheme . . . . . 34

**REVISION HISTORY . . . . . 35**

Table 16. Document Revision History . . . . . 35

## SUMMARY DESCRIPTION

The M45PE80 is a 8Mbit (1M x 8 bit) Serial Paged Flash Memory accessed by a high speed SPI-compatible bus.

The memory can be written or programmed 1 to 256 bytes at a time, using the Page Write or Page Program instruction. The Page Write instruction consists of an integrated Page Erase cycle followed by a Page Program cycle.

The memory is organized as 16 sectors, each containing 256 pages. Each page is 256 bytes wide. Thus, the whole memory can be viewed as consisting of 4096 pages, or 1,048,576 bytes.

The memory can be erased a page at a time, using the Page Erase instruction, or a sector at a time, using the Sector Erase instruction.

**Figure 2. Logic Diagram**

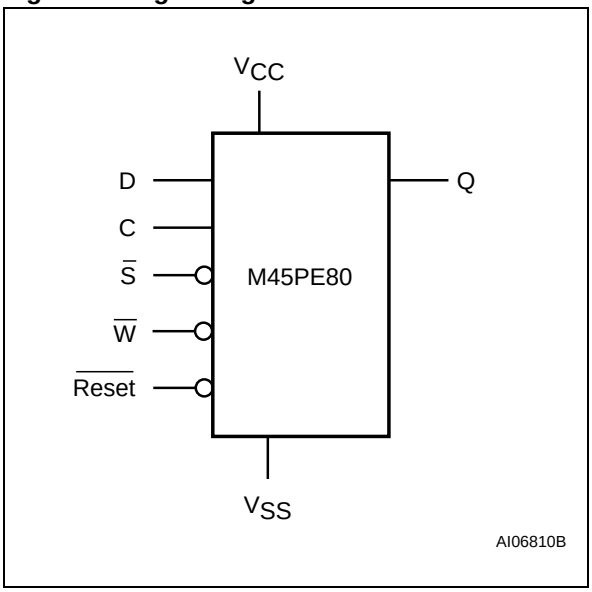
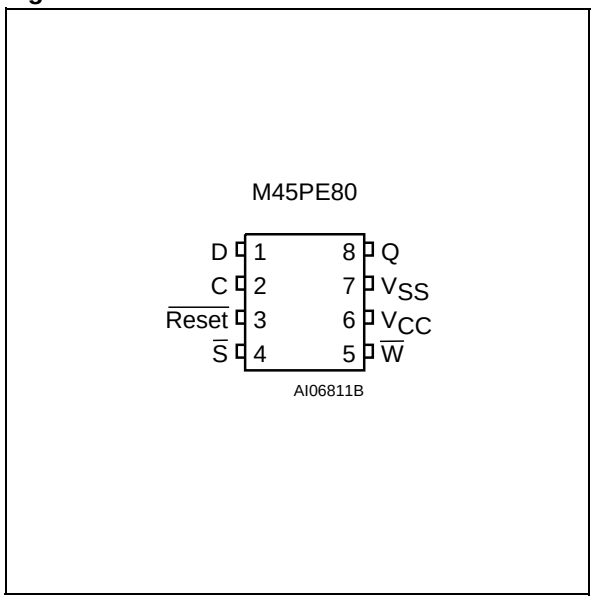



**Table 1. Signal Names**

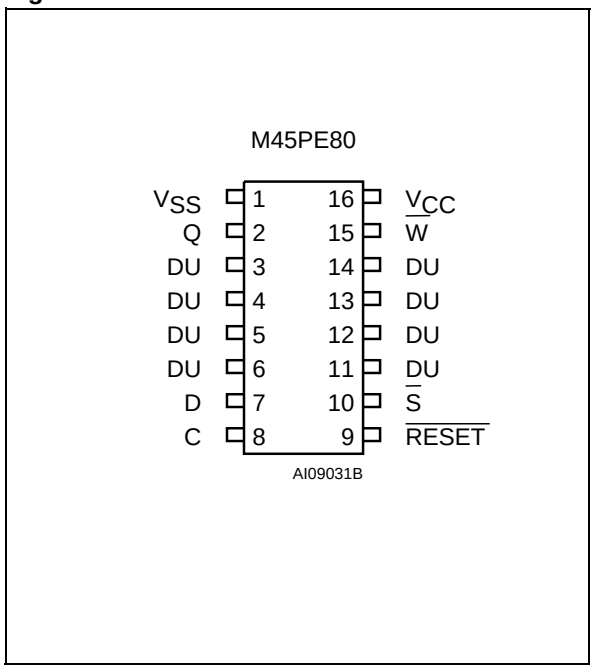
| | |
|---|---|
| C | Serial Clock |
| D | Serial Data Input |
| Q | Serial Data Output |
| $\overline{S}$ | Chip Select |
| $\overline{W}$ | Write Protect |
| $\overline{Reset}$ | Reset |
| $V_{CC}$ | Supply Voltage |
| $V_{SS}$ | Ground |

**Figure 3. VDFPN Connections**




Note: 1. There is an exposed die paddle on the underside of the MLP8 package. This is pulled, internally, to $V_{SS}$, and must not be allowed to be connected to any other voltage or signal line on the PCB.
2. See PACKAGE MECHANICAL section for package dimensions, and how to identify pin-1.

**Figure 4. SO Connections**




Note: 1. DU = Don't Use
2. See PACKAGE MECHANICAL section for package dimensions, and how to identify pin-1.

## SIGNAL DESCRIPTION

**Serial Data Output (Q).** This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

**Serial Data Input (D).** This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C).

**Serial Clock (C).** This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

**Chip Select ($\overline{S}$).** When this input signal is High, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Read, Program, Erase or Write cycle is in progress, the device will be in the Standby mode (this is not the Deep Power-down mode). Driving Chip Select ($\overline{S}$) Low enables the device, placing it in the active power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

**Reset ($\overline{Reset}$).** The Reset ($\overline{Reset}$) input provides a hardware reset for the memory. In this mode, the outputs are high impedance.

When Reset ($\overline{Reset}$) is driven High, the memory is in the normal operating mode. When Reset ($\overline{Reset}$) is driven Low, the memory will enter the Reset mode, provided that no internal operation is currently in progress. Driving Reset ($\overline{Reset}$) Low while an internal operation is in progress has no effect on that internal operation (a write cycle, program cycle, or erase cycle).

**Write Protect ($\overline{W}$).** This input signal puts the device in the Hardware Protected mode, when Write Protect ($\overline{W}$) is connected to $V_{SS}$, causing the first 256 pages of memory to become read-only by protecting them from write, program and erase operations. When Write Protect ($\overline{W}$) is connected to $V_{CC}$, the first 256 pages of memory behave like the other pages of memory.

## SPI MODES

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

– CPOL=0, CPHA=0

– CPOL=1, CPHA=1

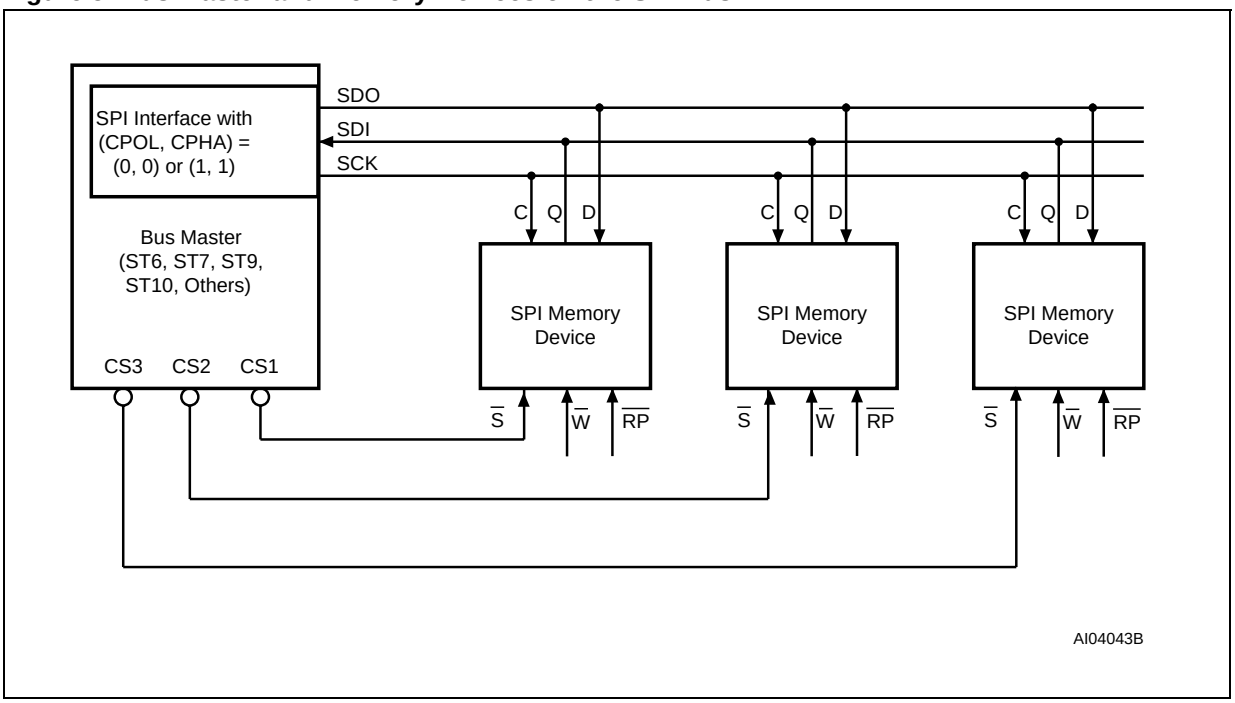
For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in Figure 6., is the clock polarity when the bus master is in Stand-by mode and not transferring data:

– C remains at 0 for (CPOL=0, CPHA=0)

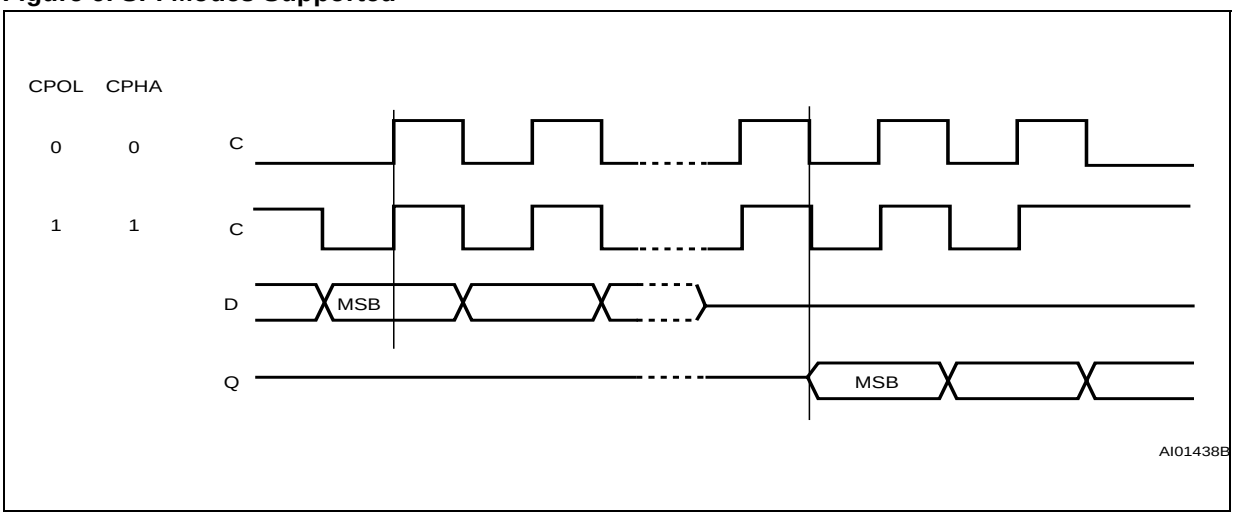
– C remains at 1 for (CPOL=1, CPHA=1)

**Figure 5. Bus Master and Memory Devices on the SPI Bus**




Note: The Write Protect ($\overline{W}$) signal should be driven, High or Low as appropriate.

**Figure 6. SPI Modes Supported**



## OPERATING FEATURES

### Sharing the Overhead of Modifying Data

To write or program one (or more) data bytes, two instructions are required: Write Enable (WREN), which is one byte, and a Page Write (PW) or Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal cycle (of duration $t_{PW}$ or $t_{PP}$).

To share this overhead, the Page Write (PW) or Page Program (PP) instruction allows up to 256 bytes to be programmed (changing bits from 1 to 0) or written (changing bits to 0 or 1) at a time, provided that they lie in consecutive addresses on the same page of memory.

### An Easy Way to Modify Data

The Page Write (PW) instruction provides a convenient way of modifying data (up to 256 contiguous bytes at a time), and simply requires the start address, and the new data in the instruction sequence.

The Page Write (PW) instruction is entered by driving Chip Select ($\overline{S}$) Low, and then transmitting the instruction byte, three address bytes (A23-A0) and at least one data byte, and then driving Chip Select ($\overline{S}$) High. While Chip Select ($\overline{S}$) is being held Low, the data bytes are written to the data buffer, starting at the address given in the third address byte (A7-A0). When Chip Select ($\overline{S}$) is driven High, the Write cycle starts. The remaining, unchanged, bytes of the data buffer are automatically loaded with the values of the corresponding bytes of the addressed memory page. The addressed memory page then automatically put into an Erase cycle. Finally, the addressed memory page is programmed with the contents of the data buffer.

All of this buffer management is handled internally, and is transparent to the user. The user is given the facility of being able to alter the contents of the memory on a byte-by-byte basis.

### A Fast Way to Modify Data

The Page Program (PP) instruction provides a fast way of modifying data (up to 256 contiguous bytes at a time), provided that it only involves resetting bits to 0 that had previously been set to 1.

This might be:

– when the designer is programming the device for the first time
– when the designer knows that the page has already been erased by an earlier Page Erase (PE) or Sector Erase (SE) instruction. This is useful, for example, when storing a fast stream of data, having first performed the erase cycle when time was available
– when the designer knows that the only changes involve resetting bits to 0 that are still set to 1. When this method is possible, it has the additional advantage of minimising the number of unnecessary erase operations, and the extra stress incurred by each page.

### Polling During a Write, Program or Erase Cycle

A further improvement in the write, program or erase time can be achieved by not waiting for the worst case delay ($t_{PW}$, $t_{PP}$, $t_{PE}$, or $t_{SE}$). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous cycle is complete.

### Reset

An internal Power-On Reset circuit helps protect against inadvertant data writes. Addition protection is provided by driving Reset ($\overline{Reset}$) Low during the Power-on process, and only driving it High when $V_{CC}$ has reached the correct voltage level, $V_{CC}$(min).

### Active Power, Stand-by Power and Deep Power-Down Modes

When Chip Select ($\overline{S}$) is Low, the device is enabled, and in the Active Power mode.

When Chip Select ($\overline{S}$) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write). The device then goes in to the Stand-by Power mode. The device consumption drops to $I_{CC1}$.

The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to $I_{CC2}$. The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Electronic Signature (RES) instruction) is executed.

All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertant Write, Program or Erase instructions.

### Status Register

The Status Register contains two status bits that can be read by the Read Status Register (RDSR) instruction.

**WIP bit.** The Write In Progress (WIP) bit indicates whether the memory is busy with a Write, Program or Erase cycle.

**WEL bit.** The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch.

**Table 2. Status Register Format**

| b7 | | | | | | | b0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | WEL | WIP |

Note: 1. WEL and WIP are volatile read-only bits (WEL is set and reset by specific instructions; WIP is automatically set and reset by the internal logic of the device).

### Protection Modes

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the M45PE80 boasts the following data protection mechanisms:

- Power-On Reset and an internal timer ($t_{PUW}$) can provide protection against inadvertant changes while the power supply is outside the operating specification.
- Program, Erase and Write instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit . This bit is returned to its reset state by the following events:
  - Power-up
  - Reset ($\overline{\text{RESET}}$) driven Low
  - Write Disable (WRDI) instruction completion
  - Page Write (PW) instruction completion
  - Page Program (PP) instruction completion
  - Page Erase (PE) instruction completion
  - Sector Erase (SE) instruction completion
- The Hardware Protected mode is entered when Write Protect ($\overline{\text{W}}$) is driven Low, causing the first 256 pages of memory to become read-only. When Write Protect ($\overline{\text{W}}$) is driven High, the first 256 pages of memory behave like the other pages of memory
- The Reset ($\overline{\text{Reset}}$) signal can be driven Low to protect the contents of the memory during any critical time, not just during Power-up and Power-down.
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertant Write, Program and Erase instructions while the device is not in active use.

## MEMORY ORGANIZATION

The memory is organized as:

- 4096 pages (256 bytes each).
- 1,048,576 bytes (8 bits each)
- 16 sectors (512 Kbits, 65536 bytes each)

Each page can be individually:

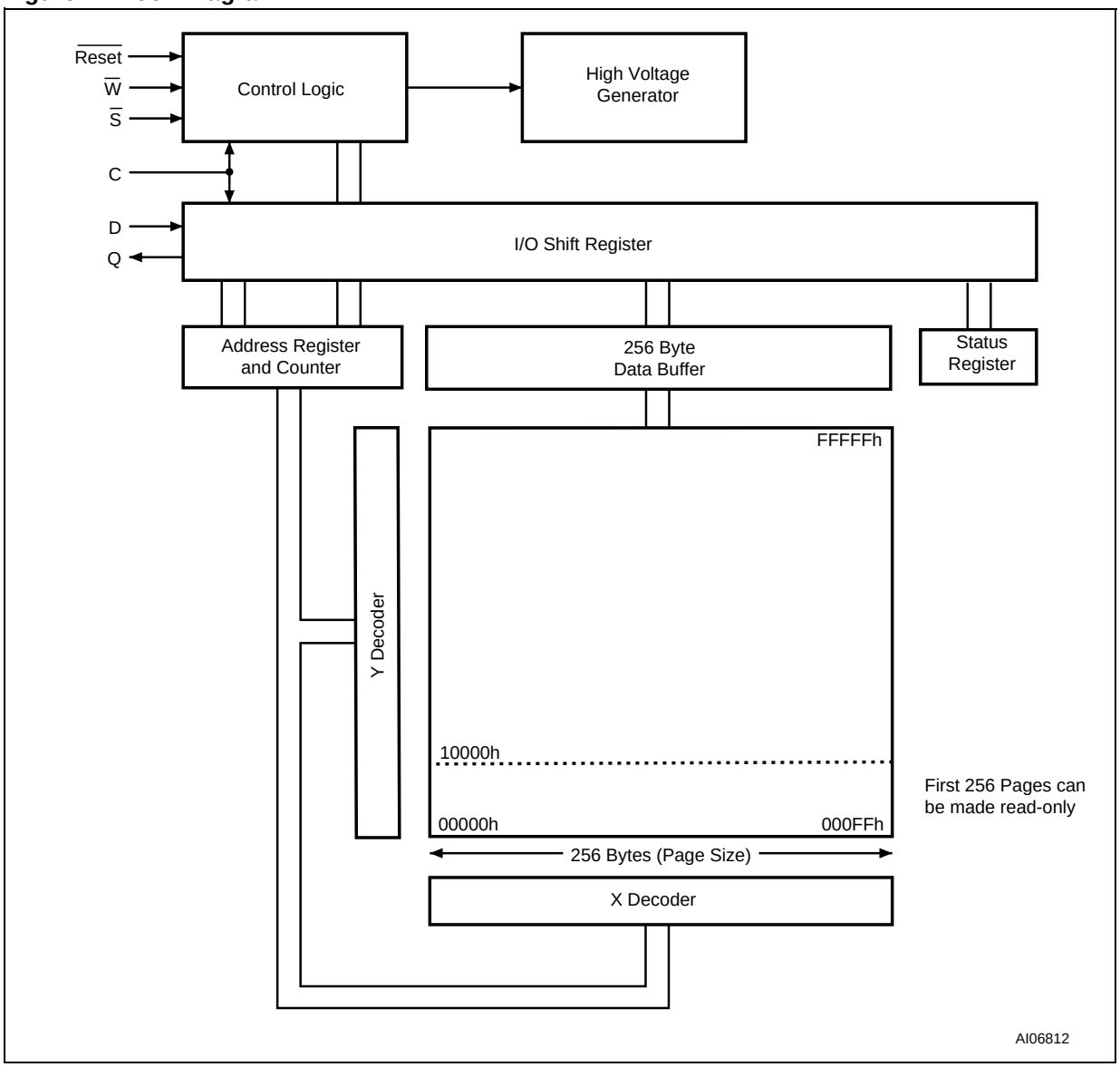
– programmed (bits are programmed from 1 to 0)
– erased (bits are erased from 0 to 1)
– written (bits are changed to either 0 or 1)

The device is Page or Sector Erasable (bits are erased from 0 to 1).

**Table 3. Memory Organization**

| Sector | Address Range | |
|---|---|---|
| 15 | F0000h | FFFFFh |
| 14 | E0000h | EFFFFh |
| 13 | D0000h | DFFFFh |
| 12 | C0000h | CFFFFh |
| 11 | B0000h | BFFFFh |
| 10 | A0000h | AFFFFh |
| 9 | 90000h | 9FFFFh |
| 8 | 80000h | 8FFFFh |
| 7 | 70000h | 7FFFFh |
| 6 | 60000h | 6FFFFh |
| 5 | 50000h | 5FFFFh |
| 4 | 40000h | 4FFFFh |
| 3 | 30000h | 3FFFFh |
| 2 | 20000h | 2FFFFh |
| 1 | 10000h | 1FFFFh |
| 0 | 00000h | 0FFFFh |

**Figure 7. Block Diagram**



## INSTRUCTIONS

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial Data Input (D) is sampled on the first rising edge of Serial Clock (C) after Chip Select ($\overline{S}$) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (D), each bit being latched on the rising edges of Serial Clock (C).

The instruction set is listed in Table 4..

Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none.

In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast_Read) or Read Status Register (RDSR) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select ($\overline{S}$) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Write (PW), Page Program (PP), Page Erase (PE), Sector Erase (SE), Write Enable (WREN), Write Disable (WRDI), Deep Power-down (DP) or Release from Deep Power-down (RDP) instruction, Chip Select ($\overline{S}$) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select ($\overline{S}$) must driven High when the number of clock pulses after Chip Select ($\overline{S}$) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a Write cycle, Program cycle or Erase cycle are ignored, and the internal Write cycle, Program cycle or Erase cycle continues unaffected.

**Table 4. Instruction Set**

| Instruction | Description | One-byte Instruction Code | | Address Bytes | Dummy Bytes | Data Bytes |
|---|---|---|---|---|---|---|
| WREN | Write Enable | 0000 0110 | 06h | 0 | 0 | 0 |
| WRDI | Write Disable | 0000 0100 | 04h | 0 | 0 | 0 |
| RDID | Read Identification | 1001 1111 | 9Fh | 0 | 0 | 1 to 3 |
| RDSR | Read Status Register | 0000 0101 | 05h | 0 | 0 | 1 to ∞ |
| READ | Read Data Bytes | 0000 0011 | 03h | 3 | 0 | 1 to ∞ |
| FAST_READ | Read Data Bytes at Higher Speed | 0000 1011 | 0Bh | 3 | 1 | 1 to ∞ |
| PW | Page Write | 0000 1010 | 0Ah | 3 | 0 | 1 to 256 |
| PP | Page Program | 0000 0010 | 02h | 3 | 0 | 1 to 256 |
| PE | Page Erase | 1101 1011 | DBh | 3 | 0 | 0 |
| SE | Sector Erase | 1101 1000 | D8h | 3 | 0 | 0 |
| DP | Deep Power-down | 1011 1001 | B9h | 0 | 0 | 0 |
| RDP | Release from Deep Power-down | 1010 1011 | ABh | 0 | 0 | 0 |

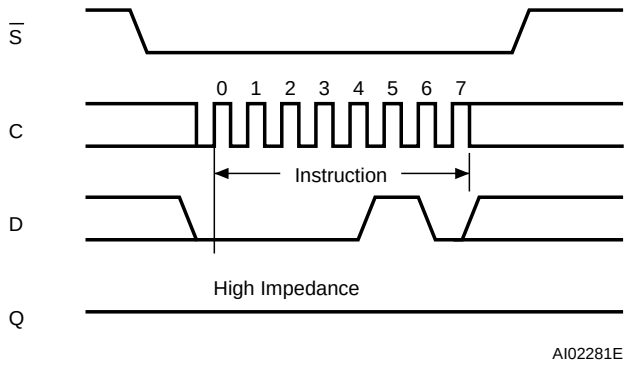
### Write Enable (WREN)

The Write Enable (WREN) instruction (Figure 8.) sets the Write Enable Latch (WEL) bit.

The Write Enable Latch (WEL) bit must be set prior to every Page Write (PW), Page Program (PP), Page Erase (PE), and Sector Erase (SE) instruction.

The Write Enable (WREN) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

**Figure 8. Write Enable (WREN) Instruction Sequence**




### Write Disable (WRDI)

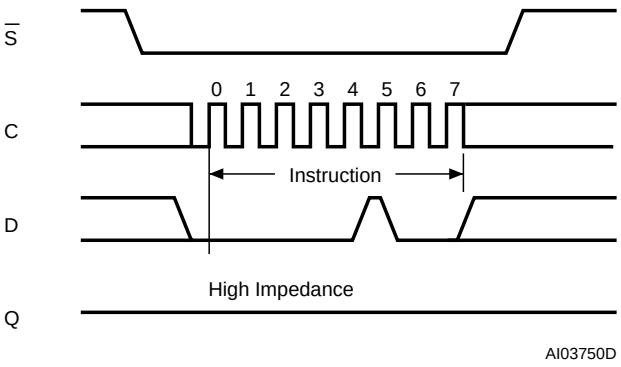
The Write Disable (WRDI) instruction (Figure 9.) resets the Write Enable Latch (WEL) bit.

The Write Disable (WRDI) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

The Write Enable Latch (WEL) bit is reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Page Write (PW) instruction completion
- Page Program (PP) instruction completion
- Page Erase (PE) instruction completion
- Sector Erase (SE) instruction completion

**Figure 9. Write Disable (WRDI) Instruction Sequence**



### Read Identification (RDID)

The Read Identification (RDID) instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The manufacturer identification is assigned by JEDEC, and has the value 20h for STMicroelectronics. The device identification is assigned by the device manufacturer, and indicates the memory type in the first byte (40h), and the memory capacity of the device in the second byte (14h).

Any Read Identification (RDID) instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving Chip Select ($\overline{S}$) Low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output (Q), each bit being shifted out during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 10..

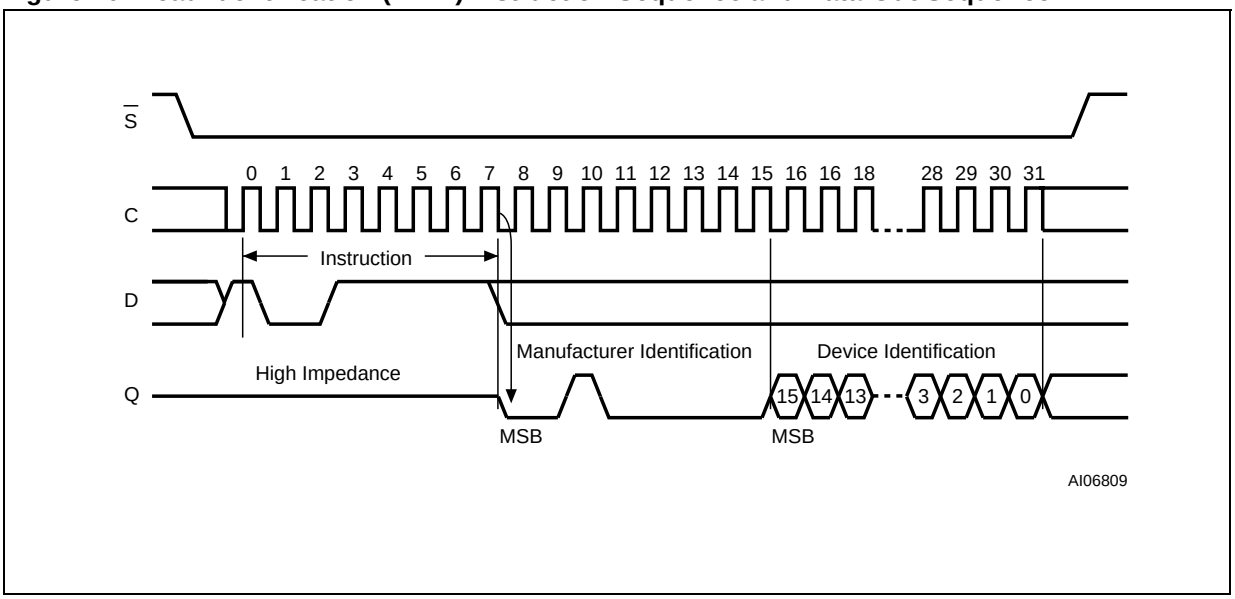
The Read Identification (RDID) instruction is terminated by driving Chip Select ($\overline{S}$) High at any time during data output.

When Chip Select ($\overline{S}$) is driven High, the device is put in the Stand-by Power mode. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

**Table 5. Read Identification (RDID) Data-Out Sequence**

| Manufacturer Identification | Device Identification | |
|---|---|---|
| | Memory Type | Memory Capacity |
| 20h | 40h | 14h |

**Figure 10. Read Identification (RDID) Instruction Sequence and Data-Out Sequence**



### Read Status Register (RDSR)

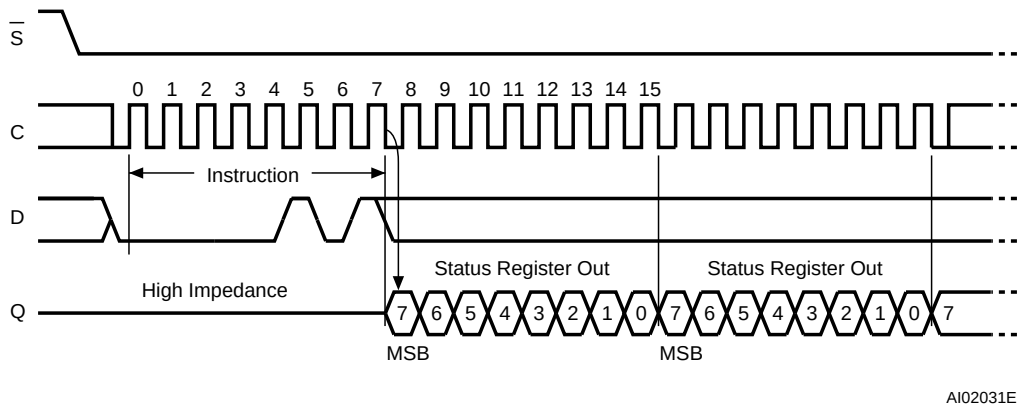
The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Figure 11..

The status bits of the Status Register are as follows:

**WIP bit.** The Write In Progress (WIP) bit indicates whether the memory is busy with a Write, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

**WEL bit.** The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write, Program or Erase instruction is accepted.

**Figure 11. Read Status Register (RDSR) Instruction Sequence and Data-Out Sequence**



### Read Data Bytes (READ)

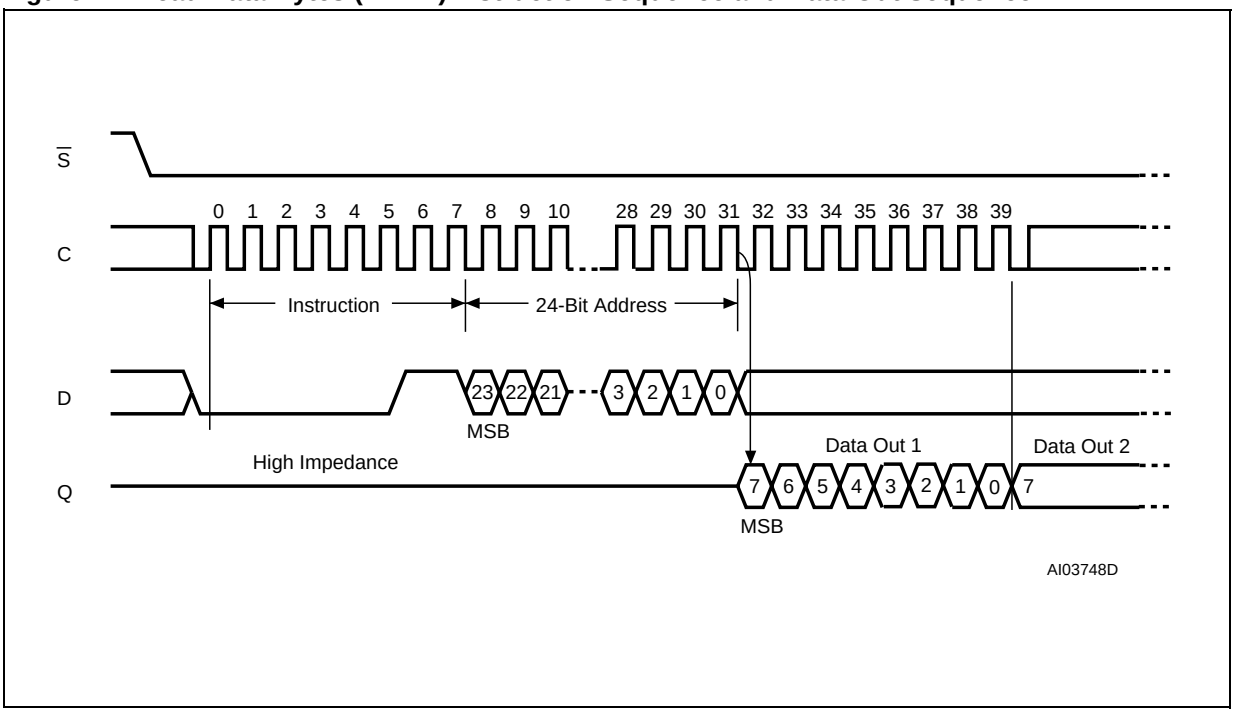
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data Output (Q), each bit being shifted out, at a maximum frequency $f_R$, during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 12..

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure 12. Read Data Bytes (READ) Instruction Sequence and Data-Out Sequence**




Note: Address bits A23 to A20 are Don't Care.

### Read Data Bytes at Higher Speed (FAST_READ)

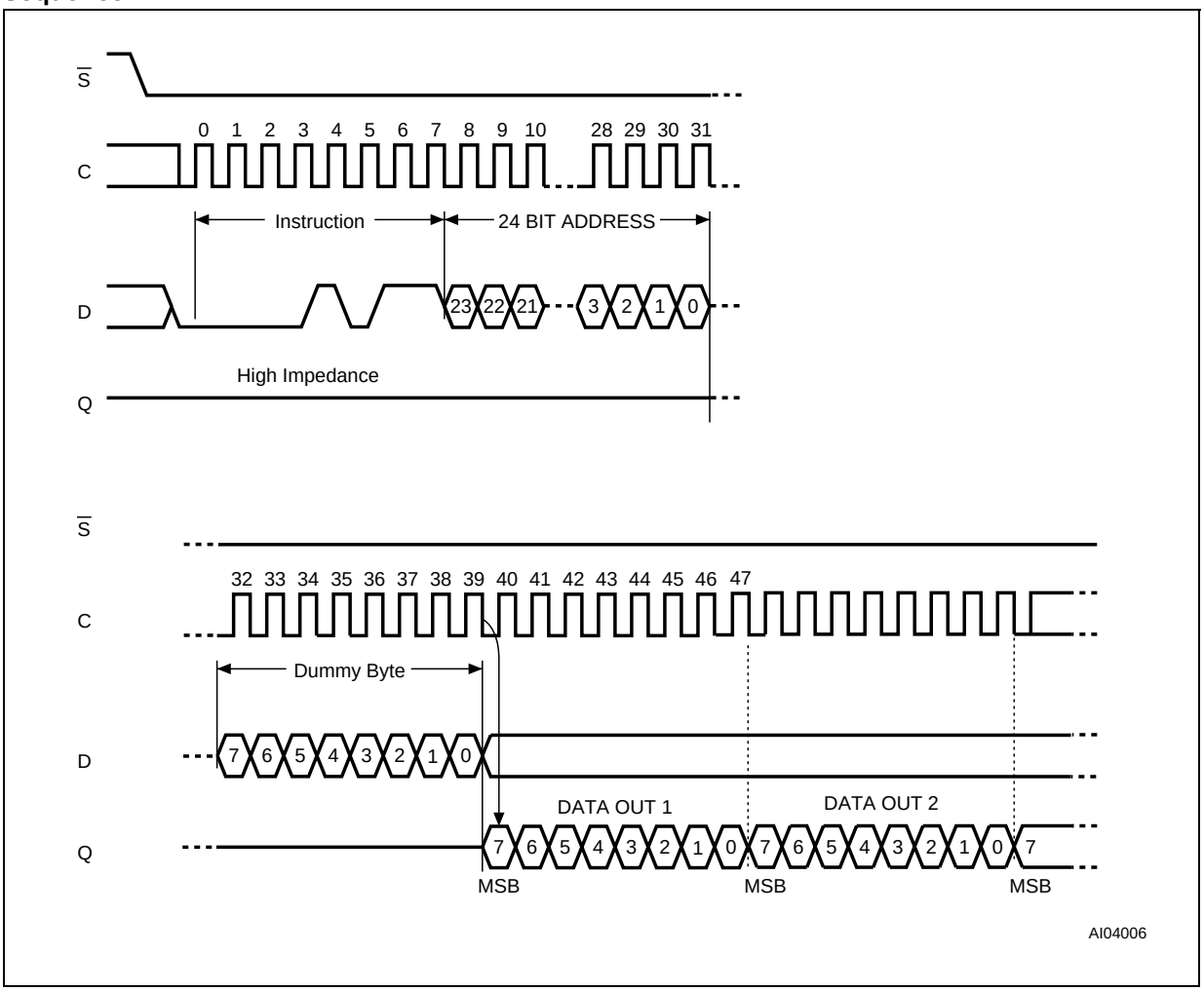
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data Output (Q), each bit being shifted out, at a maximum frequency $f_C$, during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 13..

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure 13. Read Data Bytes at Higher Speed (FAST_READ) Instruction Sequence and Data-Out Sequence**




Note: Address bits A23 to A20 are Don't Care.

### Page Write (PW)

The Page Write (PW) instruction allows bytes to be written in the memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Write (PW) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input (D). The rest of the page remains unchanged if no power failure occurs during this write cycle.

The Page Write (PW) instruction performs a page erase cycle even if only one byte is updated.

If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data exceeding the addressed page boundary roll over, and are written from the start address of the same page (the one whose 8 least significant address bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 14..

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be written correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly written at the requested addresses without having any effects on the other bytes of the same page.

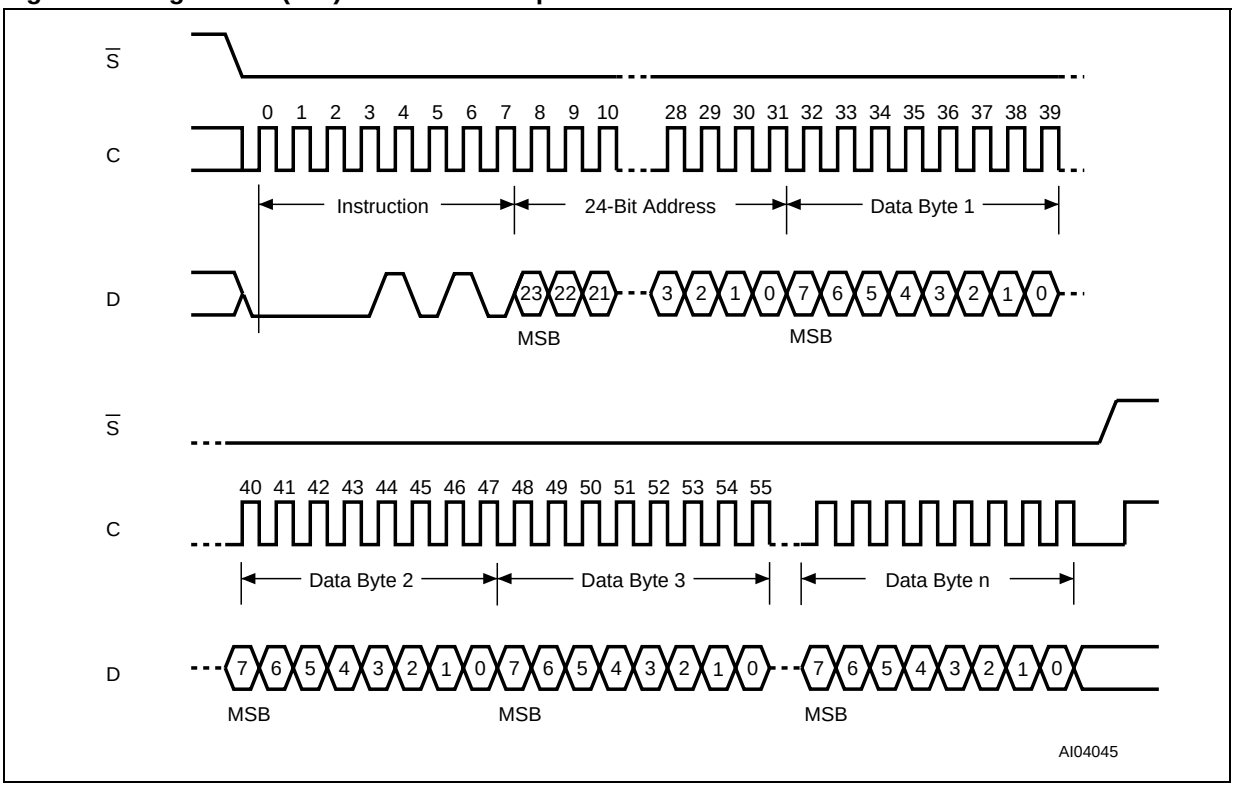
Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Write (PW) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Write cycle (whose duration is $t_{PW}$) is initiated. While the Page Write cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Write cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

A Page Write (PW) instruction applied to a page that is Hardware Protected is not executed.

Any Page Write (PW) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure 14. Page Write (PW) Instruction Sequence**




Note: 1. Address bits A23 to A20 are Don't Care
2. $1 \leq n \leq 256$

### Page Program (PP)

The Page Program (PP) instruction allows bytes to be programmed in the memory (changing bits from 1 to 0, only). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input (D). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data exceeding the addressed page boundary roll over, and are programmed from the start address of the same page (the one whose 8 least significant address bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 15..

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

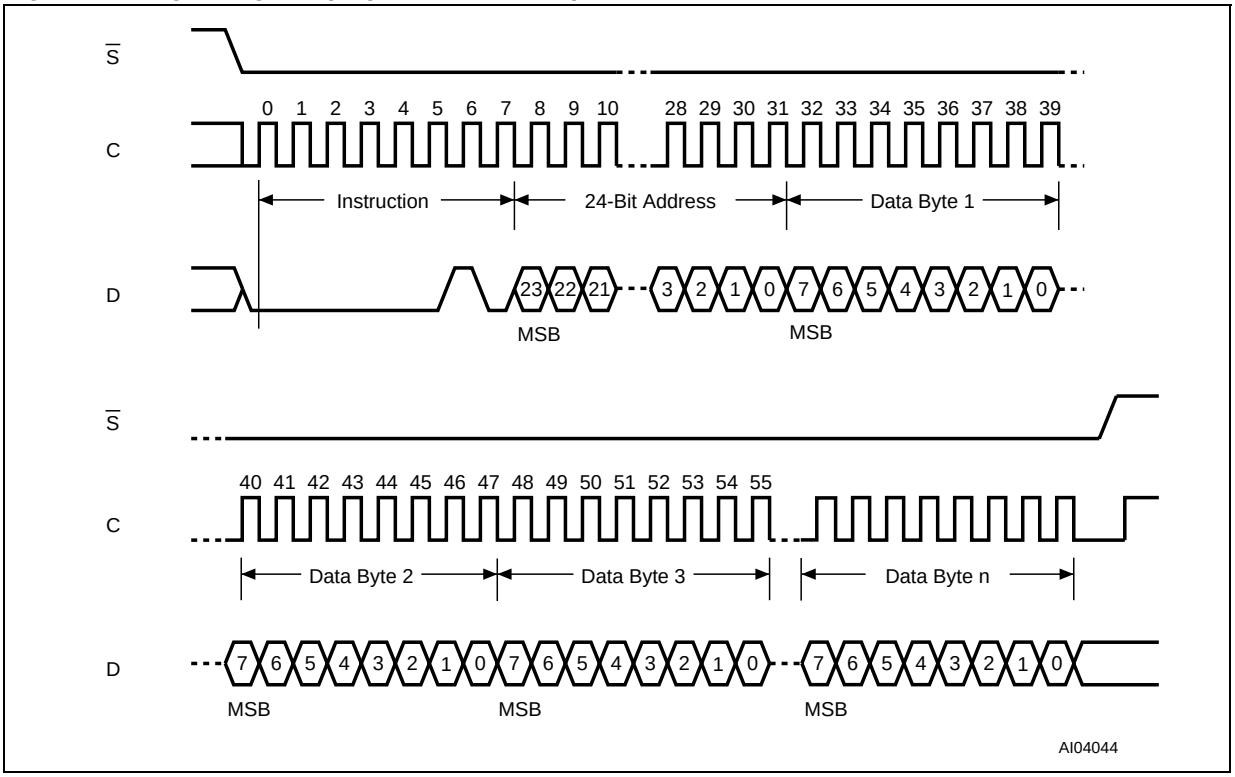
Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Program cycle (whose duration is $t_{PP}$) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page that is Hardware Protected is not executed.

Any Page Program (PP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure 15. Page Program (PP) Instruction Sequence**




Note: 1. Address bits A23 to A20 are Don't Care
2. $1 \leq n \leq 256$

### Page Erase (PE)

The Page Erase (PE) instruction sets to 1 (FFh) all bits inside the chosen page. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Erase (PE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, and three address bytes on Serial Data Input (D). Any address inside the Page is a valid address for the Page Erase (PE) instruction. Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

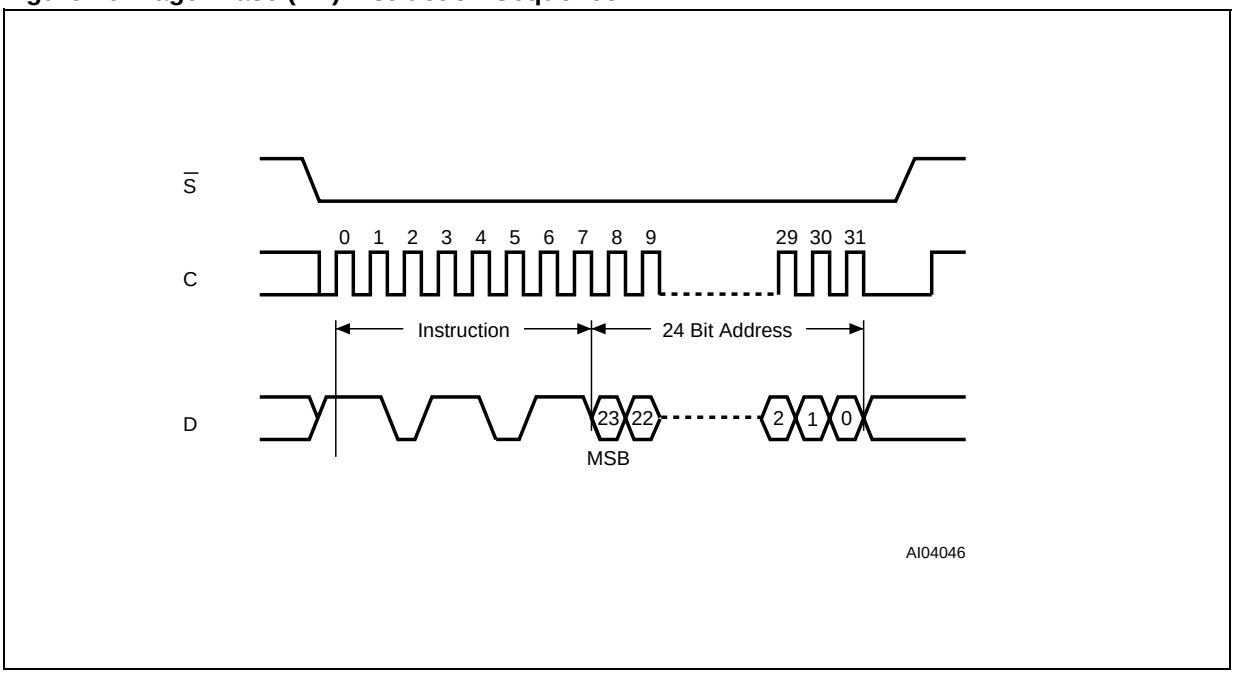
The instruction sequence is shown in Figure 16..

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Page Erase (PE) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Erase cycle (whose duration is $t_{PE}$) is initiated. While the Page Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

A Page Erase (PE) instruction applied to a page that is Hardware Protected is not executed.

Any Page Erase (PE) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure 16. Page Erase (PE) Instruction Sequence**




Note: Address bits A23 to A20 are Don't Care.

### Sector Erase (SE)

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Sector Erase (SE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, and three address bytes on Serial Data Input (D). Any address inside the Sector (see Table 3.) is a valid address for the Sector Erase (SE) instruction. Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

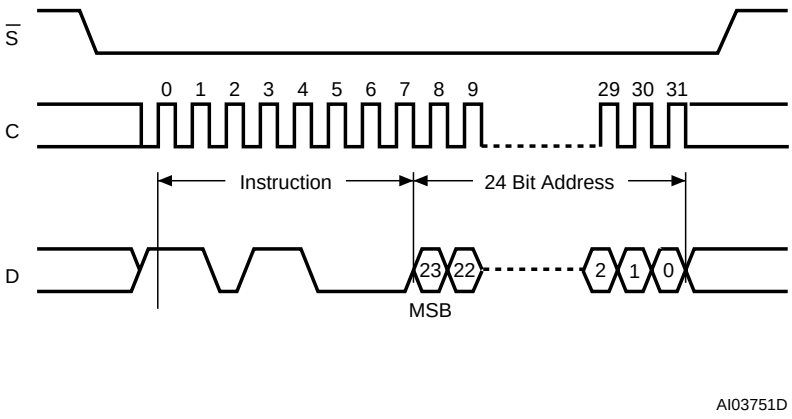
The instruction sequence is shown in Figure 17..

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Sector Erase cycle (whose duration is $t_{SE}$) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

A Sector Erase (SE) instruction applied to a sector that contains a page that is Hardware Protected is not executed.

Any Sector Erase (SE) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure 17. Sector Erase (SE) Instruction Sequence**




Note: Address bits A23 to A20 are Don't Care.

### Deep Power-down (DP)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

Driving Chip Select ($\overline{S}$) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, to reduce the standby current (from $I_{CC1}$ to $I_{CC2}$, as specified in Table 11.).

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down (RDP) instruction. This releases the device from this mode.

The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode.

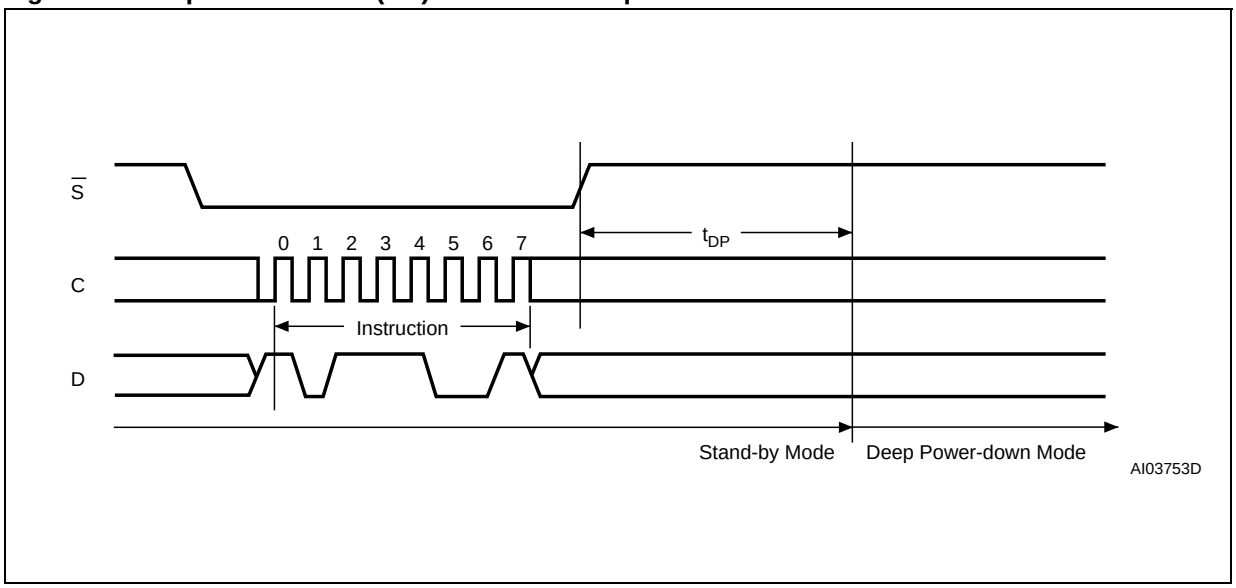
The Deep Power-down (DP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (D). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 18..

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, it requires a delay of $t_{DP}$ before the supply current is reduced to $I_{CC2}$ and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure 18. Deep Power-down (DP) Instruction Sequence**



### Release from Deep Power-down (RDP)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down (RDP) instruction. Executing this instruction takes the device out of the Deep Power-down mode.

The Release from Deep Power-down (RDP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (D). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

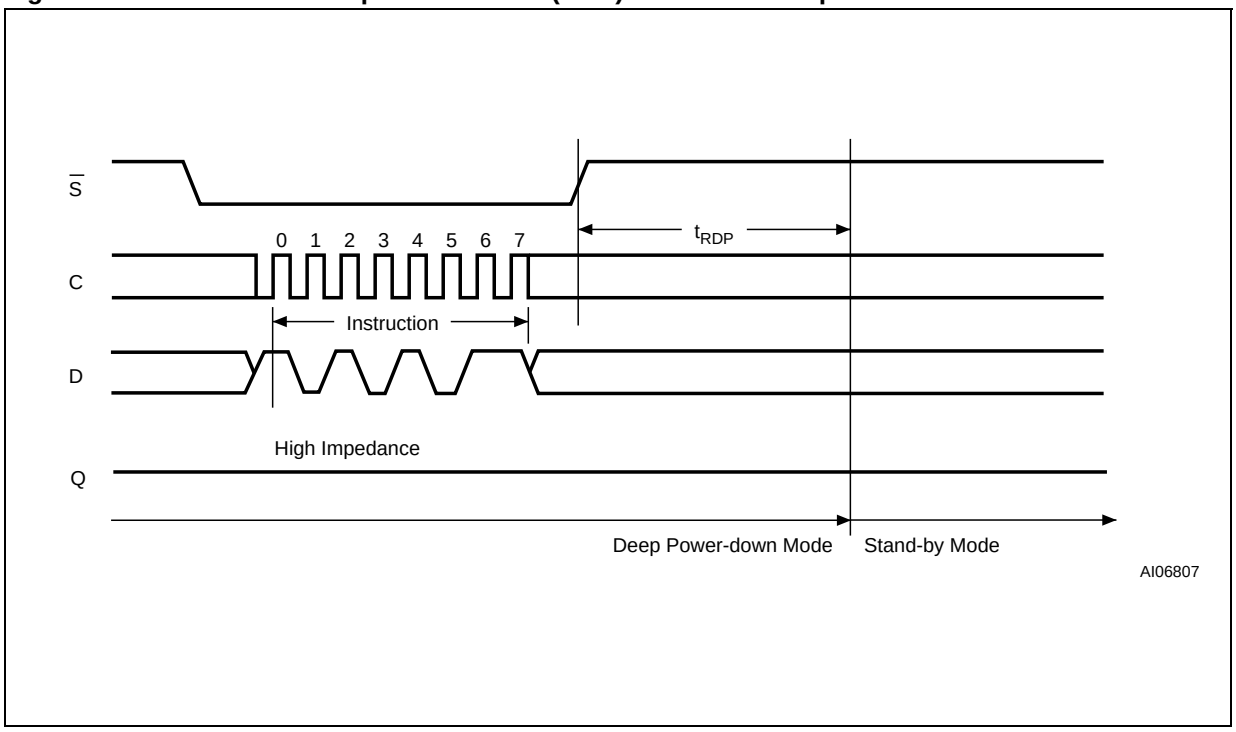
The instruction sequence is shown in Figure 19..

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select ($\overline{S}$) High. Sending additional clock cycles on Serial Clock (C), while Chip Select ($\overline{S}$) is driven Low, cause the instruction to be rejected, and not executed.

After Chip Select ($\overline{S}$) has been driven High, followed by a delay, $t_{RDP}$, the device is put in the Standby mode. Chip Select ($\overline{S}$) must remain High at least until this period is over. The device waits to be selected, so that it can receive, decode and execute instructions.

Any Release from Deep Power-down (RDP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure 19. Release from Deep Power-down (RDP) Instruction Sequence**



## POWER-UP AND POWER-DOWN

At Power-up and Power-down, the device must not be selected (that is Chip Select ($\overline{S}$) must follow the voltage applied on $V_{CC}$) until $V_{CC}$ reaches the correct value:

– $V_{CC}$(min) at Power-up, and then for a further delay of $t_{VSL}$

– $V_{SS}$ at Power-down

Usually a simple pull-up resistor on Chip Select ($\overline{S}$) can be used to insure safe and proper Power-up and Power-down.

To avoid data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while $V_{CC}$ is less than the POR threshold value, $V_{WI}$ – all operations are disabled, and the device does not respond to any instruction.

Moreover, the device ignores all Write Enable (WREN), Page Write (PW), Page Program (PP), Page Erase (PE) and Sector Erase (SE) instructions until a time delay of $t_{PUW}$ has elapsed after the moment that $V_{CC}$ rises above the $V_{WI}$ threshold. However, the correct operation of the device is not guaranteed if, by this time, $V_{CC}$ is still below $V_{CC}$(min). No Write, Program or Erase instructions should be sent until the later of:

– $t_{PUW}$ after $V_{CC}$ passed the $V_{WI}$ threshold

– $t_{VSL}$ after $V_{CC}$ passed the $V_{CC}$(min) level

These values are specified in Table 6..

If the delay, $t_{VSL}$, has elapsed, after $V_{CC}$ has risen above $V_{CC}$(min), the device can be selected for READ instructions even if the $t_{PUW}$ delay is not yet fully elapsed.

As an extra protection, the Reset ($\overline{Reset}$) signal could be driven Low for the whole duration of the Power-up and Power-down phases.

At Power-up, the device is in the following state:

– The device is in the Standby mode (not the Deep Power-down mode).

– The Write Enable Latch (WEL) bit is reset.

Normal precautions must be taken for supply rail decoupling, to stablise the $V_{CC}$ feed. Each device in a system should have the $V_{CC}$ rail decoupled by a suitable capacitor close to the package pins. (Generally, this capacitor is of the order of 0.1µF).

At Power-down, when $V_{CC}$ drops from the operating voltage, to below the POR threshold value, $V_{WI}$, all operations are disabled and the device does not respond to any instruction. (The designer needs to be aware that if a Power-down occurs while a Write, Program or Erase cycle is in progress, some data corruption can result.)

**Figure 20. Power-up Timing**

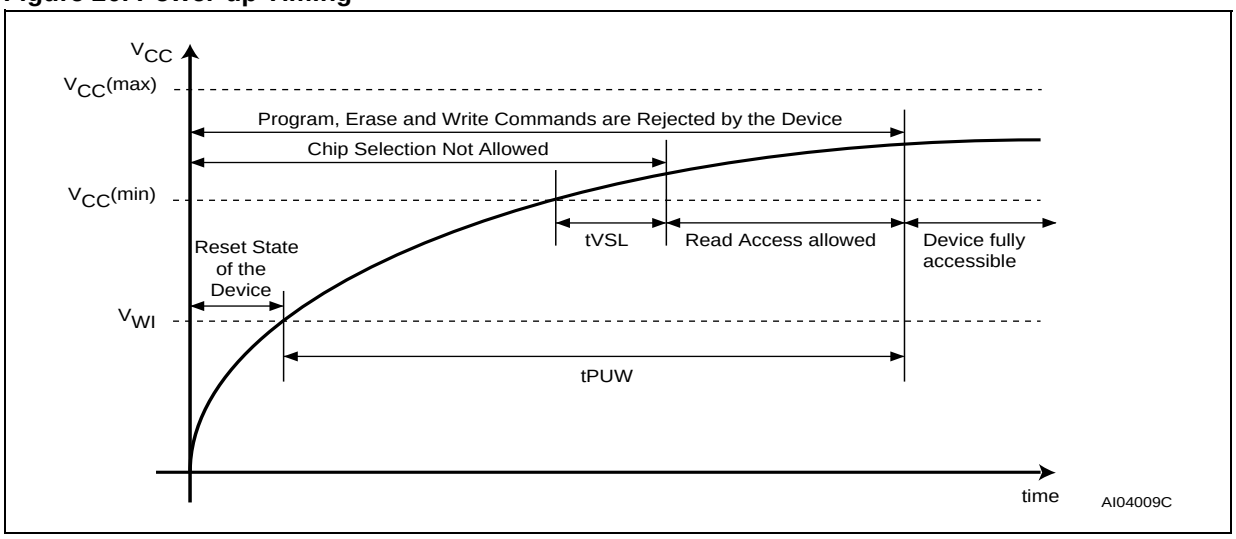


**Table 6. Power-Up Timing and $V_{WI}$ Threshold**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{VSL}$[1] | $V_{CC}$(min) to $\overline{S}$ low | 30 | | µs |
| $t_{PUW}$[1] | Time delay before the first Write, Program or Erase instruction | 1 | 10 | ms |
| $V_{WI}$[1] | Write Inhibit Voltage | 1.5 | 2.5 | V |

Note: 1. These parameters are characterized only, over the temperature range –40°C to +85°C.

## INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). All usable Status Register bits are 0.

## MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 7. Absolute Maximum Ratings**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_{STG}$ | Storage Temperature | –65 | 150 | °C |
| $T_{LEAD}$ | Lead Temperature during Soldering | See note [1] | | °C |
| $V_{IO}$ | Input and Output Voltage (with respect to Ground) | –0.6 | 4.0 | V |
| $V_{CC}$ | Supply Voltage | –0.6 | 4.0 | V |
| $V_{ESD}$ | Electrostatic Discharge Voltage (Human Body model) [2] | –2000 | 2000 | V |

Note: 1. Compliant with JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

## DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

**Table 8. Operating Conditions**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2.7 | 3.6 | V |
| $T_A$ | Ambient Operating Temperature | –40 | 85 | °C |

**Table 9. AC Measurement Conditions**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_L$ | Load Capacitance | 30 | | pF |
| | Input Rise and Fall Times | | 5 | ns |
| | Input Pulse Voltages | $0.2V_{CC}$ to $0.8V_{CC}$ | | V |
| | Input and Output Timing Reference Voltages | $0.3V_{CC}$ to $0.7V_{CC}$ | | V |

Note: Output Hi-Z is defined as the point where data out is no longer driven.

**Figure 21. AC Measurement I/O Waveform**

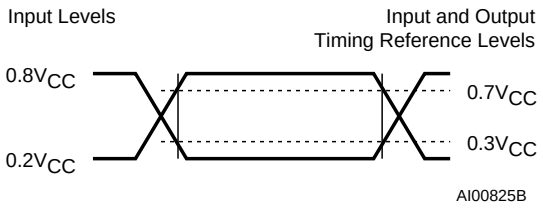



**Table 10. Capacitance**

| Symbol | Parameter | Test Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{OUT}$ | Output Capacitance (Q) | $V_{OUT}$ = 0V | | 8 | pF |
| $C_{IN}$ | Input Capacitance (other pins) | $V_{IN}$ = 0V | | 6 | pF |

Note: Sampled only, not 100% tested, at $T_A$=25°C and a frequency of 20 MHz.

**Table 11. DC Characteristics**

| Symbol | Parameter | Test Condition (in addition to those in Table 8.) | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | | | ± 2 | µA |
| $I_{LO}$ | Output Leakage Current | | | ± 2 | µA |
| $I_{CC1}$ | Standby Current (Standby and Reset modes) | $\overline{S}$ = $V_{CC}$, $V_{IN}$ = $V_{SS}$ or $V_{CC}$ | | 50 | µA |
| $I_{CC2}$ | Deep Power-down Current | $\overline{S}$ = $V_{CC}$, $V_{IN}$ = $V_{SS}$ or $V_{CC}$ | | 10 | µA |
| $I_{CC3}$ | Operating Current (FAST_READ) | C = 0.1$V_{CC}$ / 0.9.$V_{CC}$ at 25 MHz, Q = open | | 6 | mA |
| $I_{CC4}$ | Operating Current (PW) | $\overline{S}$ = $V_{CC}$ | | 15 | mA |
| $I_{CC5}$ | Operating Current (SE) | $\overline{S}$ = $V_{CC}$ | | 15 | mA |
| $V_{IL}$ | Input Low Voltage | | – 0.5 | 0.3$V_{CC}$ | V |
| $V_{IH}$ | Input High Voltage | | 0.7$V_{CC}$ | $V_{CC}$+0.4 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 1.6 mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –100 µA | $V_{CC}$–0.2 | | V |

**Table 12. AC Characteristics**

| Test conditions specified in Table 8. and Table 9. | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Alt.** | **Parameter** | **Min.** | **Typ.** | **Max.** | **Unit** |
| $f_C$ | $f_C$ | Clock Frequency for the following instructions: FAST_READ, PW, PP, PE, SE, DP, RDP, WREN, WRDI, RDSR | D.C. | | 25 | MHz |
| $f_R$ | | Clock Frequency for READ instructions | D.C. | | 20 | MHz |
| $t_{CH}$ [1] | $t_{CLH}$ | Clock High Time | 18 | | | ns |
| $t_{CL}$ [1] | $t_{CLL}$ | Clock Low Time | 18 | | | ns |
| | | Clock Slew Rate [2] (peak to peak) | 0.03 | | | V/ns |
| $t_{SLCH}$ | $t_{CSS}$ | $\overline{S}$ Active Setup Time (relative to C) | 10 | | | ns |
| $t_{CHSL}$ | | $\overline{S}$ Not Active Hold Time (relative to C) | 10 | | | ns |
| $t_{DVCH}$ | $t_{DSU}$ | Data In Setup Time | 5 | | | ns |
| $t_{CHDX}$ | $t_{DH}$ | Data In Hold Time | 5 | | | ns |
| $t_{CHSH}$ | | $\overline{S}$ Active Hold Time (relative to C) | 10 | | | ns |
| $t_{SHCH}$ | | $\overline{S}$ Not Active Setup Time (relative to C) | 10 | | | ns |
| $t_{SHSL}$ | $t_{CSH}$ | $\overline{S}$ Deselect Time | 200 | | | ns |
| $t_{SHQZ}$ [2] | $t_{DIS}$ | Output Disable Time | | | 15 | ns |
| $t_{CLQV}$ | $t_V$ | Clock Low to Output Valid | | | 15 | ns |
| $t_{CLQX}$ | $t_{HO}$ | Output Hold Time | 0 | | | ns |
| $t_{RLRH}$ [2] | $t_{RST}$ | Reset Pulse Width | 10 | | | µs |
| $t_{RHSL}$ | $t_{REC}$ | Reset Recovery Time | | | 3 | µs |
| $t_{SHRH}$ | | Chip should have been deselected before Reset is de-asserted | 10 | | | ns |
| $t_{WHSL}$ | | Write Protect Setup Time | 50 | | | ns |
| $t_{SHWL}$ | | Write Protect Hold Time | 100 | | | ns |
| $t_{DP}$ [2] | | $\overline{S}$ to Deep Power-down | | | 3 | µs |
| $t_{RDP}$ [2] | | $\overline{S}$ High to Standby Mode | | | 30 | µs |
| $t_{PW}$ | | Page Write Cycle Time | | 11 | 25 | ms |
| $t_{PP}$ | | Page Program Cycle Time | | 1.2 | 5 | ms |
| $t_{PE}$ | | Page Erase Cycle Time | | 10 | 20 | ms |
| $t_{SE}$ | | Sector Erase Cycle Time | | 1 | 5 | s |

Note: 1. $t_{CH} + t_{CL}$ must be greater than or equal to $1/f_C$
2. Value guaranteed by characterization, not 100% tested in production.

**Figure 22. Serial Input Timing**

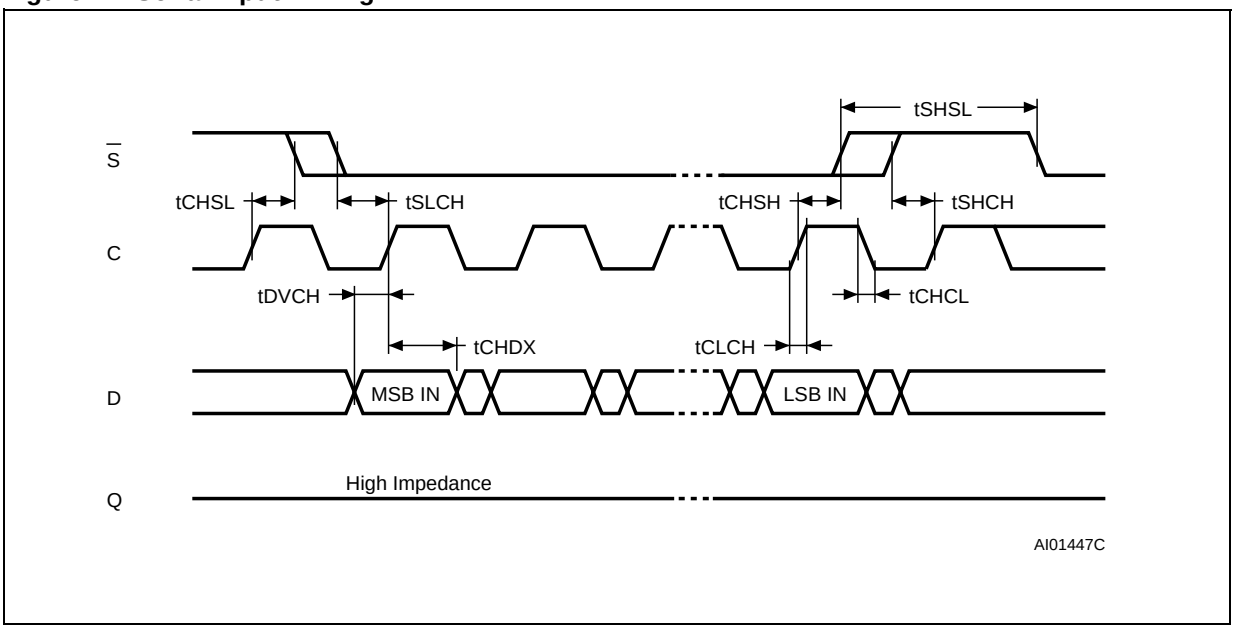



**Figure 23. Write Protect Setup and Hold Timing**

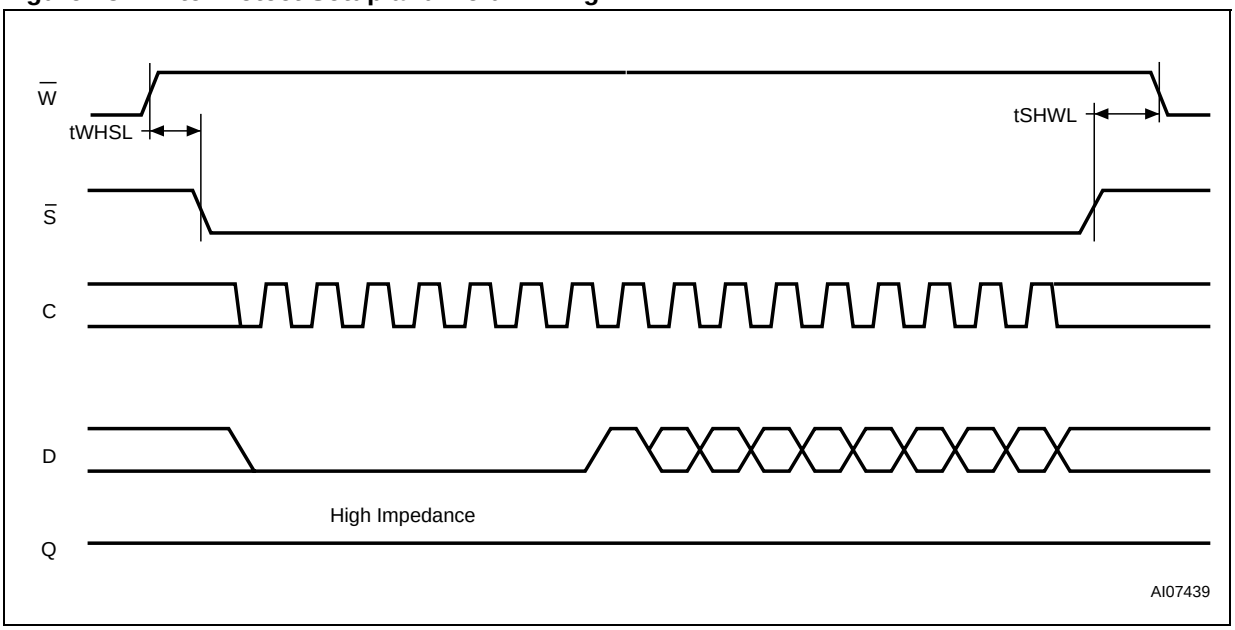


**Figure 24. Output Timing**

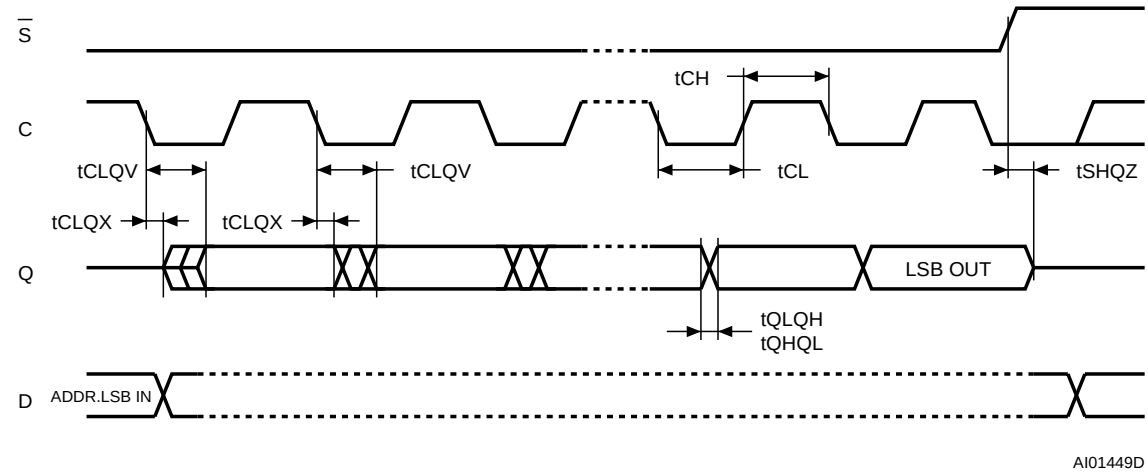
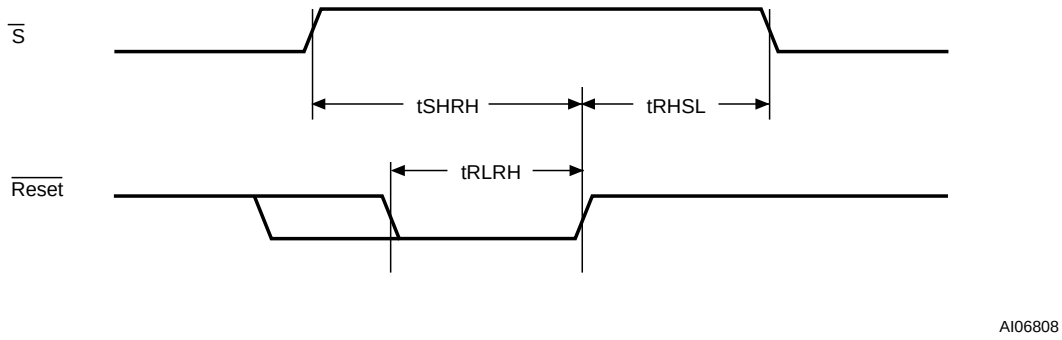
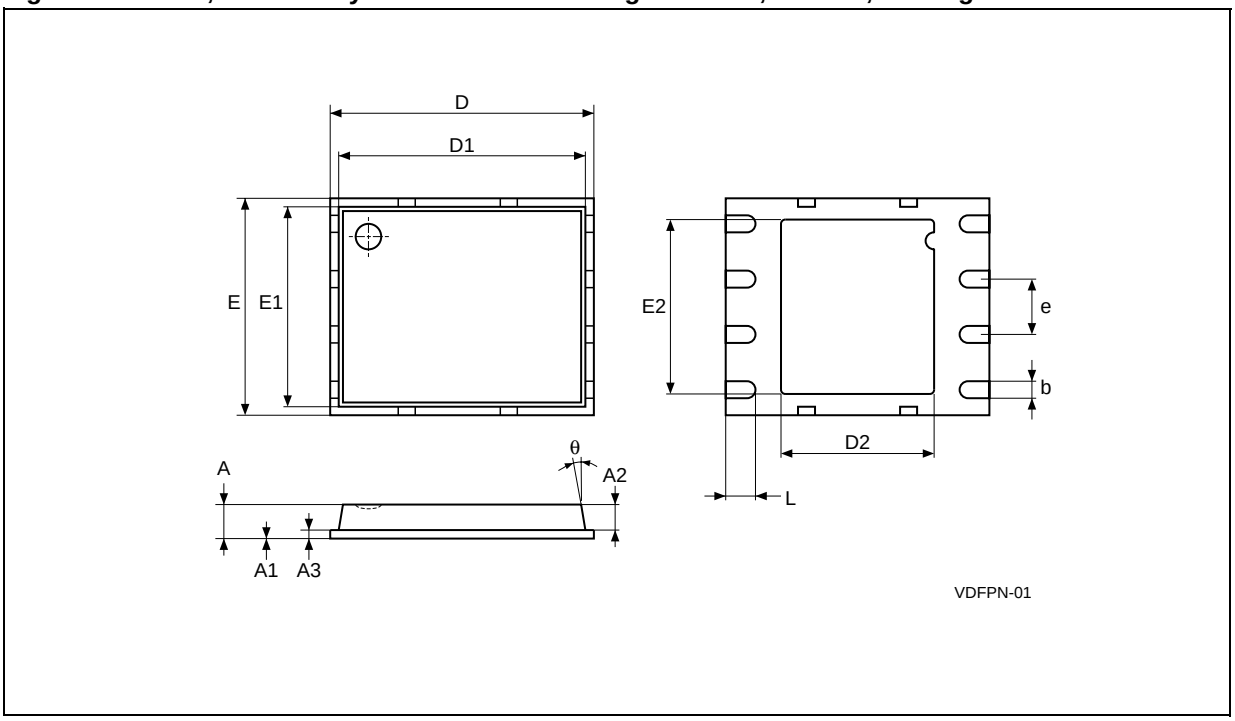



**Figure 25. Reset AC Waveforms**



# PACKAGE MECHANICAL

**Figure 26. MLP8, 8-lead Very thin Dual Flat Package No lead, 6x5mm, Package Outline**

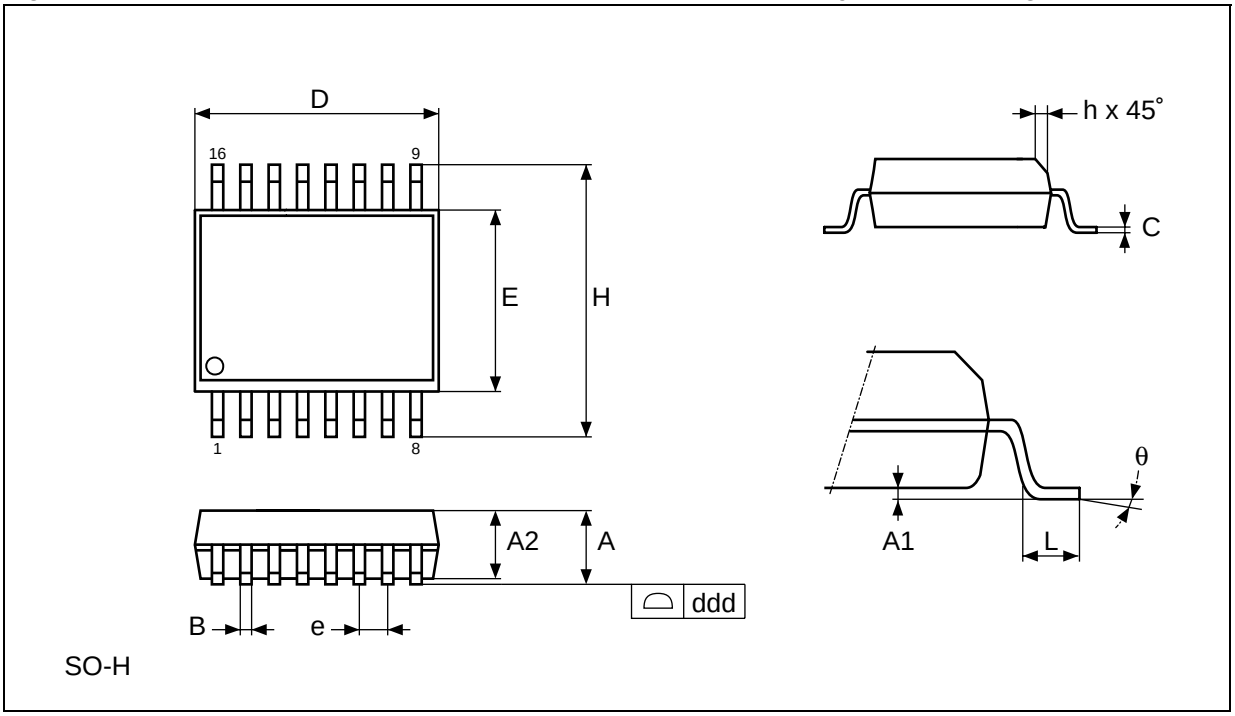



Note: Drawing is not to scale.

**Table 13. MLP8, 8-lead Very thin Dual Flat Package No lead, 6x5mm, Package Mechanical Data**

| Symb. | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | 0.85 | | 1.00 | 0.0335 | | 0.0394 |
| A1 | | 0.00 | 0.05 | | 0.0000 | 0.0020 |
| A2 | 0.65 | | | 0.0256 | | |
| A3 | 0.20 | | | 0.0079 | | |
| b | 0.40 | 0.35 | 0.48 | 0.0157 | 0.0138 | 0.0189 |
| D | 6.00 | | | 0.2362 | | |
| D1 | 5.75 | | | 0.2264 | | |
| D2 | 3.40 | 3.20 | 3.60 | 0.1339 | 0.1260 | 0.1417 |
| E | 5.00 | | | 0.1969 | | |
| E1 | 4.75 | | | 0.1870 | | |
| E2 | 4.00 | 3.80 | 4.20 | 0.1575 | 0.1496 | 0.1654 |
| e | 1.27 | | | 0.0500 | | |
| L | 0.60 | 0.50 | 0.75 | 0.0236 | 0.0197 | 0.0295 |
| θ | | | 12° | | | 12° |

**Figure 27. SO16 wide – 16-lead Plastic Small Outline, 300 mils body width, Package Outline**




Note: Drawing is not to scale.

**Table 14. SO16 wide – 16-lead Plastic Small Outline, 300 mils body width, Mechanical Data**

| Symb. | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | | 2.35 | 2.65 | | 0.093 | 0.104 |
| A1 | | 0.10 | 0.30 | | 0.004 | 0.012 |
| B | | 0.33 | 0.51 | | 0.013 | 0.020 |
| C | | 0.23 | 0.32 | | 0.009 | 0.013 |
| D | | 10.10 | 10.50 | | 0.398 | 0.413 |
| E | | 7.40 | 7.60 | | 0.291 | 0.299 |
| e | 1.27 | – | – | 0.050 | – | – |
| H | | 10.00 | 10.65 | | 0.394 | 0.419 |
| h | | 0.25 | 0.75 | | 0.010 | 0.030 |
| L | | 0.40 | 1.27 | | 0.016 | 0.050 |
| q | | 0 | 8 | | 0 | 8 |
| ddd | | | 0.10 | | | 0.004 |

# PART NUMBERING

**Table 15. Ordering Information Scheme**

Example: M45PE80 – V MP 6 T P

**Device Type**

M45PE = Page-Erasable Serial Flash Memory

**Device Function**

80 = 8Mbit (1M x 8)

**Operating Voltage**

V = $V_{CC}$ = 2.7 to 3.6V

**Package**

MF = SO16 (300 mil width)

MP = VDFPN8 6x5mm (MLP8)

**Device Grade**

6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow

**Option**

blank = Standard Packing

T = Tape & Reel Packing

**Plating Technology**

blank = Standard SnPb plating

P[1] = Lead-Free and RoHS compliant

G[2] = Lead-Free, RoHS compliant, $Sb_2O_3$-free and TBBA-free

Note: 1. Available for SO16 package only
2. Available for MLP package only

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

# REVISION HISTORY

**Table 16. Document Revision History**

| Date | Version | Description of Revision |
|---|---|---|
| 10-Feb-2003 | 1.0 | Document written |
| 02-Apr-2003 | 1.1 | VFQFPN8 (MLP) package added |
| 08-Apr-2003 | 1.2 | Document promoted to Product Preview |
| 05-May-2003 | 1.3 | Document promoted to Preliminary Data |
| 04-Jun-2003 | 1.4 | Description corrected of entering Hardware Protected mode ($\overline{W}$ must be driven, and cannot be left unconnected). Document Revision History for 05-May-2003 corrected. |
| 26-Nov-2003 | 2.0 | $V_{IO}$(min) extended to –0.6V, and $t_{PP}$(typ) improved to 1.2ms. Table of contents, SO16 package, warning about exposed paddle on MLP8, and Pb-free options added. Change of naming for VDFPN8 package. Document promoted to full datasheet |
| 23-Jan-2004 | 3.0 | SO16 pin-out corrected |
| 28-May-2004 | 4.0 | Soldering temperature information clarified for RoHS compliant devices. Device Grade clarified |

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