

M3A & MAH Series

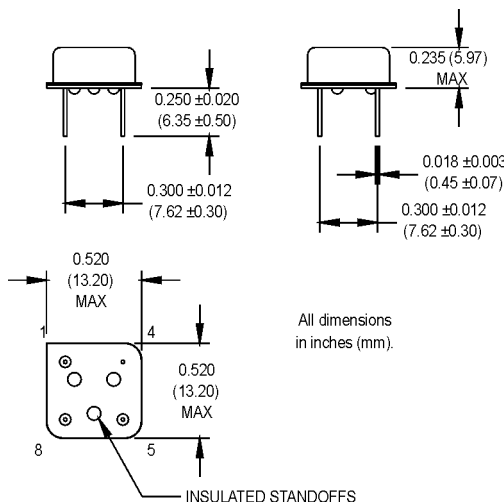
8 pin DIP, 5.0 or 3.3 Volt, ACMOS/TTL, Clock Oscillators



Ordering Information

M3A/MAH	1	3	F	A	D	-R	00.0000 MHz
Product Series M3A = 3.3 Volt MAH = 5.0 Volt							
Temperature Range 1: 0°C to +70°C 2: -40°C to +85°C 6: -20°C to +70°C 7: 0°C to +85°C							
Stability 1: ±1000 ppm 2: ±500 ppm 3: ±100 ppm 4: ±50 ppm 5: ±35 ppm 6: ±25 ppm *8: ±20 ppm							
Output Type F: Fixed T: Tristate							
Symmetry/Logic Compatibility A: 40/60 ACMOS/TTL B: 45/55 TTL C: 45/55 ACMOS							
Package/Lead Configurations A: DIP; Gold Flash Header D: DIP; Nickel Header G: Gull Wing; Nickel Header X: Gull Wing; Gold Flash Header							
RoHS Compliance Blank: non-RoHS compliant part -R: RoHS compliant part							
Frequency (customer specified)							

*Contact factory for availability.



All dimensions
in inches (mm).

Pin Connections

PIN	FUNCTION
1	N/C or Tri-state
4	Circuit/Case Ground
5	Output
8	+Vdd

Electrical Specifications	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition
	Frequency Range	F	30		133	MHz	
	Frequency Stability	ΔF/F	(See Ordering Information)				
	Operating Temperature	TA	(See Ordering Information)				
	Storage Temperature	Ts	-55		+125	°C	
	Input Voltage	Vdd	3.135 4.75	3.3 5.0	3.465 5.25	V V	M3A MAH
	Input Current	Idd		30 70	50 90	mA mA	M3A MAH
	Symmetry (Duty Cycle)		(See Ordering Information)				See Note 1
	Load				50	Ω	See Note 2
	Rise/Fall Time	Tr/Tf					
	M3A			1	2.5	ns	See Note 3
	MAH				2	ns	See Note 3
	Logic “1” Level	Voh	90% Vdd Vdd-0.5			V V	ACMOS Load TTL Load
	Logic “0” Level	Vol			10% Vdd 0.5	V V	ACMOS Load TTL Load
	Cycle to Cycle Jitter			5	15	ps RMS	1 Sigma
Tri-State Function		Input Logic “1” or floating; output active Input Logic “0”; output to high-Z					
Environmental	Mechanical Shock	Per MIL-STD-202, Method 213, Condition C					
	Vibration	Per MIL-STD-202, Method 201 & 204					
	Wave Solder Conditions	See page 147					
	Hermeticity	Per MIL-STD-202, Method 112 (1 x 10 ⁻⁵ atm.cc/s of helium)					
	Solderability	Per EIAJ-STD-002					

1. Symmetry is measured at 1.4 V with TTL load, and at 50% V_{dd} with CMOS load.
2. See load circuit diagram #6.
3. Rise/Fall times are measured between 0.5 V and 2.4 V with TTL load, and between 10% V_{dd} and 90% V_{dd} with CMOS load.

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