To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

EOL announced

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

3820 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 3820 group is the 8-bit microcomputer based on the 740 family core technology.

The 3820 group has the LCD drive control circuit and the serial I/O as additional functions.

The various microcomputers in the 3820 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 3820 group, refer to the section on group expansion.

FEATURES

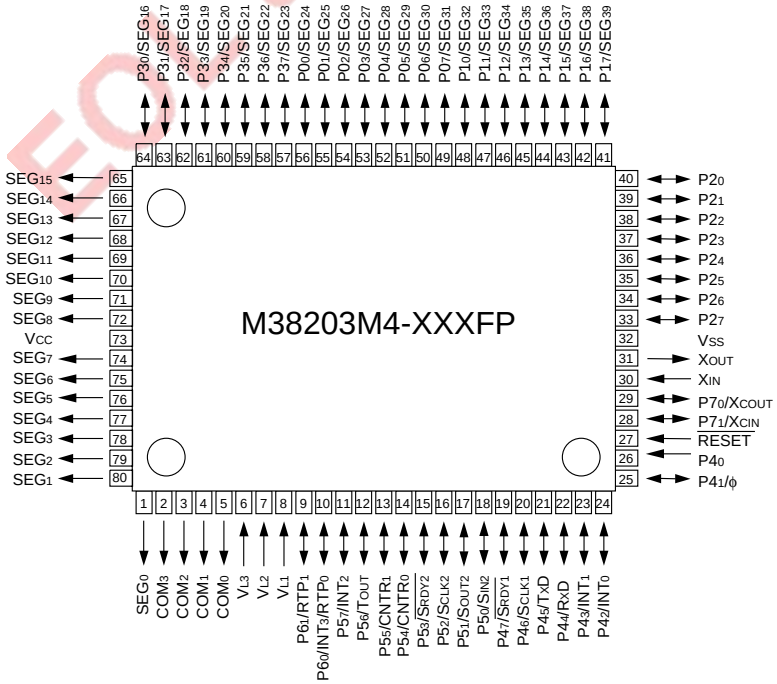
- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.5 µs
  (at 8MHz oscillation frequency)
- Memory size
  ROM ..... 4 K to 32 K bytes
  RAM ..... 192 to 1024 bytes
- Programmable input/output ports 43
- Software pull-up/pull-down resistors (Ports P0-P7 except Port P4$_0$)
- Interrupts ..... 16 sources, 16 vectors
  (includes key input interrupt)
- Timers ..... 8-bit × 3, 16-bit × 2
- Serial I/O1 ..... 8-bit × 1 (UART or Clock-synchronized)
- Serial I/O2 ..... 8-bit × 1 (Clock-synchronized)
- LCD drive control circuit
  Bias 1/2, 1/3
  Duty 1/2, 1/3, 1/4
  Common output 4
  Segment output 40
- 2 Clock generating circuit
  Clock (X_{IN}-X_{OUT}) ..... Internal feedback resistor
  Sub-clock (X_{CIN}-X_{COUT}) ..... Without internal feedback resistor
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Watchdog timer ..... 15-bit × 1
- Power source voltage
  In high-speed mode ..... 4.0 to 5.5 V
  (at 8MHz oscillation frequency and high-speed selected)
  In middle-speed mode ..... 2.5 to 5.5 V
  (at 8MHz oscillation frequency and middle-speed selected)
  In low-speed mode ..... 2.5 to 5.5 V
  (Extended operating temperature version: 3.0 V to 5.5 V)
- Power dissipation
  In high-speed mode ..... 32 mW
  (at 8 MHz oscillation frequency)
  In low-speed mode ..... 45 µW
  (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range ..... – 20 to 85°C
  (Extended operating temperature version: –40 to 85°C)

APPLICATIONS

Household appliances, consumer electronics, etc.

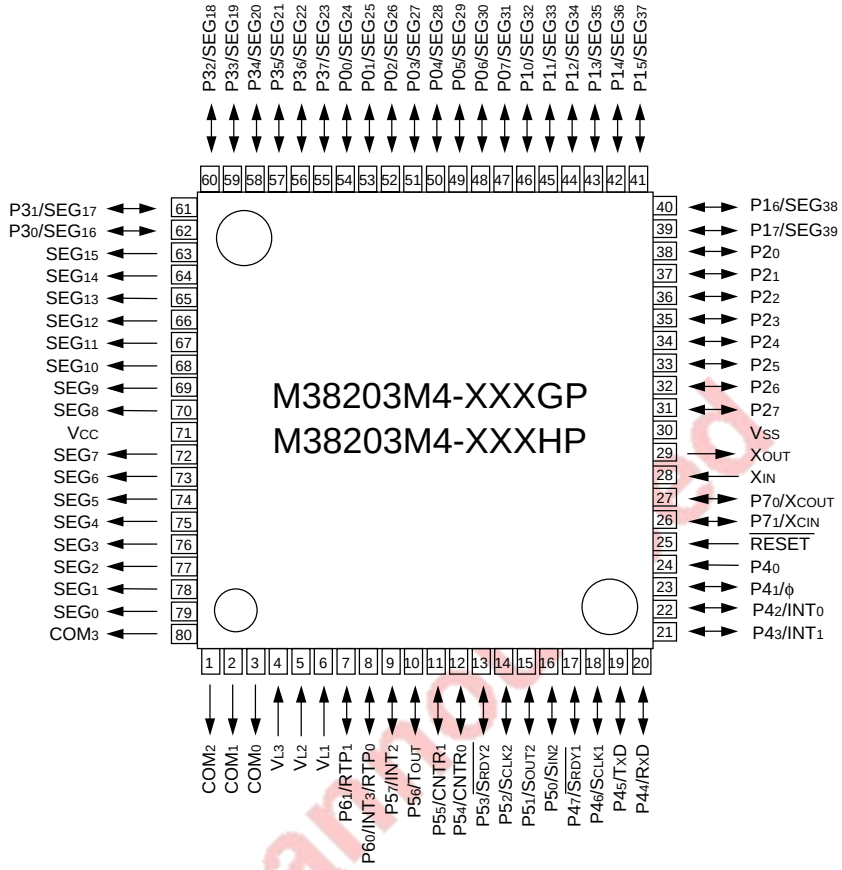
EOL announced

PIN CONFIGURATION (TOP VIEW)



Package type : 80P6N-A
80-pin plastic molded QFP

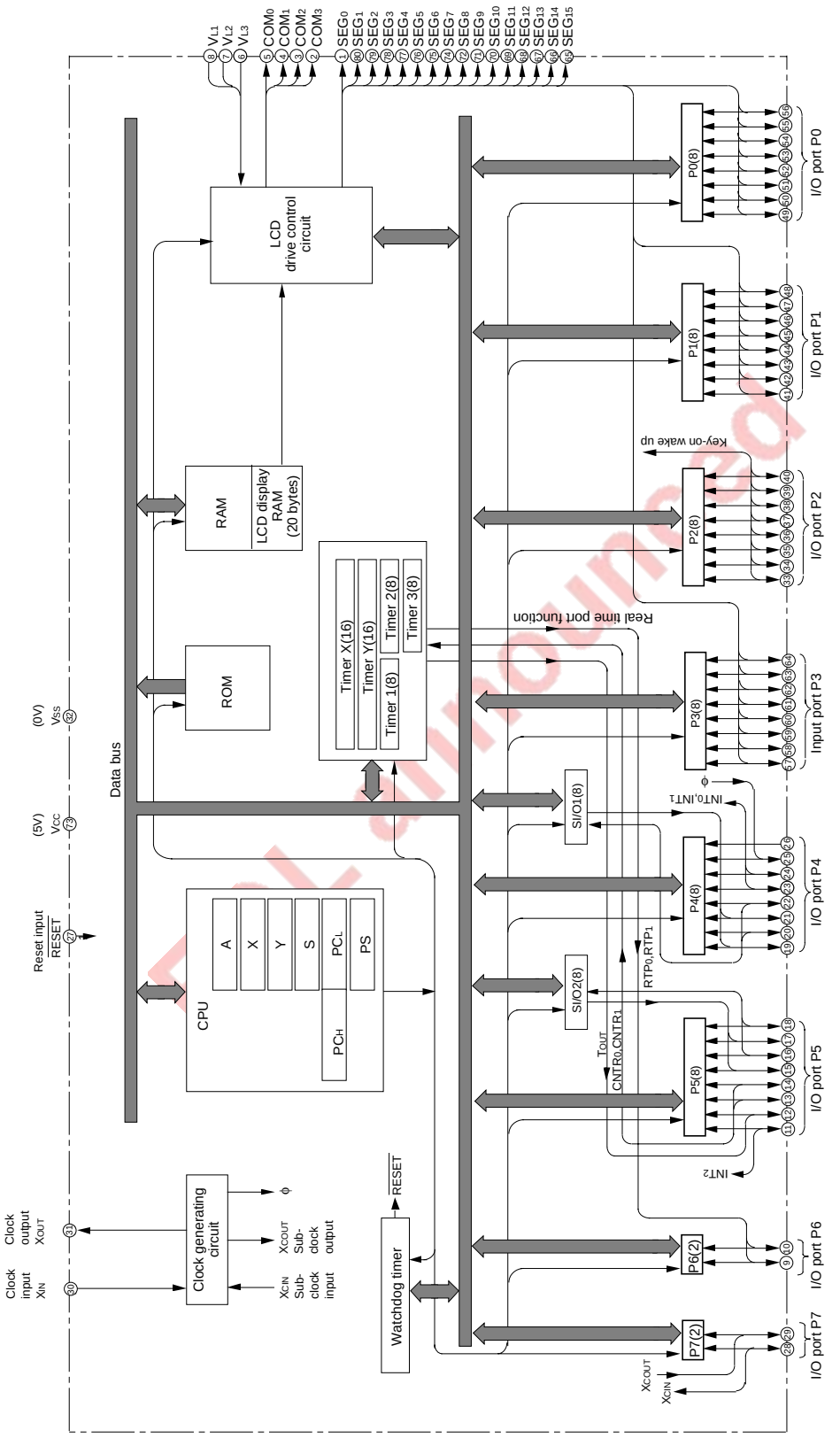
PIN CONFIGURATION (TOP VIEW)



Package type : 80P6S-A/80P6D-A
80-pin plastic-molded QFP

EOL announced

FUNCTIONAL BLOCK DIAGRAM (Package : 80P6N-A)



Not announced

PIN DESCRIPTION

Pin	Name	Function	Function except a port function
V_{CC}	Power source	• Apply voltage of 2.5 V to 5.5 V to V_{CC}, and 0 V to V_{SS}. (Extended operating temperature version : 3.0 V to 5.5 V)	
V_{SS}			
$\overline{RESET}$	Reset input	• Reset input pin for active "L"	
X_{IN}	Clock input	• Input and output pins for the main clock generating circuit. • Feedback resistor is built in between X_{IN} pin and X_{OUT} pin. • Connect a ceramic resonator or a quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. • If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open. • This clock is used as the oscillating source of system clock.	
X_{OUT}	Clock output		
V_{L1} – V_{L3}	LCD power source	• Input $0 \le V_{L1} \le V_{L2} \le V_{L3} \le V_{CC}$ voltage • Input 0 – V_{L3} voltage to LCD	
COM_0 – COM_3	Common output	• LCD common output pins • COM_2 and COM_3 are not used at 1/2 duty ratio. • COM_3 is not used at 1/3 duty ratio.	
SEG_0 – SEG_{15}	Segment output	• LCD segment output pins	
$P0_0/SEG_{24}$ – $P0_7/SEG_{31}$	I/O port P0	• 8-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each port to be individually programmed as either input or output. • Pull-down control is enabled.	• LCD segment pins
$P1_0/SEG_{32}$ – $P1_7/SEG_{39}$	I/O port P1	• 8-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each port to be individually programmed as either input or output. • Pull-down control is enabled.	
$P2_0$ – $P2_7$	I/O port P2	• 8-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• Key input (key-on wake up) interrupt input pins
$P3_0/SEG_{16}$ – $P3_7/SEG_{23}$	Input port P3	• 8-bit Input port • CMOS compatible input level • Pull-down control is enabled.	• LCD segment pins
$P4_0$	Input port P4	• 1-bit input pin • CMOS compatible input level	
$P4_1/\phi$	I/O port P4	• 7-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• ϕ clock output pin
$P4_2/INT_0$, $P4_3/INT_1$			• Interrupt input pins
$P4_4/R_XD$, $P4_5/T_XD$, $P4_6/S_{CLK1}$, $P4_7/\overline{S_{RDY1}}$			• Serial I/O1 function pins

Not announced

PIN DESCRIPTION

Pin	Name	Function	Function except a port function
P50/SIN2, P51/SOUT2, P52/SCLK2, P53/SRDY2	I/O port P5	• 8-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• Serial I/O2 function pins
P54/CNTR0, P55/CNTR1			• Timer function pins
P56/TOUT			• Timer output pin
P57/INT2			• Interrupt input pin
P60/INT3/RTP0	I/O port P6	• 2-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• Interrupt input pins(P60)
P61/RTP1			• Real time port function pin
P70/XCOUT, P71/XCIN	I/O port P7	• 2-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• Sub-clock generating circuit input pins (Connect a resonator. External clock cannot be used.)

EOL announced

PART NUMBERING

Product M3820 **3 M 4 - XXX FP**

Package type
FP : 80P6N-A package
GP : 80P6S-A package
HP : 80P6D-A package
FS : 80D0 package

ROM number
Omitted in some types.

Normally, using hyphen
When electrical characteristic, or division of quality identification code using alphanumeric character
– : standard
D : Extended operating temperature version

ROM/PROM size
1 : 4096 bytes
2 : 8192 bytes
3 : 12288 bytes
4 : 16384 bytes
5 : 20480 bytes
6 : 24576 bytes
7 : 28672 bytes
8 : 32768 bytes

The first 128 bytes and the last 2 bytes of ROM are reserved areas ; they cannot be used.

Memory type
M : Mask ROM version
E : EPROM or One Time PROM version

RAM size
0 : 192 bytes
1 : 256 bytes
2 : 384 bytes
3 : 512 bytes
4 : 640 bytes
5 : 768 bytes
6 : 896 bytes
7 : 1024 bytes

EOL announced

GROUP EXPANSION

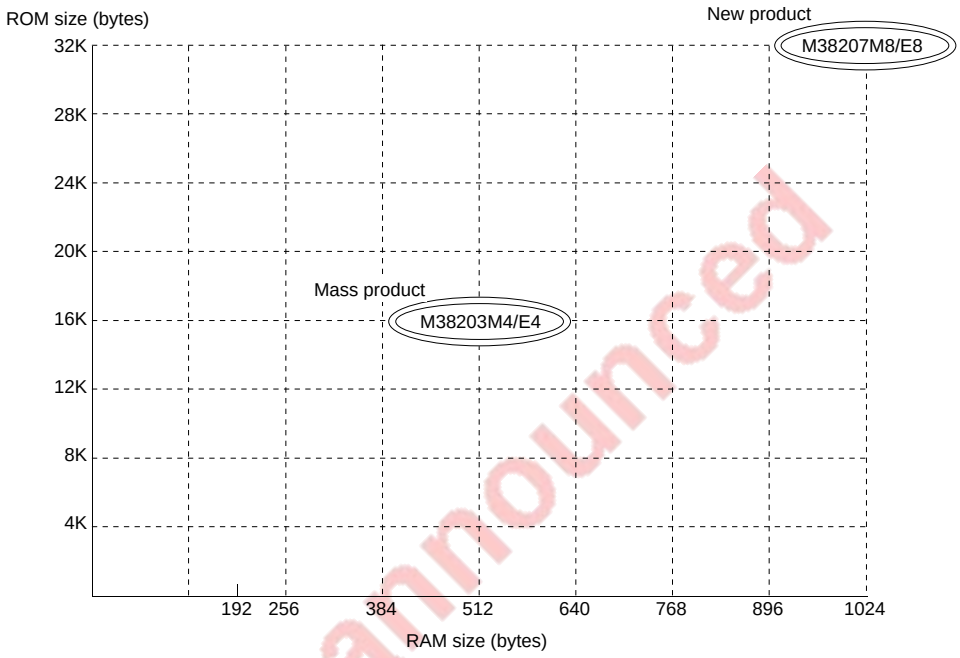
Mitsubishi plans to expand the 3820 group as follows:

(1) Support for mask ROM, One Time PROM, and EPROM versions

(2) ROM/PROM size ..... 8 K to 32 K bytes
RAM size ..... 512 to 1024 bytes

(3) Packages
80P6N-A ..... 0.8 mm-pitch plastic molded QFP
80P6S-A ..... 0.65 mm-pitch plastic molded QFP
80P6D-A ..... 0.5 mm-pitch plastic molded QFP
80D0 ..... 0.8 mm-pitch ceramic LCC (EPROM version)

Memory Expansion Plan



EOL announced

Currently supported products are listed below. **As of May 1996**

Product	(P) ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38203M4-XXXFP	16384 (16254)	512	80P6N-A	Mask ROM version
M38203E4-XXXFP				One Time PROM version
M38203E4FP				One Time PROM version (blank)
M38203M4-XXXGP			80P6S-A	Mask ROM version
M38203E4-XXXGP				One Time PROM version
M38203E4GP				One Time PROM version (blank)
M38203M4-XXXHP			80P6D-A	Mask ROM version
M38203E4-XXXHP				One Time PROM version
M38203E4HP				One Time PROM version (blank)
M38203E4FS			80D0	EPROM version
M38207M8-XXXFP	32768 (32638)	1024	80P6N-A	Mask ROM version
M38207E8-XXXFP				One Time PROM version
M38207E8FP				One Time PROM version (blank)
M38207M8-XXXGP			80P6S-A	Mask ROM version
M38207E8-XXXGP				One Time PROM version
M38207E8GP				One Time PROM version (blank)
M38207M8-XXXHP			80P6D-A	Mask ROM version
M38207E8-XXXHP				One Time PROM version
M38207E8HP				One Time PROM version (blank)
M38207E8FS			80D0	EPROM version

GROUP EXPANSION
(EXTENDED OPERATING TEMPERATURE VERSION)

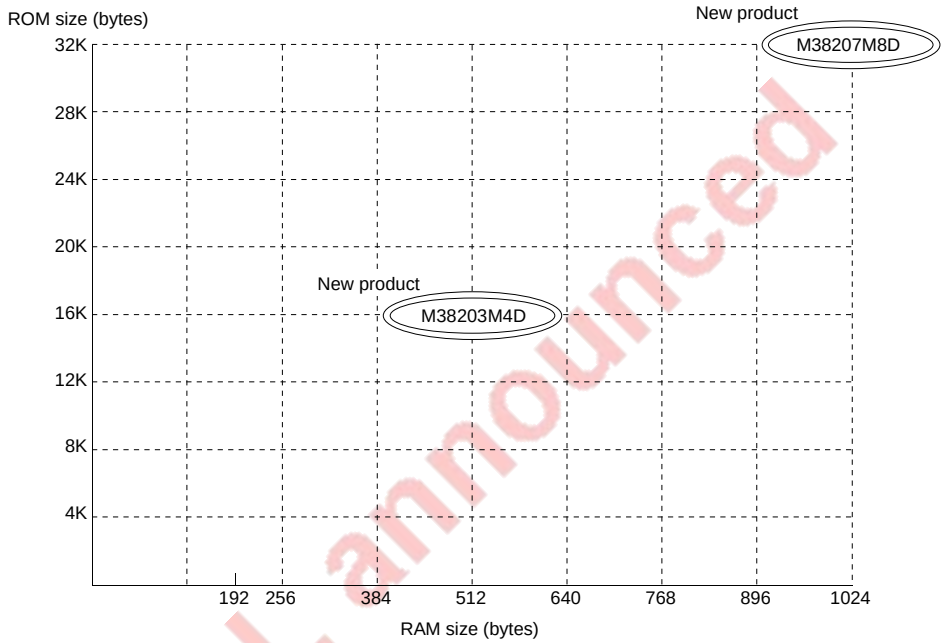
Mitsubishi plans to expand the 3820 group (extended operating temperature version) as follows:

(1) Support for mask ROM, One Time PROM, and EPROM versions

(2) ROM size ..... 16 K to 32 K bytes
RAM size ..... 512 to 1024 bytes

(3) Packages
80P6N-A ..... 0.8 mm-pitch plastic molded QFP
80P6S-A ..... 0.65 mm-pitch plastic molded QFP

Memory Expansion Plan



EOL announced

Currently supported products are listed below. **As of May 1996**

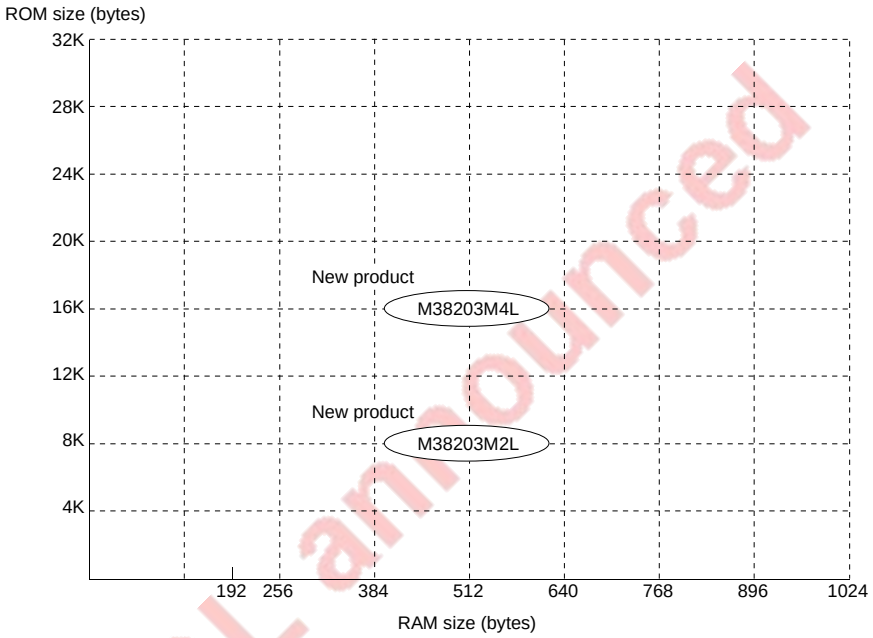
Product	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38203M4DXXXFP	16384(16254)	512	80P6N-A	Mask ROM version
M38207M8DXXXFP	32768(32638)	1024	80P6N-A	Mask ROM version
M38207M8DXXXGP	32768(32638)	1024	80P6S-A	Mask ROM version

GROUP EXPANSION (LOW POWER SOURCE VOLTAGE VERSION)

Mitsubishi plans to expand the 3820 group (low power source voltage version) as follows:

(1) Support for mask ROM version
(2) ROM size ..... 8 K to 32 K bytes
RAM size ..... 512 bytes
(3) Packages
80P6N-A ..... 0.8 mm-pitch plastic molded QFP
80P6S-A ..... 0.65 mm-pitch plastic molded QFP
80P6D-A ..... 0.5 mm-pitch plastic molded QFP

Memory Expansion Plan



EOL announced

Currently supported products are listed below. **As of May 1996**

Product	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38203M2LXXXFP	8192 (8062)	512	80P6N-A	Mask ROM version
M38203M2LXXXGP			80P6S-A	Mask ROM version
M38203M2LXXXHP			80P6D-A	Mask ROM version
M38203M4LXXXFP	16384 (16254)		80P6N-A	Mask ROM version
M38203M4LXXXGP			80P6S-A	Mask ROM version
M38203M4LXXXHP			80P6D-A	Mask ROM version

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The 3820 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST and SLW instruction cannot be used.

The STP, WIT, MUL, and DIV instruction can be used.

CPU Mode Register

The CPU mode register is allocated at address $003B_{16}$.

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

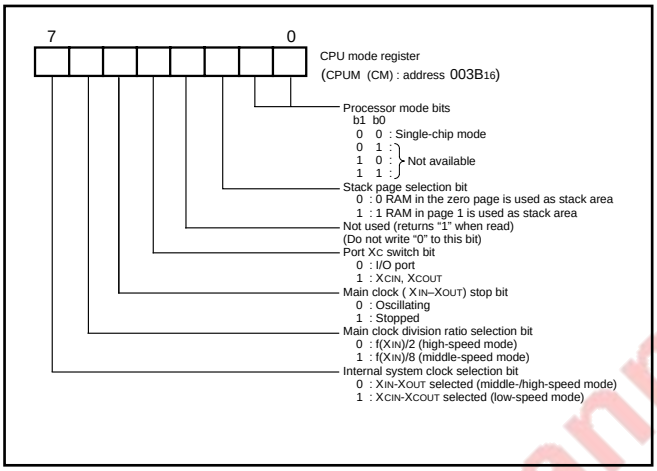


Fig. 1 Structure of CPU mode register

EOL announced

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

EOL announced

RAM area

RAM size (bytes)	Address XXXX16
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$

ROM area

ROM size (bytes)	Address YYYY16	Address ZZZZ16
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}

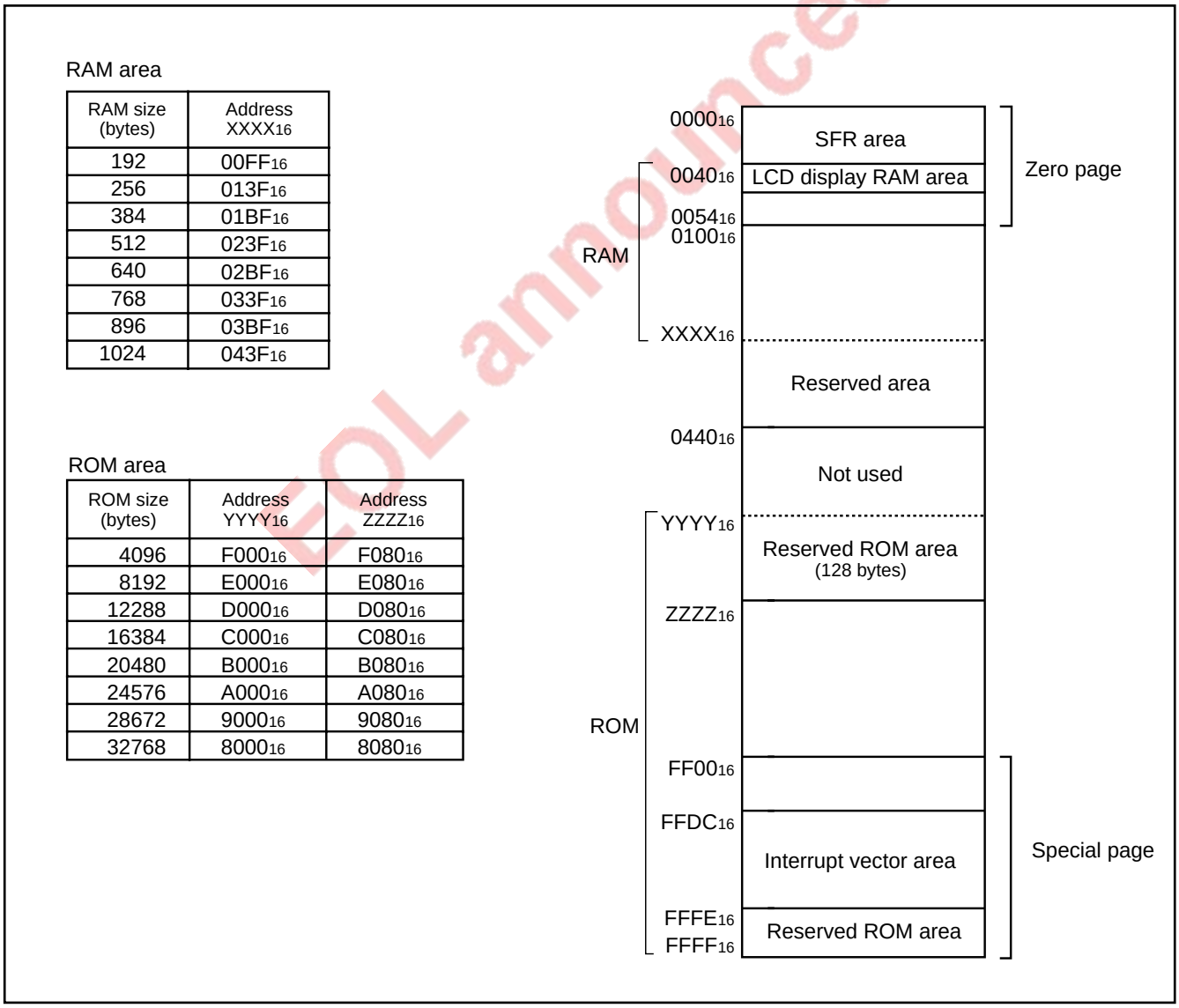


Fig. 2 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	Timer X (low-order) (TXL)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Timer X (high-order) (TXH)
0002_{16}	Port P1 (P1)	0022_{16}	Timer Y (low-order) (TYL)
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Timer Y (high-order) (TYH)
0004_{16}	Port P2 (P2)	0024_{16}	Timer 1 (T1)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer 2 (T2)
0006_{16}	Port P3 (P3)	0026_{16}	Timer 3 (T3)
0007_{16}		0027_{16}	Timer X mode register (TXM)
0008_{16}	Port P4 (P4)	0028_{16}	Timer Y mode register (TYM)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	Timer 123 mode register (T123M)
$000A_{16}$	Port P5 (P5)	$002A_{16}$	ϕ output control register (CKOUT)
$000B_{16}$	Port P5 direction register (P5D)	$002B_{16}$	
$000C_{16}$	Port P6 (P6)	$002C_{16}$	
$000D_{16}$	Port P6 direction register (P6D)	$002D_{16}$	
$000E_{16}$	Port P7 (P7)	$002E_{16}$	
$000F_{16}$	Port P7 direction register (P7D)	$002F_{16}$	
0010_{16}		0030_{16}	
0011_{16}		0031_{16}	
0012_{16}		0032_{16}	
0013_{16}		0033_{16}	
0014_{16}		0034_{16}	
0015_{16}		0035_{16}	
0016_{16}	PULL register A (PULLA)	0036_{16}	
0017_{16}	PULL register B (PULLB)	0037_{16}	Watchdog timer control register (WDTCON)
0018_{16}	Transmit/Receive buffer register (TB/RB)	0038_{16}	Segment output enable register (SEG)
0019_{16}	Serial I/O1 status register (SIO1STS)	0039_{16}	LCD mode register (LM)
$001A_{16}$	Serial I/O1 control register (SIO1CON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1(IREQ1)
$001D_{16}$	Serial I/O2 control register (SIO2CON)	$003D_{16}$	Interrupt request register 2(IREQ2)
$001E_{16}$		$003E_{16}$	Interrupt control register 1(ICON1)
$001F_{16}$	Serial I/O2 register (SIO2)	$003F_{16}$	Interrupt control register 2(ICON2)

Fig.3 Memory map of special function register (SFR)

EOL

I/O PORTS

Direction Registers (ports P2, P41–P47, and P5–P7)

The 3820 group has 43 programmable I/O pins arranged in seven I/O ports (ports P0–P2 and P4–P7). The I/O ports P2, P41–P47, and P5–P7 have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input port or output port.

When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Direction Registers (ports P0 and P1)

Ports P0 and P1 have direction registers which determine the input /output direction of each individual port.

Each port in a direction register corresponds to one port, each port can be set to be input or output.

When “0” is written to the bit 0 of a direction register, that port becomes an input port. When “1” is written to that port, that port becomes an output port.

Bits 1 to 7 of ports P0 and P1 direction registers are not used.

Ports P3 and P40

These ports are only for input.

Pull-up/Pull-down Control

By setting the PULL register A (address 0016$_{16}$) or the PULL register B (address 0017$_{16}$), ports except for port P40 can control either pull-down or pull-up (pins that are shared with the segment output pins for LCD are pull-down; all other pins are pull-up) with a program.

However, the contents of PULL register A and PULL register B do not affect ports programmed as the output ports.

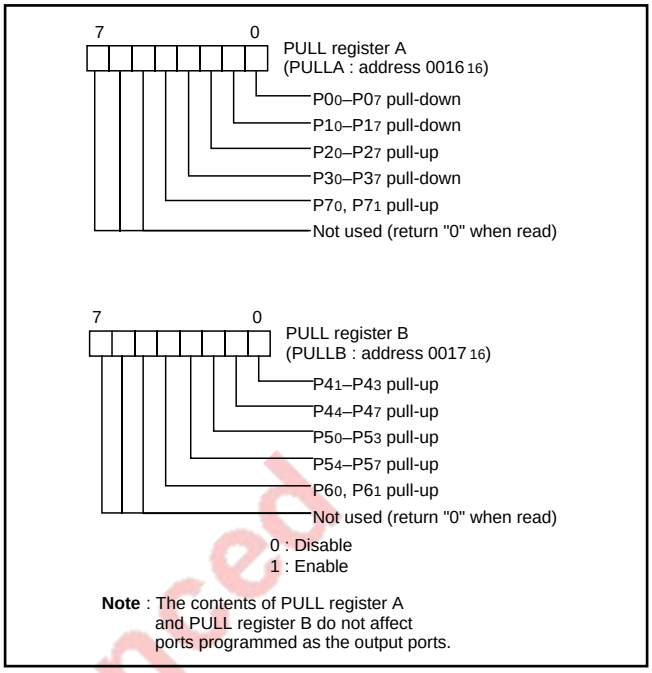


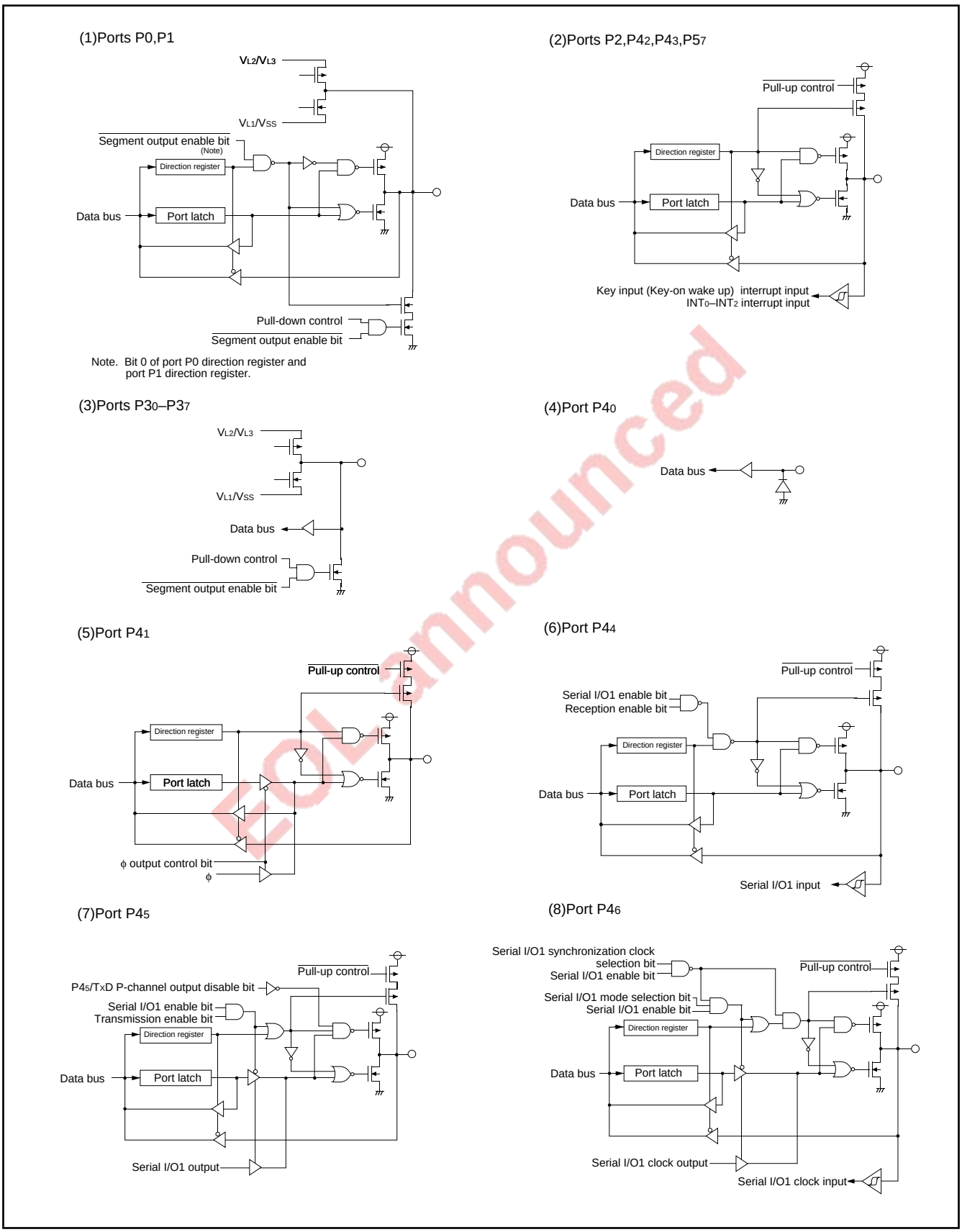
Fig. 4 Structure of PULL register A and PULL register B

EOL announced

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P00/SEG24–P07/SEG31	Port P0	Input/output, individual ports	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	(1)
P10/SEG32–P17/SEG39	Port P1	Input/output, individual ports	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	
P20 – P27	Port P2	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Key input(Key-on wake up) interrupt input	PULL register A Interrupt control register 2	(2)
P30/SEG16–P37/SEG23	Port P3	Input	CMOS compatible input level	LCD segment output	PULL register A Segment output enable register	(3)
P40	Port P4	Input	CMOS compatible input level			(4)
P41/ϕ		Input/output, individual bits	CMOS compatible input level CMOS 3-state output	ϕ clock output	PULL register B ϕ output control register	(5)
P42/INT0, P43/INT1				External interrupt input	PULL register B Interrupt edge selection register	(2)
P44/RxD				Serial I/O1 function I/O	PULL register B	(6)
P45/TxD					Serial I/O1 control register	(7)
P46/SCLK1					Serial I/O1 status register	(8)
P47/SRDY1					UART control register	(9)
P50/SIN2	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O2 function I/O	PULL register B Serial I/O2 control register	(10)
P51/SOUT2						(11)
P52/SCLK2						(12)
P53/SRDY2						(13)
P54/CNTR0				Timer I/O	PULL register B Timer X mode register	(14)
P55/CNTR1				Timer I/O	PULL register B Timer Y mode register	(10)
P56/TOUT				Timer output	PULL register B Timer 123 mode register	(15)
P57/INT2				External interrupt input	PULL register B Interrupt edge selection register	(2)
P60/INT3/RTP0	Port P6	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	External interrupt input Real time port function output	PULL register B Timer X mode register Interrupt edge selection register	(16)
P61/RTP1				Real time port function output	PULL register B Timer X mode register	
P70/XCOUT	Port P7	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Sub-clock generating circuit I/O	PULL register A CPU mode register	(17)
P71/XCIN						(18)
COM0-COM3	Common	output	LCD common output		LCD mode register	(19)
SEG0-SEG15	Segment	output	LCD segment output			(20)

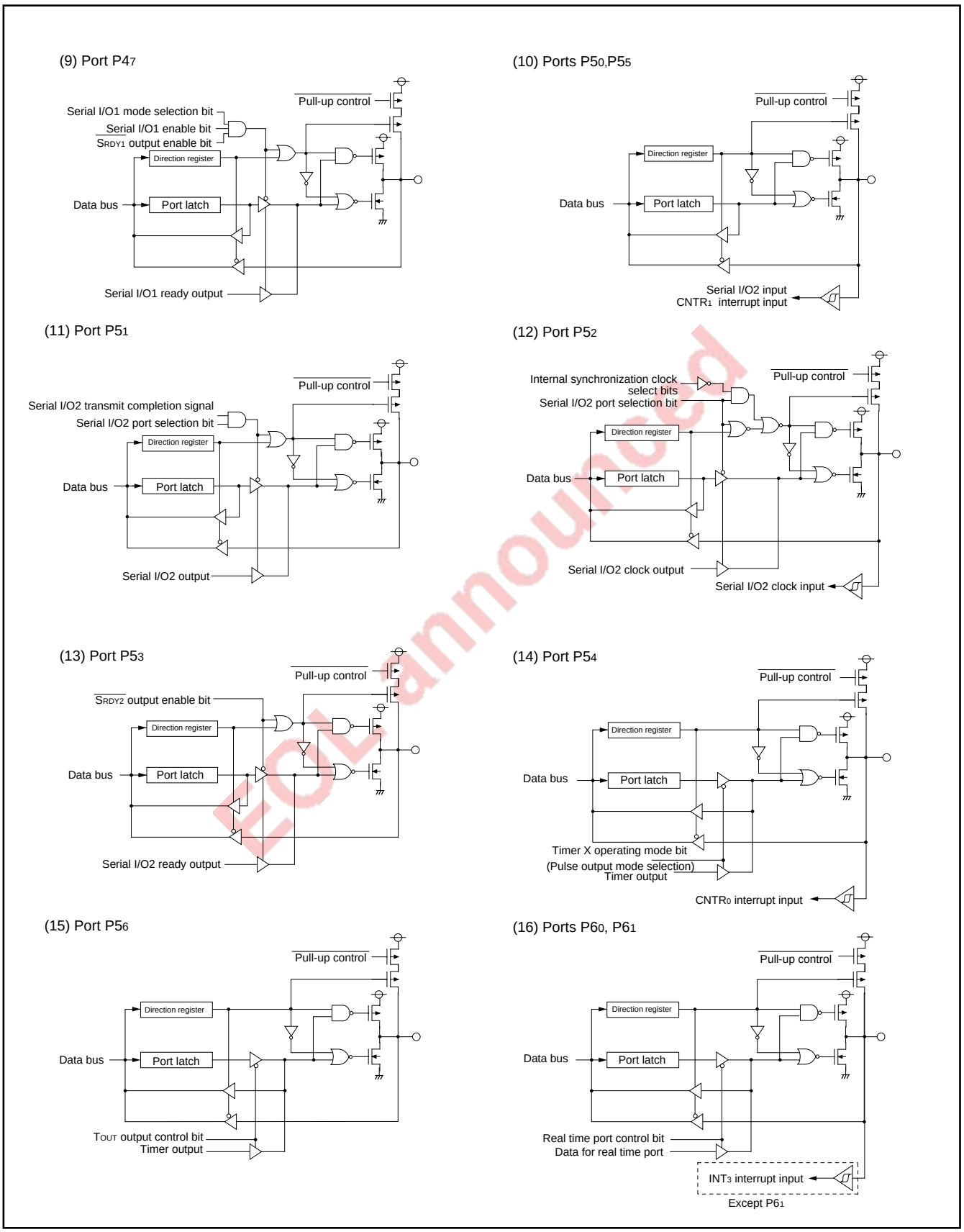
Note : Make sure that the input level at each pin is either 0 V or VCC during execution of the STP instruction.
When an input level is at an intermediate potential, a current will flow from VCC to VSS through the input-stage gate.

EOL announced



EOL announced

Fig. 5 Port block diagram (1)



EOL announced

Fig. 6 Port block diagram (2)

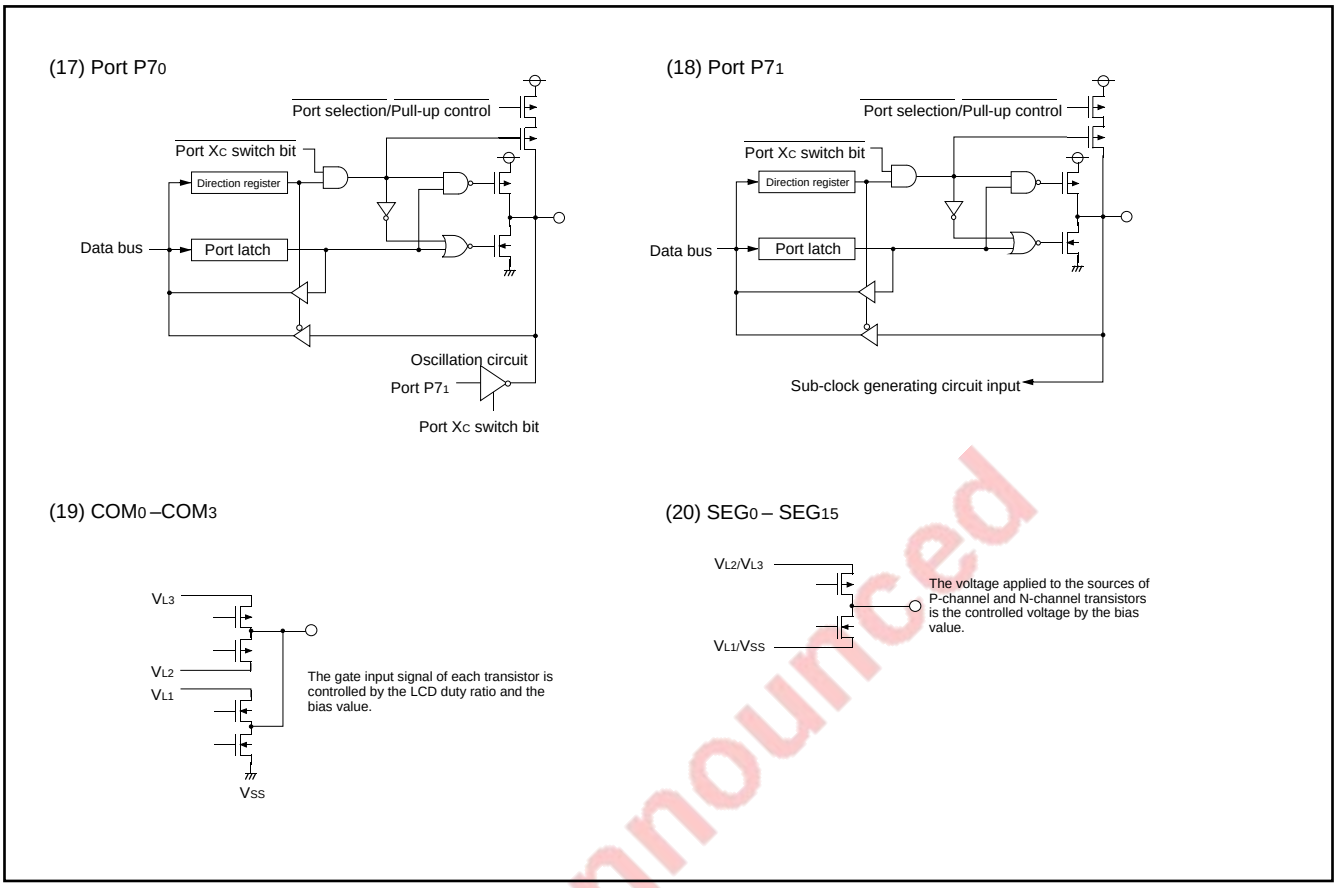


Fig. 7 Port block diagram (3)

EOL announced

INTERRUPTS

Interrupts occur by sixteen sources: seven external, eight internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.

Interrupt Operation

When an interrupt is received, the contents of the program counter and processor status register are automatically stored into the stack. The interrupt disable flag is set to inhibit other interrupts from interfering.The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

Notes on Use

When the active edge of an external interrupt (INT_0–INT_3, $CNTR_0$, or $CNTR_1$) is changed, the corresponding interrupt request bit may also be set. Therefore, please take following sequence;

(1) Disable the external interrupt which is selected.
(2) Change the active edge selection.
(3) Clear the interrupt request bit which is selected to "0".
(4) Enable the external interrupt which is selected.

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Table 1. Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Serial I/O1 receive	4	$FFF7_{16}$	$FFF6_{16}$	At completion of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O1 transmit	5	$FFF5_{16}$	$FFF4_{16}$	At completion of serial I/O1 transmit shift or when transmit buffer register is empty	Valid when serial I/O1 is selected
Timer X	6	$FFF3_{16}$	$FFF2_{16}$	At timer X underflow	
Timer Y	7	$FFF1_{16}$	$FFF0_{16}$	At timer Y underflow	
Timer 2	8	$FFEF_{16}$	$FFEE_{16}$	At timer 2 underflow	
Timer 3	9	$FFED_{16}$	$FFEC_{16}$	At timer 3 underflow	
$CNTR_0$	10	$FFEB_{16}$	$FFEA_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
$CNTR_1$	11	$FFE9_{16}$	$FFE8_{16}$	At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
Timer 1	12	$FFE7_{16}$	$FFE6_{16}$	At timer 1 underflow	
INT_2	13	$FFE5_{16}$	$FFE4_{16}$	At detection of either rising or falling edge of INT_2 input	External interrupt (active edge selectable)
INT_3	14	$FFE3_{16}$	$FFE2_{16}$	At detection of either rising or falling edge of INT_3 input	External interrupt (active edge selectable)
Key input (Key-on wake up)	15	$FFE1_{16}$	$FFE0_{16}$	At falling of conjunction of input level for port P2 (at input mode)	External interrupt (valid when an "L" level is applied)
Serial I/O2	16	$FFDF_{16}$	$FFDE_{16}$	At completion of serial I/O2 data transmission or reception	Valid when serial I/O2 is selected
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Notes **1**: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

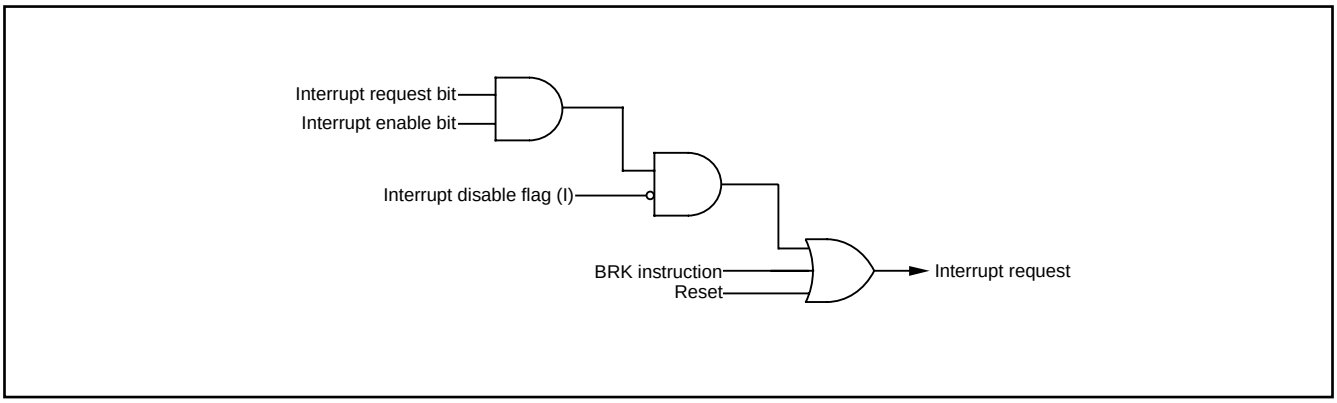


Fig. 8 Interrupt control

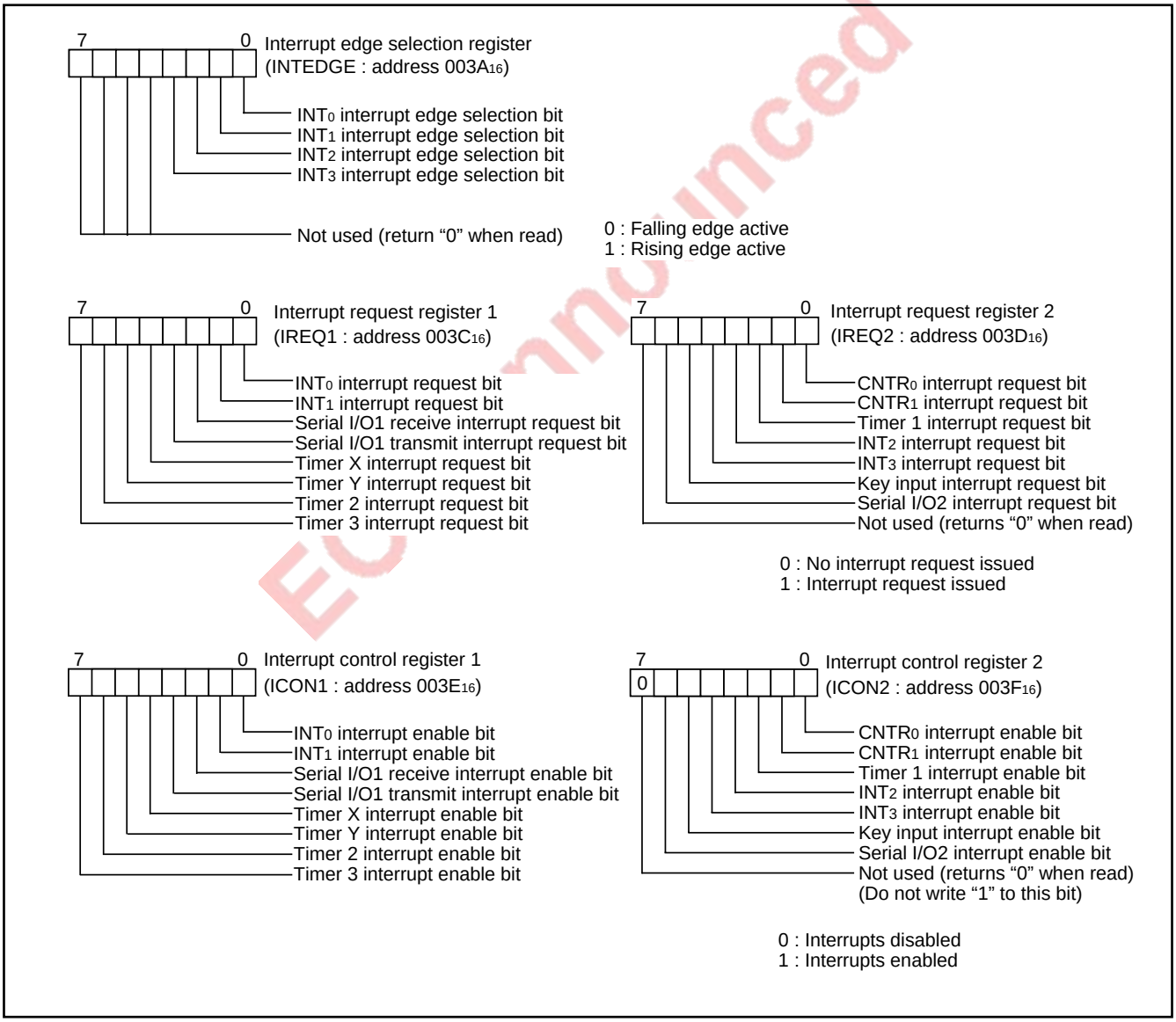
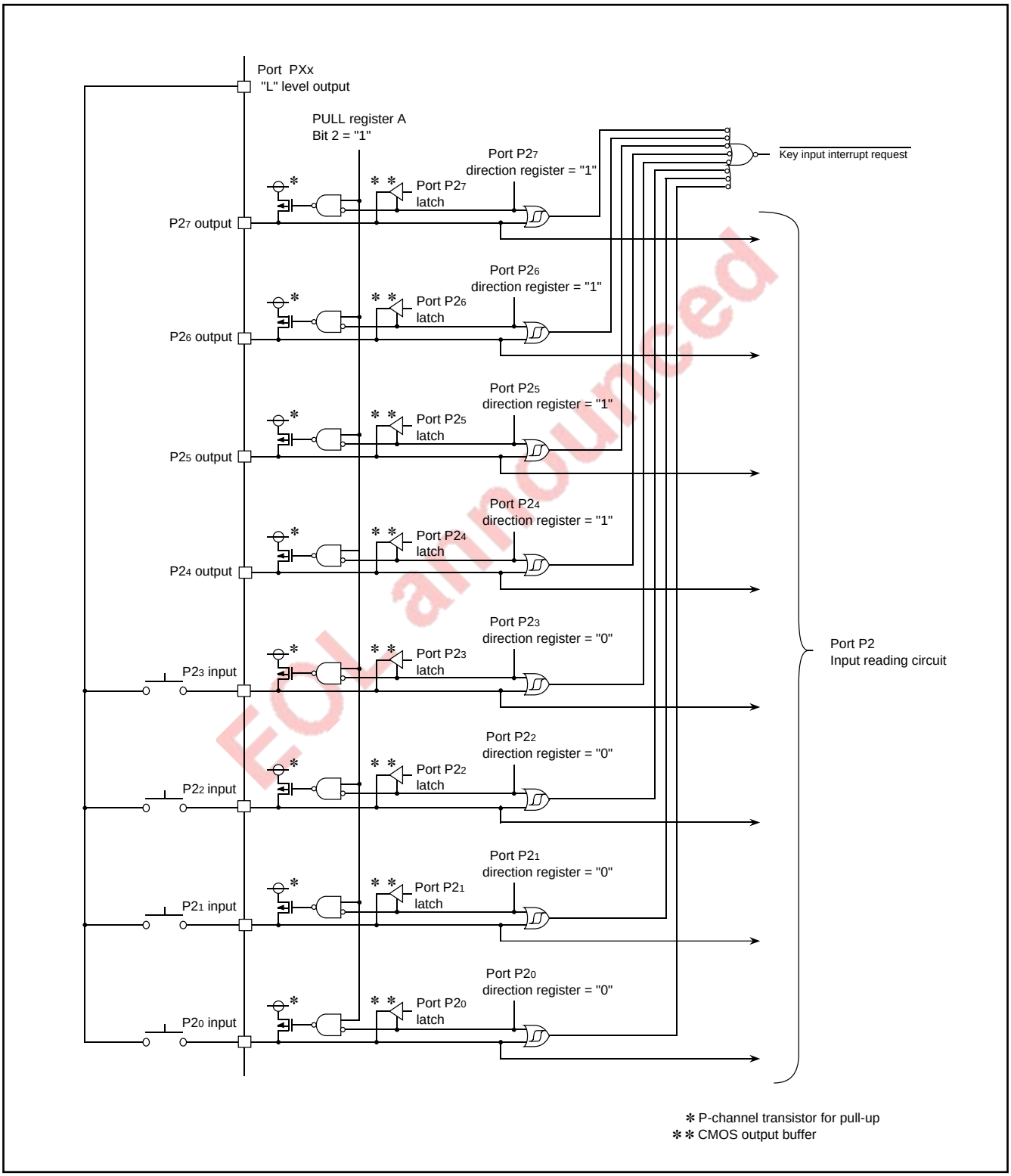


Fig. 9 Structure of interrupt-related registers

Key Input Interrupt (Key-on Wake Up)

A key input interrupt request is generated by applying “L” level to any pin of port P3 that have been set to input mode. In other words, it is generated when AND of input level goes from “1” to “0”.

An example of using a key input interrupt is shown in Figure 9, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P20–P23.



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Fig. 10 Connection example when using key input interrupt and port P2 block diagram

TIMERS

The 3820 group has five timers: timer X, timer Y, timer 1, timer 2, and timer 3. Timer X and timer Y are 16-bit timers, and timer 1, timer 2, and timer 3 are 8-bit timers.

All timers are down count timers. When the timer reaches "00$_{16}$", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

Read and write operation on 16-bit timer must be performed for both high and low-order bytes. When reading a 16-bit timer, read the high-order byte first. When writing to a 16-bit timer, write the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during the write operation, or when writing during the read operation.

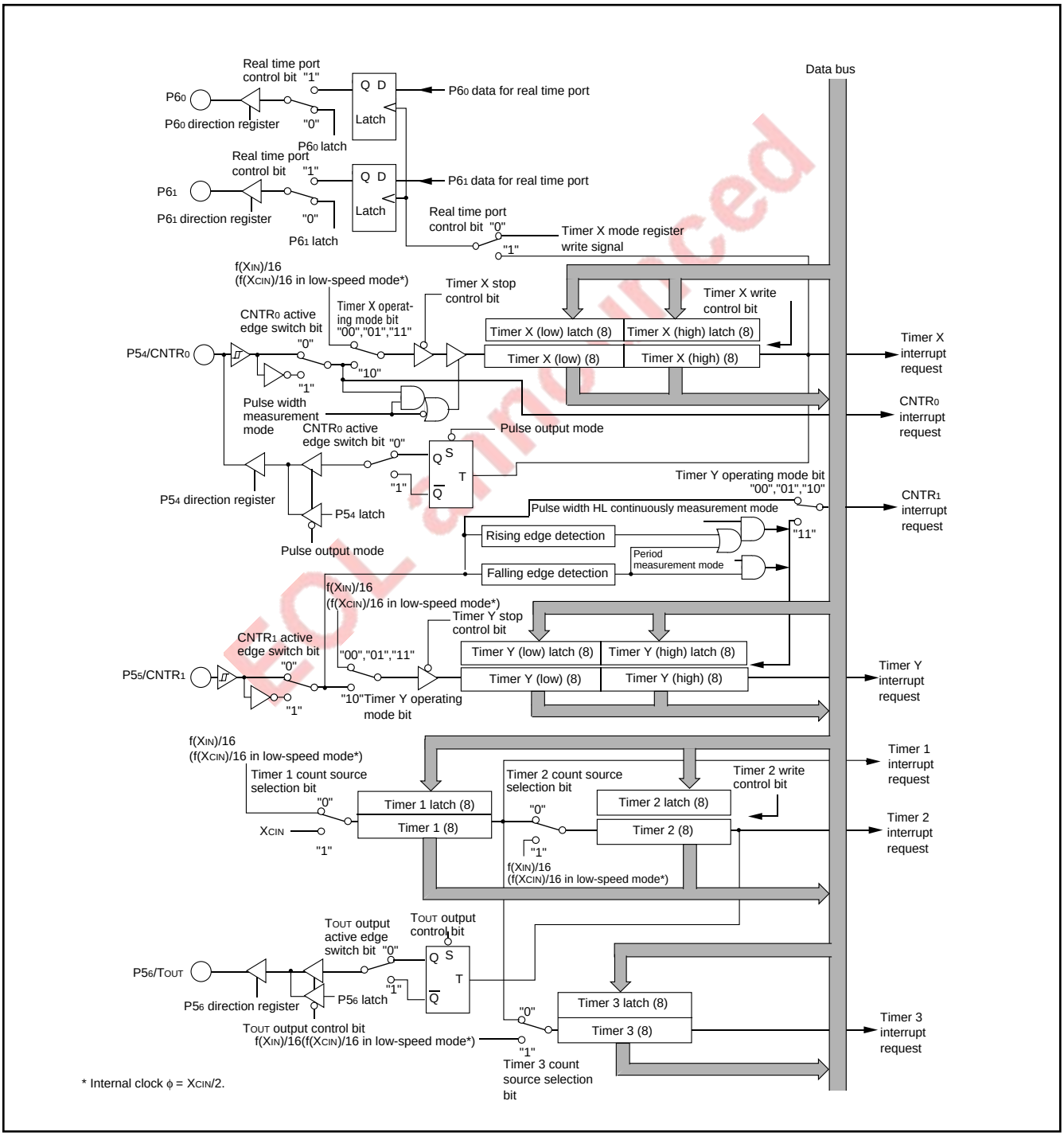


Fig. 11 Timer block diagram

Timer X

Timer X is a 16-bit timer that can be selected in one of four modes and can be controlled the timer X write and the real time port by setting the timer X mode register.

Timer mode

The timer counts f(XIN)/16 (or f(XCIN)/16 in low-speed mode).

Pulse output mode

Each time the timer underflows, a signal output from the CNTR0 pin is inverted. Except for this, the operation in pulse output mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P54 direction register to output mode.

Event counter mode

The timer counts signals input through the CNTR0 pin.
Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P54 direction register to input mode.

Pulse width measurement mode

The count source is f(XIN)/16 (or f(XCIN)/16 in low-speed mode. If CNTR0 active edge switch bit is “0”, the timer counts while the input signal of CNTR0 pin is at “H”. If it is “1”, the timer counts while the input signal of CNTR0 pin is at “L”. When using a timer in this mode, set the corresponding port P54 direction register to input mode.

Timer X Write Control

If the timer X write control bit is “0”, when the value is written in the address of timer X, the value is loaded in the timer X and the latch at the same time.
If the timer X write control bit is “1”, when the value is written in the address of timer X, the value is loaded only in the latch. The value in the latch is loaded in timer X after timer X underflows.
If the value is written in latch only, unexpected value may be set in the high-order counter when the writing in high-order latch and the underflow of timer X are performed at the same timing.

Note on CNTR0 Interrupt Active Edge Selection

CNTR0 interrupt active edge depends on the CNTR0 active edge switch bit.

Real Time Port Control

While the real time port function is valid, data for the real time port are output from ports P60 and P61 each time the timer X underflows. (However, after rewriting a data for real time port, if the real time port control bit is changed from “0” to “1”, data is output without the timer X.) If the data for the real time port is changed while the real time port function is valid, the changed data are output at the next underflow of timer X.
Before using this function, set the corresponding port direction registers to output mode.

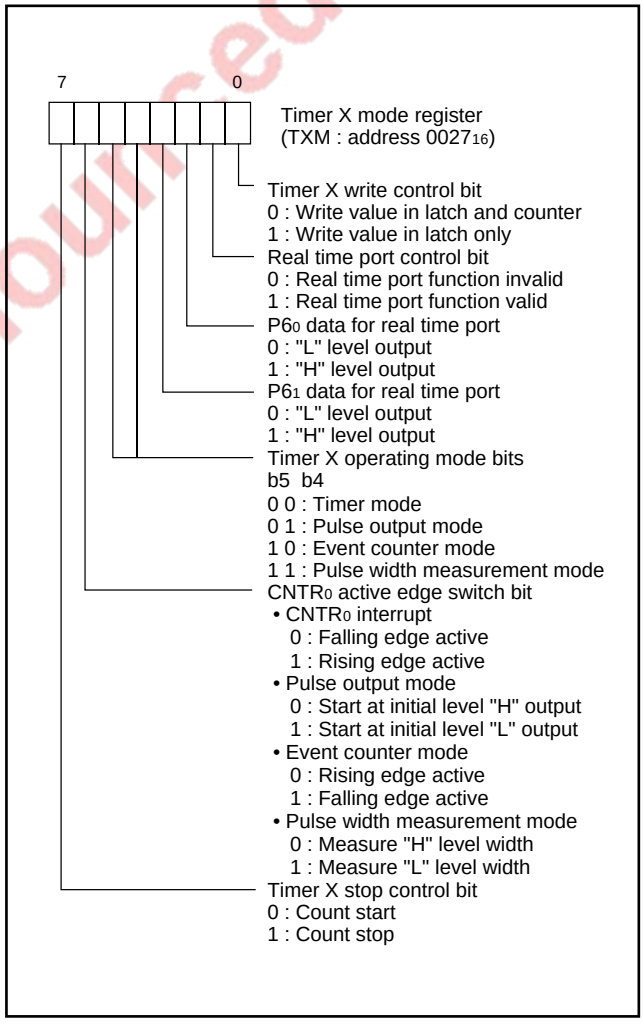


Fig. 12 Structure of timer X mode register

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Timer Y

Timer Y is a 16-bit timer that can be selected in one of four modes.

Timer mode

The timer counts f(XIN)/16 (or f(XCIN)/16 in low-speed mode).

Period measurement mode

CNTR1 interrupt request is generated at rising/falling edge of CNTR1 pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting down. /Except for the above-mentioned, the operation in period measurement mode is the same as in timer mode.

The timer value just before the reloading at rising/falling of CNTR1 pin input signal is retained until the timer Y is read once after the reload.

The rising/falling timing of CNTR1 pin input signal is found by CNTR1 interrupt. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

Event counter mode

The timer counts signals input through the CNTR1 pin.

Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

Pulse width HL continuously measurement mode

CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

Note on CNTR1 Interrupt Active Edge Selection

CNTR1 interrupt active edge depends on the CNTR1 active edge switch bit. However, in pulse width HL continuously measurement mode, CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal regardless of the setting of CNTR1 active edge switch bit.

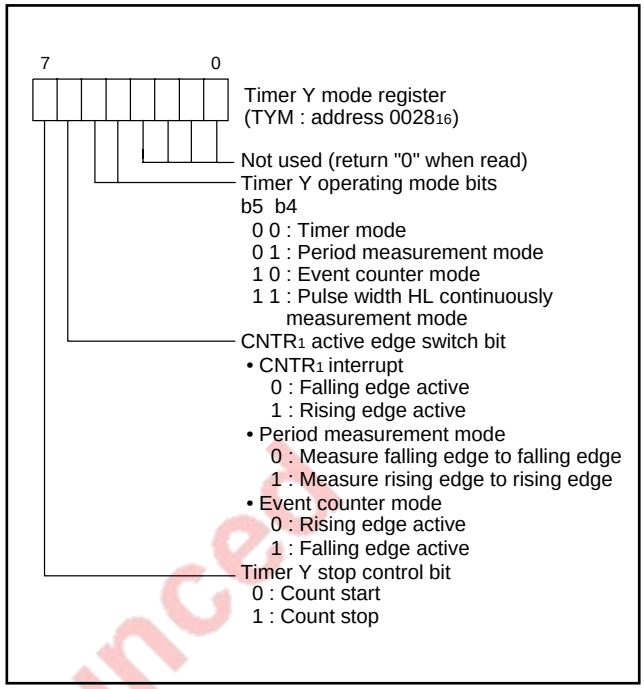


Fig. 13 Structure of timer Y mode register

EOL announced

Timer 1, Timer 2, Timer 3

Timer 1, timer 2, and timer 3 are 8-bit timers. The count source for each timer can be selected by timer 123 mode register. The timer latch value is not affected by a change of the count source. However, because changing the count source may cause an inadvertent count down of the timer. Therefore, rewrite the value of timer whenever the count source is changed.

Timer 2 Write Control

If the timer 2 write control bit is “0”, when the value is written in the address of timer 2, the value is loaded in the timer 2 and the latch at the same time.

If the timer 2 write control bit is “1”, when the value is written in the address of timer 2, the value is loaded only in the latch. The value in the latch is loaded in timer 2 after timer 2 underflows.

Timer 2 Output Control

When the timer 2 (TOUT) is output enabled, an inversion signal from pin TOUT is output each time timer 2 underflows.

In this case, set the port P56 shared with the port TOUT to the output mode.

Note on Timer 1 to Timer 3

When the count source of timer 1 to 3 is changed, the timer counting value may be changed large because a thin pulse is generated in count input of timer. If timer 1 output is selected as the count source of timer 2 or timer 3, when timer 1 is written, the counting value of timer 2 or timer 3 may be changed large because a thin pulse is generated in timer 1 output.

Therefore, set the value of timer in the order of timer 1, timer 2 and timer 3 after the count source selection of timer 1 to 3.

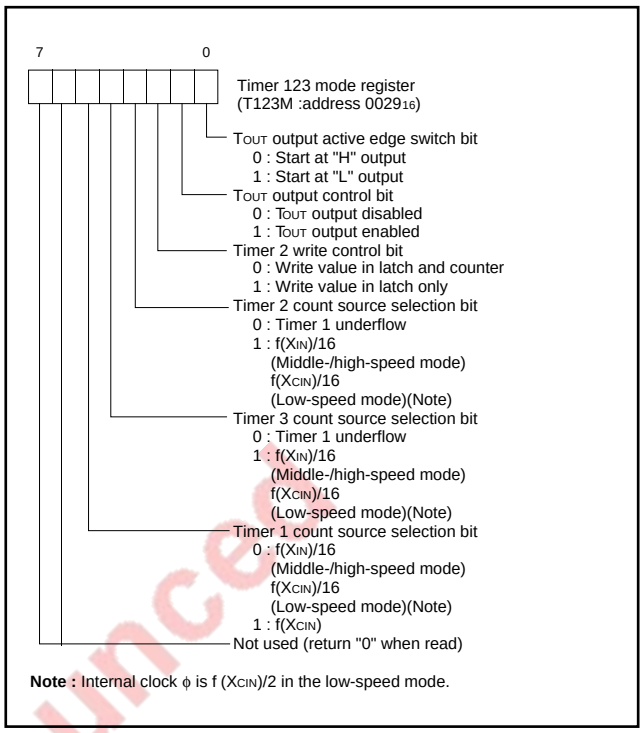


Fig. 14 Structure of timer 123 mode register

EOL announced

SERIAL I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O1. A dedicated timer (baud rate generator) is also provided for baud rate generation.

Clock Synchronous Serial I/O1 Mode

Clock synchronous serial I/O1 mode can be selected by setting the mode selection bit of the serial I/O1 control register to "1".
For clock synchronous serial I/O1, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB (address 0018_{16}).

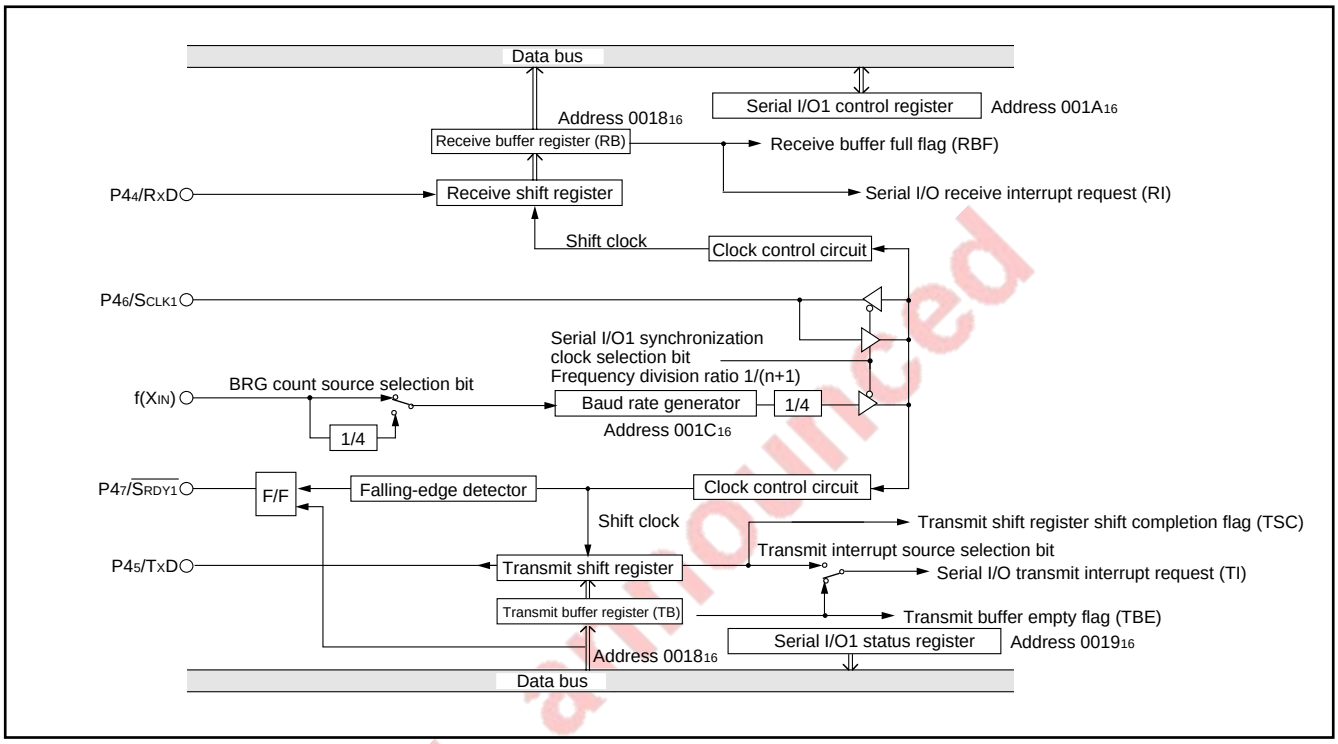
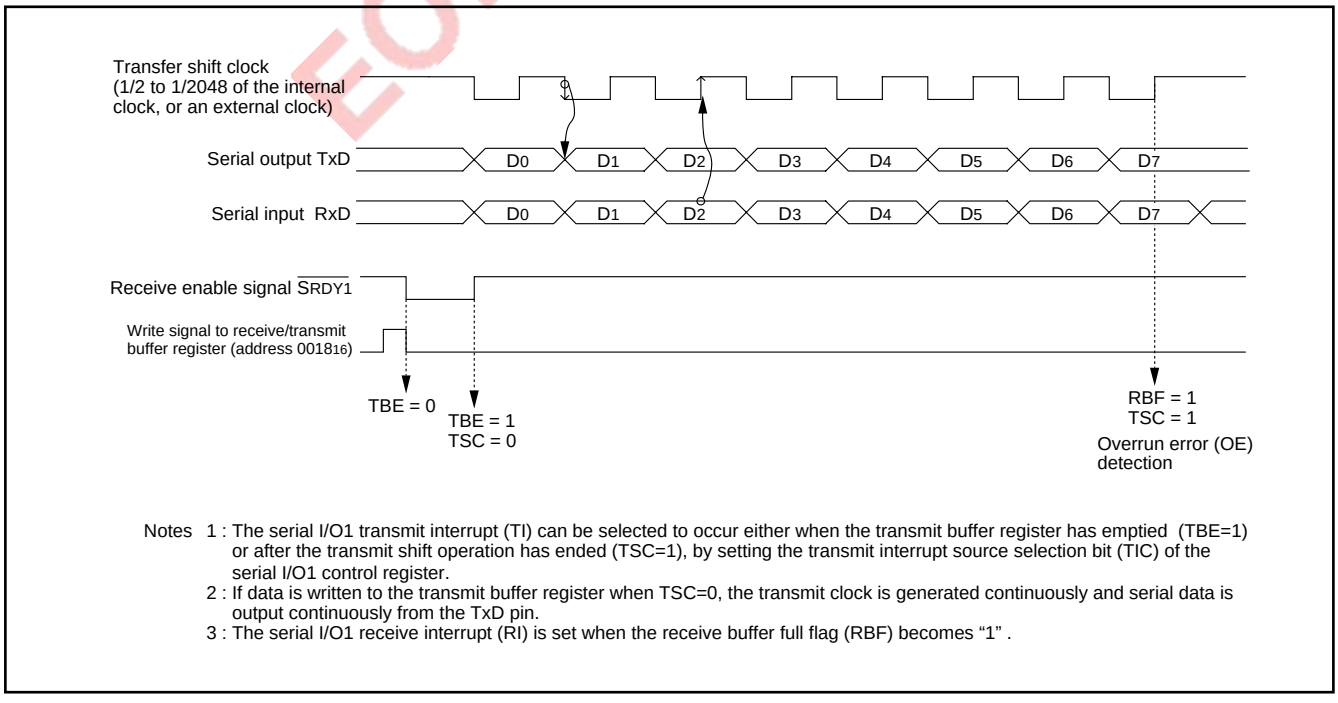


Fig. 15 Block diagram of clock synchronous serial I/O1



Notes 1 : The serial I/O1 transmit interrupt (TI) can be selected to occur either when the transmit buffer register has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
2 : If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3 : The serial I/O1 receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1" .

Fig. 16 Operation of clock synchronous serial I/O1 function

EOL announced

Asynchronous Serial I/O1 (UART) Mode

Clock asynchronous serial I/O1 mode (UART) can be selected by clearing the serial I/O1 mode selection bit of the serial I/O1 control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer register, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

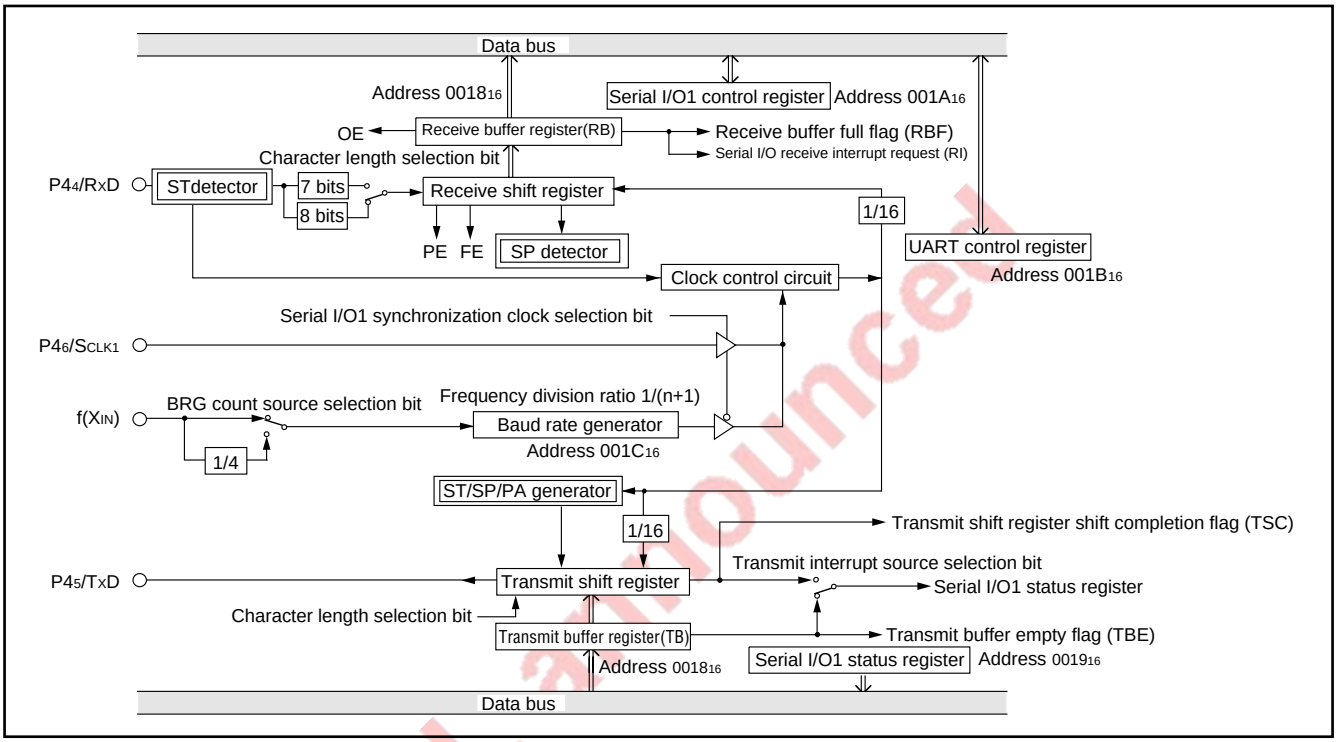
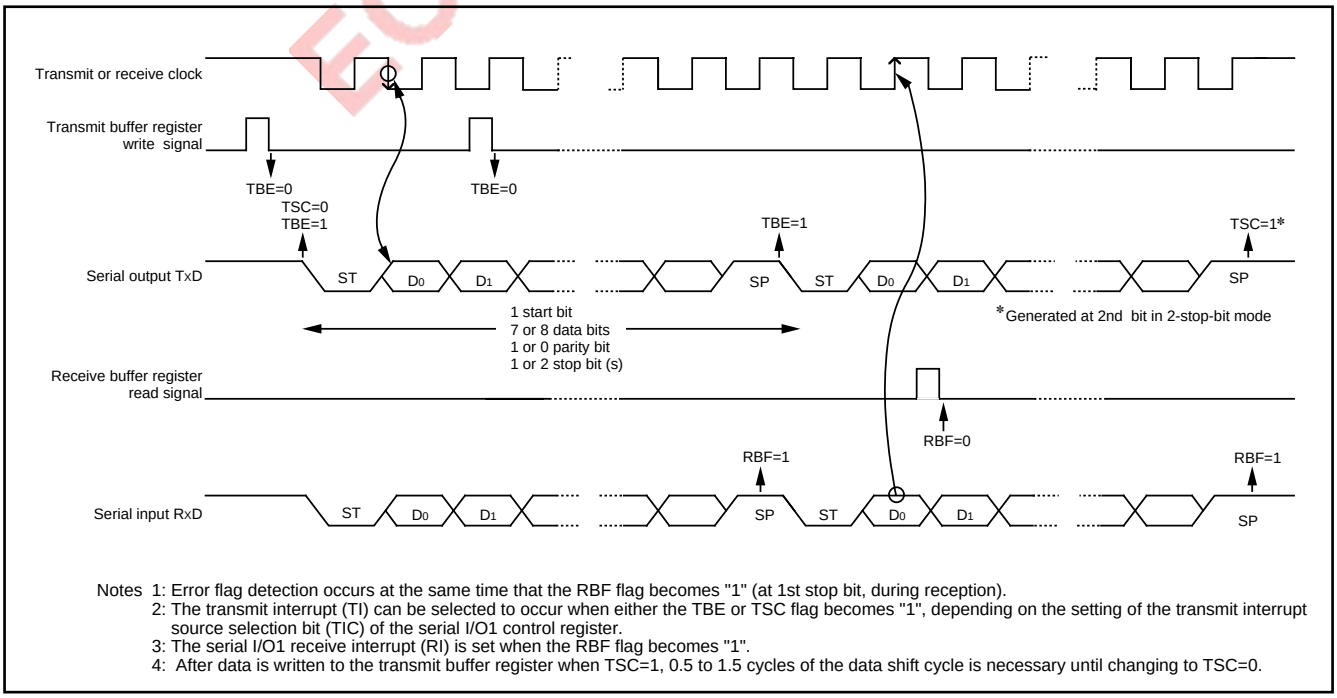


Fig. 17 Block diagram of UART serial I/O1



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2: The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes "1", depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3: The serial I/O1 receive interrupt (RI) is set when the RBF flag becomes "1".
4: After data is written to the transmit buffer register when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 18 Operation of UART serial I/O1 function

EOL announced

Serial I/O1 Control Register (SIO1CON) 001A16

The serial I/O1 control register contains eight control bits for the serial I/O1 function.

UART Control Register (UARTCON) 001B16

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the P45/TxD pin.

Serial I/O1 Status Register (SIO1STS) 001916

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing “0” to the serial I/O enable bit SIOE (bit 7 of the Serial I/O Control Register) also clears all the status flags, including the error flags.

All bits of the serial I/O1 status register are initialized to “0” at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to “1”, the transmit shift register shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

Transmit Buffer/Receive Buffer Register (TB/RB) 001816

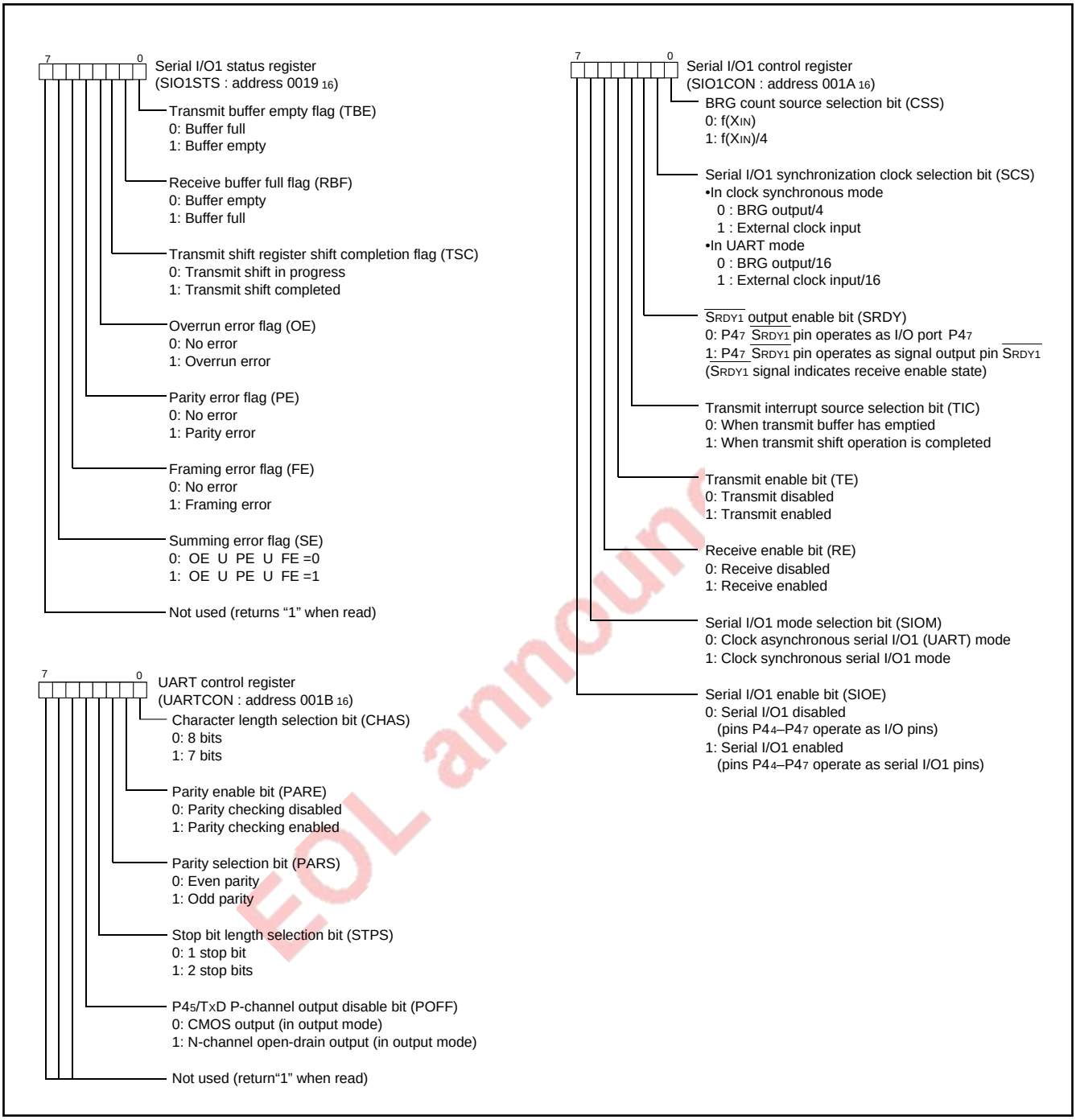
The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is write-only and the receive buffer register is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer register is “0”.

Baud Rate Generator (BRG) 001C16

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

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Fig. 19 Structure of serial I/O1 control registers

SERIAL I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O2 the transmitter and the receiver must use the same clock. If the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

Serial I/O2 Control Register (SIO2CON) 001D16

The serial I/O2 control register contains 7 bits which control various serial I/O functions.

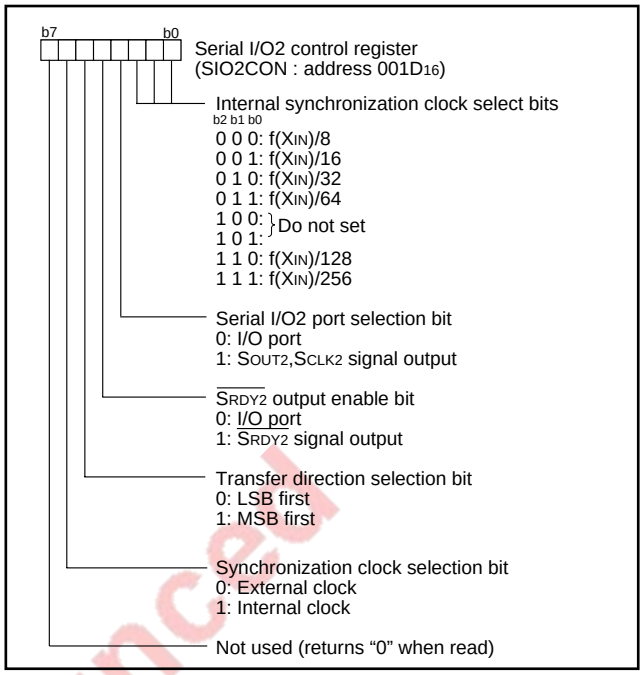


Fig. 20 Structure of serial I/O2 control register

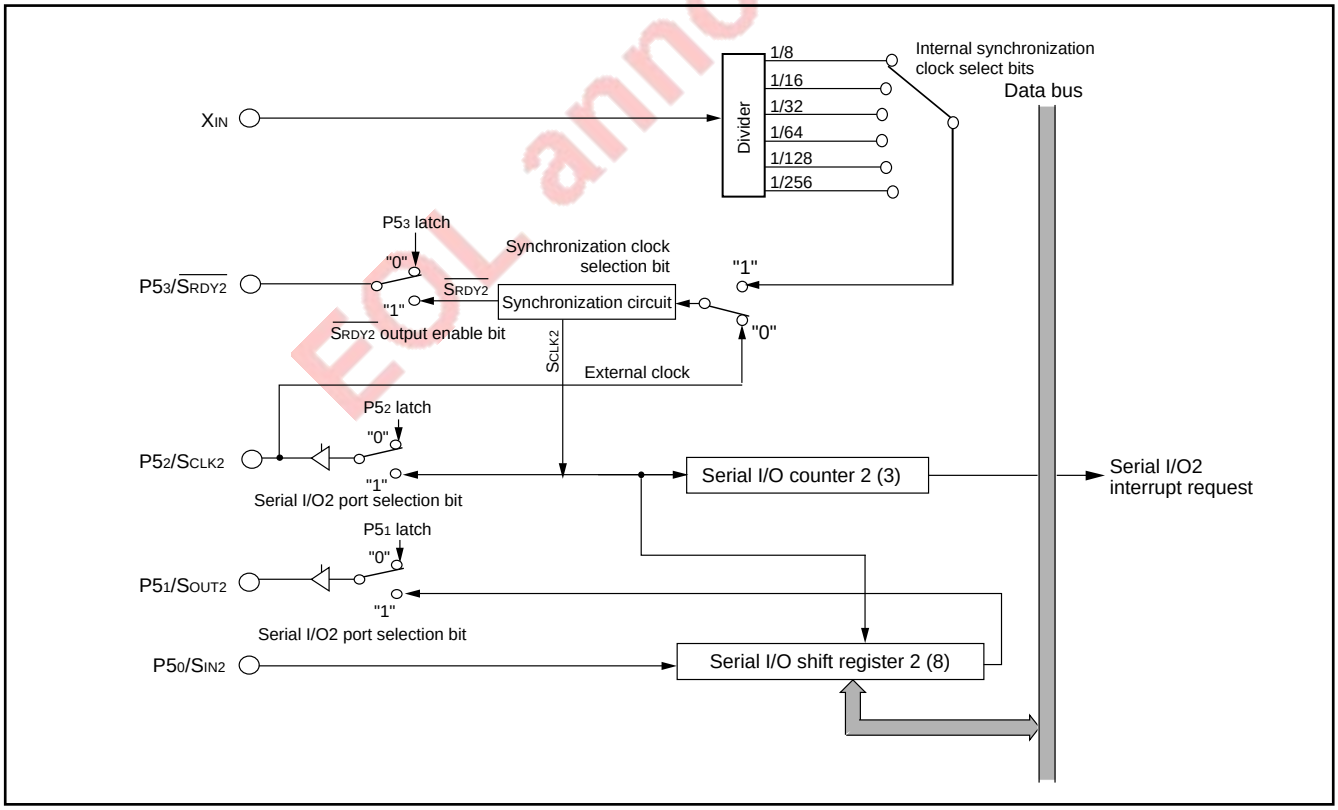
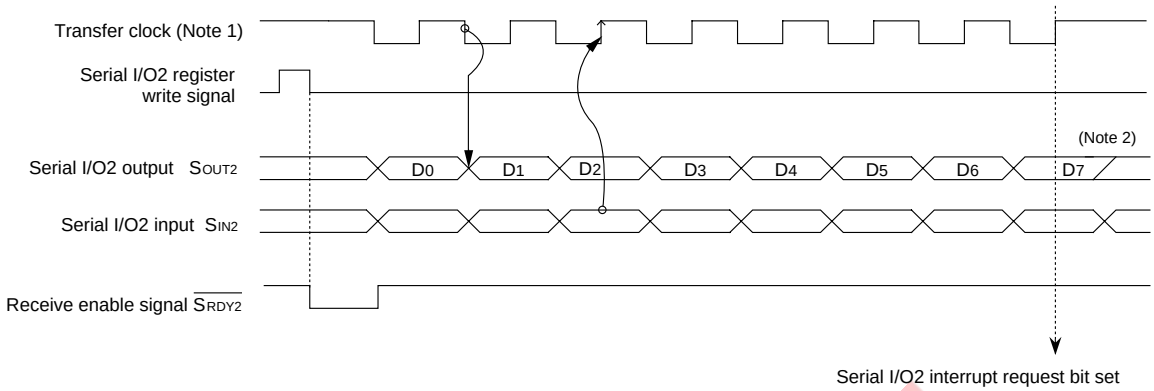


Fig. 21 Block diagram of serial I/O2 function

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Notes 1: When the internal clock is selected as the transfer clock, the divide ratio can be selected by setting bits 0 to 2 of the serial I/O2 control register.
2: When the internal clock is selected as the transfer clock, the S_{OUT2} pin goes to high impedance after transfer completion.

Fig. 22 Timing of serial I/O2 function

EOL announced

LCD DRIVE CONTROL CIRCUIT

The 3820 group has the built-in Liquid Crystal Display (LCD) drive control circuit consisting of the following.

- LCD display RAM
- Segment output enable register
- LCD mode register
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

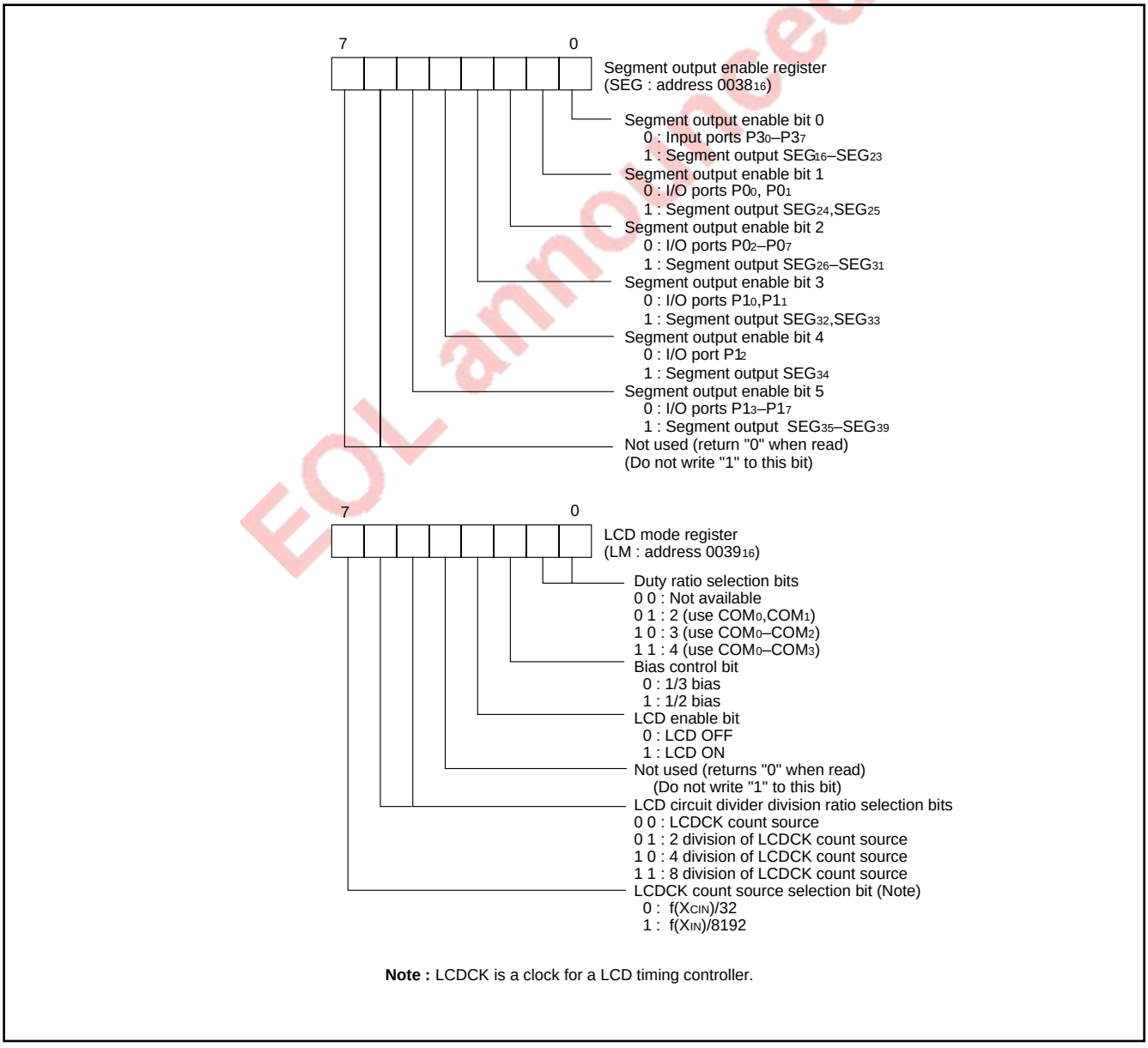
A maximum of 40 segment output pins and 4 common output pins can be used.

Up to 160 pixels can be controlled for LCD display. When the LCD enable bit is set to “1” after data is set in the LCD mode register, the segment output enable register and the LCD display RAM, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

Table 2. Maximum number of display pixels at each duty ratio

Duty ratio	Maximum number of display pixel
2	80 dots or 8 segment LCD 10 digits
3	120 dots or 8 segment LCD 15 digits
4	160 dots or 8 segment LCD 20 digits

EOL announced



Note : LCDCK is a clock for a LCD timing controller.

Fig. 23 Structure of segment output enable register and LCD mode register

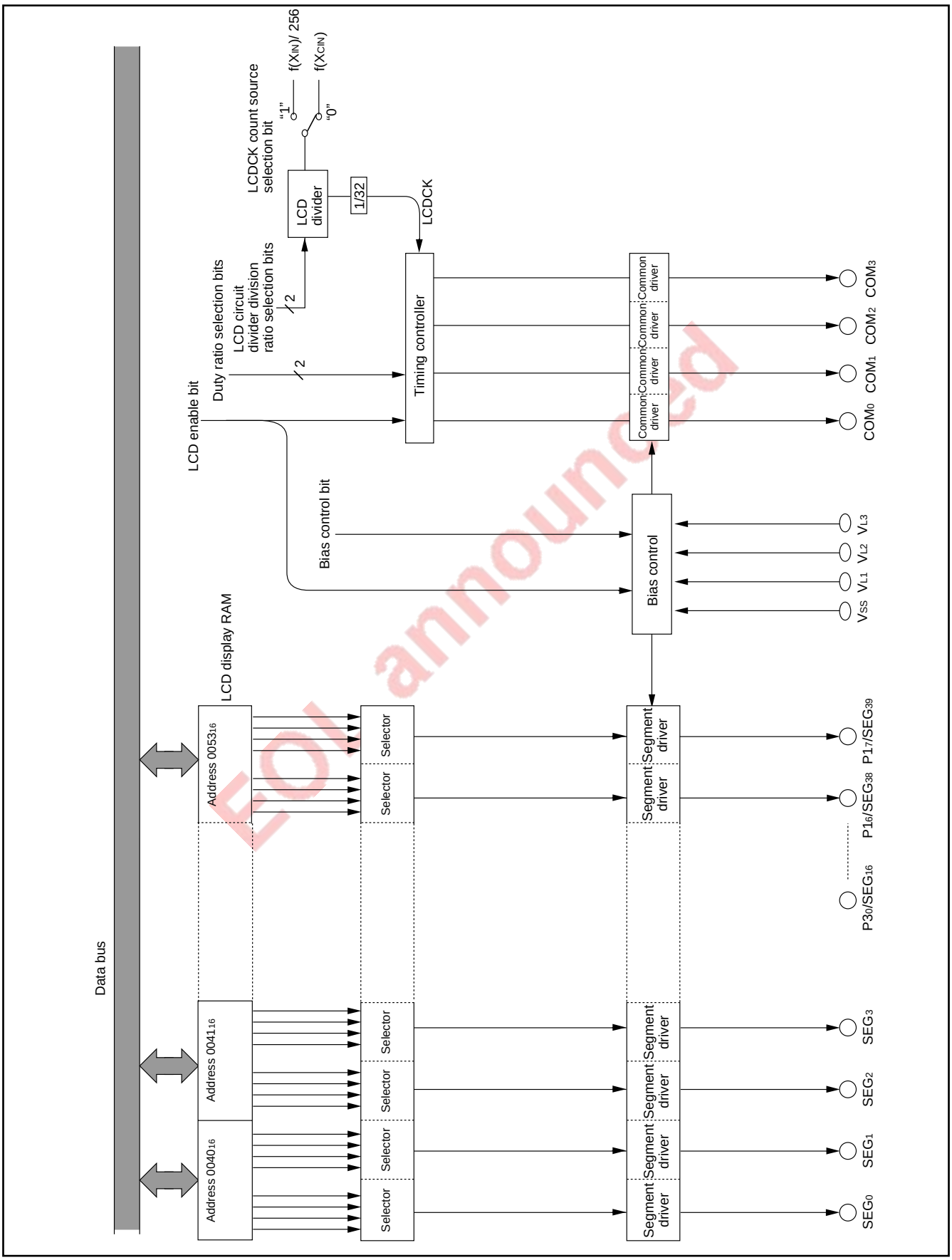


Fig. 24 Block diagram of LCD controller/driver

Bias Control and Applied Voltage to LCD Power Input Pins

To the LCD power input pins (V_{L1}–V_{L3}), apply the voltage shown in Table 3 according to the bias value.
Select a bias value by the bias control bit (bit 2 of the LCD mode register).

Common Pin and Duty Ratio Control

The common pins (COM_0–COM_3) to be used are determined by duty ratio.
Select duty ratio by the duty ratio selection bits (bits 0 and 1 of the LCD mode register).

Table 3. Bias control and applied voltage to V_{L1}–V_{L3}

Bias value	Voltage value
1/3 bias	$V_{L3}=V_{LCD}$ $V_{L2}=2/3\ V_{LCD}$ $V_{L1}=1/3\ V_{LCD}$
1/2 bias	$V_{L3}=V_{LCD}$ $V_{L2}=V_{L1}=1/2\ V_{LCD}$

Note 1 : V_{LCD} is the maximum value of supplied voltage for the LCD panel.

Table 4. Duty ratio control and common pins used

Duty ratio	Duty ratio selection bit		Common pins used
	Bit 1	Bit 0	
2	0	1	COM_0, COM_1 (Note 1)
3	1	0	COM_0–COM_2 (Note 2)
4	1	1	COM_0–COM_3

Notes 1 : COM_2 and COM_3 are open
2 : COM_3 is open

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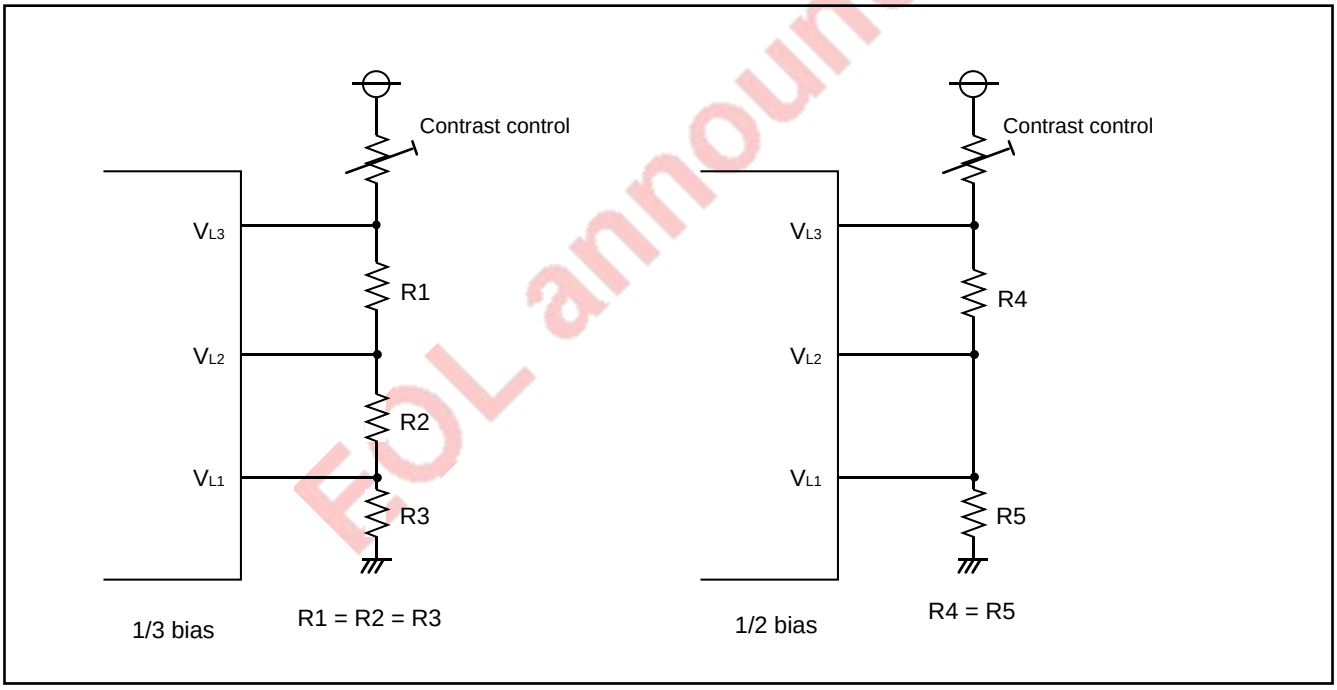


Fig. 25 Example of circuit at each bias

LCD Display RAM

Address 0040_{16} to 0053_{16} is the designated RAM for the LCD display. When "1" are written to these addresses, the corresponding segments of the LCD display panel are turned on.

LCD Drive Timing

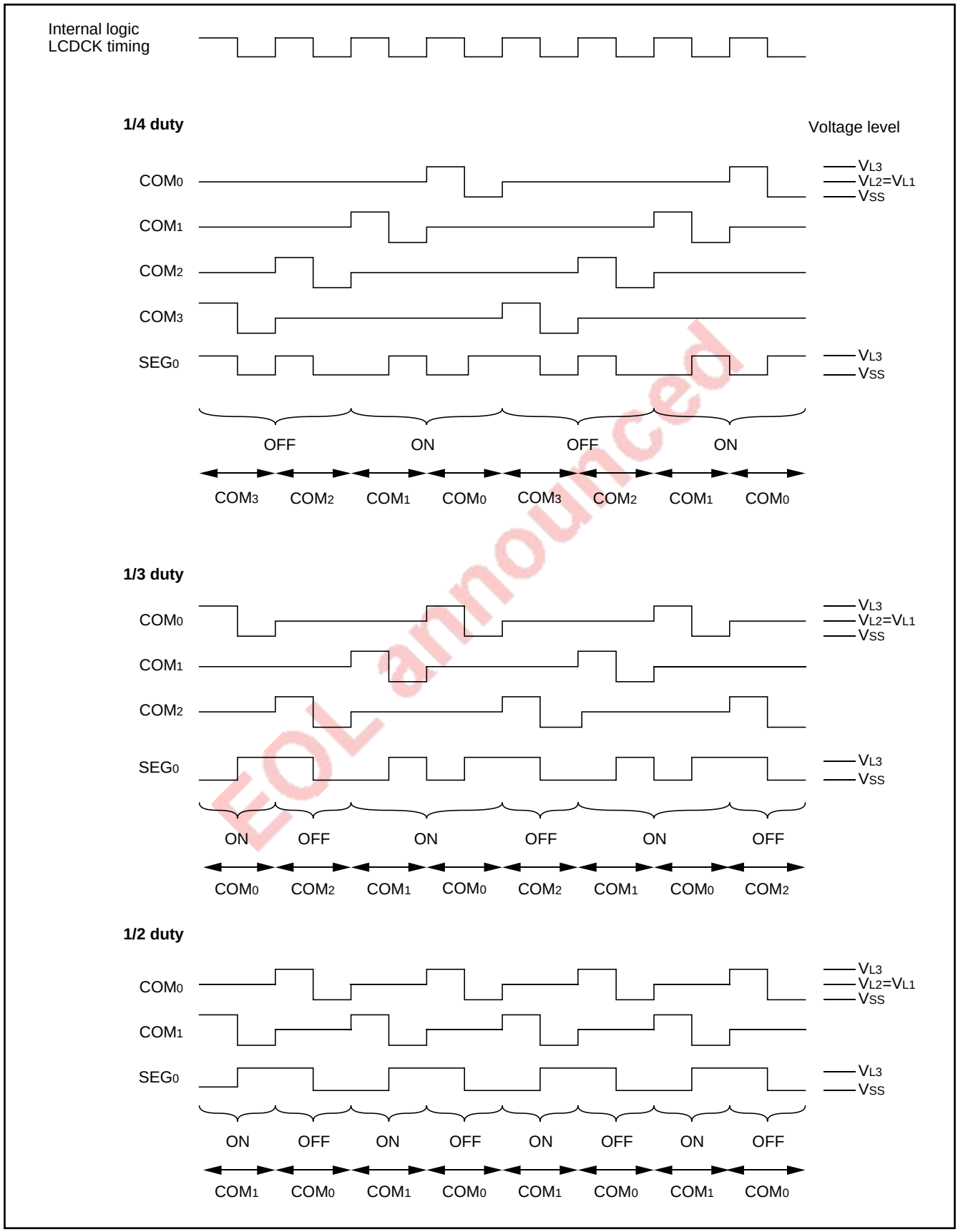
The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(LCDCK) = \frac{\text{(frequency of count source for LCDCK)}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency} = \frac{f(LCDCK)}{\text{duty ratio}}$$

Address \ Bit	7	6	5	4	3	2	1	0
	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0
0040_{16}	SEG_1				SEG_0			
0041_{16}	SEG_3				SEG_2			
0042_{16}	SEG_5				SEG_4			
0043_{16}	SEG_7				SEG_6			
0044_{16}	SEG_9				SEG_8			
0045_{16}	SEG_{11}				SEG_{10}			
0046_{16}	SEG_{13}				SEG_{12}			
0047_{16}	SEG_{15}				SEG_{14}			
0048_{16}	SEG_{17}				SEG_{16}			
0049_{16}	SEG_{19}				SEG_{18}			
$004A_{16}$	SEG_{21}				SEG_{20}			
$004B_{16}$	SEG_{23}				SEG_{22}			
$004C_{16}$	SEG_{25}				SEG_{24}			
$004D_{16}$	SEG_{27}				SEG_{26}			
$004E_{16}$	SEG_{29}				SEG_{28}			
$004F_{16}$	SEG_{31}				SEG_{30}			
0050_{16}	SEG_{33}				SEG_{32}			
0051_{16}	SEG_{35}				SEG_{34}			
0052_{16}	SEG_{37}				SEG_{36}			
0053_{16}	SEG_{39}				SEG_{38}			

Fig. 26 LCD display RAM map



EOL announced

Fig. 27 LCD drive waveform (1/2 bias)

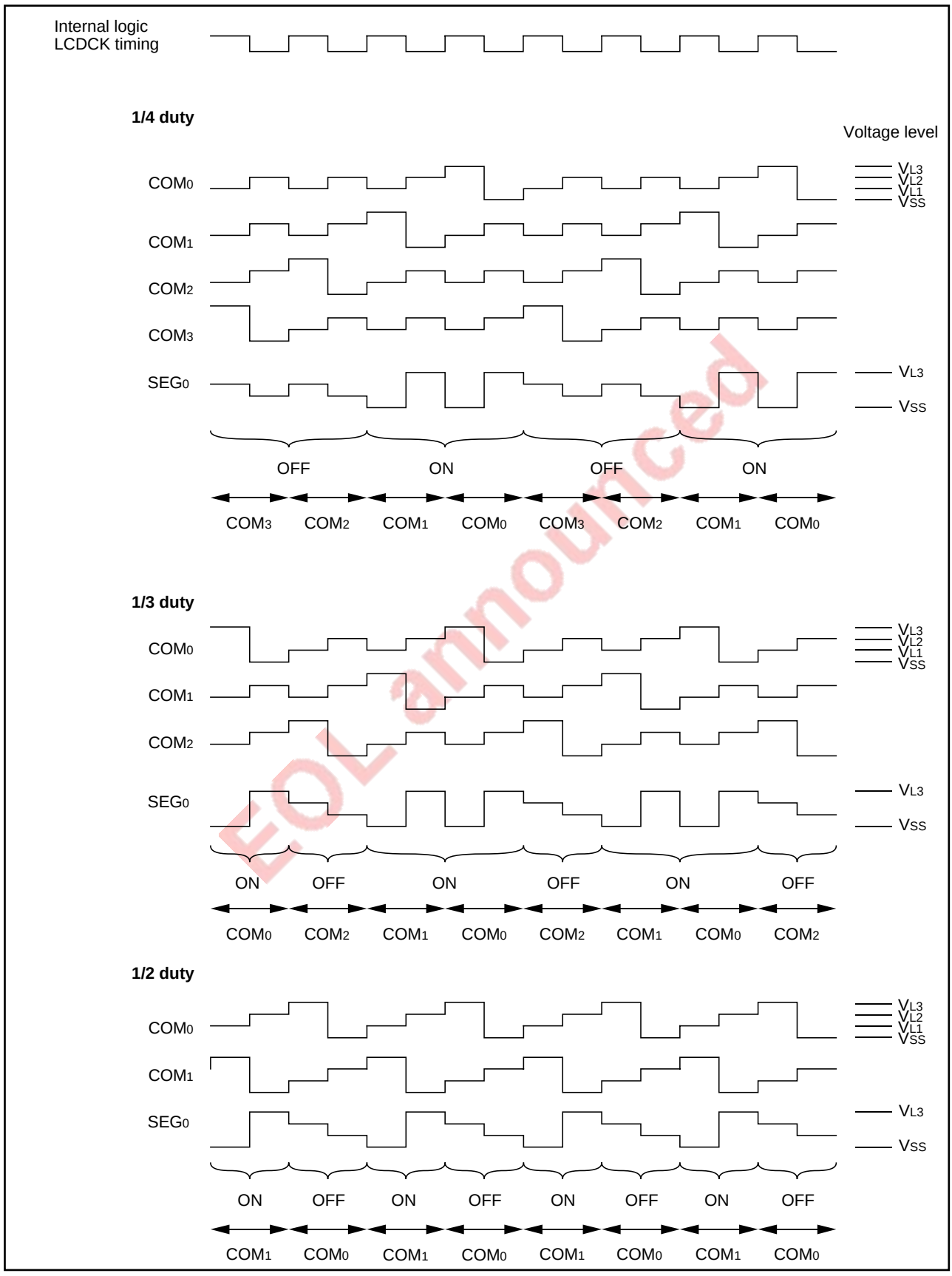


Fig. 28 LCD drive waveform (1/3 bias)

EOL announced

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away).

The watchdog timer consists of an 8-bit watchdog timer L and a 6-bit watchdog timer H.

Initial Value of Watchdog Timer

At reset or when writing data into the watchdog timer control register, the watchdog timer H is set to "3F16" and the watchdog timer L is set to "FF16". As a write instruction, it is possible to use any instruction that can cause a write signal such as STA, LDM and CLB. Write data except bit 7 has no significance and the above value is set independently.

Watchdog Timer Operation

The watchdog timer stops at reset and starts a countdown by writing to the watchdog timer control register. When the watchdog timer H underflows, an internal reset occurs, and the reset status is released after waiting the reset release time.

Then the program executes from the reset vector address.

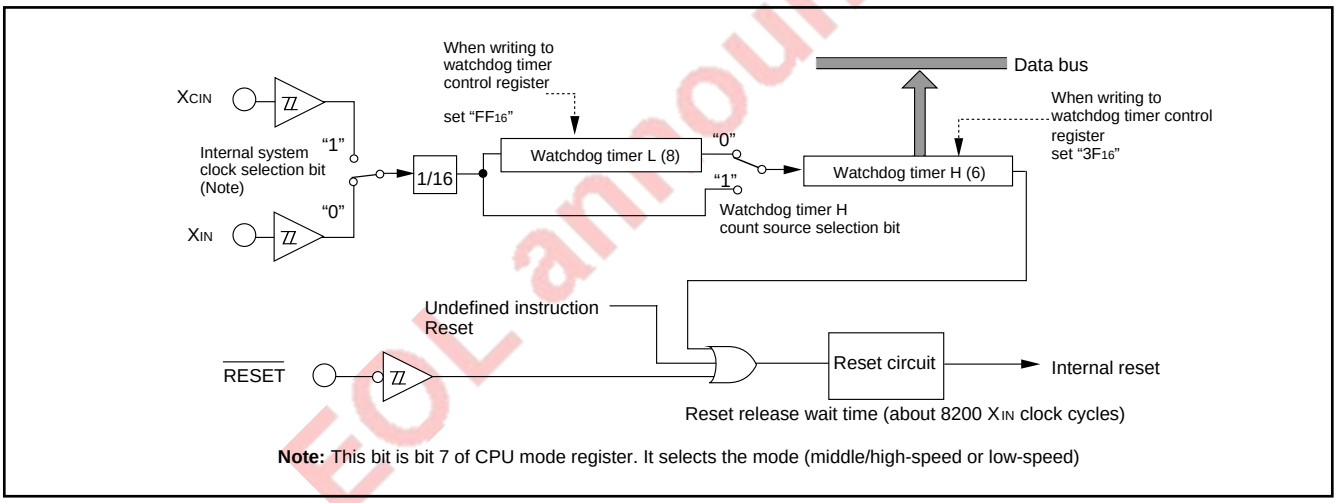
Usually, a program is designed so that data can be written into the watchdog timer control register before the watchdog timer H underflows. If data is not written once into the watchdog timer control register, the watchdog timer does not function.

At execution of the STP instruction, both clock and watchdog timer stops. At the same time that the stop mode is released, the watchdog timer restarts a count (Note). On the other hand, at execution of the WIT instruction, the watchdog timer does not stop.

The time from execution of writing to the watchdog timer control register until an underflow of the watchdog timer register H is as follows: (When bit 7 of the watchdog timer control register is "0")

- Middle / High-speed mode (f(XIN)=8 MHz) ..... 32.768 ms
- Low-speed mode (f(XCIN)=32 kHz) ..... 8.19 s

Note: During the stop release wait time [XIN (or XCIN) : about 8200 clock cycles], the watchdog timer counts.
Accordingly, does not underflow the watchdog timer H.



Note: This bit is bit 7 of CPU mode register. It selects the mode (middle/high-speed or low-speed)

Fig. 29 Watchdog timer block diagram

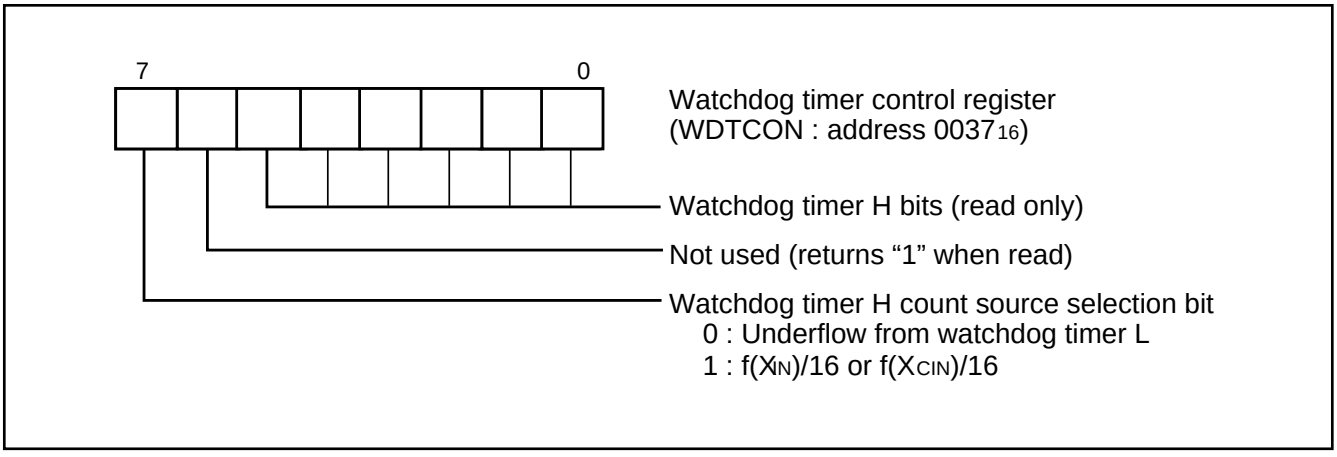


Fig. 30 Structure of watchdog timer control register

EOL announced

ϕ CLOCK OUTPUT FUNCTION

The internal system clock ϕ can be output from port P41 by setting the ϕ output control register. Set bit 1 of the port P4 direction register to when outputting ϕ clock.

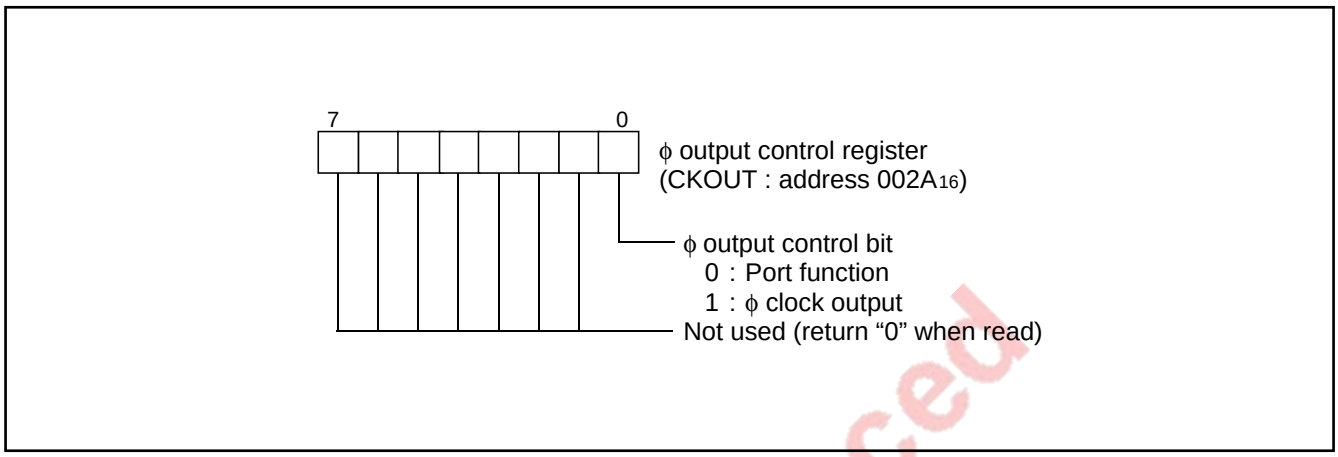


Fig. 31 Structure of ϕ output control register

EOL announced

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 2 μs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between 2.5 V and 5.5 V, and the oscillation should be stable), reset is released. In order to give the XIN clock time to stabilize, internal operation does not begin until after 8200 XIN clock cycles (timer 1 and timer 2 are connected together and 512 cycles of f(XIN)/16) are complete. After the reset is completed, the program starts from the address contained in address FFFD16 (high-order byte) and address FFFC16 (low-order byte).

Make sure that the reset input voltage is less than 0.5 V for VCC of 2.5 V (Extended operating temperature version: the reset input voltage is less than 0.6V for VCC of 3.0V).

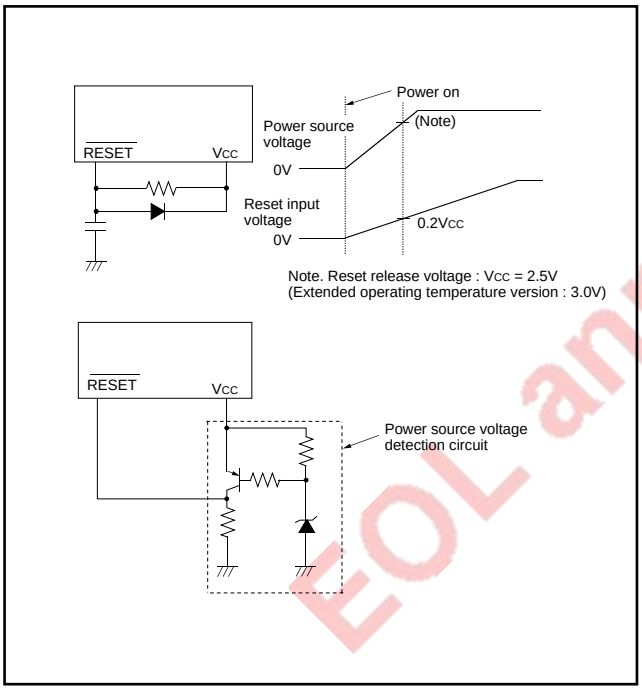


Fig. 32 Example of reset circuit

	Address	Register contents
(1) Port P0 direction register	(0001₁₆)	00₁₆
(2) Port P1 direction register	(0003₁₆)	00₁₆
(3) Port P2 direction register	(0005₁₆)	00₁₆
(4) Port P4 direction register	(0009₁₆)	00₁₆
(5) Port P5 direction register	(000B₁₆)	00₁₆
(6) Port P6 direction register	(000D₁₆)	00₁₆
(7) Port P7 direction register	(000F₁₆)	00₁₆
(8) PULL register A	(0016₁₆)	0 0 0 0 1 0 1 1
(9) PULL register B	(0017₁₆)	00₁₆
(10) Serial I/O1 status register	(0019₁₆)	1 0 0 0 0 0 0 0
(11) Serial I/O1 control register	(001A₁₆)	00₁₆
(12) UART control register	(001B₁₆)	1 1 1 0 0 0 0 0
(13) Serial I/O2 control register	(001D₁₆)	00₁₆
(14) Timer X (low-order)	(0020₁₆)	FF₁₆
(15) Timer X (high-order)	(0021₁₆)	FF₁₆
(16) Timer Y (low-order)	(0022₁₆)	FF₁₆
(17) Timer Y (high-order)	(0023₁₆)	FF₁₆
(18) Timer 1	(0024₁₆)	FF₁₆
(19) Timer 2	(0025₁₆)	01₁₆
(20) Timer 3	(0026₁₆)	FF₁₆
(21) Timer X mode register	(0027₁₆)	00₁₆
(22) Timer Y mode register	(0028₁₆)	00₁₆
(23) Timer 123 mode register	(0029₁₆)	00₁₆
(24) φ output control register	(002A₁₆)	00₁₆
(25) Watchdog timer control register	(0037₁₆)	0 1 1 1 1 1 1 1
(26) Segment output enable register	(0038₁₆)	00₁₆
(27) LCD mode register	(0039₁₆)	00₁₆
(28) Interrupt edge selection register	(003A₁₆)	00₁₆
(29) CPU mode register	(003B₁₆)	0 1 0 0 1 0 0 0
(30) Interrupt request register 1	(003C₁₆)	00₁₆
(31) Interrupt request register 2	(003D₁₆)	00₁₆
(32) Interrupt control register 1	(003E₁₆)	00₁₆
(33) Interrupt control register 2	(003F₁₆)	00₁₆
(34) Processor status register	(PS)	x x x x x 1 x x
(35) Program counter	(PCH)	Contents of address FFFD₁₆
	(PCL)	Contents of address FFFC₁₆

Note. x : Undefined
The contents of all other registers and RAM are undefined at poweron reset, so they must be initialized by software.

Fig. 33 Internal state of microcomputer immediately after reset

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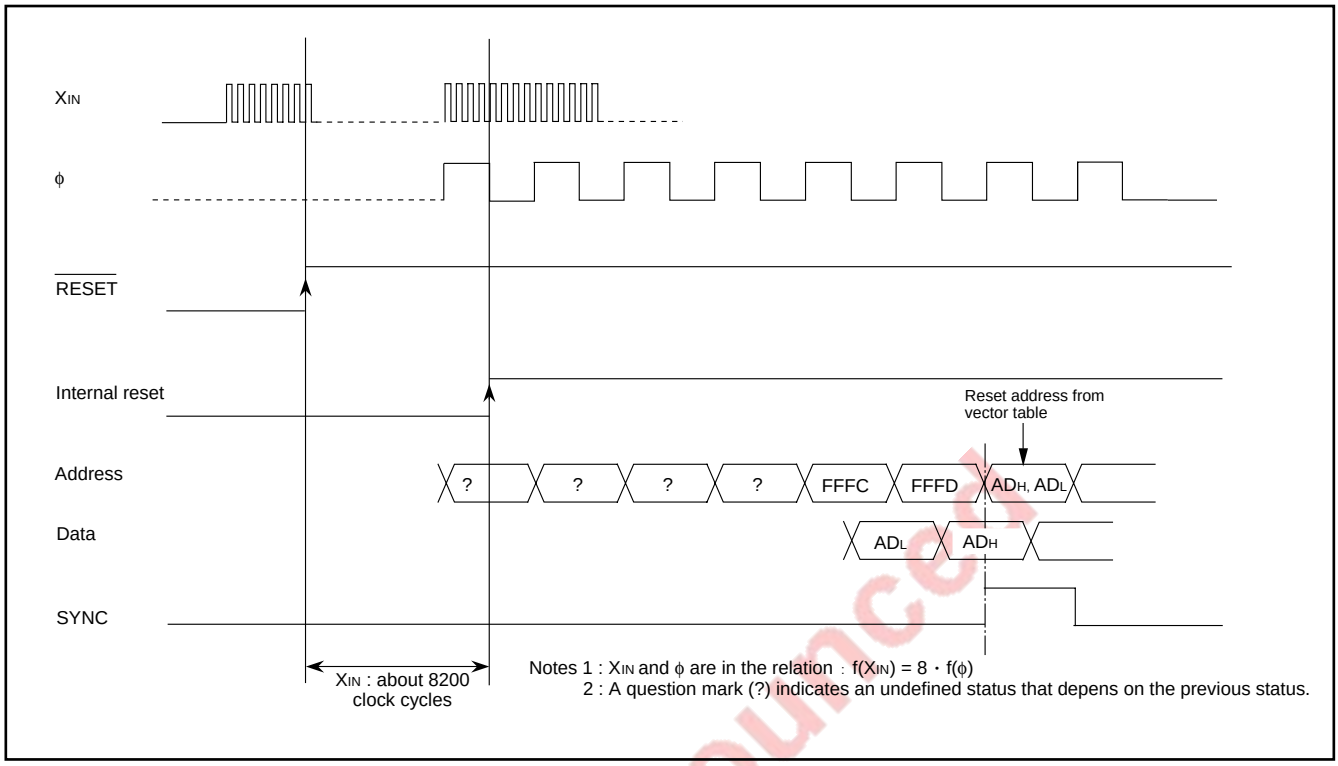


Fig. 34 Reset sequence

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CLOCK GENERATING CIRCUIT

The 3820 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT.

To supply a clock signal externally, input it to the XIN pin and make the XOUT pin open. The sub-clock XCIN-XCOUT oscillation circuit cannot directly input clocks that are externally generated. Accordingly, be sure to cause an external resonator to oscillate.

Immediately after poweron, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports. The pull-up resistor of XCIN and XCOUT pins must be made invalid to use the sub-clock.

Frequency Control

Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8.
After reset, this mode is selected.

High-speed mode

The internal clock ϕ is half the frequency of XIN.

Low-speed mode

- The internal clock ϕ is half the frequency of XCIN.
- A low-power consumption operation can be realized by stopping the main clock XIN in this mode. To stop the main clock, set bit 5 of the CPU mode register to "1".
  When the main clock XIN is restarted, set enough time for oscillation to stabilize by programming.

Note: If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub-clock to stabilize, especially immediately after poweron and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN)>3f(XCIN).

Oscillation Control

Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillators stop. Timer 1 is set to "FF16" and timer 2 is set to "0116".

Either XIN or XCIN divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2.

The bits of the timer 123 mode register except bit 4 are cleared to "0". Set the timer 1 and timer 2 interrupt enable bits to disabled ("0") before executing the STP instruction.

Oscillator restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize.

Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level. The states of XIN and XCIN are the same as the state before the executing the WIT instruction. The internal clock restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

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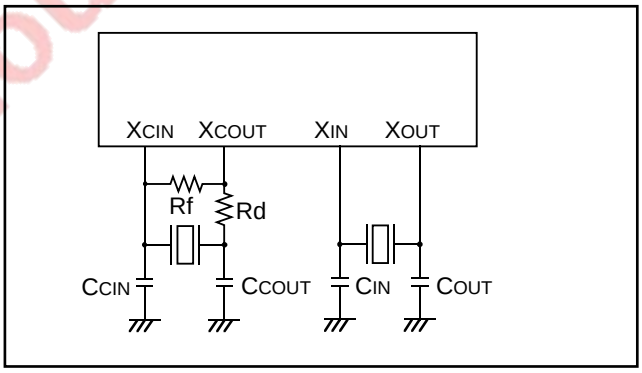


Fig. 35 Ceramic resonator circuit

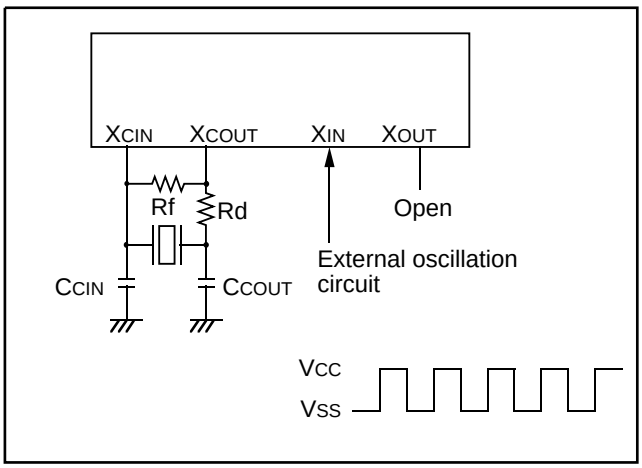
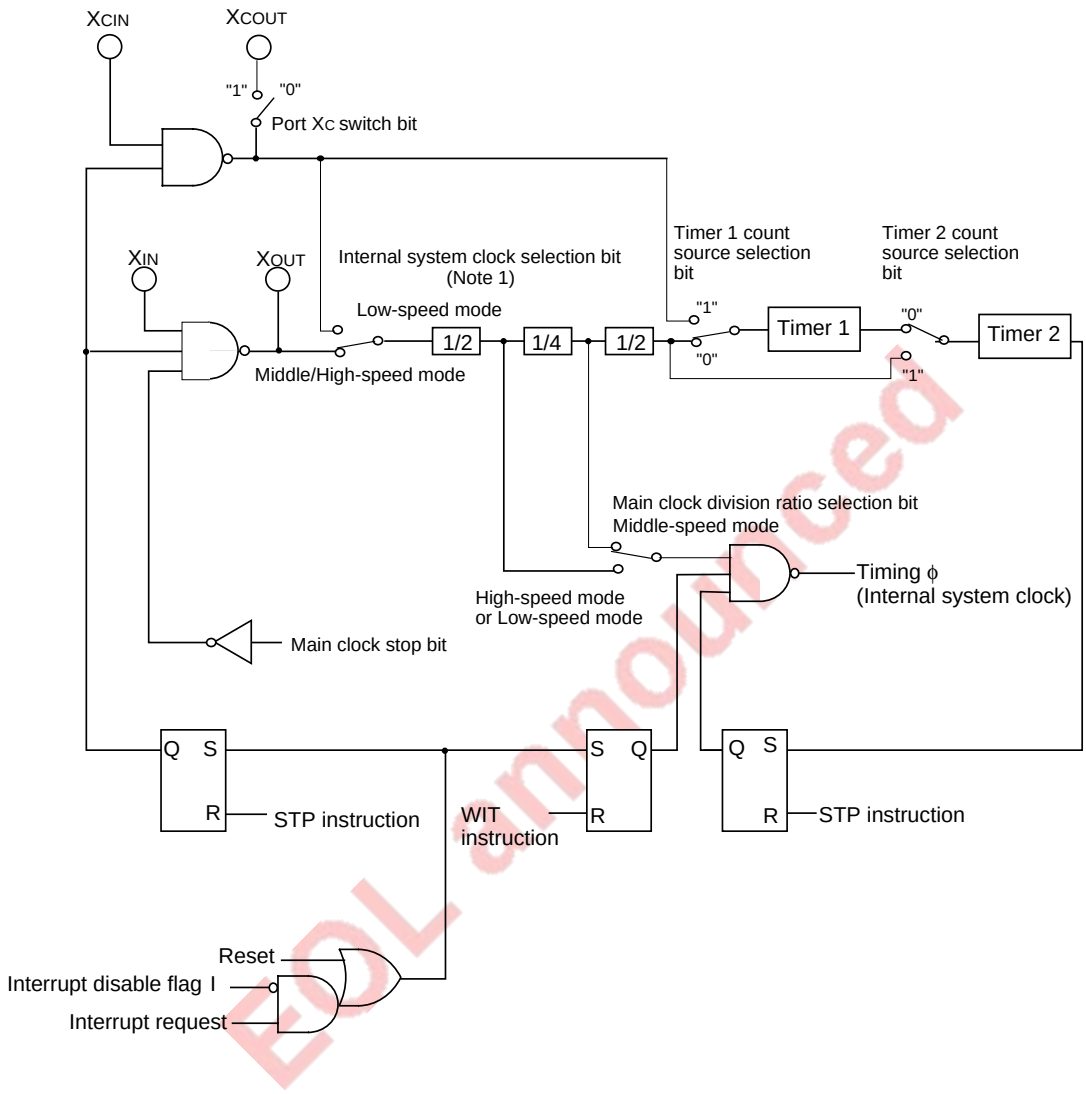


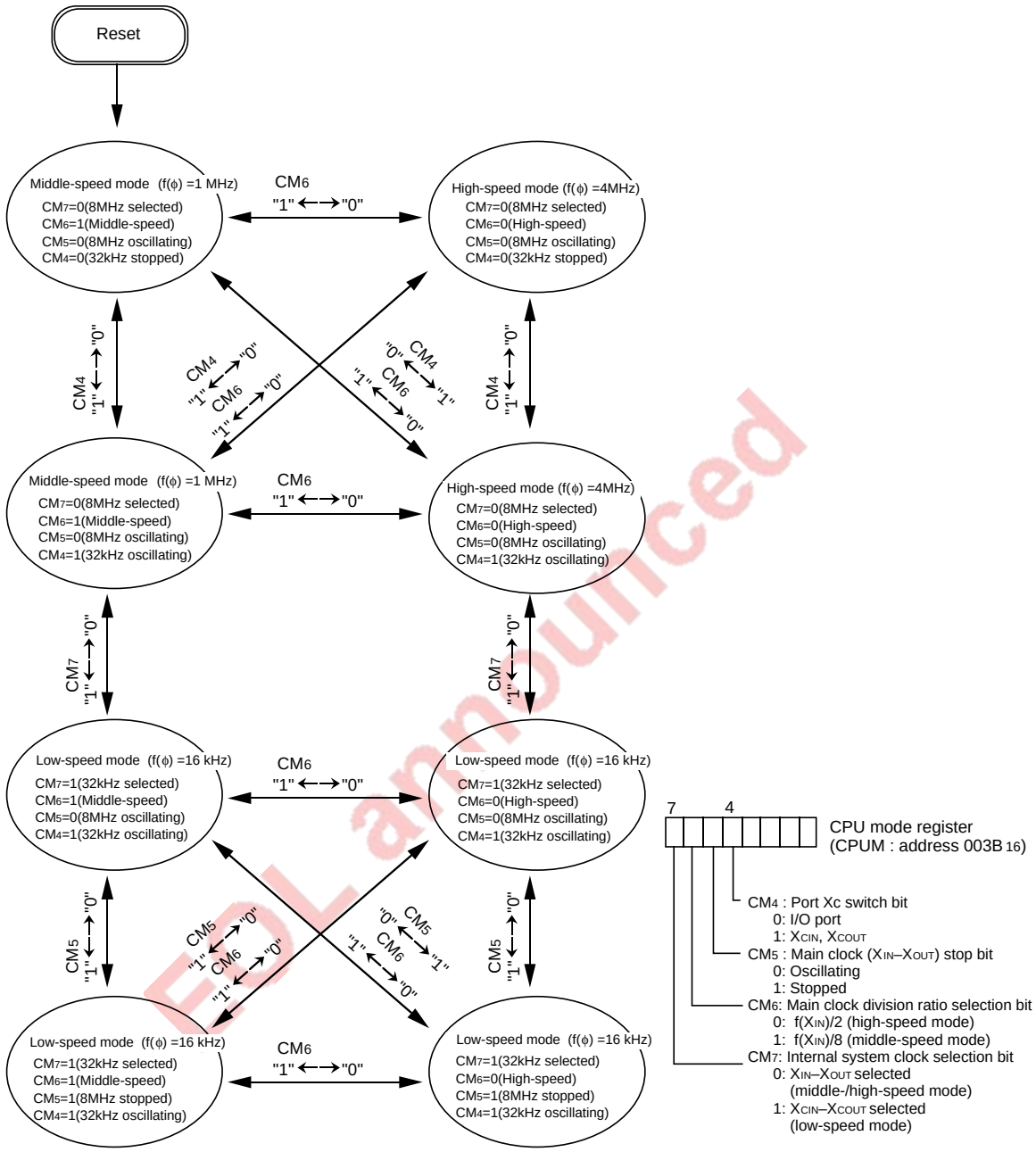
Fig. 36 External clock input circuit



Note : When using the low-speed mode, set the port Xc switch bit to "1" .

Fig. 37 Clock generating circuit block diagram

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Notes 1: Switch the mode by the allows shown between the mode blocks. (Do not switch between the mode directly without an allow.)
2: The all modes can be switched to the stop mode or the wait mode and returned to the source mode when the stop mode or the wat mode is released.
3: Timer and LCD operate in the wait mode.
4: In middle-/high-speed mode, when the stop mode is released, a delay of approximately 1 ms occurs automatically by timer 1 and timer 2.
5: In low-speed mode, when the stop mode is released, a delay of approximately 0.25 s occurs automatically by timer 1 and timer 2.
6: Wait until oscillation stabilizes after oscillating the main clock XIN before the switching from the low-speed mode to middle-/high-speed mode.
7: The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin. ϕ indicates the internal clock.

Fig. 38 State transitions of internal clock ϕ

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution.
In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.
The carry flag can be used to indicate whether a carry or borrow has occurred. Initialize the carry flag before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n + 1).

Multiplication and Division Instructions

The index mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read.
The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1".
Serial I/O1 continues to output the final bit from the TxD pin after transmission is completed. The SOUT2 pin from serial I/O2 goes to high impedance after transmission is completed.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions.
The frequency of the internal clock ϕ is half of the XIN frequency.

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DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form (three identical copies)

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Package	Name of Programming Adapter
80P6N-A	PCA4738F-80A
80P6S-A	PCA4738G-80
80P6D-A	PCA4738H-80
80D0	PCA4738L-80A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 39 is recommended to verify programming.

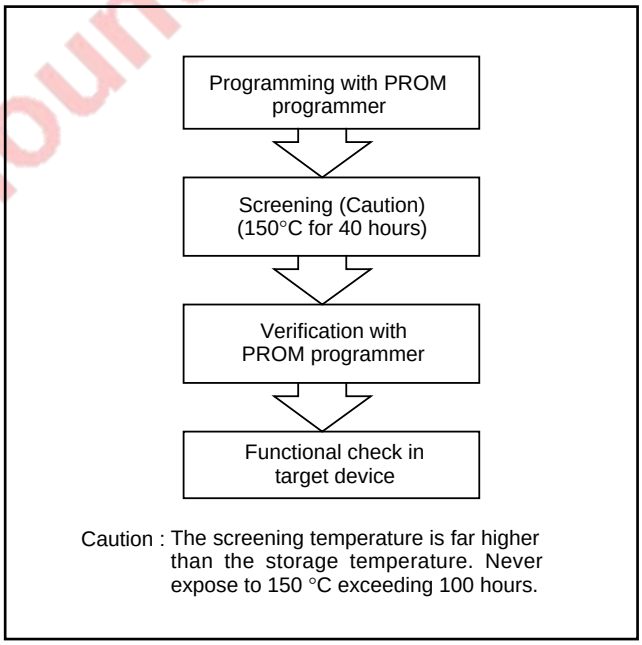


Fig. 39 Programming and testing of One Time PROM version

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$		–0.3 to V_{CC} +0.3	V
V_I	Input voltage V_{L1}		–0.3 to V_{L2}	V
V_I	Input voltage V_{L2}		V_{L1} to V_{L3}	V
V_I	Input voltage V_{L3}		V_{L2} to V_{CC} +0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$	At output port	–0.3 to V_{CC} +0.3	V
		At segment output	–0.3 to V_{L3} +0.3	V
V_O	Output voltage $P3_0$–$P3_7$	At segment output	–0.3 to V_{L3} +0.3	V
V_O	Output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$		–0.3 to V_{CC} +0.3	V
V_O	Output voltage SEG_0–SEG_{15}		–0.3 to V_{L3} +0.3	V
V_O	Output voltage X_{OUT}		–0.3 to V_{CC} +0.3	V
Pd	Power dissipation	T_a = 25 °C	300	mW
Topr	Operating temperature		–20 to 85	°C
Tstg	Storage temperature		–40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 2.5 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage	High-speed mode f(X_{IN})=8 MHz	4.0	5.0	5.5	V
		Middle-speed mode f(X_{IN})=8 MHz	2.5	5.0	5.5	
		Low-speed mode	2.5	5.0	5.5	
V_{SS}	Power source voltage			0		V
V_{IH}	“H” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_1$, $P4_5$, $P4_7$, $P5_1$, $P5_3$, $P5_6$, $P6_1$, $P7_0$, $P7_1$ (CM_4=0)	0.7 V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$P2_0$–$P2_7$, $P4_2$–$P4_4$, $P4_6$, $P5_0$, $P5_2$, $P5_4$, $P5_5$, $P5_7$, $P6_0$	0.8 V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$\overline{RESET}$	0.8 V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	X_{IN}	0.8 V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_0$, $P4_1$, $P4_5$, $P4_7$, $P5_1$, $P5_3$, $P5_6$, $P6_1$, $P7_0$, $P7_1$ (CM_4=0)	0		0.3 V_{CC}	V
V_{IL}	“L” input voltage	$P2_0$–$P2_7$, $P4_2$–$P4_4$, $P4_6$, $P5_0$, $P5_2$, $P5_4$, $P5_5$, $P5_7$, $P6_0$	0		0.2 V_{CC}	V
V_{IL}	“L” input voltage	$\overline{RESET}$	0		0.2 V_{CC}	V
V_{IL}	“L” input voltage	X_{IN}	0		0.2 V_{CC}	V

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RECOMMENDED OPERATING CONDITIONS (V_{CC} = 2.5 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (Note 1)			–40	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 1)			–40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (Note 1)			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 1)			40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (Note 1)			–20	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 1)			–20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (Note 1)			20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 1)			20	mA
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 2)			–5	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ (Note 2)			5	mA
$I_{OL(peak)}$	"L" peak output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 2)			10	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ (Note 3)			–1.0	mA
$I_{OH(avg)}$	"H" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 3)			–2.5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ (Note 3)			2.5	mA
$I_{OL(avg)}$	"L" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 3)			5.0	mA
$f(CNTR_0)$ $f(CNTR_1)$	Clock input frequency for timers X and Y (duty cycle 50 %)	4.0 V ≤ V_{CC} ≤ 5.5 V			4.0	MHz
		V_{CC} ≤ 4.0 V			$(2 \times V_{CC})-4$	MHz
$f(X_{IN})$	Main clock input oscillation frequency (Note 4)	High-speed mode (4.0 V ≤ V_{CC} ≤ 5.5 V)			8.0	MHz
		High-speed mode (V_{CC} ≤ 4.0 V)			$(4 \times V_{CC})-8$	MHz
		Middle-speed mode			8.0	MHz
$f(X_{CIN})$	Sub-clock input oscillation frequency (Note 4, 5)			32.768	50	kHz

Notes
1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2: The peak output current is the peak current flowing in each port.
3: The average output current is an average value measured over 100 ms.
4: When the oscillation frequency has a duty cycle of 50 %.
5: When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency $f(X_{CIN})$ is less than $f(X_{IN})/3$.

EOL announced

ELECTRICAL CHARACTERISTICS (V_{CC} =4.0 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$	I_{OH} = –0.1 mA	V_{CC}–2.0			V
			I_{OH} = –25 µA V_{CC} = 2.5 V	V_{CC}–1.0			V
V_{OH}	"H" output voltage	$P2_0$–$P2_7$, $P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 1)	I_{OH} = –5 mA	V_{CC}–2.0			V
			I_{OH} = –1.25 mA	V_{CC}–0.5			V
			I_{OH} = –1.25 mA V_{CC} = 2.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$	I_{OL} = 5 mA			2.0	V
			I_{OL} = 1.25 mA			0.5	V
			I_{OL} = 1.25 mA V_{CC} = 2.5 V			1.0	V
V_{OL}	"L" output voltage	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 1)	I_{OL} = 10 mA			2.0	V
			I_{OL} = 2.5 mA			0.5	V
			I_{OL} = 2.5 mA V_{CC} = 2.5 V			1.0	V
V_{T+} – V_{T-}	Hysteresis	$CNTR_0$, $CNTR_1$, INT_0–INT_3, $P2_0$–$P2_7$			0.5		V
V_{T+} – V_{T-}	Hysteresis	RxD, S_{CLK1}, S_{IN2}, S_{CLK2}			0.5		V
V_{T+} – V_{T-}	Hysteresis	$\overline{RESET}$	$\overline{RESET}$: V_{CC}=2.5 V to 5.5 V		0.5		V
I_{IH}	"H" input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$	V_I = V_{CC} Pull-downs "off"			5.0	µA
			V_{CC}= 5.0 V, V_I = V_{CC} Pull-downs "on"	30	70	140	µA
			V_{CC}= 3.0 V, V_I = V_{CC} Pull-downs "on"	6.0	25	45	µA
I_{IH}	"H" input current	$P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	$\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_0$, $P7_0$				–5.0	µA
I_{IL}	"L" input current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_1$	V_I = V_{SS} Pull-ups "off"			–5.0	µA
			V_{CC}= 5.0 V, V_I = V_{SS} Pull-ups "on"	–30	–70	–140	µA
			V_{CC}= 3.0 V, V_I = V_{SS} Pull-ups "on"	–6	–25	–45	µA
I_{IL}	"L" input current	$\overline{RESET}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current	X_{IN}	V_I = V_{SS}		–4.0		µA
V_{RAM}	RAM hold voltage		When clock is stopped	2.0		5.5	V

Note : When "1" is set to port X_C switch bit (bit 4 of address $003B_{16}$) of CPU mode register, the drive ability of port $P7_0$ is different from the value above mentioned.

EOL announced

ELECTRICAL CHARACTERISTICS (V_{CC} =2.5 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			6.4	13	mA
		• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			1.6	3.2	mA
		• Low-speed mode, V_{CC} = 5V, Ta ≤ 55°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			25	36	µA
		• Low-speed mode, V_{CC} = 5 V, Ta = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			7.0	14.0	µA
		• Low-speed mode, V_{CC} = 3 V, Ta ≤ 55°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			15	22	µA
		• Low-speed mode, V_{CC} = 3V, Ta = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			4.5	9.0	µA
		All oscillation stopped (in STP state) Output transistors “off”	T_a = 25 °C		0.1	1.0	µA
			T_a = 85 °C			10	

EOL announced

TIMING REQUIREMENTS 1 (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	250			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	105			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	105			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width	80			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width	80			ns
$t_{c(S_{CLK1})}$	Serial I/O1 clock input cycle time (Note)	800			ns
$t_{wH(S_{CLK1})}$	Serial I/O1 clock input “H” pulse width (Note)	370			ns
$t_{wL(S_{CLK1})}$	Serial I/O1 clock input “L” pulse width (Note)	370			ns
$t_{su(R_xD-S_{CLK1})}$	Serial I/O1 input set up time	220			ns
$t_{h(S_{CLK1}-R_xD)}$	Serial I/O1 input hold time	100			ns
$t_{c(S_{CLK2})}$	Serial I/O2 clock input cycle time	1000			ns
$t_{wH(S_{CLK2})}$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{wL(S_{CLK2})}$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su(S_{IN2}-S_{CLK2})}$	Serial I/O2 input set up time	200			ns
$t_{h(S_{CLK2}-S_{IN2})}$	Serial I/O2 input hold time	200			ns

Note: When f(X_{IN}) = 8 MHz and bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when f(X_{IN}) = 8 MHz and bit 6 of address $001A_{16}$ is “0” (UART).

TIMING REQUIREMENTS 2 (V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	500/(V_{CC}–2)			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	250/(V_{CC}–2)–20			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	250/(V_{CC}–2)–20			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width	230			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width	230			ns
$t_{c(S_{CLK1})}$	Serial I/O1 clock input cycle time (Note)	2000			ns
$t_{wH(S_{CLK1})}$	Serial I/O1 clock input “H” pulse width (Note)	950			ns
$t_{wL(S_{CLK1})}$	Serial I/O1 clock input “L” pulse width (Note)	950			ns
$t_{su(R_xD-S_{CLK1})}$	Serial I/O1 input set up time	400			ns
$t_{h(S_{CLK1}-R_xD)}$	Serial I/O1 input hold time	200			ns
$t_{c(S_{CLK2})}$	Serial I/O2 clock input cycle time	2000			ns
$t_{wH(S_{CLK2})}$	Serial I/O2 clock input “H” pulse width	950			ns
$t_{wL(S_{CLK2})}$	Serial I/O2 clock input “L” pulse width	950			ns
$t_{su(S_{IN2}-S_{CLK2})}$	Serial I/O2 input set up time	400			ns
$t_{h(S_{CLK2}-S_{IN2})}$	Serial I/O2 input hold time	300			ns

Note: When f(X_{IN}) = 2 MHz and bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when f(X_{IN}) = 2 MHz and bit 6 of address $001A_{16}$ is “0” (UART).

EOL announced

SWITCHING CHARACTERISTICS 1 (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK1)}$	Serial I/O1 clock output “H” pulse width	$t_{C(SCLK1)}$/2–30			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock output “L” pulse width	$t_{C(SCLK1)}$/2–30			ns
$t_{d(SCLK1–TXD)}$	Serial I/O1 output delay time (Note 1)			140	ns
$t_{v(SCLK1–TXD)}$	Serial I/O1 output valid time (Note 1)	–30			ns
$t_{r(SCLK1)}$	Serial I/O1 clock output rising time			30	ns
$t_{f(SCLK1)}$	Serial I/O1 clock output falling time			30	ns
$t_{WH(SCLK2)}$	Serial I/O2 clock output “H” pulse width	$t_{C(SCLK2)}$/2–160			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock output “L” pulse width	$t_{C(SCLK2)}$/2–160			ns
$t_{d(SCLK2–SOUT2)}$	Serial I/O2 output delay time			0.2X$t_{C(SCLK2)}$	ns
$t_{v(SCLK2–SOUT2)}$	Serial I/O2 output valid time	0			ns
$t_{f(SCLK2)}$	Serial I/O2 clock output falling time			40	ns
$t_{r(CMOS)}$	CMOS output rising time (Note 2)		10	30	ns
$t_{f(CMOS)}$	CMOS output falling time (Note 2)		10	30	ns

Notes1: When the P45/TXD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is “0”.
2: XOUT and XCOUT pins are excluded.

SWITCHING CHARACTERISTICS 2 (V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK1)}$	Serial I/O1 clock output “H” pulse width	$t_{C(SCLK1)}$/2–50			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock output “L” pulse width	$t_{C(SCLK1)}$/2–50			ns
$t_{d(SCLK1–TXD)}$	Serial I/O1 output delay time (Note 1)			350	ns
$t_{v(SCLK1–TXD)}$	Serial I/O1 output valid time (Note 1)	–30			ns
$t_{r(SCLK1)}$	Serial I/O1 clock output rising time			50	ns
$t_{f(SCLK1)}$	Serial I/O1 clock output falling time			50	ns
$t_{WH(SCLK2)}$	Serial I/O2 clock output “H” pulse width	$t_{C(SCLK2)}$/2–240			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock output “L” pulse width	$t_{C(SCLK2)}$/2–240			ns
$t_{d(SCLK2–SOUT2)}$	Serial I/O2 output delay time			0.2X$t_{C(SCLK2)}$	ns
$t_{v(SCLK2–SOUT2)}$	Serial I/O2 output valid time	0			ns
$t_{f(SCLK2)}$	Serial I/O2 clock output falling time			50	ns
$t_{r(CMOS)}$	CMOS output rising time (Note 2)		20	50	ns
$t_{f(CMOS)}$	CMOS output falling time (Note 2)		20	50	ns

Notes1: When the P45/TXD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is “0”.
2: XOUT and XCOUT pins are excluded.

Not announced

ABSOLUTE MAXIMUM RATINGS (Extended Operating Temperature Version)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$		–0.3 to V_{CC} +0.3	V
V_I	Input voltage V_{L1}		–0.3 to V_{L2}	V
V_I	Input voltage V_{L2}		V_{L1} to V_{L3}	V
V_I	Input voltage V_{L3}		V_{L2} to V_{CC} +0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$	At output port	–0.3 to V_{CC} +0.3	V
		At segment output	–0.3 to V_{L3} +0.3	V
V_O	Output voltage $P3_0$–$P3_7$	At segment output	–0.3 to V_{L3} +0.3	V
V_O	Output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$		–0.3 to V_{CC} +0.3	V
V_O	Output voltage SEG_0–SEG_{15}		–0.3 to V_{L3} +0.3	V
V_O	Output voltage X_{OUT}		–0.3 to V_{CC} +0.3	V
Pd	Power dissipation	T_a = 25 °C	300	mW
Topr	Operating temperature		–40 to 85	°C
Tstg	Storage temperature		–65 to 150	°C

RECOMMENDED OPERATING CONDITIONS (Extended Operating Temperature Version)

(V_{CC} = 3.0 to 5.5 V, T_a = –40 to –20 °C and V_{CC} = 2.5 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter			Limits			Unit
				Min.	Typ.	Max.	
V_{CC}	Power source voltage	High-speed mode f(X_{IN})=8 MHz		4.0	5.0	5.5	V
		Middle-speed mode f(X_{IN})=8 MHz	T_a = –20 to 85 °C	2.5	5.0	5.5	
			T_a = –40 to –20 °C	3.0	5.0	5.5	
		Low-speed mode	T_a = –20 to 85 °C	2.5	5.0	5.5	
			T_a = –40 to –20 °C	3.0	5.0	5.5	
V_{SS}	Power source voltage				0		V
V_{IH}	“H” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_1$, $P4_5$, $P4_7$, $P5_1$, $P5_3$, $P5_6$, $P6_1$, $P7_0$, $P7_1$ (CM_4=0)		0.7 V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$P2_0$–$P2_7$, $P4_2$–$P4_4$, $P4_6$, $P5_0$, $P5_2$, $P5_4$, $P5_5$, $P5_7$, $P6_0$		0.8 V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$\overline{RESET}$		0.8 V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	X_{IN}		0.8 V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_0$, $P4_1$, $P4_5$, $P4_7$, $P5_1$, $P5_3$, $P5_6$, $P6_1$, $P7_0$, $P7_1$ (CM_4=0)		0		0.3 V_{CC}	V
V_{IL}	“L” input voltage	$P2_0$–$P2_7$, $P4_2$–$P4_4$, $P4_6$, $P5_0$, $P5_2$, $P5_4$, $P5_5$, $P5_7$, $P6_0$		0		0.2 V_{CC}	V
V_{IL}	“L” input voltage	$\overline{RESET}$		0		0.2 V_{CC}	V
V_{IL}	“L” input voltage	X_{IN}		0		0.2 V_{CC}	V

EOL announced

RECOMMENDED OPERATING CONDITIONS (Extended Operating Temperature Version)

(V_{CC} = 3.0 to 5.5 V, T_a = –40 to –20 °C and V_{CC} = 2.5 to 5.5 V, T_a = –20 to 85 °C unless otherwise noted.)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (Note 1)			–40	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 1)			–40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (Note 1)			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 1)			40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (Note 1)			–20	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 1)			–20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (Note 1)			20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 1)			20	mA
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 2)			–5	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ (Note 2)			5	mA
$I_{OL(peak)}$	"L" peak output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 2)			10	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ (Note 3)			–1.0	mA
$I_{OH(avg)}$	"H" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 3)			–2.5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ (Note 3)			2.5	mA
$I_{OL(avg)}$	"L" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 3)			5.0	mA
$f(CNTR_0)$ $f(CNTR_1)$	Clock input frequency for timers X and Y (duty cycle 50 %)	4.0 V ≤ V_{CC} ≤ 5.5 V			4.0	MHz
		V_{CC} ≤ 4.0 V			$(2 \times V_{CC})-4$	MHz
$f(X_{IN})$	Main clock input oscillation frequency (Note 4)	High-speed mode (4.0 V ≤ V_{CC} ≤ 5.5 V)			8.0	MHz
		High-speed mode (V_{CC} ≤ 4.0 V)			$(4 \times V_{CC})-8$	MHz
		Middle-speed mode			8.0	MHz
$f(X_{CIN})$	Sub-clock input oscillation frequency (Note 4, 5)			32.768	50	kHz

Notes **1:** The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2: The peak output current is the peak current flowing in each port.
3: The average output current is an average value measured over 100 ms.
4: When the oscillation frequency has a duty cycle of 50 %.
5: When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency $f(X_{CIN})$ is less than $f(X_{IN})/3$.

EOL announced

ELECTRICAL CHARACTERISTICS (Extended Operating Temperature Version)

(V_{CC} =2.5 to 5.5 V, T_a = –20 to 85 °C, and V_{CC} =3.0 to 5.5 V, T_a = –40 to –20 °C, unless otherwise noted.)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$	I_{OH} = –2.5 mA	V_{CC}–2.0			V
			I_{OH} = –0.6 mA V_{CC} = 3.0 V	V_{CC}–0.9			V
V_{OH}	"H" output voltage	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note)	I_{OH} = –5 mA	V_{CC}–2.0			V
			I_{OH} = –1.25 mA	V_{CC}–0.5			V
			I_{OH} = –1.25 mA V_{CC} = 3.0 V	V_{CC}–0.9			V
V_{OL}	"L" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$	I_{OL} = 5 mA			2.0	V
			I_{OL} = 1.25 mA			0.5	V
			I_{OL} = 1.25 mA V_{CC} = 3.0 V			1.1	V
V_{OL}	"L" output voltage	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note)	I_{OL} = 10 mA			2.0	V
			I_{OL} = 2.5 mA			0.5	V
			I_{OL} = 2.5 mA V_{CC} = 3.0 V			1.1	V
V_{T+} – V_{T-}	Hysteresis	$CNTR_0$, $CNTR_1$, INT_0–INT_3, $P2_0$–$P2_7$			0.5		V
V_{T+} – V_{T-}	Hysteresis	RxD, S_{CLK1}, S_{IN2}, S_{CLK2}			0.5		V
V_{T+} – V_{T-}	Hysteresis	$\overline{RESET}$	$\overline{RESET}$: V_{CC}=3.0 V to 5.5 V		0.5		V
I_{IH}	"H" input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$	V_I = V_{CC} Pull-downs "off"			5.0	µA
			V_{CC}= 5.0 V, V_I = V_{CC} Pull-downs "on"	30	70	170	µA
			V_{CC}= 3.0 V, V_I = V_{CC} Pull-downs "on"	6.0	25	55	µA
I_{IH}	"H" input current	$P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	$\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_0$, $P7_0$				–5.0	µA
I_{IL}	"L" input current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_1$	V_I = V_{SS} Pull-ups "off"			–5.0	µA
			V_{CC}= 5.0 V, V_I = V_{SS} Pull-ups "on"	–30	–70	–140	µA
			V_{CC}= 3.0 V, V_I = V_{SS} Pull-ups "on"	–6	–25	–45	µA
I_{IL}	"L" input current	$\overline{RESET}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current	X_{IN}	V_I = V_{SS}		–4.0		µA
V_{RAM}	RAM hold voltage		When clock is stopped	2.0		5.5	V

Note : When "1" is set to port X_C switch bit (bit 4 of address $003B_{16}$) of CPU mode register, the drive ability of port $P7_0$ is different from the value above mentioned.

EOL announced

ELECTRICAL CHARACTERISTICS (Extended Operating Temperature Version)

(V_{CC} =3.0 to 5.5 V, T_a = –40 to –20 °C and V_{CC} =2.5 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			6.4	13	mA
		• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			1.6	3.2	mA
		• Low-speed mode, V_{CC} = 5V, Ta ≤ 55°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			25	36	µA
		• Low-speed mode, V_{CC} = 5 V, Ta = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			7.0	14.0	µA
		• Low-speed mode, V_{CC} = 3 V, Ta ≤ 55°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			15	22	µA
		• Low-speed mode, V_{CC} = 3V, Ta = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			4.5	9.0	µA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	

EOL announced

TIMING REQUIREMENTS 1 (Extended Operating Temperature Version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –40 to 85 °C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	250			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	105			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	105			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width	80			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width	80			ns
$t_{c(S_{CLK1})}$	Serial I/O1 clock input cycle time (Note)	800			ns
$t_{wH(S_{CLK1})}$	Serial I/O1 clock input “H” pulse width (Note)	370			ns
$t_{wL(S_{CLK1})}$	Serial I/O1 clock input “L” pulse width (Note)	370			ns
$t_{su(R_{XD}–S_{CLK1})}$	Serial I/O1 input set up time	220			ns
$t_{h(S_{CLK1}–R_{XD})}$	Serial I/O1 input hold time	100			ns
$t_{c(S_{CLK2})}$	Serial I/O2 clock input cycle time	1000			ns
$t_{wH(S_{CLK2})}$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{wL(S_{CLK2})}$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su(S_{IN2}–S_{CLK2})}$	Serial I/O2 input set up time	200			ns
$t_{h(S_{CLK2}–S_{IN2})}$	Serial I/O2 input hold time	200			ns

Note: When f(X_{IN}) = 8 MHz and bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when f(X_{IN}) = 8 MHz and bit 6 of address $001A_{16}$ is “0” (UART).

TIMING REQUIREMENTS 2 (Extended Operating Temperature Version)

(V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, and V_{CC} = 3.0 to 4.0 V, V_{SS} = 0 V, T_a = –40 to –20 °C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	500/ (V_{CC}–2)			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	250/ (V_{CC}–2)–20			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	250/ (V_{CC}–2)–20			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width	230			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width	230			ns
$t_{c(S_{CLK1})}$	Serial I/O1 clock input cycle time (Note)	2000			ns
$t_{wH(S_{CLK1})}$	Serial I/O1 clock input “H” pulse width (Note)	950			ns
$t_{wL(S_{CLK1})}$	Serial I/O1 clock input “L” pulse width (Note)	950			ns
$t_{su(R_{XD}–S_{CLK1})}$	Serial I/O1 input set up time	400			ns
$t_{h(S_{CLK1}–R_{XD})}$	Serial I/O1 input hold time	200			ns
$t_{c(S_{CLK2})}$	Serial I/O2 clock input cycle time	2000			ns
$t_{wH(S_{CLK2})}$	Serial I/O2 clock input “H” pulse width	950			ns
$t_{wL(S_{CLK2})}$	Serial I/O2 clock input “L” pulse width	950			ns
$t_{su(S_{IN2}–S_{CLK2})}$	Serial I/O2 input set up time	400			ns
$t_{h(S_{CLK2}–S_{IN2})}$	Serial I/O2 input hold time	300			ns

Note: When f(X_{IN}) = 2 MHz and bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when f(X_{IN}) = 2 MHz and bit 6 of address $001A_{16}$ is “0” (UART).

RE.announced

SWITCHING CHARACTERISTICS 1 (Extended Operating Temperature Version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –40 to 85 °C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK1)}$	Serial I/O1 clock output “H” pulse width	$t_{C(SCLK1)}$/2–30			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock output “L” pulse width	$t_{C(SCLK1)}$/2–30			ns
$t_{d(SCLK1–TXD)}$	Serial I/O1 output delay time (Note 1)			140	ns
$t_{v(SCLK1–TXD)}$	Serial I/O1 output valid time (Note 1)	–30			ns
$t_{r(SCLK1)}$	Serial I/O1 clock output rising time			30	ns
$t_{f(SCLK1)}$	Serial I/O1 clock output falling time			30	ns
$t_{WH(SCLK2)}$	Serial I/O2 clock output “H” pulse width	$t_{C(SCLK2)}$/2–160			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock output “L” pulse width	$t_{C(SCLK2)}$/2–160			ns
$t_{d(SCLK2–SOUT2)}$	Serial I/O2 output delay time			0.2×$t_{C(SCLK2)}$	ns
$t_{v(SCLK2–SOUT2)}$	Serial I/O2 output valid time	0			ns
$t_{f(SCLK2)}$	Serial I/O2 clock output falling time			40	ns
$t_{r(CMOS)}$	CMOS output rising time (Note 2)		10	30	ns
$t_{f(CMOS)}$	CMOS output falling time (Note 2)		10	30	ns

Notes1: When the P45/TXD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is “0”.
2: XOUT and XCOUT pins are excluded.

SWITCHING CHARACTERISTICS 2 (Extended Operating Temperature Version)

(V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, and V_{CC} = 3.0 to 4.0 V, T_a = –40 to –20 °C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK1)}$	Serial I/O1 clock output “H” pulse width	$t_{C(SCLK1)}$/2–50			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock output “L” pulse width	$t_{C(SCLK1)}$/2–50			ns
$t_{d(SCLK1–TXD)}$	Serial I/O1 output delay time (Note 1)			350	ns
$t_{v(SCLK1–TXD)}$	Serial I/O1 output valid time (Note 1)	–30			ns
$t_{r(SCLK1)}$	Serial I/O1 clock output rising time			50	ns
$t_{f(SCLK1)}$	Serial I/O1 clock output falling time			50	ns
$t_{WH(SCLK2)}$	Serial I/O2 clock output “H” pulse width	$t_{C(SCLK2)}$/2–240			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock output “L” pulse width	$t_{C(SCLK2)}$/2–240			ns
$t_{d(SCLK2–SOUT2)}$	Serial I/O2 output delay time			0.2×$t_{C(SCLK2)}$	ns
$t_{v(SCLK2–SOUT2)}$	Serial I/O2 output valid time	0			ns
$t_{f(SCLK2)}$	Serial I/O2 clock output falling time			50	ns
$t_{r(CMOS)}$	CMOS output rising time (Note 2)		20	50	ns
$t_{f(CMOS)}$	CMOS output falling time (Note 2)		20	50	ns

Notes1: When the P45/TXD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is “0”.
2: XOUT and XCOUT pins are excluded.

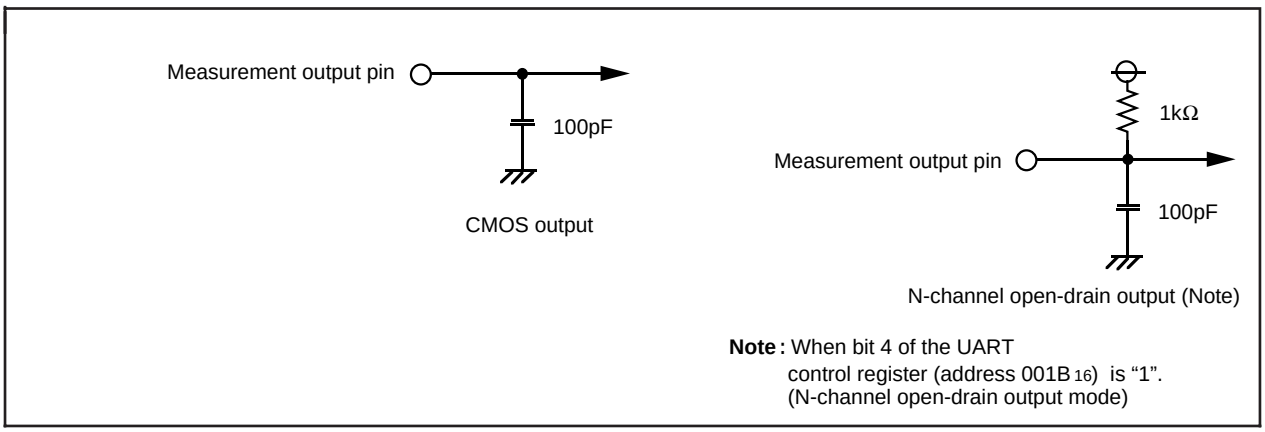


Fig.40 Circuit for measuring output switching characteristics

Not announced

ABSOLUTE MAXIMUM RATINGS (Low Power Source Voltage Version)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$		–0.3 to V_{CC} +0.3	V
V_I	Input voltage V_{L1}		–0.3 to V_{L2}	V
V_I	Input voltage V_{L2}		V_{L1} to V_{L3}	V
V_I	Input voltage V_{L3}		V_{L2} to V_{CC} +0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$	At output port	–0.3 to V_{CC} +0.3	V
		At segment output	–0.3 to V_{L3} +0.3	V
V_O	Output voltage $P3_0$–$P3_7$	At segment output	–0.3 to V_{L3} +0.3	V
V_O	Output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$		–0.3 to V_{CC} +0.3	V
V_O	Output voltage SEG_0–SEG_{15}		–0.3 to V_{L3} +0.3	V
V_O	Output voltage X_{OUT}		–0.3 to V_{CC} +0.3	V
Pd	Power dissipation	T_a = 25 °C	300	mW
Topr	Operating temperature		–20 to 85	°C
Tstg	Storage temperature		–40 to 150	°C

RECOMMENDED OPERATING CONDITIONS (Low Power Source Voltage Version)

(V_{CC} = 2.2 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage	High-speed mode f(X_{IN})=8 MHz	4.0	5.0	5.5	V
		Middle-speed mode f(X_{IN})=8 MHz	2.2	5.0	5.5	
		Low-speed mode	2.2	5.0	5.5	
V_{SS}	Power source voltage			0		V
V_{IH}	“H” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_1$, $P4_5$, $P4_7$, $P5_1$, $P5_3$, $P5_6$, $P6_1$, $P7_0$, $P7_1$ (CM_4=0)	0.7 V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$P2_0$–$P2_7$, $P4_2$–$P4_4$, $P4_6$, $P5_0$, $P5_2$, $P5_4$, $P5_5$, $P5_7$, $P6_0$	0.8 V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$\overline{RESET}$	0.8 V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	X_{IN}	0.8 V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_0$, $P4_1$, $P4_5$, $P4_7$, $P5_1$, $P5_3$, $P5_6$, $P6_1$, $P7_0$, $P7_1$ (CM_4=0)	0		0.3 V_{CC}	V
V_{IL}	“L” input voltage	$P2_0$–$P2_7$, $P4_2$–$P4_4$, $P4_6$, $P5_0$, $P5_2$, $P5_4$, $P5_5$, $P5_7$, $P6_0$	0		0.2 V_{CC}	V
V_{IL}	“L” input voltage	$\overline{RESET}$	0		0.2 V_{CC}	V
V_{IL}	“L” input voltage	X_{IN}	0		0.2 V_{CC}	V

EOL announced

RECOMMENDED OPERATING CONDITIONS (Low Power Source Voltage Version)

(V_{CC} = 2.2 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (Note 1)			–40	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 1)			–40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (Note 1)			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 1)			40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (Note 1)			–20	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 1)			–20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ (Note 1)			20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 1)			20	mA
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 2)			–5	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ (Note 2)			5	mA
$I_{OL(peak)}$	"L" peak output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 2)			10	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ (Note 3)			–1.0	mA
$I_{OH(avg)}$	"H" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 3)			–2.5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ (Note 3)			2.5	mA
$I_{OL(avg)}$	"L" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note 3)			5.0	mA
$f(CNTR_0)$ $f(CNTR_1)$	Clock input frequency for timers X and Y (duty cycle 50 %)	4.0 V ≤ V_{CC} ≤ 5.5 V			4.0	MHz
		V_{CC} ≤ 4.0 V			$\frac{(10 \times V_{CC}-4)}{9}$	MHz
$f(X_{IN})$	Main clock input oscillation frequency (Note 4)	High-speed mode (4.0 V ≤ V_{CC} ≤ 5.5 V)			8.0	MHz
		High-speed mode (V_{CC} ≤ 4.0 V)			$\frac{(20 \times V_{CC}-8)}{9}$	MHz
		Middle-speed mode			8.0	MHz
$f(X_{CIN})$	Sub-clock input oscillation frequency (Note 4, 5)			32.768	50	kHz

Notes **1:** The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2: The peak output current is the peak current flowing in each port.
3: The average output current is an average value measured over 100 ms.
4: When the oscillation frequency has a duty cycle of 50 %.
5: When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency $f(X_{CIN})$ is less than $f(X_{IN})/3$.

EOL announced

ELECTRICAL CHARACTERISTICS (Low Power Source Voltage Version)

(V_{CC} =4.0 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$	I_{OH} = –0.1 mA	V_{CC}–2.0			V
			I_{OH} = –25 µA V_{CC} = 2.2 V	V_{CC}–1.0			V
V_{OH}	"H" output voltage	$P2_0$–$P2_7$, $P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note)	I_{OH} = –5 mA	V_{CC}–2.0			V
			I_{OH} = –1.25 mA	V_{CC}–0.5			V
			I_{OH} = –1.25 mA V_{CC} = 2.2 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$	I_{OL} = 5 mA			2.0	V
			I_{OL} = 1.25 mA			0.5	V
			I_{OL} = 1.25 mA V_{CC} = 2.2 V			1.1	V
V_{OL}	"L" output voltage	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$ (Note)	I_{OL} = 10 mA			2.0	V
			I_{OL} = 2.5 mA			0.5	V
			I_{OL} = 2.5 mA V_{CC} = 2.2 V			1.0	V
V_{T+} – V_{T-}	Hysteresis	$CNTR_0$, $CNTR_1$, INT_0–INT_3, $P2_0$–$P2_7$			0.5		V
V_{T+} – V_{T-}	Hysteresis	RxD, S_{CLK1}, S_{IN2}, S_{CLK2}			0.5		V
V_{T+} – V_{T-}	Hysteresis	$\overline{RESET}$	$\overline{RESET}$: V_{CC}=2.2 V to 5.5 V		0.5		V
I_{IH}	"H" input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$	V_I = V_{CC} Pull-downs "off"			5.0	µA
			V_{CC}= 5.0 V, V_I = V_{CC} Pull-downs "on"	30	70	170	µA
			V_{CC}= 3.0 V, V_I = V_{CC} Pull-downs "on"	6.0	25	55	µA
I_{IH}	"H" input current	$P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_0$, $P7_1$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	$\overline{RESET}$	V_I = V_{CC}		8.0	5.0	µA
I_{IH}	"H" input current	X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_0$, $P7_0$				–5.0	µA
I_{IL}	"L" input current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_1$	V_I = V_{SS} Pull-ups "off"			–5.0	µA
			V_{CC}= 5.0 V, V_I = V_{SS} Pull-ups "on"	–30	–70	–140	µA
			V_{CC}= 3.0 V, V_I = V_{SS} Pull-ups "on"	–6	–25	–45	µA
I_{IL}	"L" input current	$\overline{RESET}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current	X_{IN}	V_I = V_{SS}		–8.0		µA

Note : When "1" is set to port X_C switch bit (bit 4 of address $003B_{16}$) of CPU mode register, the drive ability of port $P7_0$ is different from the value above mentioned.

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ELECTRICAL CHARACTERISTICS (Low Power Source Voltage Version)

(V_{CC} =2.2 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{RAM}	RAM hold voltage	When clock is stopped	2.0		5.5	V
I_{CC}	Power source current	• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”		6.4	13	mA
		• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off”		1.6	3.2	mA
		• Low-speed mode, V_{CC} = 5V, $T_a \leq 55°C$ $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”		25	36	µA
		• Low-speed mode, V_{CC} = 5 V, T_a = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”		7.0	14.0	µA
		• Low-speed mode, V_{CC} = 3 V, $T_a \leq 55°C$ $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”		15	22	µA
		• Low-speed mode, V_{CC} = 3V, T_a = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”		4.5	9.0	µA
		All oscillation stopped (in STP state) Output transistors “off” — T_a = 25 °C		0.2	2.0	µA
		All oscillation stopped (in STP state) Output transistors “off” — T_a = 85 °C			20	µA

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TIMING REQUIREMENTS 1 (Low Power Source Voltage Version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	250			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	105			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	105			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width	80			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width	80			ns
$t_{c(S_{CLK1})}$	Serial I/O1 clock input cycle time (Note)	800			ns
$t_{wH(S_{CLK1})}$	Serial I/O1 clock input “H” pulse width (Note)	370			ns
$t_{wL(S_{CLK1})}$	Serial I/O1 clock input “L” pulse width (Note)	370			ns
$t_{su(R_{XD}–S_{CLK1})}$	Serial I/O1 input set up time	220			ns
$t_{h(S_{CLK1}–R_{XD})}$	Serial I/O1 input hold time	100			ns
$t_{c(S_{CLK2})}$	Serial I/O2 clock input cycle time	1000			ns
$t_{wH(S_{CLK2})}$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{wL(S_{CLK2})}$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su(S_{IN2}–S_{CLK2})}$	Serial I/O2 input set up time	200			ns
$t_{h(S_{CLK2}–S_{IN2})}$	Serial I/O2 input hold time	200			ns

Note: When f(X_{IN}) = 8 MHz and bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when f(X_{IN}) = 8 MHz and bit 6 of address $001A_{16}$ is “0” (UART).

TIMING REQUIREMENTS 2 (Low Power Source Voltage Version)

(V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock iuput cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	900/ (V_{CC}–0.4)			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	450/ (V_{CC}–0.4)–20			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	450/ (V_{CC}–0.4)–20			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width	230			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width	230			ns
$t_{c(S_{CLK1})}$	Serial I/O1 clock input cycle time (Note)	2000			ns
$t_{wH(S_{CLK1})}$	Serial I/O1 clock input “H” pulse width (Note)	950			ns
$t_{wL(S_{CLK1})}$	Serial I/O1 clock input “L” pulse width (Note)	950			ns
$t_{su(R_{XD}–S_{CLK1})}$	Serial I/O1 input set up time	400			ns
$t_{h(S_{CLK1}–R_{XD})}$	Serial I/O1 input hold time	200			ns
$t_{c(S_{CLK2})}$	Serial I/O2 clock input cycle time	2000			ns
$t_{wH(S_{CLK2})}$	Serial I/O2 clock input “H” pulse width	950			ns
$t_{wL(S_{CLK2})}$	Serial I/O2 clock input “L” pulse width	950			ns
$t_{su(S_{IN2}–S_{CLK2})}$	Serial I/O2 input set up time	400			ns
$t_{h(S_{CLK2}–S_{IN2})}$	Serial I/O2 input hold time	300			ns

Note: When f(X_{IN}) = 2 MHz and bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when f(X_{IN}) = 2 MHz and bit 6 of address $001A_{16}$ is “0” (UART).

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SWITCHING CHARACTERISTICS 1 (Low Power Source Voltage Version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK1)}$	Serial I/O1 clock output “H” pulse width	$t_{C(SCLK1)}$/2–30			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock output “L” pulse width	$t_{C(SCLK1)}$/2–30			ns
$t_{d(SCLK1-TXD)}$	Serial I/O1 output delay time (Note 1)			140	ns
$t_{v(SCLK1-TXD)}$	Serial I/O1 output valid time (Note 1)	–30			ns
$t_{r(SCLK1)}$	Serial I/O1 clock output rising time			30	ns
$t_{f(SCLK1)}$	Serial I/O1 clock output falling time			30	ns
$t_{WH(SCLK2)}$	Serial I/O2 clock output “H” pulse width	$t_{C(SCLK2)}$/2–160			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock output “L” pulse width	$t_{C(SCLK2)}$/2–160			ns
$t_{d(SCLK2-SOUT2)}$	Serial I/O2 output delay time			0.2×$t_{C(SCLK2)}$	ns
$t_{v(SCLK2-SOUT2)}$	Serial I/O2 output valid time	0			ns
$t_{f(SCLK2)}$	Serial I/O2 clock output falling time			40	ns
$t_{r(CMOS)}$	CMOS output rising time (Note 2)		10	30	ns
$t_{f(CMOS)}$	CMOS output falling time (Note 2)		10	30	ns

Notes 1: When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is “0”.
2: XOUT and XCOUT pins are excluded.

SWITCHING CHARACTERISTICS 2 (Low Power Source Voltage Version)

(V_{CC} = 2.2 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK1)}$	Serial I/O1 clock output “H” pulse width	$t_{C(SCLK1)}$/2–50			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock output “L” pulse width	$t_{C(SCLK1)}$/2–50			ns
$t_{d(SCLK1-TXD)}$	Serial I/O1 output delay time (Note 1)			350	ns
$t_{v(SCLK1-TXD)}$	Serial I/O1 output valid time (Note 1)	–30			ns
$t_{r(SCLK1)}$	Serial I/O1 clock output rising time			50	ns
$t_{f(SCLK1)}$	Serial I/O1 clock output falling time			50	ns
$t_{WH(SCLK2)}$	Serial I/O2 clock output “H” pulse width	$t_{C(SCLK2)}$/2–240			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock output “L” pulse width	$t_{C(SCLK2)}$/2–240			ns
$t_{d(SCLK2-SOUT2)}$	Serial I/O2 output delay time			0.2×$t_{C(SCLK2)}$	ns
$t_{v(SCLK2-SOUT2)}$	Serial I/O2 output valid time	0			ns
$t_{f(SCLK2)}$	Serial I/O2 clock output falling time			50	ns
$t_{r(CMOS)}$	CMOS output rising time (Note 2)		20	50	ns
$t_{f(CMOS)}$	CMOS output falling time (Note 2)		20	50	ns

Notes 1: When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is “0”.
2: XOUT and XCOUT pins are excluded.

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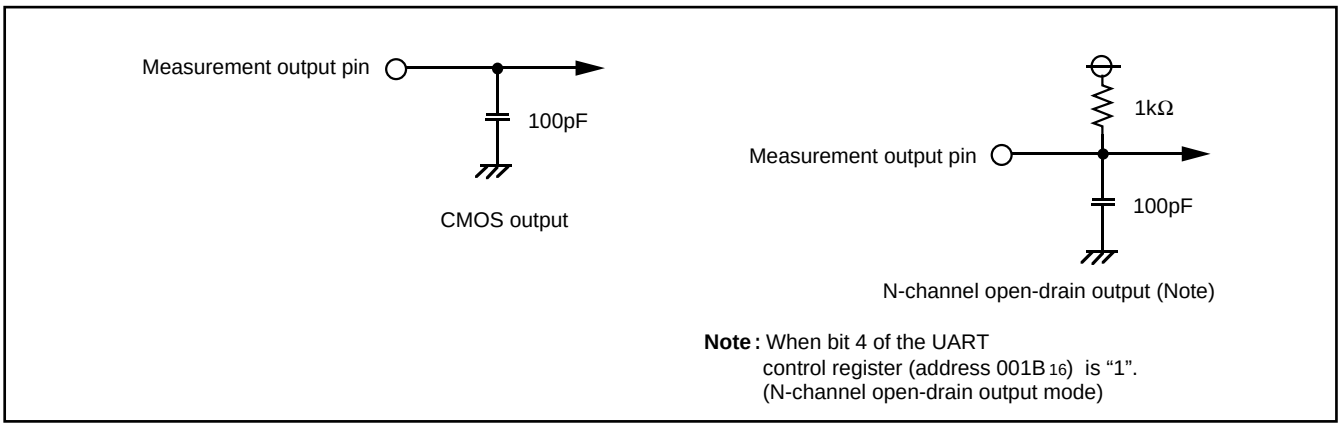
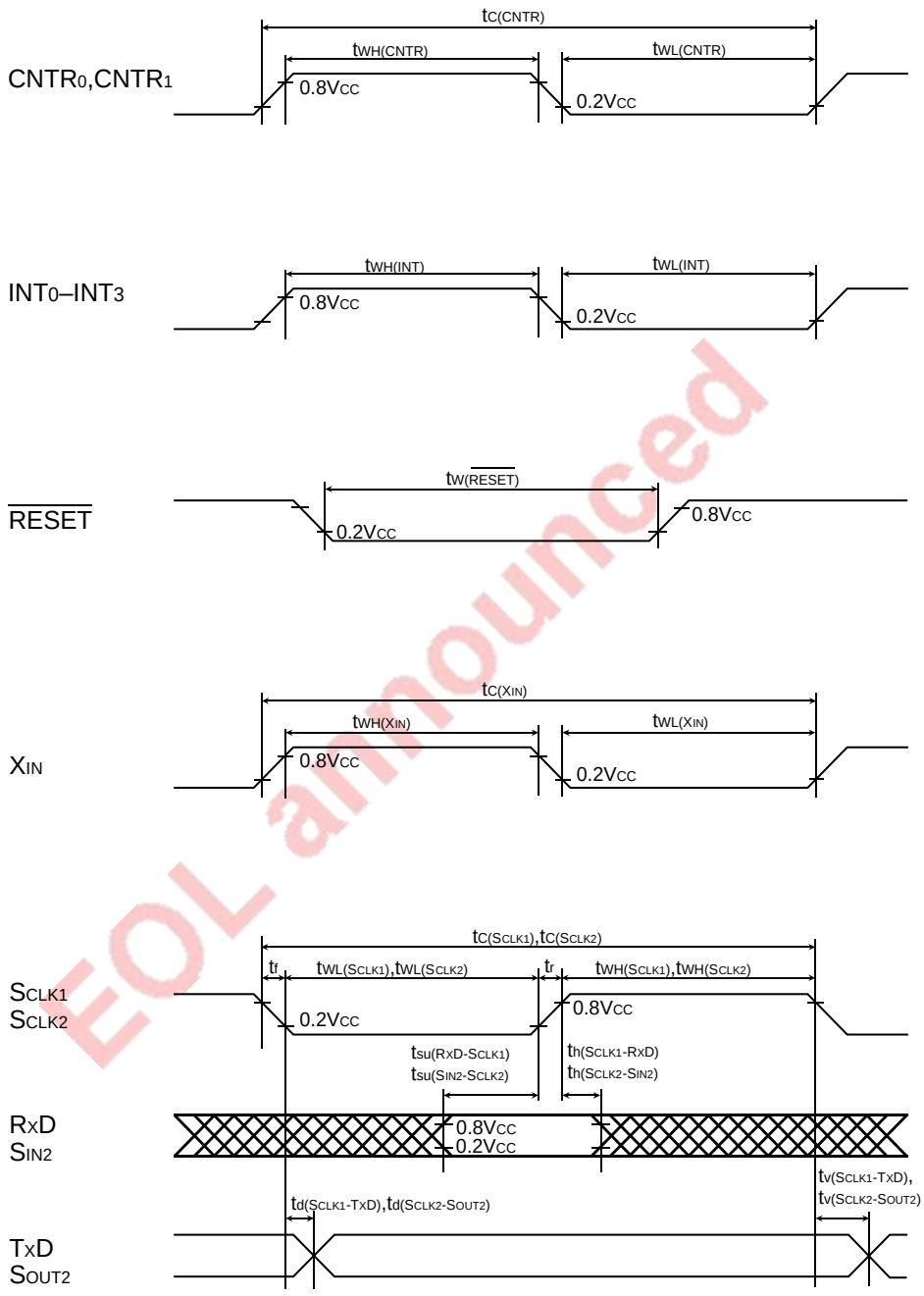


Fig.41 Circuit for measuring output switching characteristics

TIMING DIAGRAM



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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

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