M2VD-2HL

MPEG-2 Video Decoder for 1080p Single Stream or 1080i Dual Stream

Silicon Image's M2VD-2HL* is designed to be used in system-on-a-chip solutions for DVD and STB/DTV markets. With its extensive set of features M2VD-2HL enables companies to easily provide functions like parallel viewing and recording, picture-in-picture or simultaneous viewing of several channels in television, PC or other relevant environments. The M2VD-2HL decoder is optimized to satisfy a wide range of applications and technologies with optimal performance at lowest possible silicon costs. Its interfaces are optimized for easy integration into a System-on-Chip architecture using the standard on-chip bus approach. This dramatically reduces the integration effort and enables fast time-to-market developments.

Features

- ISO/IEC 13818-2 - MPEG-2 Main Profile @ High Level
- ISO/IEC 11172-2 - MPEG-1 constrained parameter set
- Support of all ATSC and DVB HDTV formats
- Real-time decoding of multiple streams only limited by frequency.
- Error detection and autonomous error concealment with concealment vectors on slice, macroblock and block layer
- Counter for concealed MBs within a picture and threshold register which indicates the level of interrupt generation
- Software access to relevant internal registers and parameter stores to provide the possibility of a flexible error handling and a robust and error tolerant decoding control
- Decoding of Packetized Elementary Stream (PES) and Elementary Stream (ES)

Applications

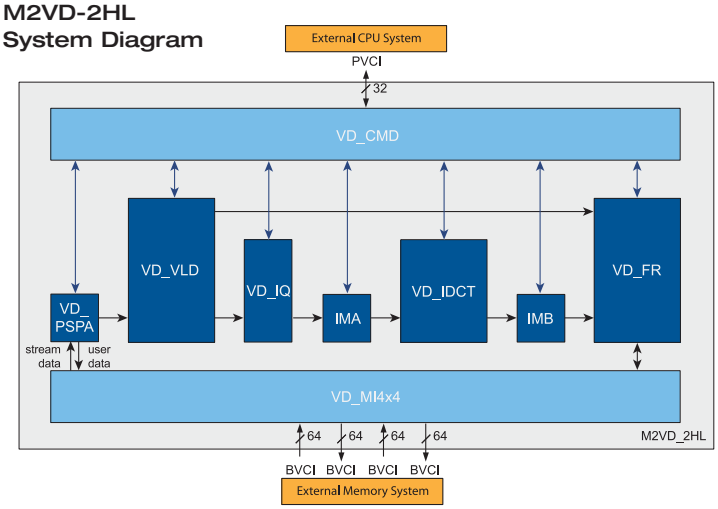
- **Set-top boxes**
- **Digital TV sets and IPTV applications**
- **DVD players and recorders**
- **Portable multimedia players**
- **Surveillance**

Key Features

- **Supports MPEG-1/2 to 1080p @ 60 fps**
- **Full bit rate support up to 80 Mbps**
- **Small gate count reduces chip area**
- **Only one IRQ per picture to external host**

*M2VD-2HL was formerly part of the sci-worx GmbH product portfolio. Silicon Image acquired sci-worx in January 2007.

M2VD-2HL System Diagram



M2VD-2HL Gate Count and RAM Size Estimation

Sub-Modules	Gate Count	Memory	
		Single-ported	Two ported
VD Pipeline	69K	64x32	2x64x32
		128x26	2x64x12
		32x34	96x36
VD_M14x4	70K		96x64
			48x64
			200x96

Gate = 2 Input-NAND equivalent, using TSMC 0.13 µm process and standard cell libraries

M2VD-2HL Features

Real-time decoding of multiple streams only limited by frequency

For example:

- Six streams MP@ML (PAL or NTSC) @ 133 MHz in a typical system
- One stream MP@HL (HDTV / 1080i) @ 133 MHz in a typical system
- Two streams MP@HL (HDTV / 1080i) @ 266 MHz in a typical system
- One stream MP@HL (HDTV / 1080p) @ 266 MHz in a typical system

PES Parser (VD_PSPA)

The VD_PSPA reads the transmitted Packetized Elementary Stream (PES) from memory interface (VD_MI4x4) and extracts the enclosed video Elementary Stream (ES) data from each PES payload section. All extracted ES data is passed to the variable length decoder (VD_VLD). Presentation Time Stamps (PTS), which are used for video synchronization during picture presentation, are collected from PES. Further on, the exact position of a picture header in the external stream buffer is detected. This can be used for trick mode, etc.

Variable Length Decoder (VD_VLD)

The VD_VLD scans the incoming video bit stream for synchronization and decoding. This stream has a multilayer syntax. On higher layers, general information about the current video sequence is transmitted in a fixed length code. Depending on this information, the data of a picture is decoded on macro block and block layer from the variable length code of the stream. Concealment vectors are derived from the stream and stored internally. They are used for picture reconstruction from a corrupted stream.

Inverse Quantization (VD_IQ)

The inverse quantization is performed block oriented in an 8x8 matrix in default or alternate scan order regarding the MPEG-1 and MPEG-2 standard. Quantizer weighting matrices from higher stream layers are stored in a RAM to be used for inverse quantization.

Inverse Discrete Cosine Transformation (VD_IDCT)

After a block of coefficients has been de-quantized, the VD_IDCT unit performs the two dimensional IDCT on the 8x8 block to form a reconstructed image block. A transposition RAM is used for storing interim results.

Frame Reconstruction (VD_FR)

The frame reconstruction process forms prediction values from previously decoded pictures which are added to the transmitted difference values (output of VD_IDCT via intermediate memory) to recover the final decoded pels of a picture. The location of the values in previously decoded pictures depends on the specified prediction type and the motion vectors. A shared RAM is used for the reconstruction process.

Command Interface (VD_CMD)

The system processor has transparent access to all relevant internal registers and parameter stores via the command interface. The built-in control logic of the VD_CMD allows control over the video decoder by a well defined and powerful set of instructions.

Memory Interface (VD_MI4x4)

The high performance memory interface contains buffers for stream data, user data, video data write and reference data read. The buffers, together with a four by four pixel mapping of the reference data, allow efficient burst access to a system memory (e.g. DDR2 SDRAM) via four 64-bit BVCI interfaces. The reference data read port copes with pipelined latencies of more than 100 clock cycles without impact on the decoding performance.

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