Parallel NOR Flash Embedded Memory

M29W256GH, M29W256GL

Features

- Supply voltage
  - V_{CC} = 2.7–3.6V (program, erase, read)
  - V_{CCQ} = 1.65–3.6V (I/O buffers)
  - V_{PPH} = 12V for fast program (optional)
- Asynchronous random/page read
  - Page size: 8words or 16 bytes
  - Page access: 25, 30ns
  - Random access: 60ns[1], 70, 80ns
- Fast program commands: 32-word (64-byte) write buffer
- Enhanced buffered program commands: 256-word
- Program time
  - 16µs per byte/word TYP
  - Chip program time: 10s with V_{PPH} and 16s without V_{PPH}
- Memory organization
  - Uniform blocks: 256 main blocks, 128-Kbytes or 64-Kwords each
- Program/erase controller
  - Embedded byte/word program algorithms
- Program/erase suspend and resume capability
  - Read from any block during a PROGRAM SUSPEND operation
  - Read or program another block during an ERASE SUSPEND operation
- Unlock bypass, block erase, chip erase, write to buffer and program
  - Fast buffered/batch programming
  - Fast block/chip erase
- V_{PP}/WP# pin protection
  - Protects first or last block regardless of block protection settings
- Software protection
  - Volatile protection
  - Nonvolatile protection
  - Password protection
- Extended memory block
  - 128-word (256-byte) memory block for permanent, secure identification
  - Programmed or locked at the factory or by the customer
- Common flash interface
  - 64-bit security code
- Low power consumption: Standby and automatic mode
- JESD47H-compliant
  - 100,000 minimum PROGRAM/ERASE cycles per block
  - Data retention: 20 years (TYP)
- 65nm single-level cell (SLC) process technology
- Fortified BGA, TBGA, and TSOP packages
- Green packages available
  - RoHS-compliant
  - Halogen-free
- Automotive device grade (6): temperature –40°C to +85°C (automotive grade certified)
- Automotive device grade (3): temperature –40°C to +125°C (automotive grade certified)

Note: 1. The 60ns device is available upon customer request.

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Part Numbering Information

Available with extended memory block prelocked by Micron. Devices are shipped from the factory with memory content bits erased to 1. For available options, such as packages or high/low protection, or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Table 1: Part Number Information

Part Number Category	Category Details	Notes
Device Type	M29W	
Operating Voltage	W = VCC = 2.7 to 3.6V	
Device function	256GH = 256Mb (x8/x16) page, uniform block Flash memory, highest block protected by V_{PP}/WP#	
	256GL = 256Mb (x8/x16) page, uniform block Flash memory, lowest block protected by V_{PP}/WP#	
Speed	70 = 70ns	1
	60 = 60ns	1, 2
	7A = 70ns	1, 3
Package	N = 56-pin TSOP, 14mm x 20mm, lead-free, halogen-free, RoHS-compliant	
	ZA = 64-pin TBGA, 10mm x 13mm, lead-free, halogen-free, RoHS-compliant	
	ZS = 64-pin Fortified BGA, 11mm x 13mm	
Temperature Range	1 = 0 to 70°C	
	6 = –40°Cto +85°C	
	3 = –40°C to +125°C	
Shipping Options	E = RoHS-compliant package, standard packing	
	F = RoHS-compliant package, tape and reel packing	

Notes:
1. 80ns if VCCQ = 1.65V to VCC.
2. The 60ns device is available upon customer request.
3. Automotive qualified, available only with option 6. Qualified and characterized according to AEC Q100 and Q003 or equivalent; advanced screening according to AEC Q001 and Q002 or equivalent.

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General Description

The M29W is an asynchronous, uniform block, parallel NOR Flash memory device manufactured on 65nm single-level cell (SLC) technology. READ, ERASE, and PROGRAM operations are performed using a single low-voltage supply. Upon power-up, the device defaults to read array mode.

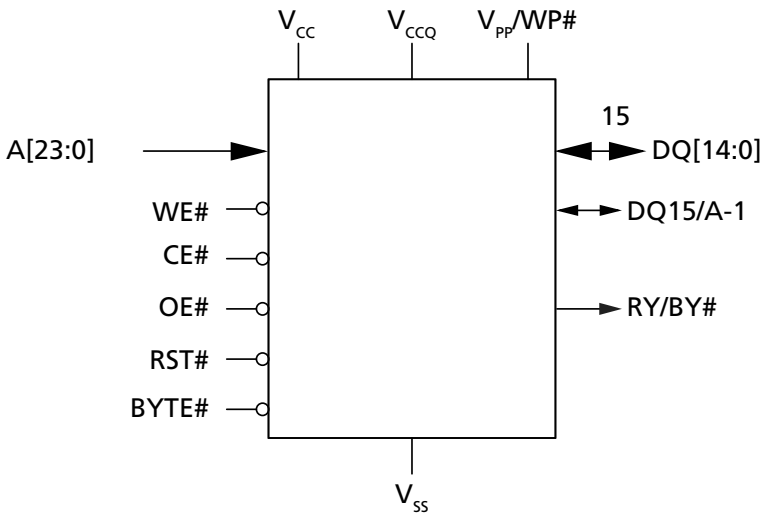
The main memory array is divided into uniform blocks that can be erased independently so that valid data can be preserved while old data is purged. PROGRAM and ERASE commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all special operations required to update the memory contents. The end of a PROGRAM or ERASE operation can be detected and any error condition can be identified. The command set required to control the device is consistent with JEDEC standards.

CE#, OE#, and WE# control the bus operation of the device and enable a simple connection to most microprocessors, often without additional logic.

The M29W supports asynchronous random read and page read from all blocks of the array. It features a write to buffer program capability that improves throughput by programming a buffer of 32 words in one command sequence. Also, in x16 mode, the enhanced buffered program capability improves throughput by programming 256 words in one command sequence. The device V_{PP}/WP# signal enables faster programming.

The device contains a 128-word (x16) and 256-byte (x8) extended memory block. The user can program this additional space and then protect it to permanently secure the contents. The device also features different levels of hardware and software protection to secure blocks from unwanted modification.

Figure 1: Logic Diagram



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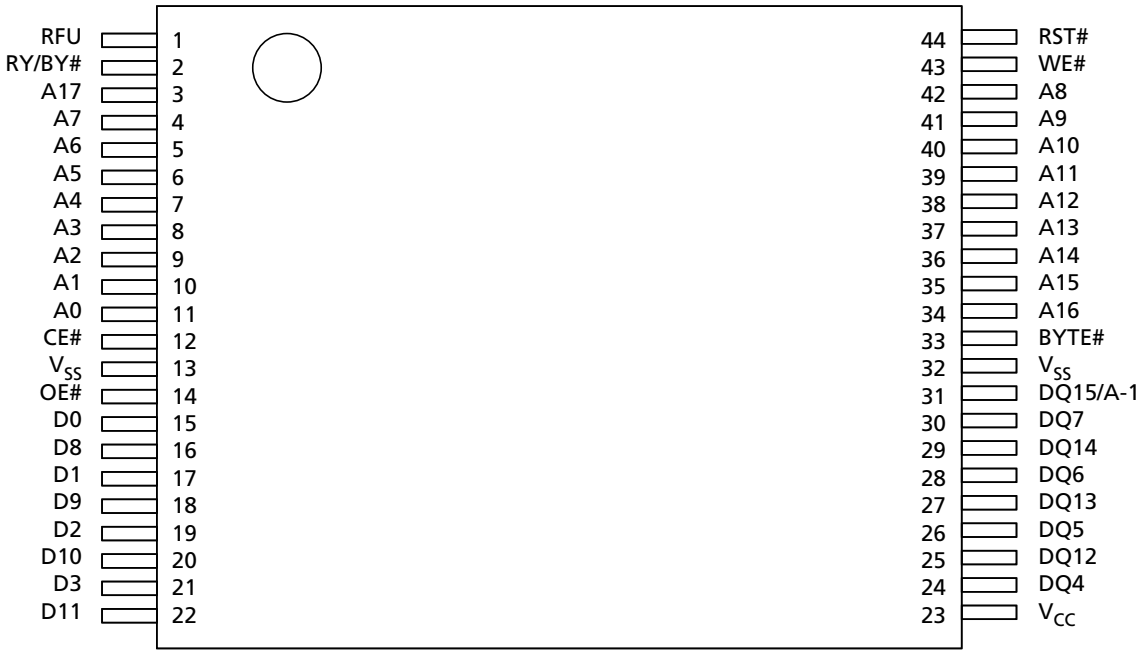
Signal Assignments

Figure 2: 44-Pin SO (Top View)



Notes:
1. A17 = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

Figure 3: 44-Pin SO (Top View)

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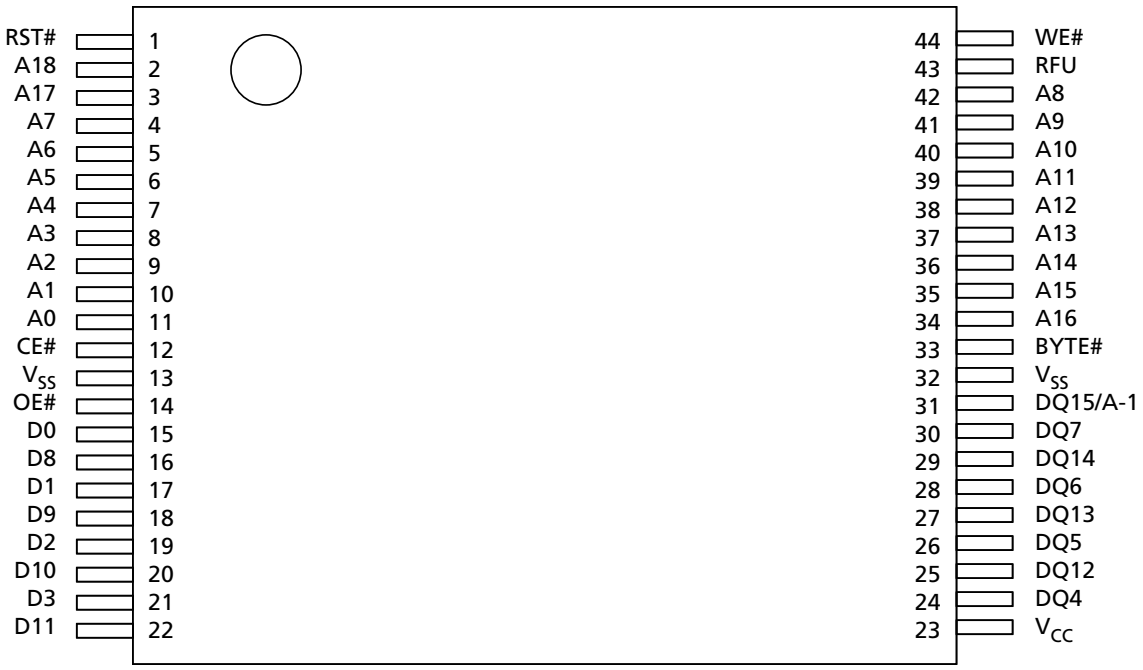
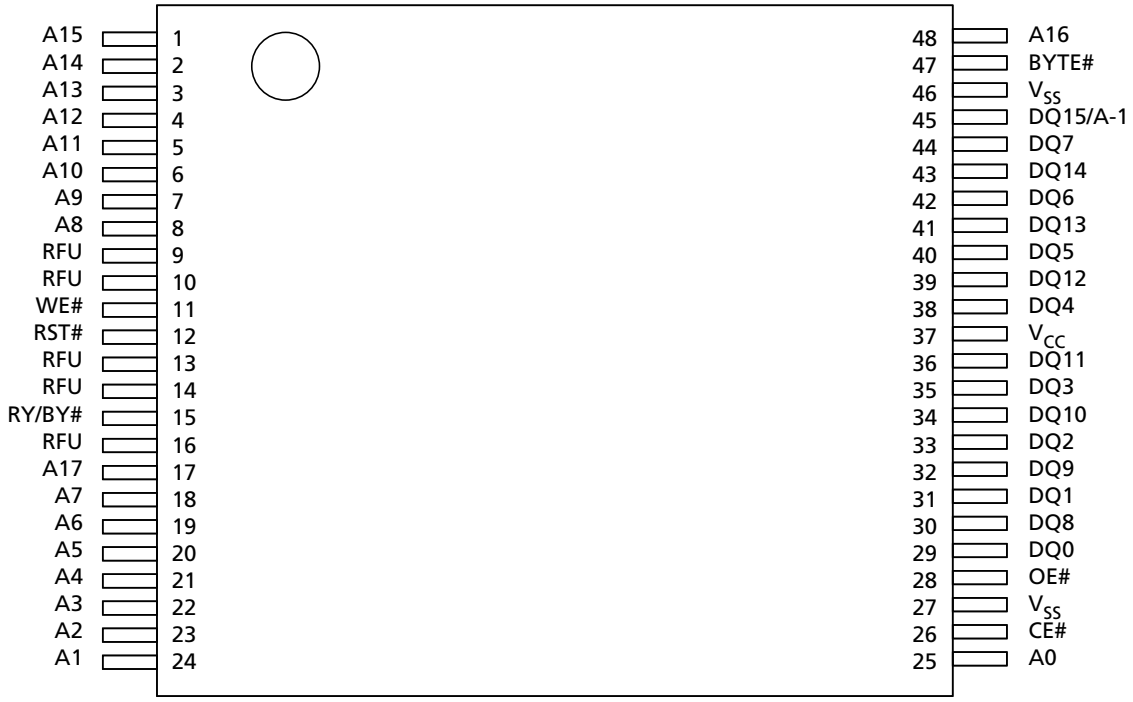


Notes: 1. A18 = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

Figure 4: 48-Pin TSOP (Top View)



Notes: 1. A17 = A[MAX].

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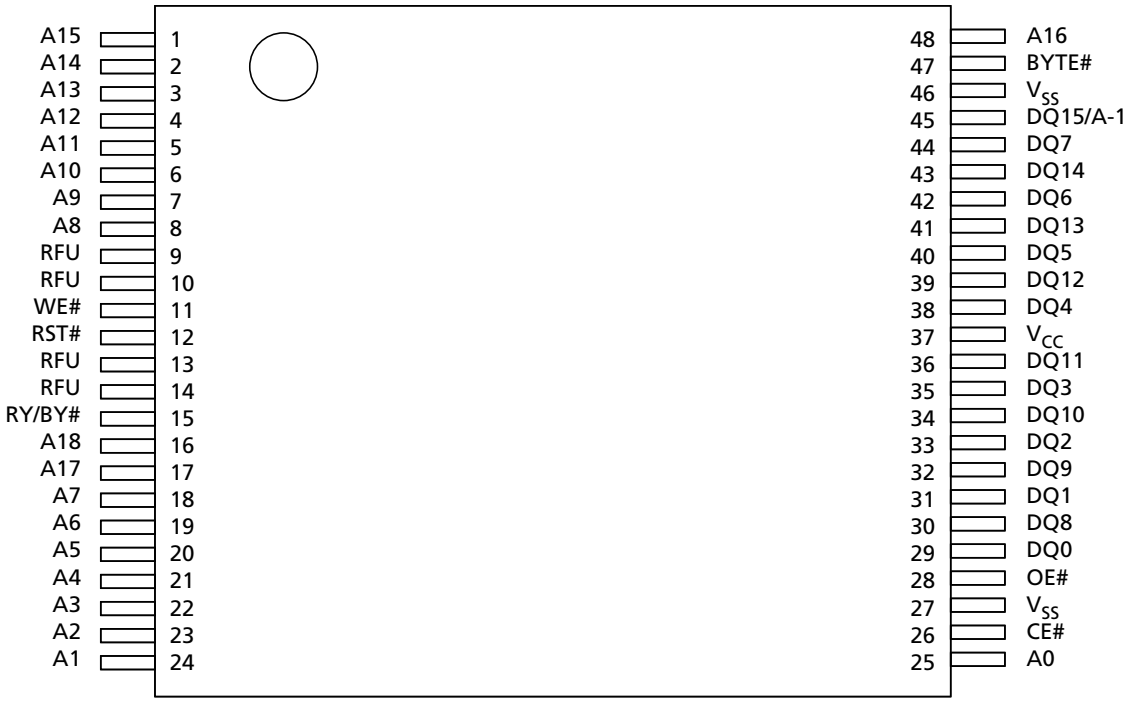
2. A-1 is the least significant address bit in x8 mode.

Figure 5: 48-Pin TSOP (Top View)



Notes: 1. A18 = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

Figure 6: 48-Pin TSOP (Top View)

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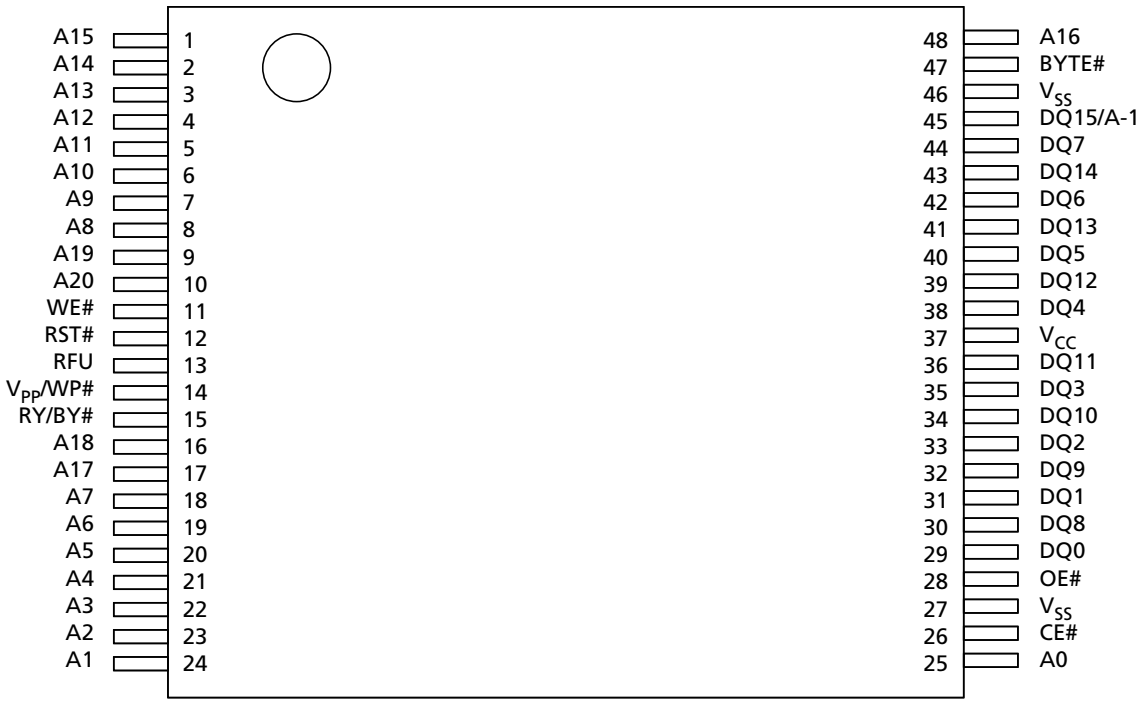
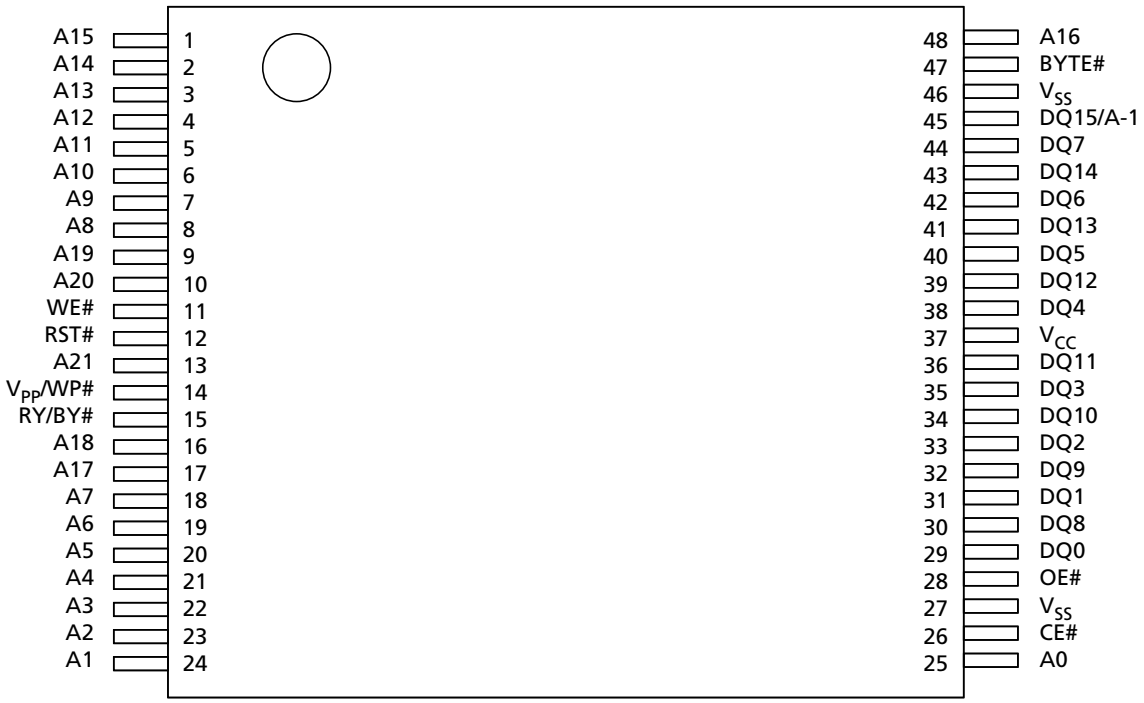


Notes: 1. A20 = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

Figure 7: 48-Pin TSOP (Top View)



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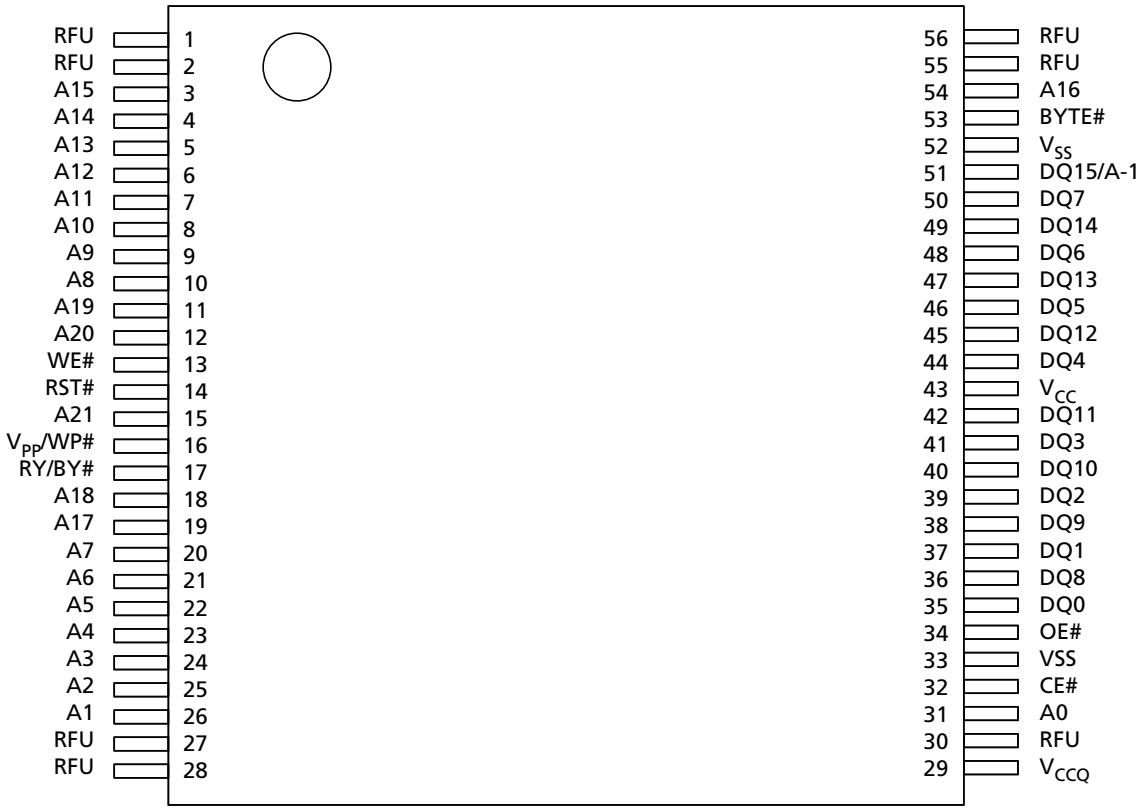
Notes: 1. A21 = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

Figure 8: 56-Pin TSOP (Top View)



Notes: 1. A21 = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

Figure 9: 56-Pin TSOP (Top View)

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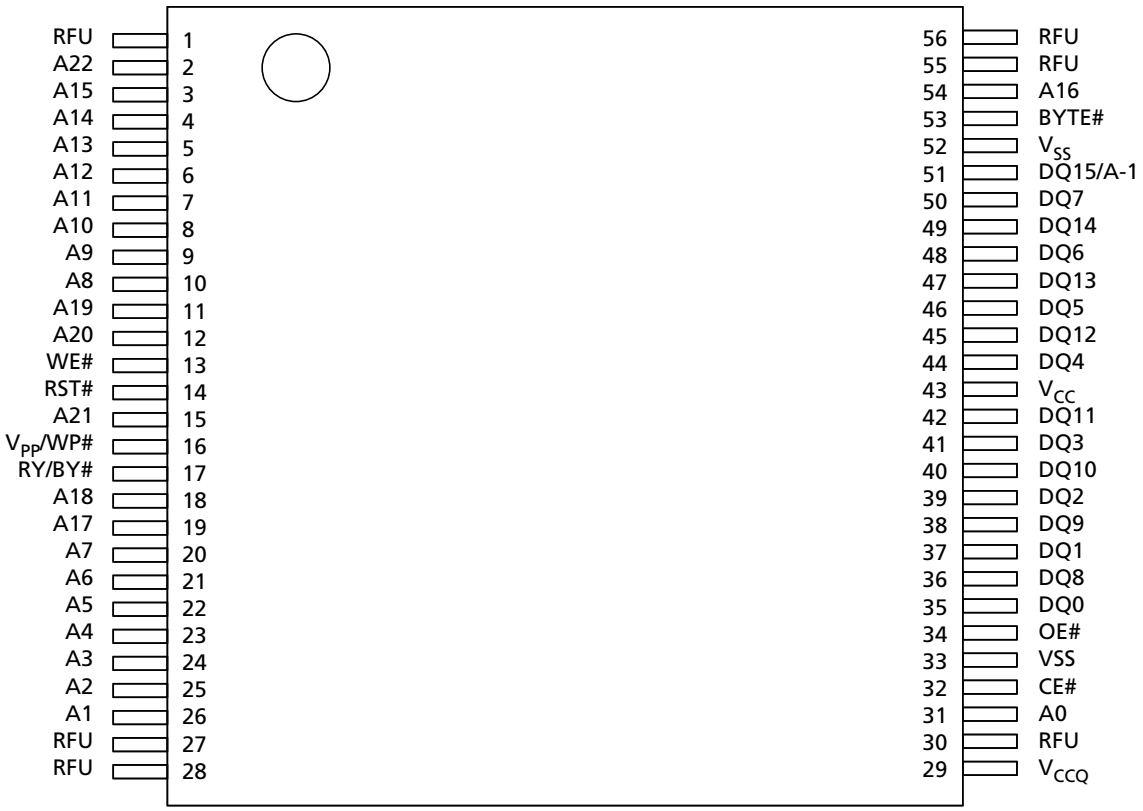

Notes: 1. A22 = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

Figure 10: 56-Pin TSOP (Top View)

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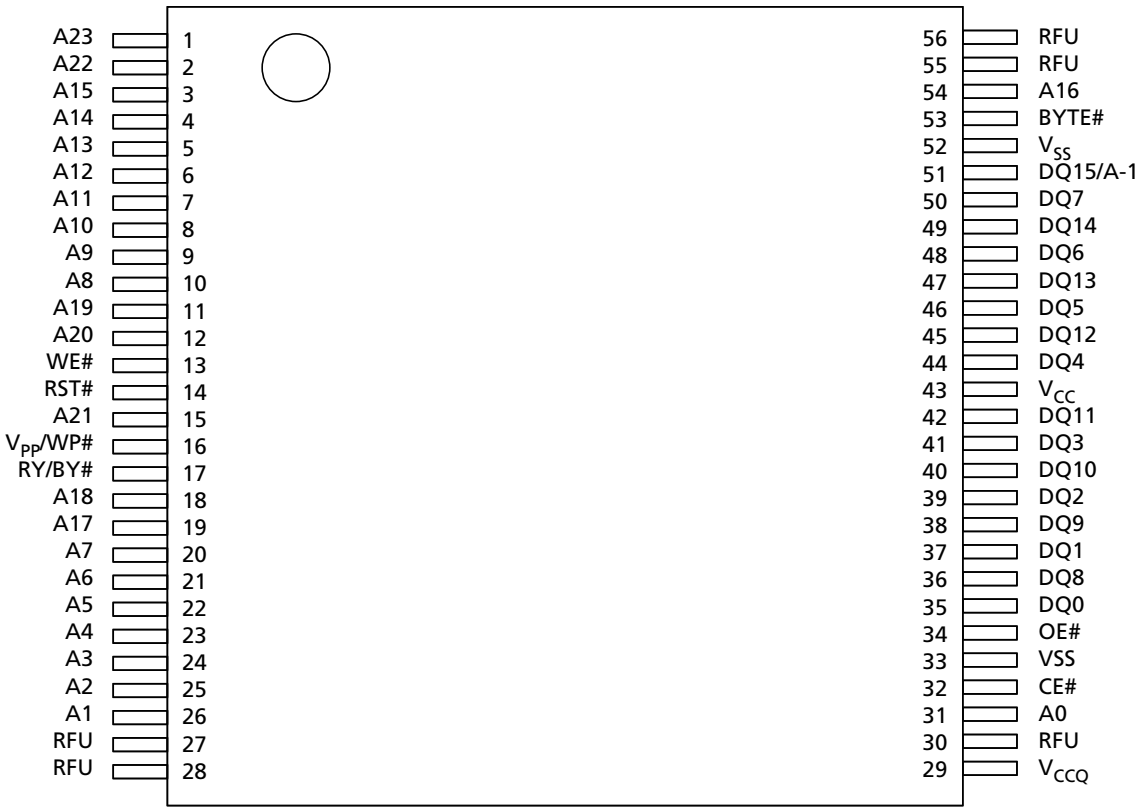

Notes:
1. A23 = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

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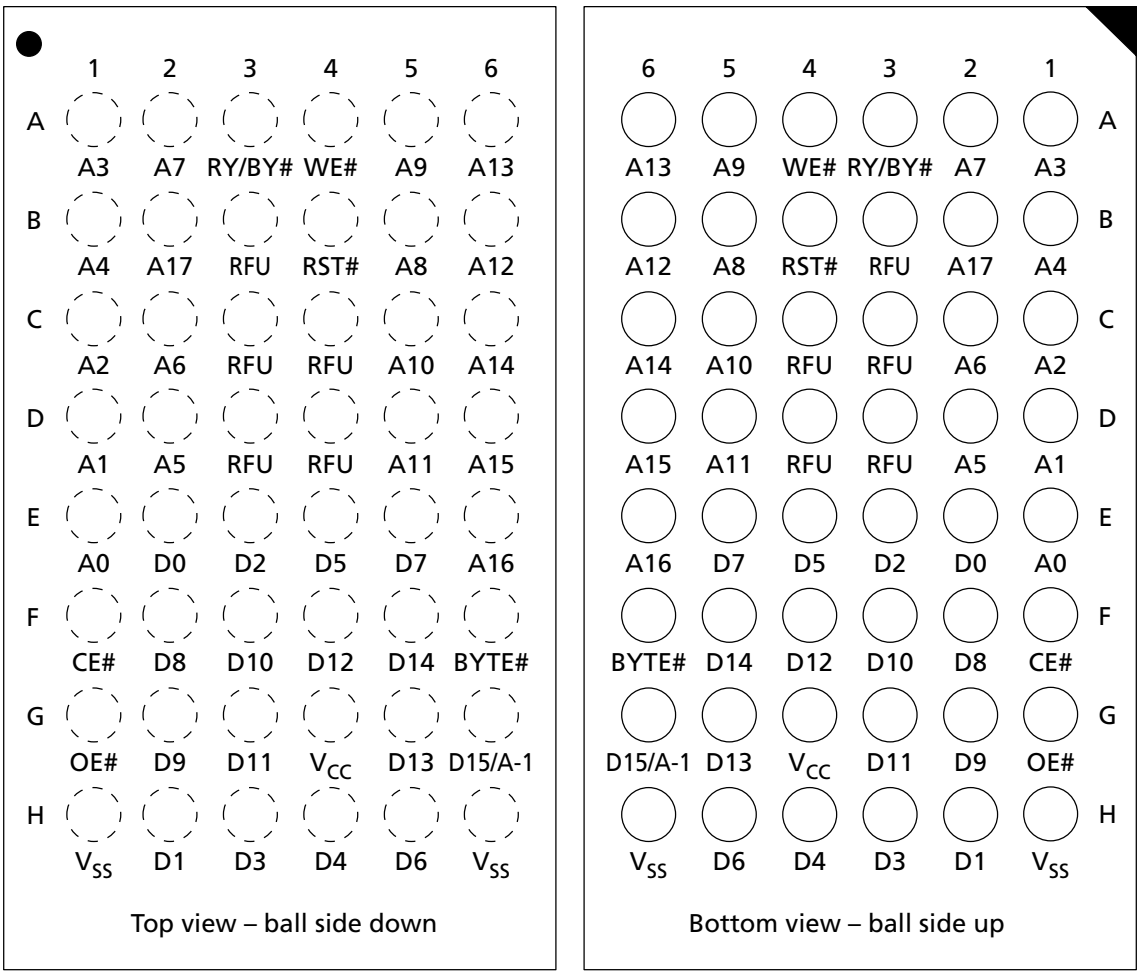
Figure 11: 48-Ball Fortified BGA and 48-Ball TBGA



Notes:
1. A[17] = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

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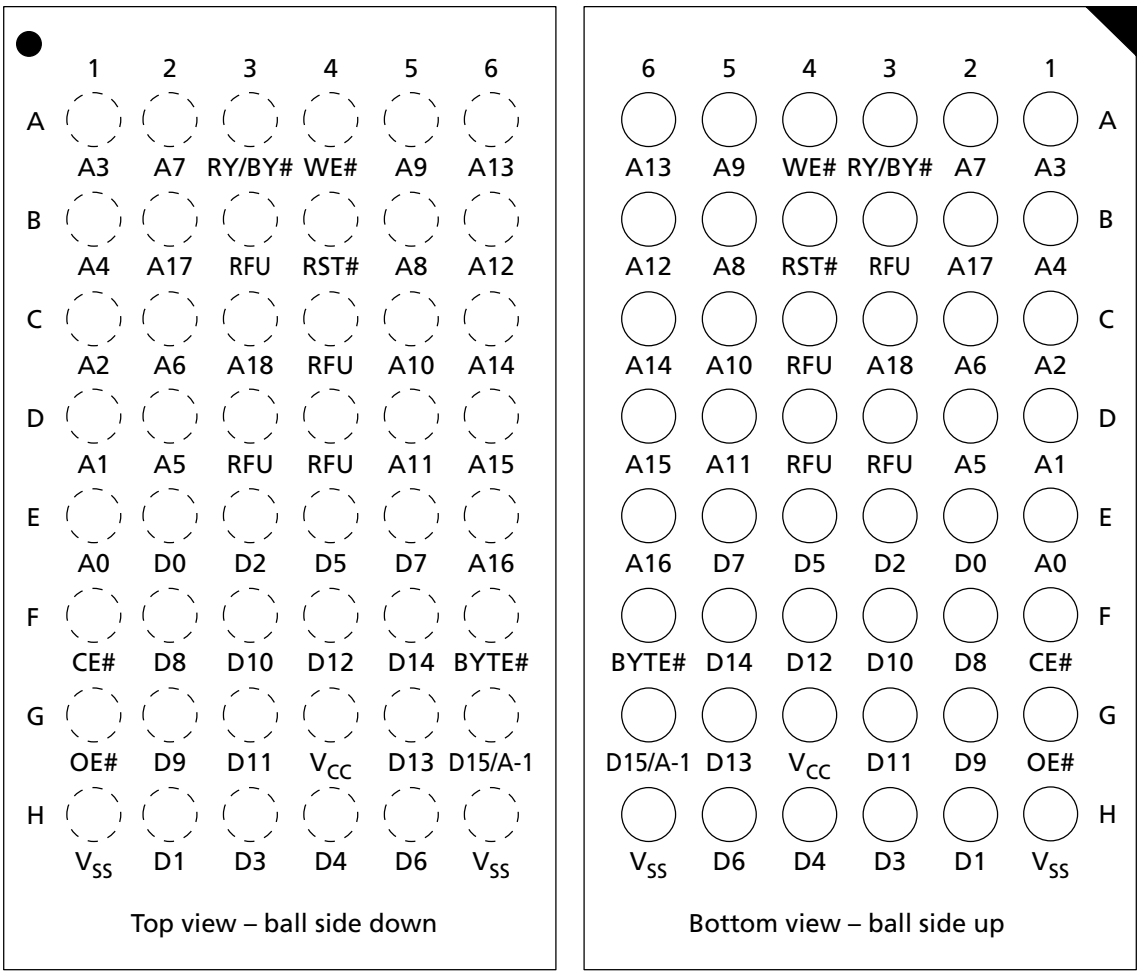
Figure 12: 48-Ball Fortified BGA and 48-Ball TBGA



Notes:
1. A[18] = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

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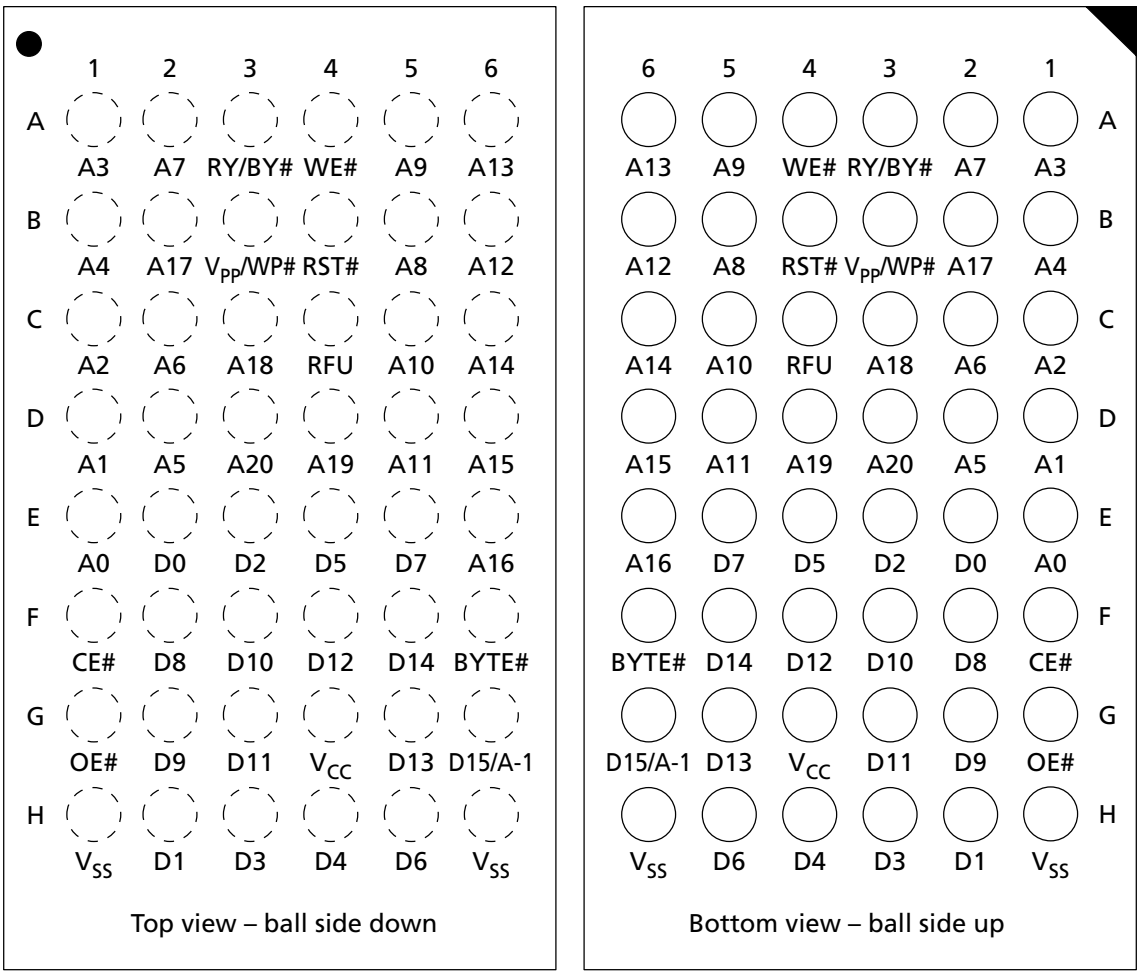
Figure 13: 48-Ball Fortified BGA and 48-Ball TBGA



Notes:
1. A[20] = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

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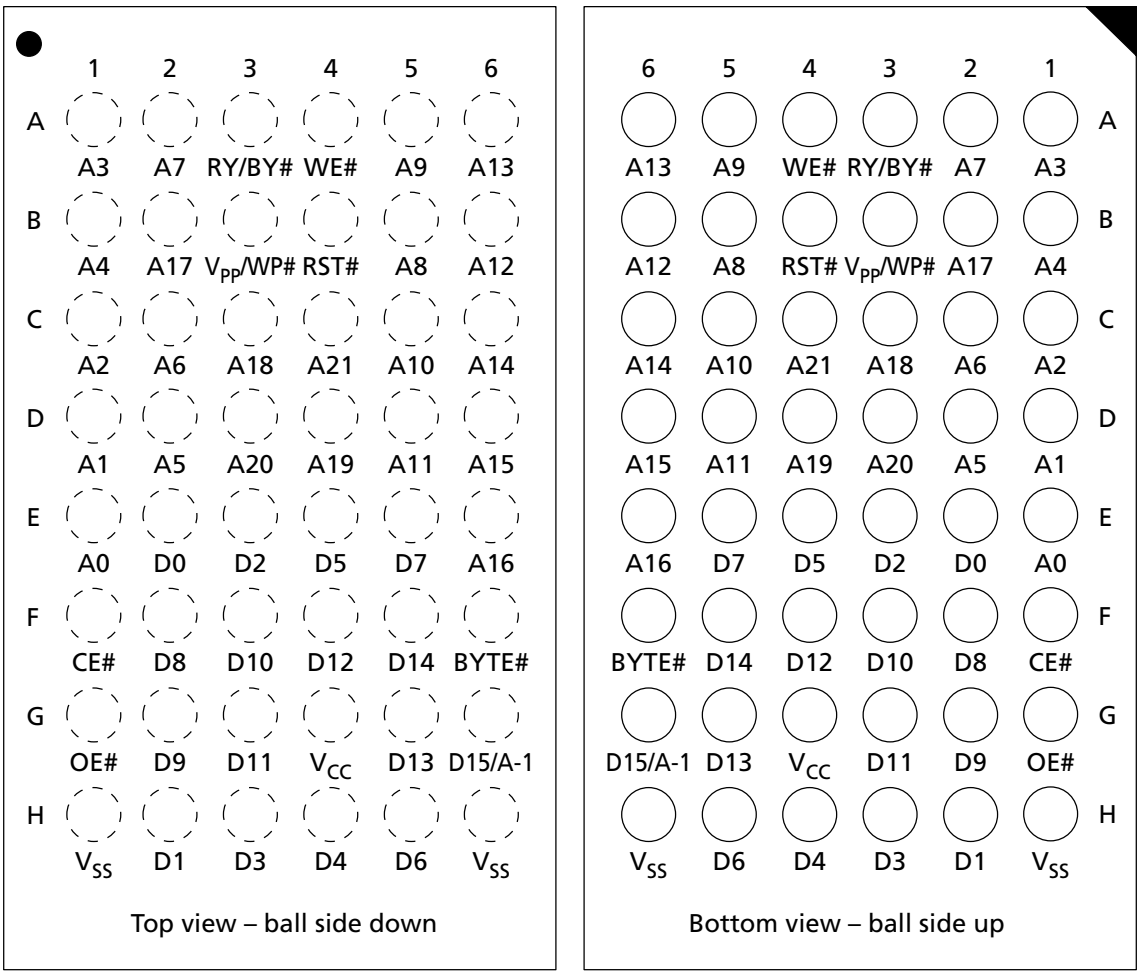
Figure 14: 48-Ball Fortified BGA and 48-Ball TBGA



Notes:
1. A[21] = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

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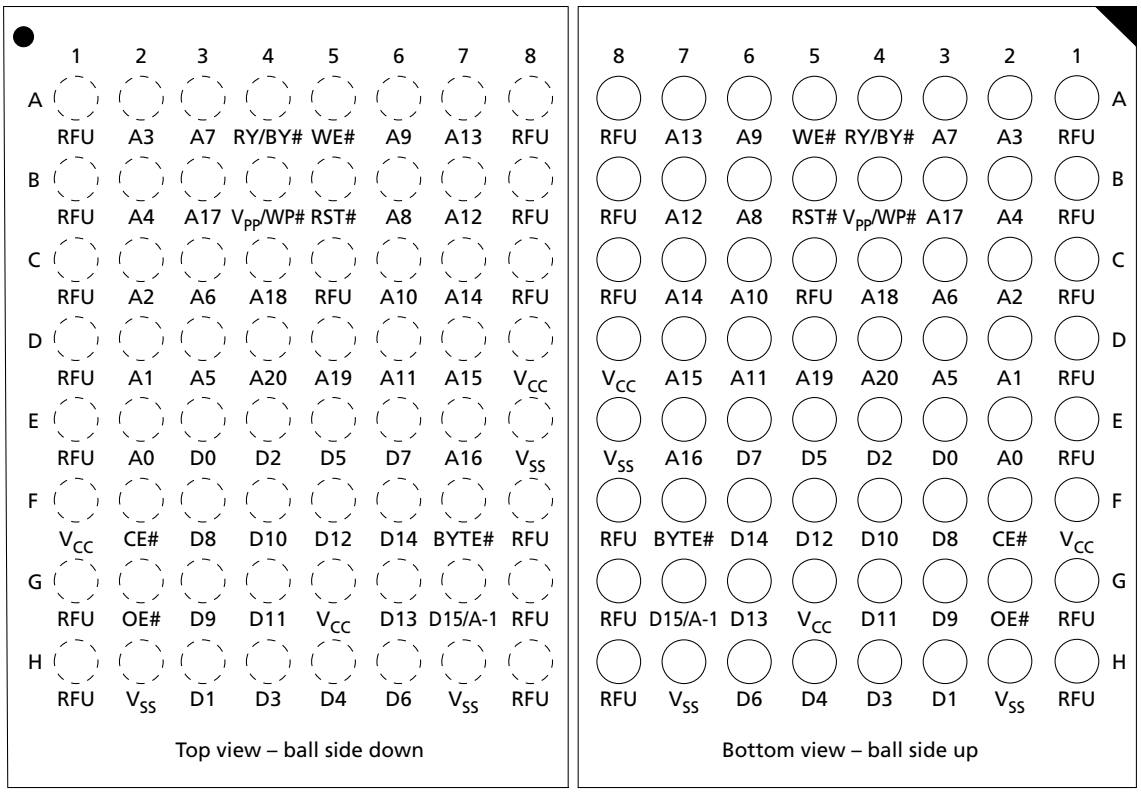
Figure 15: 64-Ball Fortified BGA and 64-Ball TBGA



Notes: 1. A[20] = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

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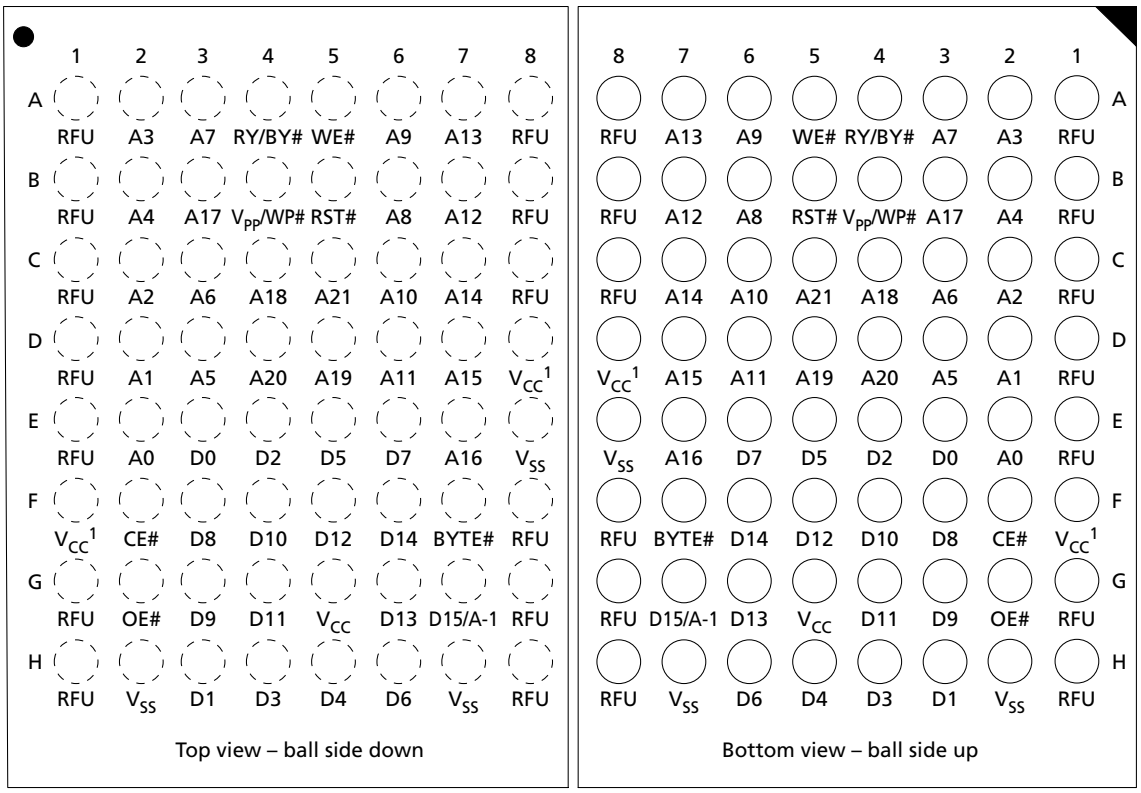
Figure 16: 64-Ball Fortified BGA and 64-Ball TBGA



Notes:
1. A[21] = A[MAX].
2. A-1 is the least significant address bit in x8 mode.
3. Pads D8 and F1 are not connected (NC) on the M29W640GT and M29W640GB devices.

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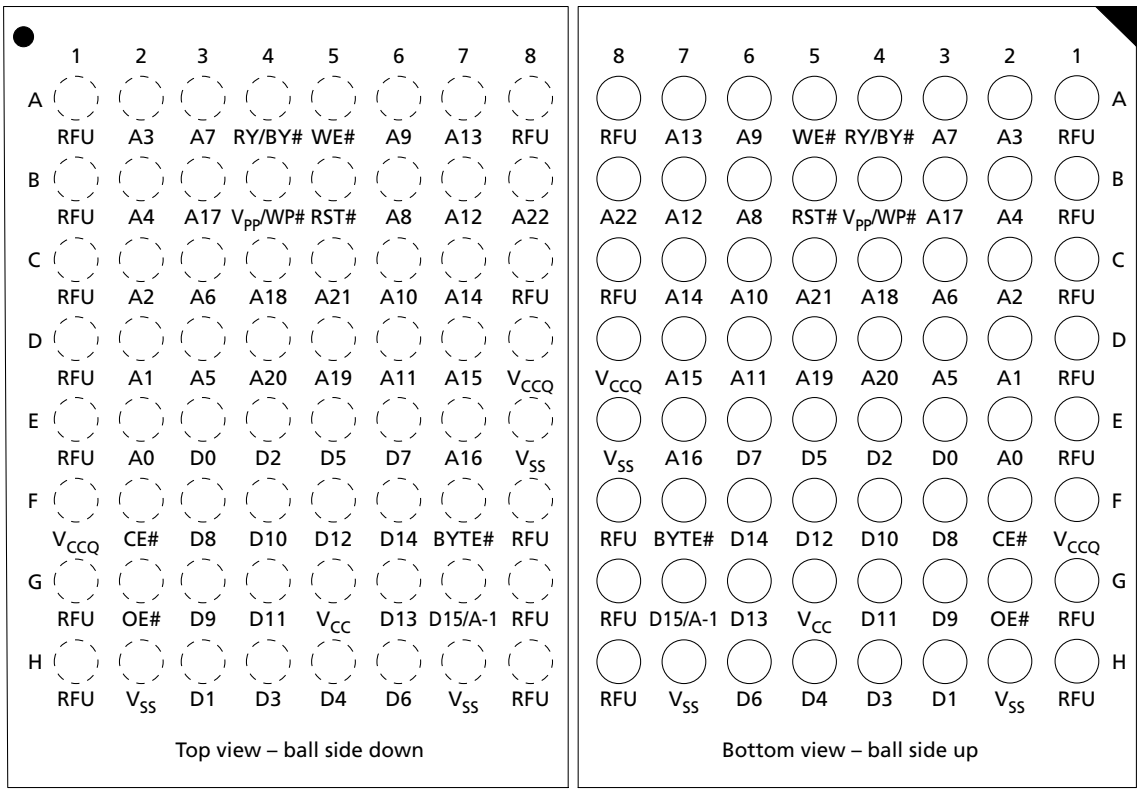
Figure 17: 64-Ball Fortified BGA and 64-Ball TBGA



Notes: 1. A[22] = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

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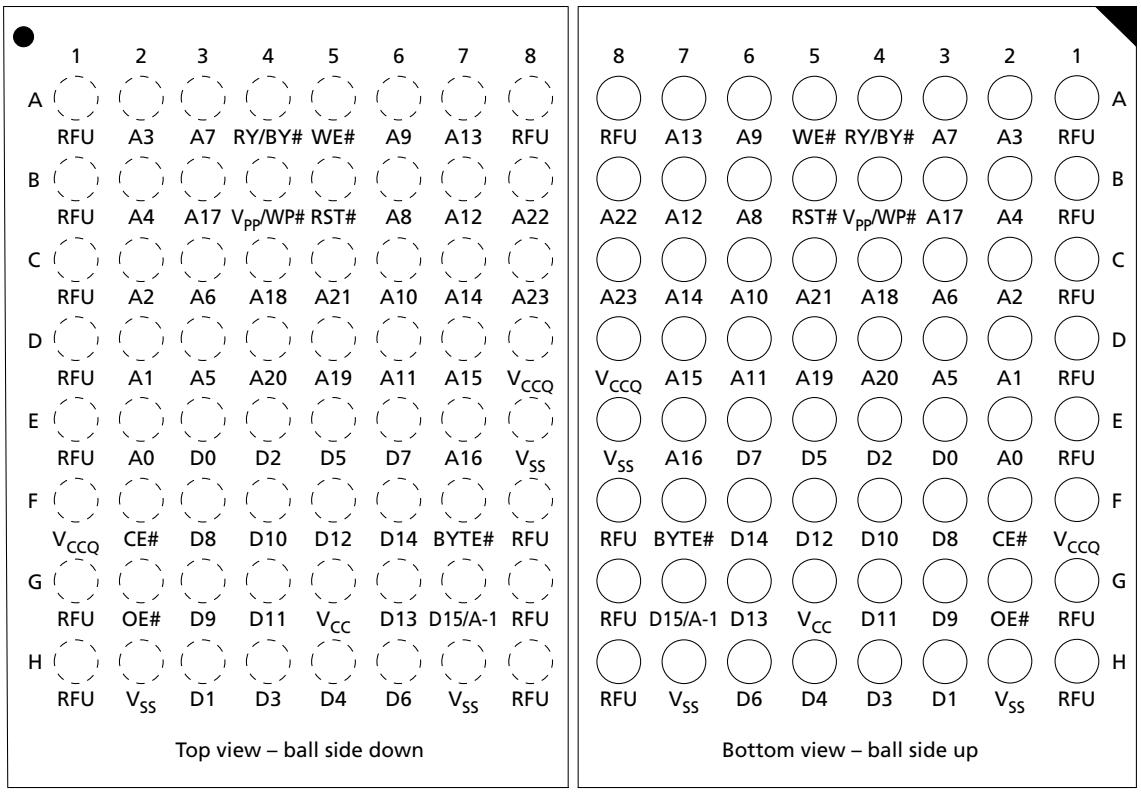
Figure 18: 64-Ball Fortified BGA and 64-Ball TBGA



Notes: 1. A[23] = A[MAX].
2. A-1 is the least significant address bit in x8 mode.

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Signal Descriptions

The signal description table below is a comprehensive list of signals for this device family. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 2: Signal Descriptions

Name	Type	Description
A[MAX:0]	Input	**Address:** Selects the cells in the array to access during READ operations. During WRITE operations, they control the commands sent to the command interface of the program/erase controller.
CE#	Input	**Chip enable:** Activates the device, enabling READ and WRITE operations to be performed. When CE# is HIGH, the device goes to standby and data outputs are at HIGH-Z.
OE#	Input	**Output enable:** Controls the bus READ operation.
WE#	Input	**Write enable:** Controls the bus WRITE operation of the command interface.
V_{PP}/WP#	Input	**V_{PP}/Write Protect:** Provides WRITE PROTECT function and V_{PPH} function. These functions protect the lowest or highest block and enable the device to enter unlock bypass mode, respectively. (Refer to Hardware Protection and Bypass Operations for details.)
BYTE#	Input	**Byte/word organization select:** Switches between x8 and x16 bus modes. When BYTE# is LOW, the device is in x8 mode; when HIGH, the device is in x16 mode.
RST#	Input	**Reset:** Applies a hardware reset to the device, which is achieved by holding RST# LOW for at least ^{t}PLPX. After RST# goes HIGH, the device is ready for READ and WRITE operations (after ^{t}PHEL or ^{t}RHEL, whichever occurs last). See RESET AC Specifications for more details.
DQ[7:0]	I/O	**Data I/O:** Outputs the data stored at the selected address during a READ operation. During WRITE operations, they represent the commands sent to the command interface of the internal state machine.
DQ[14:8]	I/O	**Data I/O:** Outputs the data stored at the selected address during a READ operation when BYTE# is HIGH. When BYTE# is LOW, these pins are not used and are High-Z. During WRITE operations, these bits are not used. When reading the status register, these bits should be ignored.
DQ15/A-1	I/O	**Data I/O or address input:** When the device operates in x16 bus mode, this pin behaves as data I/O, together with DQ[14:8]. When the device operates in x8 bus mode, this pin behaves as the least significant bit of the address. Except where stated explicitly otherwise, DQ15 = data I/O (x16 mode); A-1 = address input (x8 mode).
RY/BY#	Output	**Ready busy:** Open-drain output that can be used to identify when the device is performing a PROGRAM or ERASE operation. During PROGRAM or ERASE operations, RY/BY# is LOW, and is High-Z during read mode, auto select mode, and erase suspend mode. After a hardware reset, READ and WRITE operations cannot begin until RY/BY# goes High-Z (see RESET AC Specifications for more details). The use of an open-drain output enables the RY/BY# pins from several devices to be connected to a single pull-up resistor to V_{CCQ}. A low value will then indicate that one (or more) of the devices is (are) busy. A 10K Ohm or bigger resistor is recommended as pull-up resistor to achieve 0.1V V_{OL}.

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Table 2: Signal Descriptions (Continued)

Name	Type	Description
V_{CC}	Supply	**Supply voltage:** Provides the power supply for READ, PROGRAM, and ERASE operations. The command interface is disabled when V_{CC} <= V_{LKO}. This prevents WRITE operations from accidentally damaging the data during power-up, power-down, and power surges. If the program/erase controller is programming or erasing during this time, then the operation aborts and the contents being altered will be invalid. A 0.1µF capacitor should be connected between V_{CC} and V_{SS} to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during PROGRAM and ERASE operations (see DC Characteristics).
V_{CCQ}	Supply	**I/O supply voltage:** Provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}.
V_{SS}	Supply	**Ground:** All V_{SS} pins must be connected to the system ground.
RFU	–	**Reserved for future use:** RFUs should be not connected.

Memory Organization

Memory Configuration

The main memory array is divided into 128KB or 64KW uniform blocks.

Memory Map – 256Mb Density

Table 3: 256Mb, Blocks[255:0]

Block	Block Size	Address Range (x8)		Block Size	Address Range (x16)	
		Start	End		Start	End
255	128KB	1FE 0000h	1FF FFFFh	64KW	0FF 0000h	0FF FFFFh
⋮		⋮	⋮		⋮	⋮
127		0FE 0000h	0FF FFFFh		07F 0000h	07F FFFFh
⋮		⋮	⋮		⋮	⋮
63		07E 0000h	07F FFFFh		03F 0000h	03F FFFFh
⋮		⋮	⋮		⋮	⋮
0		000 0000h	001 FFFFh		000 0000h	000 FFFFh

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Bus Operations

Table 4: Bus Operations

Notes 1 and 2 apply to entire table

Operation	CE#	OE#	WE#	RST#	V_{PP}/WP#	8-Bit Mode			16-Bit Mode	
						A[MAX:0], DQ15/A-1	DQ[14:8]	DQ[7:0]	A[MAX:0]	DQ15/A-1, DQ[14:0]
READ	L	L	H	H	X	Cell address	High-Z	Data output	Cell address	Data output
WRITE	L	H	L	H	X[3]	Command address	High-Z	Data input[4]	Command address	Data input[4]
STANDBY	H	X	X	H	X	X	High-Z	High-Z	X	High-Z
OUTPUT DISABLE	L	H	H	H	X	X	High-Z	High-Z	X	High-Z
RESET	X	X	X	L	X	X	High-Z	High-Z	X	High-Z

Notes:
1. Typical glitches of less than 5ns on CE#, WE#, and RST# are ignored by the device and do not affect bus operations.
2. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
3. If WP# is LOW, then the highest or the lowest block remains protected, depending on line item.
4. Data input is required when issuing a command sequence or when performing data polling or block protection.

Read

Bus READ operations read from the memory cells, registers, or CFI space. To accelerate the READ operation, the memory array can be read in page mode where data is internally read and stored in a page buffer.

Page size is 8 words (16 bytes) and is addressed by address inputs A[2:0] in x16 bus mode and A[2:0] plus DQ15/A-1 in x8 bus mode. The extended memory blocks and CFI area do not support page read mode.

A valid READ operation requires setting the appropriate address on the address inputs, taking CE# and OE# LOW, and holding WE# HIGH. Data I/O signals output the value.

Write

Bus WRITE operations write to the command interface. A valid WRITE operation requires setting the appropriate address on the address inputs. These are latched by the command interface on the falling edge of CE# or WE#, whichever occurs last. Values on data I/O signals are latched by the command interface on the rising edge of CE# or WE#, whichever occurs first. OE# must remain HIGH during the entire operation.

Standby and Automatic Standby

When the device is in read mode, driving CE# HIGH places the device in standby mode and drives data I/Os to High-Z. Supply current is reduced to standby (I_{CC2}), by holding CE# within V_{CC} ±0.3V.

During PROGRAM or ERASE operations the device continues to use the program/erase supply current (I_{CC3}) until the operation completes.

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Automatic standby enables low power consumption during read mode. When CMOS levels (VCC ± 0.3 V) drive the bus and following a READ operation and a period of inactivity specified in DC Characteristics, the memory enters automatic standby as internal supply current is reduced to ICC2. Data I/O signals still output data if a READ operation is in progress. Depending on load circuits connected with data bus, VCCQ, can have a null consumption when the memory enters automatic standby.

Output Disable

Data I/Os are High-Z when OE# is HIGH.

Reset

During reset mode the device is deselected and outputs are High-Z. The device is in reset mode when RST# is LOW. Power consumption is reduced to standby level independently from CE#, OE#, or WE# inputs.

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Registers

Status Register

Table 5: Status Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ7	Data polling bit	0 or 1, depending on operations	Monitors whether the program/erase controller has successfully completed its operation, or has responded to an ERASE SUSPEND operation.	2, 3, 4
DQ6	Toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors whether the program/erase controller has successfully completed its operations, or has responded to an ERASE SUSPEND operation. During a PROGRAM/ERASE operation, DQ6 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from any address.	3, 4, 5
DQ5	Error bit	0 = Success 1 = Failure	Identifies errors detected by the program/erase controller. DQ5 is set to 1 when a PROGRAM, BLOCK ERASE, or CHIP ERASE operation fails to write the correct data to the memory.	4, 6
DQ3	Erase timer bit	0 = Erase not in progress 1 = Erase in progress	Identifies the start of program/erase controller operation during a BLOCK ERASE command. Before the program/erase controller starts, this bit set to 0, and additional blocks to be erased can be written to the command interface.	4
DQ2	Alternative toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors the program/erase controller during ERASE operations. During CHIP ERASE, BLOCK ERASE, and ERASE SUSPEND operations, DQ2 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from addresses within the blocks being erased.	3, 4
DQ1	Buffered program abort bit	1 = Abort	Indicates a BUFFER PROGRAM operation abort. The BUFFERED PROGRAM ABORT and RESET command must be issued to return the device to read mode (see WRITE TO BUFFER PROGRAM command).	

Notes:
1. The status register can be read during PROGRAM, ERASE, or ERASE SUSPEND operations; the READ operation outputs data on DQ[7:0].
2. For a PROGRAM operation in progress, DQ7 outputs the complement of the bit being programmed. For a READ operation from the address previously programmed successfully, DQ7 outputs existing DQ7 data. For a READ operation from addresses with blocks to be erased while an ERASE SUSPEND operation is in progress, DQ7 outputs 0; upon successful completion of the ERASE SUSPEND operation, DQ7 outputs 1. For an ERASE operation in progress, DQ7 outputs 0; upon either operation's successful completion, DQ7 outputs 1.
3. After successful completion of a PROGRAM or ERASE operation, the device returns to read mode.
4. During erase suspend mode, READ operations to addresses within blocks not being erased output memory array data as if in read mode. A protected block is treated the same as a block not being erased. See the Toggle Flowchart for more information.
5. During erase suspend mode, DQ6 toggles when addressing a cell within a block being erased. The toggling stops when the program/erase controller has suspended the ERASE operation. See the Toggle Flowchart for more information.

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6. When DQ5 is set to 1, a READ/RESET command must be issued before any subsequent command.

Table 6: Operations and Corresponding Bit Settings

Note 1 applies to entire table

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/BY#	Notes
PROGRAM	Any address	DQ7#	Toggle	0	–	No toggle	0	0	2
PROGRAM during ERASE SUSPEND	Any address	DQ7#	Toggle	0	–	–	–	0	
ENHANCED BUFFERED PROGRAM	Any address	–	Toggle	0	–	–	–	0	
BUFFERED PROGRAM ABORT	Any address	DQ7#	Toggle	0	–	–	1	0	2
PROGRAM error	Any address	DQ7#	Toggle	1	–	–	–	High-Z	
CHIP ERASE	Any address	0	Toggle	0	1	Toggle	–	0	
BLOCK ERASE before time-out	Erasing block	0	Toggle	0	0	Toggle	–	0	
	Non-erasing block	0	Toggle	0	0	No toggle	–	0	
BLOCK ERASE	Erasing block	0	Toggle	0	1	Toggle	–	0	
	Non-erasing block	0	Toggle	0	1	No toggle	–	0	
ERASE SUSPEND	Erasing block	1	No toggle	0	–	Toggle	–	High-Z	
	Non-erasing block	Outputs memory array data as if in read mode					–	High-Z	
BLOCK ERASE error	Good block address	0	Toggle	1	1	No toggle	–	High-Z	
	Faulty block address	0	Toggle	1	1	Toggle	–	High-Z	

Notes: 1. Unspecified data bits should be ignored.
2. DQ7# for buffer program is related to the last address location loaded.

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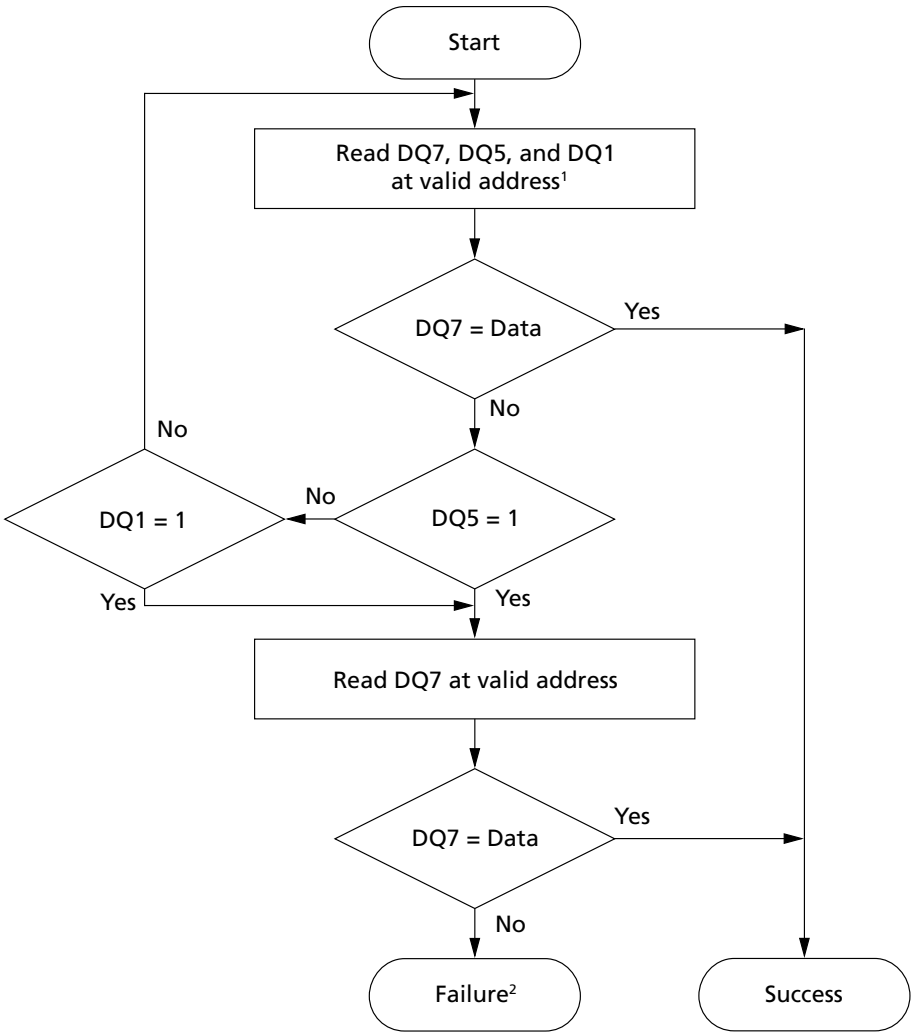
Figure 19: Data Polling Flowchart



Notes:
1. Valid address is the address being programmed or an address within the block being erased.
2. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

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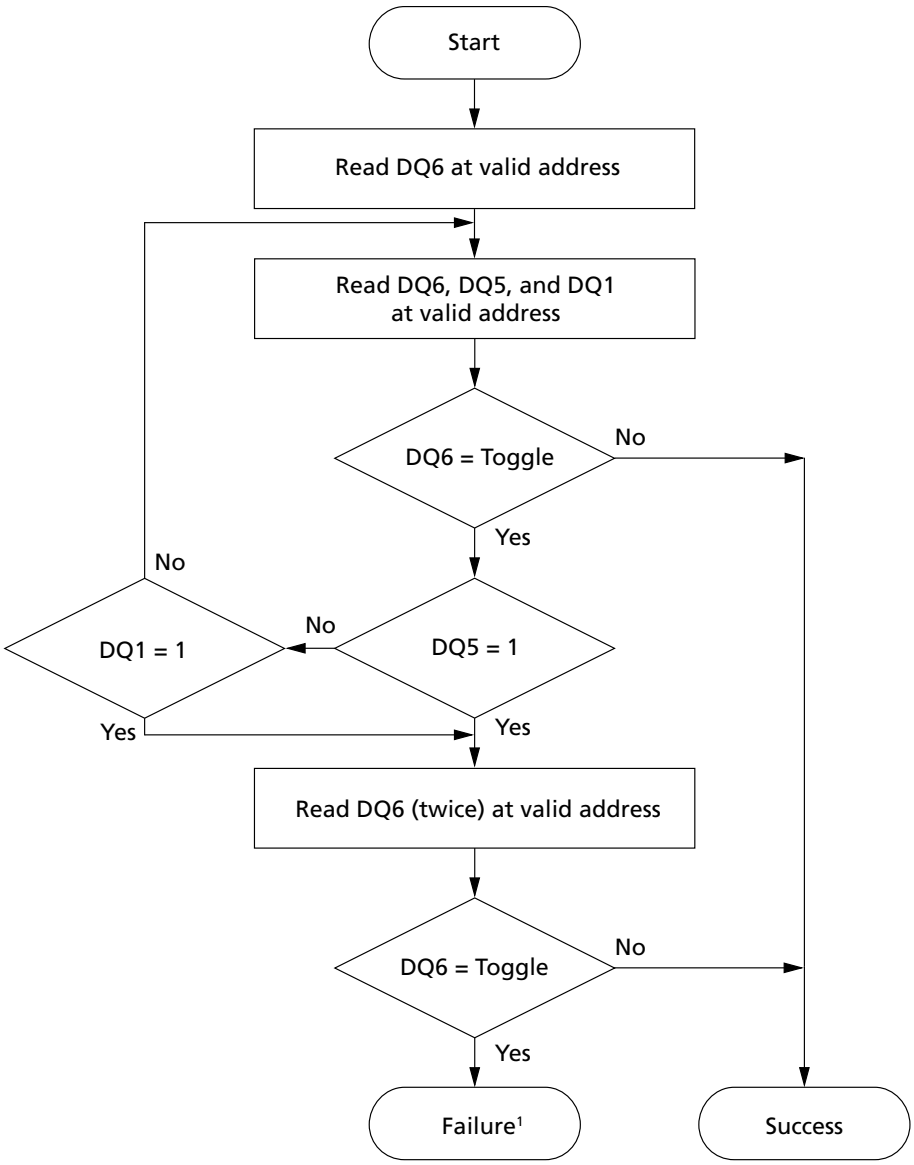
Figure 20: Toggle Bit Flowchart



Note: 1. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

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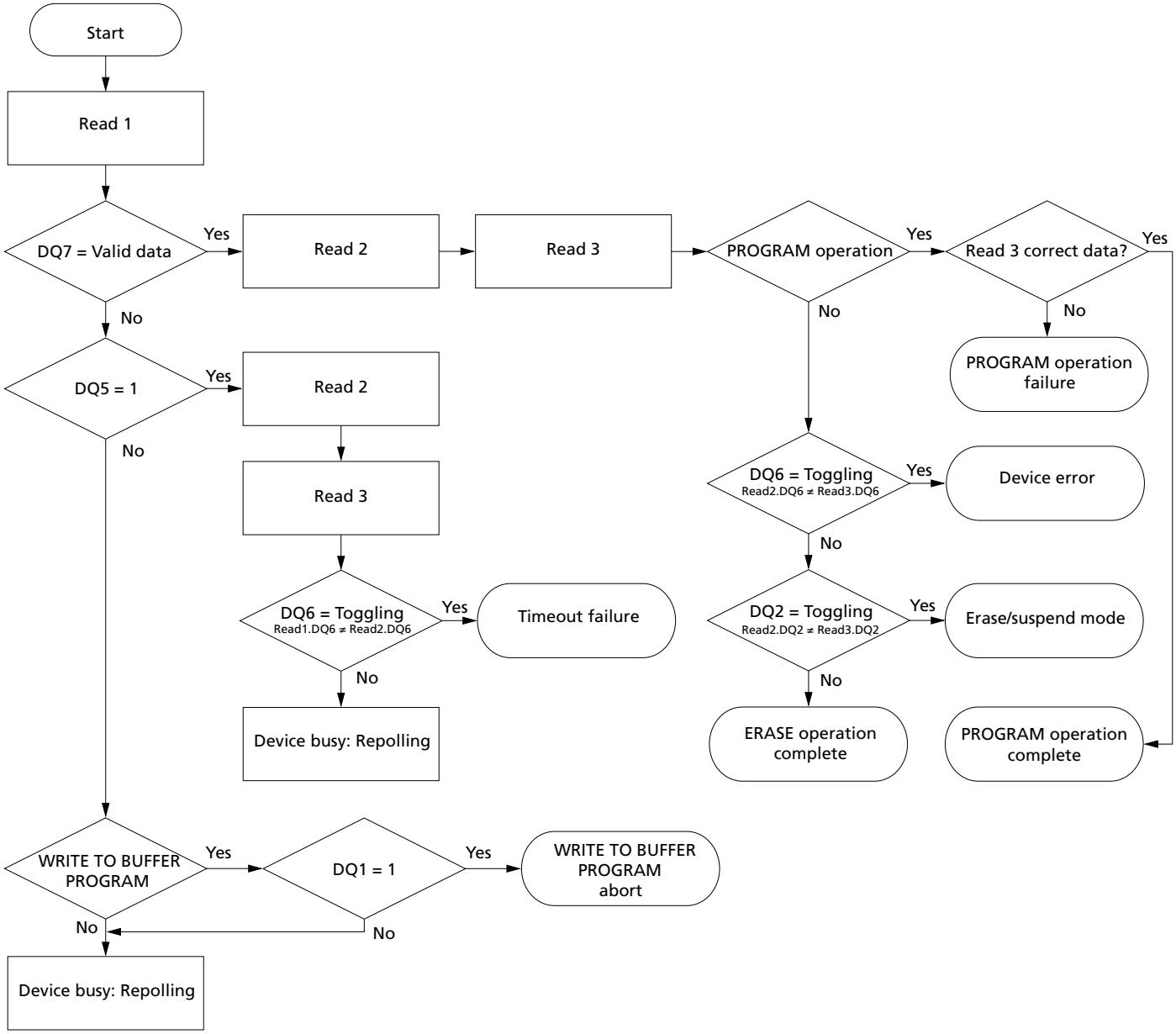
Figure 21: Status Register Polling Flowchart



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Lock Register

Table 7: Lock Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ2	Password protection mode lock bit	0 = Password protection mode enabled 1 = Password protection mode disabled (Default)	Places the device permanently in password protection mode.	2
DQ1	Nonvolatile protection mode lock bit	0 = Nonvolatile protection mode enabled with password protection mode permanently disabled 1 = Nonvolatile protection mode enabled (Default)	Places the device in nonvolatile protection mode with password protection mode permanently disabled. When shipped from the factory, the device will operate in nonvolatile protection mode, and the memory blocks are unprotected.	2
DQ0	Extended memory block protection bit	0 = Protected 1 = Unprotected (Default)	If the device is shipped with the extended memory block unlocked, the block can be protected by setting this bit to 0. The extended memory block protection status can be read in auto select mode by issuing an AUTO SELECT command.	

Notes:
1. The lock register is a 16-bit, one-time programmable register. DQ[15:3] are reserved and are set to a default value of 1.
2. The password protection mode lock bit and nonvolatile protection mode lock bit cannot both be programmed to 0. Any attempt to program one while the other is programmed causes the operation to abort, and the device returns to read mode. The device is shipped from the factory with the default setting.

Table 8: Block Protection Status

Nonvolatile Protection Bit Lock Bit[1]	Nonvolatile Protection Bit[2]	Volatile Protection Bit[3]	Block Protection Status	Block Protection Status
1	1	1	00h	Block unprotected; nonvolatile protection bit changeable.
1	1	0	01h	Block protected by volatile protection bit; nonvolatile protection bit changeable.
1	0	1	01h	Block protected by nonvolatile protection bit; nonvolatile protection bit changeable.
1	0	0	01h	Block protected by nonvolatile protection bit and volatile protection bit; nonvolatile protection bit changeable.
0	1	1	00h	Block unprotected; nonvolatile protection bit unchangeable.
0	1	0	01h	Block protected by volatile protection bit; nonvolatile protection bit unchangeable.
0	0	1	01h	Block protected by nonvolatile protection bit; nonvolatile protection bit unchangeable.
0	0	0	01h	Block protected by nonvolatile protection bit and volatile protection bit; nonvolatile protection bit unchangeable.

Notes:
1. Nonvolatile protection bit lock bit: when cleared to 1, all nonvolatile protection bits are unlocked; when set to 0, all nonvolatile protection bits are locked.

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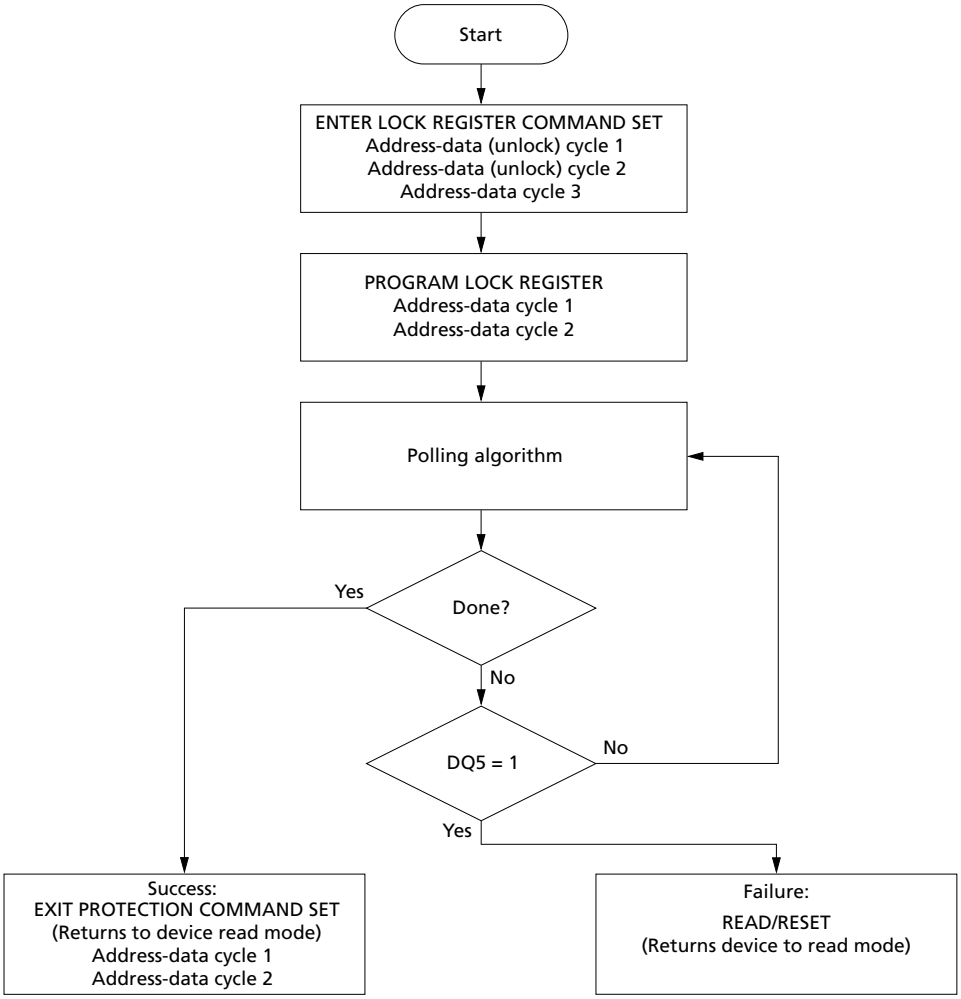
2. Block nonvolatile protection bit: when cleared to 1, the block is unprotected; when set to 0, the block is protected.
3. Block volatile protection bit: when cleared to 1, the block is unprotected; when set to 0, the block is protected.

Figure 22: Lock Register Program Flowchart



Notes:
1. Each lock register bit can be programmed only once.
2. See the Block Protection Command Definitions table for address-data cycle details.

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Standard Command Definitions – Address-Data Cycles

Table 9: Standard Command Definitions – Address-Data Cycles, 8-Bit and 16-Bit

Note 1 applies to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
READ and AUTO SELECT Operations														
READ/RESET (F0h)	x8	X	F0											
		AAA	AA	555	55	X	F0							
	x16	X	F0											
		555	AA	2AA	55	X	F0							
READ CFI (98h)	x8	AA	98											
	x16	55												
AUTO SELECT (90h)	x8	AAA	AA	555	55	AAA	90	Note 2	Note 2					2, 3, 4
	x16	555		2AA		555								
BYPASS Operations														
UNLOCK BYPASS (20h)	x8	AAA	AA	555	55	AAA	20							
	x16	555		2AA		555								
UNLOCK BYPASS RESET (90h/00h)	x8	X	90	X	00									
	x16													
PROGRAM Operations														
PROGRAM (A0h)	x8	AAA	AA	555	55	AAA	A0	PA	PD					
	x16	555		2AA		555								
UNLOCK BYPASS PROGRAM (A0h)	x8	X	A0	PA	PD									5
	x16													
WRITE TO BUFFER PROGRAM (25h)	x8	AAA	AA	555	55	BAd	25	BAd	N	PA	PD			6, 7, 8
	x16	555		2AA										
UNLOCK BYPASS WRITE TO BUFFER PROGRAM (25h)	x8	BAd	25	BAd	N	PA	PD							5
	x16													
WRITE TO BUFFER PROGRAM CONFIRM (29h)	x8	BAd	29											
	x16													
BUFFERED PROGRAM ABORT and RESET (F0h)	x8	AAA	AA	555	55	AAA	F0							
	x16	555		2AA		555								
ENTER ENHANCED BUFFERED PROGRAM (38h)	x8	NA												
	x16	555	AA	2AA	55	555	38							
ENHANCED BUFFERED PROGRAM (33h)	x8	NA												9
	x16	BAd	33	BAd (00)	Data	BAd (01)	Data							

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Table 9: Standard Command Definitions – Address-Data Cycles, 8-Bit and 16-Bit (Continued)

Note 1 applies to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
EXIT ENHANCED BUFFERED PROGRAM (90h)	x8	NA												
	x16	X	90	X	00									
ENHANCED BUFFERED PROGRAM ABORT (F0h)	x8	NA												
	x16	555	AA	2AA	55	555	F0							
PROGRAM SUSPEND (B0h)	x8	X	B0											
	x16													
PROGRAM RESUME (30h)	x8	X	30											
	x16													
ERASE Operations														
CHIP ERASE (80/10h)	x8	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10	
	x16	555		2AA		555		555		2AA		555		
UNLOCK BYPASS CHIP ERASE (80/10h)	x8	X	80	X	10									5
	x16													
BLOCK ERASE (80/30h)	x8	AAA	AA	555	55	AAA	80	AAA	AA	555	55	BAd	30	10
	x16	555		2AA		555		555		2AA				
UNLOCK BYPASS BLOCK ERASE (80/30h)	x8	X	80	BAd	30									5
	x16													
ERASE SUSPEND (B0h)	x8	X	B0											
	x16													
ERASE RESUME (30h)	x8	X	30											
	x16													

Notes:
1. A = Address; D = Data; X = "Don't Care;" BAd = Any address in the block; N = Number of bytes to be programmed; PA = Program address; PD = Program data; Gray shading = Not applicable. All values in the table are hexadecimal. Some commands require both a command code and subcode.
2. These cells represent READ cycles (versus WRITE cycles for the others).
3. AUTO SELECT enables the device to read the manufacturer code, device code, block protection status, and extended memory block protection indicator.
4. AUTO SELECT addresses and data are specified in the Electronic Signature table and the Extended Memory Block Protection table.
5. For any UNLOCK BYPASS ERASE/PROGRAM command, the first two UNLOCK cycles are unnecessary.
6. BAd must be the same as the address loaded during the WRITE TO BUFFER PROGRAM 3rd and 4th cycles.
7. WRITE TO BUFFER PROGRAM operation: maximum cycles = 68(x8) and 36 (x16). UNLOCK BYPASS WRITE TO BUFFER PROGRAM operation: maximum cycles = 66 (x8), 34 (x16). WRITE TO BUFFER PROGRAM operation: N + 1 = bytes to be programmed; maximum buffer size = 64 bytes (x8) and 32 words (x16).

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8. For x8, A[MAX:5] address pins should remain unchanged while A[4:0] and A-1 pins are used to select a byte within the N + 1 byte page. For x16, A[MAX:5] address pins should remain unchanged while A[4:0] pins are used to select a word within the N + 1 word page.
9. The following is content for address-data cycles 256 through 258: BAd (FE) - Data; BAd (FF) - Data; BAd (00) - 29.
10. BLOCK ERASE address cycles can extend beyond six address-data cycles, depending on the number of blocks to erase.

READ Operations

READ/RESET Command

The READ/RESET (F0h) command returns the device to read mode and resets the errors in the status register. One or three bus WRITE operations can be used to issue the READ/RESET command.

To return the device to read mode, this command can be issued between bus WRITE cycles before the start of a PROGRAM or ERASE operation. If the READ/RESET command is issued during the timeout of a BLOCK ERASE operation, the device requires up to 10µs to abort, during which time no valid data can be read.

This command will not abort an ERASE operation while in erase suspend.

READ CFI Command

The READ CFI (98h) command puts the device in read CFI mode and is only valid when the device is in read array or auto select mode. One bus WRITE cycle is required to issue the command.

Once in read CFI mode, bus READ operations will output data from the CFI memory area (Refer to the Common Flash Interface for details). A READ/RESET command must be issued to return the device to the previous mode (read array or auto select). A second READ/RESET command is required to put the device in read array mode from auto select mode.

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AUTO SELECT Operations

AUTO SELECT Command

At power-up or after a hardware reset, the device is in read mode. It can then be put in auto select mode by issuing an AUTO SELECT (90h) command or by applying V_{ID} to A9. Auto select mode enables the following device information to be read:

- Electronic signature, which includes manufacturer and device code information as shown in the Electronic Signature table.
- Block protection, which includes the block protection status and extended memory block protection indicator, as shown in the Block Protection table.

Electronic signature or block protection information is read by executing a READ operation with control signals and addresses set, as shown in the Read Electronic Signature table or the Block Protection table, respectively.

Auto select mode can be used by the programming equipment to automatically match a device with the application code to be programmed.

Three consecutive bus WRITE operations are required to issue an AUTO SELECT command. The device remains in auto select mode until a READ/RESET or READ CFI command is issued.

The device cannot enter auto select mode when a PROGRAM or ERASE operation is in progress (RY/BY# LOW). However, auto select mode can be entered if the PROGRAM or ERASE operation has been suspended by issuing a PROGRAM SUSPEND or ERASE SUSPEND command.

To enter auto select mode by appling VID to A9, see the Read Electronic Signature table and the Block Protection table.

Auto select mode is exited by performing a reset. The device returns to read mode unless it entered auto select mode after an ERASE SUSPEND or PROGRAM SUSPEND command, in which case it returns to erase or program suspend mode.

Table 10: Read Electronic Signature

Note 1 applies to entire table

Signal	Read Cycle				Notes
	Manufacturer Code	Device Code 1	Device Code 3	Device Code 3	
CE#	L	L	L	L	
OE#	L	L	L	L	
WE#	H	H	H	H	
Address Input, 8-Bit and 16-Bit					
A[MAX:10]	X	X	X	X	
A9	V_{ID}	V_{ID}	V_{ID}	V_{ID}	2
A8	X	X	X	X	
A[7:5]	L	L	L	L	
A4	X	X	X	X	
A[3:1]	L	L	H	H	

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Table 10: Read Electronic Signature (Continued)

Note 1 applies to entire table

Signal	Read Cycle				Notes
	Manufacturer Code	Device Code 1	Device Code 3	Device Code 3	
A0	L	H	L	H	
Address Input, 8-Bit Only					
DQ[15]/A-1	X	X	X	X	
Data Input/Output, 8-Bit Only					
DQ[14:8]	X	X	X	X	
DQ[7:0]	20h	7Eh	22h	01h	
Data Input/Output, 16-Bit Only					
DQ[15]/A-1, and DQ[14:0]	0020h	227Eh	2222h	2201h	

Notes:
1. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
2. When using the AUTO SELECT command to enter auto select mode, applying V_{ID} to A9 is not required. A9 can be either V_{IL} or V_{IH}.

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Table 11: Block Protection

Note 1 applies to entire table

Signal	Read Cycle			Notes
	GL	GH	Block Protection Status	
CE#	L	L	L	
OE#	L	L	L	
WE#	H	H	H	
Address Input, 8-Bit and 16-Bit				
A[MAX:16]	X	X	Block base address	
A[15:10]	X	X	X	
A9	V_{ID}	V_{ID}	V_{ID}	2
A8	X	X	X	
A[7:5]	L	L	L	
A4	X	X	X	
A[3:2]	L	L	L	
A1	H	H	H	
A0	H	H	L	
Address Input, 8-Bit Only				
DQ[15]/A-1	X	X	X	
Data Input/Output, 8-Bit Only				
DQ[14:8]	X	X	X	
DQ[7:0]	89h	99h	01h	3, 5
	09h	19h	00h	4, 6
Data Input/Output, 16-Bit Only				
DQ[15]/A-1, and DQ[14:0]	0089h	0099h	0001h	3, 5
	0009h	0019h	0000h	4, 6

Notes:
1. Read cycle output to DQ7 = Extended memory block protection indicator; GL = High block protection; GH = Low block protection; BPS = Block protection status; H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
2. When using the AUTO SELECT command to enter auto select mode, applying V_{ID} to A9 is not required. A9 can be either V_{IL} or V_{IH}.
3. GL and GH devices are Micron-prelocked (permanent).
4. GL and GH devices are customer-lockable.
5. Block protection status = protected: 01h (in x8 mode) is output on DQ[7:0]; indicates that the extended memory block is permanently prelocked by Micron.
6. Block protection status = unprotected: 00h (in x8 mode) is output on DQ[7:0]; indicates that the extended memory block can be locked by customer.

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Bypass Operations

UNLOCK BYPASS Command

The UNLOCK BYPASS (20h) command is used to place the device in unlock bypass mode. Three bus WRITE operations are required to issue the UNLOCK BYPASS command.

When the device enters unlock bypass mode, the two initial UNLOCK cycles required for a standard PROGRAM or ERASE operation are not needed, thus enabling faster total program or erase time.

The UNLOCK BYPASS command is used in conjunction with UNLOCK BYPASS PROGRAM or UNLOCK BYPASS ERASE commands to program or erase the device faster than with standard PROGRAM or ERASE commands. When the cycle time to the device is long, considerable time savings can be gained by using these commands. When in unlock bypass mode, only the following commands are valid:

- The UNLOCK BYPASS PROGRAM command can be issued to program addresses within the device.
- The UNLOCK BYPASS BLOCK ERASE command can then be issued to erase one or more memory blocks.
- The UNLOCK BYPASS CHIP ERASE command can be issued to erase the whole memory array.
- The UNLOCK BYPASS WRITE TO BUFFER PROGRAM and UNLOCK BYPASS ENHANCED WRITE TO BUFFER PROGRAM commands can be issued to speed up the programming operation.
- The UNLOCK BYPASS RESET command can be issued to return the device to read mode.

In unlock bypass mode, the device can be read as if in read mode.

In addition to the UNLOCK BYPASS command, when V_{PP}/WP# is raised to V_{PPH}, the device automatically enters unlock bypass mode. When V_{PP}/WP# returns to V_{IH} or V_{IL}, the device is no longer in unlock bypass mode and normal operation resumes. The transitions from V_{IH} to V_{PPH} and from V_{PPH} to V_{IH} must be slower than ^{t}VHVPP (see the Accelerated Program, Data Polling/Toggle AC Characteristics).

Note: Micron recommends the user enter and exit unlock bypass mode using ENTER UNLOCK BYPASS and UNLOCK BYPASS RESET commands rather than raising V_{PP}/WP# to V_{PPH}. V_{PP}/WP# should never be raised to V_{PPH} from any mode except read mode; otherwise, the device may be left in an indeterminate state.

UNLOCK BYPASS RESET Command

The UNLOCK BYPASS RESET (90/00h) command is used to return to read/reset mode from unlock bypass mode. Two bus WRITE operations are required to issue the UNLOCK BYPASS RESET command. The READ/RESET command does not exit from unlock bypass mode.

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Program Operations

PROGRAM Command

The PROGRAM (A0h) command can be used to program a value to one address in the memory array. The command requires four bus WRITE operations, and the final WRITE operation latches the address and data in the internal state machine and starts the program/erase controller. After programming has started, bus READ operations output the status register content.

Programming can be suspended and then resumed by issuing a PROGRAM SUSPEND command and a PROGRAM RESUME command, respectively.

If the address falls in a protected block, the PROGRAM command is ignored, and the data remains unchanged. The status register is not read, and no error condition is given.

After the PROGRAM operation has completed, the device returns to read mode, unless an error has occurred. When an error occurs, bus READ operations to the device continue to output the status register. A READ/RESET command must be issued to reset the error condition and return the device to read mode.

The PROGRAM command cannot change a bit set to 0 back to 1, and an attempt to do so is masked during a PROGRAM operation. Instead, an ERASE command must be used to set all bits in one memory block or in the entire memory from 0 to 1.

The PROGRAM operation is aborted by performing a reset or by powering-down the device. In this case, data integrity cannot be ensured, and it is recommended that the words or bytes that were aborted be reprogrammed.

UNLOCK BYPASS PROGRAM Command

When the device is in unlock bypass mode, the UNLOCK BYPASS PROGRAM (A0h) command can be used to program one address in the memory array. The command requires two bus WRITE operations instead of four required by a standard PROGRAM command; the final WRITE operation latches the address and data and starts the program/erase controller (The standard PROGRAM command requires four bus WRITE operations). The PROGRAM operation using the UNLOCK BYPASS PROGRAM command behaves identically to the PROGRAM operation using the PROGRAM command. The operation cannot be aborted. A bus READ operation to the memory outputs the status register.

WRITE TO BUFFER PROGRAM Command

The WRITE TO BUFFER PROGRAM (25h) command makes use of the 32-word program buffer to speed up programming. A maximum of 32 words can be loaded into the program buffer. The WRITE TO BUFFER PROGRAM command dramatically reduces system programming time compared to the standard non-buffered PROGRAM command.

When issuing a WRITE TO BUFFER PROGRAM command, V_{PP}/WP# can be either held HIGH or raised to V_{PPH}. Also, it can be held LOW if the block is not the lowest or highest block, depending on the part number. The following successive steps are required to issue the WRITE TO BUFFER PROGRAM command:

First, two UNLOCK cycles are issued. Next, a third bus WRITE cycle sets up the WRITE TO BUFFER PROGRAM command. The set-up code can be addressed to any location

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within the targeted block. Then, a fourth bus WRITE cycle sets up the number of words/bytes to be programmed. Value *n* is written to the same block address, where *n + 1* is the number of words/bytes to be programmed. Value *n + 1* must not exceed the size of the program buffer, or the operation will abort. A fifth cycle loads the first address and data to be programmed. Last, *n* bus WRITE cycles load the address and data for each word/byte into the program buffer. Addresses must lie within the range from *the start address +1* to *the start address + (n - 1)*.

Optimum programming performance and lower power usage are achieved by aligning the starting address at the beginning of a 32-word boundary. Any buffer size smaller than 32 words is allowed within a 32-word boundary, while all addresses used in the operation must lie within the 32-word boundary. In addition, any crossing boundary buffer program will result in a program abort.

To program the content of the program buffer, this command must be followed by a WRITE TO BUFFER PROGRAM CONFIRM command.

If an address is written several times during a WRITE TO BUFFER PROGRAM operation, the address/data counter will be decremented at each data load operation, and the data will be programmed to the last word loaded into the buffer.

Invalid address combinations or the incorrect sequence of bus WRITE cycles will abort the WRITE TO BUFFER PROGRAM command.

The status register bits DQ1, DQ5, DQ6, DQ7 can be used to monitor the device status during a WRITE TO BUFFER PROGRAM operation.

The WRITE BUFFER PROGRAM command should not be used to change a bit set to 0 back to 1, and an attempt to do so is masked during the operation. Rather than the WRITE BUFFER PROGRAM command, the ERASE command should be used to set memory bits from 0 to 1.

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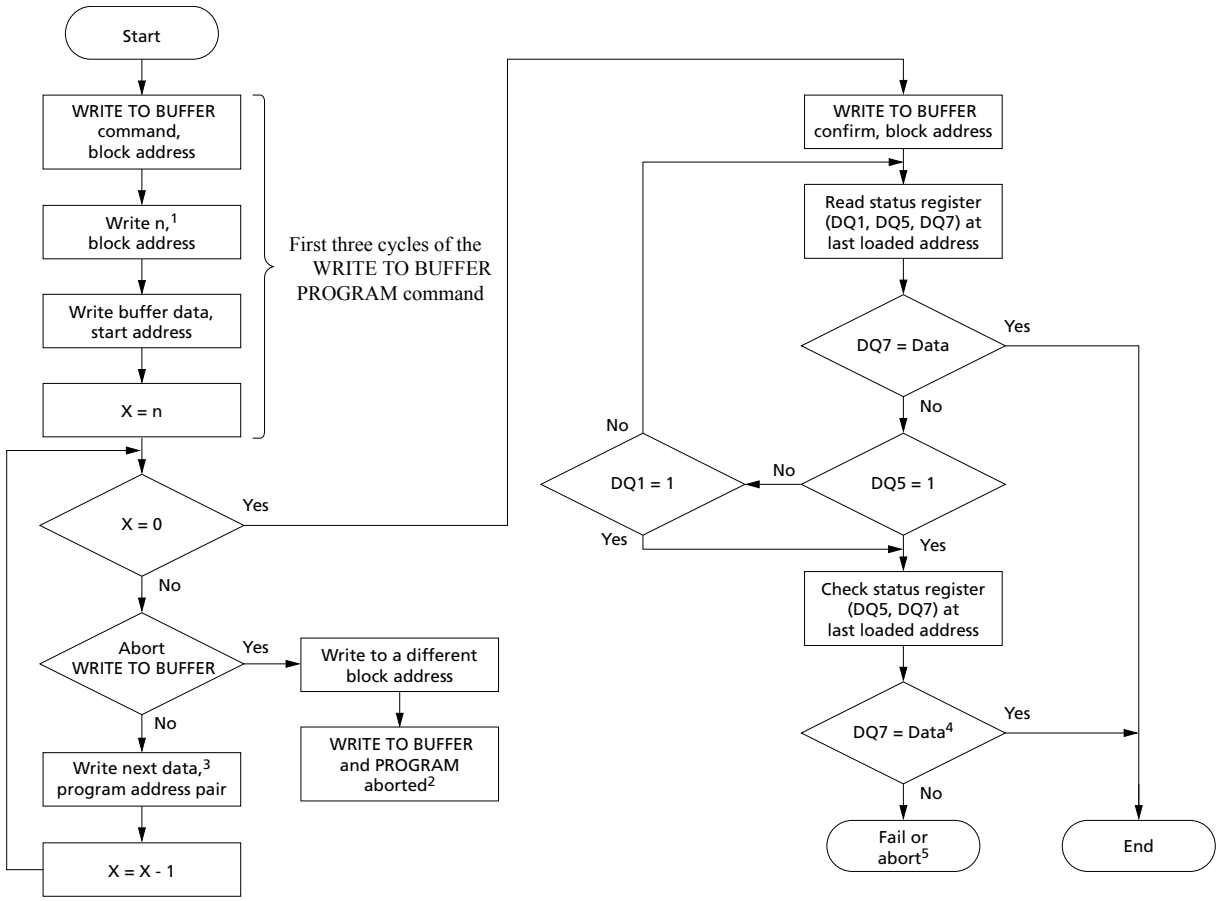
Figure 23: WRITE TO BUFFER PROGRAM Flowchart



Notes:
1. *n + 1* is the number of addresses to be programmed.
2. The BUFFERED PROGRAM ABORT and RESET command must be issued to return the device to read mode.
3. When the block address is specified, any address in the selected block address space is acceptable. However, when loading program buffer address with data, all addresses must fall within the selected program buffer page.
4. DQ7 must be checked because DQ5 and DQ7 may change simultaneously.
5. If this flowchart location is reached because DQ5 = 1, then the WRITE TO BUFFER PROGRAM command failed. If this flowchart location is reached because DQ1 = 1, then the WRITE TO BUFFER PROGRAM command aborted. In both cases, the appropriate RESET command must be issued to return the device to read mode: A RESET command if the operation failed; a WRITE TO BUFFER PROGRAM ABORT AND RESET command if the operation aborted.
6. See the Standard Command Definitions – Address-Data Cycles, 8-Bit and 16-Bit table for details about the WRITE TO BUFFER PROGRAM command sequence.

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UNLOCK BYPASS WRITE TO BUFFER PROGRAM Command

When the device is in unlock bypass mode, the UNLOCK BYPASS WRITE TO BUFFER (25h) command can be used to program the device in fast program mode. The command requires two bus WRITE operations fewer than the standard WRITE TO BUFFER PROGRAM command.

The UNLOCK BYPASS WRITE TO BUFFER PROGRAM command behaves the same way as the WRITE TO BUFFER PROGRAM command: the operation cannot be aborted, and a bus READ operation to the memory outputs the status register.

The WRITE TO BUFFER PROGRAM CONFIRM command is used to confirm an UNLOCK BYPASS WRITE TO BUFFER PROGRAM command and to program the *n + 1* words/bytes loaded in the program buffer by this command.

WRITE TO BUFFER PROGRAM CONFIRM Command

The WRITE TO BUFFER PROGRAM CONFIRM (29h) command is used to confirm a WRITE TO BUFFER PROGRAM command and to program the *n + 1* words/bytes loaded in the program buffer by this command.

BUFFERED PROGRAM ABORT AND RESET Command

A BUFFERED PROGRAM ABORT AND RESET (F0h) command must be issued to reset the device to read mode when the BUFFER PROGRAM operation is aborted. The buffer programming sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the number of locations to program in the WRITE TO BUFFER PROGRAM command.
- Write to an address in a different block than the one specified during the WRITE BUFFER LOAD command.
- Write an address/data pair to a different write buffer page than the one selected by the starting address during the program buffer data loading stage of the operation.
- Write data other than the CONFIRM command after the specified number of data load cycles.

The abort condition is indicated by DQ1 = 1, DQ7 = DQ7# (for the last address location loaded), DQ6 = toggle, and DQ5 = 0 (all of which are status register bits). A BUFFERED PROGRAM ABORT and RESET command sequence must be written to reset the device for the next operation.

Note: The full three-cycle BUFFERED PROGRAM ABORT and RESET command sequence is required when using buffer programming features in unlock bypass mode.

PROGRAM SUSPEND Command

The PROGRAM SUSPEND (B0h) command can be used to interrupt a program operation so that data can be read from any block. When the PROGRAM SUSPEND command is issued during a program operation, the device suspends the operation within the program suspend latency time and updates the status register bits.

After the program operation has been suspended, data can be read from any address. However, data is invalid when read from an address where a program operation has been suspended.

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The PROGRAM SUSPEND command may also be issued during a PROGRAM operation while an erase is suspended. In this case, data may be read from any address not in erase suspend or program suspend mode. To read from the extended memory block area (one-time programmable area), the ENTER/EXIT EXTENDED MEMORY BLOCK command sequences must be issued.

The system may also issue the AUTO SELECT command sequence when the device is in program suspend mode. The system can read as many auto select codes as required. When the device exits auto select mode, the device reverts to program suspend mode and is ready for another valid operation.

The PROGRAM SUSPEND operation is aborted by performing a device reset or power-down. In this case, data integrity cannot be ensured, and it is recommended that the words or bytes that were aborted be reprogrammed.

PROGRAM RESUME Command

The PROGRAM RESUME (30h) command must be issued to exit a program suspend mode and resume a PROGRAM operation. The controller can use DQ7 or DQ6 status bits to determine the status of the PROGRAM operation. After a PROGRAM RESUME command is issued, subsequent PROGRAM RESUME commands are ignored. Another PROGRAM SUSPEND command can be issued after the device has resumed programming.

ENTER and EXIT ENHANCED BUFFERED PROGRAM Command

The Enhanced Buffered Program commands are available only in x16 mode. When the ENTER ENHANCED BUFFERED PROGRAM command is issued, the device accepts only these commands, which can be executed multiple times. To ensure successful completion of the ENTER ENHANCED BUFFERED PROGRAM command, it is recommended that users monitor the toggle bit. The EXIT ENHANCED BUFFERED PROGRAM command returns the device to read mode; two bus write operations are required to issue the command.

ENHANCED BUFFERED PROGRAM Command

The ENHANCED BUFFERED PROGRAM command makes use of a 256-word write buffer to speed up programming. Each write buffer has the same A23-A8 addresses. This command dramatically reduces system programming time compared to both the standard non-buffered PROGRAM command and the WRITE TO BUFFER command.

When issuing the ENHANCED BUFFERED PROGRAM command, the V_{PP}/WP pin can be held HIGH or raised to V_{PPH} (see Program/Erase Characteristics). The following successive steps are required to issue the WRITE TO BUFFER PROGRAM command:

First, the ENTER ENHANCED BUFFERED PROGRAM command issued. Next, one bus WRITE cycle sets up the ENHANCED BUFFERED PROGRAM command. The set-up code can be addressed to any location within the targeted block. Then, a second bus WRITE cycle loads the first address and data to be programmed. There are a total of 256 address and data loading cycles. When the 256 words are loaded to the buffer, a third WRITE cycle programs the content of the buffer. Last, when the command completes, the EXIT ENHANCED BUFFERED PROGRAM command is issued.

Address/data cycles must be loaded in an increasing address order, from A[7:0] = 00000000 to A[7:0] = 11111111 until all 256 words are loaded. Invalid address combina-

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tions or the incorrect sequence of bus WRITE cycles will abort the WRITE TO BUFFER PROGRAM command.

The status register bits DQ1, DQ5, DQ6, DQ7 can be used to monitor the device status during a WRITE TO BUFFER PROGRAM operation.

An external 12V supply can be used to improve programming efficiency.

When reprogramming data in a portion of memory already programmed (changing programmed data from '0' to '1') operation failure can be detected by a logical OR between the previous and the current value.

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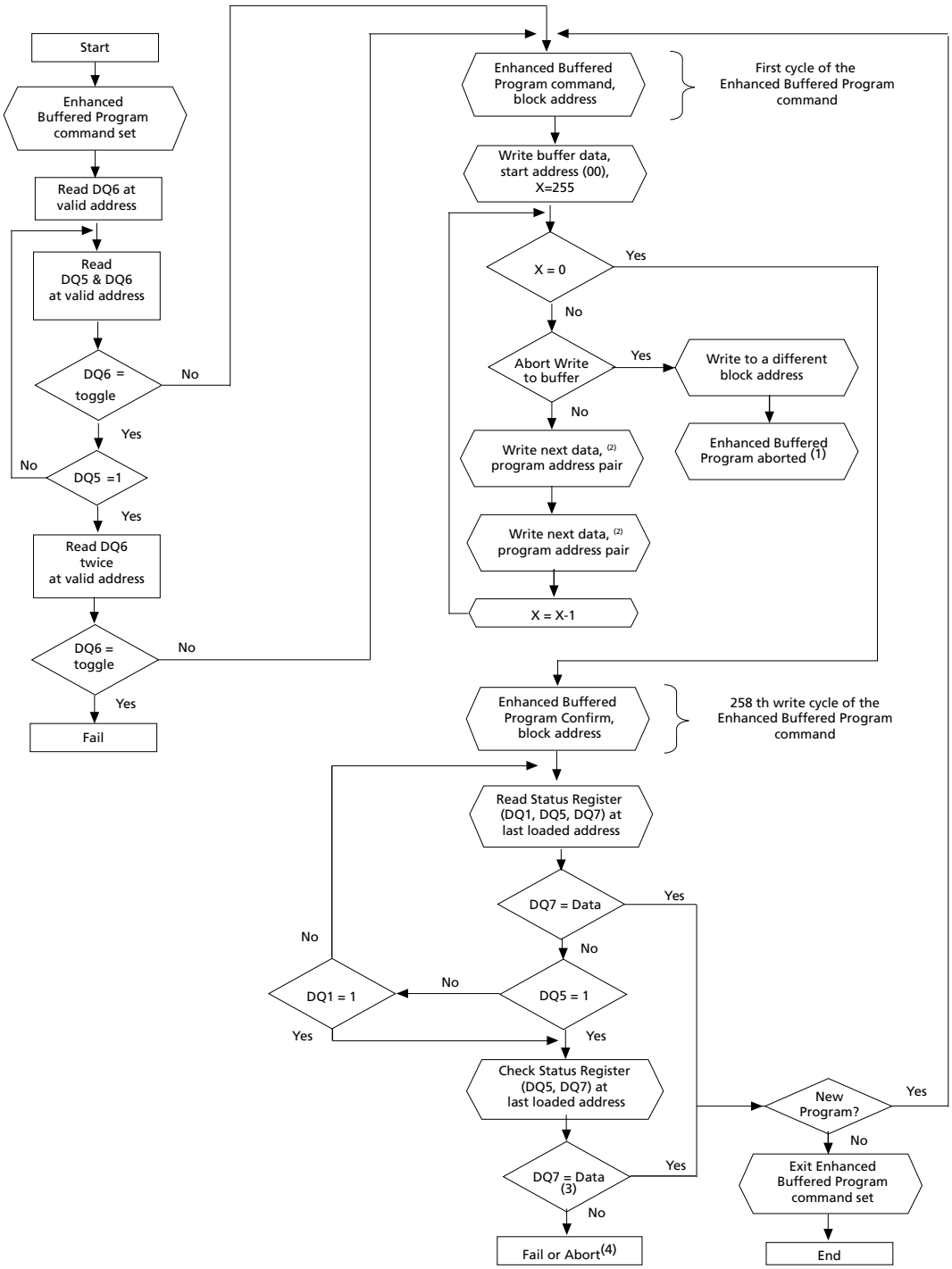
Figure 24: ENHANCED BUFFERED PROGRAM Flowchart



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Notes:
1. The ENHANCED BUFFERED PROGRAM ABORT AND RESET command must be issued to return the device to read mode.
2. When the block address is specified, all addresses in the selected block address space must be issued starting from 00h. Furthermore, when loading the write buffer address with data, data program addresses must be consecutive.
3. DQ7 must be checked since DQ5 and DQ7 may change simultaneously.
4. If this flowchart location is reached because DQ5 = 1, then the ENHANCED WRITE TO BUFFER PROGRAM command failed. If this flowchart location is reached because DQ1 = 1, then the ENHANCED WRITE TO BUFFER PROGRAM command aborted. In both cases, the appropriate RESET command must be issued to return the device to read mode: A RESET command if the operation failed; an ENHANCED WRITE TO BUFFER PROGRAM ABORT AND RESET command if the operation aborted.

ENHANCED BUFFERED PROGRAM ABORT AND RESET Command

An ENHANCED BUFFERED PROGRAM ABORT AND RESET command must be issued to reset the device to read mode when the ENHANCED BUFFERED PROGRAM operation is aborted. The buffer programming sequence can be aborted in the following ways:

- Write to an address in a different block than the one specified during the buffer load.
- Write an address/data pair to a different write buffer page than the one selected by the starting address during the program buffer data loading stage of the operation.
- Write data other than the CONFIRM command after the 256 data load cycles.
- Load a value that is greater than or less than the 256 buffer size.
- Load address/data pairs in an incorrect sequence.

The abort condition is indicated by DQ1 = 1, DQ6 = toggle, and DQ5 = 0 (all of which are status register bits).

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Erase Operations

CHIP ERASE Command

The CHIP ERASE (80/10h) command erases the entire chip. Six bus WRITE operations are required to issue the command and start the program/erase controller.

Protected blocks are not erased. If all blocks are protected, the CHIP ERASE operation appears to start, but will terminate within approximately100µs, leaving the data unchanged. No error is reported when protected blocks are not erased.

During the CHIP ERASE operation, the device ignores all other commands, including ERASE SUSPEND. It is not possible to abort the operation. All bus READ operations during CHIP ERASE output the status register on the data I/Os. See the Status Register section for more details.

After the CHIP ERASE operation completes, the device returns to read mode, unless an error has occurred. If an error occurs, the device will continue to output the status register. A READ/RESET command must be issued to reset the error condition and return to read mode.

The CHIP ERASE command sets all of the bits in unprotected blocks of the device to 1. All previous data is lost.

The operation is aborted by performing a reset or by powering-down the device. In this case, data integrity cannot be ensured, and it is recommended that the entire chip be erased again.

UNLOCK BYPASS CHIP ERASE Command

When the device is in unlock bypass mode, the UNLOCK BYPASS CHIP ERASE (80/10h) command can be used to erase all memory blocks at one time. The command requires only two bus WRITE operations instead of six using the standard CHIP ERASE command. The final bus WRITE operation starts the program/erase controller.

The UNLOCK BYPASS CHIP ERASE command behaves the same way as the CHIP ERASE command: the operation cannot be aborted, and a bus READ operation to the memory outputs the status register.

BLOCK ERASE Command

The BLOCK ERASE (80/30h) command erases a list of one or more blocks. It sets all of the bits in the unprotected selected blocks to 1. All previous data in the selected blocks is lost.

Six bus WRITE operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth bus WRITE operation using the address of the additional block. After the command sequence is written, a block erase timeout occurs. During the timeout period, additional block addresses and BLOCK ERASE commands can be written. After the program/erase controller has started, it is not possible to select any more blocks. Each additional block must therefore be selected within the timeout period of the last block. The timeout timer restarts when an additional block is selected. After the sixth bus WRITE operation, a bus READ operation outputs the status register. See the WE#-Controlled Program waveforms for details on how to identify if the program/erase controller has started the BLOCK ERASE operation.

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After the BLOCK ERASE operation completes, the device returns to read mode, unless an error has occurred. If an error occurs, bus READ operations will continue to output the status register. A READ/RESET command must be issued to reset the error condition and return to read mode.

If any selected blocks are protected, they are ignored, and all the other selected blocks are erased. If all of the selected blocks are protected, the BLOCK ERASE operation appears to start, but will terminate within approximately100µs, leaving the data unchanged. No error condition is given when protected blocks are not erased.

During the BLOCK ERASE operation, the device ignores all commands except the ERASE SUSPEND command and the READ/RESET command, which is accepted only during the timeout period. The operation is aborted by performing a reset or powering-down the device. In this case, data integrity cannot be ensured, and it is recommended that the aborted blocks be erased again.

UNLOCK BYPASS BLOCK ERASE Command

When the device is in unlock bypass mode, the UNLOCK BYPASS BLOCK ERASE (80/30h) command can be used to erase one or more memory blocks at a time. The command requires two bus WRITE operations instead of six using the standard BLOCK ERASE command. The final bus WRITE operation latches the address of the block and starts the program/erase controller.

To erase multiple blocks (after the first two bus WRITE operations have selected the first block in the list), each additional block in the list can be selected by repeating the second bus WRITE operation using the address of the additional block.

The UNLOCK BYPASS BLOCK ERASE command behaves the same way as the BLOCK ERASE command: the operation cannot be aborted, and a bus READ operation to the memory outputs the status register. See the BLOCK ERASE Command section for details.

ERASE SUSPEND Command

The ERASE SUSPEND (B0h) command temporarily suspends a BLOCK ERASE operation. One bus WRITE operation is required to issue the command. The block address is "Don't Care."

The program/erase controller suspends the ERASE operation within the erase suspend latency time of the ERASE SUSPEND command being issued. However, when the ERASE SUSPEND command is written during the block erase timeout, the device immediately terminates the timeout period and suspends the ERASE operation. After the program/erase controller has stopped, the device operates in read mode, and the erase is suspended.

During an ERASE SUSPEND operation, it is possible to read and execute PROGRAM operations or WRITE TO BUFFER PROGRAM operations in blocks that are not suspended. Both READ and PROGRAM operations behave normally on these blocks. Reading from blocks that are suspended will output the status register. If any attempt is made to program in a protected block or in the suspended block, the PROGRAM command is ignored, and the data remains unchanged. In this case, the status register is not read, and no error condition is given.

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It is also possible to issue AUTO SELECT and UNLOCK BYPASS commands during an ERASE SUSPEND operation. The READ/RESET command must be issued to return the device to read array mode before the RESUME command will be accepted.

During an ERASE SUSPEND operation, a bus READ operation to the extended memory block will output the extended memory block data. After the device enters extended memory block mode, the EXIT EXTENDED MEMORY BLOCK command must be issued before the ERASE operation can be resumed.

An ERASE SUSPEND command is ignored if it is written during a CHIP ERASE operation.

If the ERASE SUSPEND operation is aborted by performing a device reset or power-down, data integrity cannot be ensured, and it is recommended that the suspended blocks be erased again.

ERASE RESUME Command

The ERASE RESUME (30h) command restarts the program/erase controller after an ERASE SUSPEND operation.

The device must be in read array mode before the RESUME command will be accepted. An erase can be suspended and resumed more than once.

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Block Protection Command Definitions – Address-Data Cycles

Table 12: Block Protection Command Definitions – Address-Data Cycles, 8-Bit and 16-Bit

Notes 1 and 2 apply to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles											Notes
		1st		2nd		3rd		4th		…	*n*th		
		A	D	A	D	A	D	A	D		A	D	
LOCK REGISTER Commands													
ENTER LOCK REGISTER COMMAND SET (40h)	x8	AAA	AA	555	55	AAA	40						3
	x16	555	AA	2AA	55	555							
PROGRAM LOCK REGISTER (A0h)	x8	X	A0	X	Data								5
	x16												
READ LOCK REGISTER	x8	X	Data										4, 5, 6
	x16												
PASSWORD PROTECTION Commands													
ENTER PASSWORD PROTECTION COMMAND SET (60h)	x8	AAA	AA	555	55	AAA	60						3
	x16	555	AA	2AA	55	555							
PROGRAM PASSWORD (A0h)	x8	X	A0	PWAn	PWDn								7
	x16												
READ PASSWORD	x8	00	PWD0	01	PWD1	02	PWD2	03	PWD3	…	07	PWD7	4, 6, 8, 9
	x16	00	PWD0	01	PWD1	02	PWD2	03	PWD3				
UNLOCK PASSWORD (25h/03)	x8	00	25	00	03	00	PWD0	01	PWD1	…	00	29	8, 10
	x16												
NONVOLATILE PROTECTION Commands													
ENTER NONVOLATILE PROTECTION COMMAND SET (C0h)	x8	AAA	AA	555	55	AAA	C0						3
	x16	555	AA	2AA	55	555							
PROGRAM NONVOLATILE PROTECTION BIT (A0h)	x8	X	A0	BAd	00								
	x16												
READ NONVOLATILE PROTECTION BIT STATUS	x8	BAd	READ(0)										4, 6, 11
	x16												
CLEAR ALL NONVOLATILE PROTECTION BITS (80/30h)	x8	X	80	00	30								12
	x16												
NONVOLATILE PROTECTION BIT LOCK BIT Commands													
ENTER NONVOLATILE PROTECTION BIT LOCK BIT COMMAND SET (50h)	x8	AAA	AA	555	55	AAA	50						3
	x16	555	AA	2AA	55	555							
PROGRAM NONVOLATILE PROTECTION BIT LOCK BIT (A0h)	x8	X	A0	X	00								11
	x16												

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Table 12: Block Protection Command Definitions – Address-Data Cycles, 8-Bit and 16-Bit (Continued)

Notes 1 and 2 apply to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles											Notes
		1st		2nd		3rd		4th		...	*n*th		
		A	D	A	D	A	D	A	D		A	D	
READ NONVOLATILE PROTECTION BIT LOCK BIT STATUS	x8	X	READ(0)										4, 6, 11
	x16												
VOLATILE PROTECTION Commands													
ENTER VOLATILE PROTECTION COMMAND SET (E0h)	x8	AAA	AA	555	55	AAA	E0						3
	x16	555	AA	2AA	55	555							
PROGRAM VOLATILE PROTECTION BIT (A0h)	x8	X	A0	BAd	00								
	x16												
READ VOLATILE PROTECTION BIT STATUS	x8	BAd	READ(0)										4, 6, 11
	x16												
CLEAR VOLATILE PROTECTION BIT (A0h)	x8	X	A0	BAd	01								
	x16												
EXTENDED MEMORY BLOCK Commands													
ENTER EXTENDED MEMORY BLOCK (88h)	x8	AAA	AA	555	55	AAA	88						3
	x16	555	AA	2AA	55	555							
EXIT EXTENDED MEMORY BLOCK (90/00h)	x8	AAA	AA	555	55	AAA	90	X	00				
	x16	555	AA	2AA	55	555							
EXIT PROTECTION Commands													
EXIT PROTECTION COMMAND SET (90/00h)	x8	X	90	X	00								3
	x16												

Notes:
1. Key: A = Address and D = Data; X = "Don't Care;" BAd = any address in the block; PWDn = password bytes 0 to 7; PWAn = password address, n = 0 to 7; Gray = not applicable. All values in the table are hexadecimal.
2. DQ[15:8] are "Don't Care" during UNLOCK and COMMAND cycles. A[MAX:16] are "Don't Care" during UNLOCK and COMMAND cycles, unless an address is required.
3. The ENTER command sequence must be issued prior to any operation. It disables READ and WRITE operations from and to block 0. READ and WRITE operations from and to any other block are allowed. Also, when an ENTER COMMAND SET command is issued, an EXIT PROTECTION COMMAND SET command must be issued to return the device to READ mode.
4. READ REGISTER/PASSWORD commands have no command code; CE# and OE# are driven LOW and data is read according to a specified address.
5. Data = Lock register content.
6. All address cycles shown for this command are READ cycles.
7. Only one portion of the password can be programmed or read by each PROGRAM PASSWORD command.
8. Each portion of the password can be entered or read in any order as long as the entire 64-bit password is entered or read.

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9. For the x8 READ PASSWORD command, the *n*th (and final) address cycle equals the 8th address cycle. From the 5th to the 8th address cycle, the values for each address and data pair continue the pattern shown in the table as follows: for x8, address and data = 04 and PWD4; 05 and PWD5; 06 and PWD6; 07 and PWD7.
10. For the x8 UNLOCK PASSWORD command, the *n*th (and final) address cycle equals the 11th address cycle. From the 5th to the 10th address cycle, the values for each address and data pair continue the pattern shown in the table as follows: address and data = 02 and PWD2; 03 and PWD3; 04 and PWD4; 05 and PWD5; 06 and PWD6; 07 and PWD7.

    For the x16 UNLOCK PASSWORD command, the *n*th (and final) address cycle equals the 7th address cycle. For the 5th and 6th address cycles, the values for the address and data pair continue the pattern shown in the table as follows: address and data = 02 and PWD2; 03 and PWD3.
11. Both nonvolatile and volatile protection bit settings are as follows: Protected state = 00; Unprotected state= 01.
12. The CLEAR ALL NONVOLATILE PROTECTION BITS command programs all nonvolatile protection bits before erasure. This prevents over-erasure of previously cleared nonvolatile protection bits.

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Protection Operations

Blocks can be protected individually against accidental PROGRAM, ERASE, or READ operations on both 8-bit and 16-bit configurations. The block protection scheme is shown in the Software Protection Scheme figure. Memory block and extended memory block protection is configured through the lock register.

LOCK REGISTER Commands

The ENTER LOCK REGISTER COMMAND SET (40h) command enables execution of all READ or PROGRAM LOCK REGISTER commands. PROGRAM LOCK REGISTER (A0h) configures the lock register, and READ LOCK REGISTER reads/confirms programmed data.

PASSWORD PROTECTION Commands

The ENTER PASSWORD PROTECTION COMMAND SET (60h) command enables execution of password protection commands. PROGRAM PASSWORD (A0h) programs the 64-bit password used in the password protection mode. To program the 64-bit password in 8-bit mode, the complete command sequence must be entered eight times at eight consecutive addresses selected by A[1:0] plus DQ15/A-1; in 16-bit mode, the command sequence must be entered four times at four consecutive addresses selected by A[1:0]. By default, all password bits are set to 1. The password can be checked by issuing a READ PASSWORD command.

READ PASSWORD verifies the password used in password protection mode. To verify the 64-bit password in 8-bit mode, the complete command sequence must be entered eight times at eight consecutive addresses selected by A[1:0] plus DQ15/A-1. In 16-bit mode, the command sequence must be entered four times at four consecutive addresses selected by A[1:0]. If the password mode lock bit is programmed and a user attempts to read the password, the device outputs FFh.

UNLOCK PASSWORD (25/03h) clears the nonvolatile protection bit lock bit, allowing the nonvolatile protection bits to be modified. UNLOCK PASSWORD must be issued with the correct password and requires a 1µs delay between successive UNLOCK PASSWORD commands. The delay helps prevent password intruders from trying all possible 64-bit combinations. If the delay does not occur, the latest command is ignored. After a valid 64-bit password is entered, approximately 1µs is required to unlock the device.

NONVOLATILE PROTECTION Commands

The ENTER NONVOLATILE PROTECTION COMMAND SET (C0h) command enables nonvolatile protection mode commands to be issued to the device. A block can be protected from program or erase operations using a PROGRAM NONVOLATILE PROTECTION BIT (A0h) command, along with the block address. This command sets the nonvolatile protection bit to 0 for a given block.

The status of a nonvolatile protection bit for a given block or group of blocks can be read using a READ NONVOLATILE MODIFY PROTECTION BIT command, along with the block address. The nonvolatile protection bits are erased simultaneously using a CLEAR ALL NONVOLATILE PROTECTION BITS (80/30h) command. No specific block address is required. If the nonvolatile protection bit lock bit is set to 0, the command fails.

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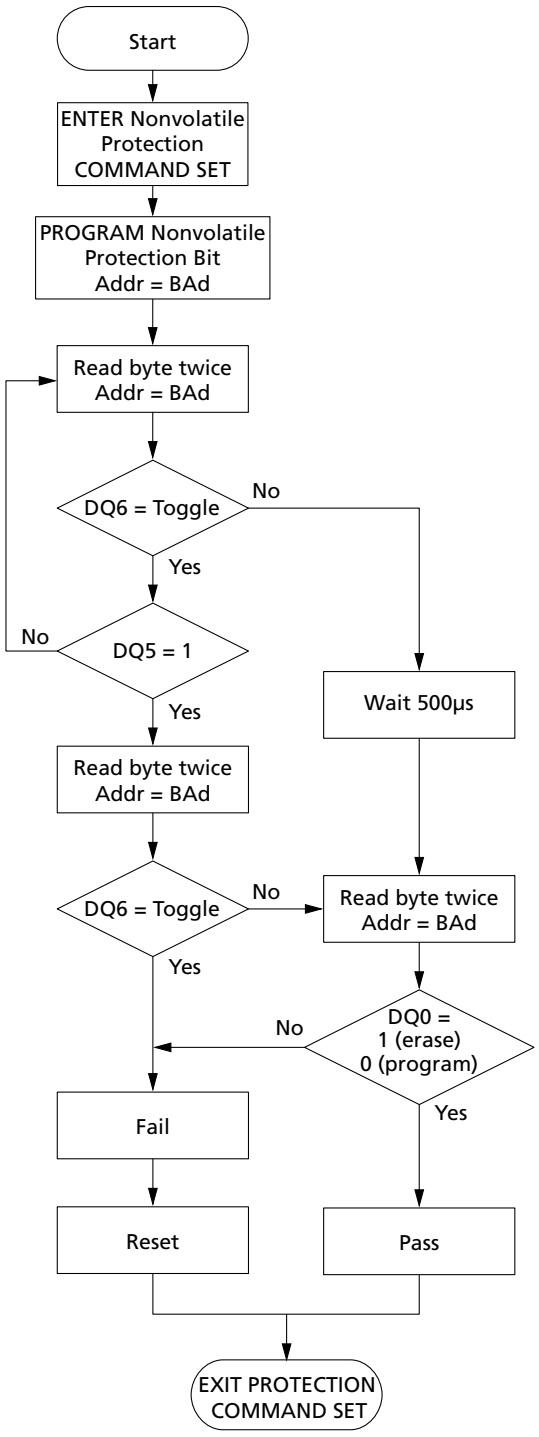
Figure 25: Program/Erase Nonvolatile Protection Bit Algorithm



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NONVOLATILE PROTECTION BIT LOCK BIT Commands

After the ENTER NONVOLATILE PROTECTION BIT LOCK BIT COMMAND SET (50h) command has been issued, the commands that allow the nonvolatile protection bit lock bit to be set can be issued to the device.

The PROGRAM NONVOLATILE PROTECTION BIT LOCK BIT (A0h) command is used to set the nonvolatile protection bit lock bit to 0, thus locking the nonvolatile protection bits and preventing them from being modified.

The READ NONVOLATILE PROTECTION BIT LOCK BIT STATUS command is used to read the status of the nonvolatile protection bit lock bit.

VOLATILE PROTECTION Commands

After the ENTER VOLATILE PROTECTION COMMAND SET (E0h) command has been issued, commands related to the volatile protection mode can be issued to the device.

The PROGRAM VOLATILE PROTECTION BIT (A0h) command individually sets a volatile protection bit to 0 for a given block. If the nonvolatile protection bit for the same block is set, the block is locked regardless of the value of the volatile protection bit. (See the Block Protection Status table.)

The status of a volatile protection bit for a given block can be read by issuing a READ VOLATILE PROTECTION BIT STATUS command along with the block address.

The CLEAR VOLATILE PROTECTION BIT (A0h) command individually clears (sets to 1) the volatile protection bit for a given block. If the nonvolatile protection bit for the same block is set, the block is locked regardless of the value of the volatile protection bit. (See the Block Protection Status table.)

EXTENDED MEMORY BLOCK Commands

The device has one extra 128-word extended memory block that can be accessed only by the ENTER EXTENDED MEMORY BLOCK (88h) command. The extended memory block is 128 words (x16) or 256 bytes (x8). It is used as a security block to provide a permanent 128-bit security identification number or to store additional information. The device can be shipped with the extended memory block prelocked permanently by Micron, including the 128-bit security identification number. Or, the device can be shipped with the extended memory block unlocked, enabling customers to permanently program and lock it. (See Lock Register, the AUTO SELECT command, and the Block Protection table.)

Table 13: Extended Memory Block Address and Data

Address		Data	
x8	x16	Micron prelocked	Customer Lockable
000000h–0000FFh	000000h–00007Fh	Secure ID number	Determined by customer

After the ENTER EXTENDED MEMORY BLOCK command has been issued, the device enters the extended memory block mode. All bus READ or PROGRAM operations are conducted on the extended memory block, and the extended memory block is addressed using the addresses occupied by block 0 in the other operating modes (see the Memory Map table).

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In extended memory block mode, ERASE, CHIP ERASE, ERASE SUSPEND, and ERASE RESUME commands are not allowed. The extended memory block cannot be erased, and each bit of the extended memory block can only be programmed once.

The extended memory block is protected from further modification by programming lock register bit 0. Once invoked, this protection cannot be undone.

The device remains in extended memory block mode until the EXIT EXTENDED MEMORY BLOCK (90/00h) command is issued, which returns the device to read mode, or until power is removed from the device. After a power-up sequence or hardware reset, the device will revert to reading memory blocks in the main array.

EXIT PROTECTION Command

The EXIT PROTECTION COMMAND SET (90/00h) command is used to exit the lock register, password protection, nonvolatile protection, volatile protection, and nonvolatile protection bit lock bit command set modes and return the device to read mode.

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Device Protection

Hardware Protection

The V_{PP}/WP# function provides a hardware method of protecting the highest or lowest block. When V_{PP}/WP# is LOW, PROGRAM and ERASE operations on either of these blocks is ignored to provide protection. When V_{PP}/WP# is HIGH, the device reverts to the previous protection status for the highest or lowest block. PROGRAM and ERASE operations can modify the data in this block unless the block is protected using block protection.

When V_{PP}/write protect is raised to VPPH, the device automatically enters the unlock bypass mode, and command execution time is faster. This must never be done from any mode except read mode; otherwise the device might be left in an indeterminate state.

A 0.1 µF capacitor should be connected between the VPP/write protect pin and the VSS ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during unlock bypass program.

When VPP/write protect returns to HIGH or LOW, normal operation resumes. When operations execute in unlock bypass mode, the device draws IPP from the pin to supply the programming circuits. Transitions from HIGH to VPPH and from VPPH to LOW must be slower than tVHVPP.

Note: Micron highly recommends driving V_{PP}/WP# HIGH or LOW. If a system needs to float the V_{PP}/WP# pin, without a pull-up/pull-down resistor and no capacitor, then an internal pull-up resistor is enabled.

Table 14: V_{PP}/WP# Functions

V_{PP}/WP# Settings	Function
V_{IL}	Highest (29WxxxGH) or lowest (29WxxxGL) block is protected.
V_{IH}	Highest or lowest block is unprotected unless software protection is activated.
V_{PPH}	Unlock bypass mode supplies current necessary to speed up PROGRAM execution time.

Software Protection

Software protection includes volatile, nonvolatile, and password protection as well as password access. The device is shipped with all blocks unprotected. On first use, the device defaults to the nonvolatile protection mode but can be activated in either the nonvolatile protection or password protection mode.

The desired protection mode is activated by setting either the nonvolatile protection mode lock bit or the password protection mode lock bit of the lock register (see the Lock Register section). Both bits are one-time-programmable and nonvolatile; therefore, after the protection mode has been activated, it cannot be changed, and the device is set permanently to operate in the selected protection mode. It is recommended that the desired software protection mode be activated when first programming the device.

For the lowest and highest blocks, a higher level of block protection can be achieved by locking the blocks using nonvolatile protection mode and holding V_{PP} /WP# LOW.

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Blocks with volatile protection and nonvolatile protection can coexist within the memory array. If the user attempts to program or erase a protected block, the device ignores the command and returns to read mode.

The block protection status can be read by performing a read electronic signature or by issuing an AUTO SELECT command (see the Block Protection table).

Refer to the Block Protection Status table and the Software Protection Scheme figure for details on the block protection scheme. Refer to the Protection Operations section for a description of the command sets.

Volatile Protection Mode

Volatile protection enables the software application to protect blocks against inadvertent change and can be disabled when changes are needed. Volatile protection bits are unique for each block and can be individually modified. Volatile protection bits control the protection scheme only for unprotected blocks whose nonvolatile protection bits are cleared to 1. Issuing a PROGRAM VOLATILE PROTECTION BIT or CLEAR VOLATILE PROTECTION BIT command sets to 0 or clears to 1 the volatile protection bits and places the associated blocks in the protected (0) or unprotected (1) state, respectively. The volatile protection bit can be set or cleared as often as needed.

When the device is first shipped, or after a power-up or hardware reset, the volatile protection bits default to 1 (unprotected).

Nonvolatile Protection Mode

A nonvolatile protection bit is assigned to each block. Each of these bits can be set for protection individually by issuing a PROGRAM NONVOLATILE PROTECTION BIT command. Also, each device has one global volatile bit called the nonvolatile protection bit lock bit; it can be set to protect all nonvolatile protection bits at once. This global bit must be set to 0 only after all nonvolatile protection bits are configured to the desired settings. When set to 0, the nonvolatile protection bit lock bit prevents changes to the state of the nonvolatile protection bits. When cleared to 1, the nonvolatile protection bits can be set and cleared using the PROGRAM NONVOLATILE PROTECTION BIT and CLEAR ALL NONVOLATILE PROTECTION BITS commands, respectively.

No software command unlocks the nonvolatile protection bit lock bit unless the device is in password protection mode; in nonvolatile protection mode, the nonvolatile protection bit lock bit can be cleared only by taking the device through a hardware reset or power-up.

Nonvolatile protection bits cannot be cleared individually; they must be cleared all at once using a CLEAR ALL NONVOLATILE PROTECTION BITS command. They will remain set through a hardware reset or a power-down/power-up sequence.

If one of the nonvolatile protection bits needs to be cleared (unprotected), additional steps are required: First, the nonvolatile protection bit lock bit must be cleared to 1, using either a power-cycle or hardware reset. Then, the nonvolatile protection bits can be changed to reflect the desired settings. Finally, the nonvolatile protection bit lock bit must be set to 0 to lock the nonvolatile protection bits. The device now will operate normally.

To achieve the best protection, the PROGRAM NONVOLATILE PROTECTION LOCK BIT command should be executed early in the boot code, and the boot code should be protected by holding V_{PP}/WP# LOW.

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Nonvolatile protection bits and volatile protection bits have the same function when V_{PP}/WP# is HIGH or when V_{PP}/WP# is at the voltage for program acceleration (V_{PPH}).

Password Protection Mode

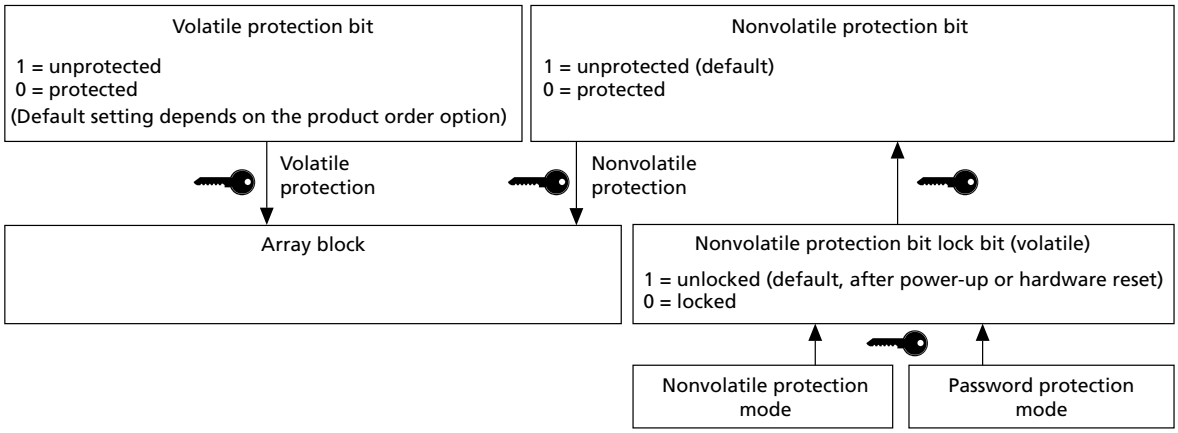
Password protection mode provides a higher level of security than the nonvolatile protection mode by requiring a 64-bit password to unlock the nonvolatile protection bit lock bit. In addition to this password requirement, the nonvolatile protection bit lock bit is set to 0 after power-up and reset to maintain the device in password protection mode.

Executing the UNLOCK PASSWORD command by entering the correct password clears the nonvolatile protection bit lock bit, enabling the block nonvolatile protection bits to be modified. If the password provided is incorrect, the nonvolatile protection bit lock bit remains locked, and the state of the nonvolatile protection bits cannot be modified.

To place the device in password protection mode, the following two steps are required: First, before activating the password protection mode, a 64-bit password must be set and the setting verified. Password verification is allowed only before the password protection mode is activated. Next, password protection mode is activated by programming the password protection mode lock bit to 0. This operation is irreversible. After the bit is programmed, it cannot be erased, the device remains permanently in password protection mode, and the 64-bit password can be neither retrieved nor reprogrammed. In addition, all commands to the address where the password is stored are disabled.

Note: There is no means to verify the password after password protection mode is enabled. If the password is lost after enabling the password protection mode, there is no way to clear the nonvolatile protection bit lock bit.

Figure 26: Software Protection Scheme



Notes:
1. Volatile protection bits are programmed and cleared individually. Nonvolatile protection bits are programmed individually and cleared collectively.
2. Once programmed to 0, the nonvolatile protection bit lock bit can be reset to 1 only by taking the device through a power-up or hardware reset.

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Common Flash Interface

The common Flash interface (CFI) is a JEDEC-approved, standardized data structure that can be read from the Flash memory device. It allows a system's software to query the device to determine various electrical and timing parameters, density information, and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the READ CFI command is issued, the device enters CFI query mode and the data structure is read from memory. The following tables show the addresses (A-1, A[7:0]) used to retrieve the data. The query data is always presented on the lowest order data outputs (DQ[7:0]), and the other data outputs (DQ[15:8]) are set to 0.

Table 15: Query Structure Overview

Note 1 applies to the entire table

Address		Subsection Name	Description
x16	x8		
10h	20h	CFI query identification string	Command set ID and algorithm data offset
1Bh	36h	System interface information	Device timing and voltage information
27h	4Eh	Device geometry definition	Flash device layout
40h	80h	Primary algorithm-specific extended query table	Additional information specific to the primary algorithm (optional)
61h	C2h	Security code area	64-bit unique device number

Note: 1. Query data are always presented on the lowest order data outputs (DQ[7:0]). DQ[15:8] are set to 0.

Table 16: CFI Query Identification String

Note 1 applies to the entire table

Address		Data	Description	Value
x16	x8			
10h	20h	0051h	Query unique ASCII string "QRY"	"Q"
11h	22h	0052h		"R"
12h	24h	0059h		"Y"
13h 14h	26h 28h	0002h 0000h	Primary algorithm command set and control interface ID code 16-bit ID code defining a specific algorithm	–
15h 16h	2Ah 2Ch	0040h 0000h	Address for primary algorithm extended query table (see the Primary Algorithm-Specific Extended Query Table)	P = 40h
17h 18h	2Eh 30h	0000h 0000h	Alternate vendor command set and control interface ID code second vendor-specified algorithm supported	–
19h 1Ah	32h 34h	0000h 0000h	Address for alternate algorithm extended query table	–

Note: 1. Query data are always presented on the lowest order data outputs (DQ[7:0]). DQ[15:8] are set to 0.

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Table 17: CFI Query System Interface Information

Note 1 applies to the entire table

Address		Data	Description	Value
x16	x8			
1Bh	36h	0027h	V_{CC} logic supply minimum program/erase voltage Bits[7:4] BCD value in volts Bits[3:0] BCD value in 100mV	2.7V
1Ch	38h	0036h	V_{CC} logic supply maximum program/erase voltage Bits[7:4] BCD value in volts Bits[3:0] BCD value in 100mV	3.6V
1Dh	3Ah	00B5h	V_{PPH} (programming) supply minimum program/erase voltage Bits[7:4] hex value in volts Bits[3:0] BCD value in 100mV	11.5V
1Eh	3Ch	00C5h	V_{PPH} (programming) supply maximum program/erase voltage Bits[7:4] hex value in volts Bits[3:0] BCD value in 100mV	12.5V
1Fh	3Eh	0004h	Typical timeout for single byte/word program = 2^nµs	16µs
20h	40h	0004h	Typical timeout for maximum size buffer program = 2^nµs	16µs
21h	42h	0009h	Typical timeout per individual block erase = 2^nms	0.5s
22h	44h	0011h	Typical timeout for full chip erase = 2^nms	80s
23h	46h	0004h	Maximum timeout for byte/word program = 2^n times typical	200µs
24h	48h	0004h	Maximum timeout for buffer program = 2^n times typical	200µs
25h	4Ah	0003h	Maximum timeout per individual block erase = 2^n times typical	2.3s
26h	4Ch	0004h	Maximum timeout for chip erase = 2^n times typical	800s

Note: 1. The values in this table are valid for both packages.

Table 18: Device Geometry Definition

Address		Data	Description	Value
x16	x8			
27h	4Eh	0019h	Device size = 2^n in number of bytes	32MB
28h 29h	50h 52h	0002h 0000h	Flash device interface code description	x8, x16 asynchronous
2Ah 2Bh	54h 56h	0006h 0000h	Maximum number of bytes in multi-byte program or page = 2^n	64
2Ch	58h	0001h	Number of erase block regions. It specifies the number of regions containing contiguous erase blocks of the same size.	1
2Dh 2Eh	5Ah 5Ch	00FFh 0000h	Erase block region 1 information Number of identical-size erase blocks = 00FFh + 1	256
2Fh 30h	5Eh 60h	0000h 0002h	Erase block region 1 information Block size in region 1 = 0200h × 256 bytes	128KB

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Table 18: Device Geometry Definition (Continued)

Address		Data	Description	Value
x16	x8			
31h 32h 33h 34h	62h 64h 66h 68h	0000h 0000h 0000h 0000h	Erase block region 2 information	0
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase block region 3 information	0
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase block region 4 information	0

Table 19: Primary Algorithm-Specific Extended Query Table

Note 1 applies to the entire table

Address		Data	Description	Value
x16	x8			
40h	80h	0050h	Primary algorithm extended query table unique ASCII string “PRI”	"P"
41h	82h	0052h		"R"
42h	84h	0049h		"I"
43h	86h	0031h	Major version number, ASCII	"1"
44h	88h	0033h	Minor version number, ASCII	"3"
45h	8Ah	0010h	Address sensitive unlock (bits[1:0]): 00 = Required 01 = Not required Silicon revision number (bits[7:2])	Yes 65nm
46h	8Ch	0002h	Erase suspend: 00 = Not supported 01 = Read only 02 = Read and write	2
47h	8Eh	0001h	Block protection: 00 = Not supported x = Number of blocks per group	1
48h	90h	0000h	Temporary block unprotect: 00 = Not supported 01 = Supported	00
49h	92h	0008h	Block protect/unprotect: 06 = M29W256GH/M29W256GL	06
4Ah	94h	0000h	Simultaneous operations: Not supported	–

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Table 19: Primary Algorithm-Specific Extended Query Table (Continued)

Note 1 applies to the entire table

Address		Data	Description	Value
x16	x8			
4Bh	96h	0000h	Burst mode: 00 = Not supported 01 = Supported	00
4Ch	98h	0002h	Page mode: 00 = Not supported 02 = 8-word page	02
4Dh	9Ah	00B5h	V_{PPH} supply minimum program/erase voltage: Bits[7:4] hex value in volts Bits[3:0] BCD value in 100mV	11.5V
4Eh	9Ch	00C5h	V_{PPH} supply maximum program/erase voltage: Bits[7:4] hex value in volts Bits[3:0] BCD value in 100mV	12.5V
4Fh	9Eh	00xxh	Top/bottom boot block flag: xx = 04h: M29W256GL, first block protected by V_{PP}/WP# xx = 05h: M29W256GL, last block protected by V_{PP}/WP#	Uniform + V_{PP}/WP# protecting highest or lowest block
50h	A0h	0001h	Program suspend: 00 = Not supported 01 = Supported	01

Note: 1. The values in this table are valid for both packages.

Table 20: Security Code Area

Address		Data	Description
x16	x8		
61h	C3h, C2h	XXXX	64-bit unique device number
62h	C5h, C4h	XXXX	
63h	C7h, C6h	XXXX	
64h	C9h, C8h	XXXX	

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Power-Up and Reset Characteristics

Table 21: Power-Up Wait Timing Specifications

Note 1 applies to the entire table

Parameter	Symbol		Min	Unit	Notes
	Legacy	JEDEC			
V_{CC} HIGH to CE# LOW	^{t}VCH	^{t}VCHEL	55	µs	2, 3
V_{CCQ} HIGH to CE# LOW	–	^{t}VCQHEL	55	µs	2, 3
V_{CC} HIGH to WE# LOW	–	^{t}VCHWL	500	µs	
V_{CCQ} HIGH to WE# LOW	–	^{t}VCQHWL	500	ns	

Notes:
1. Specifications apply to 60, 70, and 80ns devices unless otherwise noted. The 60ns device is available upon customer request.
2. V_{CC} and V_{CCQ} ramps must be synchronized during power-up.
3. If RST# is not stable for ^{t}VCS or ^{t}VIOS, the device will not allow any READ or WRITE operations, and a hardware reset is required.

Figure 27: Power-Up Timing

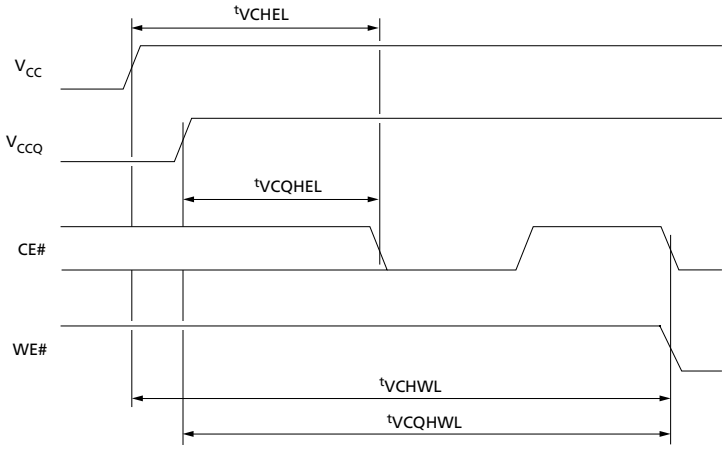

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Table 22: Reset AC Specifications

Note 1 applies to the entire table

Condition/Parameter	Symbol		Min	Max	Unit	Notes
	Legacy	JEDEC				
RST# LOW to read mode during program or erase	^{t}READY	^{t}PLRH	–	55	µs	2
RST# pulse width	^{t}RP	^{t}PLPH	20	–	µs	
RST# HIGH to CE# LOW, OE# LOW	^{t}RH	^{t}PHEL, ^{t}PHGL, ^{t}PHWL	55	–	ns	2
RST# LOW to standby mode during read mode	^{t}RPD	–	20	–	µs	
RST# LOW to standby mode during program or erase			55	–	µs	
RY/BY# HIGH to CE# LOW, OE# LOW	^{t}RB	^{t}RHEL, ^{t}RHGL, ^{t}RHWL	0	–	ns	2

Notes:
1. Specifications apply to 60, 70, and 80ns devices unless otherwise noted. The 60ns device is available upon customer request.
2. Sampled only; not 100% tested.

Figure 28: Reset AC Timing – No PROGRAM/ERASE Operation in Progress

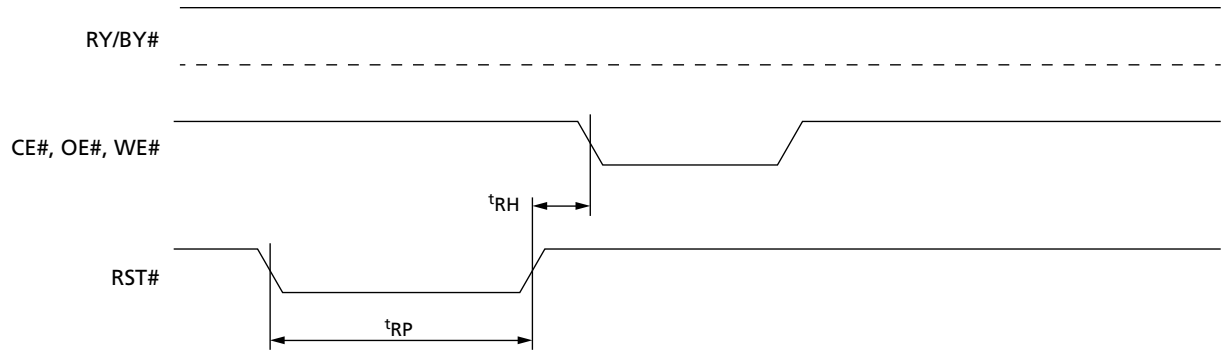

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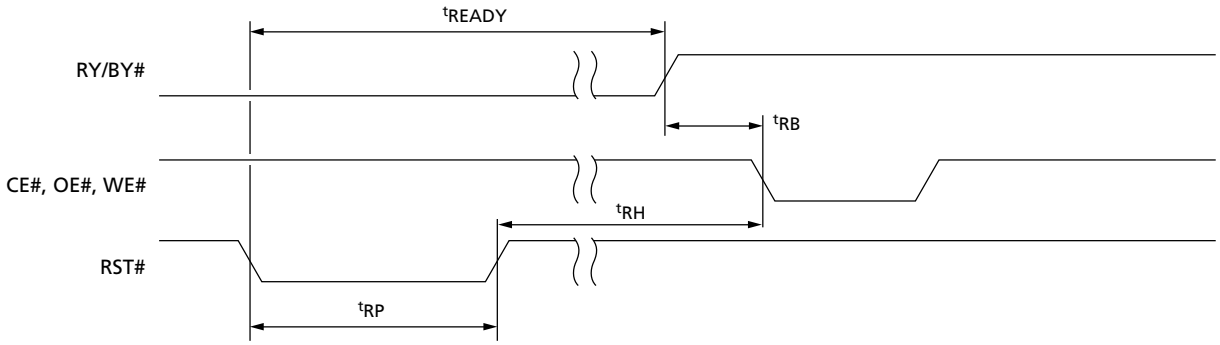
Figure 29: Reset AC Timing During PROGRAM/ERASE Operation



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Absolute Ratings and Operating Conditions

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 23: Absolute Maximum/Minimum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Temperature under bias	T_{BIAS}	–50	125	°C	
Storage temperature	T_{STG}	–65	150	°C	
Input/output voltage	V_{IO}	–0.6	V_{CC} + 0.6	V	1, 2
Supply voltage	V_{CC}	–0.6	4	V	
Input/output supply voltage	V_{CCQ}	–0.6	4	V	
Identification voltage	V_{ID}	–0.6	13.5	V	
Program voltage	V_{PPH}	–0.6	13.5	V	3

Notes:
1. During signal transitions, minimum voltage may undershoot to –2V for periods less than 20ns.
2. During signal transitions, maximum voltage may overshoot to V_{CC} + 2V for periods less than 20ns.
3. V_{PPH} must not remain at 12V for more than 80 hours cumulative.

Table 24: Operating Conditions

Note 1 applies to the entire table.

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage	V_{CC}	2.7	3.6	V	
Input/output supply voltage ($V_{CCQ} \le V_{CC}$)	V_{CCQ}	1.65	3.6	V	2
Ambient operating temperature (range 1)	T_A	0	70	°C	
Ambient operating temperature (range 6)	T_A	–40	125	°C	
Load capacitance	C_L	30		pF	
Input rise and fall times	–	–	10	ns	
Input pulse voltages	–	0 to V_{CCQ}		V	
Input and output timing reference voltages	–	$V_{CCQ}/2$		V	

Notes:
1. Specifications apply to 60, 70, and 80ns devices unless otherwise noted. The 60ns device is available upon customer request.
2. For the 80ns device, input/output supply voltage ($V_{CCQ} \le V_{CC}$) = 1.65V (MIN) and 3.6V (MAX). For the 60ns and 70ns devices, input/output supply voltage ($V_{CCQ} \le V_{CC}$) = 2.7V (MIN) and 3.6V (MAX).

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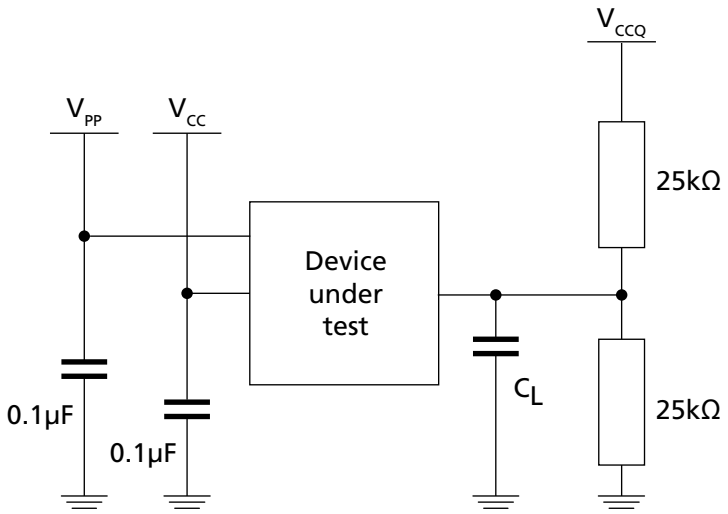
Figure 30: AC Measurement Load Circuit



Note: 1. C_L includes jig capacitance.

Figure 31: AC Measurement I/O Waveform

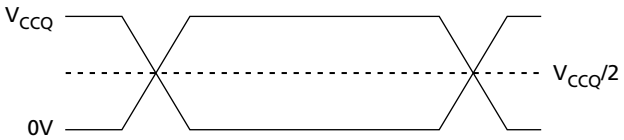


Table 25: Input/Output Capacitance[1]

Parameter	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	–	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0V	–	12	pF

Note: 1. Sampled only, not 100% tested.

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DC Characteristics

Table 26: DC Current Characteristics

Parameter		Symbol	Conditions		Min	Typ	Max	Unit	Notes
Input leakage current		I_{LI}	$0V \le V_{IN} \le V_{CC}$		–	–	±1	µA	1
Output leakage current		I_{LO}	$0V \le V_{OUT} \le V_{CC}$		–	–	±1	µA	
VCC read current	Random read	I_{CC1}	CE# = V_{IL}, OE# = V_{IH}, f = 6 MHz		–	–	10	mA	
	Page read		CE# = V_{IL}, OE# = V_{IH}, f = 10 MHz		–	–	1	mA	
VCC standby current	Grade 6	I_{CC2}	CE# = V_{CCQ} ±0.2V, RST# = V_{CCQ} ±0.2V		–	–	100	µA	2
	Grade 3				–	–	200	µA	2
VCC program/erase current		I_{CC3}	Program/ erase controller active	V_{PP}/WP# = V_{IL} or V_{IH}	–	–	20	mA	3
				V_{PP}/WP# = V_{PPH}	–	–	15	mA	
V_{PP} current	Read	I_{PP1}	V_{PP}/WP# ≤ V_{CC}		–	1	5	µA	
	Standby				–	1	5	µA	
	Reset	I_{PP2}	RST# = V_{SS} ±0.2V		–	1	5	µA	
	PROGRAM operation ongoing	I_{PP3}	V_{PP}/WP# = 12V ±5%		–	1	10	mA	
			V_{PP}/WP# = V_{CC}		–	1	5	mA	
	ERASE operation ongoing	I_{PP4}	V_{PP}/WP# = 12V ±5%		–	3	10	mA	
			V_{PP}/WP# = V_{CC}		–	1	5	mA	

Notes:
1. The maximum input leakage current is ±5µA on the V_{PP}/WP# pin.
2. When the bus is inactive for ^{t}AVQV +30ns or more, the memory enters automatic standby.
3. Sampled only; not 100% tested.

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Table 27: DC Voltage Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Notes
Input LOW voltage	V_{IL}	$V_{CC} \geq 2.7V$	–0.5	–	$0.3V_{CCQ}$	V	
Input HIGH voltage	V_{IH}	$V_{CC} \geq 2.7V$	$0.7V_{CCQ}$	–	$V_{CCQ} + 0.4$	V	
Output LOW voltage	V_{OL}	$I_{OL} = 100\mu A$, $V_{CC} = V_{CC,min}$, $V_{CCQ} = V_{CCQ,min}$	–	–	$0.15V_{CCQ}$	V	
Output HIGH voltage	V_{OH}	$I_{OH} = 100\mu A$, $V_{CC} = V_{CC,min}$, $V_{CCQ} = V_{CCQ,min}$	$0.85V_{CCQ}$	–	–	V	
Identification voltage	V_{ID}	–	11.5	–	12.5	V	
Voltage for V_{PP}/WP# program acceleration	V_{PPH}	–	11.5	–	12.5	V	
Program/erase lockout supply voltage	V_{LKO}	–	1.8	–	2.5	V	1

Note: 1. Sampled only; not 100% tested.

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Read AC Characteristics

Table 28: Read AC Characteristics

Parameter	Symbol		Condition	60ns $V_{CCQ} = V_{CC}$		70ns $V_{CCQ} = V_{CC}$		80ns V_{CCQ} = 1.65V to V_{CC}		Unit	Notes
	Legacy	JEDEC		Min	Max	Min	Max	Min	Max		
Address valid to next address valid	tRC	tAVAV	CE# = V_{IL}, OE# = V_{IL}	60	–	70	–	80	–	ns	
Address valid to output valid	tACC	tAVQV	CE# = V_{IL}, OE# = V_{IL}	–	60	–	70	–	80	ns	
Address valid to output valid (page)	tPAGE	tAVQV1	CE# = V_{IL}, OE# = V_{IL}	–	25	–	25	–	30	ns	
CE# LOW to output transition	tLZ	tELQX	OE# = V_{IL}	0	–	0	–	0	–	ns	2
CE# LOW to output valid	tE	tELQV	OE# = V_{IL}	–	60	–	70	–	80	ns	
OE# LOW to output transition	tOLZ	tGLQX	CE# = V_{IL}	0	–	0	–	0	–	ns	2
OE# LOW to output valid	tOE	tGLQV	CE# = V_{IL}	–	25	–	25	–	30	ns	
CE# HIGH to output High-Z	tHZ	tEHQZ	OE# = V_{IL}	–	25	–	25	–	30	ns	2
OE# HIGH to output High-Z	tDF	tGHQZ	CE# = V_{IL}	–	25	–	25	–	30	ns	2
CE#, OE#, or address transition to output transition	tOH	tEHQX, tGHQX, tAXQX	–	0	–	0	–	0	–	ns	
		tEHQV									
CE# to BYTE# LOW	tELFL	tELBL	–	–	5	–	5	–	5	ns	
CE# to BYTE# HIGH	tELFH	tELBH	–	–	5	–	5	–	5	ns	
		tELQZ									
BYTE# LOW to output HIgh-Z	tFLQZ	tBLQZ	–	–	25	–	25	–	30	ns	
BYTE# HIGH to output valid	tFHQV	tBHQV	–	–	30	–	30	–	30	ns	

Notes:
1. The 60ns device is available upon customer request.
2. Sampled only; not 100% tested.

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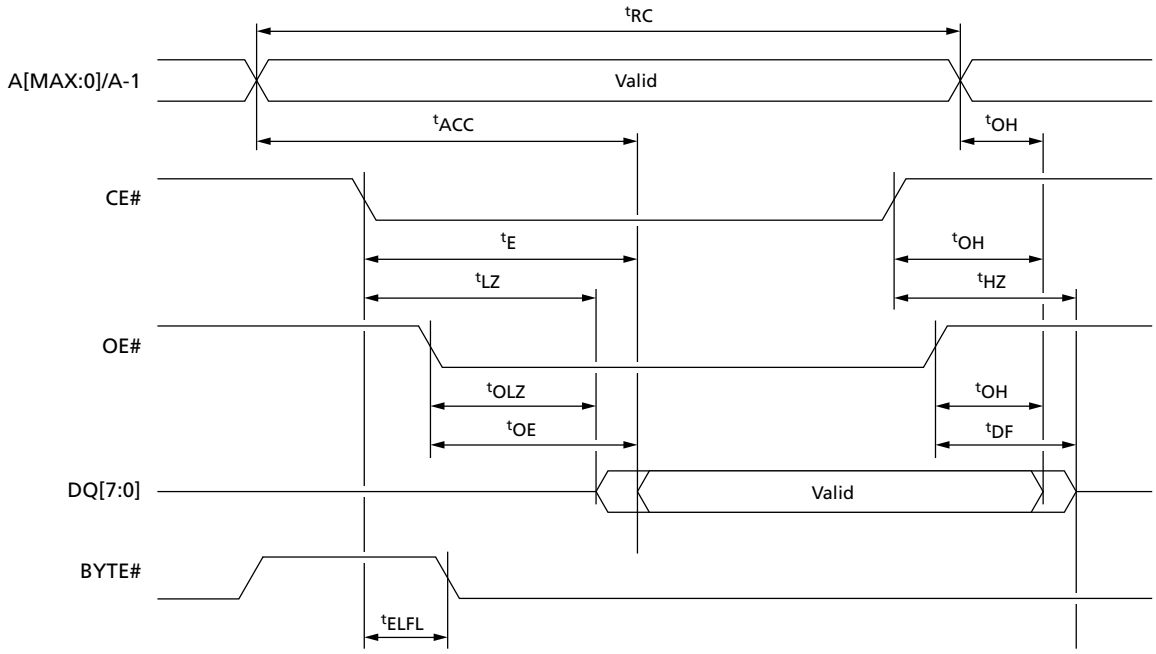
Figure 32: Random Read AC Timing (8-Bit Mode)



Note: 1. BYTE# = V_{IL}

Figure 33: Random Read AC Timing (16-Bit Mode)

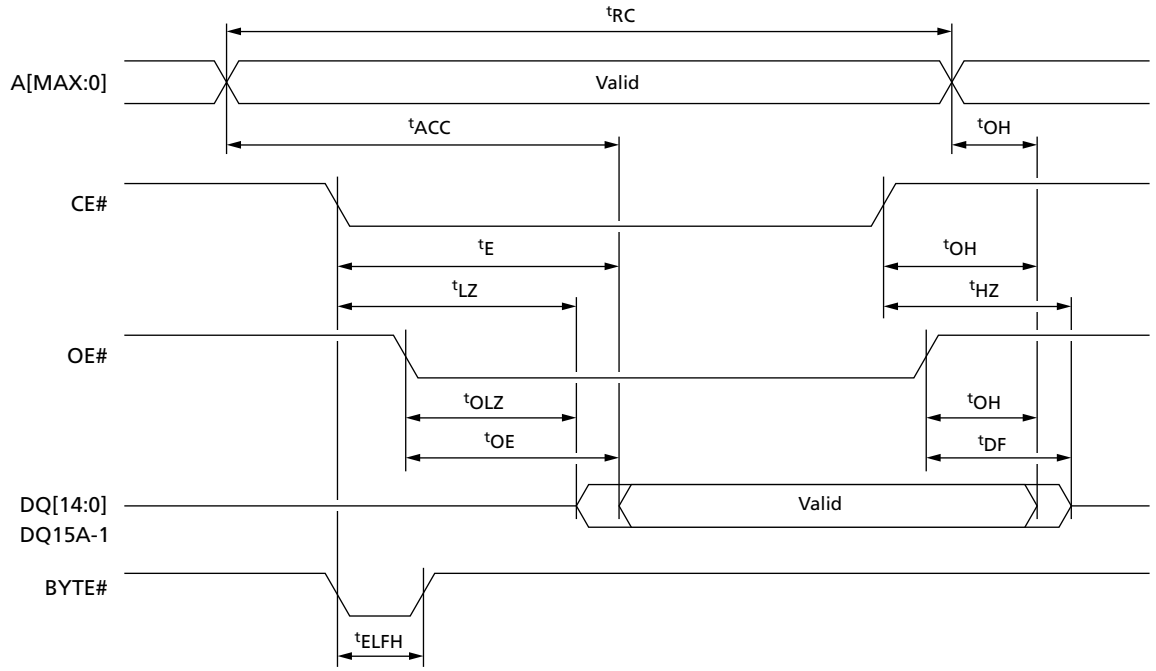


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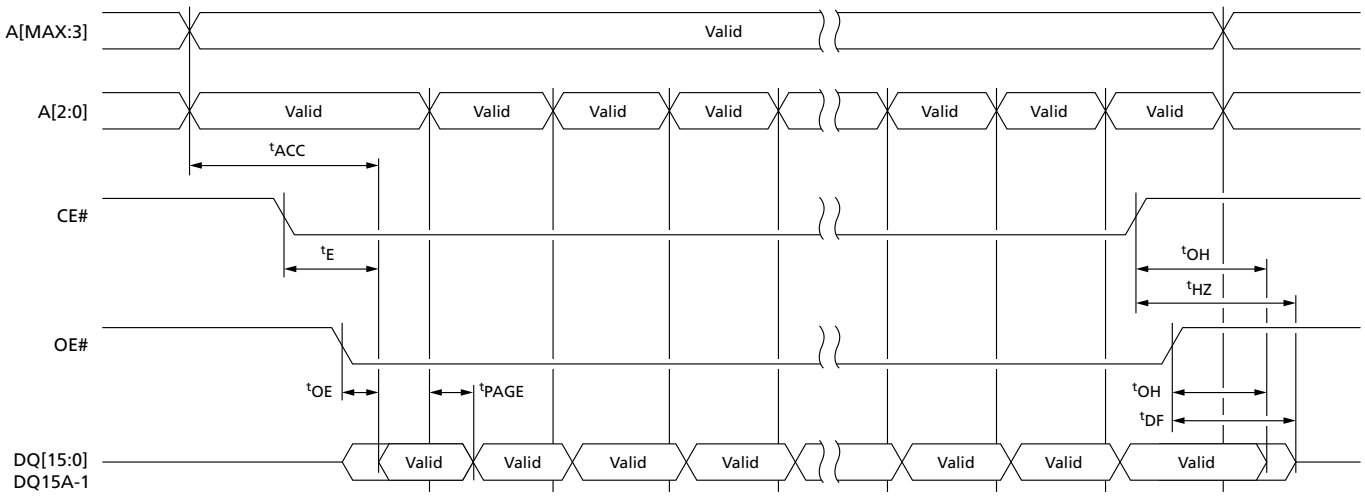
Figure 34: Page Read AC Timing (16-Bit Mode)



Note: 1. Page size is 8 words (16 bytes) and is addressed by address inputs A[2:0] in x16 bus mode and A[2:0] plus DQ15/A–1 in x8 bus mode.

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Write AC Characteristics

Table 29: WE#-Controlled Write AC Characteristics

Parameter	Symbol		60ns[2] $V_{CCQ} = V_{CC}$		70ns $V_{CCQ} = V_{CC}$		80ns V_{CCQ} = 1.65V to V_{CC}		Unit	Notes
	Legacy	JEDEC	Min	Max	Min	Max	Min	Max		
Address valid to next address valid	^{t}WC	^{t}AVAV	65	–	75	–	85	–	ns	
CE# LOW to WE# LOW	^{t}CS	^{t}ELWL	0	–	0	–	0	–	ns	
WE# LOW to WE# HIGH	^{t}WP	^{t}WLWH	35	–	35	–	35	–	ns	
Input valid to WE# HIGH	^{t}DS	^{t}DVWH	45	–	45	–	45	–	ns	2
WE# HIGH to input transition	^{t}DH	^{t}WHDX	0	–	0	–	0	–	ns	
WE# HIGH to CE# HIGH	^{t}CH	^{t}WHEH	0	–	0	–	0	–	ns	
WE# HIGH to WE# LOW	^{t}WPH	^{t}WHWL	30	–	30	–	30	–	ns	
Address valid to WE# LOW	^{t}AS	^{t}AVWL	0	–	0	–	0	–	ns	
WE# LOW to address transition	^{t}AH	^{t}WLAX	45	–	45	–	45	–	ns	
OE# HIGH to WE# LOW	–	^{t}GHWL	0	–	0	–	0	–	ns	
WE# HIGH to OE# LOW	^{t}OEH	^{t}WHGL	0	–	0	–	0	–	ns	
Program/erase valid to RY/BY# LOW	^{t}BUSY	^{t}WHRL	–	30	–	30	–	30	ns	3
V_{CC} HIGH to CE# LOW	^{t}VCS	^{t}VCHEL	50	–	50	–	50	–	µs	

Notes:
1. The 60ns device is available upon customer request.
2. The user's write timing must comply with this specification. Any violation of this write timing specification may result in permanent damage to the NOR Flash device.
3. Sampled only; not 100% tested.

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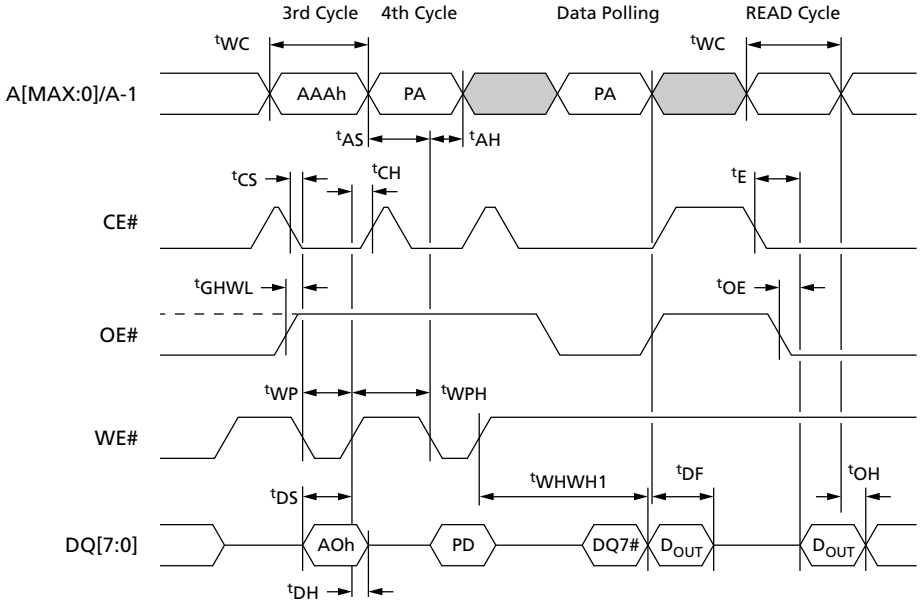
Figure 35: WE#-Controlled Program AC Timing (8-Bit Mode)



Notes:
1. Only the third and fourth cycles of the PROGRAM command are represented. The PROGRAM command is followed by checking of the status register data polling bit and by a READ operation that outputs the data (D_{OUT}) programmed by the previous PROGRAM command.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (See Data Polling Bit [DQ7]).
4. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

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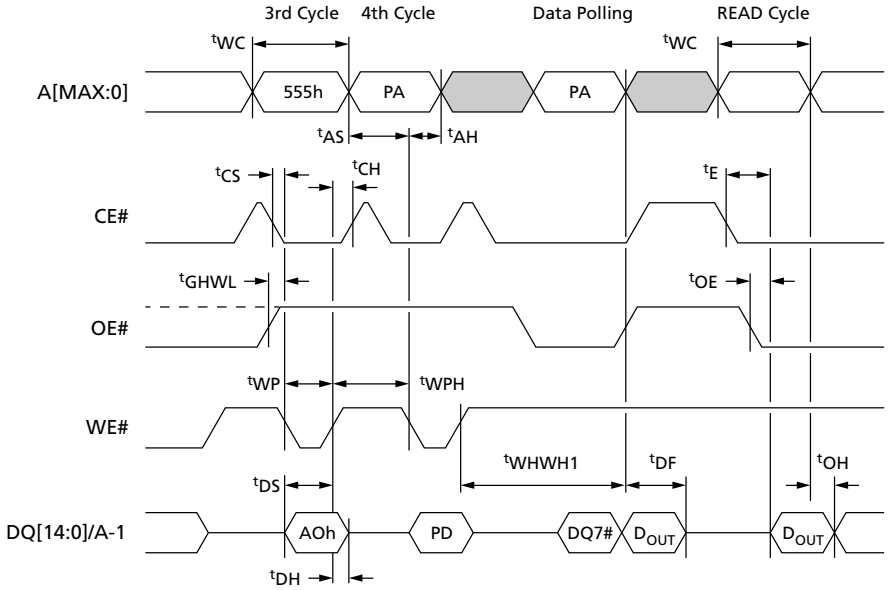
Figure 36: WE#-Controlled Program AC Timing (16-Bit Mode)



Notes:
1. Only the third and fourth cycles of the PROGRAM command are represented. The PROGRAM command is followed by checking of the status register data polling bit and by a READ operation that outputs the data (D_{OUT}) programmed by the previous PROGRAM command.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (See Data Polling Bit [DQ7]).
4. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

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Table 30: CE#-Controlled Write AC Characteristics

Parameter	Symbol		60ns[2] $V_{CCQ} = V_{CC}$		70ns $V_{CCQ} = V_{CC}$		80ns V_{CCQ} = 1.65V to V_{CC}		Unit	Notes
	Legacy	JEDEC	Min	Max	Min	Max	Min	Max		
Address valid to next address valid	tWC	tAVAV	65	–	75	–	85	–	ns	
WE# LOW to CE# LOW	tWS	tWLEL	0	–	0	–	0	–	ns	
CE# LOW to CE# HIGH	tCP	tELEH	35	–	35	–	35	–	ns	
Input valid to CE# HIGH	tDS	tDVEH	45	–	45	–	45	–	ns	2
CE# HIGH to input transition	tDH	tEHDX	0	–	0	–	0	–	ns	
CE# HIGH to WE# HIGH	tWH	tEHWH	0	–	0	–	0	–	ns	
CE# HIGH to CE# LOW	tCPH	tEHEL	30	–	30	–	30	–	ns	
Address valid to CE# LOW	tAS	tAVEL	0	–	0	–	0	–	ns	
CE# LOW to address transition	tAH	tELAX	45	–	45	–	45	–	ns	
OE# HIGH to CE# LOW	–	tGHEL	0	–	0	–	0	–	ns	

Notes:
1. The 60ns device is available upon customer request.
2. The user's write timing must comply with this specification. Any violation of this write timing specification may result in permanent damage to the NOR Flash device.

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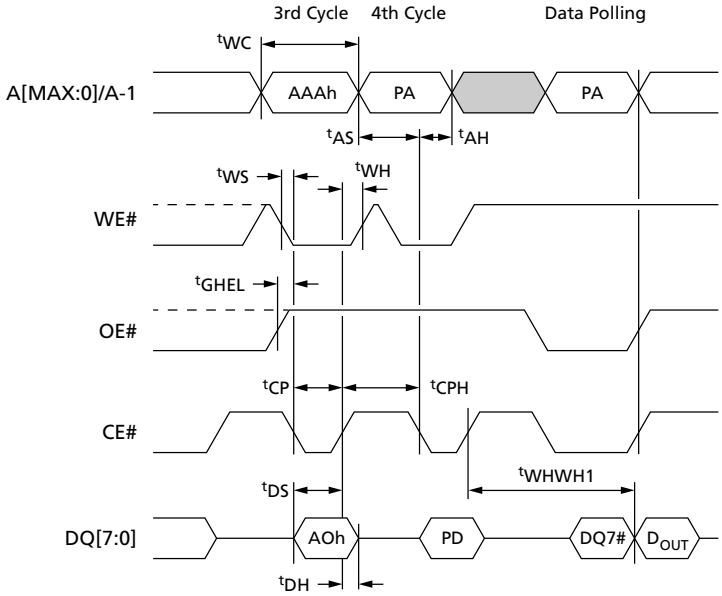
Figure 37: CE#-Controlled Program AC Timing (8-Bit Mode)



Notes:
1. Only the third and fourth cycles of the PROGRAM command are represented. The PROGRAM command is followed by checking of the status register data polling bit.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (See Data Polling Bit [DQ7]).
4. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

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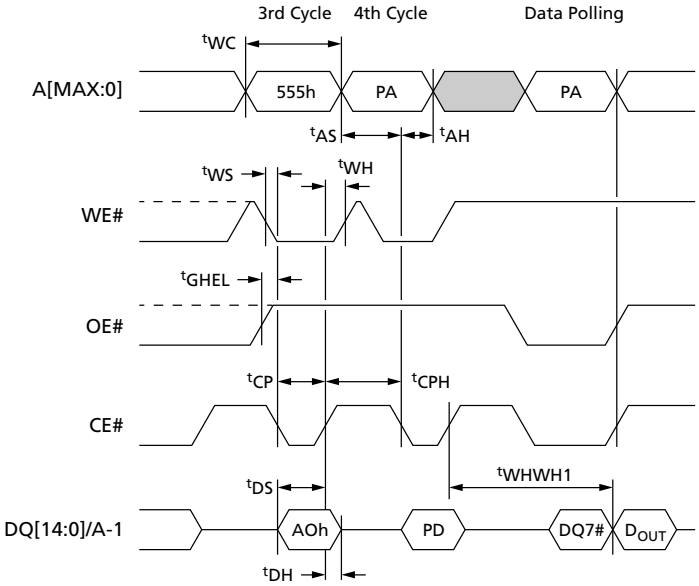
Figure 38: CE#-Controlled Program AC Timing (16-Bit Mode)



Notes:
1. Only the third and fourth cycles of the PROGRAM command are represented. The PROGRAM command is followed by checking of the status register data polling bit.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (See Data Polling Bit [DQ7]).
4. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

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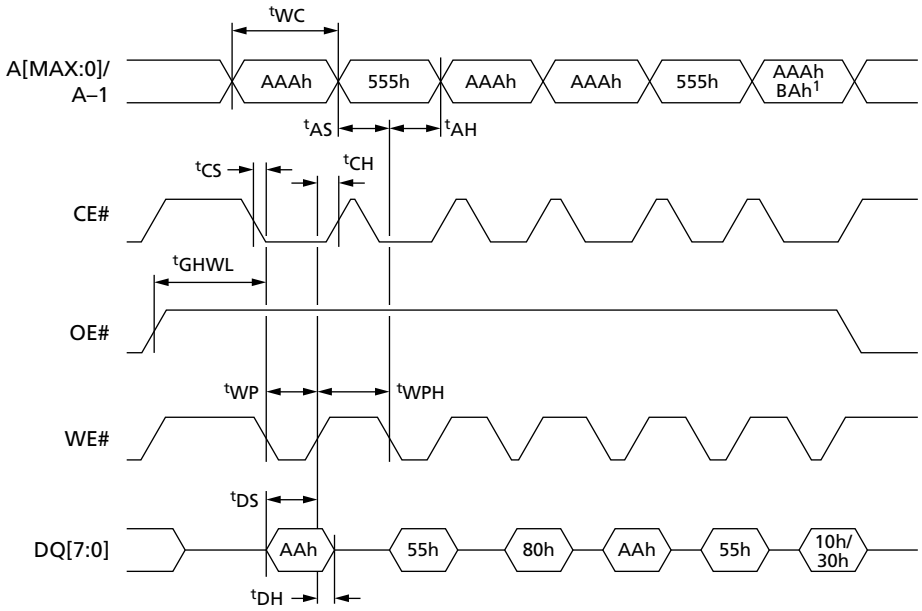
Figure 39: Chip/Block Erase AC Timing (8-Bit Mode)



Notes:
1. For a CHIP ERASE command, the address is AAAh, and the data is 10h; for a BLOCK ERASE command, the address is BAd, and the data is 30h.
2. BAd is the block address.
3. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

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Accelerated Program, Data Polling/Toggle AC Characteristics

Table 31: Accelerated Program and Data Polling/Data Toggle AC Characteristics

Note 1 and 2 apply to the entire table.

Parameter	Symbol		Min	Max	Unit
	Legacy	JEDEC			
V_{PP}/WP# rising or falling time	–	^{t}VHVPP	250	–	ns
Address setup time to OE# LOW during toggle bit polling	^{t}ASO	^{t}AXGL	10	–	ns
Address hold time from OE# during toggle bit polling	^{t}AHT	^{t}GHAX, ^{t}EHAX	10	–	ns
CE# HIGH during toggle bit polling	^{t}EPH	^{t}EHEL2	10	–	ns
Output hold time during data and toggle bit polling	^{t}OEH	^{t}WHGL2, ^{t}GHGL2	20	–	ns
Program/erase valid to RY/BY# LOW	^{t}BUSY	^{t}WHRL	–	30	ns

Notes:
1. Specifications apply to 60, 70, and 80ns devices unless otherwise noted. The 60ns device is available upon customer request.
2. Sampled only; not 100% tested.

Figure 40: Accelerated Program AC Timing

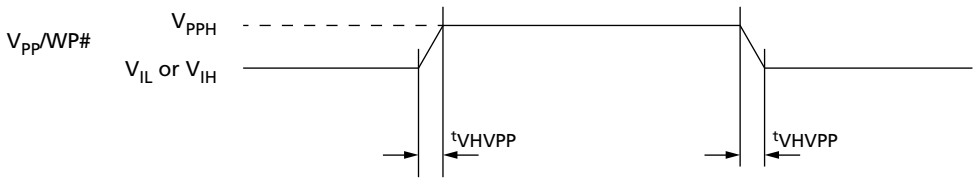

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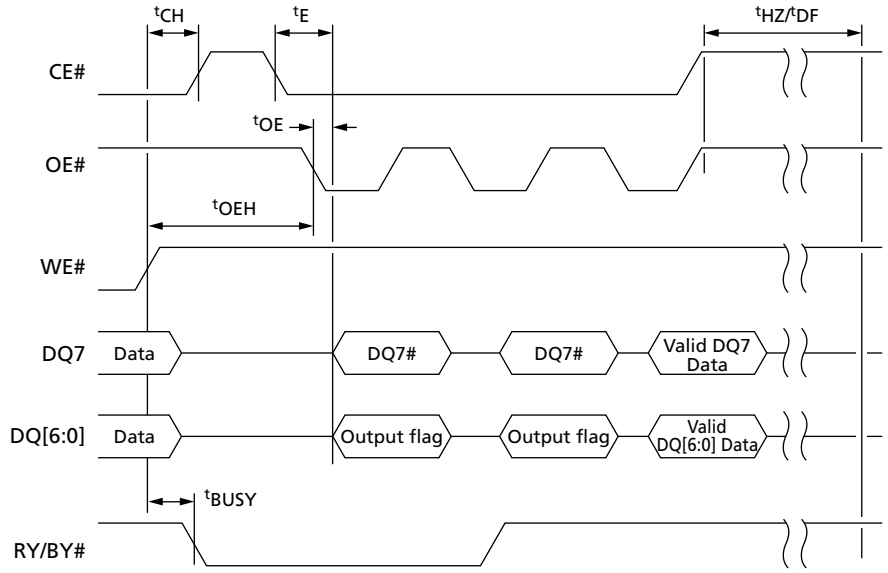
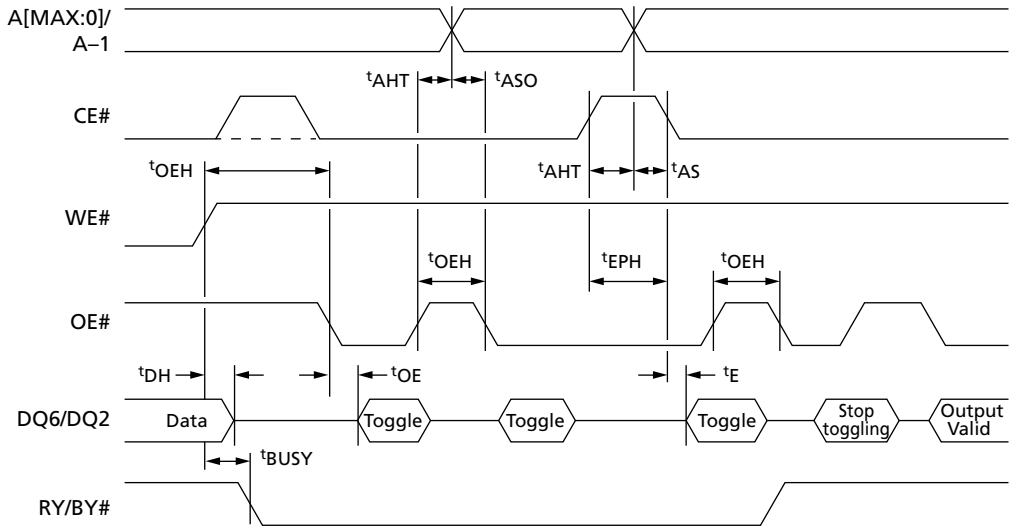
Figure 41: Data Polling AC Timing



Notes:
1. DQ7 returns a valid data bit when the PROGRAM or ERASE command has completed.
2. See the following tables for timing details: Read AC Characteristics, Accelerated Program and Data Polling/Data Toggle AC Characteristics.

Figure 42: Toggle/Alternative Toggle Bit Polling AC Timing (8-Bit Mode)



Notes:
1. DQ6 stops toggling when the PROGRAM or ERASE command has completed. DQ2 stops toggling when the CHIP ERASE or BLOCK ERASE command has completed.
2. See the following tables for timing details: Read AC Characteristics, Accelerated Program and Data Polling/Data Toggle AC Characteristics.

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Program/Erase Characteristics

Table 32: Program/Erase Characteristics

Notes 1 and 2 apply to the entire table

Parameter			Min	Typ	Max	Unit	Notes
Chip erase			–	145	400	s	3, 4
Chip erase		V_{PP}/WP# = V_{PPH}	–	125	400	s	4
Block erase (128KB)			–	0.5	2	s	4, 5
Erase suspend latency time			–	25	45	µs	
Block erase timeout			50	–	–	µs	
Byte program	Single-byte program		–	16	200	µs	4
	Write to buffer program (64 bytes at-a-time)	V_{PP}/WP# = V_{PPH}	–	50	200	µs	4
		V_{PP}/WP# = V_{IH}	–	70	200	µs	4
Word program	Single-word program		–	16	200	µs	4
	Write to buffer program (32 bytes at-a-time)	V_{PP}/WP# = V_{PPH}	–	50	200	µs	4
		V_{PP}/WP# = V_{IH}	–	70	200	µs	4
Chip program (byte by byte)			–	540	800	s	4
Chip program (word by word)			–	270	400	s	4
Chip program (write to buffer program)			–	25	200	s	4, 6
Chip program (write to buffer program with V_{PP}/WP# = V_{PPH})			–	13	50	s	4, 6
Chip program (enhanced buffered program)			–	15	60	s	6
Chip program (enhanced buffered program with V_{PP}/WP# = V_{PP})			–	10	40	s	6
Program suspend latency time			–	5	15	µs	
PROGRAM/ERASE cycles (per block)			100,000	–	–	cycles	
Data retention			20	–	–	years	

Notes:
1. Typical values measured at room temperature and nominal voltages and for not cycled devices.
2. Typical and maximum values are sampled, but not 100% tested.
3. Time needed to program the whole array at 0 is included.
4. Maximum value measured at worst case conditions for both temperature and V_{CC} after 100,000 PROGRAM/ERASE cycles.
5. Block erase polling cycle time (see Data polling AC waveforms figure).
6. Intrinsic program timing, that means without the time required to execute the bus cycles to load the PROGRAM commands.

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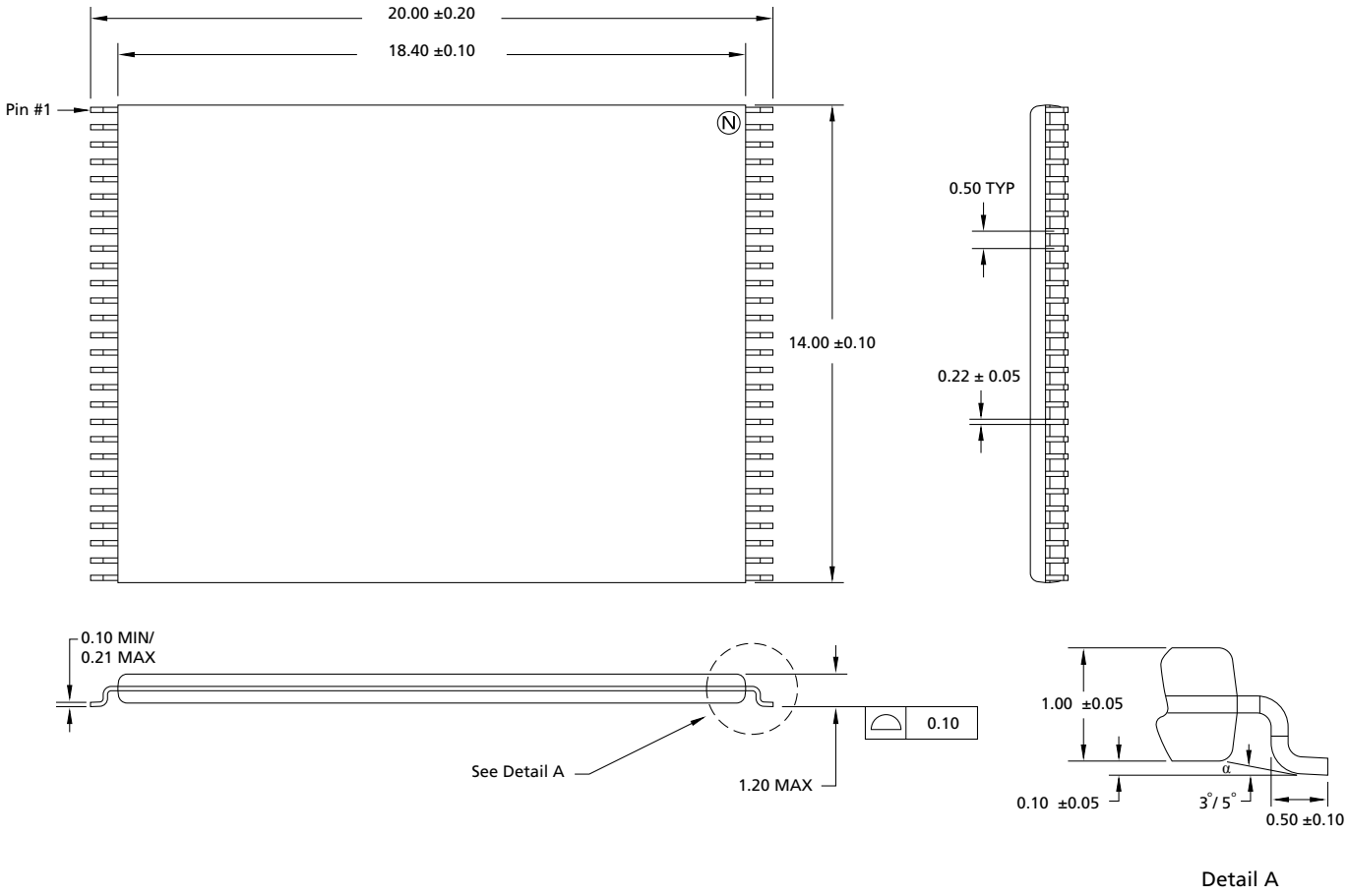
Package Dimensions

Figure 43: 56-Pin TSOP – 14mm x 20mm



Notes:
1. All dimensions are in millimeters.
2. For the lead width value of 0.22 ±0.05, there is also a legacy value of 0.15 ±0.05.

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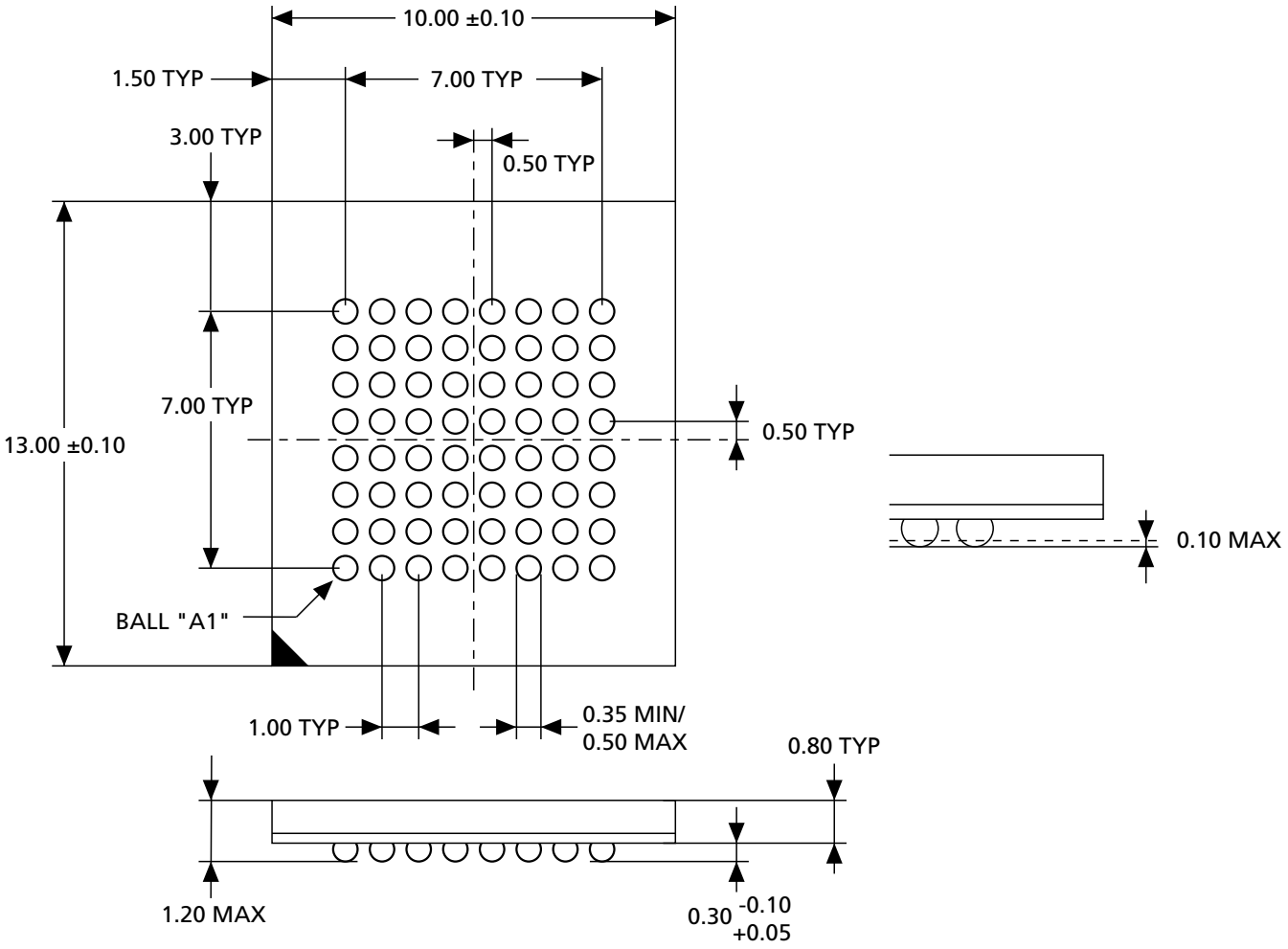
Figure 44: 64-Pin TBGA – 10mm x 13mm



Note: 1. All dimensions are in millimeters.

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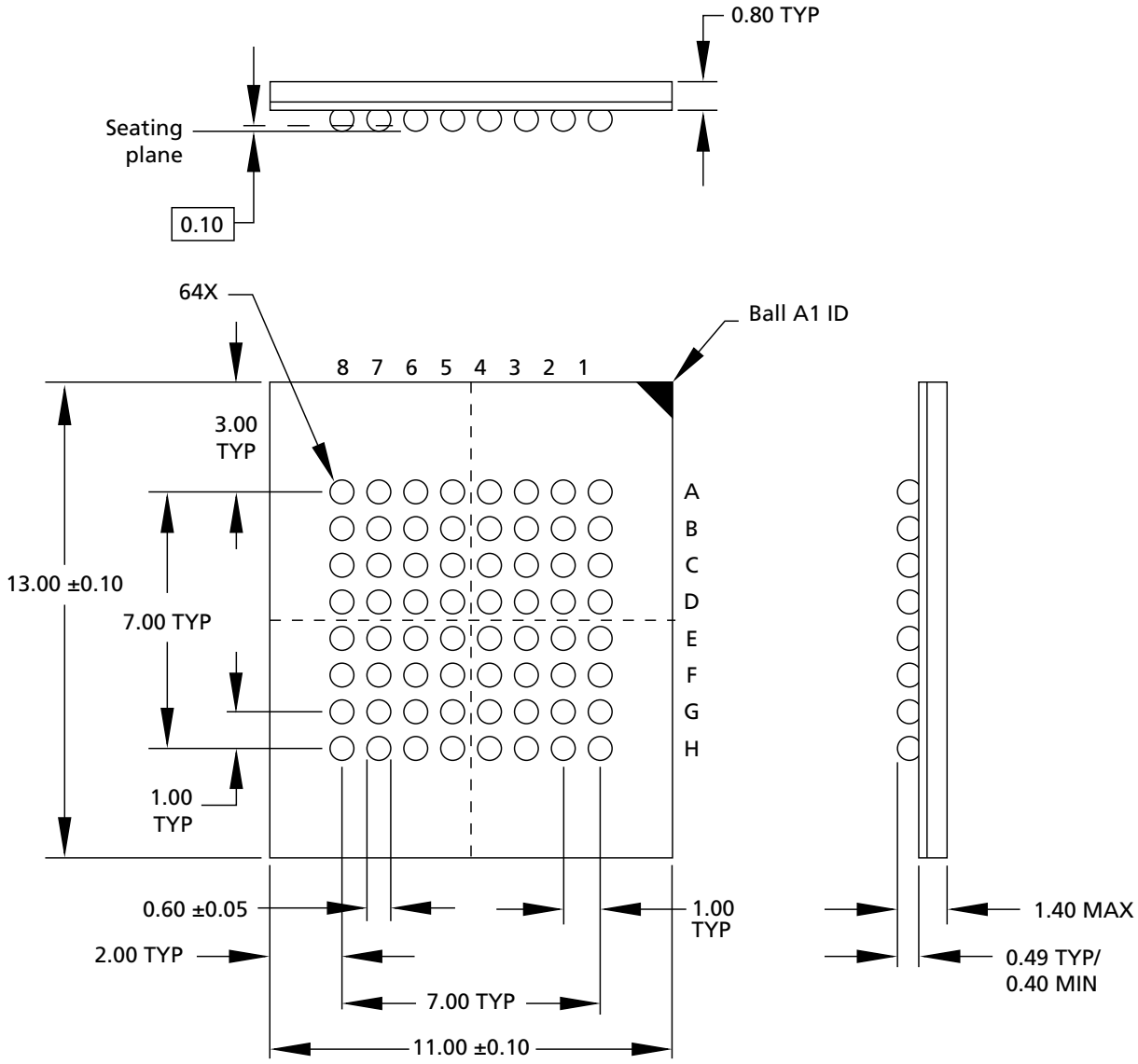
Figure 45: 64-Ball Fortified BGA – 11mm x 13mm



Note: 1. All dimensions are in millimeters.

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Revision History

Rev. B – 05/13

- Synchronized TBGA (ZA) package dimensions in the order information table with dimensions in the package diagram

Rev. A – 05/12

- Initial Micron brand release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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