GENERAL DESCRIPTION

The M1040 is a VCSO (Voltage Controlled SAW Oscillator) based clock generator PLL designed for clock protection, frequency translation and jitter attenuation in OC-12/48 class optical networking systems. It features dual differential inputs with two modes of input selection: manual and automatic upon clock failure. The clock multiplication ratios and output divider ratio are pin selectable. This device provides two outputs. External loop components allow the tailoring of PLL loop response.



FEATURES

- **Integrated SAW (surface acoustic wave) delay line; low phase jitter of < 0.5ps rms, typical (12kHz to 20MHz)**
- **Output frequencies of 62.5 to 175 MHz *; Two differential LVPECL outputs (CML, LVDS options available)**
- **Loss of Lock (LOL) indicator output**
- **Narrow Bandwidth control input (NBW pin); Initialization (INIT) input overrides NBW at power-up**
- **Dual reference clock inputs support LVDS, LVPECL, LVCMOS, LVTTL**
- **AutoSwitch (AUTO pin) - automatic (non-revertive) reference clock reselection upon clock failure; Hitless Switching (HS), Phase Build-out (PBO) options enable SONET (GR-253)/SDH (G.813) MTIE/TDEV compliance**
- **Acknowledge pin (REF_ACK pin) indicates the actively selected reference input**
- **Industrial temperature available**
- **Single 3.3V power supply**
- **Small 9 x 9 mm SMT (surface mount) package**

PIN ASSIGNMENT (9 x 9 mm SMT)

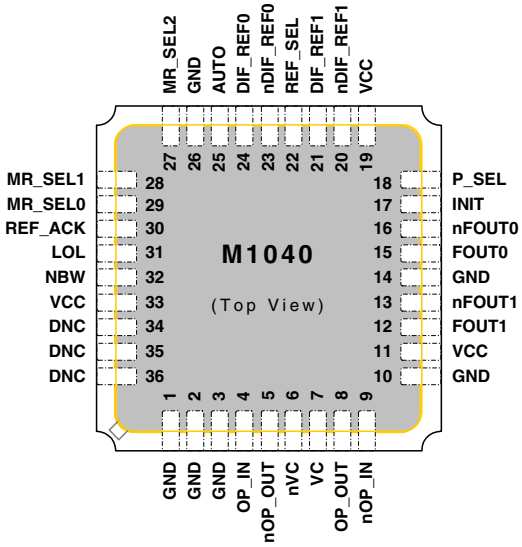


Figure 1: Pin Assignment

Example I/O Clock Frequency Combinations Using M1040-11-155.5200

Input Reference Clock (MHz)	PLL Ratio (Pin Selectable)	Output Clock (MHz) (Pin Selectable)
19.44	8	155.52 or 77.76
77.76	2	
155.52	1	
622.08	0.25	

Table 1: Example I/O Clock Frequency Combinations

* Specify VCSO center frequency at time of order.

SIMPLIFIED BLOCK DIAGRAM

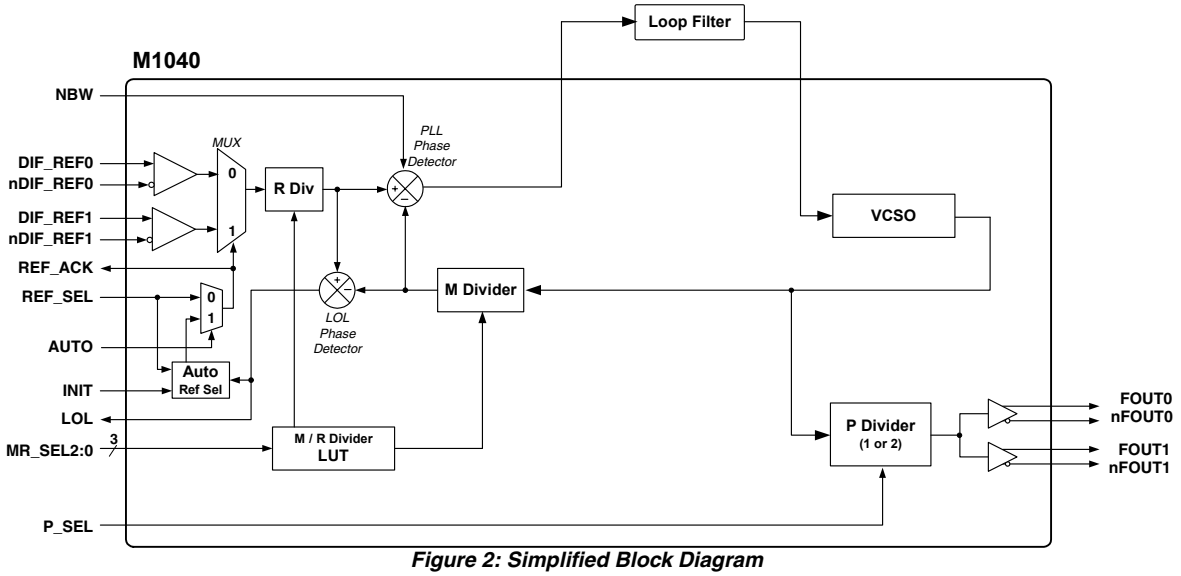


Figure 2: Simplified Block Diagram

PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4 9	OP_IN nOP_IN	Input		External loop filter connections. See Figure 5, External Loop Filter, on pg. 8.
5 8	nOP_OUT OP_OUT	Output		
6 7	nVC VC	Input		
11, 19, 33	VCC	Power		Power supply connection, connect to +3.3V.
12 13	FOUT1 nFOUT1	Output	No internal terminator	Clock output pair 1. Differential LVPECL.
15 16	FOUT0 nFOUT0	Output	No internal terminator	Clock output pair 0. Differential LVPECL.
17	INIT	Input	Internal pull-UP resistor[1]	Power-on Initialization; LVCMOS/LVTTL: Logic 1 allows device to enter narrow mode if selected (in addition must have 8 LOL=0 counts) Logic 0 forced device into wide bandwidth mode.
18	P_SEL		Internal pull-down[1]	Post-PLL , P divider selection. LVCMOS/LVTTL. See Table 4, P Divider Selector Values and Frequencies, on pg. 3.
20	nDIF_REF1	Input	Biased to Vcc/2 [2]	Reference clock input pair 1. Differential LVPECL/ LVDS
21	DIF_REF1		Internal pull-down resistor[1]	Reference clock input pair 1. Differential LVPECL/ LVDS, or single ended LVCMOS/ LVTTL
22	REF_SEL	Input	Internal pull-down resistor[1]	Reference clock input selection. LVCMOS/LVTTL. Logic 1 selects DIF_REF1/nDIF_REF1 inputs Logic 0 selects DIF_REF0/nDIF_REF0 inputs
23	nDIF_REF0	Input	Biased to Vcc/2 [3]	Reference clock input pair 0. Differential LVPECL/ LVDS
24	DIF_REF0		Internal pull-down resistor[1]	Reference clock input pair 0. Differential LVPECL/ LVDS, or single ended LVCMOS/ LVTTL
25	AUTO	Input	Internal pull-down resistor[1]	Automatic/manual reselection mode for clock input: Logic 1 automatic reselection upon clock failure (non-revertive) Logic 0 manual selection only (using REF_SEL)
27 28 29	MR_SEL2 MR_SEL1 MR_SEL0	Input	Internal pull-UP resistor[1]	M and R divider value selection. LVCMOS/ LVTTL. See Table 3, M and R Divider Look-Up Tables (LUT) on pg. 3.
30	REF_ACK	Output		Reference Acknowledgement pin for input mux state; outputs the currently selected reference input pair: Logic 1 indicates nDIF_REF1, DIF_REF1 Logic 0 indicates nDIF_REF0, DIF_REF0
31	LOL	Output		Loss of Lock indicator output. [4] Logic 1 indicates loss of lock. Logic 0 indicates locked condition.
32	NBW	Input	Internal pull-UP resistor[1]	Narrow Bandwidth enable. LVCMOS/LVTTL: Logic 1 - Narrow loop bandwidth, R_{IN} = 2100kΩ Logic 0 - Wide bandwidth, R_{IN} = 100kΩ
34, 35, 36	DNC			Do Not Connect.

Table 2: Pin Descriptions

Note 1: For typical values of internal pull-down and pull-up resistors, see **DC Characteristics** on pg. 10.
Note 2: Biased to Vcc/2, with 50kΩ to Vcc and 50kΩ to ground. Float if using DIF_REF1 as LVCMOS input. See **DC Characteristics** on pg. 10.
Note 3: Biased to Vcc/2, with 50kΩ to Vcc and 50kΩ to ground. Float if using DIF_REF0 as LVCMOS input. See **DC Characteristics** on pg. 10.
Note 4: See LVCMOS Outputs in DC Characteristics on pg. 10.

DETAILED BLOCK DIAGRAM

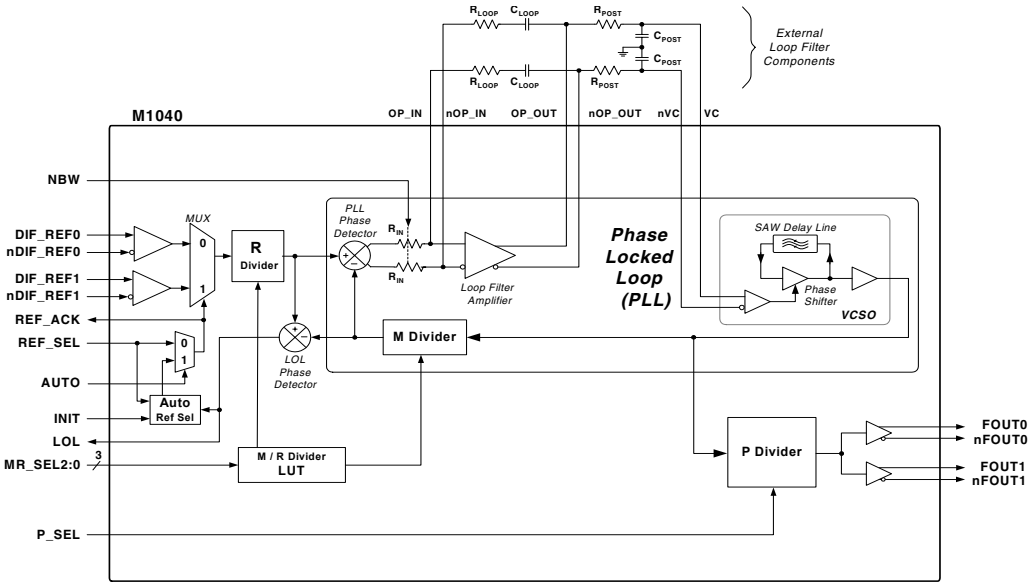


Figure 3: Detailed Block Diagram

PLL DIVIDER SELECTION TABLES

M and R Divider Look-Up Tables (LUT)

The MR_SEL2:0 pins select the feedback and reference divider values M and R to enable adjustment of loop bandwidth and jitter tolerance. The look-up is defined in Table 3.

M1040 M/R Divider LUT

MR_SEL3:0	M Div	R Div	Total PLL Ratio	Fin for 155.52MHz VCSO (MHz)	Phase Det. Freq. for 155.52MHz VCSO (MHz)
0 0 0	8	1	8	19.44	19.44
0 0 1	64	8	8	19.44	2.43
0 1 0	2	1	2	77.76	77.76
0 1 1	16	8	2	77.76	9.72
1 0 0	1	1	1	155.52	155.52
1 0 1	8	8	1	155.52	19.44
1 1 0	Test Mode[1]		N/A	N/A	N/A
1 1 1	2	8	0.25	622.08	77.76

Table 3: M1040 M/R Divider LUT

Note 1: Factory test mode; do not use.

Table 3 provides example Fin and phase detector frequencies with 155.52MHz *VCSO devices (e.g.,* **M1040-11-155.5200***). See "Ordering Information" on pg. 12.*

General Guidelines for M and R Divider Selection

General guidelines for M/R divider selection (see following pages for more detail):

- A lower phase detector frequency should be used for loop timing applications to assure PLL tracking, especially during GR-253 jitter tolerance testing. The recommended maximum phase detector frequency for loop timing mode is 19.44MHz. The LOL pin should not be used during loop timing mode.
- When LOL is to be used for system health monitoring, the phase detector frequency should be 5MHz or greater. Low phase detector frequencies make LOL overly sensitive, and higher phase detector frequencies make LOL less sensitive.
- The preceding guideline also applies when using the AutoSwitch Mode, since AutoSwitch uses the LOL output for clock fault detection.

Post-PLL Divider

The M1040 also features a post-PLL (P) divider for the output clocks. It divides the VCSO frequency to produce one of two selectable output frequencies (1/2 or 1/1 of the VCSO frequency). That selected frequency appears on both clock output pairs. The P_SEL pin selects the value for the P divider.

P_SEL	P Value	M1040-11-155.52 Output Frequency (MHz)
1	2	77.76
0	1	155.52

Table 4: P Divider Selector Values and Frequencies

FUNCTIONAL DESCRIPTION

The M1040 is a PLL (Phase Locked Loop) based clock generator that generates two output clocks synchronized to one of two selectable input reference clocks. An internal high “Q” SAW delay line provides a low jitter clock output.

A pin-selected look-up table is used to select the PLL feedback divider (M Div) and reference divider (R Div) as shown in Table 3 on pg. 3. The look-up table provides flexibility in both the overall frequency multiplication ratio (total PLL ratio) and phase detector frequency.

External loop filter component values influence the PLL bandwidth, which is used to optimize jitter attenuation characteristics.

The device features dual differential inputs with two input selection modes: manual and automatic upon clock failure. (The differential inputs are internally configured for easy single-ended operation.)

The M1040 also includes: a Loss of Lock (LOL) indicator, a reference mux state acknowledge pin (REF_ACK), a Narrow Bandwidth control input pin (NBW pin), and a Power-on Initialization (INIT) input (which overrides NBW=0 to facilitate acquisition of phase lock).

An automatic input reselection feature, or “AutoSwitch” is also included in the M1040. When the AutoSwitch mode is enabled, the device will automatically switch to the other reference clock input when the currently selected reference clock fails. Reference selection is non-revertive, meaning that only one reference reselection will be made each time that AutoSwitch is re-enabled.

In addition to the AutoSwitch feature, Hitless Switching and Phase Build-out options can be ordered with the device. The Hitless Switching and Phase Build-out options help assure SONET/SDH MTIE and TDEV compliance during either a manual or automatic input reference reselection.

Hitless Switching (HS) provides a controlled output clock phase change during a reference clock reselection. HS is triggered by a Loss of Lock detection by the PLL.

Input Reference Clocks

Two clock reference inputs and a selection mux are provided. Either reference clock input can accept a differential clock signal (such as LVPECL or LVDS) or a single-ended clock input (LVCMOS or LVTTL on the non-inverting input).

A single-ended reference clock on the unselected reference input can cause an increase in output clock jitter. For this reason, differential reference inputs are preferred; interference from a differential input on the non-selected input is minimal.

Implementation of single-ended input has been facilitated by biasing nDIF_REF0 and nDEF_REF1 to Vcc/2, with 50kΩ to Vcc and 50kΩ to ground. Figure 4 shows the input clock structure and how it is used with either LVCMOS / LVTTL inputs or a DC- coupled LVPECL clock.

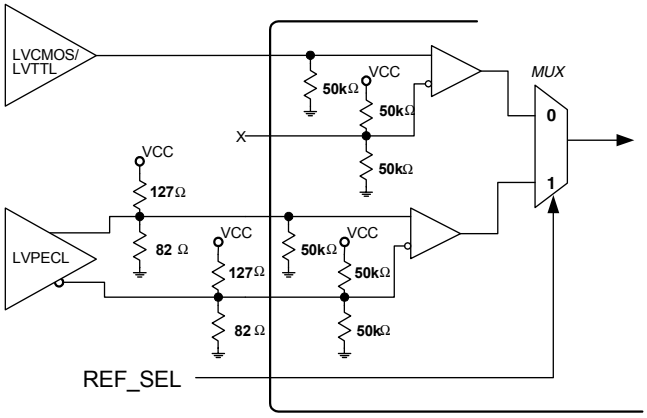


Figure 4: Input Reference Clocks

Differential Inputs

Differential LVPECL inputs are connected to both reference input pins in the usual manner. The external load termination resistors shown in Figure 4 (the 127Ω and 82Ω resistors) will work for both AC and DC coupled LVPECL reference clock lines. These provide the 50Ω load termination and the V_{TT} bias voltage.

Single-ended Inputs

Single-ended inputs (LVCMOS or LVTTL) are connected to the non-inverting reference input pin (DIF_REF0 or DIF_REF1). The inverting reference input pin (nDIF_REF0 or nDIF_REF1) must be left unconnected.

*In single-ended operation, when the unused inverting input pin (*nDIF_REF0 *or* nDEF_REF1*) is left floating (not connected), the input will self-bias at VCC/2.*

PLL Operation

The M1040 is a complete clock PLL. It uses a phase detector and configurable dividers to synchronize the output of the VCSO with the selected reference clock.

The "M" divider divides the VCSO output frequency, feeding the result into the plus input of the phase detector. The output of the "R" divider is fed into the minus input of the phase detector. The phase detector compares its two inputs. The phase detector output, filtered externally, causes the VCSO to increase or decrease in speed as needed to phase- and frequency-lock the VCSO to the reference input.

The value of the M divider directly affects closed loop bandwidth.

The relationship between the nominal VCSO center frequency (Fvcso), the M divider, the R divider, and the input reference frequency (Fin) is:

$$Fvcso = Fin \times \frac{M}{R}$$

For the available M divider and R divider look-up table combinations, Tables 3 and 4 on pg. 3 list the Total PLL Ratio as well as Fin when using the **M1040-11-155.5200**. (See "Ordering Information", pg. 12.)

Due to the narrow tuning range of the VCSO (±200ppm), appropriate selection of all of the following are required for the PLL be able to lock: VCSO center frequency, input frequency, and divider selections.

Post-PLL Divider

The M1040 features a post-PLL (P) divider. By using the P Divider, the device's output frequency (Fout) can be the VCSO center frequency (Fvcso) or 1/2 Fvcso.

The P_SEL pin selects the value for the P divider: logic 1 sets P to 2, logic 0 sets P to 1. (See Table 5 on pg. 6.)

When the P divider is included, the complete relationship for the output frequency (Fout) is defined as:

$$Fout = \frac{Fvcso}{P} = Fin \times \frac{M}{R \times P}$$

Loss of Lock Indicator Output Pin

Under normal device operation, when the PLL is locked, the LOL Phase Detector drives LOL to logic 0. Under circumstances when the VCSO cannot lock to the input (as measured by a greater than 4 ns discrepancy between the feedback and reference clock rising edges at the LOL Phase Detector) the LOL output goes to logic 1. The LOL pin will return back to logic 0 when the phase detector error is less than 2 ns. The loss of lock indicator is a low current LVCMOS output.

Guidelines Using LOL

As described, the LOL pin indicates when the PLL is out-of-lock with the input reference. The LOL condition is also used by the AutoSwitch circuit to detect a lost reference, as described in following sections. LOL is also used by the Hitless Switching and Phase Build-out functions (optional device features). To ensure reliable operation of LOL and guard against false out-of-lock indications, the following conditions should be met:

- The phase detector frequency should be no less than 5MHz, and preferably it should be 10MHz or greater. Phase detector frequency is defined by Fin / R. A higher phase detector frequency will result in lower phase error and less chance of false triggering the LOL phase detector. Refer to Tables 3 and 4 on pg. 3 for phase detector frequency when using the **M1040-11-155.5200**.
- The input reference should have an intrinsic jitter of less than 1 ns pk-pk. If reference jitter is greater than 1 ns pk-pk, the LOL circuit might falsely trigger. Due to this limitation, the LOL circuit should not be used in loop timing mode, nor should it be used with a noisy reference clock. Likewise, the AutoSwitch, Hitless Switching, or Phase Build-out features should not be used in loop timing mode or with a noisy reference clock, since these features depend on LOL.

Reference Acknowledgement (REF_ACK) Output

The REF_ACK (reference acknowledgement) pin outputs the value of the reference clock input that is routed to the phase detector. Logic 1 indicates input pair 1 (nDIF_REF1, DIF_REF1); logic 0 indicates input pair 0 (nDIF_REF0, DIF_REF0). The REF_ACK indicator is an LVCMOS output.

AutoSwitch (AUTO) Reference Clock Reselection

This device offers an automatic reference clock reselection feature for switching input reference clocks upon a reference clock failure. With the AUTO input pin set to high and the LOL output low, the device is placed into automatic reselection (AutoSwitch) mode. Once in AutoSwitch mode, when LOL then goes high (due to a reference clock fault), the input clock reference is automatically reselected internally, as indicated by the state change of the REF_ACK output. Automatic clock reselection is made only once (it is non-revertive). Re-arming of automatic mode requires placing the device into manual selection (Manual Select) mode (AUTO pin low) before returning to AutoSwitch mode (AUTO pin high).

Using the AutoSwitch Feature

See alsoTable 5, Example AutoSwitch Sequence.

In application, the system is powered up with the device in Manual Select mode (AUTO pin is set low), allowing sufficient time for the reference clock and device PLL to settle. The REF_SEL input selects the reference clock to be used in Manual Select mode and the initial reference clock used in AutoSwitch mode. The REF_SEL input state must be maintained when switching to AutoSwitch mode (AUTO pin high) and must still be maintained until a reference fault occurs.

Once a reference fault occurs, the LOL output goes high and the input reference is automatically reselected. The REF_ACK output always indicates the reference selection status and the LOL output always indicates the PLL lock status.

A successful automatic reselection is indicated by a change of state of the REF_ACK output and a momentary level high of the LOL output (minimum high time is 10 ns).

If an automatic reselection is made to a non-valid reference clock (one to which the PLL cannot lock), the REF_ACK *output will change state but the* LOL *output will remain high.*

No further automatic reselection is made; only one reselection is made each time the AutoSwitch mode is armed. AutoSwitch mode is re-armed by placing the device into Manual Select mode (AUTO pin low) and then into AutoSwitch mode again (AUTO pin high).

Following an automatic reselection and prior to selecting Manual Select mode (AUTO pin low), the REF_SEL pin has no control of reference selection. To prevent an unintential reference reselection, AutoSwitch mode must not be re-enabled until the desired state of the REF_SEL pin is set and the LOL output is low. It is recommended to delay the re-arming of AutoSwitch mode, following an automatic reselection, to ensure the PLL is fully locked on the new reference. In most system configurations, where loop bandwidth is in the range of 100-1000 Hz and damping factor below 10, a delay of 500 ms should be sufficient. Until the PLL is fully locked intermittent LOL pulses may occur.

Example AutoSwitch Sequence

0 = Low; 1 = High. Example with REF_SEL initially set to 0 (*i.e.,* DIF_REF0 selected)

REF_SEL Input	Selected Clock Input	REF_ACK Output	AUTO Input	LOL Output	Conditions
					Initialization
0	DIF_REF0	0	0	1	Device power-up. Manual Select mode. DIF_REF0 input selected reference, not yet locked to.
0	DIF_REF0	0	0	**-0-**	LOL to 0: Device locked to reference (may get intermittent LOL pulses until fully locked).
0	DIF_REF0	0	**-1-**	0	AUTO set to 1: Device placed in AutoSwitch mode (with DIF_REF0 as initial reference clock).
					Operation & Activation
0	DIF_REF0	0	1	0	Normal operation with AutoSwitch mode armed, with DIF_REF0 as initial reference clock.
0	DIF_REF0	0	1	**-1-**	LOL to 1: Clock fault on DIF_REF0, loss of lock indicated by LOL pin, ...
0	**-DIF_REF1-**	**-1-**	1	1	... and immediate automatic reselection to DIF_REF1 (indicated by REF_ACK pin).
0	DIF_REF1	1	1	**-0-**	LOL to 0: Device locks to DIF_REF1 (assuming valid clock on DIF_REF1).
					Re-initialization
-1-	DIF_REF1	1	1	0	REF_SEL set to 1: Prepares for Manual Selection of DIF_REF1 before then re-arming AutoSwitch.
1	DIF_REF1	1	**-0-**	0	AUTO set to 0: Manual Select mode entered briefly, manually selecting DIF_REF1 as reference.
1	DIF_REF1	1	**-1-**	0	AUTO set to 1: Device is placed in AutoSwitch mode (delay recommended to ensure device fully locked), re-initializing AutoSwitch with DIF_REF1 now specified as the initial reference clock.

Table 5: Example AutoSwitch Sequence

Optional Hitless Switching and Phase Build-out

The M1040 is available with a Hitless Switching feature that is enabled during device manufacturing.
In addition, a Phase Build-out feature is also offered. These features are offered as device options and are specified by device order code. Refer to Section , "Ordering Information" on pg. 12.

The Hitless Switching feature (with or without Phase Build-out) is designed for applications where switching occurs between two stable system reference clocks. It should not be used in loop timing applications, or when reference clock jitter is greater than 1 ns pk-pk. Hitless Switching is triggered by the LOL circuit, which is activated by a 4 ns phase transient. This magnitude of phase transient can generated by the CDR (Clock & Data Recovery unit) in loop timing mode, especially during a system jitter tolerance test. It can also be generated by some types of Stratum clock DPLLs (digital PLL), especially those that do not include a post de-jitter APLL (analog PLL).

When the Hitless Switching feature is enabled, it is always triggered by LOL, whether in AutoSwitch mode (AUTO pin high) or Select mode (AUTO pin low). For example, in Manual mode, the Hitless Switching feature operates when LOL goes high even if there is no reselection of the input mux. This enables the use of an upstream clock mux (such as on the host card), while still providing MTIE compliance when readjusting to the resultant phase change.

When the M1040 is operating in wide bandwidth mode (NBW=0), the optional Hitless Switching function puts the device into narrow bandwidth mode when activated. This allows the PLL to lock the new input clock phase gradually. With proper configuration of the external loop filter, the output clock complies with MTIE and TDEV specifications for GR-253 (SONET) and ITU G.813 (SDH) during input reference clock changes.

The optional proprietary Phase Build-out (PBO) function enables the PLL to absorb most of the phase change of the input clock. The PBO function selects a new VCSO clock edge for the PLL Phase Detector feedback clock, selecting the edge closest in phase to the new input clock phase. This reduces re-lock time, the generation of wander, and extra output clock cycles.

The Hitless Switching and Phase Build-out functions are triggered by the LOL circuit. For proper operation, a low phase detector frequency must be avoided. See Section , "Guidelines Using LOL" on pg. 5 for information regarding the phase detector frequency.

HS/PBO Triggers

The HS function (or the combined HS/PBO function) is armed after the device locks to the input clock reference. Once armed, HS is triggered by the occurance of a Loss of Lock condition. This would typically occur as a consequence of a clock reference failure, a clock failure upstream to the M1040, or a M1040 clock reference mux reselection.

> *When pin AUTO = 1 (automatic reference reselection mode) HS is used in conjunction with input reselection. When AUTO = 0 (manual mode), HS will still occur upon an input phase transient, however the clock input is not reselected (this enables hitless switching when using an external MUX for clock selection).*

HS/PBO Operation

Once triggered, the following HS/PBO sequence occurs:

1. The HS function disables the PLL Phase Detector and puts the device into NBW (narrow bandwidth) mode. The internal resistor Rin is changed to 2100kΩ. See the Narrow Loop Bandwidth Control Pin (NBW Pin) on pg. 7.
2. If included, the PBO function adds to (builds out) the phase in the clock feedback path (in VCSO clock cycle increments) to align the feedback clock with the (new) reference clock input phase.
3. The PLL Phase Detector is enabled, allowing the PLL to re-lock.
4. Once the PLL Phase Detector feedback and input clocks are locked to within 2 ns for eight consecutive cycles, a timer (WBW timer) for resuming wide bandwidth (in 175 ns) is started.
5. When the WBW timer times out, the device reverts to wide loop bandwidth mode (*i.e.,* Rin is returned to 100kΩ) and the HS/PBO function is re-armed.

Narrow Loop Bandwidth Control Pin (NBW Pin)

A Narrow Loop Bandwidth control pin (NBW pin) is included to adjust the PLL loop bandwidth. In wide bandwidth mode (NBW=0), the internal resistor Rin is 100kΩ. With the NBW pin asserted, the internal resistor Rin is changed to 2100kΩ. This lowers the loop bandwidth by a factor of about 21 (approximately 2100 / 100) and lowers the damping factor by a factor of about 4.6 (the square root of 21), assuming the same loop filter components.

Power-Up Initialization Function (INIT Pin)

The initialization function provides a short-term override of the narrow bandwidth mode when the device is powered up in order to facilitate phase locking.

When INIT is set to logic 1, initialization is enabled. With NBW set to logic 1 (narrow bandwidth mode), the initialization function puts the PLL into wide bandwidth mode until eight consecutive phase detector cycles occur without a single LOL event. Once the eight valid PLL locked states have occurred, the PLL bandwidth is automatically reduced to narrow bandwidth mode.

When INIT is logic 0, the device is forced into wide bandwidth mode unconditionally.

External Loop Filter

The M1040 requires the use of an external loop filter components. These are connected to the provided filter pins (see Figure 5).

Because of the differential signal path design, the implementation consists of two identical complementary RC filters as shown in Figure 5.

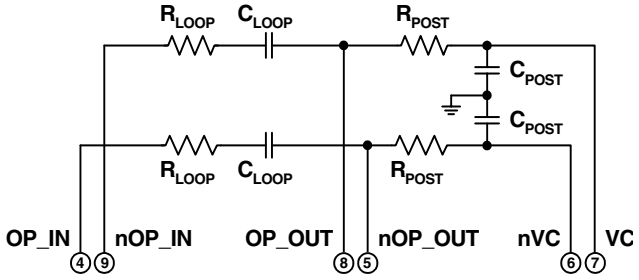


Figure 5: External Loop Filter

PLL bandwidth is affected by the total "M" (feedback divider) value, loop filter component values, and other device parameters. See Table 6, Example External Loop Filter Component Values, below.

PLL Simulator Tool Available

A free PC software utility is available on the ICS website (www.icst.com). The M2000 Timing Modules PLL Simulator is a downloadable application that simulates PLL jitter and wander transfer characteristics. This enables the user to set appropriate external loop component values in a given application.

For guidance on device or loop filter implementation, contact CMBU (Commercial Business Unit) Product Applications at (508) 852-5400.

Example External Loop Filter Component Values[1] for M1040-yz-155.5200

VCSO Parameters: K_{VCO} = 200kHz/V, R_{IN} = 100kΩ (pin NBW = 0), VCSO Bandwidth = 700kHz.

Device Configuration					Example External Loop Filter Comp. Values				Nominal Performance Using These Values		
F_{REF} (MHz)	F_{VCSO} (MHz)	MR_SEL2:0	MDiv	NBW	R_{LOOP}	C_{LOOP}	R_{POST}	C_{POST}	PLL Loop Bandwidth	Damping Factor	Passband Peaking (dB)
19.44 [2]	155.52	0 0 0	8	0	6.8kΩ	10µF	82kΩ	1000pF	315Hz	5.4	0.07
77.76 [3]	155.52	0 1 0	2	0	3.9kΩ	10µF	33kΩ	1000pF	715Hz	6.2	0.05
77.76 [2]	155.52	0 1 1	16	0	12kΩ	2.2µF	82kΩ	1000pF	275Hz	3.1	0.20
155.52 [3]	155.52	1 0 0	1	0	2.7kΩ	10µF	47kΩ	470pF	980Hz	6.0	0.05
155.52 [2]	155.52	1 0 1	8	0	5.6kΩ	4.7µF	82kΩ	1000pF	260Hz	3.0	0.20

Table 6: Example External Loop Filter Component Values

Note 1: K_{VCO} , VCSO Bandwidth, M Divider Value, and External Loop Filter Component Values determine Loop Bandwidth, Damping Factor, and Passband Peaking. For PLL Simulator software, go to www.icst.com.

Note 2: Optimal for system clock filtering.

Note 3: Optimal for loop timing mode (LOL or Hitless Switching should not be used).

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_I	Inputs	-0.5 to V_{CC} +0.5	V
V_O	Outputs	-0.5 to V_{CC} +0.5	V
V_{CC}	Power Supply Voltage	4.6	V
T_S	Storage Temperature	-45 to +100	°C

Table 7: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
T_A	Ambient Operating Temperature	Commercial	0		+70	°C
		Industrial	-40		+85	°C

Table 8: Recommended Conditions of Operation

ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), T_A = -40 °C to +85 °C (industrial), F_{VCSO} = F_{OUT} = 150-175MHz, LVPECL outputs terminated with 50Ω to V_{CC} - 2V

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
Power Supply	V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V	
	I_{CC}	Power Supply Current			175	225	mA	
All Differential Inputs	V_{P-P}	Peak to Peak Input Voltage	DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1	0.15			V	
	V_{CMR}	Common Mode Input		0.5		V_{cc} - .85	V	
	C_{IN}	Input Capacitance				4	pF	
Differential Inputs with Pull-down	I_{IH}	Input High Current (Pull-down)	DIF_REF0, DIF_REF1			150	µA	V_{CC} = V_{IN} = 3.456V
	I_{IL}	Input Low Current (Pull-down)		-5			µA	
	$R_{pulldown}$	Internal Pull-down Resistance			50		kΩ	
Differential Inputs Biased to VCC/2	I_{IH}	Input High Current (Biased)	nDIF_REF0, nDIF_REF1			150	µA	V_{IN} = 0 to 3.456V
	I_{IL}	Input Low Current (Biased)		-150			µA	
	R_{bias}	Biased to Vcc/2		See Figure 4				
All LVCMOS / LVTTL Inputs	V_{IH}	Input High Voltage	AUTO, REF_SEL,, P_SEL, MR_SEL2, MR_SEL1, MR_SEL0, INIT, NBW	2		V_{cc} + 0.3	V	
	V_{IL}	Input Low Voltage		-0.3		0.8	V	
	C_{IN}	Input Capacitance				4	pF	
LVCMOS / LVTTL Inputs with Pull-down	I_{IH}	Input High Current (Pull-down)	AUTO, REF_SEL, P_SEL			150	µA	V_{CC} = V_{IN} = 3.456V
	I_{IL}	Input Low Current (Pull-down)		-5			µA	
	$R_{pulldown}$	Internal Pull-down Resistance			50		kΩ	
LVCMOS / LVTTL Inputs with Pull-UP	I_{IH}	Input High Current (Pull-UP)	MR_SEL2, MR_SEL1, MR_SEL0, INIT, NBW			5	µA	V_{CC} = 3.456V V_{IN} = 0 V
	I_{IL}	Input Low Current (Pull-UP)		-150			µA	
	R_{pullup}	Internal Pull-UP Resistance			50		kΩ	
Differential Outputs	V_{OH}	Output High Voltage	FOUT1, nFOUT1 FOUT0. nFOUT0	V_{cc} - 1.4		V_{cc} - 1.0	V	
	V_{OL}	Output Low Voltage		V_{cc} - 2.0		V_{cc} - 1.7	V	
	V_{P-P}	Peak to Peak Output Voltage [1]		0.4		0.85	V	
LVCMOS Outputs	V_{OH}	Output High Voltage	LOL, REF_ACK	2.4		V_{CC}	V	I_{OH}= 1mA
	V_{OL}	Output Low Voltage		GND		0.4	V	I_{OL}= 1mA

Note 1: Single-ended measurement. See Figure 6, Input and Output Rise and Fall Time, on pg. 11.

Table 9: DC Characteristics

ELECTRICAL SPECIFICATIONS (CONTINUED)

AC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), T_A = -40 °C to +85 °C (industrial), $F_{VCSO} = F_{OUT}$ = 150-175MHz, LVPECL outputs terminated with 50Ω to V_{CC} - 2V

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
	F_{IN}	Input Frequency	DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1	15		700	MHz	
	F_{OUT}	Output Frequency	FOUT0, nFOUT0, FOUT1, nFOUT1	62.5		175	MHz	
	APR	Absolute Pull-Range of VCSO	Commercial	±120	±200		ppm	
			Industrial	±50	±150		ppm	
PLL Loop Constants [1]	K_{VCO}	VCO Gain			200		kHz/V	
	R_{IN}	Internal Loop Resistor	Wide Bandwidth		100		kΩ	
			Narrow Bandwidth		2100		kΩ	
	BW_{VCSO}	VCSO Bandwidth			700		kHz	
Phase Noise and Jitter	Φn	Single Side Band Phase Noise @155.52MHz	1kHz Offset		-72		dBc/Hz	Fin=19.44_MHz Tot. PLL ratio = 8. See pg. 3
			10kHz Offset		-94		dBc/Hz	
			100kHz Offset		-123		dBc/Hz	
	J(t)	Jitter (rms) @155.52MHz	12kHz to 20MHz		0.4	0.6	ps	
	odc	Output Duty Cycle [2]		45	50	55	%	
	t_R	Output Rise Time [2] for FOUT0, nFOUT0, FOUT1, nFOUT1		350	450	550	ps	20% to 80%
	t_F	Output Fall Time [2] for FOUT0, nFOUT0, FOUT1, nFOUT1		350	450	550	ps	20% to 80%

Table 10: AC Characteristics

Note 1: Parameters needed for PLL Simulator software; see Table 6, Example External Loop Filter Component Values, on pg. 8.
Note 2: See Parameter Measurement Information on pg. 11.

PARAMETER MEASUREMENT INFORMATION

Input and Output Rise and Fall Time

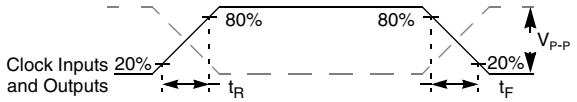


Figure 6: Input and Output Rise and Fall Time

Differential Input Level

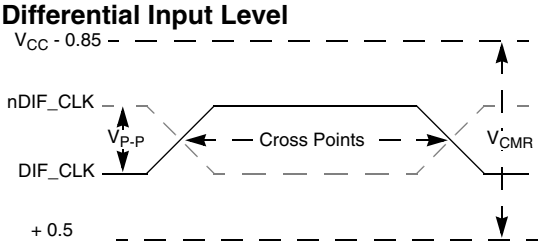


Figure 7: Differential Input Level

Output Duty Cycle

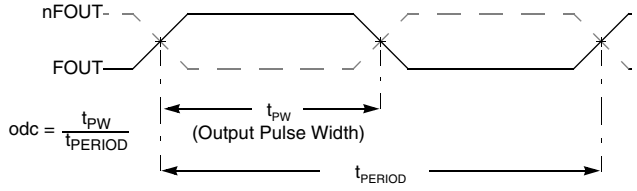


Figure 8: Output Duty Cycle

DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

Mechanical Dimensions:

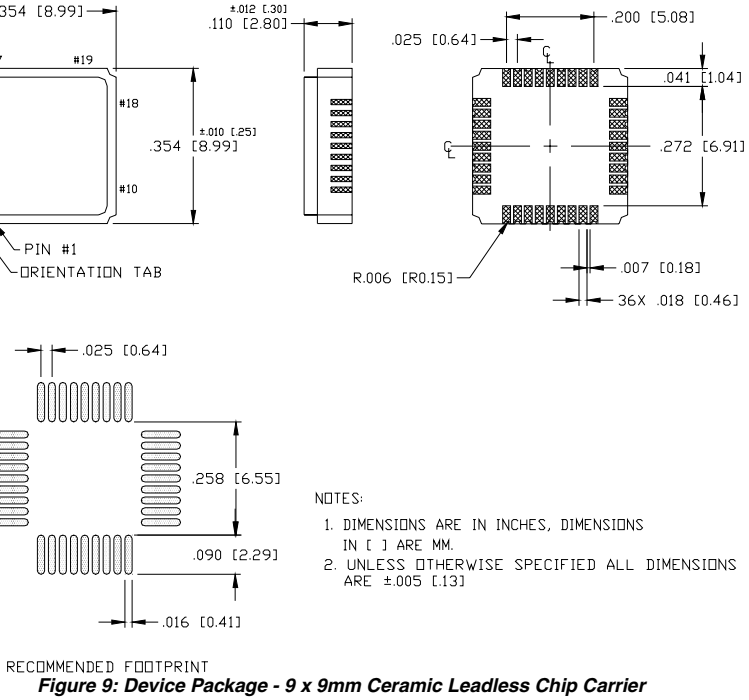


Figure 9: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier

ORDERING INFORMATION

Part Numbering Scheme

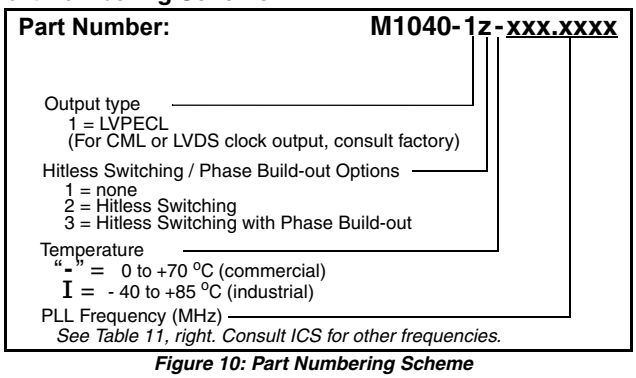


Figure 10: Part Numbering Scheme

Standard VCSO Output Frequencies (MHz)*

155.5200	167.3280
156.2500	167.3316
156.8324	167.7097
161.1328	168.0400
166.6286	172.6423
167.2820	173.3708

Table 11: Standard VCSO Output Frequencies

* Fout can equal Fvcso divided by: 1 or 2

Consult ICS for the availability of other VCSO frequencies.

Example Part Numbers

VCSO Frequency (MHz)	Temperature	Order Part Number (Examples)
155.52	commercial	**M1040-11-155.5200**
	industrial	**M1040-11I155.5200**
156.25	commercial	**M1040-11-156.2500**
	industrial	**M1040-11I156.2500**

Table 12: Example Part Numbers

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