ARM CORTEX®-M

32-BIT MICROCONTROLLER

NuMicro® Family
M0564 Series
Datasheet

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1 GENERAL DESCRIPTION

The NuMicro® M0564 series microcontroller based on the ARM® Cortex®-M0 core operates at up to 72 MHz. It features adjustable V_{DDIO} pins for specific I/O pins with a wide range of voltage from 1.8V to 5.5V for various operating voltages of external components, a unique high-speed PWM with clock frequency up to 144 MHz for precision control, and an integrated hardware divider to speed up the calculation for the control algorithms. Apart from that, the M0564 also integrates SPROM (Security Protection ROM) which provides a secure code execution area to protect the intelligent property of developers. The M0564 series is ideal for industrial control, motor control and metering applications.

The M0564 series supports the wide voltage range from 2.5V to 5.5V and temperature ranging from -40℃ to 105℃, up to 256 Kbytes of Flash memory, 20 Kbytes of SRAM , 4 Kbytes of ISP (In-System Programming) ROM as well as ICP (In-Circuit Programming) ROM and IAP (In-Application Programming) ROM in 48-, 64- or 100-pin packages. It also supports high immunity of 8KV ESD (HBM)/4KV EFT. It is also equipped with plenty of peripherals such as Timers, Watchdog Timers, RTC, PDMA, EBI, UART, Smart Card Interface, SPI, I²S, I²C, GPIO, up to 12 channels of 16-bit PWM, up to 20 channels of 12-bit ADC, analog comparator, temperature sensor, LVR (Low Voltage Reset), BOD (Brown-out Detector), 96-bit UID (Unique Identification), and 128-bit UCID (Unique Customer Identification).

1.1 Key Features Support Table

Product Line	USB	USCI	UART	I^2C	SPI/I^2S	ISO 7816	PWM	EBI	PDMA	ADC	ACMP	RTC V_{BAT}	V_{DDIO}
M0564	-	3	3	2	2	2	12	Y	5	20	2	Y	Y

Table 1.1-1 Key Features Support Table

The NuMicro® M0564 series is suitable for a wide range of applications such as:

- Industrial Automation
- PLCs
- Inverters
- Home Automation
- Security Alarm System
- Power Metering
- Portable Data Collector
- Portable RFID Reader
- System Supervisors
- Smart Card Reader
- Printer
- Bar Code Scanner
- Motor Control
- Digital Power

2 FEATURES

2.1 NuMicro® M0564 Features

- Core
  - ARM® Cortex®-M0 core running up to 72 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Supports programmable mask-able interrupts
  - Serial Wire Debug supports with 2 watch-points/4 breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5V to 5.5V
- Flash Memory
  - Supports 256/128 KB application ROM (APROM)
  - Supports 4 KB Flash for loader (LDROM)
  - Supports 2 KB Security Protection Rom (SPROM)
  - Supports 12 bytes User Configuration block to control system initiation
  - Supports Data Flash with configurable memory size
  - Supports 2 KB page erase for all embedded flash
  - Supports In-System-Programming (ISP), In-Application-Programming (IAP) update embedded flash memory
  - Supports CRC-32 checksum calculation function
  - Supports flash all one verification function
  - Hardware external read protection of whole flash memory by Security Lock Bit
  - Supports 2-wired ICP update through SWD/ICE interface
- SRAM Memory
  - 20 KB embedded SRAM
  - Supports byte-, half-word- and word-access
  - Supports PDMA mode
- Hardware Divider
  - Signed (two's complement) integer calculation
  - 32-bit dividend with 16-bit divisor calculation capacity
  - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
  - Divided by zero warning flag
  - 6 HCLK clocks taken for one cycle calculation
  - Write divisor to trigger calculation
  - Waiting for calculation ready automatically when reading quotient and remainder
- PDMA (Peripheral DMA)
  - Supports 5 independent configurable channels for automatic data transfer between memories and peripherals
  - Supports single and burst transfer type
  - Supports Normal and Scatter-Gather Transfer modes
  - Supports two types of priorities modes: Fixed-priority and Round-robin modes
  - Supports byte-, half-word- and word-access
  - Supports incrementing mode for the source and destination address for each channel
  - Supports time-out function for channel 0 and channel 1
  - Supports software and SPI/I2S, UART, USCI, ADC, PWM and TIMER request
- Clock Control

- Built-in 22.1184 MHz high speed RC oscillator for system operation (Frequency variation < 2% at -40°C ~ +105°C)
- Built-in 48 MHz internal high speed RC oscillator (Frequency variation < 2% at -40°C ~ +105°C)
- Built-in 10 kHz low speed RC oscillator for Watchdog Timer and Wake-up operation
- Built-in 4~24 MHz high speed crystal oscillator for precise timing operation
- Built-in 32.768 kHz low speed crystal oscillator for Real Time Clock
- Supports PLL up to 144 MHz for high resolution PWM operation
- Supports dynamically calibrating the HIRC48 to 48 MHz ±0.25% by external 32.768K crystal oscillator (LXT)
- Supports dynamically calibrating the HIRC to 22.1184Mhz by external 32.768K crystal oscillator (LXT)
- Supports clock on-the-fly switch
- Supports clock failure detection for system clock
- Supports auto clock switch once clock failure detected
- Supports exception (NMI) generated once a clock failure detected
- Supports divided clock output

● GPIO

- Four I/O modes
- TTL/Schmitt trigger input selectable
- I/O pin configured as interrupt source with edge/level trigger setting
- Supports high driver and high sink current I/O (up to 20 mA at 5V)
- Supports software selectable slew rate control
- Supports up to 81/49/35 GPIOs for LQFP100/64/48 respectively

● Timer/PWM

- Supports 4 sets of Timers/PWM

Timer Mode	PWM Mode
TM_CNT_OUT	PWM_CH0
TM_EXT	PWM_CH1 (Complementary)

- Timer Mode
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function to count the event from external pin
  - Supports input capture function to capture or reset counter value
  - Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
  - Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, EADC and PDMA function
  - Supports Inter-Timer trigger mode
- PWM Mode
  - Supports maximum clock frequency up to 72MHz
  - Supports independent mode for 4 sets of independent PWM output channel
  - Supports complementary mode for 4 sets of complementary paired PWM output channel with 12-bit Dead-time generator
  - Supports 12-bit pre-scalar from 1 to 4096

- Supports 16-bit resolution PWM counter, each timer provides 1 PWM counter
- Supports up, down and up/down counter operation type
- Supports one-shot or Auto-reload counter operation mode
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
- Supports interrupt when PWM counter match zero, period value or compared value, and brake condition happened
- Supports trigger ADC when PWM counter match zero, period value or compared value

● Watchdog Timer

- Supports multiple clock sources from LIRC(default selection), HCLK/2048 and LXT
  8 selectable time-out period from 1.6ms ~ 26.0sec (depending on clock source)
- Able to wake up from Power-down or Idle mode
- Interrupt or reset selectable on watchdog time-out

● Window Watchdog Timer

- Supports multiple clock sources from HCLK/2048 (default selection) and LIRC
  Window set by 6-bit counter with 11-bit prescale
- Interrupt or reset selectable on time-out

● RTC

- Supports separate battery power pin V_{BAT}
- Supports software compensation by setting frequency compensate register (FCR)
- Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
- Supports Alarm registers (second, minute, hour, day, month, year)
- Supports Alarm mask registers
- Selectable 12-hour or 24-hour mode
- Automatic leap year recognition
- Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports wake-up function

• PWM

- Supports maximum clock frequency up to144MHz
- Supports up to two PWM modules, each module provides 6 output channels.
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 2 complementary paired PWM output channel
  - Dead-time insertion with 12-bit resolution
  - Two compared values during one period
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution PWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
  - Brake source from pin and system safety events: clock failed, Brown-out detection and CPU lockup.
  - Noise filter for brake source from pin
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM counter match zero, period value or compared value
  - Brake condition happened
- Supports trigger ADC on the following events:

- PWM counter match zero, period value or compared value
- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

- USCI
  - Supports up to 3 sets of USCI

USCI	UART Mode	SPI Mode	I^2C Mode
USCI_CLK	-	SPI_CLK	SCL
USCI_CTL0	nCTS	SPI_SS	-
USCI_CTL1	nRTS	-	-
USCI_DAT0	Rx	SPI_MOSI	SDA
USCI_DAT1	Tx	SPI_MISO	-

  - UART Mode
    - Supports one transmit buffer and two receive buffer for data payload
    - Supports hardware auto flow control function
    - Supports programmable baud-rate generator
    - Support 9-Bit Data Transfer (Support 9-Bit RS-485)
    - Baud rate detection possible by built-in capture event of baud rate generator
    - Supports Wake-up function (Data and nCTS Wakeup Only)
  - SPI Mode
    - Supports Master or Slave mode operation (the maximum frequency -- Master = fPCLK / 2, Slave = fPCLK / 5)
    - Supports one transmit buffer and two receive buffers for data payload
    - Configurable bit length of a transfer word from 4 to 16-bit
    - Supports MSB first or LSB first transfer sequence
    - Supports Word Suspend function
    - Supports 3-wire, no slave select signal, bi-direction interface
    - Supports wake-up function by slave select signal in Slave mode
    - Supports one data channel half-duplex transfer
  - I^2C Mode
    - Full master and slave device capability
    - Supports of 7-bit addressing, as well as 10-bit addressing
    - Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
    - Supports multi-master bus
    - Supports one transmit buffer and two receive buffer for data payload
    - Supports 10-bit bus time-out capability
    - Supports bus monitor mode.
    - Supports Power down wake-up by data toggle or address match
    - Supports setup/hold time programmable
    - Supports multiple address recognition (two slave address with mask option)

- UART
  - Supports up to 3 sets of UART
  - Full-duplex asynchronous communications
  - Separates receive and transmit 16/16 bytes entry FIFO for data payloads
  - Supports hardware auto-flow control (RX, TX, CTS and RTS)
  - Programmable receiver buffer trigger level
  - Supports programmable baud rate generator for each channel individually
  - Supports 8-bit receiver buffer time-out detection function
  - Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])

- Supports Auto-Baud Rate measurement and baud rate compensation function
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports LIN function mode
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detection function for receiver
- Supports RS-485 mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports PDMA transfer

● Smart Card Host (SC)

- Supports up to two Smart Card Hosts

SC Mode	UART Mode
SC_DATA	Rx
SC_CLK	Tx
SC_CD	-
SC_PWR	-
SC_RST	-

- SC Mode
  - Supports up to two ISO-7816-3 ports
  - Compliant to ISO-7816-3 T=0, T=1
  - Separate receive / transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 266 ETU)
  - One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detecting the card is removal
- UART Mode
  - Full duplex, asynchronous communications
  - Supports receiving / transmitting 4-bytes FIFO
  - Supports programmable baud rate generator for each channel
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1 or 2 stop bit generation

● SPI/I^2S

- Supports up to two SPI/I²S controllers

SPI Mode	I²S Mode
SPI_CLK	I2S_BCLK
SPI_SS	I2S_LRCLK
SPI_MOSI	I2S_DO
SPI_MISO	I2S_DI
-	I2S_MCLK

  - SPI Mode
    - Supports Master or Slave mode operation
    - Configurable bit length of a transfer word from 8 to 32-bit
    - Provides separate 4-/8-level depth transmit and receive FIFO buffers
    - Supports MSB first or LSB first transfer sequence
    - Supports Byte Reorder function
    - Supports PDMA transfer
  - I²S Mode
    - Supports Master or Slave mode operation
    - Capable of handling 8-, 16-, 24- and 32-bit word sizes in I2S mode
    - Provides separate 4-level depth transmit and receive FIFO buffers in I2S mode
    - Supports monaural and stereo audio data in I2S mode
    - Supports PCM mode A, PCM mode B, I2S and MSB justified data format in I2S mode
    - Supports PDMA transfer

- I²C
  - Supports up to two sets of I2C device
  - Supports Master/Slave mode
  - Supports bidirectional data transfer between masters and slaves
  - Supports multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Supports 14-bit time-out counter requesting the I2C interrupt if the I2C bus hangs up and timer-out counter overflows
  - Programmable clocks allow versatile rate control
  - Supports multiple address recognition, four slave address with mask option
  - Supports two-level buffer function
  - Supports setup/hold time programmable
  - Supports wake-up function

- ADC
  - Supports 12-bit SAR ADC
  - 12-bit resolution and 10-bit accuracy is guaranteed
  - Analog input voltage range: 0~ AV_{DD}
  - Supports external V_{REF} pin
  - Up to 20 single-end analog input channels
  - Maximum ADC peripheral clock frequency is 16 MHz
  - Conversion rate up to 800K SPS at 5V
  - Configurable ADC internal sampling time
  - Supports single-scan, single-cycle-scan, and continuous scan and scan on enabled channels

- Supports individual conversion result register with valid and overrun indicators for each channel
- Supports digital comparator to monitor conversion result and user can select whether to generate an interrupt when conversion result matches the compare register setting
- An A/D conversion can be triggered by:
  - Software enable
  - External pin (STADC)
  - Timer 0~3 overflow pulse trigger
  - PWM triggers with optional start delay period
- Supports 4 internal channels for
  - Operational amplifier output
  - Band-gap VBG input
  - Temperature sensor input
  - VBAT voltage measure
- Supports internal reference voltage: 2.048V, 2.560V, 3.072V and 4.096V
- Supports PDMA transfer

● Analog Comparator

- Supports up to 2 rail-to-rail analog comparators
- Supports 4 multiplexed I/O pins at positive node.
- Supports I/O pin and internal voltages at negative node
- Support selectable internal voltage reference from:
  - Band-gap V_{BG}
  - Voltage divider source from AV_{DD} and internal reference voltage.
- Supports programmable hysteresis
- Supports programmable speed and power consumption
- Interrupts generated when compare results change, interrupt event condition is programmable.
- Supports power-down wake-up
- Supports triggers for break events and cycle-by-cycle control for PWM

● Cyclic Redundancy Calculation Unit

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
- Programmable initial value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum.
- Supports 8/16/32-bit of data width
- Interrupt generated once checksum error occurs

● User Configurable VDD1=1.8~5.5V IO Interface

- Supports UART0, SPI0 and I2C0

● Supports 96-bit Unique ID (UID)

● Supports 128-bit Unique Customer ID (UCID)

● One built-in temperature sensor with 1℃ resolution

● Brown-out detector

- With 8 levels: 4.3 V/ 3.7V/ 2.7V/ 2.2V
- Supports Brown-out Interrupt and Reset option

● Low Voltage Reset

- Threshold voltage levels: 2.0 V

● Power consumption

- Chip power down current < 10 uA with RAM data retention.
- V_{BAT} power domain operating current <1.5 uA

- Operating Temperature: -40℃~105℃
- Packages
  - All Green package (RoHS)
  - LQFP 100-pin
  - LQFP 64-pin(7mmx7mm)
  - LQFP 48-pin

3 ABBREVIATIONS

3.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface

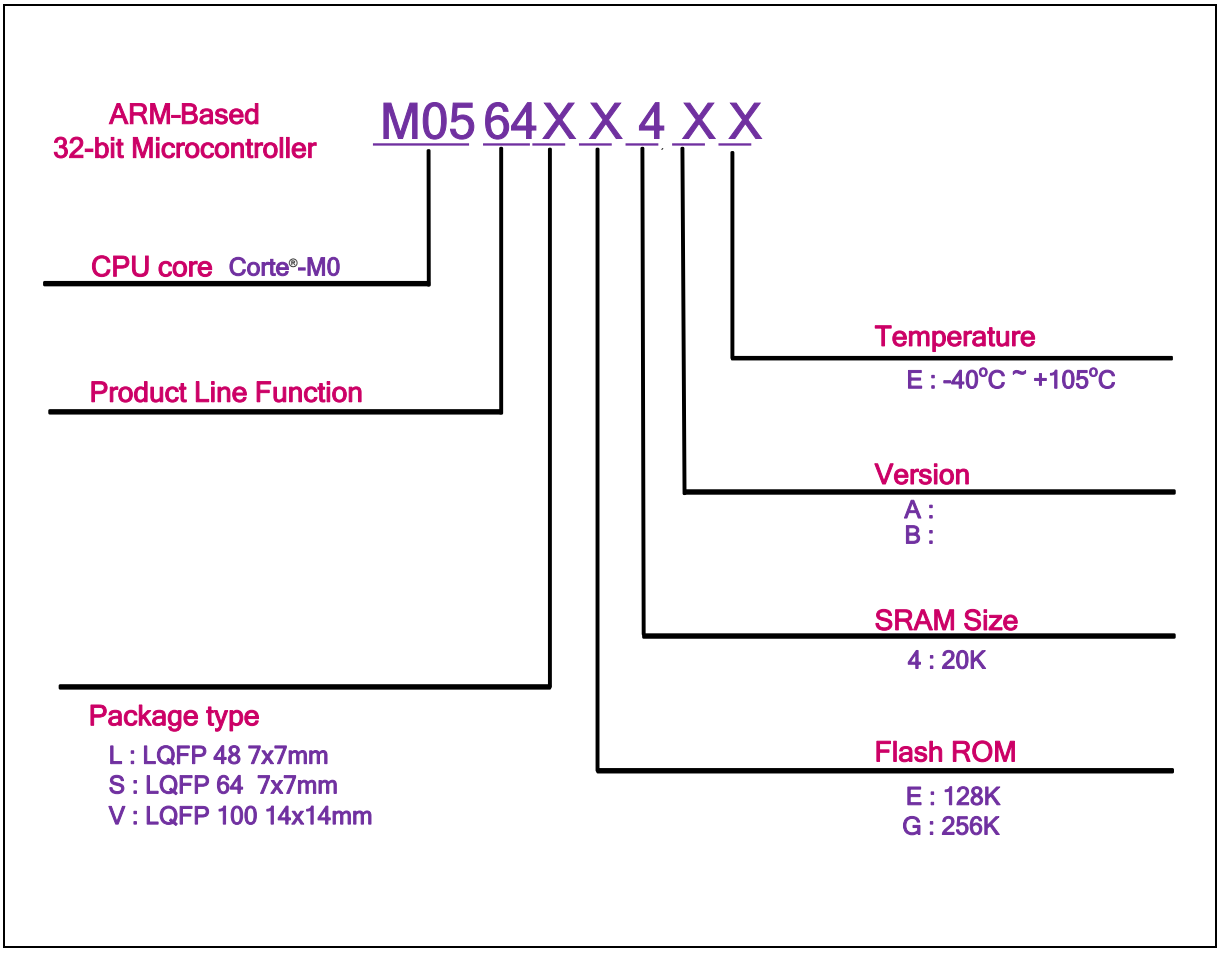
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3.1-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® M0564 Selection Guide

4.1.1 NuMicro® M0564 Naming Rule



4.1.2 NuMicro® M0564 Base Series (M051 Compatible) Selection Guide

Part Number	Flash (KB)	SRAM (KB)	Data Flash(KB)	SPROM(KB)	ISP ROM (KB)	I/O	Timer/PWM	PWM	Connectivity					ADC(12-Bit)	ACMP	PDMA	VBAT(RTC)	V_{DDIO}	EBI	ICP/IAP/ISP	Package
									USCI*	UART	SC/UART	SPI/I^2S	I^2C								
M0564LE4AE	128	20	**Conf***	2	4	41	4	12	3	3	2	2	2	10-ch	2	5	--	√	√	√	LQFP48
M0564LG4AE	256	20	**Conf***	2	4	41	4	12	3	3	2	2	2	10-ch	2	5	--	√	√	√	LQFP48
M0564SE4AE	128	20	**Conf***	2	4	53	4	12	3	3	2	2	2	15-ch	2	5	√	√	√	√	LQFP64*
M0564SG4AE	256	20	**Conf***	2	4	53	4	12	3	3	2	2	2	15-ch	2	5	√	√	√	√	LQFP64*
M0564VG4AE	256	20	**Conf***	2	4	85	4	12	3	3	2	2	2	20-ch	2	5	√	√	√	√	LQFP100

Conf*: Configurable
USCI*: support UART, SPI or I^2C
LQFP64*: 7x7 mm

4.2 Pin Configuration

4.2.1 NuMicro® M0564 Base Series LQFP48 Pin Diagram

Corresponding Part Number: M0564LE4AE, M0564LG4AE

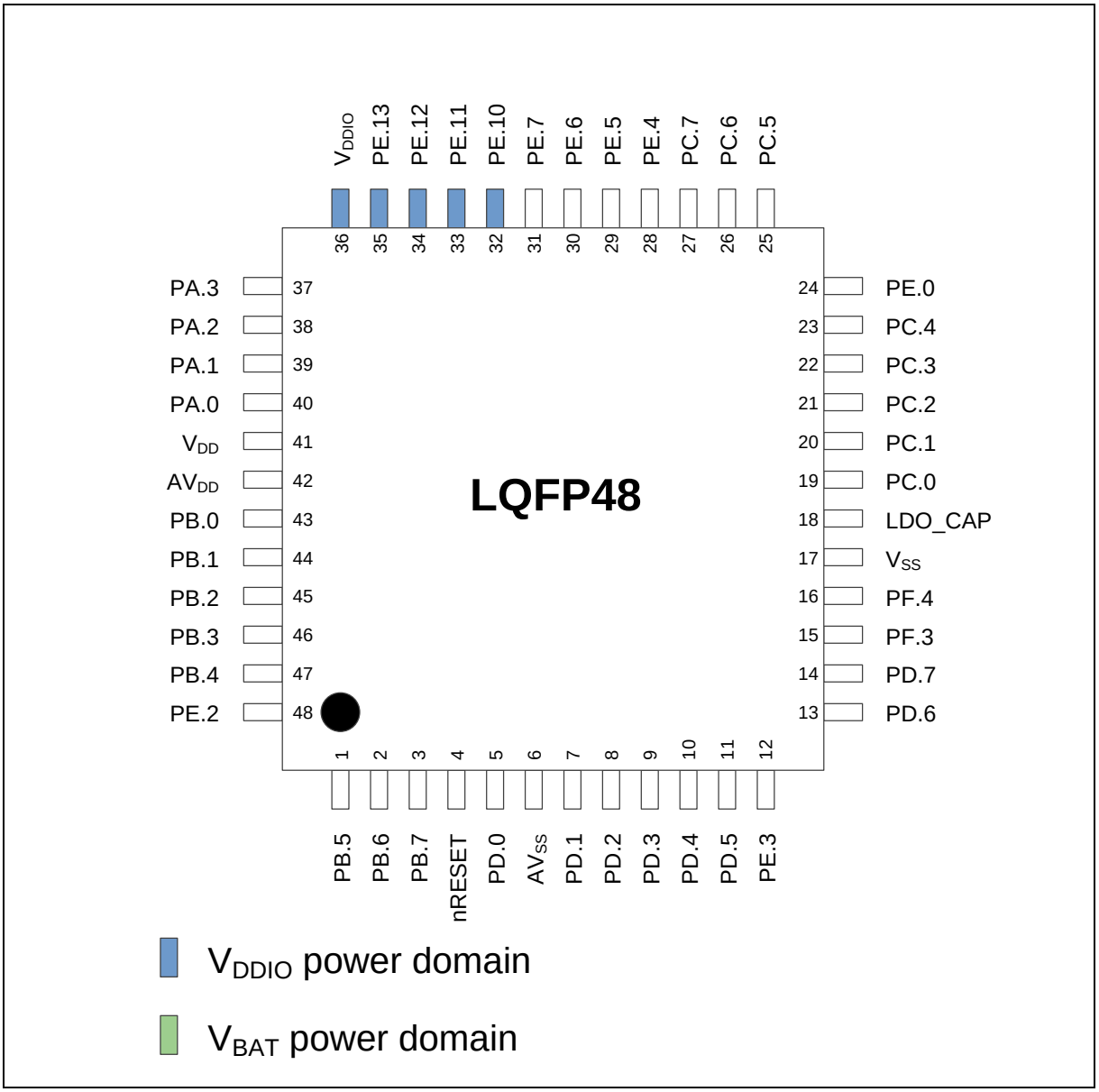


Figure 4.2-1 NuMicro® M0564 Base Series LQFP 48-pin Diagram

4.2.2 NuMicro® M0564 Base Series LQFP64 Pin Diagram

Corresponding Part Number: M0564SE4AE, M0564SG4AE

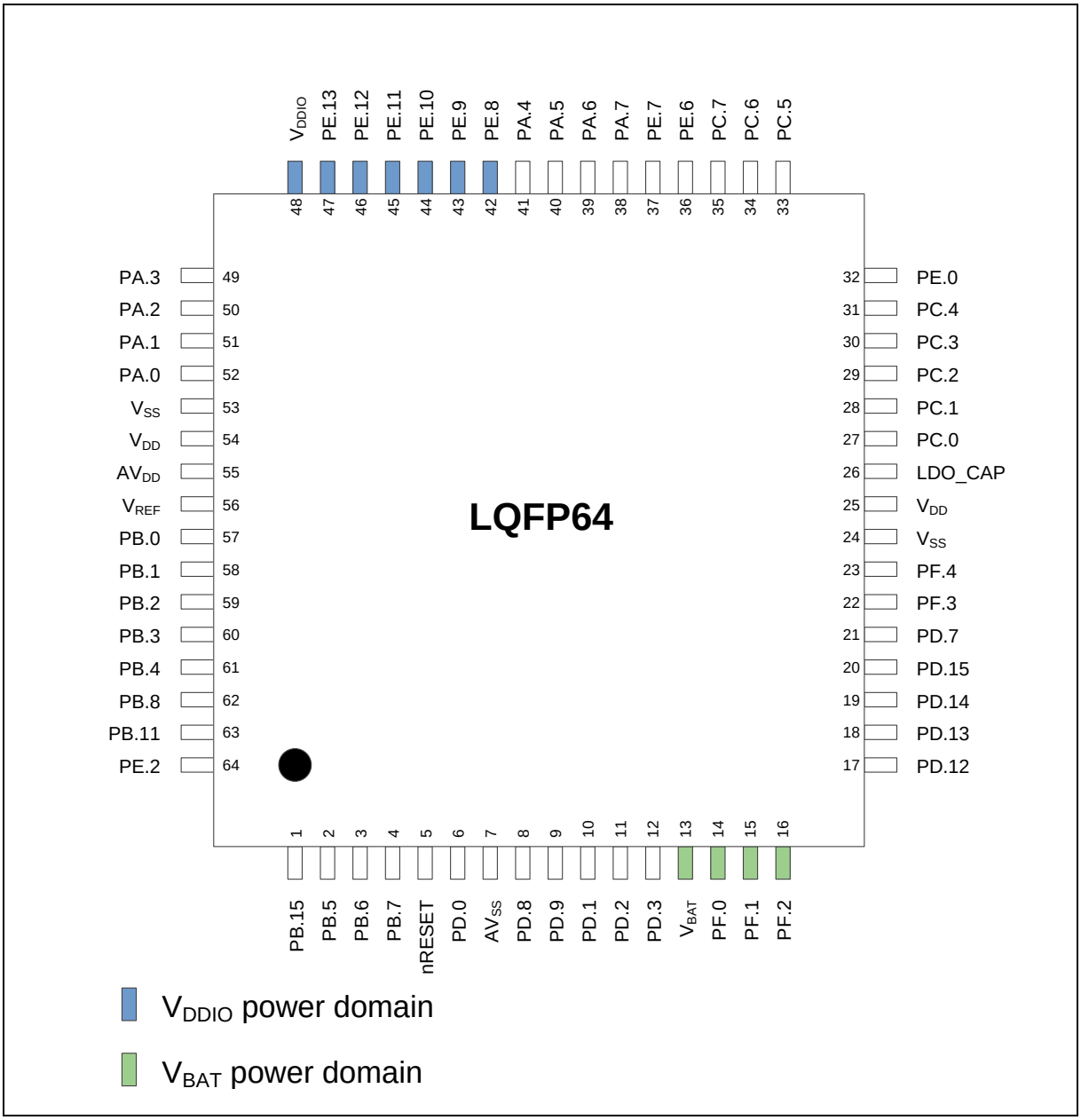


Figure 4.2-2 NuMicro® M0564 Base Series LQFP 64-pin Diagram

4.2.3 NuMicro® M0564 Base Series LQFP100 Pin Diagram

Corresponding Part Number: M0564VG4AE

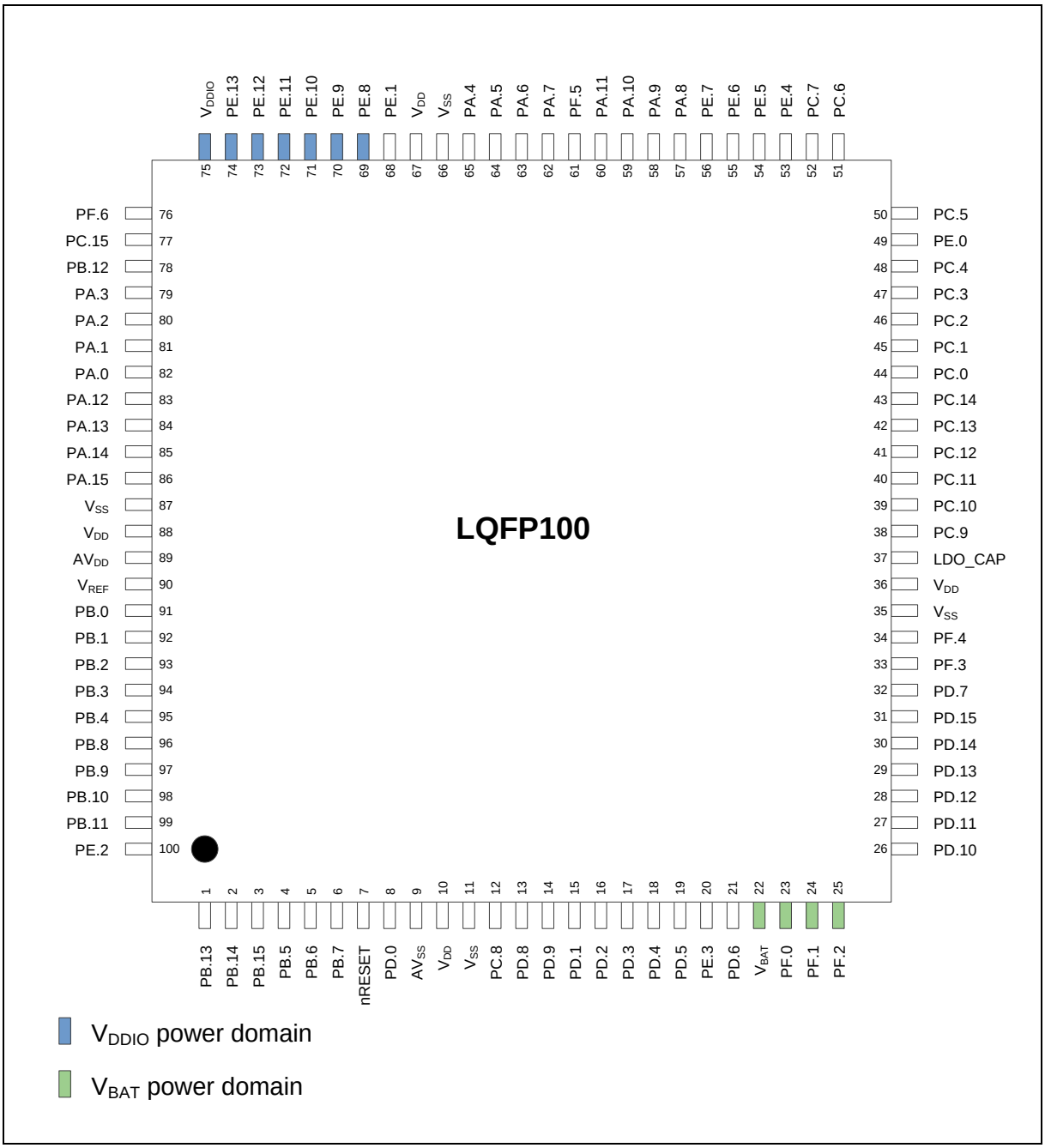


Figure 4.2-3 NuMicro® M0564 Base Series LQFP 100-pin Diagram

4.3 Pin Description

4.3.1 M0564 Base Series Pin Description

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFPL and SYS_GPx_MFPH)

PA.0 MFP0 means SYS_GP0_MFPL[3:0]=0x0.

PA.9 MFP5 means SYS_GP0_MFPH[7:4]=0x5.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
		1	PB.13	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH10	A	MFP1	ADC0 channel 10 analog input.
		2	PB.14	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH11	A	MFP1	ADC0 channel 11 analog input.
	1	3	PB.15	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH12	A	MFP1	ADC0 channel 12 analog input.
			ACMP0_P3	A	MFP5	Analog comparator 0 positive input 3 pin.
			EBI_nCS1	O	MFP7	EBI chip select 1 output pin.
1	2	4	PB.5	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH13	A	MFP1	ADC0 channel 13 analog input.
			SPI0_MOSI	I/O	MFP2	SPI0 MOSI (Master Out, Slave In) pin.
			SPI1_MOSI	I/O	MFP3	SPI1 MOSI (Master Out, Slave In) pin.
			ACMP0_P2	A	MFP5	Analog comparator 0 positive input 2 pin.
			SC1_RST	O	MFP6	Smart Card 1 reset pin.
			EBI_AD6	I/O	MFP7	EBI address/data bus bit 6.
2	3	5	PB.6	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH14	A	MFP1	ADC0 channel 14 analog input.
			SPI0_MISO	I/O	MFP2	SPI0 MISO (Master In, Slave Out) pin.
			SPI1_MISO	I/O	MFP3	SPI1 MISO (Master In, Slave Out) pin.
			ACMP0_P1	A	MFP5	Analog comparator 0 positive input 1 pin.
			SC1_PWR	O	MFP6	Smart Card 1 power pin.
			EBI_AD5	I/O	MFP7	EBI address/data bus bit 5.
3	4	6	PB.7	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH15	A	MFP1	ADC0 channel 15 analog input.
			SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
			SPI1_CLK	I/O	MFP3	SPI1 serial clock pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			USCI2_CTL1	I/O	MFP4	USCI2 control 1 pin.
			ACMP0_P0	A	MFP5	Analog comparator 0 positive input 0 pin.
			SC1_DAT	I/O	MFP6	Smart Card 1 data pin.
			EBI_AD4	I/O	MFP7	EBI address/data bus bit 4.
4	5	7	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
5	6	8	PD.0	I/O	MFP0	General purpose digital I/O pin.
			SPI0_I2SMCLK	I/O	MFP1	SPI0 I2S master clock output pin
			SPI1_I2SMCLK	I/O	MFP2	SPI1 I2S master clock output pin
			UART0_RXD	I	MFP3	UART0 data receiver input pin.
			USCI2_CTL0	I/O	MFP4	USCI2 control 0 pin.
			ACMP1_N	A	MFP5	Analog comparator 1 negative input pin.
			SC1_CLK	O	MFP6	Smart Card 1 clock pin.
			INT3	I	MFP8	External interrupt 3 input pin.
6	7	9	AV_{SS}	P	MFP0	Ground pin for analog circuit.
		10	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
		11	V_{SS}	P	MFP0	Ground pin for digital circuit.
		12	PC.8	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH16	A	MFP1	ADC0 channel 16 analog input.
			UART0_nRTS	O	MFP3	UART0 request to Send output pin.
	8	13	PD.8	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH17	A	MFP1	ADC0 channel 17 analog input.
			UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
			USCI2_CTL1	I/O	MFP4	USCI2 control 1 pin.
			TM2	I/O	MFP6	Timer2 event counter input/toggle output pin.
			EBI_nCS0	O	MFP7	EBI chip select 0 output pin.
	9	14	PD.9	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH18	A	MFP1	ADC0 channel 18 analog input.
			UART0_RXD	I	MFP3	UART0 data receiver input pin.
			USCI2_CTL0	I/O	MFP4	USCI2 control 0 pin.
			ACMP1_P3	A	MFP5	Analog comparator 1 positive input 3 pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			TM3	I/O	MFP6	Timer3 event counter input/toggle output pin.
			EBI_ALE	O	MFP7	EBI address latch enable output pin.
7	10	15	PD.1	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH19	A	MFP1	ADC0 channel 19 analog input.
			PWM0_SYNC_IN	I	MFP2	PWM0 counter synchronous trigger input pin.
			UART0_TXD	O	MFP3	UART0 data transmitter output pin.
			USCI2_CLK	I/O	MFP4	USCI2 clock pin.
			ACMP1_P2	A	MFP5	Analog comparator 1 positive input 2 pin.
			TM0	I/O	MFP6	Timer0 event counter input/toggle output pin.
			EBI_nRD	O	MFP7	EBI read enable output pin.
8	11	16	PD.2	I/O	MFP0	General purpose digital I/O pin.
			ADC0_ST	I	MFP1	ADC0 external trigger input pin.
			TM0_EXT	I/O	MFP3	Timer0 external capture input/toggle output pin.
			USCI2_DAT0	I/O	MFP4	USCI2 data 0 pin.
			ACMP1_P1	A	MFP5	Analog comparator 1 positive input 1 pin.
			PWM0_BRAKE0	I	MFP6	PWM0 Brake 0 input pin.
			EBI_nWR	O	MFP7	EBI write enable output pin.
			INT0	I	MFP8	External interrupt 0 input pin.
9	12	17	PD.3	I/O	MFP0	General purpose digital I/O pin.
			TM2	I/O	MFP1	Timer2 event counter input/toggle output pin.
			SPI0_I2SMCLK	I/O	MFP2	SPI0 I2S master clock output pin
			TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin.
			USCI2_DAT1	I/O	MFP4	USCI2 data 1 pin.
			ACMP1_P0	A	MFP5	Analog comparator 1 positive input 0 pin.
			PWM0_BRAKE1	I	MFP6	PWM0 Brake 1 input pin.
			EBI_MCLK	O	MFP7	EBI external clock output pin.
			INT1	I	MFP8	External interrupt 1 input pin.
10		18	PD.4	I/O	MFP0	General purpose digital I/O pin.
			SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
			I2C0_SDA	I/O	MFP3	I2C0 data input/output pin.
			UART2_nRTS	O	MFP4	UART2 request to Send output pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			PWM0_BRAKE0	I	MFP5	PWM0 Brake 0 input pin.
			TM0	I/O	MFP6	Timer0 event counter input/toggle output pin.
11		19	PD.5	I/O	MFP0	General purpose digital I/O pin.
			CLKO	O	MFP1	Clock Out
			SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin.
			I2C0_SCL	I/O	MFP3	I2C0 clock pin.
			UART2_nCTS	I	MFP4	UART2 clear to Send input pin.
			PWM0_BRAKE1	I	MFP5	PWM0 Brake 1 input pin.
			TM1	I/O	MFP6	Timer1 event counter input/toggle output pin.
12		20	PE.3	I/O	MFP0	General purpose digital I/O pin.
			SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
			UART2_RXD	I	MFP4	UART2 data receiver input pin.
			PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
13		21	PD.6	I/O	MFP0	General purpose digital I/O pin.
			CLKO	O	MFP1	Clock Out
			SPI1_SS	I/O	MFP2	SPI1 slave select pin.
			UART0_RXD	I	MFP3	UART0 data receiver input pin.
			UART2_TXD	O	MFP4	UART2 data transmitter output pin.
			ACMP0_O	O	MFP5	Analog comparator 0 output pin.
			PWM0_CH5	I/O	MFP6	PWM0 channel 5 output/capture input.
			EBI_nWR	O	MFP7	EBI write enable output pin.
	13	22	V_{BAT}	P	MFP0	Power supply by batteries for RTC.
	14	23	PF.0	I/O	MFP0	General purpose digital I/O pin.
			X32_OUT	O	MFP1	External 32.768 kHz crystal output pin.
			USCI2_CTL1	I/O	MFP5	USCI2 control 1 pin.
			INT5	I	MFP8	External interrupt 5 input pin.
	15	24	PF.1	I/O	MFP0	General purpose digital I/O pin.
			X32_IN	I	MFP1	External 32.768 kHz crystal input pin.
			USCI2_CTL0	I/O	MFP5	USCI2 control 0 pin.
			PWM1_BRAKE0	I	MFP6	PWM1 Brake 0 input pin.
	16	25	PF.2	I/O	MFP0	General purpose digital I/O pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			USCI2_CLK	I/O	MFP5	USCI2 clock pin.
			PWM1_BRAKE1	I	MFP6	PWM1 Brake 1 input pin.
		26	PD.10	I/O	MFP0	General purpose digital I/O pin.
			TM2	I/O	MFP4	Timer2 event counter input/toggle output pin.
			USCI2_DAT0	I/O	MFP5	USCI2 data 0 pin.
		27	PD.11	I/O	MFP0	General purpose digital I/O pin.
			TM3	I/O	MFP4	Timer3 event counter input/toggle output pin.
			USCI2_DAT1	I/O	MFP5	USCI2 data 1 pin.
	17	28	PD.12	I/O	MFP0	General purpose digital I/O pin.
			USCI1_CTL0	I/O	MFP1	USCI1 control 0 pin.
			SPI1_SS	I/O	MFP2	SPI1 slave select pin.
			UART0_TXD	O	MFP3	UART0 data transmitter output pin.
			PWM1_CH0	I/O	MFP6	PWM1 channel 0 output/capture input.
			EBI_ADR16	O	MFP7	EBI address bus bit 16.
	18	29	PD.13	I/O	MFP0	General purpose digital I/O pin.
			USCI1_DAT1	I/O	MFP1	USCI1 data 1 pin.
			SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
			UART0_RXD	I	MFP3	UART0 data receiver input pin.
			PWM1_CH1	I/O	MFP6	PWM1 channel 1 output/capture input.
			EBI_ADR17	O	MFP7	EBI address bus bit 17.
	19	30	PD.14	I/O	MFP0	General purpose digital I/O pin.
			USCI1_DAT0	I/O	MFP1	USCI1 data 0 pin.
			SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin.
			UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
			PWM1_CH2	I/O	MFP6	PWM1 channel 2 output/capture input.
			EBI_ADR18	O	MFP7	EBI address bus bit 18.
	20	31	PD.15	I/O	MFP0	General purpose digital I/O pin.
			USCI1_CLK	I/O	MFP1	USCI1 clock pin.
			SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
			UART0_nRTS	O	MFP3	UART0 request to Send output pin.
			PWM1_CH3	I/O	MFP6	PWM1 channel 3 output/capture input.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			EBI_ADR19	O	MFP7	EBI address bus bit 19.
14	21	32	PD.7	I/O	MFP0	General purpose digital I/O pin.
			USCI1_CTL1	I/O	MFP1	USCI1 control 1 pin.
			SPI0_I2SMCLK	I/O	MFP2	SPI0 I2S master clock output pin
			PWM0_SYNC_IN	I	MFP3	PWM0 counter synchronous trigger input pin.
			TM1	I/O	MFP4	Timer1 event counter input/toggle output pin.
			ACMP0_O	O	MFP5	Analog comparator 0 output pin.
			PWM0_CH5	I/O	MFP6	PWM0 channel 5 output/capture input.
			EBI_nRD	O	MFP7	EBI read enable output pin.
15	22	33	PF.3	I/O	MFP0	General purpose digital I/O pin.
			XT1_OUT	O	MFP1	External 4~24 MHz (high speed) crystal output pin.
			I2C1_SCL	I/O	MFP3	I2C1 clock pin.
16	23	34	PF.4	I/O	MFP0	General purpose digital I/O pin.
			XT1_IN	I	MFP1	External 4~24 MHz (high speed) crystal input pin.
			I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
17	24	35	V_{SS}	P	MFP0	Ground pin for digital circuit.
	25	36	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
18	26	37	LDO_CAP	A	MFP0	LDO output pin.
		38	PC.9	I/O	MFP0	General purpose digital I/O pin.
			SPI0_I2SMCLK	I/O	MFP2	SPI0 I2S master clock output pin
			I2C1_SCL	I/O	MFP3	I2C1 clock pin.
			USCI2_CTL1	I/O	MFP4	USCI2 control 1 pin.
			PWM1_CH0	I/O	MFP6	PWM1 channel 0 output/capture input.
		39	PC.10	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MOSI	I/O	MFP2	SPI0 MOSI (Master Out, Slave In) pin.
			I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
			USCI2_DAT1	I/O	MFP4	USCI2 data 1 pin.
			PWM1_CH1	I/O	MFP6	PWM1 channel 1 output/capture input.
		40	PC.11	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MISO	I/O	MFP2	SPI0 MISO (Master In, Slave Out) pin.
			USCI2_CLK	I/O	MFP4	USCI2 clock pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			PWM1_CH2	I/O	MFP6	PWM1 channel 2 output/capture input.
		41	PC.12	I/O	MFP0	General purpose digital I/O pin.
			SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
			USCI2_CTL0	I/O	MFP4	USCI2 control 0 pin.
			PWM1_CH3	I/O	MFP6	PWM1 channel 3 output/capture input.
		42	PC.13	I/O	MFP0	General purpose digital I/O pin.
			SPI0_SS	I/O	MFP2	SPI0 slave select pin.
			USCI2_DAT0	I/O	MFP4	USCI2 data 0 pin.
			PWM1_CH4	I/O	MFP6	PWM1 channel 4 output/capture input.
		43	PC.14	I/O	MFP0	General purpose digital I/O pin.
			PWM1_CH5	I/O	MFP6	PWM1 channel 5 output/capture input.
19	27	44	PC.0	I/O	MFP0	General purpose digital I/O pin.
			SC0_DAT	I/O	MFP1	Smart Card 0 data pin.
			SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
			UART2_nCTS	I	MFP3	UART2 clear to Send input pin.
			USCI0_DAT0	I/O	MFP4	USCI0 data 0 pin.
			ACMP0_WLAT	I	MFP5	Analog comparator 0 window latch input pin
			PWM0_CH0	I/O	MFP6	PWM0 channel 0 output/capture input.
			EBI_AD8	I/O	MFP7	EBI address/data bus bit 8.
			INT2	I	MFP8	External interrupt 2 input pin.
20	28	45	PC.1	I/O	MFP0	General purpose digital I/O pin.
			CLKO	O	MFP1	Clock Out
			SC0_CLK	O	MFP2	Smart Card 0 clock pin.
			UART2_nRTS	O	MFP3	UART2 request to Send output pin.
			USCI0_DAT1	I/O	MFP4	USCI0 data 1 pin.
			ACMP1_WLAT	I	MFP5	Analog comparator 1 window latch input pin
			PWM0_CH1	I/O	MFP6	PWM0 channel 1 output/capture input.
			EBI_AD9	I/O	MFP7	EBI address/data bus bit 9.
21	29	46	PC.2	I/O	MFP0	General purpose digital I/O pin.
			SC0_RST	O	MFP1	Smart Card 0 reset pin.
			SPI0_SS	I/O	MFP2	SPI0 slave select pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			UART2_TXD	O	MFP3	UART2 data transmitter output pin.
			USCI0_CTL1	I/O	MFP4	USCI0 control 1 pin.
			ACMP1_O	O	MFP5	Analog comparator 1 output pin.
			PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
			EBI_AD10	I/O	MFP7	EBI address/data bus bit 10.
22	30	47	PC.3	I/O	MFP0	General purpose digital I/O pin.
			SC0_PWR	O	MFP1	Smart Card 0 power pin.
			SPI0_MOSI	I/O	MFP2	SPI0 MOSI (Master Out, Slave In) pin.
			UART2_RXD	I	MFP3	UART2 data receiver input pin.
			USCI0_CTL0	I/O	MFP5	USCI0 control 0 pin.
			PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
			EBI_AD11	I/O	MFP7	EBI address/data bus bit 11.
23	31	48	PC.4	I/O	MFP0	General purpose digital I/O pin.
			SC0_nCD	I	MFP1	Smart Card 0 card detect pin.
			SPI0_MISO	I/O	MFP2	SPI0 MISO (Master In, Slave Out) pin.
			I2C1_SCL	I/O	MFP3	I2C1 clock pin.
			USCI0_CLK	I/O	MFP5	USCI0 clock pin.
			PWM0_CH4	I/O	MFP6	PWM0 channel 4 output/capture input.
			EBI_AD12	I/O	MFP7	EBI address/data bus bit 12.
24	32	49	PE.0	I/O	MFP0	General purpose digital I/O pin.
			SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
			I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
			TM2_EXT	I/O	MFP4	Timer2 external capture input/toggle output pin.
			SC0_nCD	I	MFP5	Smart Card 0 card detect pin.
			PWM0_CH0	I/O	MFP6	PWM0 channel 0 output/capture input.
			EBI_nCS1	O	MFP7	EBI chip select 1 output pin.
			INT4	I	MFP8	External interrupt 4 input pin.
25	33	50	PC.5	I/O	MFP0	General purpose digital I/O pin.
			SPI0_I2SMCLK	I/O	MFP2	SPI0 I2S master clock output pin
			I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
			USCI0_DAT0	I/O	MFP4	USCI0 data 0 pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			PWM0_CH5	I/O	MFP6	PWM0 channel 5 output/capture input.
			EBI_AD13	I/O	MFP7	EBI address/data bus bit 13.
26	34	51	PC.6	I/O	MFP0	General purpose digital I/O pin.
			USCI0_DAT1	I/O	MFP4	USCI0 data 1 pin.
			ACMP1_O	O	MFP5	Analog comparator 1 output pin.
			PWM1_CH0	I/O	MFP6	PWM1 channel 0 output/capture input.
			EBI_AD14	I/O	MFP7	EBI address/data bus bit 14.
27	35	52	PC.7	I/O	MFP0	General purpose digital I/O pin.
			USCI0_CTL1	I/O	MFP4	USCI0 control 1 pin.
			PWM1_CH1	I/O	MFP6	PWM1 channel 1 output/capture input.
			EBI_AD15	I/O	MFP7	EBI address/data bus bit 15.
28		53	PE.4	I/O	MFP0	General purpose digital I/O pin.
			I2C0_SCL	I/O	MFP2	I2C0 clock pin.
			I2C1_SCL	I/O	MFP3	I2C1 clock pin.
			USCI0_CTL0	I/O	MFP4	USCI0 control 0 pin.
			SC0_PWR	O	MFP5	Smart Card 0 power pin.
			PWM1_BRAKE0	I	MFP6	PWM1 Brake 0 input pin.
			EBI_nCS0	O	MFP7	EBI chip select 0 output pin.
			INT0	I	MFP8	External interrupt 0 input pin.
29		54	PE.5	I/O	MFP0	General purpose digital I/O pin.
			I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
			I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
			USCI0_CLK	I/O	MFP4	USCI0 clock pin.
			SC0_RST	O	MFP5	Smart Card 0 reset pin.
			PWM1_BRAKE1	I	MFP6	PWM1 Brake 1 input pin.
			EBI_ALE	O	MFP7	EBI address latch enable output pin.
			INT1	I	MFP8	External interrupt 1 input pin.
30	36	55	PE.6	I/O	MFP0	General purpose digital I/O pin.
			ICE_CLK	I	MFP1	Serial wired debugger clock pin.
			I2C0_SCL	I/O	MFP2	I2C0 clock pin.
			UART0_RXD	I	MFP3	UART0 data receiver input pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
31	37	56	PE.7	I/O	MFP0	General purpose digital I/O pin.
			ICE_DAT	O	MFP1	Serial wired debugger data pin.
			I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
			UART0_TXD	O	MFP3	UART0 data transmitter output pin.
		57	PA.8	I/O	MFP0	General purpose digital I/O pin.
			UART1_TXD	O	MFP3	UART1 data transmitter output pin.
			SC1_RST	O	MFP5	Smart Card 1 reset pin.
			TM_BRAKE0	I	MFP6	Timer Brake 0 input pin.
		58	PA.9	I/O	MFP0	General purpose digital I/O pin.
			UART1_RXD	I	MFP3	UART1 data receiver input pin.
			SC1_PWR	O	MFP5	Smart Card 1 power pin.
			TM_BRAKE1	I	MFP6	Timer Brake 1 input pin.
		59	PA.10	I/O	MFP0	General purpose digital I/O pin.
			UART1_nCTS	I	MFP3	UART1 clear to Send input pin.
			SC1_DAT	I/O	MFP5	Smart Card 1 data pin.
		60	PA.11	I/O	MFP0	General purpose digital I/O pin.
			UART1_nRTS	O	MFP3	UART1 request to Send output pin.
			SC1_CLK	O	MFP5	Smart Card 1 clock pin.
		61	PF.5	I/O	MFP0	General purpose digital I/O pin.
			TM3_EXT	I/O	MFP3	Timer3 external capture input/toggle output pin.
			SC1_nCD	I	MFP5	Smart Card 1 card detect pin.
			TM_BRAKE0	I	MFP6	Timer Brake 0 input pin.
	38	62	PA.7	I/O	MFP0	General purpose digital I/O pin.
			SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
			TM0_EXT	I/O	MFP3	Timer0 external capture input/toggle output pin.
			TM_BRAKE1	I	MFP6	Timer Brake 1 input pin.
			EBI_AD7	I/O	MFP7	EBI address/data bus bit 7.
	39	63	PA.6	I/O	MFP0	General purpose digital I/O pin.
			SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin.
			TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin.
			TM_BRAKE2	I	MFP6	Timer Brake 2 input pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			EBI_AD6	I/O	MFP7	EBI address/data bus bit 6.
	40	64	PA.5	I/O	MFP0	General purpose digital I/O pin.
			SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
			TM2_EXT	I/O	MFP3	Timer2 external capture input/toggle output pin.
			TM_BRAKE3	I	MFP6	Timer Brake 3 input pin.
			EBI_AD5	I/O	MFP7	EBI address/data bus bit 5.
	41	65	PA.4	I/O	MFP0	General purpose digital I/O pin.
			SPI1_SS	I/O	MFP2	SPI1 slave select pin.
			TM3_EXT	I/O	MFP3	Timer3 external capture input/toggle output pin.
			EBI_AD4	I/O	MFP7	EBI address/data bus bit 4.
		66	V_{SS}	P	MFP0	Ground pin for digital circuit.
		67	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
		68	PE.1	I/O	MFP0	General purpose digital I/O pin.
			TM3_EXT	I/O	MFP3	Timer3 external capture input/toggle output pin.
			SC0_nCD	I	MFP5	Smart Card 0 card detect pin.
			PWM0_CH1	I/O	MFP6	PWM0 channel 1 output/capture input.
	42	69	PE.8	I/O	MFP0	General purpose digital I/O pin.
			UART1_TXD	O	MFP1	UART1 data transmitter output pin.
			TM0	I/O	MFP3	Timer0 event counter input/toggle output pin.
			I2C1_SCL	I/O	MFP4	I2C1 clock pin.
			SC0_PWR	O	MFP5	Smart Card 0 power pin.
	43	70	PE.9	I/O	MFP0	General purpose digital I/O pin.
			UART1_RXD	I	MFP1	UART1 data receiver input pin.
			TM1	I/O	MFP3	Timer1 event counter input/toggle output pin.
			I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
			SC0_RST	O	MFP5	Smart Card 0 reset pin.
32	44	71	PE.10	I/O	MFP0	General purpose digital I/O pin.
			SPI1_MISO	I/O	MFP1	SPI1 MISO (Master In, Slave Out) pin.
			SPI0_MISO	I/O	MFP2	SPI0 MISO (Master In, Slave Out) pin.
			UART1_nCTS	I	MFP3	UART1 clear to Send input pin.
			SC0_DAT	I/O	MFP5	Smart Card 0 data pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			SPI1_CLK	I/O	MFP6	SPI1 serial clock pin.
			EBI_AD7	I/O	MFP7	EBI address/data bus bit 7.
			TM0_EXT	I/O	MFP8	Timer0 external capture input/toggle output pin.
33	45	72	PE.11	I/O	MFP0	General purpose digital I/O pin.
			SPI1_MOSI	I/O	MFP1	SPI1 MOSI (Master Out, Slave In) pin.
			SPI0_MOSI	I/O	MFP2	SPI0 MOSI (Master Out, Slave In) pin.
			UART1_nRTS	O	MFP3	UART1 request to Send output pin.
			SC0_CLK	O	MFP5	Smart Card 0 clock pin.
			SPI1_MISO	I/O	MFP6	SPI1 MISO (Master In, Slave Out) pin.
			EBI_AD6	I/O	MFP7	EBI address/data bus bit 6.
			TM1_EXT	I/O	MFP8	Timer1 external capture input/toggle output pin.
34	46	73	PE.12	I/O	MFP0	General purpose digital I/O pin.
			SPI1_SS	I/O	MFP1	SPI1 slave select pin.
			SPI0_SS	I/O	MFP2	SPI0 slave select pin.
			UART1_TXD	O	MFP3	UART1 data transmitter output pin.
			I2C0_SCL	I/O	MFP4	I2C0 clock pin.
			SPI1_MOSI	I/O	MFP6	SPI1 MOSI (Master Out, Slave In) pin.
			EBI_AD5	I/O	MFP7	EBI address/data bus bit 5.
			TM2_EXT	I/O	MFP8	Timer2 external capture input/toggle output pin.
35	47	74	PE.13	I/O	MFP0	General purpose digital I/O pin.
			SPI1_CLK	I/O	MFP1	SPI1 serial clock pin.
			SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
			UART1_RXD	I	MFP3	UART1 data receiver input pin.
			I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
			SPI1_SS	I/O	MFP6	SPI1 slave select pin.
			EBI_AD4	I/O	MFP7	EBI address/data bus bit 4.
			TM3_EXT	I/O	MFP8	Timer3 external capture input/toggle output pin.
36	48	75	V_{DDIO}	P	MFP0	Power supply for PE.1, PE.8~PE.13.
		76	PF.6	I/O	MFP0	General purpose digital I/O pin.
		77	PC.15	I/O	MFP0	General purpose digital I/O pin.
			PWM1_CH0	I/O	MFP6	PWM1 channel 0 output/capture input.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
		78	PB.12	I/O	MFP0	General purpose digital I/O pin.
			PWM1_CH1	I/O	MFP6	PWM1 channel 1 output/capture input.
37	49	79	PA.3	I/O	MFP0	General purpose digital I/O pin.
			UART0_RXD	I	MFP2	UART0 data receiver input pin.
			UART0_nRTS	O	MFP3	UART0 request to Send output pin.
			I2C0_SCL	I/O	MFP4	I2C0 clock pin.
			SC0_PWR	O	MFP5	Smart Card 0 power pin.
			PWM1_CH2	I/O	MFP6	PWM1 channel 2 output/capture input.
			EBI_AD3	I/O	MFP7	EBI address/data bus bit 3.
			USCI1_CLK	I/O	MFP8	USCI1 clock pin.
38	50	80	PA.2	I/O	MFP0	General purpose digital I/O pin.
			UART0_TXD	O	MFP2	UART0 data transmitter output pin.
			UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
			I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
			SC0_RST	O	MFP5	Smart Card 0 reset pin.
			PWM1_CH3	I/O	MFP6	PWM1 channel 3 output/capture input.
			EBI_AD2	I/O	MFP7	EBI address/data bus bit 2.
			USCI1_CTL0	I/O	MFP8	USCI1 control 0 pin.
39	51	81	PA.1	I/O	MFP0	General purpose digital I/O pin.
			UART1_nRTS	O	MFP1	UART1 request to Send output pin.
			UART1_RXD	I	MFP3	UART1 data receiver input pin.
			USCI1_CTL1	I/O	MFP4	USCI1 control 1 pin.
			SC0_DAT	I/O	MFP5	Smart Card 0 data pin.
			PWM1_CH4	I/O	MFP6	PWM1 channel 4 output/capture input.
			EBI_AD1	I/O	MFP7	EBI address/data bus bit 1.
40	52	82	PA.0	I/O	MFP0	General purpose digital I/O pin.
			UART1_nCTS	I	MFP1	UART1 clear to Send input pin.
			UART1_TXD	O	MFP3	UART1 data transmitter output pin.
			USCI1_CTL0	I/O	MFP4	USCI1 control 0 pin.
			SC0_CLK	O	MFP5	Smart Card 0 clock pin.
			PWM1_CH5	I/O	MFP6	PWM1 channel 5 output/capture input.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			EBI_AD0	I/O	MFP7	EBI address/data bus bit 0.
			INT0	I	MFP8	External interrupt 0 input pin.
		83	PA.12	I/O	MFP0	General purpose digital I/O pin.
			SPI1_I2SMCLK	I/O	MFP2	SPI1 I2S master clock output pin
			UART2_RXD	I	MFP3	UART2 data receiver input pin.
			UART1_RXD	I	MFP4	UART1 data receiver input pin.
			TM_BRAKE2	I	MFP6	Timer Brake 2 input pin.
		84	PA.13	I/O	MFP0	General purpose digital I/O pin.
			UART2_TXD	O	MFP3	UART2 data transmitter output pin.
			UART1_TXD	O	MFP4	UART1 data transmitter output pin.
			TM_BRAKE3	I	MFP6	Timer Brake 3 input pin.
		85	PA.14	I/O	MFP0	General purpose digital I/O pin.
			UART2_nCTS	I	MFP3	UART2 clear to Send input pin.
			USCI1_CTL1	I/O	MFP4	USCI1 control 1 pin.
			TM2	I/O	MFP6	Timer2 event counter input/toggle output pin.
		86	PA.15	I/O	MFP0	General purpose digital I/O pin.
			UART2_nRTS	O	MFP3	UART2 request to Send output pin.
			USCI1_CLK	I/O	MFP4	USCI1 clock pin.
			TM3	I/O	MFP6	Timer3 event counter input/toggle output pin.
	53	87	V_{SS}	P	MFP0	Ground pin for digital circuit.
41	54	88	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
42	55	89	AV_{DD}	P	MFP0	Power supply for internal analog circuit.
	56	90	V_{REF}	A	MFP0	ADC reference voltage input. Note: This pin needs to be connected with a 1uF capacitor.
43	57	91	PB.0	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH0	A	MFP1	ADC0 channel 0 analog input.
			VDET_P0	A	MFP2	Voltage detector positive input 0 pin.
			UART2_RXD	I	MFP3	UART2 data receiver input pin.
			TM2	I/O	MFP4	Timer2 event counter input/toggle output pin.
			USCI1_DAT0	I/O	MFP6	USCI1 data 0 pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			EBI_nWRL	O	MFP7	EBI low byte write enable output pin.
			INT1	I	MFP8	External interrupt 1 input pin.
44	58	92	PB.1	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH1	A	MFP1	ADC0 channel 1 analog input.
			VDET_P1	A	MFP2	Voltage detector positive input 1 pin.
			UART2_TXD	O	MFP3	UART2 data transmitter output pin.
			TM3	I/O	MFP4	Timer3 event counter input/toggle output pin.
			SC0_RST	O	MFP5	Smart Card 0 reset pin.
			PWM0_SYNC_OUT	O	MFP6	PWM0 counter synchronous trigger output pin.
			EBI_nWRH	O	MFP7	EBI high byte write enable output pin
			USCI1_DAT1	I/O	MFP8	USCI1 data 1 pin.
45	59	93	PB.2	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH2	A	MFP1	ADC0 channel 2 analog input.
			SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
			SPI1_CLK	I/O	MFP3	SPI1 serial clock pin.
			UART1_RXD	I	MFP4	UART1 data receiver input pin.
			SC0_nCD	I	MFP5	Smart Card 0 card detect pin.
			TM_BRAKE0	I	MFP6	Timer Brake 0 input pin.
			EBI_nCS0	O	MFP7	EBI chip select 0 output pin.
			USCI0_DAT0	I/O	MFP8	USCI0 data 0 pin.
46	60	94	PB.3	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH3	A	MFP1	ADC0 channel 3 analog input.
			SPI0_MISO	I/O	MFP2	SPI0 MISO (Master In, Slave Out) pin.
			SPI1_MISO	I/O	MFP3	SPI1 MISO (Master In, Slave Out) pin.
			UART1_TXD	O	MFP4	UART1 data transmitter output pin.
			TM_BRAKE1	I	MFP6	Timer Brake 1 input pin.
			EBI_ALE	O	MFP7	EBI address latch enable output pin.
			USCI0_DAT1	I/O	MFP8	USCI0 data 1 pin.
47	61	95	PB.4	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH4	A	MFP1	ADC0 channel 4 analog input.
			SPI0_SS	I/O	MFP2	SPI0 slave select pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			SPI1_SS	I/O	MFP3	SPI1 slave select pin.
			UART1_nCTS	I	MFP4	UART1 clear to Send input pin.
			ACMP0_N	A	MFP5	Analog comparator 0 negative input pin.
			SC1_nCD	I	MFP6	Smart Card 1 card detect pin.
			EBI_AD7	I/O	MFP7	EBI address/data bus bit 7.
			USCI0_CTL1	I/O	MFP8	USCI0 control 1 pin.
	62	96	PB.8	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH5	A	MFP1	ADC0 channel 5 analog input.
			UART1_nRTS	O	MFP4	UART1 request to Send output pin.
			TM_BRAKE2	I	MFP5	Timer Brake 2 input pin.
			PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
			USCI0_CTL0	I/O	MFP8	USCI0 control 0 pin.
		97	PB.9	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH6	A	MFP1	ADC0 channel 6 analog input.
			USCI0_CLK	I/O	MFP8	USCI0 clock pin.
		98	PB.10	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH7	A	MFP1	ADC0 channel 7 analog input.
	63	99	PB.11	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH8	A	MFP1	ADC0 channel 8 analog input.
48	64	100	PE.2	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH9	A	MFP1	ADC0 channel 9 analog input.
			UART1_nRTS	O	MFP4	UART1 request to Send output pin.
			TM_BRAKE3	I	MFP5	Timer Brake 3 input pin.
			PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
			USCI0_CTL0	I/O	MFP8	USCI0 control 0 pin.

4.3.2 GPIO Multi-function Pin Summary

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFPL and SYS_GPx_MFPH)

PA.0 MFP0 means SYS_GP0_MFPL[3:0]=0x0.

PA.9 MFP5 means SYS_GP0_MFPH[7:4]=0x5.

Group	Pin Name	GPIO	MFP	Type	Description
ACMP0	ACMP0_N	PB.4	MFP5	A	Analog comparator 0 negative input pin.
	ACMP0_O	PD.6	MFP5	O	Analog comparator 0 output pin.
		PD.7	MFP5	O	
	ACMP0_P0	PB.7	MFP5	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1	PB.6	MFP5	A	Analog comparator 0 positive input 1 pin.
	ACMP0_P2	PB.5	MFP5	A	Analog comparator 0 positive input 2 pin.
	ACMP0_P3	PB.15	MFP5	A	Analog comparator 0 positive input 3 pin.
	ACMP0_WLAT	PC.0	MFP5	I	Analog comparator 0 window latch input pin
ACMP1	ACMP1_N	PD.0	MFP5	A	Analog comparator 1 negative input pin.
	ACMP1_O	PC.2	MFP5	O	Analog comparator 1 output pin.
		PC.6	MFP5	O	
	ACMP1_P0	PD.3	MFP5	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1	PD.2	MFP5	A	Analog comparator 1 positive input 1 pin.
	ACMP1_P2	PD.1	MFP5	A	Analog comparator 1 positive input 2 pin.
	ACMP1_P3	PD.9	MFP5	A	Analog comparator 1 positive input 3 pin.
	ACMP1_WLAT	PC.1	MFP5	I	Analog comparator 1 window latch input pin
ADC0	ADC0_CH0	PB.0	MFP1	A	ADC0 channel 0 analog input.
	ADC0_CH1	PB.1	MFP1	A	ADC0 channel 1 analog input.
	ADC0_CH2	PB.2	MFP1	A	ADC0 channel 2 analog input.
	ADC0_CH3	PB.3	MFP1	A	ADC0 channel 3 analog input.
	ADC0_CH4	PB.4	MFP1	A	ADC0 channel 4 analog input.
	ADC0_CH5	PB.8	MFP1	A	ADC0 channel 5 analog input.
	ADC0_CH6	PB.9	MFP1	A	ADC0 channel 6 analog input.
	ADC0_CH7	PB.10	MFP1	A	ADC0 channel 7 analog input.
	ADC0_CH8	PB.11	MFP1	A	ADC0 channel 8 analog input.
	ADC0_CH9	PE.2	MFP1	A	ADC0 channel 9 analog input.
	ADC0_CH10	PB.13	MFP1	A	ADC0 channel 10 analog input.

Group	Pin Name	GPIO	MFP	Type	Description
	ADC0_CH11	PB.14	MFP1	A	ADC0 channel 11 analog input.
	ADC0_CH12	PB.15	MFP1	A	ADC0 channel 12 analog input.
	ADC0_CH13	PB.5	MFP1	A	ADC0 channel 13 analog input.
	ADC0_CH14	PB.6	MFP1	A	ADC0 channel 14 analog input.
	ADC0_CH15	PB.7	MFP1	A	ADC0 channel 15 analog input.
	ADC0_CH16	PC.8	MFP1	A	ADC0 channel 16 analog input.
	ADC0_CH17	PD.8	MFP1	A	ADC0 channel 17 analog input.
	ADC0_CH18	PD.9	MFP1	A	ADC0 channel 18 analog input.
	ADC0_CH19	PD.1	MFP1	A	ADC0 channel 19 analog input.
	ADC0_ST	PD.2	MFP1	I	ADC0 external trigger input pin.
CLKO	CLKO	PD.5	MFP1	O	Clock Out
		PD.6	MFP1	O	
		PC.1	MFP1	O	
EBI	EBI_AD0	PA.0	MFP7	I/O	EBI address/data bus bit 0.
	EBI_AD1	PA.1	MFP7	I/O	EBI address/data bus bit 1.
	EBI_AD2	PA.2	MFP7	I/O	EBI address/data bus bit 2.
	EBI_AD3	PA.3	MFP7	I/O	EBI address/data bus bit 3.
	EBI_AD4	PB.7	MFP7	I/O	EBI address/data bus bit 4.
		PA.4	MFP7	I/O	
		PE.13	MFP7	I/O	
	EBI_AD5	PB.6	MFP7	I/O	EBI address/data bus bit 5.
		PA.5	MFP7	I/O	
		PE.12	MFP7	I/O	
	EBI_AD6	PB.5	MFP7	I/O	EBI address/data bus bit 6.
		PA.6	MFP7	I/O	
		PE.11	MFP7	I/O	
	EBI_AD7	PA.7	MFP7	I/O	EBI address/data bus bit 7.
		PE.10	MFP7	I/O	
		PB.4	MFP7	I/O	
	EBI_AD8	PC.0	MFP7	I/O	EBI address/data bus bit 8.
	EBI_AD9	PC.1	MFP7	I/O	EBI address/data bus bit 9.
	EBI_AD10	PC.2	MFP7	I/O	EBI address/data bus bit 10.

Group	Pin Name	GPIO	MFP	Type	Description
	EBI_AD11	PC.3	MFP7	I/O	EBI address/data bus bit 11.
	EBI_AD12	PC.4	MFP7	I/O	EBI address/data bus bit 12.
	EBI_AD13	PC.5	MFP7	I/O	EBI address/data bus bit 13.
	EBI_AD14	PC.6	MFP7	I/O	EBI address/data bus bit 14.
	EBI_AD15	PC.7	MFP7	I/O	EBI address/data bus bit 15.
	EBI_ADR16	PD.12	MFP7	O	EBI address bus bit 16.
	EBI_ADR17	PD.13	MFP7	O	EBI address bus bit 17.
	EBI_ADR18	PD.14	MFP7	O	EBI address bus bit 18.
	EBI_ADR19	PD.15	MFP7	O	EBI address bus bit 19.
	EBI_ALE	PD.9	MFP7	O	EBI address latch enable output pin.
		PE.5	MFP7	O	
		PB.3	MFP7	O	
	EBI_MCLK	PD.3	MFP7	O	EBI external clock output pin.
	EBI_nCS0	PD.8	MFP7	O	EBI chip select 0 output pin.
		PE.4	MFP7	O	
		PB.2	MFP7	O	
	EBI_nCS1	PB.15	MFP7	O	EBI chip select 1 output pin.
		PE.0	MFP7	O	
	EBI_nRD	PD.1	MFP7	O	EBI read enable output pin.
		PD.7	MFP7	O	
	EBI_nWR	PD.2	MFP7	O	EBI write enable output pin.
		PD.6	MFP7	O	
	EBI_nWRH	PB.1	MFP7	O	EBI high byte write enable output pin
	EBI_nWRL	PB.0	MFP7	O	EBI low byte write enable output pin.
I2C0	I2C0_SCL	PD.5	MFP3	I/O	I2C0 clock pin.
		PE.4	MFP2	I/O	
		PE.6	MFP2	I/O	
		PE.12	MFP4	I/O	
		PA.3	MFP4	I/O	
	I2C0_SDA	PD.4	MFP3	I/O	I2C0 data input/output pin.
		PE.5	MFP2	I/O	
		PE.7	MFP2	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PE.13	MFP4	I/O	
		PA.2	MFP4	I/O	
I2C1	I2C1_SCL	PF.3	MFP3	I/O	I2C1 clock pin.
		PC.9	MFP3	I/O	
		PC.4	MFP3	I/O	
		PE.4	MFP3	I/O	
		PE.8	MFP4	I/O	
	I2C1_SDA	PF.4	MFP3	I/O	I2C1 data input/output pin.
		PC.10	MFP3	I/O	
		PE.0	MFP3	I/O	
		PC.5	MFP3	I/O	
		PE.5	MFP3	I/O	
		PE.9	MFP4	I/O	
ICE	ICE_CLK	PE.6	MFP1	I	Serial wired debugger clock pin.
	ICE_DAT	PE.7	MFP1	O	Serial wired debugger data pin.
INT0	INT0	PD.2	MFP8	I	External interrupt 0 input pin.
		PE.4	MFP8	I	
		PA.0	MFP8	I	
INT1	INT1	PD.3	MFP8	I	External interrupt 1 input pin.
		PE.5	MFP8	I	
		PB.0	MFP8	I	
INT2	INT2	PC.0	MFP8	I	External interrupt 2 input pin.
INT3	INT3	PD.0	MFP8	I	External interrupt 3 input pin.
INT4	INT4	PE.0	MFP8	I	External interrupt 4 input pin.
INT5	INT5	PF.0	MFP8	I	External interrupt 5 input pin.
PWM0	PWM0_BRAKE0	PD.2	MFP6	I	PWM0 Brake 0 input pin.
		PD.4	MFP5	I	
	PWM0_BRAKE1	PD.3	MFP6	I	PWM0 Brake 1 input pin.
		PD.5	MFP5	I	
	PWM0_CH0	PC.0	MFP6	I/O	PWM0 channel 0 output/capture input.
		PE.0	MFP6	I/O	
	PWM0_CH1	PC.1	MFP6	I/O	PWM0 channel 1 output/capture input.

Group	Pin Name	GPIO	MFP	Type	Description
		PE.1	MFP6	I/O	
	PWM0_CH2	PC.2	MFP6	I/O	PWM0 channel 2 output/capture input.
		PB.8	MFP6	I/O	
		PE.2	MFP6	I/O	
	PWM0_CH3	PE.3	MFP6	I/O	PWM0 channel 3 output/capture input.
		PC.3	MFP6	I/O	
	PWM0_CH4	PC.4	MFP6	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH5	PD.6	MFP6	I/O	PWM0 channel 5 output/capture input.
		PD.7	MFP6	I/O	
		PC.5	MFP6	I/O	
	PWM0_SYNC_IN	PD.1	MFP2	I	PWM0 counter synchronous trigger input pin.
		PD.7	MFP3	I	
	PWM0_SYNC_OUT	PB.1	MFP6	O	PWM0 counter synchronous trigger output pin.
PWM1	PWM1_BRAKE0	PF.1	MFP6	I	PWM1 Brake 0 input pin.
		PE.4	MFP6	I	
	PWM1_BRAKE1	PF.2	MFP6	I	PWM1 Brake 1 input pin.
		PE.5	MFP6	I	
	PWM1_CH0	PD.12	MFP6	I/O	PWM1 channel 0 output/capture input.
		PC.9	MFP6	I/O	
		PC.6	MFP6	I/O	
		PC.15	MFP6	I/O	
	PWM1_CH1	PD.13	MFP6	I/O	PWM1 channel 1 output/capture input.
		PC.10	MFP6	I/O	
		PC.7	MFP6	I/O	
		PB.12	MFP6	I/O	
	PWM1_CH2	PD.14	MFP6	I/O	PWM1 channel 2 output/capture input.
		PC.11	MFP6	I/O	
		PA.3	MFP6	I/O	
	PWM1_CH3	PD.15	MFP6	I/O	PWM1 channel 3 output/capture input.
		PC.12	MFP6	I/O	
		PA.2	MFP6	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
	PWM1_CH4	PC.13	MFP6	I/O	PWM1 channel 4 output/capture input.
		PA.1	MFP6	I/O	
	PWM1_CH5	PC.14	MFP6	I/O	PWM1 channel 5 output/capture input.
		PA.0	MFP6	I/O	
SC0	SC0_CLK	PC.1	MFP2	O	Smart Card 0 clock pin.
		PE.11	MFP5	O	
		PA.0	MFP5	O	
	SC0_DAT	PC.0	MFP1	I/O	Smart Card 0 data pin.
		PE.10	MFP5	I/O	
		PA.1	MFP5	I/O	
	SC0_PWR	PC.3	MFP1	O	Smart Card 0 power pin.
		PE.4	MFP5	O	
		PE.8	MFP5	O	
		PA.3	MFP5	O	
	SC0_RST	PC.2	MFP1	O	Smart Card 0 reset pin.
		PE.5	MFP5	O	
		PE.9	MFP5	O	
		PA.2	MFP5	O	
		PB.1	MFP5	O	
	SC0_nCD	PC.4	MFP1	I	Smart Card 0 card detect pin.
		PE.0	MFP5	I	
		PE.1	MFP5	I	
		PB.2	MFP5	I	
SC1	SC1_CLK	PD.0	MFP6	O	Smart Card 1 clock pin.
		PA.11	MFP5	O	
	SC1_DAT	PB.7	MFP6	I/O	Smart Card 1 data pin.
		PA.10	MFP5	I/O	
	SC1_PWR	PB.6	MFP6	O	Smart Card 1 power pin.
		PA.9	MFP5	O	
	SC1_RST	PB.5	MFP6	O	Smart Card 1 reset pin.
		PA.8	MFP5	O	
	SC1_nCD	PF.5	MFP5	I	Smart Card 1 card detect pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PB.4	MFP6	I	
SPI0	SPI0_CLK	PB.7	MFP2	I/O	SPI0 serial clock pin.
		PC.12	MFP2	I/O	
		PC.0	MFP2	I/O	
		PE.0	MFP2	I/O	
		PE.13	MFP2	I/O	
		PB.2	MFP2	I/O	
	SPI0_I2SMCLK	PD.0	MFP1	I/O	SPI0 I2S master clock output pin
		PD.3	MFP2	I/O	
		PD.7	MFP2	I/O	
		PC.9	MFP2	I/O	
		PC.5	MFP2	I/O	
	SPI0_MISO	PB.6	MFP2	I/O	SPI0 MISO (Master In, Slave Out) pin.
		PC.11	MFP2	I/O	
		PC.4	MFP2	I/O	
		PE.10	MFP2	I/O	
		PB.3	MFP2	I/O	
	SPI0_MOSI	PB.5	MFP2	I/O	SPI0 MOSI (Master Out, Slave In) pin.
		PC.10	MFP2	I/O	
		PC.3	MFP2	I/O	
		PE.11	MFP2	I/O	
	SPI0_SS	PC.13	MFP2	I/O	SPI0 slave select pin.
		PC.2	MFP2	I/O	
		PE.12	MFP2	I/O	
		PB.4	MFP2	I/O	
SPI1	SPI1_CLK	PB.7	MFP3	I/O	SPI1 serial clock pin.
		PD.4	MFP2	I/O	
		PD.15	MFP2	I/O	
		PA.7	MFP2	I/O	
		PE.10	MFP6	I/O	
		PE.13	MFP1	I/O	
		PB.2	MFP3	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
	SPI1_I2SMCLK	PD.0	MFP2	I/O	SPI1 I2S master clock output pin
		PA.12	MFP2	I/O	
	SPI1_MISO	PB.6	MFP3	I/O	SPI1 MISO (Master In, Slave Out) pin.
		PD.5	MFP2	I/O	
		PD.14	MFP2	I/O	
		PA.6	MFP2	I/O	
		PE.10	MFP1	I/O	
		PE.11	MFP6	I/O	
		PB.3	MFP3	I/O	
	SPI1_MOSI	PB.5	MFP3	I/O	SPI1 MOSI (Master Out, Slave In) pin.
		PE.3	MFP2	I/O	
		PD.13	MFP2	I/O	
		PA.5	MFP2	I/O	
		PE.11	MFP1	I/O	
		PE.12	MFP6	I/O	
	SPI1_SS	PD.6	MFP2	I/O	SPI1 slave select pin.
		PD.12	MFP2	I/O	
		PA.4	MFP2	I/O	
		PE.12	MFP1	I/O	
		PE.13	MFP6	I/O	
		PB.4	MFP3	I/O	
TM0	TM0	PD.1	MFP6	I/O	Timer0 event counter input/toggle output pin.
		PD.4	MFP6	I/O	
		PE.8	MFP3	I/O	
	TM0_EXT	PD.2	MFP3	I/O	Timer0 external capture input/toggle output pin.
		PA.7	MFP3	I/O	
		PE.10	MFP8	I/O	
TM1	TM1	PD.5	MFP6	I/O	Timer1 event counter input/toggle output pin.
		PD.7	MFP4	I/O	
		PE.9	MFP3	I/O	
	TM1_EXT	PD.3	MFP3	I/O	Timer1 external capture input/toggle output pin.
		PA.6	MFP3	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PE.11	MFP8	I/O	
TM2	TM2	PD.8	MFP6	I/O	Timer2 event counter input/toggle output pin.
		PD.3	MFP1	I/O	
		PD.10	MFP4	I/O	
		PA.14	MFP6	I/O	
		PB.0	MFP4	I/O	
	TM2_EXT	PE.0	MFP4	I/O	Timer2 external capture input/toggle output pin.
		PA.5	MFP3	I/O	
		PE.12	MFP8	I/O	
TM3	TM3	PD.9	MFP6	I/O	Timer3 event counter input/toggle output pin.
		PD.11	MFP4	I/O	
		PA.15	MFP6	I/O	
		PB.1	MFP4	I/O	
	TM3_EXT	PF.5	MFP3	I/O	Timer3 external capture input/toggle output pin.
		PA.4	MFP3	I/O	
		PE.1	MFP3	I/O	
		PE.13	MFP8	I/O	
TM	TM_BRAKE0	PA.8	MFP6	I	Timer Brake 0 input pin.
		PF.5	MFP6	I	
		PB.2	MFP6	I	
	TM_BRAKE1	PA.9	MFP6	I	Timer Brake 1 input pin.
		PA.7	MFP6	I	
		PB.3	MFP6	I	
	TM_BRAKE2	PA.6	MFP6	I	Timer Brake 2 input pin.
		PA.12	MFP6	I	
		PB.8	MFP5	I	
	TM_BRAKE3	PA.5	MFP6	I	Timer Brake 3 input pin.
		PA.13	MFP6	I	
		PE.2	MFP5	I	
UART0	UART0_RXD	PD.0	MFP3	I	UART0 data receiver input pin.
		PD.9	MFP3	I	
		PD.6	MFP3	I	

Group	Pin Name	GPIO	MFP	Type	Description
		PD.13	MFP3	I	
		PE.6	MFP3	I	
		PA.3	MFP2	I	
	UART0_TXD	PD.1	MFP3	O	UART0 data transmitter output pin.
		PD.12	MFP3	O	
		PE.7	MFP3	O	
		PA.2	MFP2	O	
	UART0_nCTS	PD.8	MFP3	I	UART0 clear to Send input pin.
		PD.14	MFP3	I	
		PA.2	MFP3	I	
	UART0_nRTS	PC.8	MFP3	O	UART0 request to Send output pin.
		PD.15	MFP3	O	
		PA.3	MFP3	O	
UART1	UART1_RXD	PA.9	MFP3	I	UART1 data receiver input pin.
		PE.9	MFP1	I	
		PE.13	MFP3	I	
		PA.1	MFP3	I	
		PA.12	MFP4	I	
		PB.2	MFP4	I	
	UART1_TXD	PA.8	MFP3	O	UART1 data transmitter output pin.
		PE.8	MFP1	O	
		PE.12	MFP3	O	
		PA.0	MFP3	O	
		PA.13	MFP4	O	
		PB.3	MFP4	O	
	UART1_nCTS	PA.10	MFP3	I	UART1 clear to Send input pin.
		PE.10	MFP3	I	
		PA.0	MFP1	I	
		PB.4	MFP4	I	
	UART1_nRTS	PA.11	MFP3	O	UART1 request to Send output pin.
		PE.11	MFP3	O	
		PA.1	MFP1	O	

Group	Pin Name	GPIO	MFP	Type	Description
		PB.8	MFP4	O	
		PE.2	MFP4	O	
UART2	UART2_RXD	PE.3	MFP4	I	UART2 data receiver input pin.
		PC.3	MFP3	I	
		PA.12	MFP3	I	
		PB.0	MFP3	I	
	UART2_TXD	PD.6	MFP4	O	UART2 data transmitter output pin.
		PC.2	MFP3	O	
		PA.13	MFP3	O	
		PB.1	MFP3	O	
	UART2_nCTS	PD.5	MFP4	I	UART2 clear to Send input pin.
		PC.0	MFP3	I	
		PA.14	MFP3	I	
	UART2_nRTS	PD.4	MFP4	O	UART2 request to Send output pin.
		PC.1	MFP3	O	
		PA.15	MFP3	O	
USCI0	USCI0_CLK	PC.4	MFP5	I/O	USCI0 clock pin.
		PE.5	MFP4	I/O	
		PB.9	MFP8	I/O	
	USCI0_CTL0	PC.3	MFP5	I/O	USCI0 control 0 pin.
		PE.4	MFP4	I/O	
		PB.8	MFP8	I/O	
		PE.2	MFP8	I/O	
	USCI0_CTL1	PC.2	MFP4	I/O	USCI0 control 1 pin.
		PC.7	MFP4	I/O	
		PB.4	MFP8	I/O	
	USCI0_DAT0	PC.0	MFP4	I/O	USCI0 data 0 pin.
		PC.5	MFP4	I/O	
		PB.2	MFP8	I/O	
	USCI0_DAT1	PC.1	MFP4	I/O	USCI0 data 1 pin.
		PC.6	MFP4	I/O	
		PB.3	MFP8	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
USCI1	USCI1_CLK	PD.15	MFP1	I/O	USCI1 clock pin.
		PA.3	MFP8	I/O	
		PA.15	MFP4	I/O	
	USCI1_CTL0	PD.12	MFP1	I/O	USCI1 control 0 pin.
		PA.2	MFP8	I/O	
		PA.0	MFP4	I/O	
	USCI1_CTL1	PD.7	MFP1	I/O	USCI1 control 1 pin.
		PA.1	MFP4	I/O	
		PA.14	MFP4	I/O	
	USCI1_DAT0	PD.14	MFP1	I/O	USCI1 data 0 pin.
		PB.0	MFP6	I/O	
	USCI1_DAT1	PD.13	MFP1	I/O	USCI1 data 1 pin.
		PB.1	MFP8	I/O	
USCI2	USCI2_CLK	PD.1	MFP4	I/O	USCI2 clock pin.
		PF.2	MFP5	I/O	
		PC.11	MFP4	I/O	
	USCI2_CTL0	PD.0	MFP4	I/O	USCI2 control 0 pin.
		PD.9	MFP4	I/O	
		PF.1	MFP5	I/O	
		PC.12	MFP4	I/O	
	USCI2_CTL1	PB.7	MFP4	I/O	USCI2 control 1 pin.
		PD.8	MFP4	I/O	
		PF.0	MFP5	I/O	
		PC.9	MFP4	I/O	
	USCI2_DAT0	PD.2	MFP4	I/O	USCI2 data 0 pin.
		PD.10	MFP5	I/O	
		PC.13	MFP4	I/O	
	USCI2_DAT1	PD.3	MFP4	I/O	USCI2 data 1 pin.
		PD.11	MFP5	I/O	
		PC.10	MFP4	I/O	
VDET	VDET_P0	PB.0	MFP2	A	Voltage detector positive input 0 pin.
	VDET_P1	PB.1	MFP2	A	Voltage detector positive input 1 pin.

Group	Pin Name	GPIO	MFP	Type	Description
X32	X32_IN	PF.1	MFP1	I	External 32.768 kHz crystal input pin.
	X32_OUT	PF.0	MFP1	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	PF.4	MFP1	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	PF.3	MFP1	O	External 4~24 MHz (high speed) crystal output pin.

Table 4.3-1 M0564 GPIO Multi-function Table

5 BLOCK DIAGRAM

5.1 NuMicro® M0564 Block Diagram

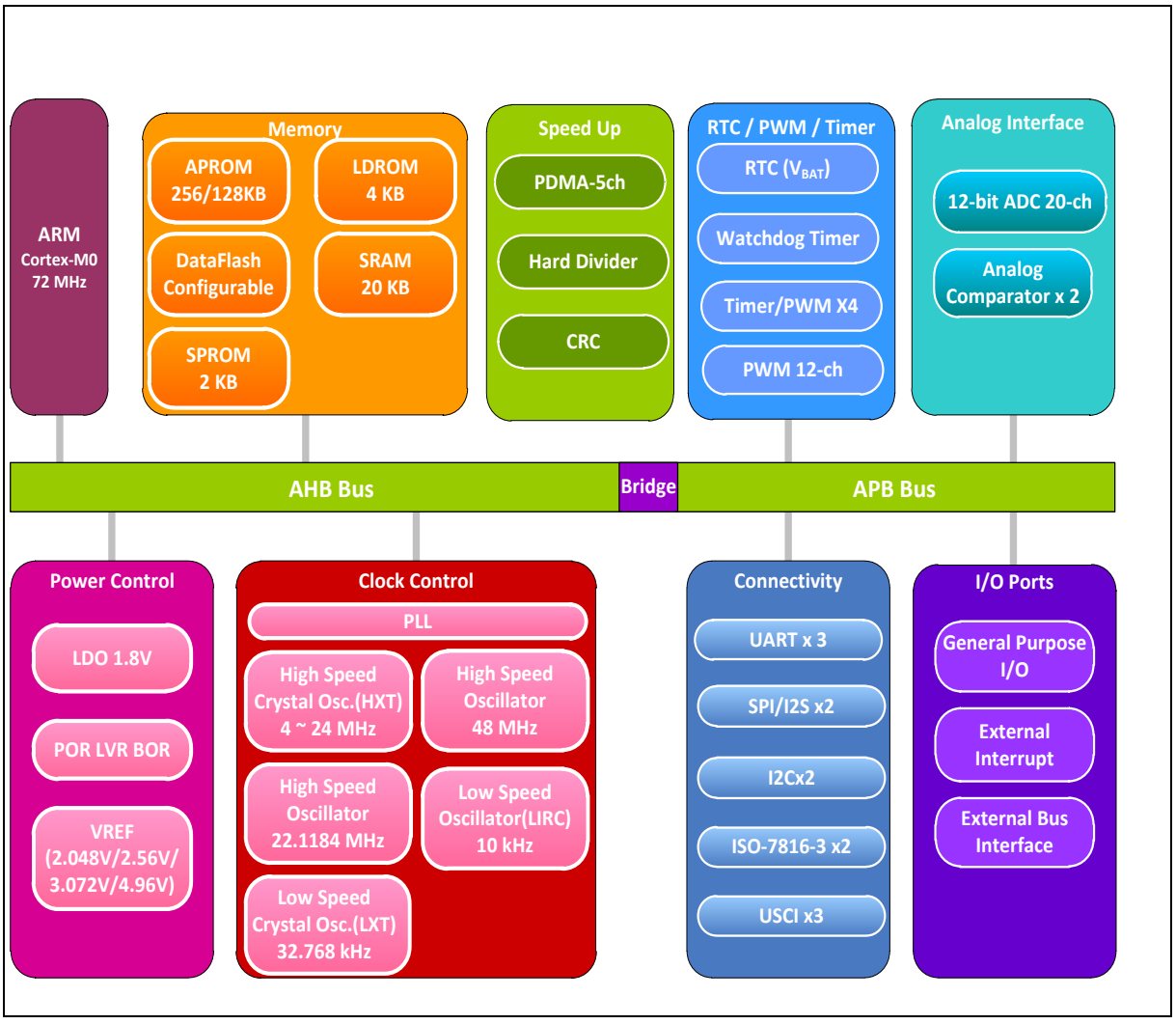


Figure 5.1-1 NuMicro® M0564 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6.1-1 shows the functional controller of processor.

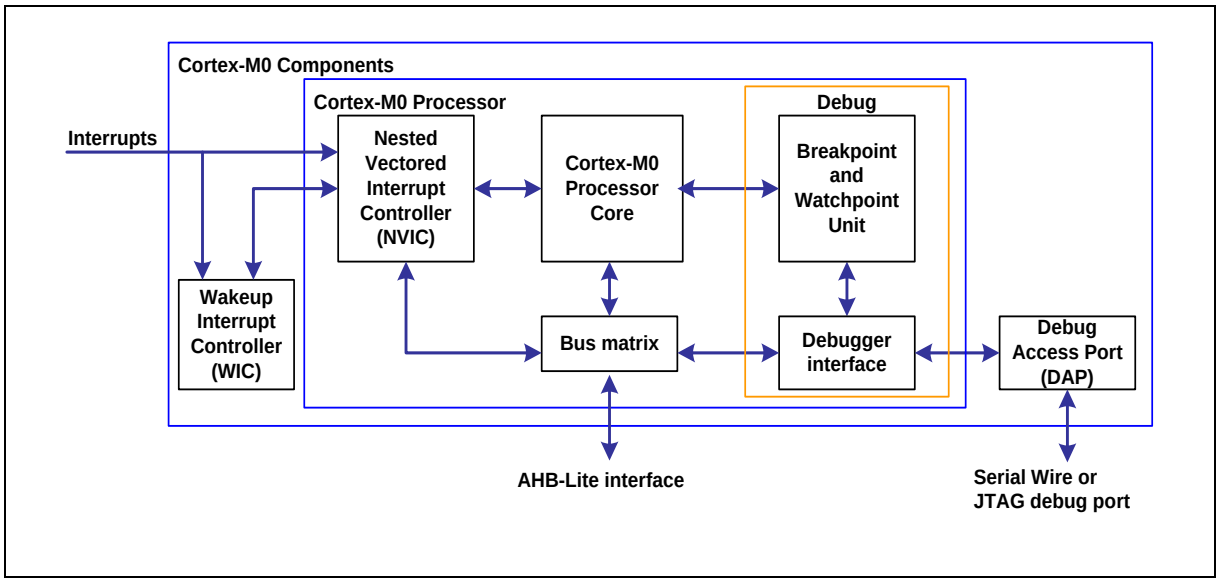


Figure 6.1-1 Functional Block Diagram

The implemented device provides:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature
- NVIC:

- 32 external interrupt inputs, each with four levels of priority
- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode

- Debug support:
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

The system manager provides the functions of system control, power modes, wake-up sources, reset sources, system memory map, product ID and multi-function pin control. The following sections describe the functions for

- System Reset
- Power Modes and Wake-up Sources
- System Power Distribution
- SRAM Memory organization
- System Control Register for Part Number ID, Chip Reset and Multi-function Pin Control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sourcces are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M0 core Only by writing 1 to CPURST (SYS_IPRST0[1])

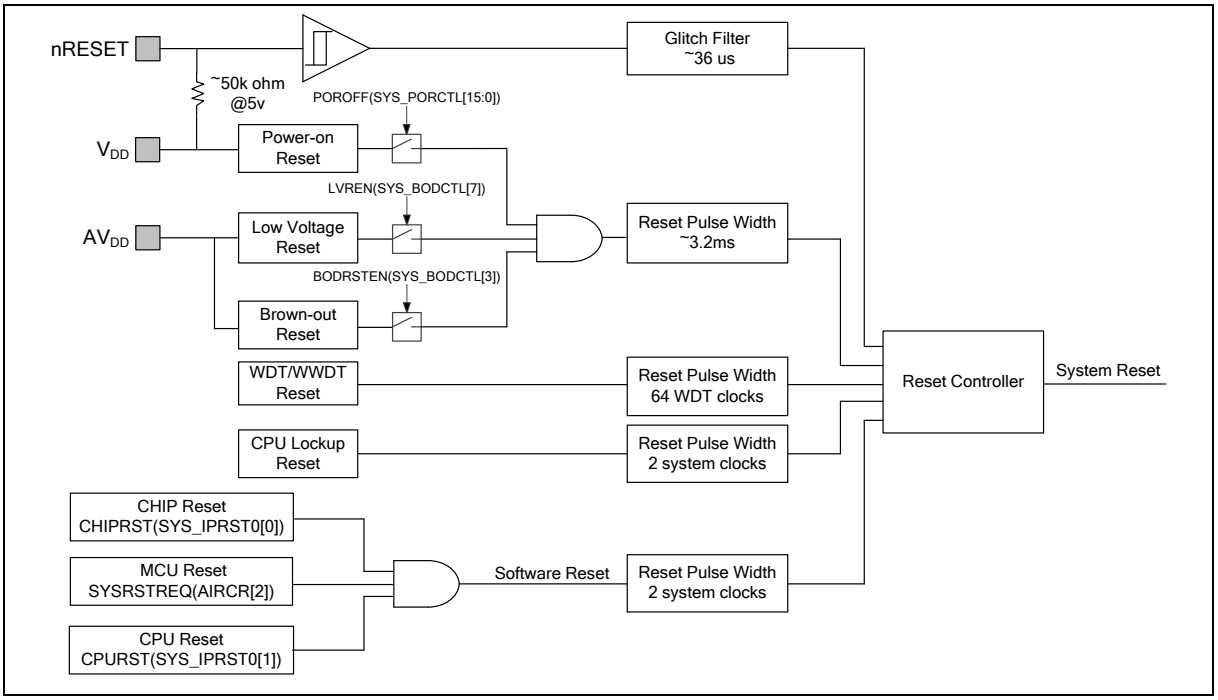


Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M0 only; the other reset sources will reset Cortex®-M0 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
SYS_RSTSTS	0x01	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[2:1])									
BODRSTEN (SYS_BODCTL[3])									
HXTEN (CLK_PWRCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
HCLKSEL (CLK_CLKSEL0[2:0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	-	-	-	-	-	-	-	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
PLLSTB (CLK_STATUS[2])	0x0	-	-	-	-	-	-	-	-
HIRCSTB (CLK_STATUS[4])	0x0	-	-	-	-	-	-	-	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDTEN (WDT_CTL[7])									
WDT_CTL except bit 1 and bit 7.	0x0700	0x0700	0x0700	0x0700	0x0700	-	0x0700	-	-

WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
BS (FMC_ISPCTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
BL (FMC_ISPCTL[16])									
FMC_DFBA	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	Reload from CONFIG1	-	-
CBS (FMC_ISPSTS[2:1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
VECMAP (FMC_ISPSTS[23:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value								-
FMC Registers	Reset Value								
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 36 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 36 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.

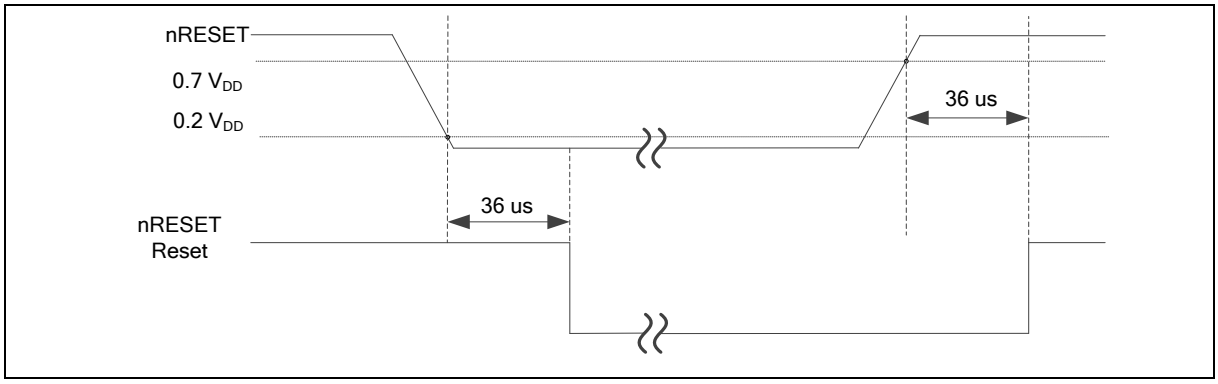


Figure 6.2-2 nRESET Reset Waveform

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the power-on reset waveform.

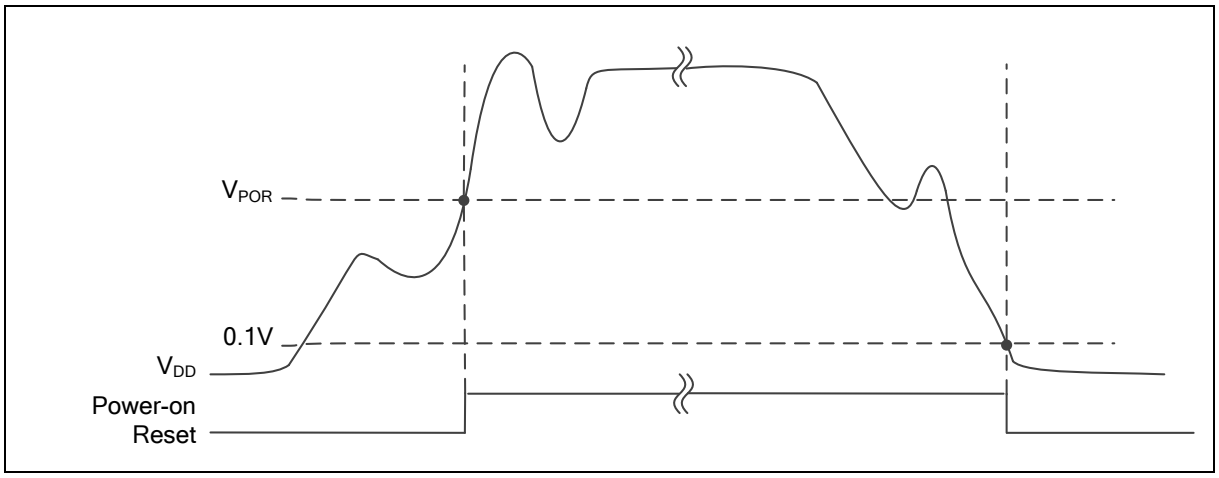


Figure 6.2-3 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-4 shows the Low Voltage Reset waveform.

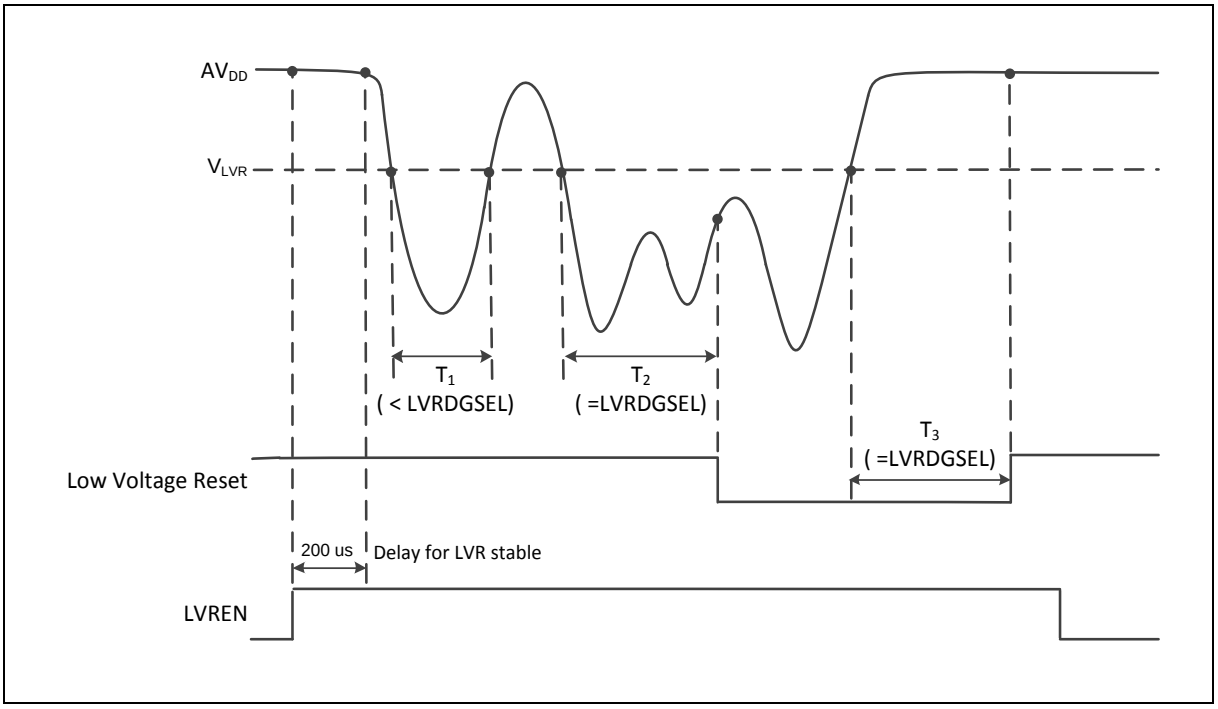


Figure 6.2-4 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN (SYS_BODCTL[0]) and BODVL (SYS_BODCTL[2:1]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]). The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by flash controller user configuration register CBODEN (CONFIG0 [23]), CBOV (CONFIG0 [22:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-out Detector waveform.

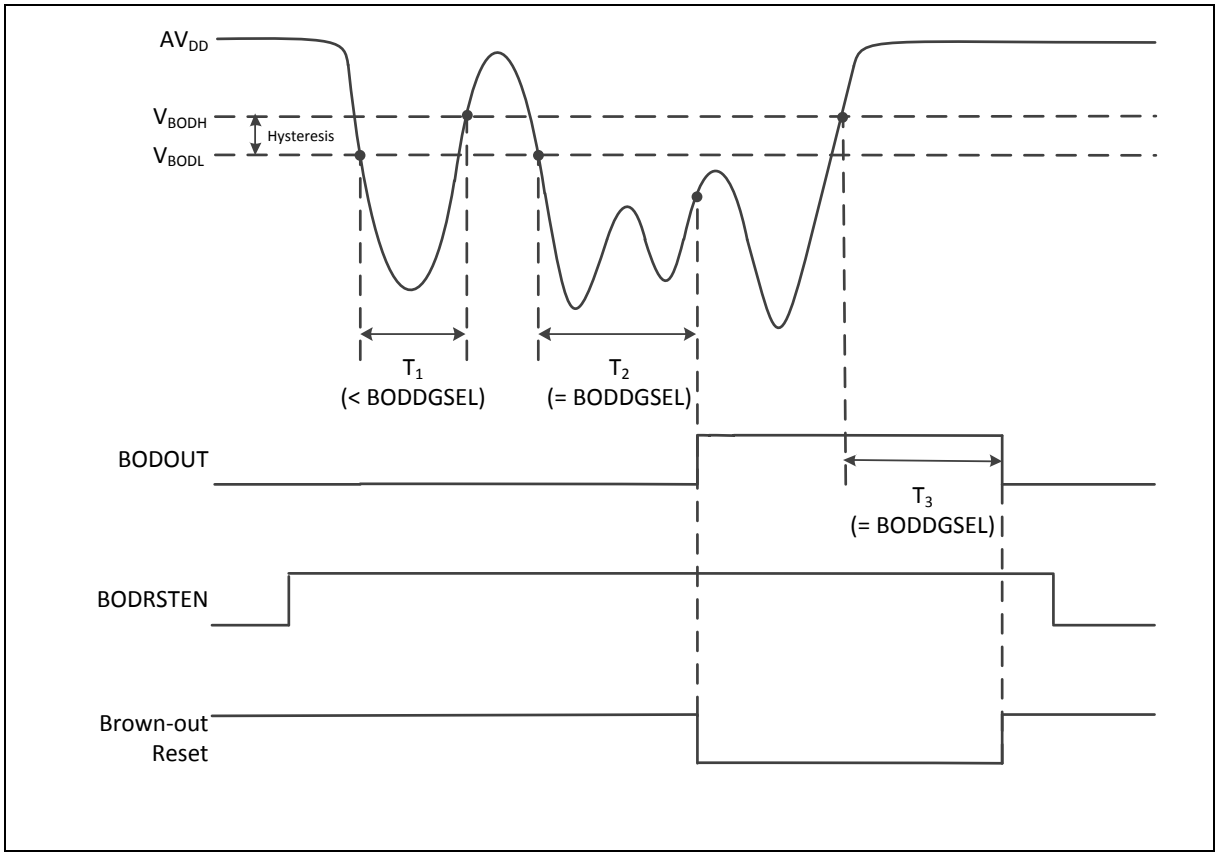


Figure 6.2-5 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M0 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[1]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 Power Modes and Wake-up Sources

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-2 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	RTC, WDT, I²C, Timer, UART, BOD, GPIO, EINT, USCI, ACMP and VDET.
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-2 Power Mode Difference Table

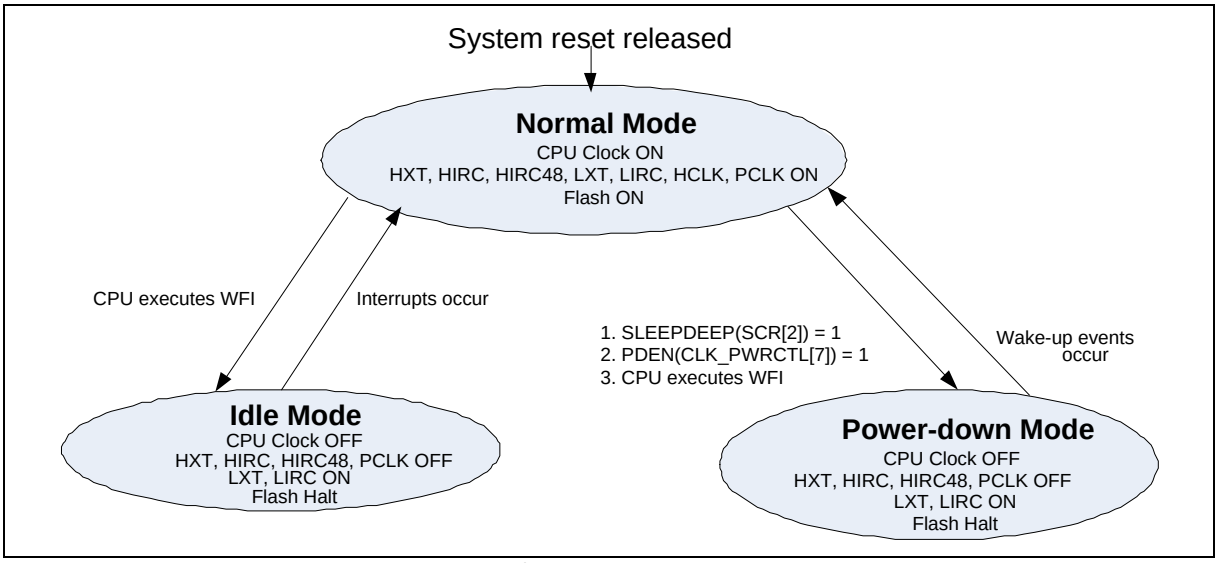


Figure 6.2-6 NuMicro® M0564 Power Mode State Machine

1. LXT (32768 Hz XTL) ON or OFF depends on SW setting in normal mode.
2. LIRC (10 kHz OSC) ON or OFF depends on S/W setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.
5. If RTC clock source is selected as LXT and LXT is on.
6. If UART clock source is selected as LXT and LXT is on.

	Normal Mode	Idle Mode	Power-Down Mode
HXT (4~20 MHz XTL)	ON	ON	Halt
HIRC (22.1184 MHz OSC)	ON	ON	Halt
HIRC48 (48 MHz OSC)	ON	ON	Halt
LXT (32768 Hz XTL)	ON	ON	ON/OFF[1]
LIRC (10 kHz OSC)	ON	ON	ON/OFF[2]
PLL	ON	ON	Halt
LDO	ON	ON	ON
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON	Halt
GPIO	ON	ON	Halt
PDMA	ON	ON	Halt
TIMER	ON	ON	ON/OFF[3]
PWM	ON	ON	Halt
WDT	ON	ON	ON/OFF[4]

WWDT	ON	ON	Halt
RTC	ON	ON	ON/OFF[5]
UART	ON	ON	ON/OFF[6]
SC	ON	ON	Halt
USCI	ON	ON	Halt
I^2C	ON	ON	Halt
SPI	ON	ON	Halt
ADC	ON	ON	Halt
ACMP	ON	ON	Halt

Table 6.2-3 Clocks in Power Modes

Wake-up sources in Power-down mode:

RTC, WDT, I²C, Timer, UART, USCI, BOD, VDET, GPIO, and ACMP.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-4 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	System Can Enter Power-Down Mode Again Condition*
BOD	Brown-Out Detector Interrupt	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
VDET	Voltage Detector Interrupt	After software writes 1 to clear VDETIF (SYS_BODCTL[19]).
GPIO	GPIO Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
TIMER	Timer Interrupt	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
WDT	WDT Interrupt	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
RTC	Alarm Interrupt	After software writes 1 to clear ALMIF (RTC_INTSTS[0]).
	Time Tick Interrupt	After software writes 1 to clear TICKIF (RTC_INTSTS[1]).
UART	nCTS wake-up	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
USCI UART	CTS Toggle	After software writes 1 to clear WKF (UUART_WKSTS[0]).
	Data Toggle	After software writes 1 to clear WKF (UUART_WKSTS[0]).
USCI I^2C	Data toggle	After software writes 1 to clear WKF (UI2C_WKSTS[0]).

	Address match	After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], then writes 1 to clear WKF (UI2C_WKSTS[0]).
USCI SPI	SS Toggle	After software writes 1 to clear WKF (USPI_WKSTS[0]).
I^2C	Address match wake-up	After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to clear WKIF(I2C_WKSTS[0]).
ACMP	Comparator Power-Down Wake-Up Interrupt	After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]).

Table 6.2-4 Condition of Entering Power-down Mode Again

6.2.4 System Power Distribution

In this chip, power distribution is divided into four segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation. The V_{REF} should be connected with an external 1uF capacitor that should be located close to the V_{REF} pin to avoid power noise for analog applications.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- RTC power from V_{BAT} provides the power for RTC.
- A dedicated power from V_{DDIO} supplies the power for PE.8 ~ PE.13.

The outputs of internal voltage regulators, LDO and VDD33, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 6.2-7 shows the power distribution of the M0564 series.

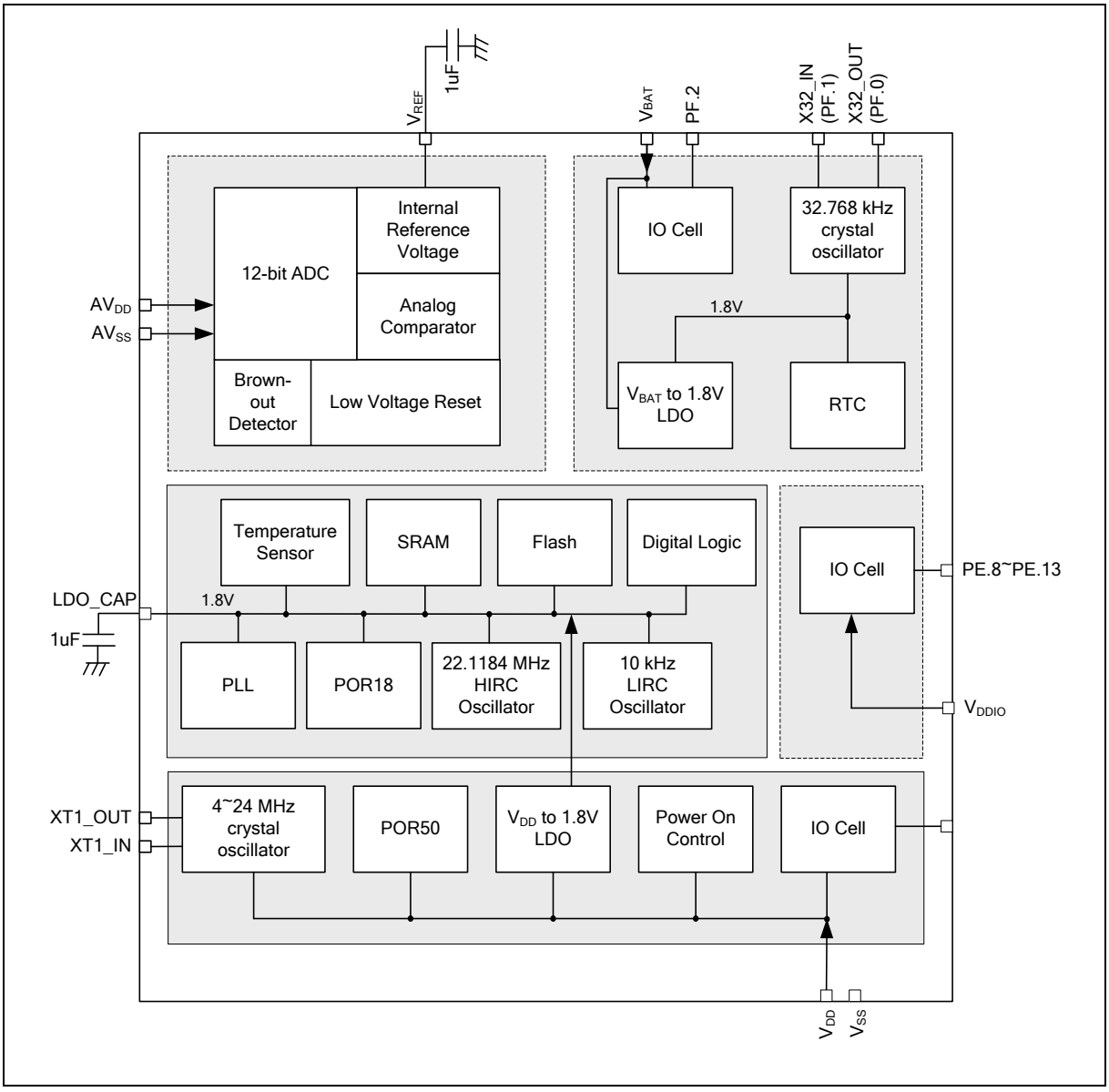


Figure 6.2-7 NuMicro® M0564 Power Distribution Diagram

6.2.5 System Memory Map

The M0564 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-5. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The M0564 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128 KB)
0x0000_0000 – 0x0003_FFFF	FLASH_BA	FLASH Memory Space (256 KB)
0x0004_0000 – 0x0005_FFFF	Reserved	Reserved
0x0006_0000 – 0x0007_FFFF	Reserved	Reserved
0x2000_0000 – 0x2000_4FFF	SRAM_BA	SRAM Memory Space (20 KB)
0x2000_4000 – 0x2000_BFFF	Reserved	Reserved
0x2000_C000 – 0x2000_FFFF	Reserved	Reserved
0x6000_0000 – 0x601F_FFFF	EXTMEM_BA	External Memory Space for EBI Interface (2 MB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	SYS_BA	System Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_BA	EBI Control Registers
0x5001_4000 – 0x5001_7FFF	HDIV_BA	Hardware Divider Registers
0x5001_8000 – 0x5001_FFFF	CRC_BA	CRC Generator Registers
Peripheral Controllers Space (0x4000_0000 – 0x401F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWM0_BA	PWM0 Control Registers
0x4004_4000 – 0x4004_7FFF	Reserved	Reserved
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	Reserved	Reserved
0x4007_0000 – 0x4007_3FFF	USCI0_BA	USCI0 Control Registers

0x4007_4000 – 0x4007_7FFF	USCI2_BA	USCI2 Control Registers
0x400D_0000 – 0x400D_3FFF	ACMP01_BA	Analog Comparator Control Registers
0x400D_4000 – 0x400D_7FFF	Reserved	Reserved
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
0x4010_0000 – 0x4010_3FFF	Reserved	Reserved
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4014_0000 – 0x4014_3FFF	PWM1_BA	PWM1 Control Registers
0x4014_4000 – 0x4014_7FFF	Reserved	Reserved
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_7FFF	UART2_BA	UART2 Control Registers
0x4017_0000 – 0x4017_3FFF	USCI1_BA	USCI1 Control Registers
0x4017_4000 – 0x4017_7FFF	Reserved	Reserved
0x4019_0000 – 0x4019_3FFF	SC0_BA	SC0 Control Registers
0x4019_4000 – 0x4019_7FFF	SC1_BA	SC1 Control Registers
0x401A_0000 – 0x401A_3FFF	Reserved	Reserved
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-5 Address Space Assignments for On-Chip Controllers

6.2.6 SRAM Memory Orginization

The M0564 supports embedded SRAM with total 20 Kbytes size in one bank.

- Supports total 20 Kbytes SRAM
- Supports byte / half word / word write
- Supports oversize response error

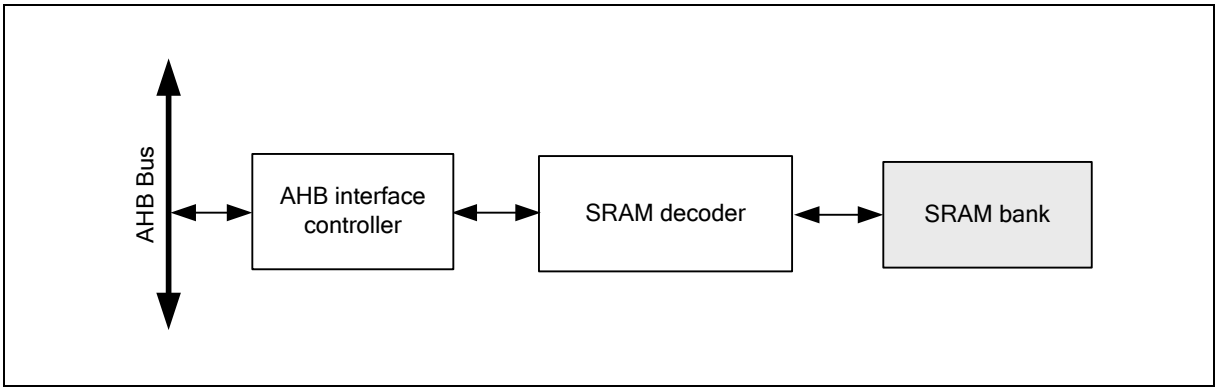


Figure 6.2-8 SRAM Block Diagram

Figure 6.2-9 shows the SRAM organization of M0564. There is one SRAM bank in the M0564 and addressed to 20 Kbytes. The address space is from 0x2000_0000 to 0x2000_4FFF. The address between 0x2000_5000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

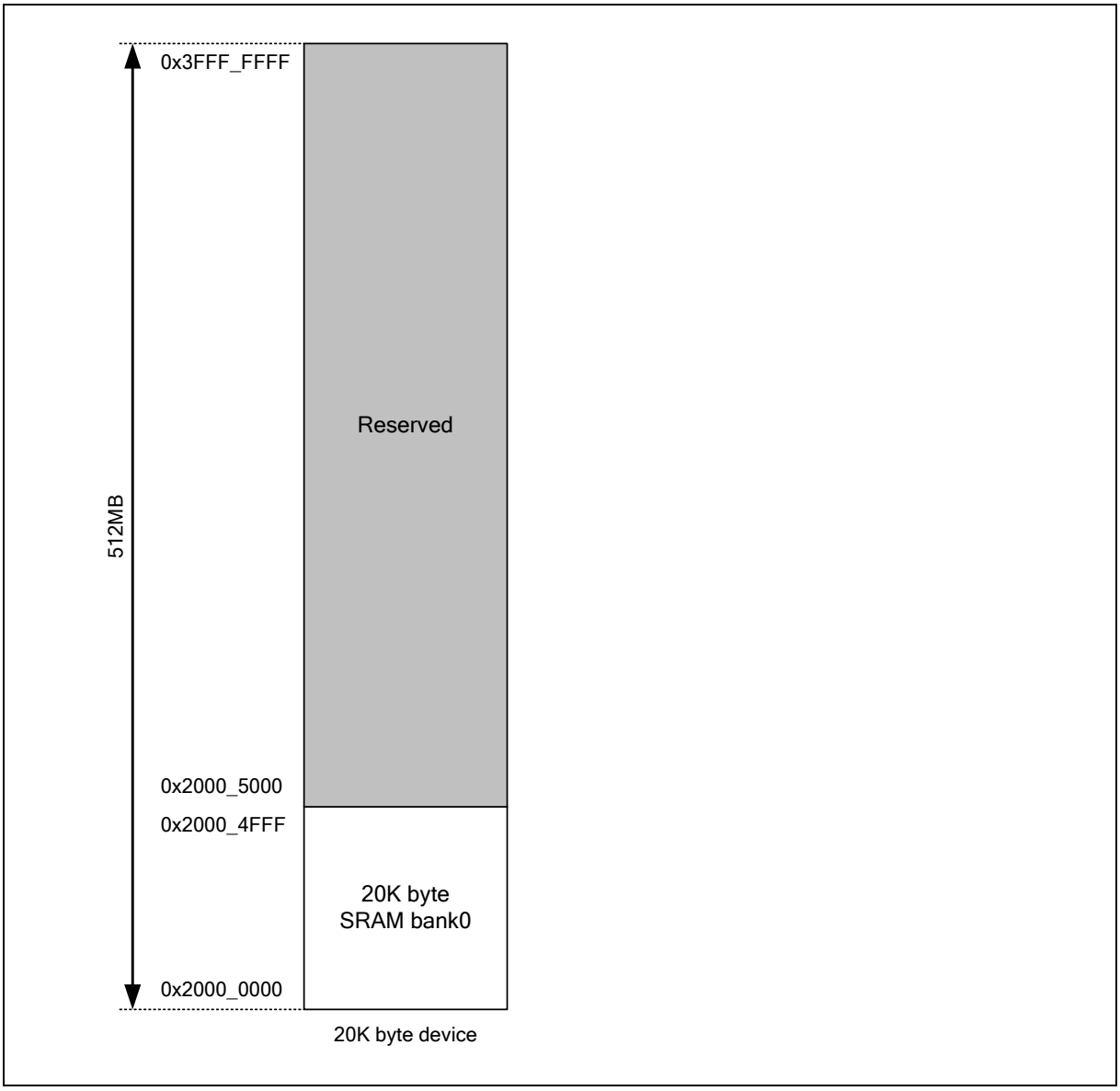


Figure 6.2-9 SRAM Memory Organization

6.2.7 Register Lock

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x5000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

After the protection is disabled, user can check the protection disable bit at address 0x5000_0100 bit0, 1 is protection disable, and 0 is protection enable. Then user can update the target protected register value and then write any data to the address “0x5000_0100” to enable register protection.

6.2.8 Auto Trim

This chip supports auto-trim function: the HIRC trim (48 MHz and 22.1184 MHz RC oscillator),

according to the accurate LXT (32.768 kHz crystal oscillator), automatically gets accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 22.1184 MHz clock. In such case, if users do not want to use PLL as the system clock source, they need to solder 32.768 kHz crystal in system, and set FREQSEL (SYS_IRCTCTL0[1:0] trim frequency selection) to “01”, set REFCKSEL (SYS_IRCTCTL0[9] reference clock selection) to “0”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[0] HIRC frequency lock status) “1” indicates the HIRC0 output frequency is accurate within 0.25% deviation. To get better results, it is recommended to set both LOOPSEL (SYS_IRCTCTL[5:4] trim calculation loop) and RETRYCNT (SYS_IRCTCTL[7:6] trim value update limitation count) to “11”.

6.2.9 UART1_TXD modulation with PWM

This chip supports UART1_TXD to modulate with PWM channel. User can set MODPWMSEL(SYS_MODCTL[6:4]) to choice which PWM0 channel to modulate with UART1_TXD and set MODEN(SYS_MODCTL[0]) to enable modulation function. User can set TXDINV(UART_LINE[8]) to inverse UART1_TXD before moulating with PWM.

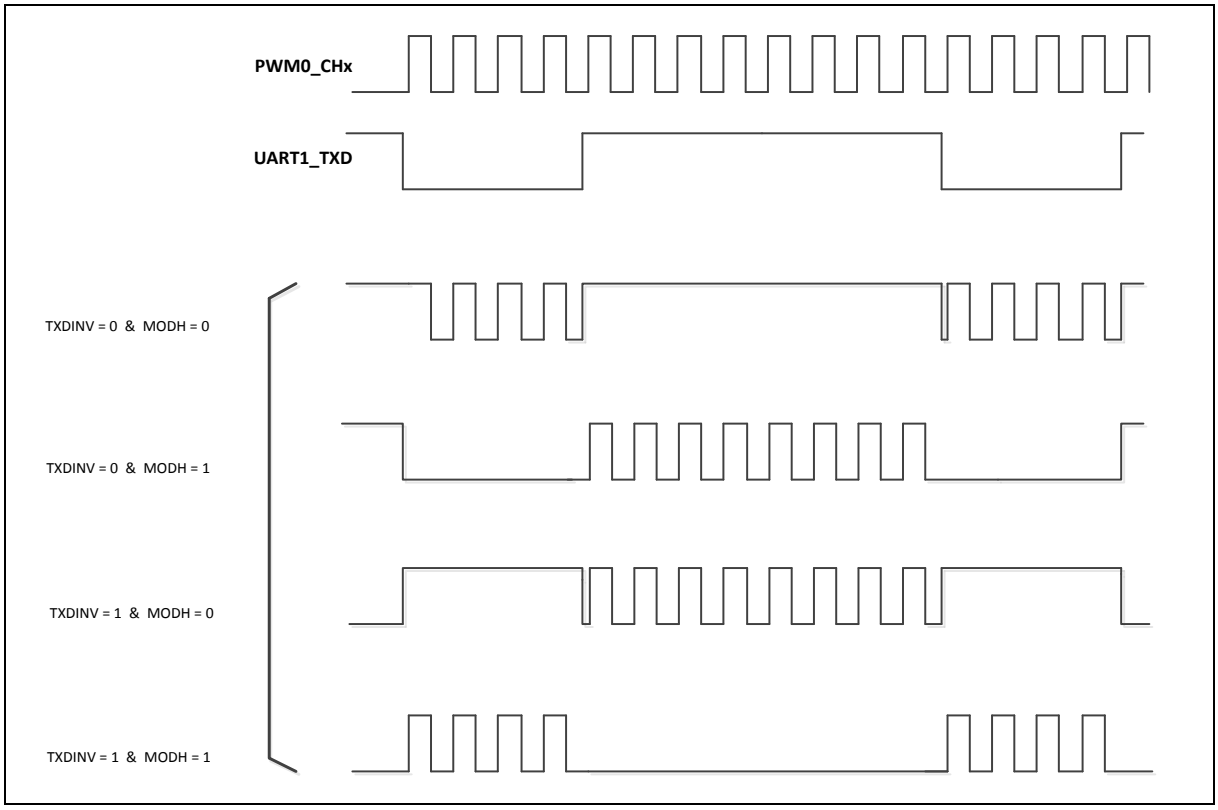


Figure 6.2-10 UART1_TXD Modulated with PWM Channel

6.2.10 Voltage Detector (VDET)

This chip supports low power comparator to detect external voltage. User can control Bandgap active interval and comparator active interval to achieve low power detection purpose. There is no debounce function in Power-down mode since no HCLK available in Power-down mode.

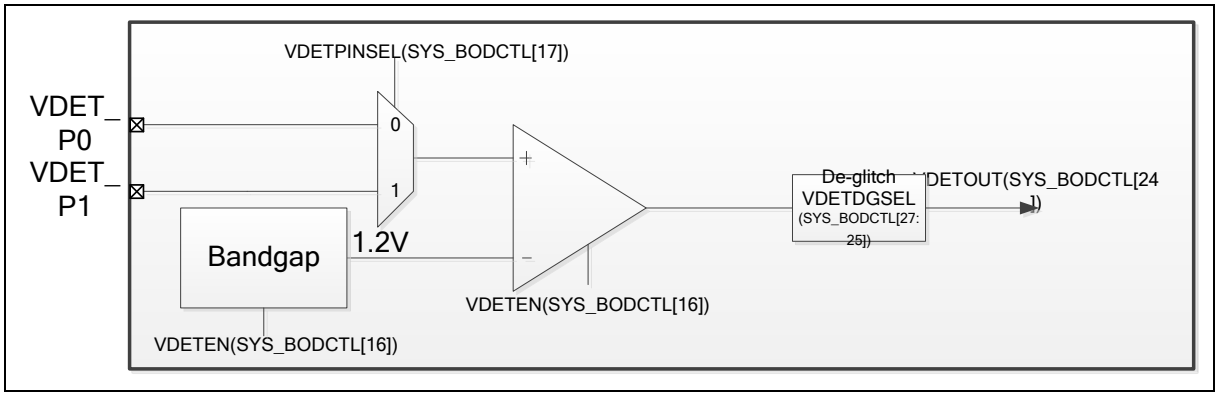


Figure 6.2-11 VDET Block Diagram

6.2.11 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.2.12 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as “Nested Vectored Interrupt Controller (NVIC)”, which is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in “Handler Mode”. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one’s priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers “PC, PSR, LR, R0~R3, R12” to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports “Tail Chaining” which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports “Late Arrival” which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.2.12.1 Exception Model and System Interrupt Map

Table 6.2-6 lists the exception model supported by the M0564 series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Type	Vector Number	Vector Address	Priority
Reset	1	0x00000004	-3
NMI	2	0x00000008	-2
Hard Fault	3	0x0000000C	-1
Reserved	4 ~ 10		Reserved
SVCall	11	0x0000002C	Configurable
Reserved	12 ~ 13		Reserved
PendSV	14	0x00000038	Configurable
SysTick	15	0x0000003C	Configurable
Interrupt (IRQ0 ~ IRQ)	16 ~ 47	0x00000000 + (Vector Number)*4	Configurable

Table 6.2-6 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BOD_INT	Brown-out low voltage detected interrupt
17	1	WDT_INT	Window Watchdog Timer interrupt
18	2	EINT024	External interrupt from PA.0/PC.0/PD.2/PE.0/PE.4 pin
19	3	EINT135	External interrupt from PB.0/PC.0/ PD.0/PD.3/PE.5/PF.0 pin
20	4	GPAB_INT	External signal interrupt from PA[15:0]/PB[13:0]
21	5	GPCDEF_INT	External interrupt from PC[15:0]/PD[15:0]/PE[13:0]/PF[7:0]
22	6	PWM0_INT	PWM0 interrupt
23	7	PWM1_INT	PWM1 interrupt
24	8	TMR0_INT	Timer 0 interrupt
25	9	TMR1_INT	Timer 1 interrupt
26	10	TMR2_INT	Timer 2 interrupt
27	11	TMR3_INT	Timer 3 interrupt
28	12	UART02_INT	UART0 and UART2 interrupt
29	13	UART1_INT	UART1 interrupt
30	14	SPI0_INT	SPI0 interrupt
31	15	SPI1_INT	SPI1 interrupt
32	16		Reserved
33	17		Reserved

34	18	I2C0_INT	I^2C0 interrupt
35	19	I2C1_INT	I^2C1 interrupt
36	20		Reserved
37	21		Reserved
38	22	USCI_INT	USCI0, USCI1 and USCI2 interrupt
39	23		Reserved
40	24	SC_INT	SC0 and SC1 interrupt
41	25	ACMP01_INT	Analog Comparator interrupt
42	26	PDMA_INT	PDMA interrupt
43	27		Reserved
44	28	PWRWU_INT	Clock controller interrupt for chip wake-up from Power-down state
45	29	ADC_INT	ADC interrupt
46	30	CLKDIRC_INT	Clock fail detect and IRC TRIM interrupt
47	31	RTC_INT	Real Time Clock interrupt

Table 6.2-7 Interrupt Number Table

6.2.12.2 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.2.13 System Control

The Cortex®-M0 status and operating mode control are managed by System Control Registers. Including CPUID, Cortex®-M0 interrupt priority and Cortex®-M0 power management can be controlled through these system control registers.

For more detailed information, please refer to the "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M0 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT), internal 22.1184 MHz internal high speed RC oscillator (HIRC) and 48 MHz internal high speed RC oscillator (HIRC48) to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.

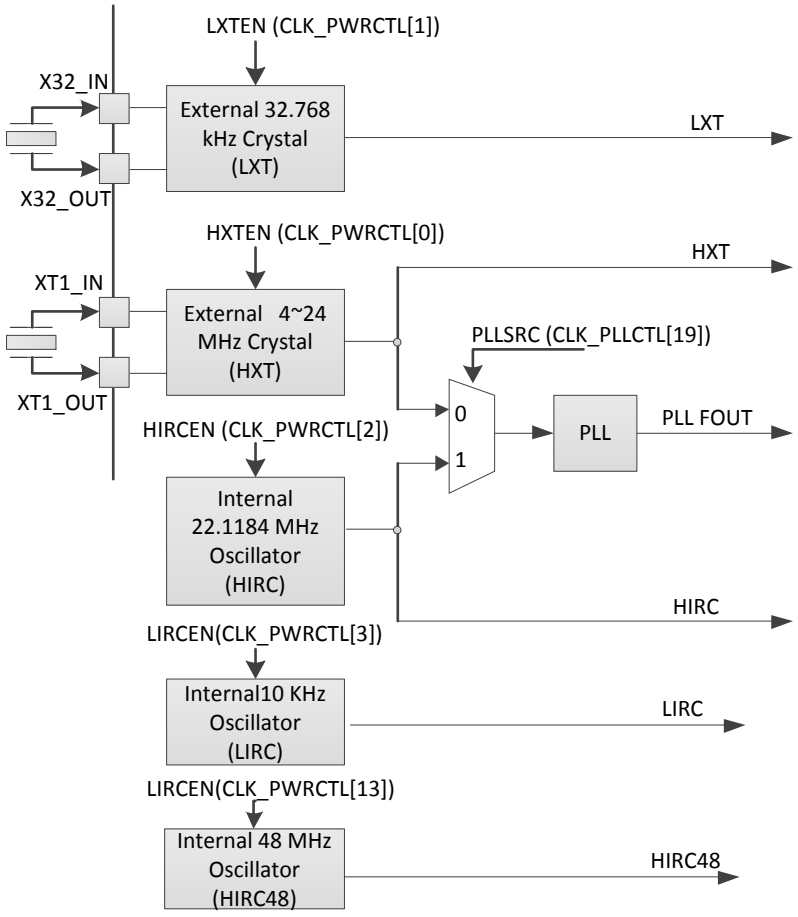
The clock generator consists of 6 clock sources, which are listed below:

- 32.768 kHz external low-speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 22.1184 MHz internal high speed oscillator (HIRC)
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 48 MHz internal high speed RC oscillator (HIRC48)
- 10 kHz internal low speed RC oscillator (LIRC)

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter start counting and correlated clock stable index (HIRCSTB(CLK_STATUS[4]), LIRCSTB(CLK_STATUS[3]), PLLSTB(CLK_STATUS[2]), HXTSTB(CLK_STATUS[0]), LXTSTB(CLK_STATUS[1]) and HIRC48STB(CLK_STATUS[5])) are set to 1 after stable counter value reach a define value as shown in Table 6.3-8. System and peripheral can use the clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index will auto clear when user disables the clock source (LIRCEN(CLK_PWRCTL[3]), HIRCEN(CLK_PWRCTL[2]), HXTEN(CLK_PWRCTL[0]), PD(CLK_PLLCTL[16]), LXTEN(CLK_PWRCTL[1]) and HIRC48EN(CLK_PWRCTL[13])). Besides, the clock stable index of HXT, HIRC and PLL will auto clear when chip enter power-down and clock stable counter will re-counting after chip wake-up if correlate clock is enabled.

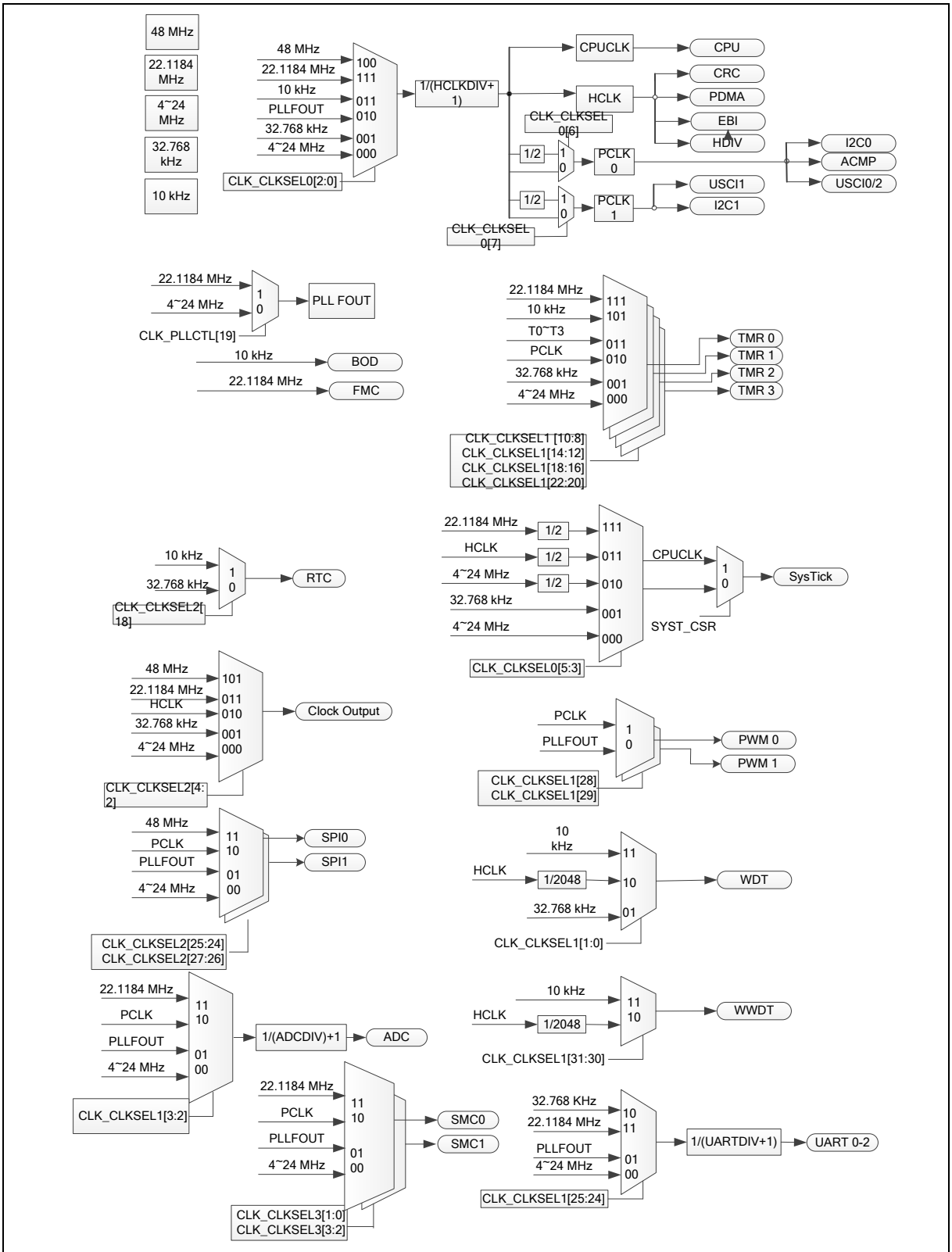
Clock Source	Clock Stable Count Value	Clock Stable Time
HXT	4096 HXT clock	341.33 uS for 12 Mhz
PLL	It's based on the value of STBSEL (CLK_PLLCTL[23]) STBSEL = 0, stable count is 6144 clocks of PLL clock source. STBSEL = 1, stable count is 12288 clocks of PLL clock source. (Default)	STBSEL = 0, 512 uS for 512 Mhz STBSEL = 1, 1024 uS for 12 Mhz
HIRC48	512 HIRC48 clock	10.67 uS for 48 Mhz
HIRC	256 HIRC clock	11.574 uS for 22.1184 Mhz
LIRC	1 LIRC clock	100 uS for 10 kHz
LXT	1 LXT clock	30.51 uS for 32.768 khz

Table 6.3-8 Clock Stable Count Value Table



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-1 Clock Generator Block Diagram



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-2 Clock Generator Global View Diagram

6.3.2 System Clock and SysTick Clock

The system clock has 6 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0 [2:0]). The block diagram is shown in Figure 6.3-3.

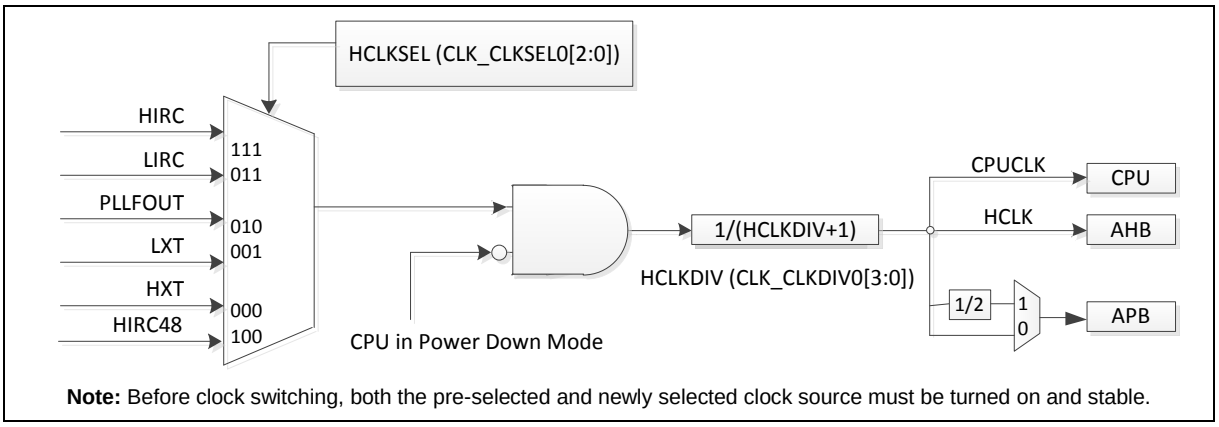


Figure 6.3-3 System Clock Block Diagram

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIEN (CLK_CLKDCTL[5]) is set to 1. User can trying to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

The HXT clock stop detect and system clock switch to HIRC procedure is shown in Figure 6.3-4.

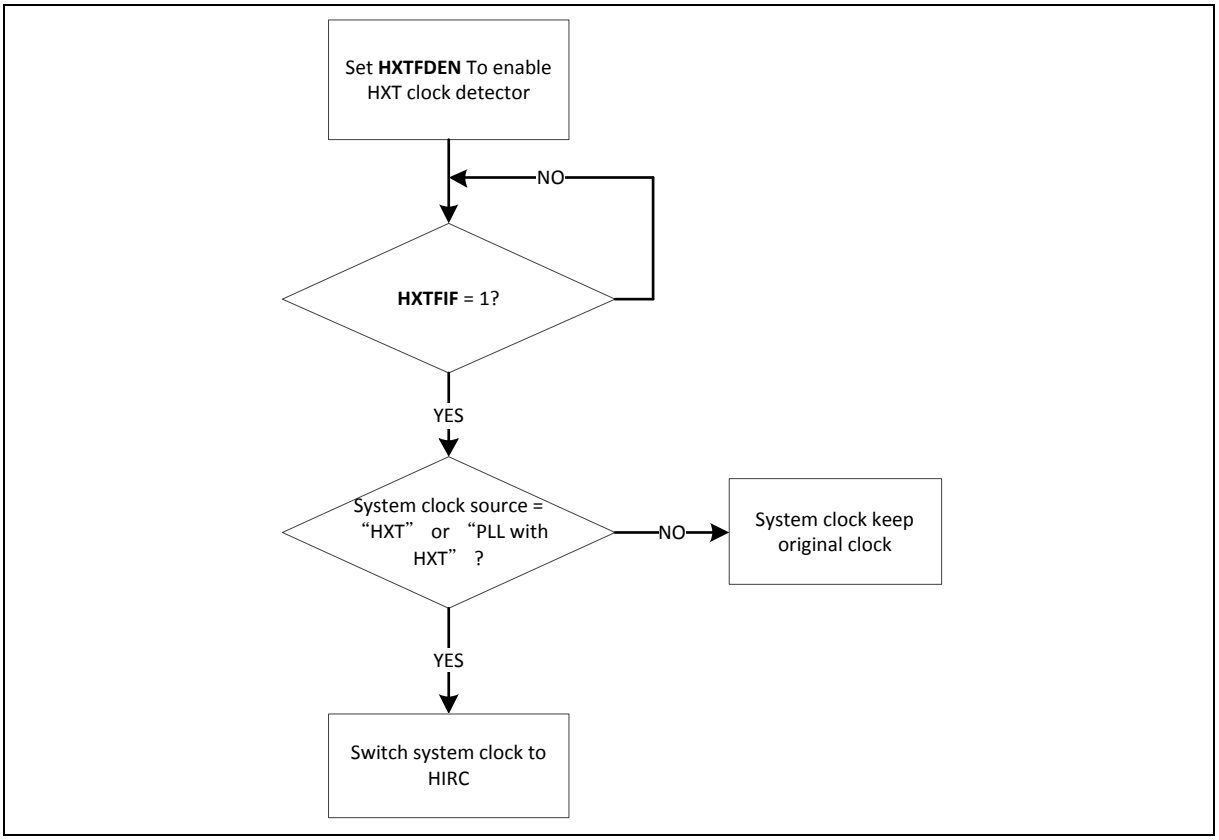
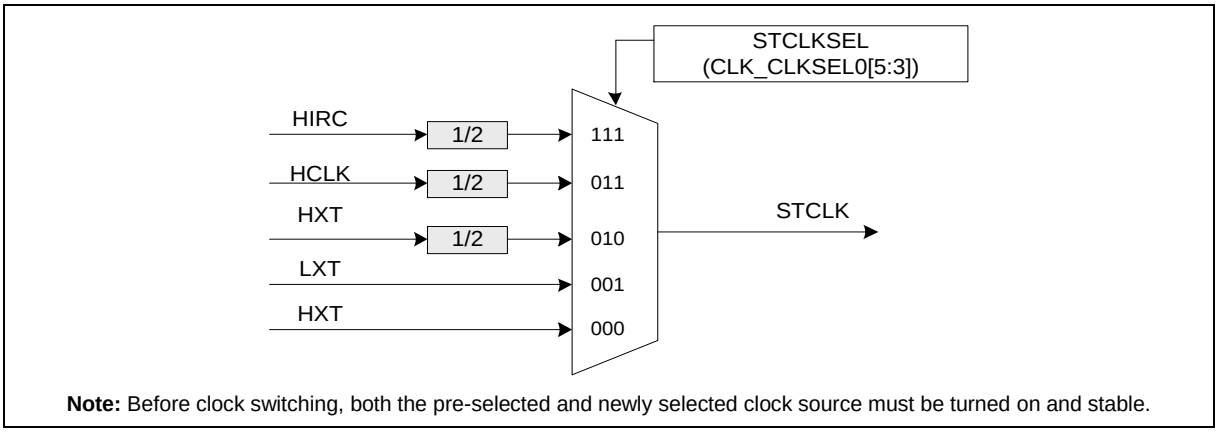


Figure 6.3-4 HXT Stop Protect Procedure

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-5 SysTick Clock Control Block Diagram

6.3.3 Peripherals Clock

The peripherals clock had different clock source switch setting, which depends on the different peripheral. Please refer to the CLK_CLKSEL1, CLK_CLKSEL2 and CLK_CLKSEL3 register description in section 6.3.7.

6.3.4 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources, and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For theses clocks, which still keep active, are listed below:

- Clock Generator
  - 10 kHz internal low-speed RC oscillator (LIRC) clock
  - 32.768 kHz external low-speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

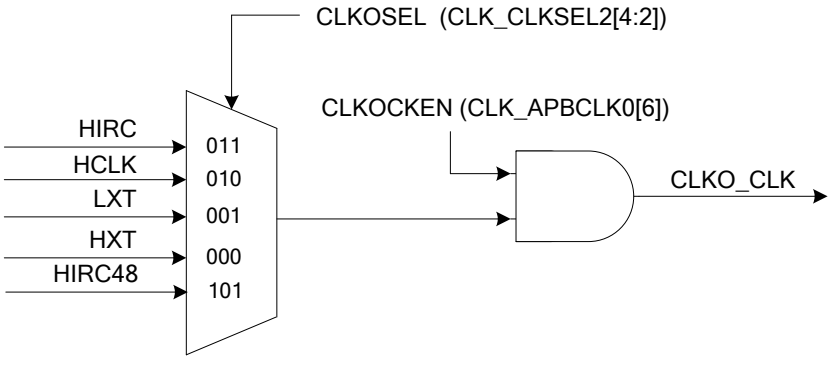
6.3.5 Clock Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^{1}$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

if DIVI1EN(CLK_CLKOCTL[5]) set to 1, the clock output clock (CLKO_CLK) will bypass power-of-2 frequency divider. The clock output clock will be output to CLKO pin directly.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-6 Clock Source of Clock Output

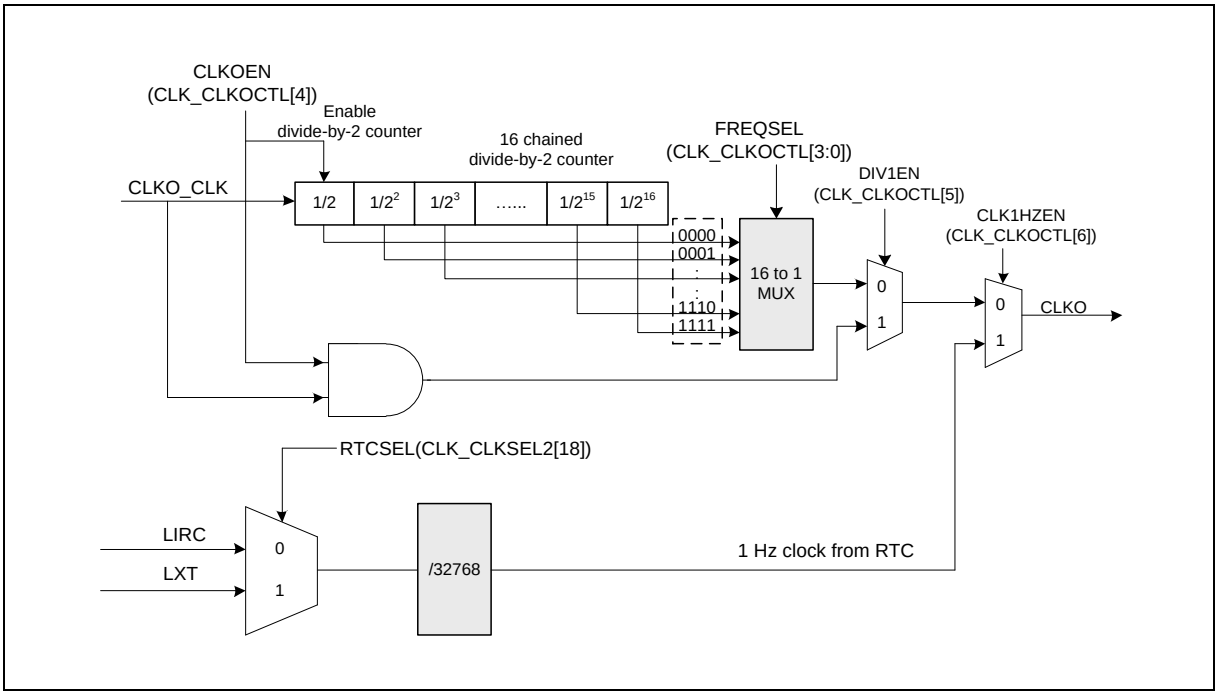


Figure 6.3-7 Clock Output Block Diagram

6.4 Flash Memeory Controller (FMC)

6.4.1 Overview

The M0564 series is equipped with 128/256 Kbytes on-chip embedded flash for application and configurable Data Flash to store some application dependent data. A User Configuration block provides for system initiation. A 4 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. A 2 Kbytes security protection ROM (SPROM) can conceal user program. A 4KB cache with zero wait cycle is used to improve flash access performance. This chip also supports In-Application-Programming (IAP) function, user switches the code executing without the chip reset after the embedded flash updated.

6.4.2 Features

- Supports 128/256 Kbytes application ROM (APROM).
- Supports 4 Kbytes loader ROM (LDROM).
- Supports 2 Kbytes security protection ROM (SPROM) to conceal user program.
- Supports Data Flash with configurable memory size.
- Supports 12 bytes User Configuration block to control system initiation.
- Supports 2 Kbytes page erase for all embedded flash.
- Supports 32-bit/64-bit and multi-word flash programming function.
- Supports CRC-32 checksum calculation function.
- Supports flash all one verification function.
- Supports embedded SRAM remap to system vector memory.
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded flash memory.
- Supports cache memory to improve flash access performance and reduce power consumption.

6.5 Analog Comparator Controller (ACMP)

6.5.1 Overview

M0564 contains two analog comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output state changes.

6.5.2 Features

- Analog input voltage range: 0 ~ V_{DDA} (voltage of AV_{DD} pin)
- Supports hysteresis function
- Supports wake-up function
- Selectable input sources of positive input and negative input
- ACMP0 supports
  - 4 positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2, or ACMP0_P3
  - 3 negative sources:
    - ACMP0_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (V_{BG})
- ACMP1 supports
  - 4 positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP1_P2, or ACMP1_P3
  - 3 negative sources
    - ACMP1_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (V_{BG})
- Shares one ACMP interrupt vector for all comparators
- Supports window Latch mode
- Supports window compare mode

6.6 Analog-to-Digital Converter (ADC)

6.6.1 Overview

The M0564 series contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with twenty input channels. The A/D converter supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin (STADC/PD.2), timer0~3 overflow pulse trigger and PWM trigger.

6.6.2 Features

- Analog input voltage range: 0 ~ AV_{DD}.
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 20 single-end analog input channels or 10 differential analog input channels
- Maximum ADC peripheral clock frequency is 16 MHz
- Up to 800k SPS sampling rate
- Configurable ADC internal sampling time
- Four operation modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software Write 1 to ADST bit
  - External pin (STADC)
  - Timer 0~3 overflow pulse trigger
  - PWM trigger with optional start delay period
- Each conversion result is held in data register of each channel with valid and overrun indicators.
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- 3 internal channels, they are band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}), and Battery power (V_{BAT})
- Support PDMA transfer mode.

Note1: ADC sampling rate = (ADC peripheral clock frequency) / (total ADC conversion cycle)

Note2: If the internal channel (V_{TEMP}) is selected to convert, the sampling rate needs to be less than 300k SPS for accurate result.

Note3: If the internal channel for band-gap voltage is active, the maximum sampling rate will be 300k SPS.

6.7 CRC Controller (CRC)

6.7.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

6.7.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to program DATA (CRC_DAT[31:0]) to perform CRC operation

6.8 External Bus Interface (EBI)

6.8.1 Overview

The M0564 series is equipped with an external bus interface (EBI) for external device used. To save the connections between external device and the M0564, EBI operating at address bus and data bus multiplex mode. The EBI supports two chip selects that can connect two external devices with different timing setting requirement.

6.8.2 Features

- Supports address bus and data bus multiplex mode to save the address pins
- Supports two chip selects with polarity control
- Supports external devices with maximum 1 MB size for each chip select
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports 8-bit or 16-bit data width for each chip select
- Supports variable address latch enable time (tALE)
- Supports variable data access time (tACC) and data access hold time (tAHD) for each chip select
- Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R)
- Supports continuous data access mode to bypass tASU, tALE and tLHD cycles for improving EBI access

6.9 General Purpose I/O (GPIO)

6.9.1 Overview

The M0564 series has up to 86 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 86 pins are arranged in 6 ports named as PA, PB, PC, PD, PE and PF. PA, PB, PC, PD has 16 pins on port. PE has 14 pins on port. PF has 8 pins on port. Each of the 86 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOIN (CONFIG0[10]). Each I/O pin has a very weakly individual pull-up resistor which is about 110 kΩ ~ 300 kΩ for V_{DD} is from 5.0 V to 2.5 V.

6.9.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOIN = 0, all GPIO pins in input tri-state mode after chip reset
  - CIOIN = 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the wake-up function

6.10 Hardware Divider (HDIV)

6.10.1 Overview

The hardware divider (HDIV) is useful to the high performance application. The hardware divider is a signed, integer divider with both quotient and remainder outputs.

6.10.2 Features

- Signed (two's complement) integer calculation
- 32-bit dividend with 16-bit divisor calculation capacity
- 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
- Divided by zero warning flag
- 6 HCLK clocks taken for one cycle calculation
- Write divisor to trigger calculation
- Waiting for calculation ready automatically when reading quotient and remainder

6.11 I²C Serial Interface Controller (I²C)

6.11.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I²C controllers which support Power-down wake-up function.

6.11.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports two-level buffer function
- Supports setup/hold time programmable

6.12 PDMA Controller (PDMA)

6.12.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 5 channels and each channel can perform transfer between memory and peripherals or between memory and memory. The PDMA supports time-out function for channel 0 and channel 1.

6.12.2 Features

- Supports 5 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and SPI, UART, I^2S, I^2C, ADC, PWM and TIMER request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function for channel0 and channel 1

6.13 PWM Generator and Capture Timer (PWM)

6.13.1 Overview

The M0564 provides two PWM generator: PWM0 and PWM1. Each PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM uses comparator compared with counter to generate events. These events use to generate PWM pulse, interrupt and trigger signal for ADC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various PWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for ADC. For PWM output control unit, it supports polarity output, independent pin mask and brake functions.

The PWM generator also supports input capture function. It supports latch PWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

6.13.2 Features

6.13.2.1 PWM function features

- Supports maximum clock frequency up to144MHz
- Supports up to two PWM modules, each module provides 6 output channels.
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channels:
  - Dead-time insertion with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution PWM counter
  - Up, down and up-down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each PWM output pin
- Supports brake function
  - Brake source from pin, analog comparator, ADC result monitor and system safety events (clock failed, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared

  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM zero point, period point, up-count compared or down-count compared point events
  - Brake condition happened
- Supports trigger ADC on the following events:
  - PWM zero point, period point, zero or period point, up-count compared point, down-count compared point events
  - PWM up-count free trigger compared point, down-count free trigger compared point events

6.13.2.2 Capture Function Features

- Supports up to 6 capture input channels with 16-bit resolution for each PWM module
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for PWM all channels

6.14 Real Time Clock (RTC)

6.14.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

6.14.2 Features

- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register
-
- Supports Leap Year indication in RTC_LEAPYEAR register
- Supports Day of the Week counter in RTC_WEEKDAY register
- Frequency of RTC clock source compensate by RTC_FREQADJ register
- All time and calendar message expressed in BCD format
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports RTC Time Tick and Alarm Match interrupt
- Supports chip wake-up from Idle or Power-down mode while an RTC interrupt signal is generated
- Supports Daylight Saving Time backup control in RTC_DSTCTL

6.15 Smart Card Host Interface (SC)

6.15.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

6.15.2 Features

- ISO-7816-3 T = 0, T = 1 compliant
- EMV2000 compliant
- Two ISO-7816-3 ports
- Separates receive/transmit 4 byte entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 267 ETU)
- One 24-bit timer and two 8-bit timers for Answer to Request (ATR) and waiting times processing
- Supports auto direct / inverse convention function
- Supports transmitter and receiver error retry and error number limiting function
- Supports hardware activation sequence process, and the interval between PWR on and CLK start is configurable
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detected the card removal
- Supports UART mode
  - Full duplex, asynchronous communications
  - Separates receiving/transmitting 4 bytes entry FIFO for data payloads
  - Supports programmable baud rate generator
  - Supports programmable receiver buffer trigger level
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting EGT (SC_EGT[7:0])
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1- or 2- stop bit generation

6.16 Serial Peripheral Interface (SPI)

6.16.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The M0564 series contains up to two sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device.

This controller also supports the PDMA function to access the data buffer. The SPI controller also support I^2S mode to connect external audio CODEC.

6.16.2 Features

- SPI Mode
  - Up to two sets of SPI controllers
  - Supports Master or Slave mode operation
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports PDMA transfer
  - Supports one data channel half-duplex transfer
  - Support receive-only mode
- I^2S Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports PDMA transfer

6.17 Timer Controller (TMR)

6.17.1 Overview

The Timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The Timer controller also provides four PWM generators. Each PWM generator supports two PWM output channels in independent mode and complementary mode. The output state of PWM output pin can be control by pin mask, polarity and break control, and dead-time generator.

6.17.2 Features

6.17.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer equips one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, ADC and PDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports Inter-Timer trigger mode

6.17.2.2 PWM Function Features

- Supports maximum clock frequency up to 72MHz
- Supports independent mode for PWM generator with two output channels
- Supports complementary mode for PWM generator with paired PWM output channel
  - 12-bit dead-time insertion with 12-bit prescale
- Supports 12-bit prescale from 1 to 4096
- Supports 16-bit PWM counter
  - Up, down and up-down count operation type
  - One-shot or auto-reload counter operation mode
- Supports mask function and tri-state enable for each PWM output pin
- Supports brake function

  - Brake source from pin, analog comparator and system safety events (clock failed, Brown-out detection and CPU lockup)
  - Brake pin noise filter control for brake source
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM zero point, period point, up-count compared or down-count compared point events
  - Brake condition happened
- Supports trigger ADC on the following events:
  - PWM zero point, period, zero or period point, up-count compared or down-count compared point events

6.18 USCI - Universal Serial Control Interface Controller

6.18.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

6.18.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

6.19 USCI – UART Mode

6.19.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter being independent, frames can start at different points in time for transmission and reception.

The UART controller also provides auto flow control. There are two conditions to wake up the system.

6.19.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-Bit Data Transfer (Support 9-Bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports Wake-up function (Data and nCTS Wakeup Only)

6.20 USCI - SPI Mode

6.20.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1.

This SPI protocol can operate as master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in master and Slave mode are shown below.

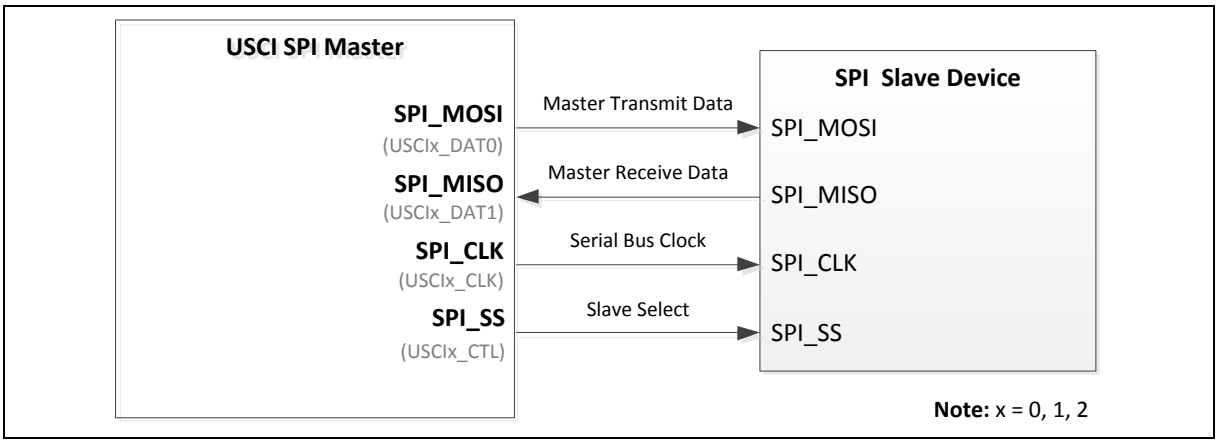


Figure 6.20-1 SPI Master Mode Application Block Diagram

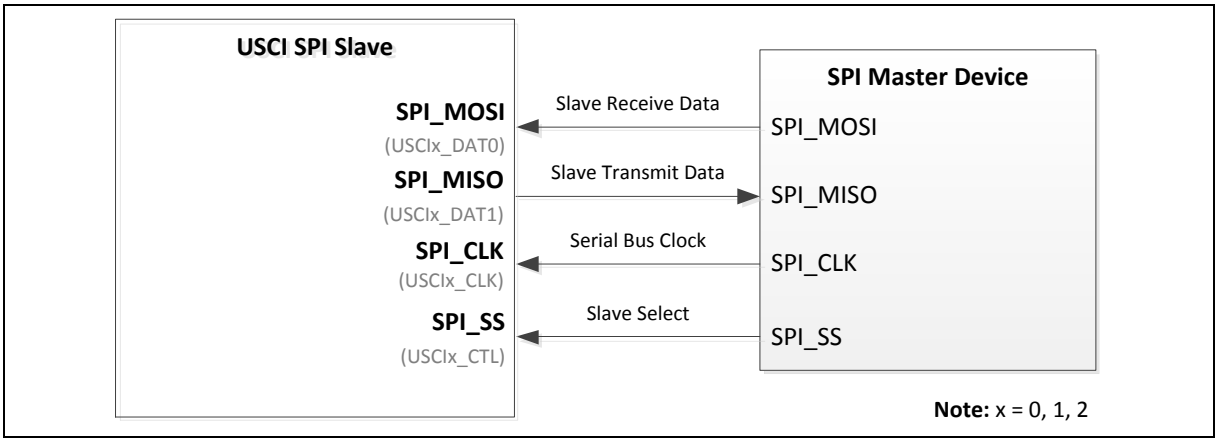


Figure 6.20-2 SPI Slave Mode Application Block Diagram

6.20.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master = f_{PCLK} / 2, Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence

- Supports Word Suspend function
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

6.21 USCI - I²C Mode

6.21.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.21-1 for more detailed I²C BUS Timing.

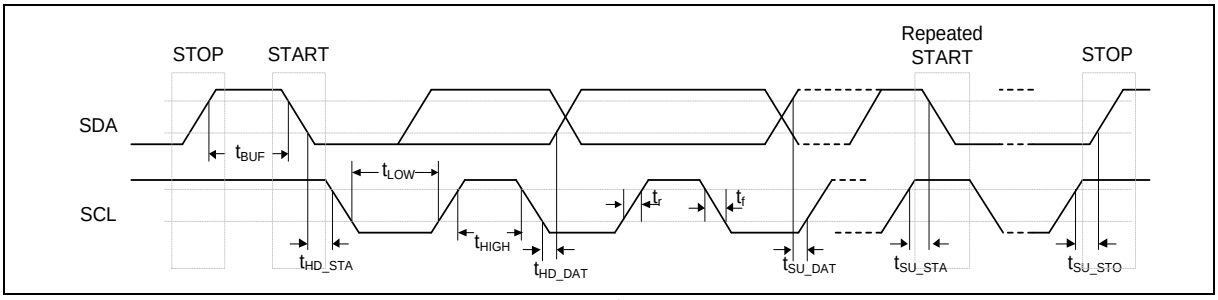


Figure 6.21-1 I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (UI2C_CTL [2:0]) = 100b. When enable this port, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

Note: Pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode .

6.21.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Supports multi-master bus
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by data toggle or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

6.22 UART Interface Controller (UART)

6.22.1 Overview

The M0564 series provides three channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs Normal Speed UART and supports flow control function. The UART controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, LIN and RS-485 function modes and auto-baud rate measuring function.

6.22.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Support for 3/16 bit duration for normal mode
- Supports LIN function mode
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detection function for receiver
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Support PDMA transfer function

6.23 Watchdog Timer (WDT)

6.23.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, the Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.23.2 Features

- Supports 18-bit free running up counter
- Selectable time-out interval (2^4 ~ 2^{18}) and the time-out interval is 1.6 ms ~ 26.214s if WDT_CLK is 10 kHzSupports selectable WDT reset delay period between WDT time-out event to WDT reset system event, and it includes 1026、130、18 or 3 * WDT_CLK delay period
- System kept in reset state about 63 * WDT_CLK period time after system reset event occurred
- Supports to force WDT function enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT

6.24 Window Watchdog Timer (WWDT)

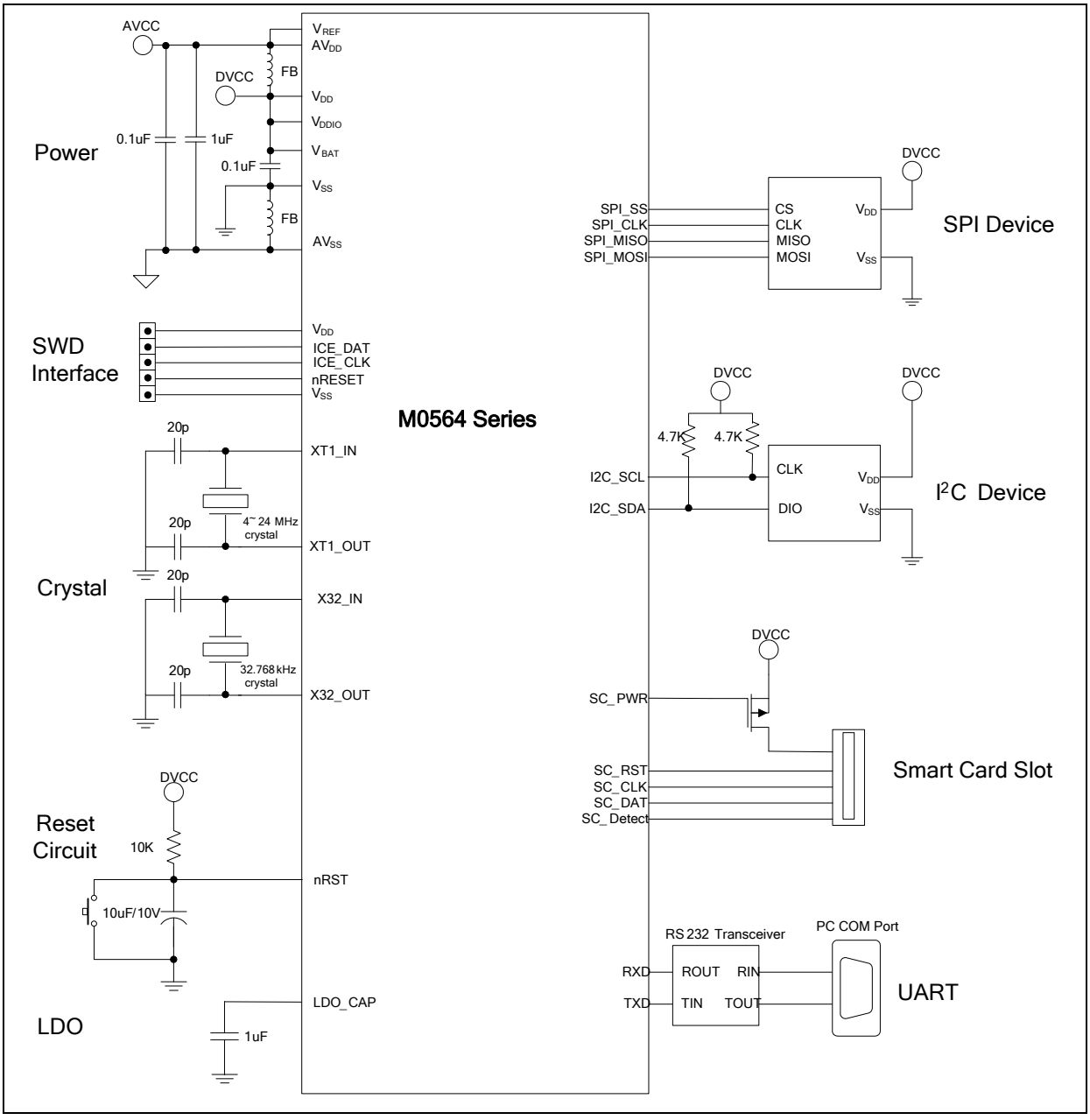
6.24.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset while WWDT counter is not reload within a specified window period when application program run to uncontrollable status by any unpredictable condition.

6.24.2 Features

- Supports 6-bit down counter value CNTDAT (WWDT_CNT[5:0]) and maximum 6-bit compare value CMPDAT (WWDT_CTL[21:16]) to adjust the WWDT compare time-out window period flexible
- Supports PSCSEL (WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode
- WWDT counter only can be reloaded within in valid window period to prevent system reset

7 APPLICATION CIRCUIT



8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	V_{DD}-V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} – 0.3	V_{DD} + 0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+105	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into V_{DD}	I_{DD}	-	120	mA
Maximum Current out of V_{SS}	I_{SS}	-	120	mA
Maximum Current sunk by a I/O Pin	I_{IO}	-	35	mA
Maximum Current Sourced by a I/O Pin		-	35	mA
Maximum Current Sunk by Total I/O Pins		-	100	mA
Maximum Current Sourced by Total I/O Pins		-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affect the lift and reliability of the device.

8.2 DC Electrical Characteristics

(V_{DD}-V_{SS} = 2.5 ~ 5.5V, TA = 25°C, F_{OSC} = 72 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS					
		MIN.	TYP.	MAX.	UNIT						
Operation Voltage	V_{DD} - V_{SS}	2.5	-	5.5	V	V_{DD} = 2.5 ~ 5.5V up to 72 MHz					
Power supply for PE.8 ~ PE.13	V_{DDIO} - V_{SS}	1.8	-	5.5	V						
Power supply for PF.0, PF.1 and PF.2	V_{BAT} - V_{SS}	2.5	-	5.5	V						
Power Ground	V_{SS} - AV_{SS}	-0.05	-	+0.05	V						
LDO Output Voltage	V_{LDO}	1.62	1.8	1.98	V	MCU operating in Run, Idle or Power-down mode					
	C_{LDO}	1			uF	Connect to LDO_CAP pin					
Band-gap Voltage	V_{BG}	-	1.21	-	V						
Allowed voltage difference for V_{DD} and AV_{DD}	V_{DD} - AV_{DD}	-0.3	-	+0.3	V						
Operating Current Normal Run Mode HCLK =72 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD1}	-	57	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	12 MHz	X	X	V	V
	I_{DD2}	-	22	-	mA	5.5 V	12 MHz	X	X	V	X
	I_{DD3}	-	57	-	mA	3.3 V	12 MHz	X	X	V	V
	I_{DD4}	-	22	-	mA	3.3 V	12 MHz	X	X	V	X
Operating Current Normal Run Mode HCLK =72 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD5}	-	55	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	X	X	V	V	V
	I_{DD6}	-	21	-	mA	5.5 V	X	X	V	V	X
	I_{DD7}	-	55	-	mA	3.3 V	X	X	V	V	V
	I_{DD8}	-	21	-	mA	3.3 V	X	X	V	V	X
Operating Current Normal Run Mode HCLK =48 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD9}	-	33	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	12 MHz	X	X	V	V
	I_{DD10}	-	14	-	mA	5.5 V	12 MHz	X	X	V	X
	I_{DD11}	-	33	-	mA	3.3 V	12 MHz	X	X	V	V
	I_{DD12}	-	14	-	mA	3.3 V	12 MHz	X	X	V	X

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS					
		MIN.	TYP.	MAX.	UNIT						
Operating Current Normal Run Mode HCLK =48 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD13}	-	TBD	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	X	X	V	X	V
	I_{DD14}	-	TBD	-	mA	5.5 V	X	X	V	X	X
	I_{DD15}	-	TBD	-	mA	3.3 V	X	X	V	X	V
	I_{DD16}	-	TBD	-	mA	3.3 V	X	X	V	X	X
Operating Current Normal Run Mode HCLK =24 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD17}	-	15.8	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	24 MHz	X	X	X	V
	I_{DD18}	-	6.7	-	mA	5.5 V	24 MHz	X	X	X	X
	I_{DD19}	-	15.8	-	mA	3.3 V	24 MHz	X	X	X	V
	I_{DD20}	-	6.7	-	mA	3.3 V	24 MHz	X	X	X	X
Operating Current Normal Run Mode HCLK =24 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD21}	-	TBD	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	X	X	HIRC48/2	X	V
	I_{DD22}	-	TBD	-	mA	5.5 V	X	X	HIRC48/2	X	X
	I_{DD23}	-	TBD	-	mA	3.3 V	X	X	HIRC48/2	X	V
	I_{DD24}	-	TBD	-	mA	3.3 V	X	X	HIRC48/2	X	X
Operating Current Normal Run Mode HCLK =22.1184 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD25}	-	16.6	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	X	V	X	X	V
	I_{DD26}	-	6.2	-	mA	5.5 V	X	V	X	X	X
	I_{DD27}	-	16.6	-	mA	3.3 V	X	V	X	X	V
	I_{DD28}	-	6.2	-	mA	3.3 V	X	V	X	X	X
Operating Current Normal Run Mode HCLK =12 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD29}	-	7.8	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	12 MHz	X	X	X	V
	I_{DD30}	-	3.1	-	mA	5.5 V	12 MHz	X	X	X	X
	I_{DD31}	-	7.8	-	mA	3.3 V	12 MHz	X	X	X	V
	I_{DD32}	-	3.1	-	mA	3.3 V	12 MHz	X	X	X	X
Operating Current Normal Run Mode HCLK =4 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD33}	-	2.74	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	4 MHz	X	X	X	V
	I_{DD34}	-	1.23	-	mA	5.5 V	4 MHz	X	X	X	X
	I_{DD35}	-	2.72	-	mA	3.3 V	4 MHz	X	X	X	V
	I_{DD36}	-	1.20	-	mA	3.3 V	4 MHz	X	X	X	X
Operating Current	I_{DD37}	-	136	-	uA	V_{DD}	LXT	LIRC	PLL	All digital module	

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Normal Run Mode HCLK =32.768 kHz while(1){}executed from flash V_{LDO}=1.8 V						5.5 V	32.768 kHz	X	X	V
	I_{DD38}	-	123	-	uA	5.5 V	32.768 kHz	X	X	X
	I_{DD39}	-	123	-	uA	3.3 V	32.768 kHz	X	X	V
	I_{DD40}	-	109	-	uA	3.3 V	32.768 kHz	X	X	X
Operating Current Normal Run Mode HCLK =10 kHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD41}	-	121	-	uA	V_{DD}	LXT	LIRC	PLL	All digital module
						5.5 V	X	10 kHz	X	V
	I_{DD42}	-	117	-	uA	5.5 V	X	10 kHz	X	X
	I_{DD43}	-	107	-	uA	3.3 V	X	10 kHz	X	V
	I_{DD44}	-	102	-	uA	3.3 V	X	10 kHz	X	X
Operating Current Idle Mode HCLK =72 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE1}	-	47	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	12 MHz	X	X	V	V
	I_{IDLE2}	-	9	-	mA	5.5 V	12 MHz	X	X	V	X
	I_{IDLE3}	-	47	-	mA	3.3 V	12 MHz	X	X	V	V
	I_{IDLE4}	-	9	-	mA	3.3 V	12 MHz	X	X	V	X
Operating Current Idle Mode HCLK =72 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE5}	-	47	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	X	X	V	V	V
	I_{IDLE6}	-	9.5	-	mA	5.5 V	X	X	V	V	X
	I_{IDLE7}	-	47	-	mA	3.3 V	X	X	V	V	V
	I_{IDLE8}	-	9.5	-	mA	3.3 V	X	X	V	V	X
Operating Current Idle Mode HCLK =48 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE9}	-	27	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	12 MHz	X	X	V	V
	I_{IDLE10}	-	5.5	-	mA	5.5 V	12 MHz	X	X	V	X
	I_{IDLE11}	-	27	-	mA	3.3 V	12 MHz	X	X	V	V
	I_{IDLE12}	-	5.5	-	mA	3.3 V	12 MHz	X	X	V	X
Operating Current Idle Mode HCLK =48 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE13}	-	TBD	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	X	X	V	X	V
	I_{IDLE14}	-	TBD	-	mA	5.5 V	X	X	V	X	X
	I_{IDLE15}	-	TBD	-	mA	3.3 V	X	X	V	X	V
	I_{IDLE16}	-	TBD	-	mA	3.3 V	X	X	V	X	X
Operating Current Idle Mode HCLK =24 MHz	I_{IDLE17}	-	12.5	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	24 MHz	X	X	X	V

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS					
		MIN.	TYP.	MAX.	UNIT						
while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE18}	-	2.2	-	mA	5.5 V	24 MHz	X	X	X	X
	I_{IDLE19}	-	12.5	-	mA	3.3 V	24 MHz	X	X	X	V
	I_{IDLE20}	-	2.2	-	mA	3.3 V	24 MHz	X	X	X	X
Operating Current Idle Mode HCLK =24 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE21}	-	TBD	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	X	X	HIRC48/2	X	V
	I_{IDLE22}	-	TBD	-	mA	5.5 V	X	X	HIRC48/2	X	X
	I_{IDLE23}	-	TBD	-	mA	3.3 V	X	X	HIRC48/2	X	V
	I_{IDLE24}	-	TBD	-	mA	3.3 V	X	X	HIRC48/2	X	X
Operating Current Idle Mode HCLK =22.1184 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE25}	-	12.3	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	X	V	X	X	V
	I_{IDLE26}	-	1.9	-	mA	5.5 V	X	V	X	X	X
	I_{IDLE27}	-	12.3	-	mA	3.3 V	X	V	X	X	V
	I_{IDLE28}	-	1.9	-	mA	3.3 V	X	V	X	X	X
Operating Current Idle Mode HCLK =12 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE29}	-	6.3	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	12 MHz	X	X	X	V
	I_{IDLE30}	-	1.2	-	mA	5.5 V	12 MHz	X	X	X	X
	I_{IDLE31}	-	6.3	-	mA	3.3 V	12 MHz	X	X	X	V
	I_{IDLE32}	-	1.2	-	mA	3.3 V	12 MHz	X	X	X	X
Operating Current Idle Mode HCLK =4 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE33}	-	2.2	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	4 MHz	X	X	X	V
	I_{IDLE34}	-	0.50	-	mA	5.5 V	4 MHz	X	X	X	X
	I_{IDLE35}	-	2.2	-	mA	3.3 V	4 MHz	X	X	X	V
	I_{IDLE36}	-	0.46	-	mA	3.3 V	4 MHz	X	X	X	X
Operating Current Idle Mode HCLK =32.768 kHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE37}	-	129	-	uA	V_{DD}	LXT	LIRC	PLL	All digital module	
						5.5 V	32.768 kHz	X	X	V	
	I_{IDLE38}	-	115	-	uA	5.5 V	32.768 kHz	X	X	X	
	I_{IDLE39}	-	115	-	uA	3.3 V	32.768 kHz	X	X	V	
	I_{IDLE40}	-	101	-	uA	3.3 V	32.768 kHz	X	X	X	
Operating Current Idle Mode HCLK =10 kHz while(1){}executed from flash	I_{IDLE41}	-	119	-	uA	V_{DD}	LXT	LIRC	PLL	All digital module	
						5.5 V	X	10 kHz	X	V	
	I_{IDLE42}	-	114	-	uA	5.5 V	X	10 kHz	X	X	

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
V_{LDO}=1.8 V	I_{IDLE43}	-	104	-	uA	3.3 V	X	10 kHz	X	V
	I_{IDLE44}	-	100	-	uA	3.3 V	X	10 kHz	X	X
Standby Current Power-down Mode V_{LDO}=1.8 V	I_{PWD1}	-	TBD	-	uA	V_{DD}	HXT/HIRC	LXT/LIRC	PLL	RAM retention
						5.5 V	X	LXT	X	V
	I_{PWD2}	-	TBD	-	uA	5.5 V	X	LIRC	X	V
	I_{PWD3}	-	TBD	-	uA	5.5 V	X	LXT & LIRC	X	V
	I_{PWD4}	-	20		uA	5.5 V	X	X	X	V
	I_{PWD5}	-	13.5	-	uA	3.3 V	X	LXT	X	V
	I_{PWD6}	-	13.3	-	uA	3.3 V	X	LIRC	X	V
	I_{PWD7}	-	14.3	-	uA	3.3 V	X	LXT & LIRC	X	V
	I_{PWD8}	-	12.5	-	uA	3.3 V	X	X	X	V
Logic 0 Input Current (Quasi-bidirectional mode)	I_{IL}	-	-70	-	uA	V_{DD} = V_{BAT} = V_{DDIO} = 5.5V, V_{IN} = 0V				
Logic 1 to 0 Transition Current (Quasi-bidirectional mode) [3]	I_{TL}	-	-620	-	uA	V_{DD} = V_{BAT} = V_{DDIO} = 5.5V, V_{IN} = 2.0V				
Input Pull Up Resistor	R_{IN}	-	TBD	-	KΩ	V_{DD} = V_{BAT} = V_{DDIO} = 5.5V				
		-	TBD	-	KΩ	V_{DD} = V_{BAT} = V_{DDIO} = 3.3V				
		-	TBD	-	KΩ	V_{DD} = V_{BAT} = 2.5 ~ 5.5 V V_{DDIO} = 1.8 V				
Input Leakage Current	I_{LK}	-	0	-	µA	V_{DD} = V_{BAT} = V_{DDIO} = 5.5V, 0 < V_{IN} < V_{DD} Open-drain or input only mode				
Input Low Voltage (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = V_{BAT} = V_{DDIO} = 4.5 V				
		-0.3	-	0.6	V	V_{DD} = V_{BAT} = V_{DDIO} = 2.5 V				
Input Low Voltage (TTL input for V_{DDIO} domain)	V_{IL2}	-0.3	-	TBD	V	V_{DD} = V_{BAT} = 2.5 ~ 5.5 V V_{DDIO} = 1.8 V				
Input High Voltage (TTL input)	V_{IH1}	2.0	-	V_{DD} + 0.3	V	V_{DD} = V_{BAT} = V_{DDIO} = 5.5V				
		1.5	-	V_{DD} + 0.3	V	V_{DD} = V_{BAT} = V_{DDIO} = 2.5V				
Input High Voltage (TTL input for V_{DDIO} domain)	V_{IH2}	TBD	-	V_{DD} + 0.3	V	V_{DD} = V_{BAT} = 2.5 ~ 5.5 V V_{DDIO} = 1.8 V				
Input Low Voltage (Schmitt input)	V_{IL3}	-0.3	-	0.3V_{DD}	V	V_{DD} = V_{BAT} = V_{DDIO} = 2.5 ~ 5.5 V				

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input Low Voltage (Schmitt input for V_{DDIO} domain)	V_{IL4}	-0.3	-	$0.3V_{DD}$	V	V_{DDIO} = 1.8 ~ 5.5V
Input High Voltage (Schmitt input)	V_{IH3}	$0.7V_{DD}$	-	V_{DD} + 0.3	V	$V_{DD} = V_{BAT} = V_{DDIO}$ = 2.5 ~ 5.5V
Input High Voltage (Schmitt input for V_{DDIO} domain)	V_{IH4}	$0.7V_{DDIO}$	-	V_{DDIO} + 0.3	V	V_{DDIO} = 1.8 ~ 5.5V
Hysteresis voltage of PA~PF (Schmitt input)	V_{HY}	-	$0.2V_{DD}$	-	V	
Negative going threshold (Schmitt input), nRESET	V_{IL5}	-0.3	-	$0.2V_{DD}$	V	
Positive going threshold (Schmitt Input), nRESET	V_{IH5}	$0.8V_{DD}$	-	V_{DD} + 0.3	V	
Internal nRESET pin pull up resistor	R_{RST}	-	16	-	KΩ	V_{DD} = 5.5V
Source Current (Quasi-bidirectional Mode)	I_{SR1}	-	-400	-	uA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 4.5V, V_S = 2.4V
	I_{SR2}	-	-80	-	uA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 2.7V, V_S = 2.2V
	I_{SR3}	-	-73	-	uA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 2.5V, V_S = 2.0V
Source Current (Quasi-bidirectional Mode for V_{DDIO} domain)	I_{SR4}	-	-19	-	uA	$V_{DD} = V_{BAT}$ = 2.5 ~ 5.5V V_{DDIO} = 1.8V, V_S = 1.6V
Source Current (Push-pull Mode)	I_{SR5}	-18	-26		mA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 4.5V, V_S = 2.4V
	I_{SR6}	-	-5.8	-	mA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 2.7V, V_S = 2.2V
	I_{SR7}	-	-5.2	-	mA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 2.5V, V_S = 2.0V
Source Current (Push-pull Mode for V_{DDIO} domain)	I_{SR8}	-	-1.5	-	mA	$V_{DD} = V_{BAT}$ = 2.5 ~ 5.5V V_{DDIO} = 1.8V, V_S = 1.6V
Sink Current (Quasi-bidirectional, Open-Drain and Push-pull Mode)	I_{SK1}	7	15	-	mA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 4.5V, V_S = 0.45V
	I_{SK2}	-	10	-	mA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 2.7V, V_S = 0.45V
	I_{SK3}	-	9	-	mA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 2.5V, V_S = 0.45V

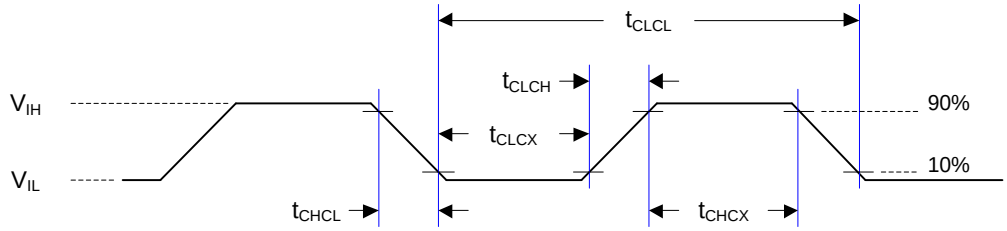
PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Sink Current (Quasi-bidirectional, Open-Drain and Push-pull Mode for V_{DDIO} domain)	I_{SK4}	-	-2.2	-	mA	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$ $V_{DDIO} = 1.8V$, $V_S = 1.6V$
Higher GPIO Rising Rate	$HIORR_1$	-	2.46	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 5.5V$, without capacitor
	$HIORR_2$		3.24		ns	$V_{DD} = V_{BAT} = V_{DDIO} = 5.5V$, with 10pF capacitor
	$HIORR_3$	-	3.12	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 3.0V$, without capacitor
	$HIORR_4$	-	4.56	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 3.0V$, with 10pF capacitor
	$HIORR_5$	-	TBD	-	ns	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$, $V_{DDIO} = 1.8V$, without capacitor (for VDDIO domain)
	$HIORR_6$	-	TBD	-	ns	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$, $V_{DDIO} = 1.8V$, with 10pF capacitor (for VDDIO domain)
Basic GPIO Rising Rate	$BIORR_1$	-	3.24	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 5.5V$, without capacitor
	$BIORR_2$	-	4.15	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 5.5V$, with 10pF capacitor
	$BIORR_3$	-	4.75	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 3.0V$, without capacitor
	$BIORR_4$	-	6.43	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 3.0V$, with 10pF capacitor
	$BIORR_5$	-	TBD	-	ns	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$, $V_{DDIO} = 1.8V$, without capacitor (for VDDIO domain)
	$BIORR_6$	-	TBD	-	ns	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$, $V_{DDIO} = 1.8V$, with 10pF capacitor (for VDDIO domain)
Higher GPIO Falling Rate	$HIOFR_1$	-	2.10	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 5.5V$, without capacitor

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	$HIOFR_2$	-	2.83	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 5.5V$, with 10pF capacitor
	$HIOFR_3$	-	3.12	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 3.3V$, without capacitor
	$HIOFR_4$	-	4.19	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 3.3V$, with 10pF capacitor
	$HIOFR_5$	-	TBD	-	ns	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$, $V_{DDIO} = 1.8V$, without capacitor (for V_{DDIO} domain)
	$HIOFR_6$	-	TBD	-	ns	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$, $V_{DDIO} = 1.8V$, with 10pF capacitor (for V_{DDIO} domain)
Basic GPIO Falling Rate	$BIOFR_1$	-	3.42	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 5.5V$, without capacitor
	$BIOFR_2$	-	4.40	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 5.5V$, with 10pF capacitor
	$BIOFR_3$	-	6.14	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 3.3V$, without capacitor
	$BIOFR_4$	-	7.87	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 3.3V$, with 10pF capacitor
	$BIOFR_5$	-	TBD	-	ns	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$, $V_{DDIO} = 1.8V$, without capacitor (for V_{DDIO} domain)
	$BIOFR_6$	-	TBD	-	ns	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$, $V_{DDIO} = 1.8V$, with 10pF capacitor (for V_{DDIO} domain)

8.3 AC Electrical Characteristics

8.3.1 External 4~24 MHz High Speed Crystal (HXT) Input Clock

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Clock High Time	t_{CHCX}	10	-	-	nS	
Clock Low Time	t_{CLCX}	10	-	-	nS	
Clock Rise Time	t_{CLCH}	2	-	15	nS	
Clock Fall Time	t_{CHCL}	2	-	15	nS	
Input High Voltage	V_{IH}	$0.7V_{DD}$	-	V_{DD}	V	
Input Low Voltage	V_{IL}	0	-	$0.3V_{DD}$	V	



Note: Duty cycle is 50%.

8.3.2 External 4~24 MHz High Speed Crystal (HXT) Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{HXT}	4	-	24	MHz	V_{DD} = 2.5 ~ 5.5V
Temperature	T_{HXT}	-40	-	+105	°C	
Operating current	I_{HXT}	-	TBD	-	mA	V_{DD} = 5.5V @ 12MHz
		-	0.4	-	mA	V_{DD} = 3.3V @ 12MHz

8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
4MHz ~ 24 MHz	20pF	20pF	without

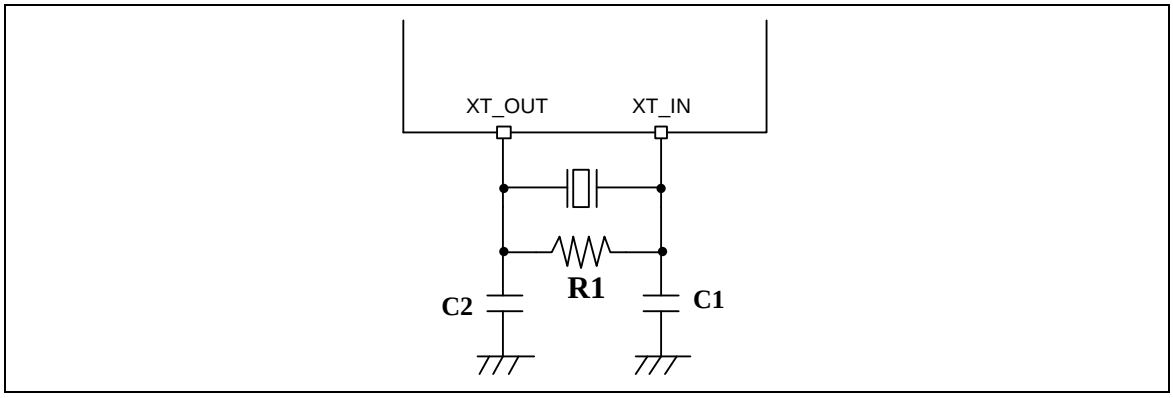
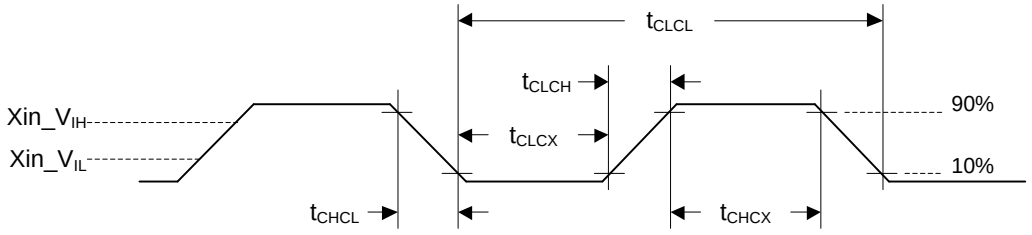


Figure 8.3-1 Typical Crystal Application Circuit

8.3.3 External 32.768 kHz Low Speed Crystal (LXT) Input Clock

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Clock High Time	t_{CHCX}	TBD	-	-	nS	
Clock Low Time	t_{CLCX}	TBD	-	-	nS	
Clock Rise Time	t_{CLCH}	TBD	-	TBD	nS	
Clock Fall Time	t_{CHCL}	TBD	-	TBD	nS	
LXT Input Pin Input High Voltage	Xin_V_{IH}	$0.7V_{LDO}$	-	V_{DD}	V	
LXT Input Pin Input Low Voltage	Xin_V_{IL}	0	-	$0.3V_{LDO}$	V	



Note: Duty cycle is 50%.

8.3.4 External 32.768 kHz Low Speed Crystal (LXT) Input Clock

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{LXT}	-	32.768	-	kHz	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$
Temperature	T_{LXT}	-40	-	+105	°C	
Operating current	I_{LXT}		0.7		μA	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$

8.3.4.1 Typical Crystal Application Circuits

CRYSTAL	C3	C4	R2
32.768 kHz	20pF	20pF	without

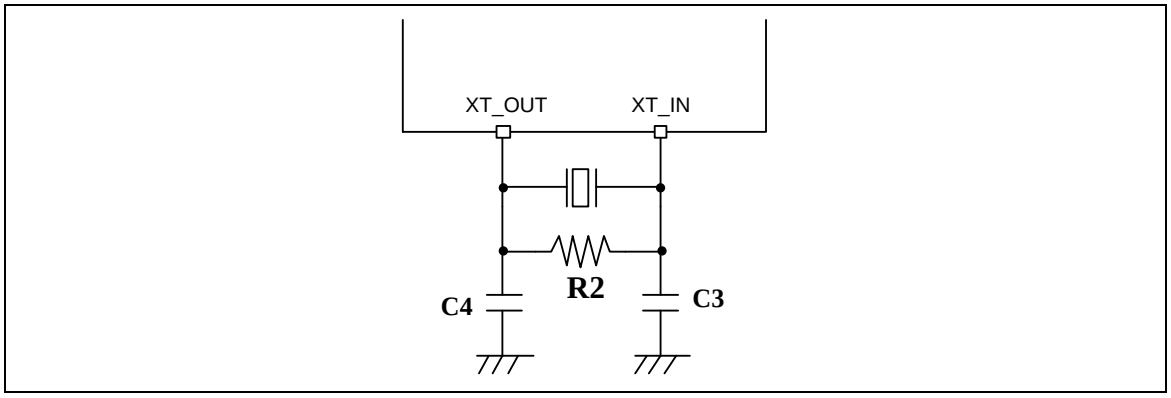


Figure 8.3-2 Typical Crystal Application Circuit

8.3.5 Internal 48 MHz High Speed RC Oscillator (HIRC48)

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Center Frequency	f_{HRC}	-	48	-	MHz	T_A = 25°C, V_{DD} = 3.3V
Calibrated Internal Oscillator Frequency		-1	-	+1	%	T_A = 25°C, V_{DD} = 2.5 ~ 5.5V
		-2	-	+2	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.5 ~ 5.5V
		-0.25	-	+0.25	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.5 ~ 5.5V Auto trimmed by LXT
Operating current	I_{HRC}	-	440	-	μA	

8.3.6 Internal 22.1184 MHz High Speed RC Oscillator (HIRC)

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Center Frequency	f_{HRC}	-	22.1184	-	MHz	T_A = 25°C, V_{DD} = 3.3V
Calibrated Internal Oscillator Frequency		-1	-	+1	%	T_A = 25°C, V_{DD} = 2.5 ~ 5.5V
		-2	-	+2	%	-40°C ~ +105 °C, V_{DD} = 2.5 ~ 5.5V
		-0.25	-	+0.25	%	-40°C ~ +105 °C, V_{DD} = 2.5 ~ 5.5V Auto trimmed by LXT
Operating current	I_{HRC}	-	470	-	μA	

8.3.7 Internal 10 kHz Low Speed RC Oscillator (LIRC)

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Center Frequency	F_{LRC}	-	10	-	kHz	T_A = 25°C, VDD = 3.3V

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Calibrated Internal Oscillator Frequency		-30	-	+30	%	T_A = 25 °C, VDD = 2.5 ~ 5.5V
		-50	-	+50	%	-40°C ~+105 °C, VDD = 2.5 ~ 5.5V
Operating current	I_{LRC}		0.9		μA	

8.4 Analog Characteristics

8.4.1 LDO

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Temperature	T_A	-40	-	+105	°C	
DC Power Supply	V_{DD}	2.5	-	5.5	V	
Output Voltage	V_{LDO}	1.62	1.8	1.98	V	

Note 1: It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

Note 2: For ensuring power stability, a 1μF Capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

8.4.2 Temperature Sensor

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Detection Temperature	T_{DET}	-40	-	+105	°C	
Gain	V_{TG}	-1.76	-1.70	-1.64	mV/°C	
Offset	V_{TO}	-	745	-	mV	Temperature at 0 °C
Operating current	I_{TEMP}	6.4	-	10.5	μA	

Note 1: The temperature sensor formula for the output voltage (Vtemp) is as below equation.

Vtemp (mV) = Gain (mV/℃) x Temperature (℃) + Offset (mV)

8.4.3 Internal Voltage Reference (Int_V_{REF})

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
V_{REF} (2.048V)	V_{REF1}	1.986	-	2.151	V	VREFCTL = 3, AV_{DD}≥2.5V
V_{REF} (2.56V)	V_{REF2}	2.483	-	2.637	V	VREFCTL = 3, AV_{DD}≥2.9V
V_{REF} (3.072V)	V_{REF3}	2.98	-	3.164	V	VREFCTL = 3, AV_{DD}≥3.4V
V_{REF} (4.096V)	V_{REF4}	3.973	-	4.219	V	VREFCTL = 3, AV_{DD}≥4.5V
Start-up Time	T_{VREF_Start}	-	700	2000	uS	C_{VREF} = 4.7uF
Operating current	I_{VREF}		100		μA	

8.4.4 Power-on Reset

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Temperature	T_A	-40	-	+105	°C	
Threshold Voltage	V_{POR}	-	2	-	V	

8.4.5 Low-Voltage Reset

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Temperature	T_A	-40	-	+105	°C	
Threshold Voltage	V_{LVR}	2.0	2.2	2.45	V	T_A = +105℃
		1.8	2.0	2.20	V	T_A = +25℃
		1.75	1.95	2.2	V	T_A = -40 ℃
Start-up Time	T_{LVR_Start}	-	130	-	uS	T_A = +25℃
Quiescent Current	I_{LVR}	-	1.1	-	uA	AV_{DD} = 5.5V

8.4.6 Brown-out Detector

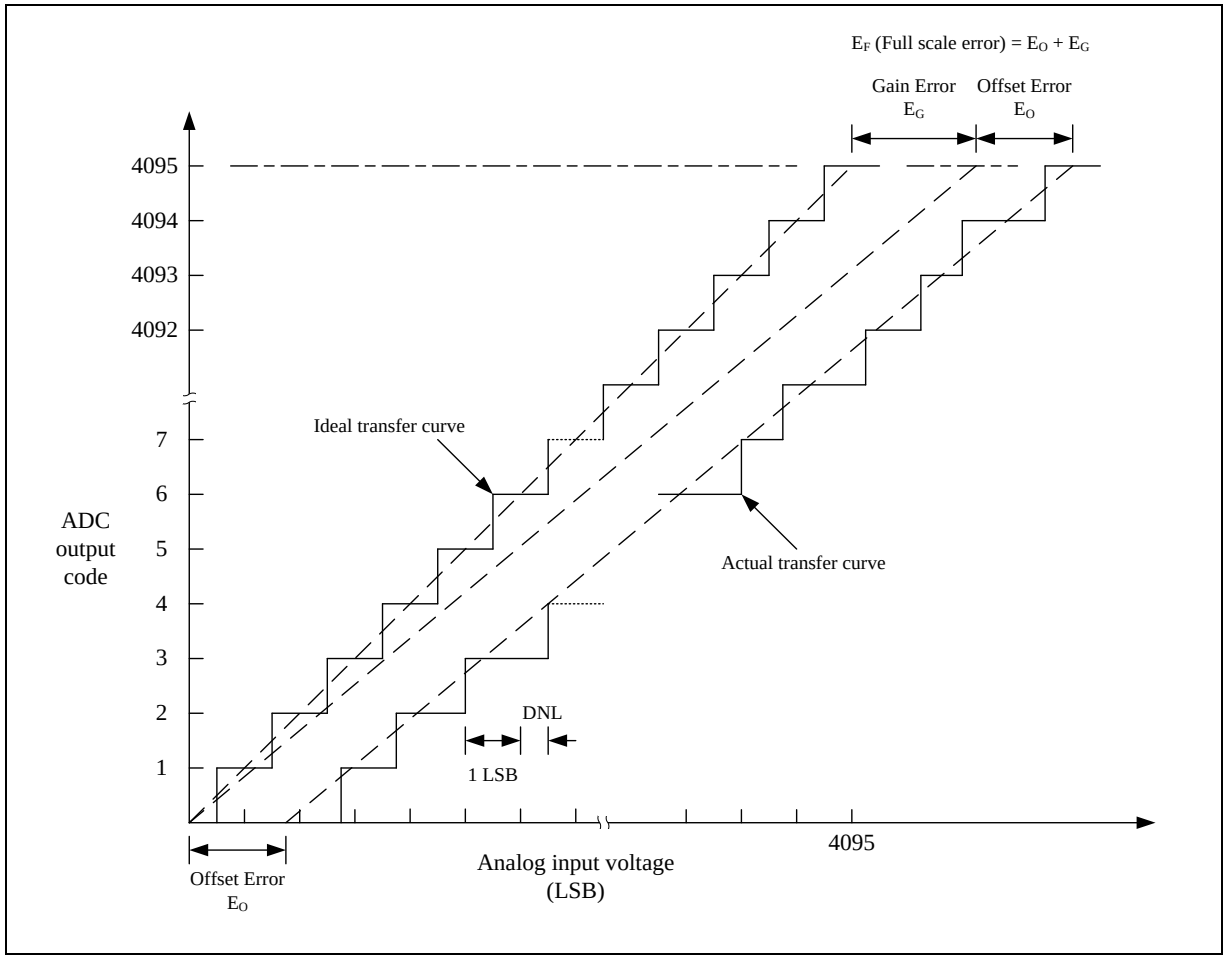
PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Temperature	T_A	-40	-	+105	°C	
Brown-out Voltage (Falling edge)	V_{BODF}	4.2	4.4	4.6	V	BODVL [1:0] = 11
		3.5	3.7	3.9	V	BODVL [1:0] = 10
		2.55	2.7	2.85	V	BODVL [1:0] = 01
		2.05	2.2	2.35	V	BODVL [1:0] = 00
Brown-out Voltage (Rising edge)	V_{BODR}	4.3	4.5	4.7	V	BODVL [1:0] = 11
		3.6	3.8	4.0	V	BODVL [1:0] = 10
		2.6	2.75	2.9	V	BODVL [1:0] = 01
		2.1	2.25	2.4	V	BODVL [1:0] = 00
Start-up Time	T_{BOD_Start}	-	1030	-	uS	T_A = +25℃
Quiescent Current	I_{BOD}		83	-	uA	T_A = +25℃, AV_{DD} = 5.5V BODLPM = 0

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
			0.7		uA	T_A = +25℃ , AV_{DD} = 5.5V BODLPM = 1

8.4.7 12-bit ADC

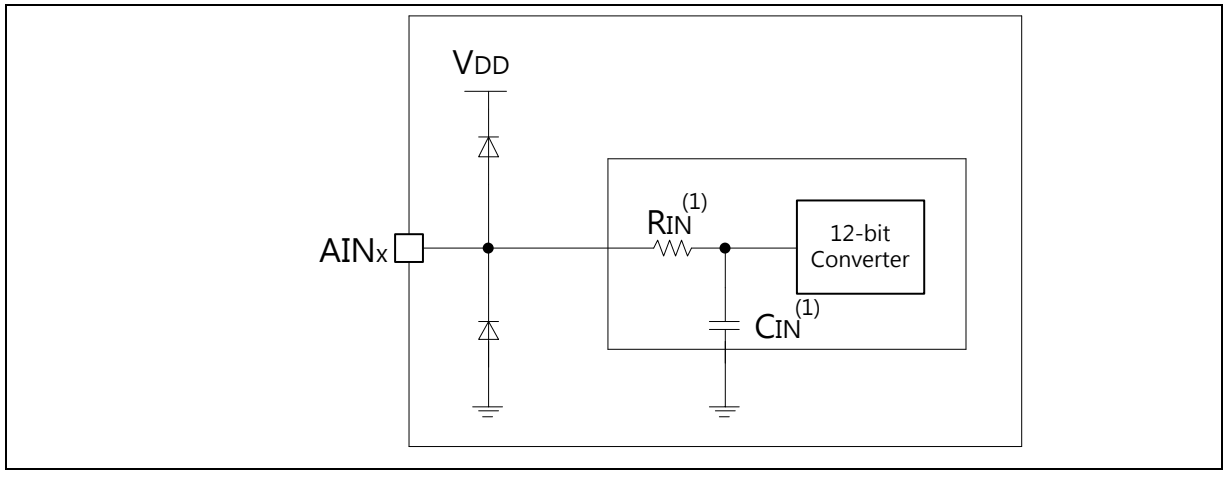
PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Temperature	T_A	-40	-	+105	°C	
Operating voltage	AV_{DD}	3.0	-	5.5	V	$AV_{DD} = V_{DD}$
Reference voltage	V_{REF}	3.0		AV_{DD}	V	
ADC input voltage	V_{IN}	0	-	AV_{REF}	V	
Resolution	R_{ADC}	12			Bit	
Integral Non-Linearity Error	INL	-2	+1.5	+2	LSB	
Differential Non-Linearity	DNL	-1	+1.5	+2	LSB	
Gain error	E_G	-4	-2	+4	LSB	
Offset error	E_{OFFSET}	-4	2	+4	LSB	
Absolute error	E_{ABS}	-4	-	+4	LSB	
Monotonic	-	Guaranteed			-	
ADC Clock frequency	F_{ADC}	1		16	MHz	
Acquisition Time (Sample Stage)	T_{ACQ}	2	7	21	$1/F_{ADC}$	Default: 7 (1/FADC)
Conversion time	T_{CONV}	15	20	34	$1/F_{ADC}$	$T_{CONV} = T_{ACQ} + 13$ Default: 20 (1/FADC)
Conversion Rate (F_{ADC}/T_{CONV})	F_{SPS}	-	-	800	kSPS	T_{CONV} = 20 clock F_{ADC} = 16 MHz
Internal Capacitance[1]	C_{IN}	-	TBD	-	pF	
Input Load[1]	R_{IN}	-	TBD	-	kΩ	
Operating current	I_{ADC1}	-	4	-	mA	$AV_{DD} = V_{DD}$ = 5V ADC Clock Rate = 16 MHz

Note 1: Design by guarantee, no test in production.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

Typical connection diagram using the ADC



Note: GND < AIN_X <V_{REF} < VDD

8.4.8 Analog Comparator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Temperature	T_A	-40	-	+105	°C	
Input Common Mode Range	V_{COM}	0.1	-	AV_{DD}-0.1	V	
Input Offset Voltage	V_{OFF}	-	10	-	mV	HYSEN = 0
Hysteresis	V_{HYS}	10	60	-	mV	HYSEN = 1, V_{CM} = AV_{DD}/2
DC Gain[1005D	-	40	70		dB	
Propagation Delay	T_{PGD}		125	200	nS	V_{CM} = 1.2 V, V_{DIFF} = 0.1 V
Stable time	T_{STB}		0.35	1	uS	AV_{DD} = 5V
Operation Current	I_{CMP}		35	70	uA	
Reference voltage	V_{REF}	3.0		AV_{DD}	V	
ADC input voltage	V_{IN}	0	-	AV_{REF}	V	

Note1: Guaranteed by design, not tested in production.

8.5 Flash DC Electrical Characteris

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply Voltage	1.62	1.8	1.98	V	T_A = 25℃
N_{ENDUR}	Endurance	20,000	-	-	cycles[2]	
T_{RET}	Data Retention	100	-	-	year	
T_{ERASE}	Page Erase Time	20	-	40	mS	
TM_{ER}	Mass Erase Time	20	-	40	mS	
T_{PROG}	Program Time	20	-	40	uS	
I_{DD1}	Read Current	-	-	TBD	mA	
I_{DD2}	Program Current	-	-	TBD	mA	
I_{DD3}	Erase Current	-	-	TBD	uA	

Note 1: V_{FLA} is source from chip LDO output voltage.

Note 2: Number of program/erase cycles.

Note 3: This table is guaranteed by design, not test in production.

8.6 I2C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min.	Max.	Min.	Max.	
t_{LOW}	SCL low period	4.7	-	1.2	-	uS
t_{HIGH}	SCL high period	4	-	0.6	-	uS
$t_{SU;STA}$	Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	20+0.1Cb	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I^2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I^2C frequency.
3. I^2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

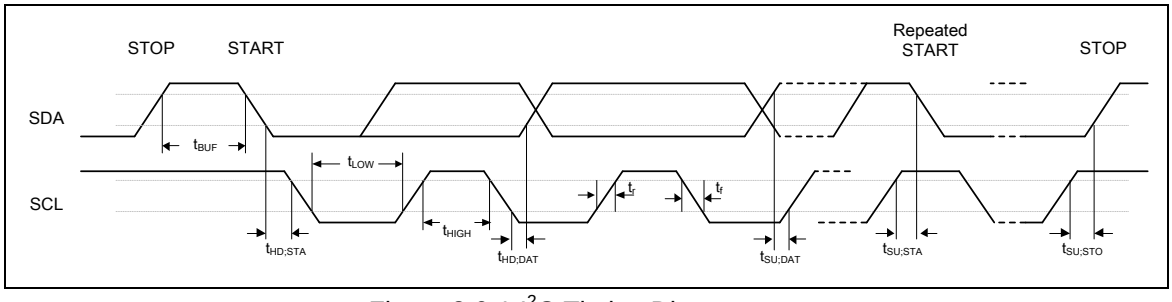


Figure 8.6-1 I^2C Timing Diagram

8.7 SPI Dynamic Characteristics

8.7.1 Dynamic Characteristics of Data Input and Output Pin

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI MASTER MODE (VDD = 4.5 V~5.5V, 30 PF LOADING CAPACITOR)					
t_{DS}	Data setup time	4	2	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	7	11	ns
SPI MASTER MODE (VDD = 3.0~3.6 V, 30 PF LOADING CAPACITOR)					
t_{DS}	Data setup time	5	3	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	13	18	ns

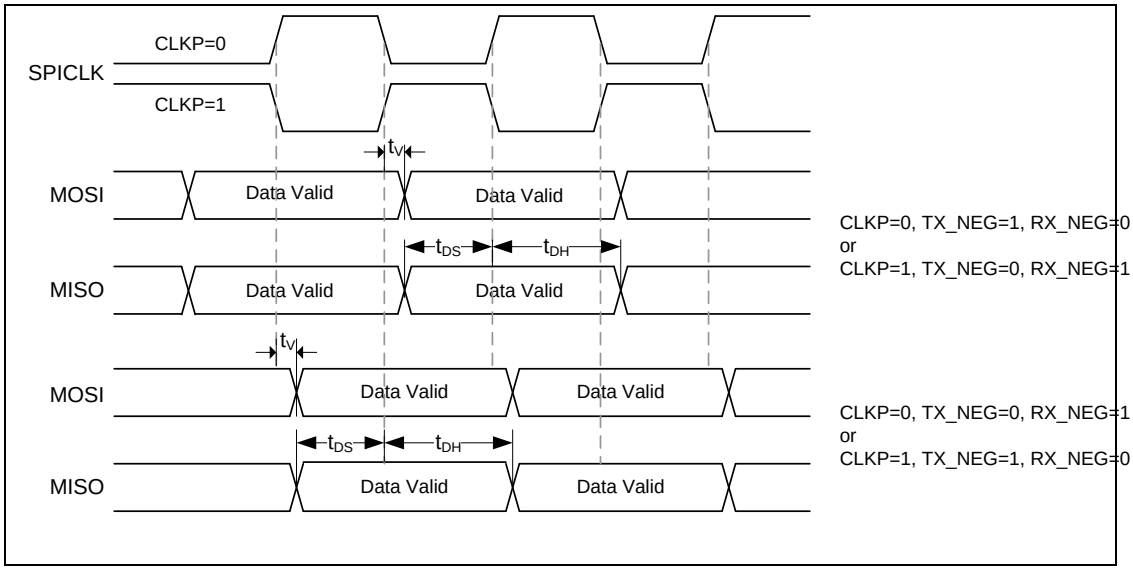


Figure 8.7-1 SPI Master Mode Timing Diagram

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI SLAVE MODE (VDD = 4.5 V~5.5V, 30 PF LOADING CAPACITOR)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+4	-	-	ns
t_V	Data output valid time	-	2*PCLK+11	2*PCLK+19	ns
SPI SLAVE MODE (VDD = 3.0 V ~ 3.6 V, 30 PF LOADING CAPACITOR)					
t_{DS}	Data setup time	0	-	-	ns

t_{DH}	Data hold time	2*PCLK+6	-	-	ns
t_V	Data output valid time	-	2*PCLK+19	2*PCLK+25	ns

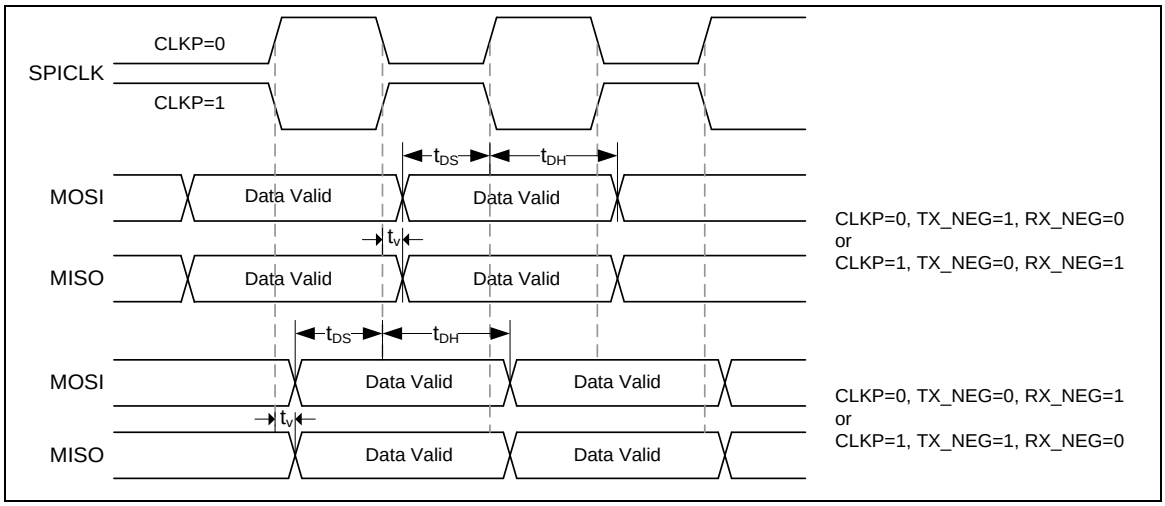
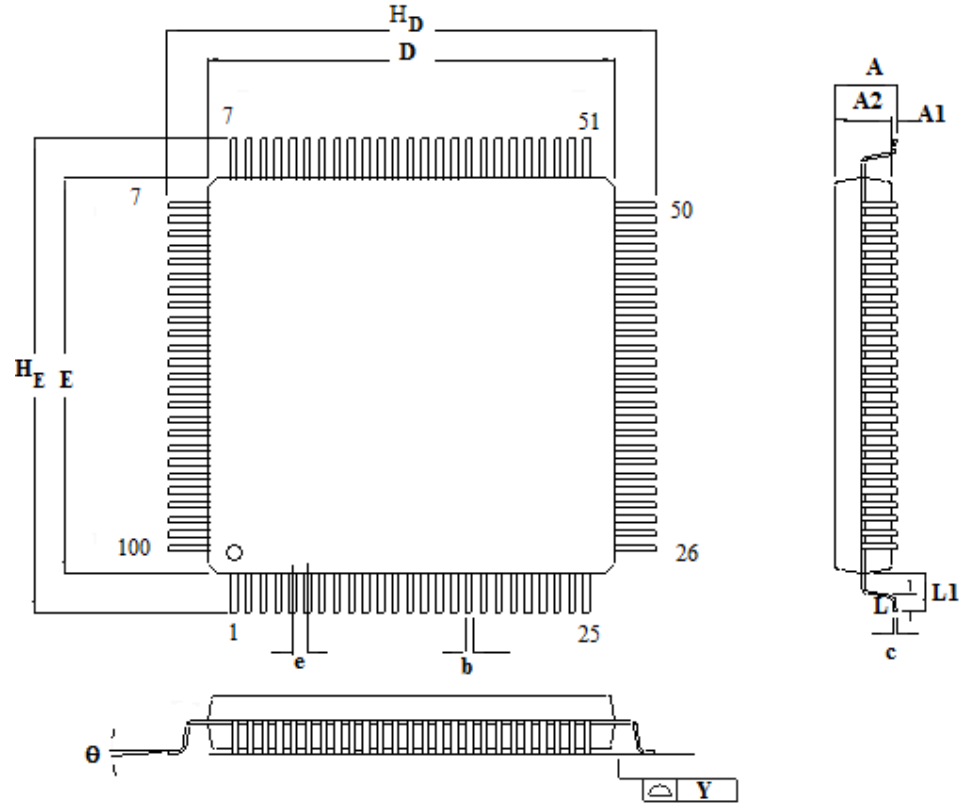


Figure 8.7-2 SPI Slave Mode Timing Diagram

9 PACKAGE DIMENSIONS

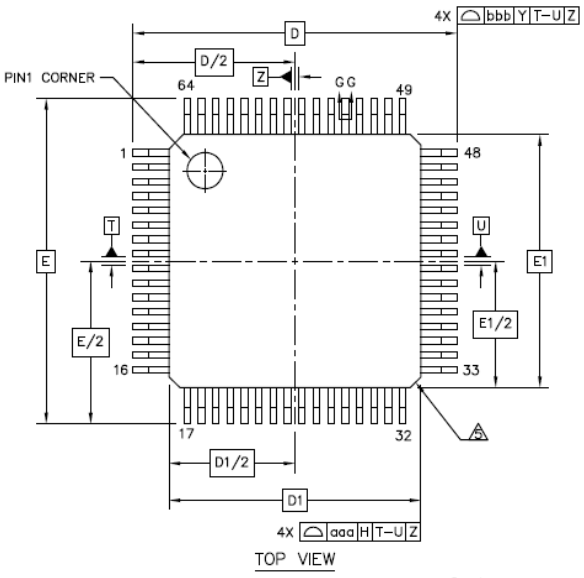
9.1 LQFP 100L (14x14x1.4 mm footprint 2.0 mm)



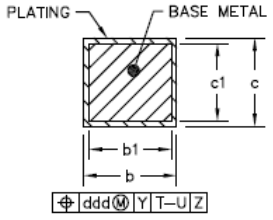
Controlling Dimension : Millimeters

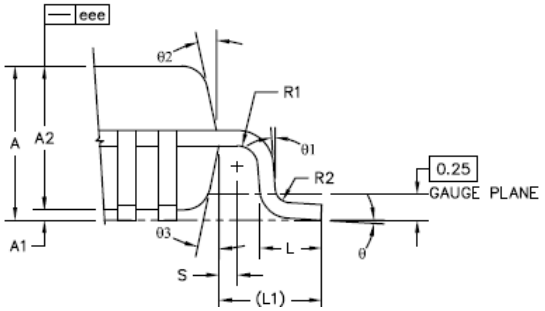
SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	-
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.10	0.15	0.20
D	13.90	14.00	14.10
E	13.90	14.00	14.10
e	-	0.50	-
HD	15.80	16.00	16.20
HE	15.80	16.00	16.20
L	0.45	0.60	0.75
L1	-	1	-
y	-	-	0.10
θ	0°	-	7°

9.2 LQFP 64L (7x7x1.4 mm footprint 2.0 mm)

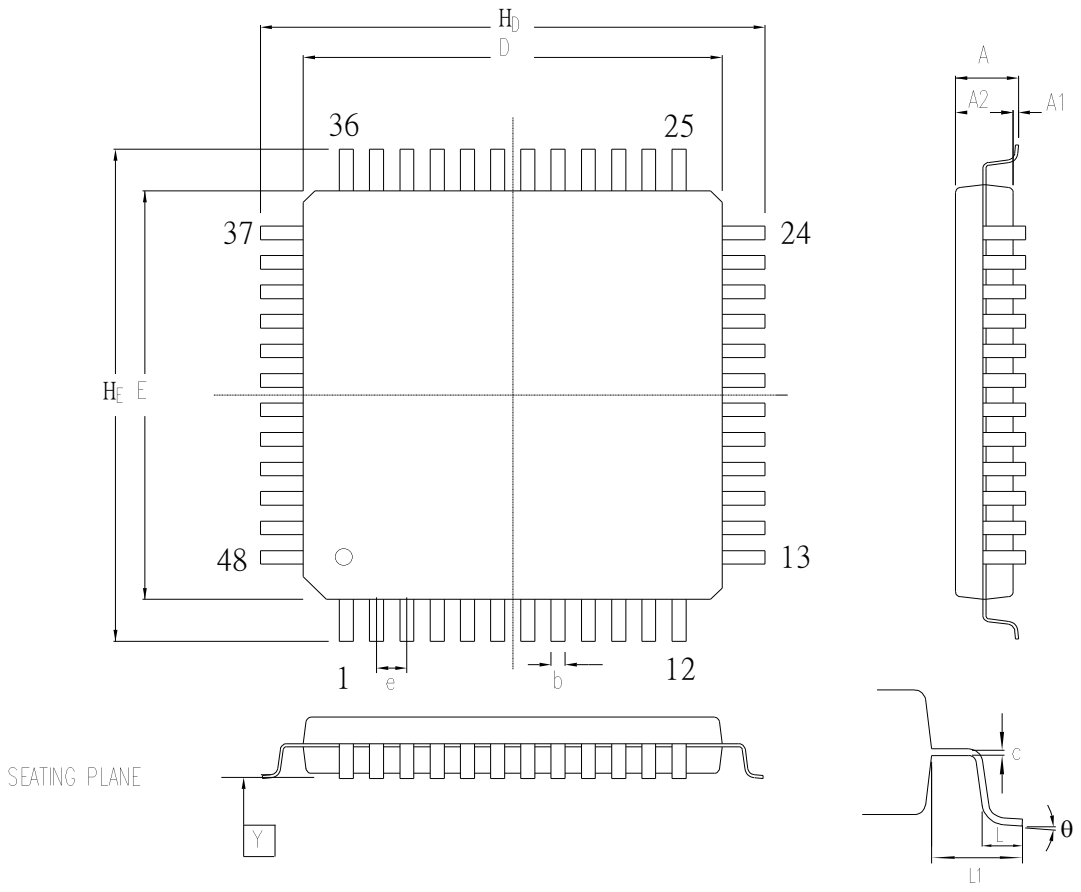


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		





9.3 LQFP 48L (7x7x1.4mm2 Footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7

10 REVISION HISTORY

Date	Revision	Description
2017.05.05	1.00	Preliminary version
2018.08.20	1.01	1. Revised V_{DDIO} description in section 1.1 and 4.1.2. 2. Revised Timer/PWM PWM mode description in section 2.1. 3. Revised $I_{PWD4,}$ MIN sink current/source current in section 8.2 4. Revised- the range of Xin_V_{IH} and Xin_V_{IL} in section 8.3.3 5. Revised LVR in section 8.4.5 6. Revised BOD in section 8.4.6 7. Removed block diagrams in section 6.10, 6.23 and 6.24. 8. Removed function descriptions in section 6.16 and 6.17.

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