

ARM[®] Cortex[®]-M0
32-bit Microcontroller

NuMicro[®] Family
M051 DN/DE Series
Product Brief

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1 GENERAL DESCRIPTION

The NuMicro® M051 DN/DE series 32-bit microcontroller is embedded with ARM® Cortex®-M0 core for industrial control and applications which need rich communication interfaces. The NuMicro® M051 DN/DE series includes the following part numbers: M052xDN/xDE, M054xDN/xDE, M058xDN/xDE and M0516xDN/xDE.

The NuMicro® M051 DN/DE series can run up to 50 MHz and operate at 2.5V ~ 5.5V, -40°C ~ 85°C, while M05xxDE operates at -40°C ~ 105°C, and thus can afford to support a variety of industrial control and applications which need high CPU performance. The NuMicro® M051 DN/DE series offers 8/16/32/64 KB flash, 4 KB Data Flash, 4 KB flash for the ISP, and 4 KB SRAM.

Many system level peripheral functions, such as I/O Port, EBI (External Bus Interface), Timer, UART, SPI, I²C, PWM, ADC, Watchdog Timer, Window Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into The NuMicro® M051 DN/DE series in order to reduce component count, board space and system cost. These useful functions make The NuMicro® M051 DN/DE series powerful for a wide range of applications.

Additionally, the NuMicro® M051 DN/DE series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, and IAP (In-Application Programming), which allow the user to update the program memory without removing the chip from the actual end product.

Item	M05xxBN	M05xxDN	M05xxDE
Operating Temperature	-40°C ~ 85°C	-40°C ~ 85°C	-40°C ~ 105°C
Hardware Divider	-	●	●
IAP Mode	-	●	●
Window WDT	-	●	●
Analog Comparators	2	4	4
Configurable I/O mode after POR	-	●	●
I ² C	1	2 (Supports Wake-up)	2 (Supports Wake-up)
SPI	- Only Supports HCLK as SPI clock source - No FIFO	- Supports HCLK and PLL as SPI clock source - 4-level FIFO	- Supports HCLK and PLL as SPI clock source - 4-level FIFO
PWM and ADC	PWM cannot trigger ADC	- PWM can trigger ADC conversion	- PWM can trigger ADC conversion

Table 1-1 M05xxBN, M05xxDN and M05xxDE Difference List

2 FEATURES

- Core
 - ARM® Cortex®-M0 core running up to 50 MHz
 - One 24-bit system timer
 - Supports Low Power Sleep mode
 - A single-cycle 32-bit hardware multiplier
 - NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - Supports Serial Wire Debug (SWD) interface and two watchpoints/four breakpoints
 - Provides hardware divider and supports signed 32-bit dividend, 16-bit divisor operation
- Wide Operating Voltage Range: 2.5V to 5.5V
- Memory
 - 8KB/16KB/32KB/64KB Flash for program memory (APROM)
 - 4KB Flash for data memory (Data Flash)
 - 4KB Flash for loader (LDROM)
 - 4KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
 - Programmable system clock source
 - 22.1184 MHz internal oscillator
 - 4~24 MHz external crystal input
 - 10 kHz low-power oscillator for Watchdog Timer and wake-up in Sleep mode
 - PLL allows CPU operation up to the maximum 50 MHz
- I/O Port
 - Up to 40 general-purpose I/O (GPIO) pins for LQFP-48 package
 - Four I/O modes:
 - ◆ Quasi-bidirectional
 - ◆ Push-Pull output
 - ◆ Open-Drain output
 - ◆ Input only with high impedance
 - TTL/Schmitt trigger input selectable
 - I/O pin can be configured as interrupt source with edge/level setting
 - Supports high driver and high sink I/O mode
 - Configurable I/O mode after POR
- Timer
 - Provides four channel 32-bit timers; one 8-bit pre-scale counter with 24-bit up-timer for each timer
 - Independent clock source for each timer
 - 24-bit timer value is readable through TDR (Timer Data Register)
 - Provides One-shot, Periodic and Toggle operation modes
 - Provides event counter function
 - Provides external capture/reset counter function
 - Two more timer clock sources from external trigger and internal 10 kHz
 - TIMER wake-up function
 - External capture input source selected from ACMP or TxEX
 - Toggle mode output pins selected from TxEX or TMx
 - Inter-Timer trigger mode
- WDT (Watchdog Timer)

- Multiple clock sources
- Supports wake-up from Power-down or Sleep mode
- Interrupt or reset selectable on watchdog time-out
- Time-out reset delay period time can be selected
- WWDT (Window Watchdog Timer)
 - 6-bit down counter with 11-bit pre-scale for wide range window selected
- PWM
 - Up to four built-in 16-bit PWM generators, providing eight PWM outputs or four complementary paired PWM outputs
 - Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
 - PWM interrupt synchronized to PWM period
 - 16-bit digital Capture timers with rising/falling capture inputs
 - Supports capture interrupt
 - Internal 10 kHz to PWM clock source
 - Polar inverse function
 - Center-aligned type function
 - Timer duty interrupt enable function
 - Two kinds of PWM interrupt period/duty type selection
 - Period/duty trigger ADC function
 - PWM Timer synchronous start function
- UART
 - Up to two sets of UART devices
 - Programmable baud-rate generator
 - Buffered receiver and transmitter, each with 15 bytes FIFO
 - Optional flow control function (CTS and RTS)
 - Supports IrDA(SIR) function
 - Supports RS485 function
 - Supports LIN function
- SPI
 - Up to two sets of SPI devices
 - Supports Master/Slave mode
 - Full-duplex synchronous serial data transfer
 - Provides 3 wire function
 - Variable length of transfer data from 1 to 32 bits
 - MSB or LSB first data transfer
 - Rx latching data can be either at rising edge or at falling edge of serial clock
 - Tx sending data can be either at rising edge or at falling edge of serial clock
 - Supports Byte Suspend mode in 32-bit transmission
 - PLL clock source
 - 4-level depth FIFO buffer for better performance and flexibility in SPI Burst Transfer mode

- I²C
 - Up to two sets of I²C modules
 - Supports Master/Slave mode
 - Bidirectional data transfer between master and slave
 - Multi-master bus (no central master)
 - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
 - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
 - Programmable clocks allow versatile rate control
 - Supports multiple address recognition (four slave addresses with mask option)
- ADC
 - 12-bit SAR ADC
 - Up to 8-ch single-ended input or 4-ch differential input
 - Supports Single mode/Burst mode/Single-cycle Scan mode/Continuous Scan mode
 - Supports 2' complement/un-signed format in differential mode conversion results
 - Each channel with an individual result register
 - Supports conversion value monitoring (or comparison) for threshold voltage detection
 - Conversion started either by software trigger or external pin trigger
 - A/D conversion started by PWM center-aligned trigger or edge-aligned trigger
 - PWM trigger delay function
 - Supports conversion result with signed format in Differential input and Burst mode
- Analog Comparator
 - Up to four sets of Comparator analog modules
 - External input or internal band-gap voltage selectable at negative node
 - Interrupt when compared results change
 - Power-down wake-up
- EBI (External Bus Interface) for external memory-mapped device access
 - Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
 - Supports 8-bit or 16-bit data width
 - Supports byte-write in 16-bit data width
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- IAP (In-Application Programming)
- One built-in temperature sensor with 1°C resolution
- BOD (Brown-out Detector)
 - With 4 levels: 4.4V/3.7V/2.7V/2.2V
 - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
 - Threshold voltage level: 2.0V
- Operating Temperature:

- M05xxDN: -40°C ~85°C
- M05xxDE: -40°C ~105°C
- Packages:
 - Green package (RoHS)
 - 48-pin LQFP, 33-pin QFN

3 PARTS INFORMATION AND PIN CONFIGURATION

3.1 NuMicro® M051 Series M05xxDN Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity			COMP	PWM (16-Bit)	ADC (12-Bit)	WDT	WWDT	EBI	ISP/CP/IAP	Package	Operating Temperature Range(°C)
							UART	SPI	I ² C									
M052LDN	8	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +85
M052ZDN	8	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +85
M054LDN	16	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +85
M054ZDN	16	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +85
M058LDN	32	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +85
M058ZDN	32	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +85
M0516LDN	64	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +85
M0516ZDN	64	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +85

Table 5-2 NuMicro® M051 Series M05xxDN Product Selection Guide

3.2 NuMicro® M051 Series M05xxDE Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity			COMP	PWM (16-Bit)	ADC (12-Bit)	WDT	WWDT	EBI	ISP/ICP/IAP	Package	Operating Temperature Range(°C)
							UART	SPI	I ² C									
M052LDE	8	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +105
M052ZDE	8	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +105
M054LDE	16	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +105
M054ZDE	16	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +105
M058LDE	32	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +105
M058ZDE	32	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +105
M0516LDE	64	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +105
M0516ZDE	64	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +105

Table 5-2 NuMicro® M051 Series M05xxDE Product Selection Guide

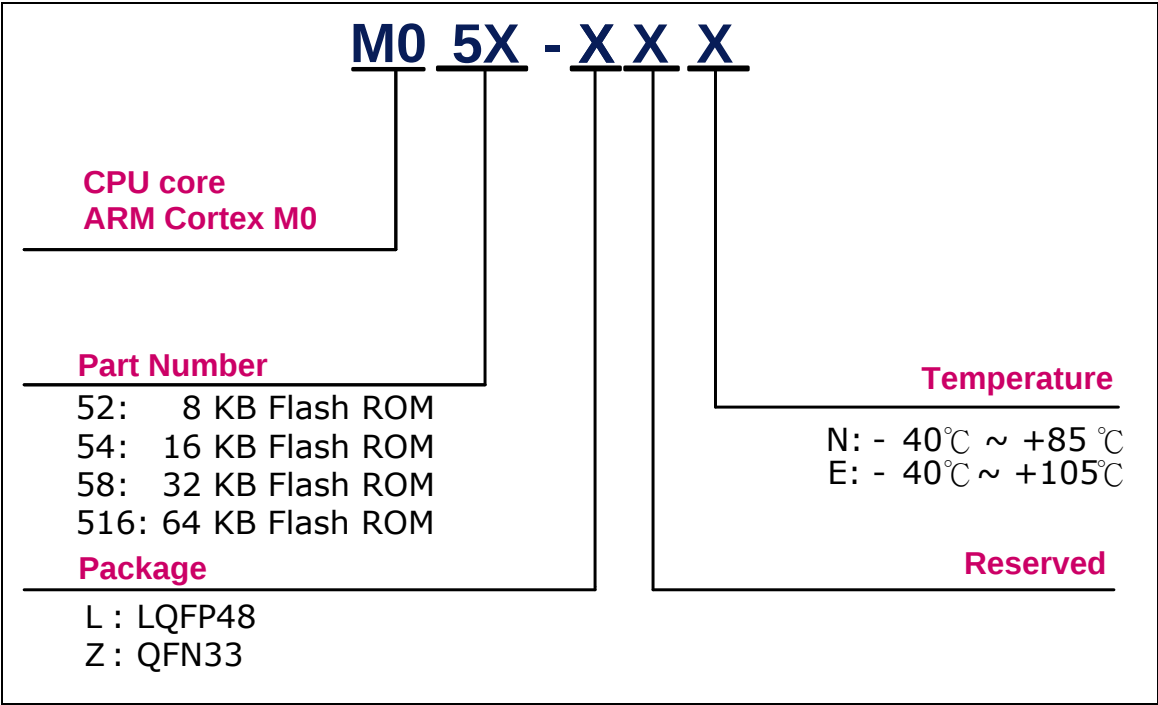


Figure 3-1 NuMicro® M051 DN/DE Series Naming Rule

3.3 Pin Diagrams

3.3.1 QFN 33-pin

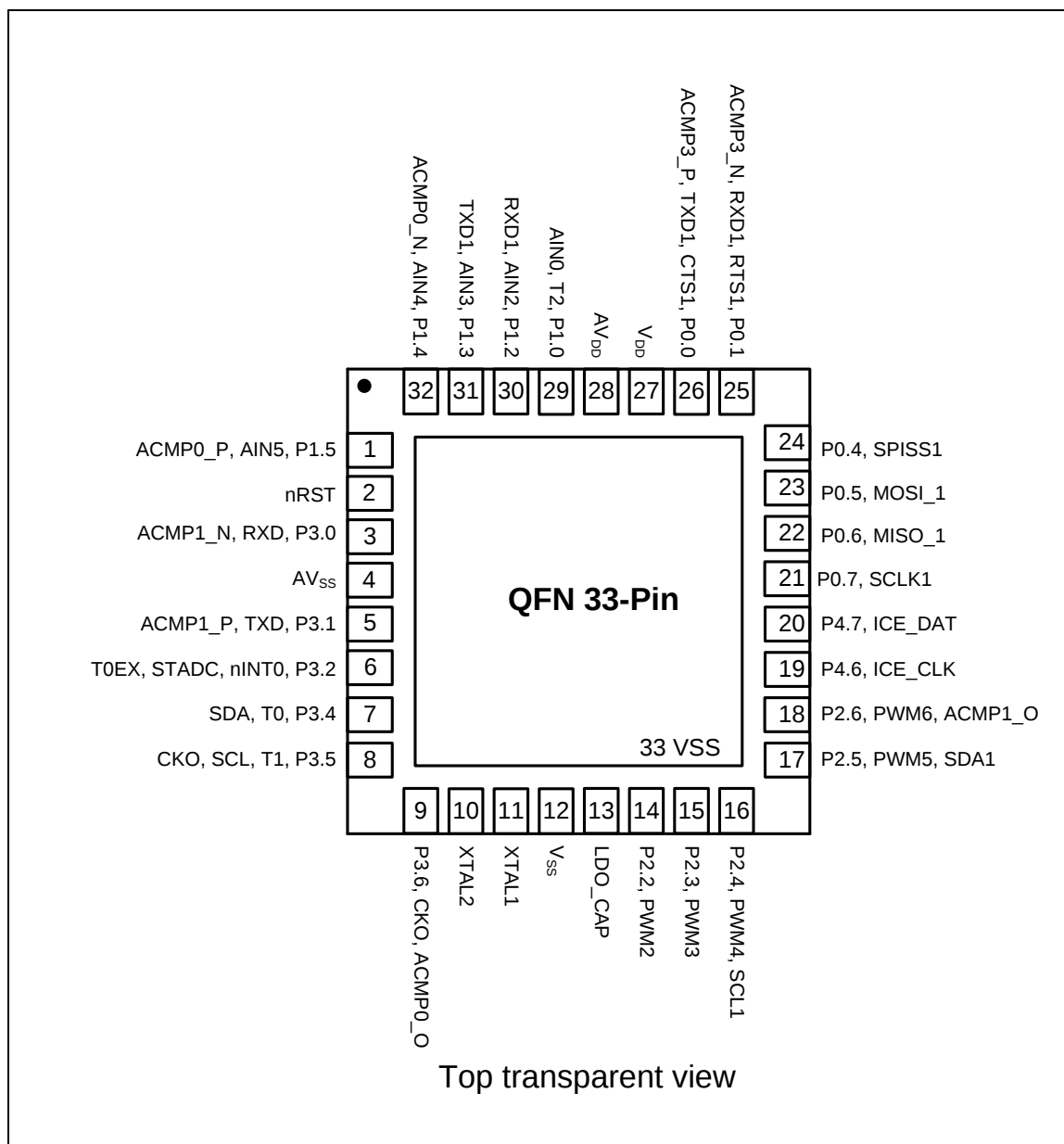


Figure 3-2 NuMicro® M051 DN/DE Series QFN-33 Pin Diagram

3.3.2 LQFP 48-pin

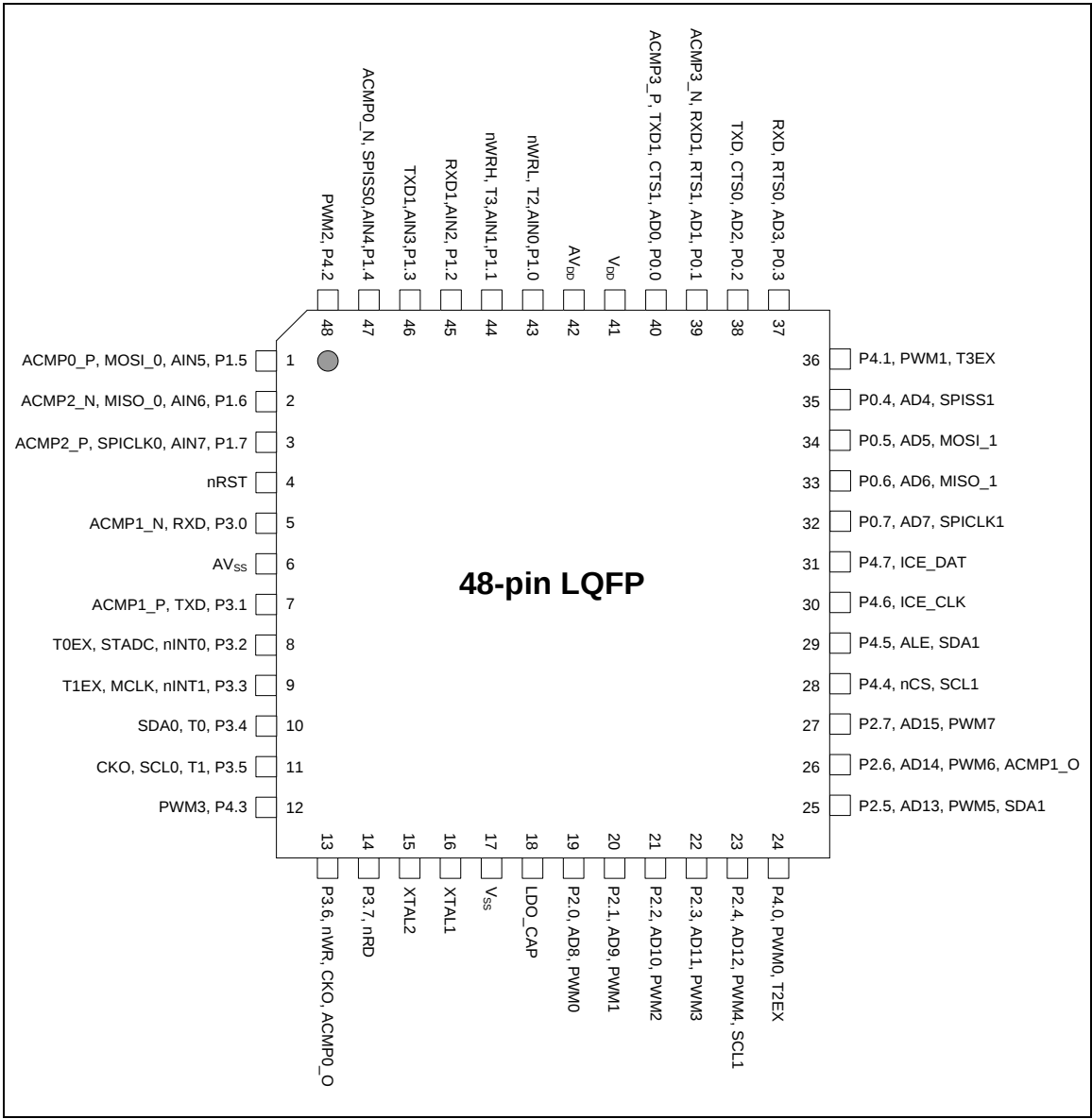


Figure 3-3 NuMicro® M051 DN/DE Series LQFP-48 Pin Diagram

4 BLOCK DIAGRAM

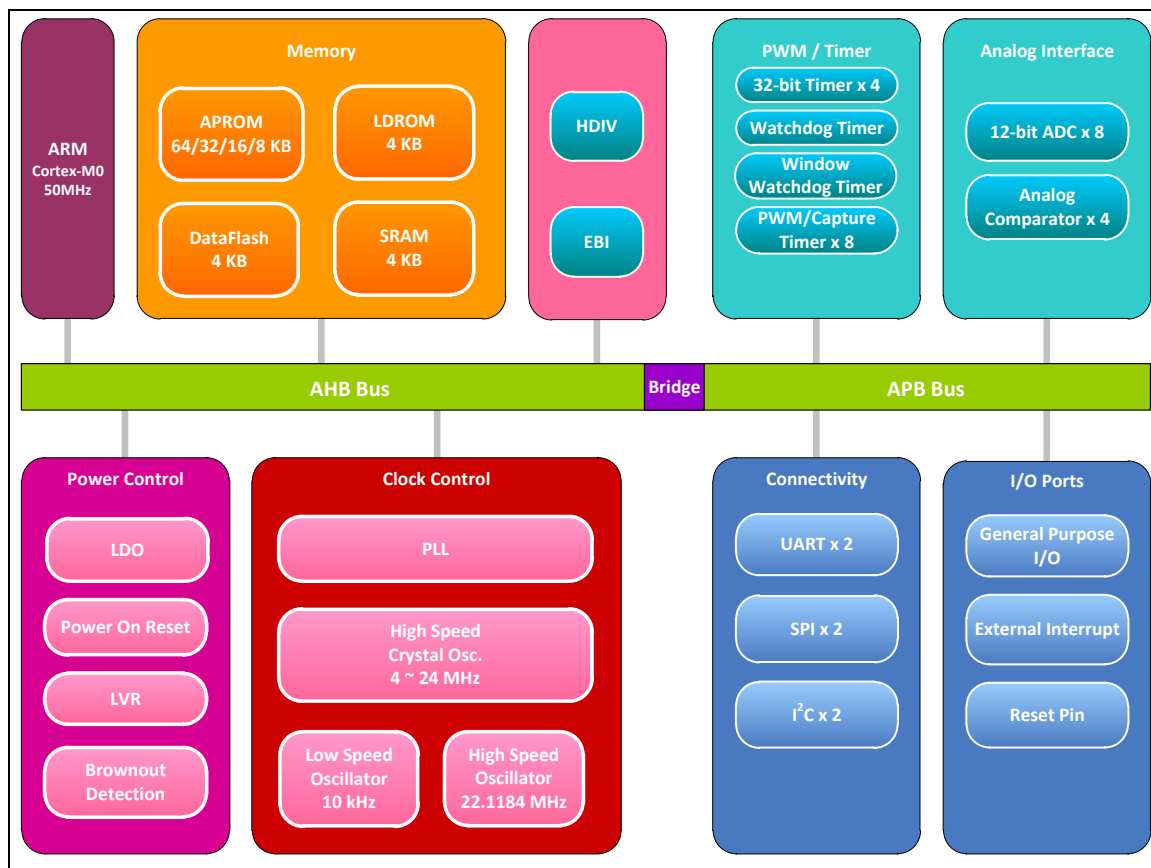
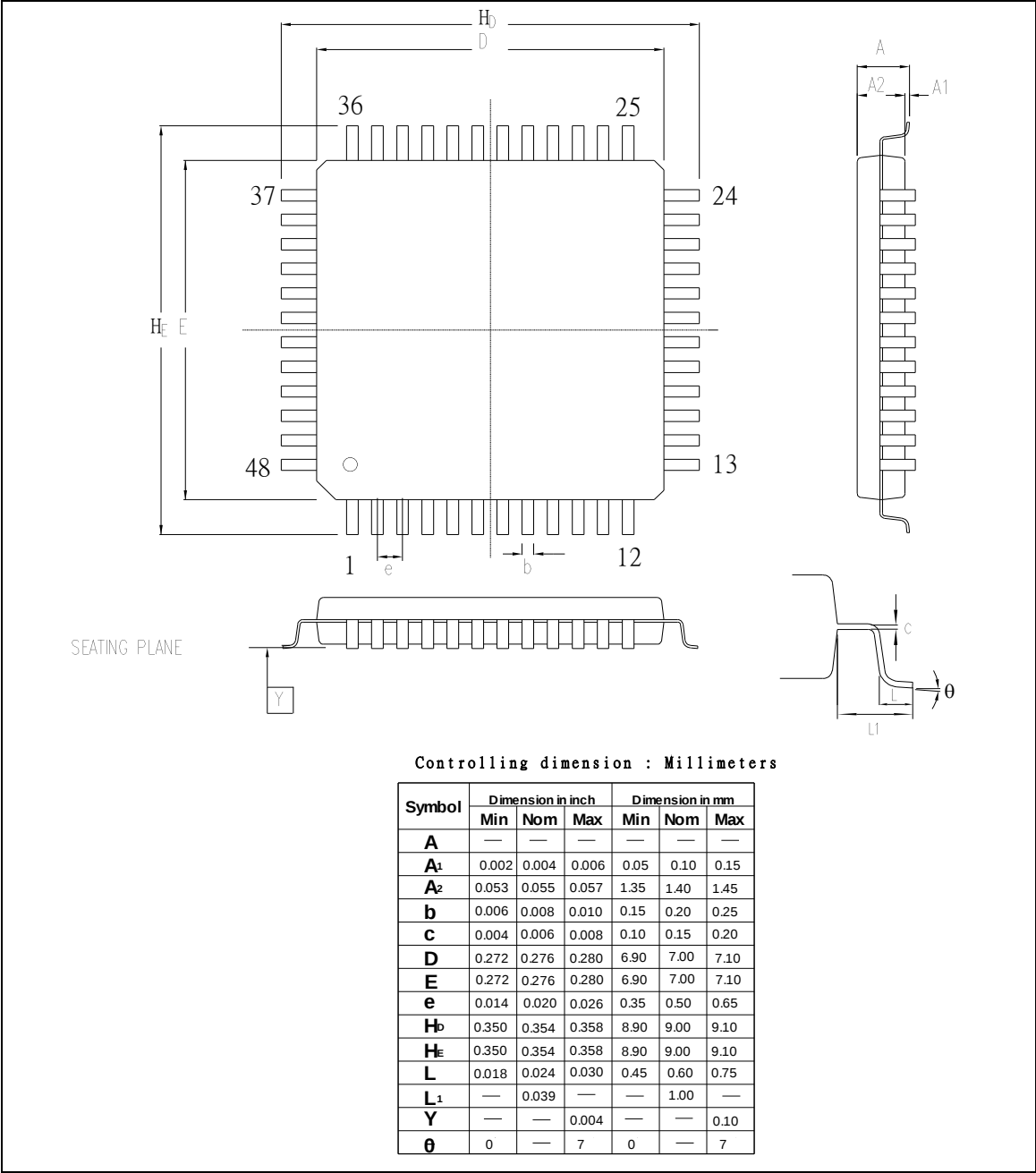


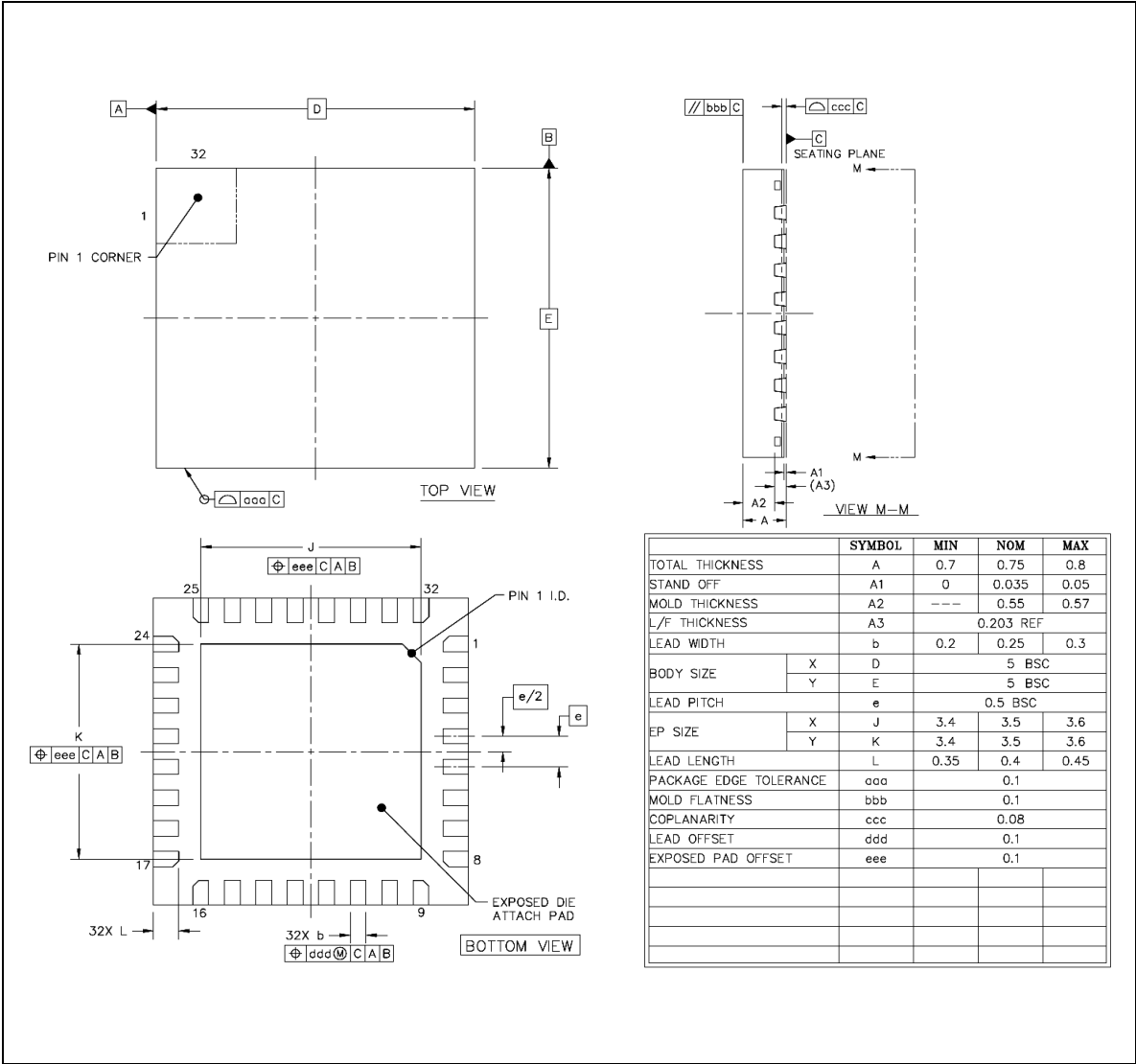
Figure 4-1 NuMicro® M051 DN/DE Series Block Diagram

5 PACKAGE DIMENSIONS

5.1 LQFP-48 (7x7x1.4mm² Footprint 2.0mm)



5.2 QFN-33 (5X5 mm², Thickness 0.8mm, Pitch 0.5 mm)



6 REVISION HISTORY

Date	Revision	Description
2013.09.15	1.00	1. Initially issued.
2015.05.12	1.01	1. Changed the order of Chapter 4 BLOCK DIAGRAM 2. Fixed typos and obscure description. 3. Fixed the number of COMP. sets in 3.1 NuMicro[®] M051 Series M05xxDN Selection Guide and 3.2 NuMicro[®] M051 Series M05xxDE Selection Guide 4. Removed description about ACMP output inverse function available on M05xxDN.
2015.10.05	1.02	1. Changed NuMicro[™] to NuMicro[®]. 2. Updated Figure 4-1 NuMicro[®] M051 DN/DE Series Block Diagram.

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