NuMicro® Family

Arm® Cortex-M0-based Microcontroller

M031BT/M032BT BLE MCU Series Datasheet

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1 GENERAL DESCRIPTION

The M031BT/M032BT series microcontroller (MCU) is based on Arm Cortex-M0 core with built-in Bluetooth Low Energy 5.0 (BLE 5.0) with rich peripherals and analog functions for applications that need wireless connectivity with multiple control functions. The M031BT/M032BT series is compliant with the BLE 5.0 standard supporting data rates up to 2 Mbps, offering 2.4 GHz proprietary stacks to achieve more possibility for wireless connectivity and Over-the-Air (OTA) for firmware upgrade. The M031BT/M032BT series solution allows those microcontroller applications to be the Internet of Things (IoT) devices with wireless connectivity.

The M031BT/M032BT series runs up to 72 MHz and features 64 Kbytes to 512 Kbytes Flash, 8 Kbytes to 96 Kbytes SRAM, 1.8V ~ 3.6V supply voltages, and supports 5V I/O tolerance within -40°C ~ 85°C operating temperature.

The M031BT/M032BT series provides a solution that need the connection with enhanced 2 MSPS fast conversion rate 12-bit ADC, 2 comparators and up to 24-ch 144 MHz PWM control. The M031BT/M032BT supports a fast and precise data conversion for the voltage, current, and sensor data, and fast response control to the external device. Additionally, the M031BT/M032BT series also provides plenty of peripherals including a Universal Serial Control Interface (USCI) that can be set as UART/SPI/I2C flexibly, 2 sets of I2C, up to 8 sets of UART, and 1-wire UART interface for data communication between master and slave devices. Moreover, part numbers with the M032BT series are all based on the M031BT series and enhanced with the crystal-less USB 2.0 full-speed device feature for USB related applications.

The M031BT series supports small form factor package QFN 48-pin (5 mm x 5 mm) that makes the PCB design to be compact size. The M032BT series offers QFN 68-pin (8 mm x 8 mm) for more functionality I/O control.

For the development, Nuvoton provides the NuMaker evaluation board and Nuvoton Nu-Link debugger. The 3rd Party IDE such as Keil MDK, IAR EWARM, Eclipse IDE with GNU GCC compilers are also supported.

USCI*: supports UART, SPI or I^2C

Product Line	UART	I^2C	Timer	USCI*	PWM	PDMA	ADC	ACMP	Divider	USBD	RTC
M031BT	3	2	4	1	12	5	16	2	1	-	-
M032BT	8	2	4	2	24	9	16	2	1	1	1

Table 1-1 NuMicro® M031BT/M032BT Series Key Features Support Table

The NuMicro® M031BT/M032BT series is suitable for a wide range of applications such as:

- IoT edge device
- Personal healthcare device with wireless connectivity
- Smart home appliances with remote control
- Assess tracking devices

2 FEATURES

2.1 M031BT/M032BT Features

Core and System	
Arm® Cortex®-M0	• Arm® Cortex®-M0 processor, running up to 72 MHz – 72 MHz at 2.0V-3.6V – 48 MHz at 1.8V-3.6V • Built-in Nested Vectored Interrupt Controller (NVIC) • 24-bit system tick timer • Programmble and maskable interrupt • Low Power Sleep mode by WFI and WFE instructions
Brown-out Detector (BOD)	• Two-level BOD with brown-out interrupt and reset option. (2.5V/2.0V)
Low Voltage Reset (LVR)	• LVR with 1.7V threshold voltage level.
Security	• 96-bit Unique ID (UID). • 128-bit Unique Customer ID (UCID).
32-bit H/W Divider(HDIV)	• Signed (two's complement) integer calculation • 32-bit dividend with 16-bit divisor calculation capacity • 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
Memories	
Flash	• Dual bank 512 KB on-chip Application ROM (APROM) for Over-The-Air (OTA) upgrade. • Up to 512 KB on-chip Application ROM (APROM). • Up to 8 KB on-chip Flash for user-defined loader (LDROM) • 512 bytes execution-only Security Protection ROM (SPROM) • All on-chip Flash support 512 bytes page erase • Fast Flash programming verification with CRC-32 checksum calculation • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • 2-wired ICP Flash updating through SWD/ICE interface
SRAM	• Up to 96 KB on-chip SRAM – 32 KB SRAM located in bank 0 that supports hardware parity check and retenion mode – 32/32 KB SRAM located in bank 1 and bank 2

	• Byte-, half-word- and word-access • PDMA operation
Cyclic Redundancy Calculation (CRC)	• Supports CRC-CCITT, CRC-8, CRC-16 and CRC-32 polynomials • Programmable initial value and seed value • Programmable order reverse setting and one's complement setting for input data and CRC checksum • 8-bit, 16-bit, and 32-bit data width • 8-bit write mode with 1-AHB clock cycle operation • 16-bit write mode with 2-AHB clock cycle operation • 32-bit write mode with 4-AHB clock cycle operation • Uses DMA to write data with performing CRC operation
Peripheral DMA (PDMA)	• Up to 9 independent and configurable channels for automatic data transfer between memories and peripherals • Basic and Scatter-Gather transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Fixed-priority and Round-robin priorities modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536 • Incremental or fixed source and destination address
Clocks	
External Clock Source	• 4~32 MHz High-speed eXternal crystal oscillator (HXT) for precise timing operation • 32.768 kHz Low-speed eXternal crystal oscillator (LXT) for RTC function and low-power system operation • 16/32 MHz eXternal crystal oscillator(RF_XTAL) for RF transceiver • Supports clock failure detection for external crystal oscillators and exception generatation (NMI)
Internal Clock Source	• 48 MHz High-speed Internal RC oscillator (HIRC) dedicated for crystal-less USB. • 38.4 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation • 32 kHz low-power on-chip RC oscillator for RF transceiver with deviation less than ± 500 ppm • Up to 144 MHz on-chip PLL, sourced from HIRC or HXT, allows CPU operation up to the maximim CPU frequency without the need for a high-frequency crystal
Real-Time Clock (RTC)	• The RTC clock source includes Low-speed external crystal oscillator (LXT)

	• Able to wake up CPU from idle or power-down mode • Supports ±5ppm within 5 seconds software clock accuracy compensation • Supports Alarm registers (second, minute, hour, day, month, year) • Supports RTC Time Tick and Alarm Match interrupt • Automatic leap year recognition • Supports 1 Hz clock output for calibration
Timers	
32-bit Timer	• Up to 4 sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle and Continuous Counting operation modes • Supports event counting function to count the event from external pins • Supports external capture pin for interval measurement and resetting 24-bit up counter • Supports chip wake-up function, if a timer interrupt signal is generated
PWM (PWM)	• Up to two PWM modules, each module provides three 16-bit counter and 6 output channels. • Up to 12 independent input capture channels with 16-bit resolution counter • Supports dead time with maximum divided 12-bit prescale • Up, down or up-down PWM counter type • Supports complementary mode for 3 complementary paired PWM output channels • Counter synchronous start function • Brake function with auto recovery mechanism • Mask function and tri-state output for each PWM channel • Able to trigger ADC to start conversion
Basic PWM (BPWM)	• Two 16-bit counters with 12-bit clock prescale for twelve 144 MHz PWM output channels. • Up to 6 independent input capture channels with 16-bit resolution counter • Up, down or up-down PWM counter type • Counter synchronous start function • Mask function and tri-state output for each PWM channel • Able to trigger ADC to start conversion
Watchdog	• 20-bit free running up counter for WDT time-out interval • Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT with 9 selectable time-out period

	• Able to wake up system from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset.
Window Watchdog	• Clock sourced from HCLK/2048 or LIRC; the window set by 6-bit counter with 11-bit prescale • Suspended in Idle/Power-down mode
Analog Interfaces	
ADC	• Analog input voltage range: 0 ~ AV_{DD} • One 12-bit, 2 MSPS SAR ADC with up to 16 single-ended input channels or 8 differential input pairs; 10-bit accuracy is guaranteed. • Internal channels for band-gap V_{BG} input. • Supports calibration capability. • Four operation modes: Single mode, Burst mode, Single-cycle Scan mode and Continuous Scan mode. • Analog-to-Digital conversion can be triggered by software enable (ADST), external pin (STADC), Timer 0~3 overflow pulse trigger, PWM trigger or BPWM trigger. • Each conversion result is held in data register of each channel with valid and overrun indicators. • Supports conversion result monitor by compare mode function. • Configurable ADC external sampling time. • PDMA operation. • Supports floating detect function.
Analog Comparator (ACMP)	• Two Analog Comparators • Supports three multiplexed I/O pins at positive input • Supports I/O pins, band-gap, and 16-level Voltage divider from AV_{DD} at negative input • Supports wake up from Power-down by interrupt • Supports triggers for brake events and cycle-by-cycle control for PWM • Supports window compare mode and window latch mode • Supports hysteresis function • Supports calibration function
Radio	• Modem with Integrated RF Radio for 2.4 GHz Bluetooth communication link • Compliant with Bluetooth 5 Low Energy Specification • Supports proprietary 2.4 GHz protocols • TX power: -20 to +8 dBm for M031BT series / +6 dBm for M032BT

	series in BLE mode • Rx Sensitivity: -94 dBm for M031BT series / -93 dBm for M032BT series (1 Mbps BLE mode) • Immune to interference (image rejection, -25dBm) • Data rate: 1Mbps and 2Mbps • Integrated security: CRC, AES-128, AES-CCM for real-time processing of the data stream • RSSI read-out • Two power supply modes (DC-DC converter and LDO regulator) for RF transceiver
Communication Interfaces	
Low-power UART	• Low-power UARTs with up to 7.2 MHz baud rate. • Auto-Baud Rate measurement and baud rate compensation function. • Supports low power UART (LPUART): baud rate clock from LXT (32.768 kHz) with 9600bps in Power-down mode even system clock is stopped. • 16-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function • Supports RS-485 9-bit mode and direction control • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode. • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • Supports wake-up function • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function • PDMA operation. • Supports Single-wire function mode.
I^2C	• Two sets of I^2C devices with Master/Slave mode. • Supports Standard mode (100 kbps), Fast mode (400 kbps), Fast mode plus (1 Mbps) • Supports 7 bits mode • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports multi-address power-down wake-up function

	• PDMA operation • I²C Port0 supports SMBus and PMBus
Quad SPI	• SPI Quad controller with Master/Slave mode. • Up to 24 MHz in Master mode and up to 16 MHz in Slave mode at 1.8V~3.6V system voltage. • Supports Dual and Quad I/O Transfer mode. • Supports one data channel half-duplex transfer. • Supports receive-only mode. • Configurable bit length of a transfer word from 8 to 32-bit. • Provides separate 8-level depth transmit and receive FIFO buffers. • Supports MSB first or LSB first transfer sequence. • Supports the byte reorder function. • Supports Byte or Word Suspend mode. • Supports 3-wired, no slave select signal, bi-direction interface. • PDMA operation. • Supports 2-bit Transfer mode.
SPI	• Dedicated SPI controller for RF transceiver. • Up to 16 MHz at 1.8V~3.6V system voltage. • Configurable bit length of a transfer word from 8 to 32-bit. • Provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers. • MSB first or LSB first transfer sequence. • Byte reorder function. • Supports Byte or Word Suspend mode. • Supports one data channel half-duplex transfer. • Supports receive-only mode. • PDMA operation. •
Universal Serial Control Interface (USCI)	• Two sets of USCI, configured as UART, SPI or I²C function. • Supports single byte TX and RX buffer mode **UART** • Supports one transmit buffer and two receive buffers for data payload. • Supports hardware auto flow control function and programmable flow control trigger level. • 9-bit Data Transfer. • Baud rate detection by built-in capture event of baud rate generator.

	• Supports wake-up function. • PDMA operation. **SPI** • Supports Master or Slave mode operation. • Supports one transmit buffer and two receive buffer for data payload. • Configurable bit length of a transfer word from 4 to 16-bit. • Supports MSB first or LSB first transfer sequence. • Supports Word Suspend function. • Supports 3-wire, no slave select signal, bi-direction interface. • Supports wake-up function: input slave select transition. • PDMA operation. • Supports one data channel half-duplex transfer. **I^2C** • Supports master and slave device capability. • Supports one transmit buffer and two receive buffer for data payload. • Communication in standard mode (100 kbps), fast mode (up to 400 kbps), and Fast mode plus (1 Mbps). • Supports 7-bit mode (10-bit mode not supported). • Supports 10-bit bus time out capability. • Supports bus monitor mode. • Supports power-down wake-up by data toggle or address match. • Supports multiple address recognition. • Supports device address flag. • Programmable setup/hold time.
	•
GPIO	• Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode. • Configured as interrupt source with edge/level trigger setting. • I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode. • Supports 5V-tolerance function except analog IO (PA.10, PA.11, PB.0~PB.15, PF.2~PF.5). • Enabling the pin interrupt function will also enable the wake-up function. • Input schmitt trigger function.
Advanced Connectivity	
USB 2.0 Full Speed with on-chip	• Compliant with USB Revision 2.0 Specification. • Supports suspend function when no bus activity existing for 3 ms.

transceiver	• 8 configurable endpoints for configurable Isochronous, Bulk, Interrupt and Control transfer types. • 512 bytes configurable RAM for endpoint buffer. • Remote wake-up capability. • Supports Crystal-less function • Start of Frame (SOF) locked clock pulse generation • USB 2.0 link power management.

3 PARTS INFORMATION

3.1 Package Type

Part No.	QFN48	QFN68
M031BTxD	M031BTYD2AN	
M031BTxE	M031BTYE3AN	
M032BTxG		M032BTAG8AN
M032BTxI		M032BTAIAAN

3.2 M031BT/M032BT Series Selection Guide

3.2.1 M031BT Series (M031BTYx)

Part Number		M031BT	
		YD2AN	YE3AN
Flash (KB)		64	128
SRAM (KB)		8	16
LDROM (KB)		2	4
SPROM(Bytes)		512	
System Frequency (MHz)		48	
PLL (MHz)		96	
I/O		29	
32-bit Timer		4	
Connectivity	USCI	1	
	UART	3	
	QSPI	-	
	I²C/SMBus	2/0	
	USB FS	-	
PWM		12	
BPWM		-	
PDMA		5	
CRC		√	
HDIV		√	
HXT		√	
LXT		√	
RTC		-	
Analog Comparator		2	
12-bit SAR ADC		16	
Package		QFN48	

3.2.2 M032BT USB Series (M032BTAx)

Part Number		M032BT	
		AG8AN	AIAAN
Flash (KB)		256	512
SRAM (KB)		64	96
LDROM (KB)		4	8
SPROM (Bytes)		2048	
System Frequency (MHz)		72	
PLL (MHz)		144	
I/O		43	
32-bit Timer		4	
Connectivity	USCI	2	
	UART	6	8
	QSPI	1	
	I²C/SMBus	2/1	
	USB FS	√	
PWM		12	
BPWM		12	
PDMA		7	9
CRC		√	
HDIV		√	
HXT		√	
LXT		√	
RTC		√	
Analog Comparator		2	
12-bit SAR ADC		16	
Package		QFN68	

3.2.3 Naming Rule

M0	32BT	A	I	A	A	N
Core	**Line**	**Package**	**Flash**	**SRAM**	**Reserve**	**Temperature**
Cortex®-M0	31BT: Base 32BT: USB	Y: QFN48 (5x5 mm) A: QFN68 (8x8 mm)	D: 64 KB E: 128 KB G: 256 KB I: 512 KB	2: 8 KB 3: 16 KB 8: 64 KB A: 96 KB		N:-40°C ~ 85°C

3.3 M031BT/M032BT Series Feature Comparison Table

Section	Sub-section	M031BTxD/E	M032BTxG/I
System Manager	6.3.6 SRAM Memory Organization	●	-
	6.3.7 SRAM Memory Organization with parity function	-	●
FMC	6.4.4.3 Physical and Virtual Address Concept	-	●
	6.4.4.4 APROM Reboot Address Operation Model Selection	-	-/●
	6.4.4.14 Cache Memory Controller	-	●
	6.4.4.15 Embedded Flash Memory Programming 64-bit Programming and Multi-word Programming	-	●
	6.4.4.17 Flash All-One Verification	-	●
	ISP Control Register (FMC_ISPCTL) INTEN (FMC_ISPCTL[24])	●	
ADC	6.25.5.11 PWM trigger	●	●
	6.25.5.12 BPWM trigger	-	●
	6.25.5.17 Floating Detect Function	-	●
I²C	6.16.5.2 Operation Modes - Bus Management (SMBus/PMBus Compatiable) - Device Identification – Slave Address - Bus Protocols - Address Resolution Protocol (ARP) - Received Command and Data acknowledge control - Host Notify Protocol - Bus Management Alert - Packet Error Checking - Time-out - Bus Management Time-out: - Bus Clock Low Time-out: - Bus Idle Detection	-	●
ACMP	6.26.5.7 Calibration function	-/●	●
USBD	6.22.7 Register Description USB Configuration Register (USB_CFGx) DSQSYNC OUT Token Transaction	-	-

4 PIN CONFIGURATION

Users can find pin configuaration informations in chapter 4 or by using NuTool - PinConfig. The NuTool - PinConfigure contains all Nuvoton NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1 Pin Configuration

4.1.1 M031BT Series Pin Diagram

4.1.1.1 M031BT Series QFN 48-Pin Diagram

Corresponding Part Number: M031BTD23AN, M031BTYE3AN

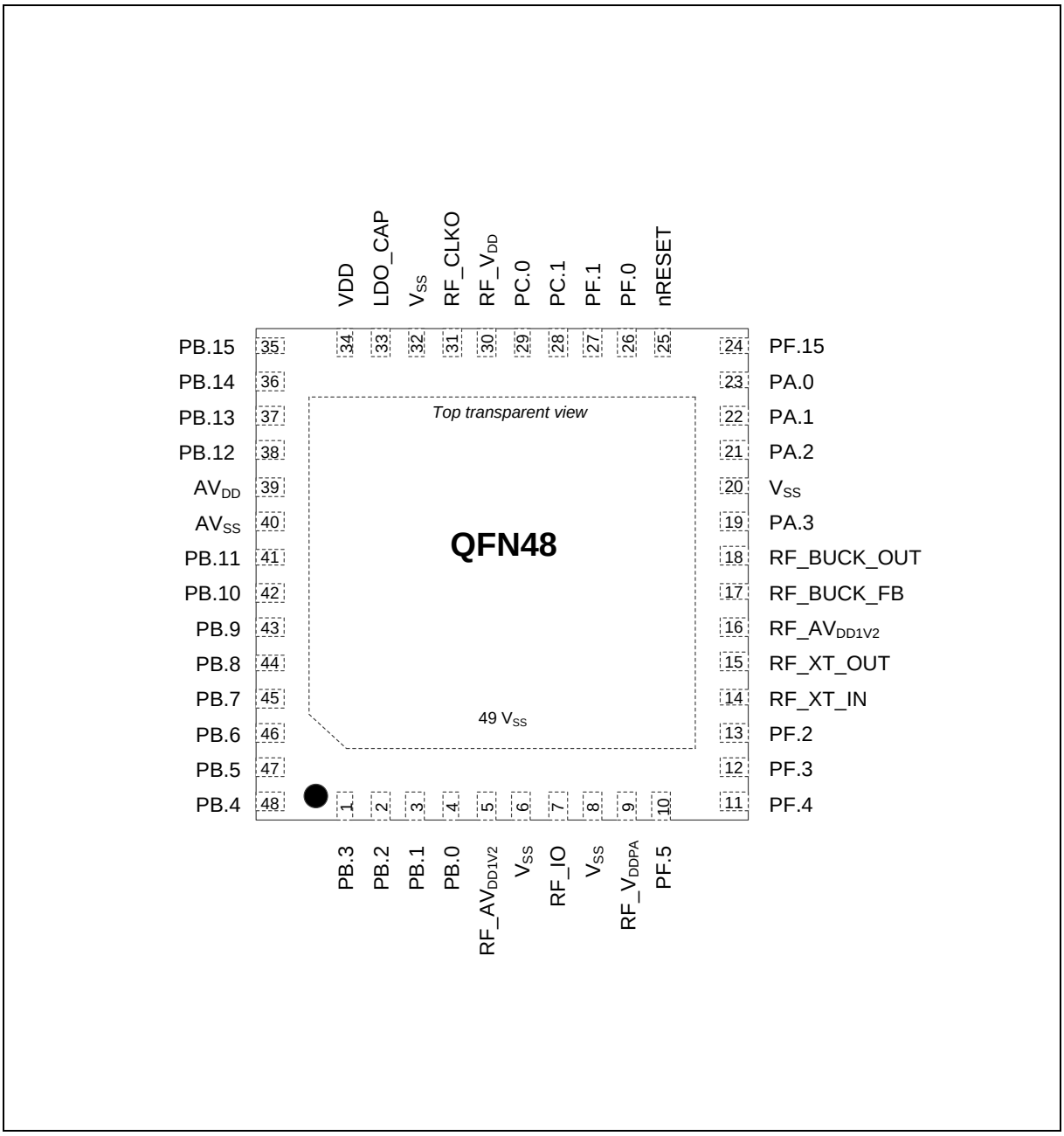


Figure 4.1-1 M031BT Series QFN 48-pin Diagram

4.1.2 M032BT Series Pin Diagram

4.1.2.1 M032BT Series QFN 68-Pin Diagram

Corresponding Part Number: M032BTAG8AN, M032BTAIAAN

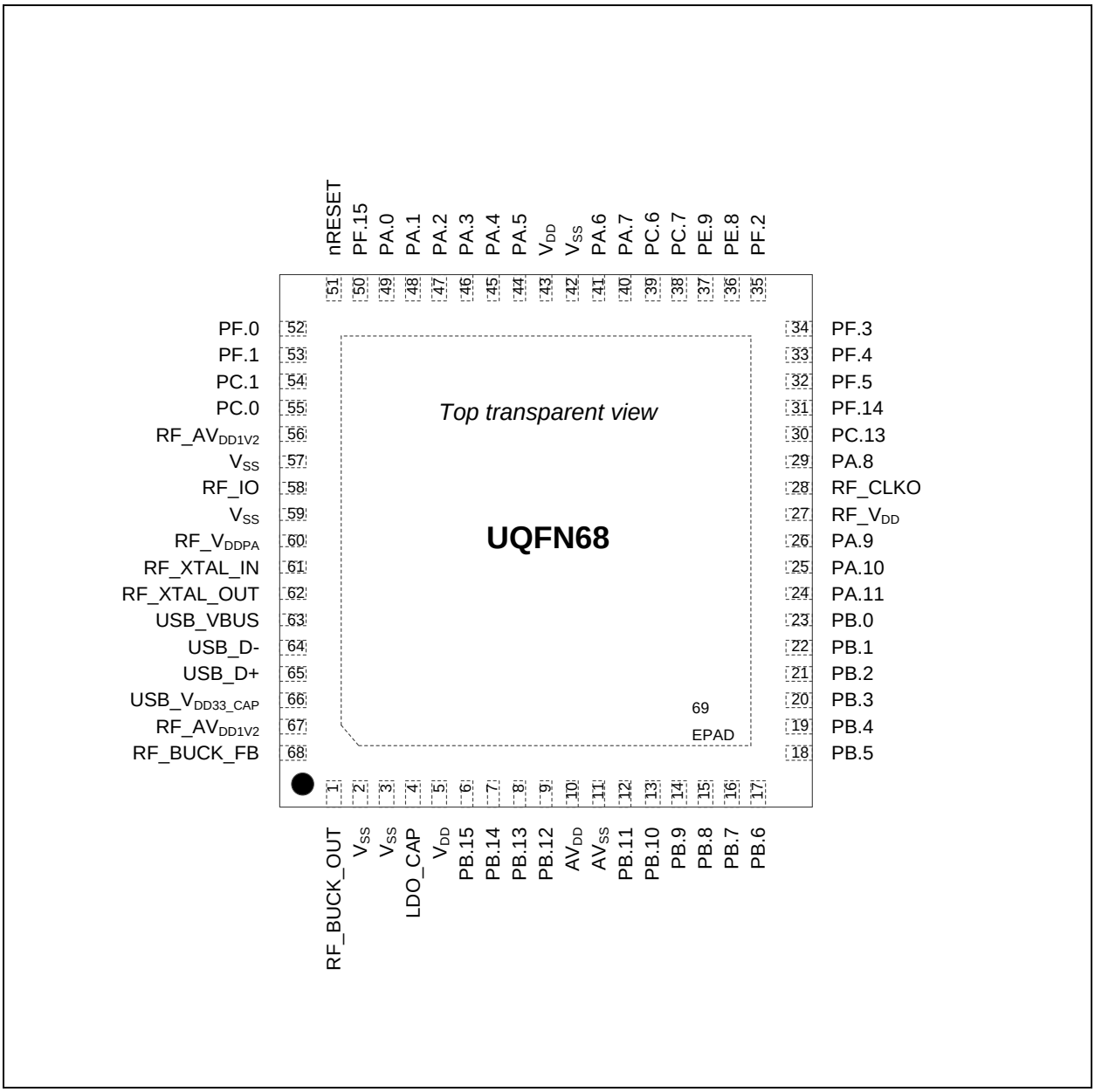


Figure 4.1-2 M032BT Series QFN 68-pin Diagram

4.1.3 M031BT Series Multi-function Pin Diagram

4.1.3.1 M031BT Series QFN 48-Pin Multi-function Pin Diagram

Corresponding Part Number: M031BTYD2AN, M031BTYE3AN

M031BTYD2AN, M031BTYE3AN

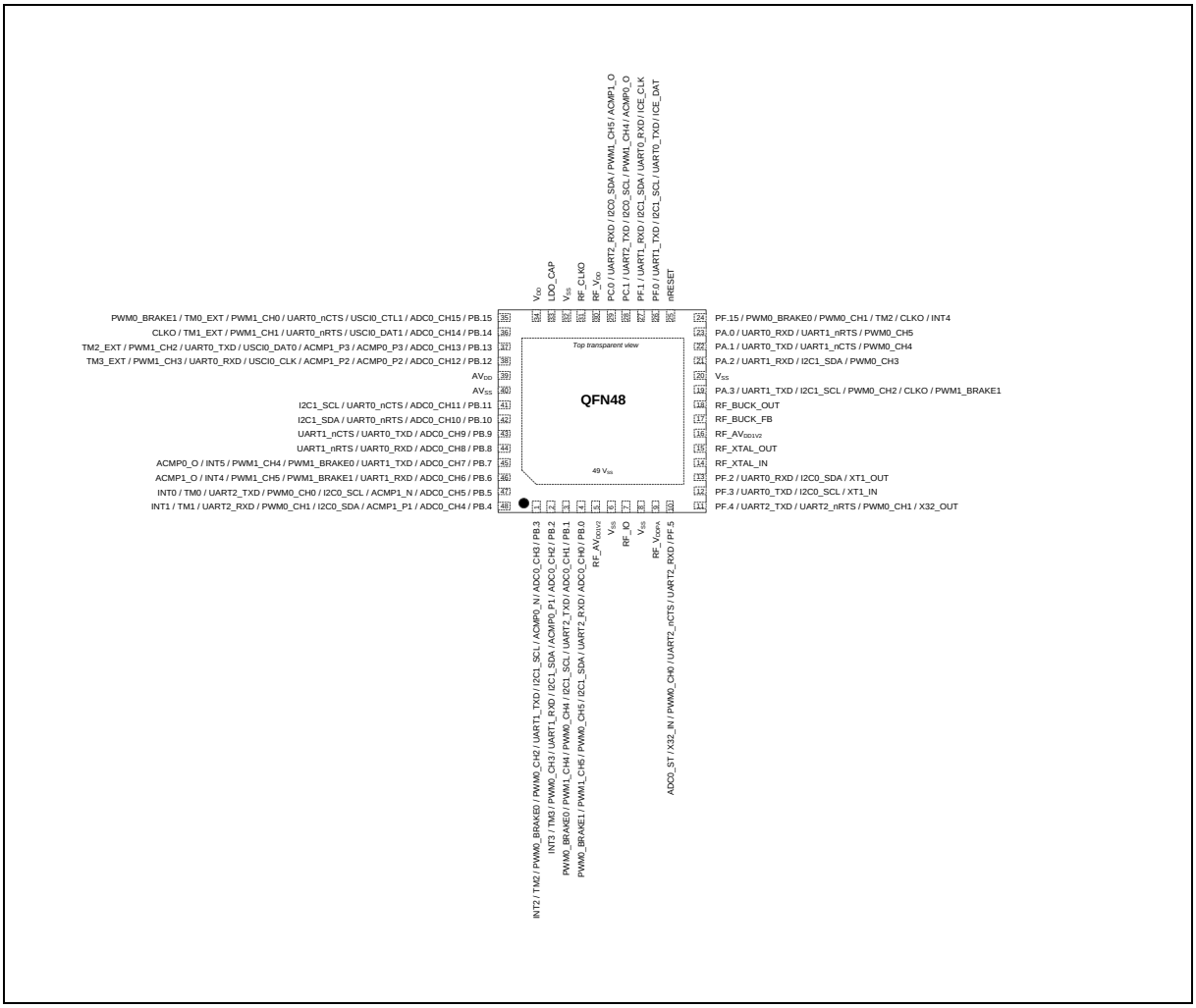


Figure 4.1-3 M031BTYD2AN / M031BTYE3AN Multi-function Pin Diagram

Pin	M031BTYD2AN / M031BTYE3AN Pin Function
1	PB.3 / ADC0_CH3 / ACMP0_N / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE0 / TM2 / INT2
2	PB.2 / ADC0_CH2 / ACMP0_P1 / I2C1_SDA / UART1_RXD / PWM0_CH3 / TM3 / INT3
3	PB.1 / ADC0_CH1 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0
4	PB.0 / ADC0_CH0 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1
5	RF_AV_{DD1V2}
6	V_{SS}
7	RF_IO
8	V_{SS}

Pin	M031BTYD2AN / M031BTYE3AN Pin Function
9	RF_V_{DDPA}
10	PF.5 / UART2_RXD / UART2_nCTS / PWM0_CH0 / X32_IN / ADC0_ST
11	PF.4 / UART2_TXD / UART2_nRTS / PWM0_CH1 / X32_OUT
12	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN
13	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT
14	RF_XTAL_IN
15	RF_XTAL_OUT
16	RF_AV_{DD1V2}
17	RF_BUCK_FB
18	RF_BUCK_OUT
19	PA.3 / UART1_TXD / I2C1_SCL / PWM0_CH2 / CLKO / PWM1_BRAKE1
20	V_{SS}
21	PA.2 / UART1_RXD / I2C1_SDA / PWM0_CH3
22	PA.1 / UART0_TXD / UART1_nCTS / PWM0_CH4
23	PA.0 / UART0_RXD / UART1_nRTS / PWM0_CH5
24	PF.15 / PWM0_BRAKE0 / PWM0_CH1 / TM2 / CLKO / INT4
25	nRESET
26	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
27	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK
28	PC.1 / UART2_TXD / I2C0_SCL / PWM1_CH4 / ACMP0_O
29	PC.0 / UART2_RXD / I2C0_SDA / PWM1_CH5 / ACMP1_O
30	RF_V_{DD}
31	RF_CLKO
32	V_{SS}
33	LDO_CAP
34	V_{DD}
35	PB.15 / ADC0_CH15 / USCI0_CTL1 / UART0_nCTS / PWM1_CH0 / TM0_EXT / PWM0_BRAKE1
36	PB.14 / ADC0_CH14 / USCI0_DAT1 / UART0_nRTS / PWM1_CH1 / TM1_EXT / CLKO
37	PB.13 / ADC0_CH13 / ACMP0_P3 / ACMP1_P3 / USCI0_DAT0 / UART0_TXD / PWM1_CH2 / TM2_EXT
38	PB.12 / ADC0_CH12 / ACMP0_P2 / ACMP1_P2 / USCI0_CLK / UART0_RXD / PWM1_CH3 / TM3_EXT
39	AV_{DD}
40	AV_{SS}
41	PB.11 / ADC0_CH11 / UART0_nCTS / I2C1_SCL
42	PB.10 / ADC0_CH10 / UART0_nRTS / I2C1_SDA

Pin	M031BTYD2AN / M031BTYE3AN Pin Function
43	PB.9 / ADC0_CH9 / UART0_TXD / UART1_nCTS
44	PB.8 / ADC0_CH8 / UART0_RXD / UART1_nRTS
45	PB.7 / ADC0_CH7 / UART1_TXD / PWM1_BRAKE0 / PWM1_CH4 / INT5 / ACMP0_O
46	PB.6 / ADC0_CH6 / UART1_RXD / PWM1_BRAKE1 / PWM1_CH5 / INT4 / ACMP1_O
47	PB.5 / ADC0_CH5 / ACMP1_N / I2C0_SCL / PWM0_CH0 / UART2_TXD / TM0 / INT0
48	PB.4 / ADC0_CH4 / ACMP1_P1 / I2C0_SDA / PWM0_CH1 / UART2_RXD / TM1 / INT1
49	EPAD (Vss)

Table 4.1-1 M031BTYD2AN / M031BTYE3AN Multi-function Pin Table

4.1.4 M032BT Series Multi-function Pin Diagram

4.1.4.1 M032BT Series QFN 68-Pin Multi-function Pin Diagram

Corresponding Part Number: M032BTAG8AN, M032BTAIAAN

M032BTAG8AN

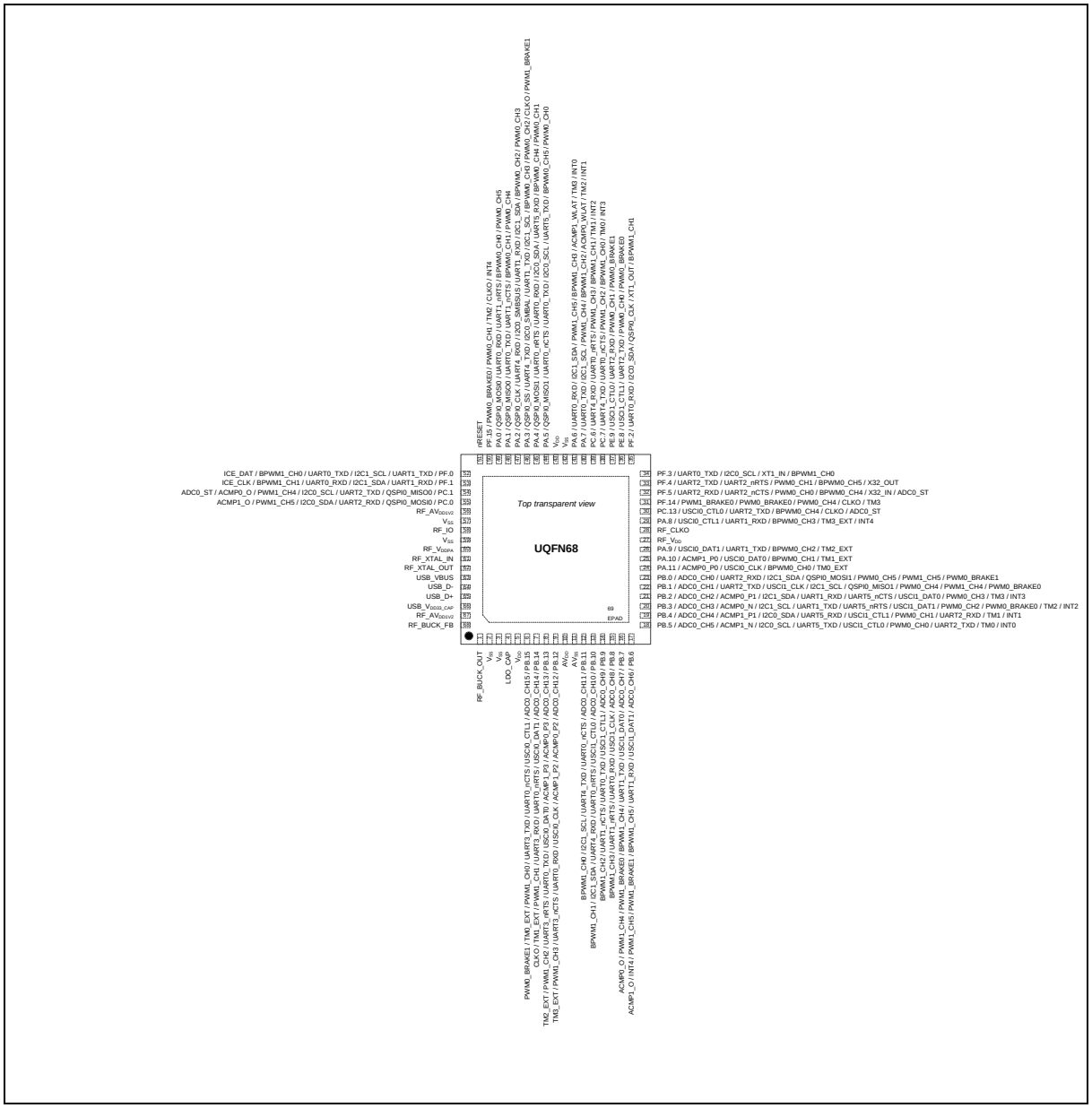


Figure 4.1-4 M032BTAG8AN Multi-function Pin Diagram

Pin	M032BTAG8AN Pin Function
1	RF_BUCK_OUT
2	V_{SS}
3	V_{SS}

Pin	M032BTAG8AN Pin Function
4	LDO_CAP
5	V_{DD}
6	PB.15 / ADC0_CH15 / USCI0_CTL1 / UART0_nCTS / UART3_TXD / PWM1_CH0 / TM0_EXT / PWM0_BRAKE1
7	PB.14 / ADC0_CH14 / USCI0_DAT1 / UART0_nRTS / UART3_RXD / PWM1_CH1 / TM1_EXT / CLKO
8	PB.13 / ADC0_CH13 / ACMP0_P3 / ACMP1_P3 / USCI0_DAT0 / UART0_TXD / UART3_nRTS / PWM1_CH2 / TM2_EXT
9	PB.12 / ADC0_CH12 / ACMP0_P2 / ACMP1_P2 / USCI0_CLK / UART0_RXD / UART3_nCTS / PWM1_CH3 / TM3_EXT
10	AV_{DD}
11	AV_{SS}
12	PB.11 / ADC0_CH11 / UART0_nCTS / UART4_TXD / I2C1_SCL / BPWM1_CH0
13	PB.10 / ADC0_CH10 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / BPWM1_CH1
14	PB.9 / ADC0_CH9 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / BPWM1_CH2
15	PB.8 / ADC0_CH8 / USCI1_CLK / UART0_RXD / UART1_nRTS / BPWM1_CH3
16	PB.7 / ADC0_CH7 / USCI1_DAT0 / UART1_TXD / BPWM1_CH4 / PWM1_BRAKE0 / PWM1_CH4 / ACMP0_O
17	PB.6 / ADC0_CH6 / USCI1_DAT1 / UART1_RXD / BPWM1_CH5 / PWM1_BRAKE1 / PWM1_CH5 / INT4 / ACMP1_O
18	PB.5 / ADC0_CH5 / ACMP1_N / I2C0_SCL / UART5_TXD / USCI1_CTL0 / PWM0_CH0 / UART2_TXD / TM0 / INT0
19	PB.4 / ADC0_CH4 / ACMP1_P1 / I2C0_SDA / UART5_RXD / USCI1_CTL1 / PWM0_CH1 / UART2_RXD / TM1 / INT1
20	PB.3 / ADC0_CH3 / ACMP0_N / I2C1_SCL / UART1_TXD / UART5_nRTS / USCI1_DAT1 / PWM0_CH2 / PWM0_BRAKE0 / TM2 / INT2
21	PB.2 / ADC0_CH2 / ACMP0_P1 / I2C1_SDA / UART1_RXD / UART5_nCTS / USCI1_DAT0 / PWM0_CH3 / TM3 / INT3
22	PB.1 / ADC0_CH1 / UART2_TXD / USCI1_CLK / I2C1_SCL / QSPI0_MISO1 / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0
23	PB.0 / ADC0_CH0 / UART2_RXD / I2C1_SDA / QSPI0_MOSI1 / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1
24	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT
25	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT
26	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
27	RF_V_{DD}
28	RF_CLKO
29	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
30	PC.13 / USCI0_CTL0 / UART2_TXD / BPWM0_CH4 / CLKO / ADC0_ST

Pin	M032BTAG8AN Pin Function
31	PF.14 / PWM1_BRAKE0 / PWM0_BRAKE0 / PWM0_CH4 / CLKO / TM3
32	PF.5 / UART2_RXD / UART2_nCTS / PWM0_CH0 / BPWM0_CH4 / X32_IN / ADC0_ST
33	PF.4 / UART2_TXD / UART2_nRTS / PWM0_CH1 / BPWM0_CH5 / X32_OUT
34	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0
35	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / BPWM1_CH1
36	PE.8 / USCI1_CTL1 / UART2_TXD / PWM0_CH0 / PWM0_BRAKE0
37	PE.9 / USCI1_CTL0 / UART2_RXD / PWM0_CH1 / PWM0_BRAKE1
38	PC.7 / UART4_TXD / UART0_nCTS / PWM1_CH2 / BPWM1_CH0 / TM0 / INT3
39	PC.6 / UART4_RXD / UART0_nRTS / PWM1_CH3 / BPWM1_CH1 / TM1 / INT2
40	PA.7 / UART0_TXD / I2C1_SCL / PWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
41	PA.6 / UART0_RXD / I2C1_SDA / PWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
42	V_{SS}
43	V_{DD}
44	PA.5 / QSPI0_MISO1 / UART0_nCTS / UART0_TXD / I2C0_SCL / UART5_TXD / BPWM0_CH5 / PWM0_CH0
45	PA.4 / QSPI0_MOSI1 / UART0_nRTS / UART0_RXD / I2C0_SDA / UART5_RXD / BPWM0_CH4 / PWM0_CH1
46	PA.3 / QSPI0_SS / UART4_TXD / I2C0_SMBAL / UART1_TXD / I2C1_SCL / BPWM0_CH3 / PWM0_CH2 / CLKO / PWM1_BRAKE1
47	PA.2 / QSPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / BPWM0_CH2 / PWM0_CH3
48	PA.1 / QSPI0_MISO0 / UART0_TXD / UART1_nCTS / BPWM0_CH1 / PWM0_CH4
49	PA.0 / QSPI0_MOSI0 / UART0_RXD / UART1_nRTS / BPWM0_CH0 / PWM0_CH5
50	PF.15 / PWM0_BRAKE0 / PWM0_CH1 / TM2 / CLKO / INT4
51	nRESET
52	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / BPWM1_CH0 / ICE_DAT
53	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / BPWM1_CH1 / ICE_CLK
54	PC.1 / QSPI0_MISO0 / UART2_TXD / I2C0_SCL / PWM1_CH4 / ACMP0_O / ADC0_ST
55	PC.0 / QSPI0_MOSI0 / UART2_RXD / I2C0_SDA / PWM1_CH5 / ACMP1_O
56	RF_AV_{DD1V2}
57	V_{SS}
58	RF_IO
59	V_{SS}
60	RF_V_{DDPA}

Pin	M032BTAG8AN Pin Function
61	RF_XTAL_IN
62	RF_XTAL_OUT
63	USB_VBUS
64	USB_D-
65	USB_D+
66	USB_V_{DD33_CAP}
67	RF_AV_{DD1V2}
68	RF_BUCK_FB
69	EPAD

Table 4.1-2 M032BTAG8AN Multi-function Pin Table

M032BTAIAAN

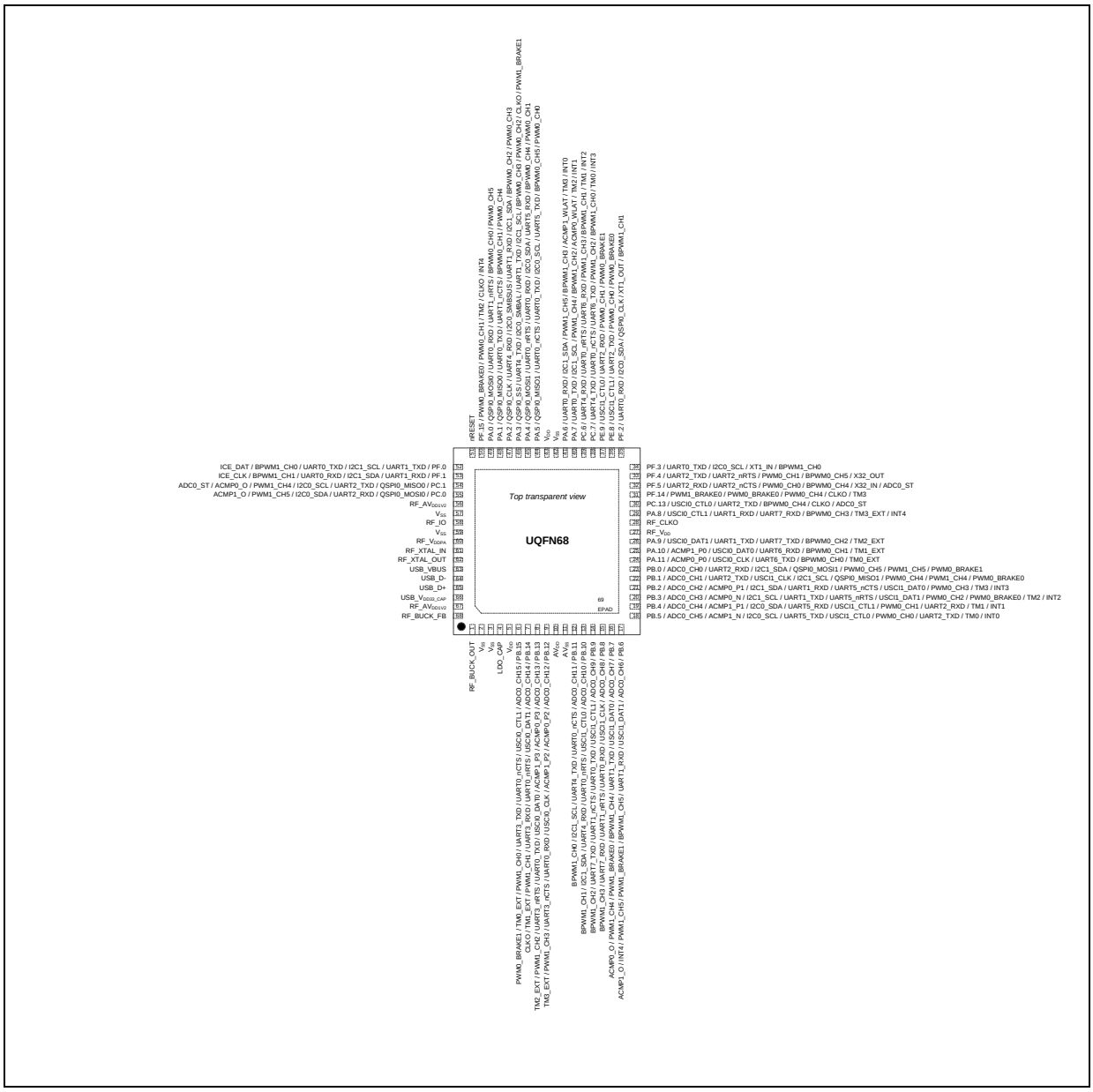


Figure 4.1-5 M032BTAG8AN / M032BTAIAAN Multi-function Pin Diagram

Pin	M032BTAIAAN Pin Function
1	RF_BUCK_OUT
2	V_{SS}
3	V_{SS}
4	LDO_CAP
5	V_{DD}
6	PB.15 / ADC0_CH15 / USCI0_CTL1 / UART0_nCTS / UART3_TXD / PWM1_CH0 / TM0_EXT / PWM0_BRAKE1
7	PB.14 / ADC0_CH14 / USCI0_DAT1 / UART0_nRTS / UART3_RXD / PWM1_CH1 / TM1_EXT / CLKO

Pin	M032BTAIAAN Pin Function
8	PB.13 / ADC0_CH13 / ACMP0_P3 / ACMP1_P3 / USCI0_DAT0 / UART0_TXD / UART3_nRTS / PWM1_CH2 / TM2_EXT
9	PB.12 / ADC0_CH12 / ACMP0_P2 / ACMP1_P2 / USCI0_CLK / UART0_RXD / UART3_nCTS / PWM1_CH3 / TM3_EXT
10	AV_{DD}
11	AV_{SS}
12	PB.11 / ADC0_CH11 / UART0_nCTS / UART4_TXD / I2C1_SCL / BPWM1_CH0
13	PB.10 / ADC0_CH10 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / BPWM1_CH1
14	PB.9 / ADC0_CH9 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / UART7_TXD / BPWM1_CH2
15	PB.8 / ADC0_CH8 / USCI1_CLK / UART0_RXD / UART1_nRTS / UART7_RXD / BPWM1_CH3
16	PB.7 / ADC0_CH7 / USCI1_DAT0 / UART1_TXD / BPWM1_CH4 / PWM1_BRAKE0 / PWM1_CH4 / ACMP0_O
17	PB.6 / ADC0_CH6 / USCI1_DAT1 / UART1_RXD / BPWM1_CH5 / PWM1_BRAKE1 / PWM1_CH5 / INT4 / ACMP1_O
18	PB.5 / ADC0_CH5 / ACMP1_N / I2C0_SCL / UART5_TXD / USCI1_CTL0 / PWM0_CH0 / UART2_TXD / TM0 / INT0
19	PB.4 / ADC0_CH4 / ACMP1_P1 / I2C0_SDA / UART5_RXD / USCI1_CTL1 / PWM0_CH1 / UART2_RXD / TM1 / INT1
20	PB.3 / ADC0_CH3 / ACMP0_N / I2C1_SCL / UART1_TXD / UART5_nRTS / USCI1_DAT1 / PWM0_CH2 / PWM0_BRAKE0 / TM2 / INT2
21	PB.2 / ADC0_CH2 / ACMP0_P1 / I2C1_SDA / UART1_RXD / UART5_nCTS / USCI1_DAT0 / PWM0_CH3 / TM3 / INT3
22	PB.1 / ADC0_CH1 / UART2_TXD / USCI1_CLK / I2C1_SCL / QSPI0_MISO1 / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0
23	PB.0 / ADC0_CH0 / UART2_RXD / I2C1_SDA / QSPI0_MOSI1 / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1
24	PA.11 / ACMP0_P0 / USCI0_CLK / UART6_TXD / BPWM0_CH0 / TM0_EXT
25	PA.10 / ACMP1_P0 / USCI0_DAT0 / UART6_RXD / BPWM0_CH1 / TM1_EXT
26	PA.9 / USCI0_DAT1 / UART1_TXD / UART7_TXD / BPWM0_CH2 / TM2_EXT
27	RF_V_{DD}
28	RF_CLKO
29	PA.8 / USCI0_CTL1 / UART1_RXD / UART7_RXD / BPWM0_CH3 / TM3_EXT / INT4
30	PC.13 / USCI0_CTL0 / UART2_TXD / BPWM0_CH4 / CLKO / ADC0_ST
31	PF.14 / PWM1_BRAKE0 / PWM0_BRAKE0 / PWM0_CH4 / CLKO / TM3
32	PF.5 / UART2_RXD / UART2_nCTS / PWM0_CH0 / BPWM0_CH4 / X32_IN / ADC0_ST
33	PF.4 / UART2_TXD / UART2_nRTS / PWM0_CH1 / BPWM0_CH5 / X32_OUT
34	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0
35	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / BPWM1_CH1
36	PE.8 / USCI1_CTL1 / UART2_TXD / PWM0_CH0 / PWM0_BRAKE0
37	PE.9 / USCI1_CTL0 / UART2_RXD / PWM0_CH1 / PWM0_BRAKE1
38	PC.7 / UART4_TXD / UART0_nCTS / UART6_TXD / PWM1_CH2 / BPWM1_CH0 / TM0 / INT3
39	PC.6 / UART4_RXD / UART0_nRTS / UART6_RXD / PWM1_CH3 / BPWM1_CH1 / TM1 / INT2
40	PA.7 / UART0_TXD / I2C1_SCL / PWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1

Pin	M032BTAIAAN Pin Function
41	PA.6 / UART0_RXD / I2C1_SDA / PWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
42	V_{SS}
43	V_{DD}
44	PA.5 / QSPI0_MISO1 / UART0_nCTS / UART0_TXD / I2C0_SCL / UART5_TXD / BPWM0_CH5 / PWM0_CH0
45	PA.4 / QSPI0_MOSI1 / UART0_nRTS / UART0_RXD / I2C0_SDA / UART5_RXD / BPWM0_CH4 / PWM0_CH1
46	PA.3 / QSPI0_SS / UART4_TXD / I2C0_SMBAL / UART1_TXD / I2C1_SCL / BPWM0_CH3 / PWM0_CH2 / CLKO / PWM1_BRAKE1
47	PA.2 / QSPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / BPWM0_CH2 / PWM0_CH3
48	PA.1 / QSPI0_MISO0 / UART0_TXD / UART1_nCTS / BPWM0_CH1 / PWM0_CH4
49	PA.0 / QSPI0_MOSI0 / UART0_RXD / UART1_nRTS / BPWM0_CH0 / PWM0_CH5
50	PF.15 / PWM0_BRAKE0 / PWM0_CH1 / TM2 / CLKO / INT4
51	nRESET
52	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / BPWM1_CH0 / ICE_DAT
53	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / BPWM1_CH1 / ICE_CLK
54	PC.1 / QSPI0_MISO0 / UART2_TXD / I2C0_SCL / PWM1_CH4 / ACMP0_O / ADC0_ST
55	PC.0 / QSPI0_MOSI0 / UART2_RXD / I2C0_SDA / PWM1_CH5 / ACMP1_O
56	RF_AV_{DD1V2}
57	V_{SS}
58	RF_IO
59	V_{SS}
60	RF_V_{DDPA}
61	RF_XTAL_IN
62	RF_XTAL_OUT
63	USB_VBUS
64	USB_D-
65	USB_D+
66	USB_VDD33_CAP
67	RF_AVDD1V2
68	RF_BUCK_FB
69	EPAD (V_{SS})

Table 4.1-3 M032BTAIAAN Multi-function Pin Table

4.2 Pin Mapping

Different part number with the same package might have different function. Please refer to the selection guide in section 3.2, Pin Configuration in section 4.1 or NuTool - PinConfig.

Corresponding Part Number: M031BTxD, M031BTxE, M032BTxG, M032BTxI series.

	M031BT series	M032BT series
Pin Name	**48 Pin**	**68 Pin**
PB.3	1	20
PB.2	2	21
PB.1	3	22
PB.0	4	23
RF_AV_{DD1V2}	5	56
V_{SS}	6	57
RF_IO	7	58
V_{SS}	8	59
RF_V_{DDPA}	9	60
PF.5	10	32
PF.4	11	33
PF.3	12	34
PF.2	13	35
RF_XTAL_IN	14	61
RF_XTAL_OUT	15	62
RF_AV_{DD1V2}	16	67
RF_BUCK_FB	17	68
RF_BUCK_OUT	18	1
PA.3	19	46
V_{SS}	20	2
PA.2	21	47
PA.1	22	48
PA.0	23	49
PF.15	24	50
nRESET	25	51
PF.0	26	52
PF.1	27	53
PC.1	28	54
PC.0	29	55
RF_V_{DD}	30	27
RF_CLKO	31	28

	M031BT series	M032BT series
Pin Name	**48 Pin**	**68 Pin**
V_{SS}	32	3
LDO_CAP	33	4
V_{DD}	34	5
PB.15	35	6
PB.14	36	7
PB.13	37	8
PB.12	38	9
AV_{DD}	39	10
AV_{SS}	40	11
PB.11	41	12
PB.10	42	13
PB.9	43	14
PB.8	44	15
PB.7	45	16
PB.6	46	17
PB.5	47	18
PB.4	48	19
EPAD (V_{SS})	49	69
PA.11		24
PA.10		25
PA.9		26
PA.8		29
PC.13		30
PF.14		31
PE.8		36
PE.9		37
PC.7		38
PC.6		39
PA.7		40
PA.6		41
VSS		42
VDD		43
PA.5		44
PA.4		45
USB_VBUS		63

	M031BT series	M032BT series
Pin Name	**48 Pin**	**68 Pin**
USB_D-		64
USB_D+		65
USB_VDD33_CAP		66

4.3 Pin Function Description

Group	Pin Name	Type	Description
ACMP0	ACMP0_N	A	Analog comparator 0 negative input pin.
	ACMP0_O	O	Analog comparator 0 output pin.
	ACMP0_P0	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1	A	Analog comparator 0 positive input 1 pin.
	ACMP0_P2	A	Analog comparator 0 positive input 2 pin.
	ACMP0_P3	A	Analog comparator 0 positive input 3 pin.
	ACMP0_WLAT	I	Analog comparator 0 window latch input pin
ACMP1	ACMP1_N	A	Analog comparator 1 negative input pin.
	ACMP1_O	O	Analog comparator 1 output pin.
	ACMP1_P0	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1	A	Analog comparator 1 positive input 1 pin.
	ACMP1_P2	A	Analog comparator 1 positive input 2 pin.
	ACMP1_P3	A	Analog comparator 1 positive input 3 pin.
	ACMP1_WLAT	I	Analog comparator 1 window latch input pin
ADC0	ADC0_CH0	A	ADC0 channel 0 analog input.
	ADC0_CH1	A	ADC0 channel 1 analog input.
	ADC0_CH2	A	ADC0 channel 2 analog input.
	ADC0_CH3	A	ADC0 channel 3 analog input.
	ADC0_CH4	A	ADC0 channel 4 analog input.
	ADC0_CH5	A	ADC0 channel 5 analog input.
	ADC0_CH6	A	ADC0 channel 6 analog input.
	ADC0_CH7	A	ADC0 channel 7 analog input.
	ADC0_CH8	A	ADC0 channel 8 analog input.
	ADC0_CH9	A	ADC0 channel 9 analog input.
	ADC0_CH10	A	ADC0 channel 10 analog input.
	ADC0_CH11	A	ADC0 channel 11 analog input.
	ADC0_CH12	A	ADC0 channel 12 analog input.
	ADC0_CH13	A	ADC0 channel 13 analog input.
	ADC0_CH14	A	ADC0 channel 14 analog input.
	ADC0_CH15	A	ADC0 channel 15 analog input.
	ADC0_ST	I	ADC0 external trigger input pin.
BPWM0	BPWM0_CH0	I/O	BPWM0 channel 0 output/capture input.
	BPWM0_CH1	I/O	BPWM0 channel 1 output/capture input.
	BPWM0_CH2	I/O	BPWM0 channel 2 output/capture input.

Group	Pin Name	Type	Description
	BPWM0_CH3	I/O	BPWM0 channel 3 output/capture input.
	BPWM0_CH4	I/O	BPWM0 channel 4 output/capture input.
	BPWM0_CH5	I/O	BPWM0 channel 5 output/capture input.
BPWM1	BPWM1_CH0	I/O	BPWM1 channel 0 output/capture input.
	BPWM1_CH1	I/O	BPWM1 channel 1 output/capture input.
	BPWM1_CH2	I/O	BPWM1 channel 2 output/capture input.
	BPWM1_CH3	I/O	BPWM1 channel 3 output/capture input.
	BPWM1_CH4	I/O	BPWM1 channel 4 output/capture input.
	BPWM1_CH5	I/O	BPWM1 channel 5 output/capture input.
CLKO	CLKO	O	Clock Out
GPIO	PA.x~PH.x	I/O	General purpose digital I/O pin.
I2C0	I2C0_SCL	I/O	I2C0 clock pin.
	I2C0_SDA	I/O	I2C0 data input/output pin.
	I2C0_SMBAL	O	I2C0 SMBus SMBALTER pin
	I2C0_SMBSUS	O	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C1	I2C1_SCL	I/O	I2C1 clock pin.
	I2C1_SDA	I/O	I2C1 data input/output pin.
ICE	ICE_CLK	I	Serial wired debugger clock pin **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin
	ICE_DAT	I/O	Serial wired debugger data pin **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin
	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
INT0	INT0	I	External interrupt 0 input pin.
INT1	INT1	I	External interrupt 1 input pin.
INT3	INT3	I	External interrupt 3 input pin.
INT4	INT4	I	External interrupt 4 input pin.
INT5	INT5	I	External interrupt 5 input pin.
PWM0	PWM0_BRAKE0	I	PWM0 Brake 0 input pin.
	PWM0_BRAKE1	I	PWM0 Brake 1 input pin.
	PWM0_CH0	I/O	PWM0 channel 0 output/capture input.
	PWM0_CH1	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH2	I/O	PWM0 channel 2 output/capture input.
	PWM0_CH3	I/O	PWM0 channel 3 output/capture input.
	PWM0_CH4	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH5	I/O	PWM0 channel 5 output/capture input.
PWM1	PWM1_BRAKE0	I	PWM1 Brake 0 input pin.
	PWM1_BRAKE1	I	PWM1 Brake 1 input pin.

Group	Pin Name	Type	Description
	PWM1_CH0	I/O	PWM1 channel 0 output/capture input.
	PWM1_CH1	I/O	PWM1 channel 1 output/capture input.
	PWM1_CH2	I/O	PWM1 channel 2 output/capture input.
	PWM1_CH3	I/O	PWM1 channel 3 output/capture input.
	PWM1_CH4	I/O	PWM1 channel 4 output/capture input.
	PWM1_CH5	I/O	PWM1 channel 5 output/capture input.
Power	V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
	V_{SS}	P	Ground pin for digital circuit.
	AV_{DD}	P	Power supply for internal analog circuit.
	AV_{SS}	P	Ground pin for analog circuit.
	LDO_CAP	A	LDO output pin. **Note:** This pin needs to be connected with a 1uF capacitor.
	EPAD	P	Exposed pad served as ground pin (V_{SS}).
QSPI0	QSPI0_CLK	I/O	Quad SPI0 serial clock pin.
	QSPI0_MISO0	I/O	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	QSPI0_MISO1	I/O	Quad SPI0 MISO1 (Master In, Slave Out) pin.
	QSPI0_MOSI0	I/O	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
	QSPI0_MOSI1	I/O	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
	QSPI0_SS	I/O	Quad SPI0 slave select pin.
RF	RF_V_{DD}	P	RF power supply **Note:** This pin needs to be connected with a 1uF capacitor.
	RF_V_{DDPA}	P	Power supply for RF signal power amplifier **Note:** This pin needs to be connected with a 0.1uF capacitor.
	RF_AV_{DD1V2}	P	RF Transceiver 1.2 V power supply pin **Note:** This pin needs to be connected with a 0.1uF capacitor.
	RF_IO	A	RF input/output signal **Note:** The impedance of this RF transmission line needs to be 50 Ω.
	RF_BUCK_OUT	P	RF DC-DC converter 1.2 V output
	RF_BUCK_FB	P	RF DC-DC converter feedback **Note:** This pin needs to be connected with a 0.1uF capacitor.
	RF_CLKO	O	RF 16 MHz clock out.
	RF_XTAL_IN	I	RF high speed crystal input pin.
	RF_XTAL_OUT	O	RF high speed crystal output pin.
SPI0	SPI0_CLK	I/O	SPI0 serial clock pin.
	SPI0_MISO	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_SS	I/O	SPI0 slave select pin.
TM0	TM0	I/O	Timer0 event counter input/toggle output pin.
	TM0_EXT	I/O	Timer0 external capture input/toggle output pin.
TM1	TM1	I/O	Timer1 event counter input/toggle output pin.
	TM1_EXT	I/O	Timer1 external capture input/toggle output pin.

Group	Pin Name	Type	Description
TM2	TM2	I/O	Timer2 event counter input/toggle output pin.
	TM2_EXT	I/O	Timer2 external capture input/toggle output pin.
TM3	TM3	I/O	Timer3 event counter input/toggle output pin.
	TM3_EXT	I/O	Timer3 external capture input/toggle output pin.
UART0	UART0_RXD	I	UART0 data receiver input pin.
	UART0_TXD	O	UART0 data transmitter output pin.
	UART0_nCTS	I	UART0 clear to Send input pin.
	UART0_nRTS	O	UART0 request to Send output pin.
UART1	UART1_RXD	I	UART1 data receiver input pin.
	UART1_TXD	O	UART1 data transmitter output pin.
	UART1_nCTS	I	UART1 clear to Send input pin.
	UART1_nRTS	O	UART1 request to Send output pin.
UART2	UART2_RXD	I	UART2 data receiver input pin.
	UART2_TXD	O	UART2 data transmitter output pin.
	UART2_nCTS	I	UART2 clear to Send input pin.
	UART2_nRTS	O	UART2 request to Send output pin.
UART3	UART3_RXD	I	UART3 data receiver input pin.
	UART3_TXD	O	UART3 data transmitter output pin.
	UART3_nCTS	I	UART3 clear to Send input pin.
	UART3_nRTS	O	UART3 request to Send output pin.
UART4	UART4_RXD	I	UART4 data receiver input pin.
	UART4_TXD	O	UART4 data transmitter output pin.
	UART4_nCTS	I	UART4 clear to Send input pin.
	UART4_nRTS	O	UART4 request to Send output pin.
UART5	UART5_RXD	I	UART5 data receiver input pin.
	UART5_TXD	O	UART5 data transmitter output pin.
	UART5_nCTS	I	UART5 clear to Send input pin.
	UART5_nRTS	O	UART5 request to Send output pin.
UART6	UART6_RXD	I	UART6 data receiver input pin.
	UART6_TXD	O	UART6 data transmitter output pin.
	UART6_nCTS	I	UART6 clear to Send input pin.
	UART6_nRTS	O	UART6 request to Send output pin.
UART7	UART7_RXD	I	UART7 data receiver input pin.
	UART7_TXD	O	UART7 data transmitter output pin.
	UART7_nCTS	I	UART7 clear to Send input pin.
	UART7_nRTS	O	UART7 request to Send output pin.

Group	Pin Name	Type	Description
USB	USB_VBUS	P	Power supply from USB host or HUB.
	USB_D-	A	USB differential signal D-.
	USB_D+	A	USB differential signal D+.
	USB_V_{DD}33_CAP	A	Internal power regulator output 3.3V decoupling pin.
USCI0	USCI0_CLK	I/O	USCI0 clock pin.
	USCI0_CTL0	I/O	USCI0 control 0 pin.
	USCI0_CTL1	I/O	USCI0 control 1 pin.
	USCI0_DAT0	I/O	USCI0 data 0 pin.
	USCI0_DAT1	I/O	USCI0 data 1 pin.
USCI1	USCI1_CLK	I/O	USCI1 clock pin.
	USCI1_CTL0	I/O	USCI1 control 0 pin.
	USCI1_CTL1	I/O	USCI1 control 1 pin.
	USCI1_DAT0	I/O	USCI1 data 0 pin.
	USCI1_DAT1	I/O	USCI1 data 1 pin.
X32	X32_IN	I	External 32.768 kHz crystal input pin.
	X32_OUT	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.

5 BLOCK DIAGRAM

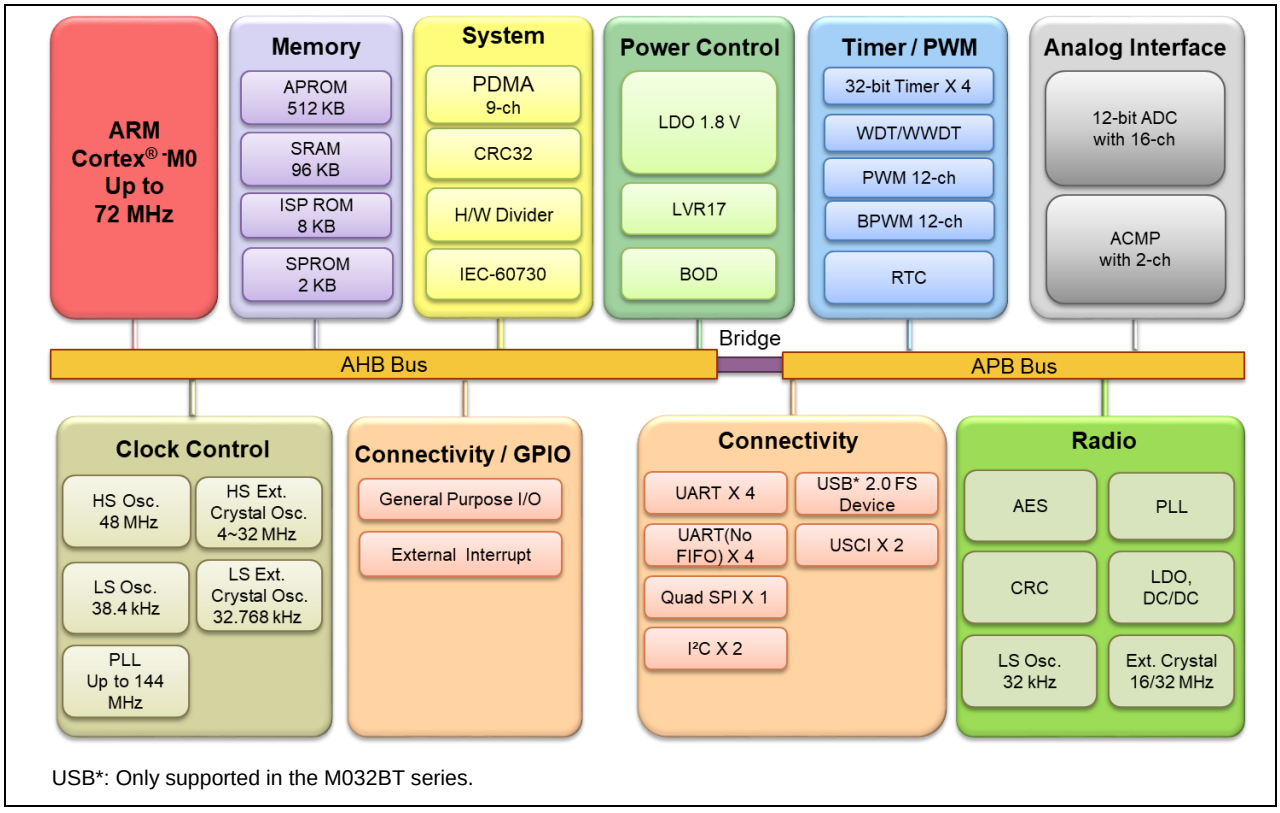


Figure 5-1 NuMicro® M031BT/M032BT Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6-1 shows the functional controller of processor.

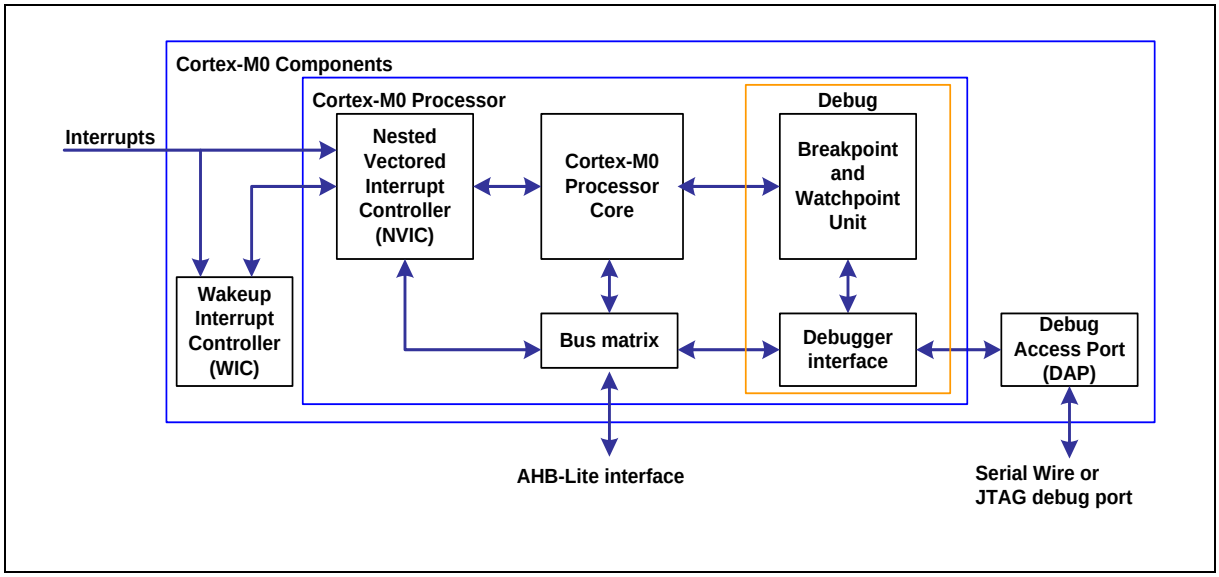


Figure 6-1 Functional Block Diagram

The implemented device provides:

- A low gate count processor:
  - Arm®6-M Thumb® instruction set
  - Thumb-2 technology
  - Arm®6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the Armv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature
- NVIC:
  - 32 external interrupt inputs, each with four levels of priority

- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode

- Debug support:
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 Clock Controller

6.2.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M0 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~32 MHz external high speed crystal (HXT), 48 MHz internal high speed RC oscillator (HIRC) and Programmable PLL output clock frequency (PLLFOUT) to reduce the overall system power consumption.Figure 6.2-1 and Figure 6.2-2 shows the clock generator and the overview of the clock source control.

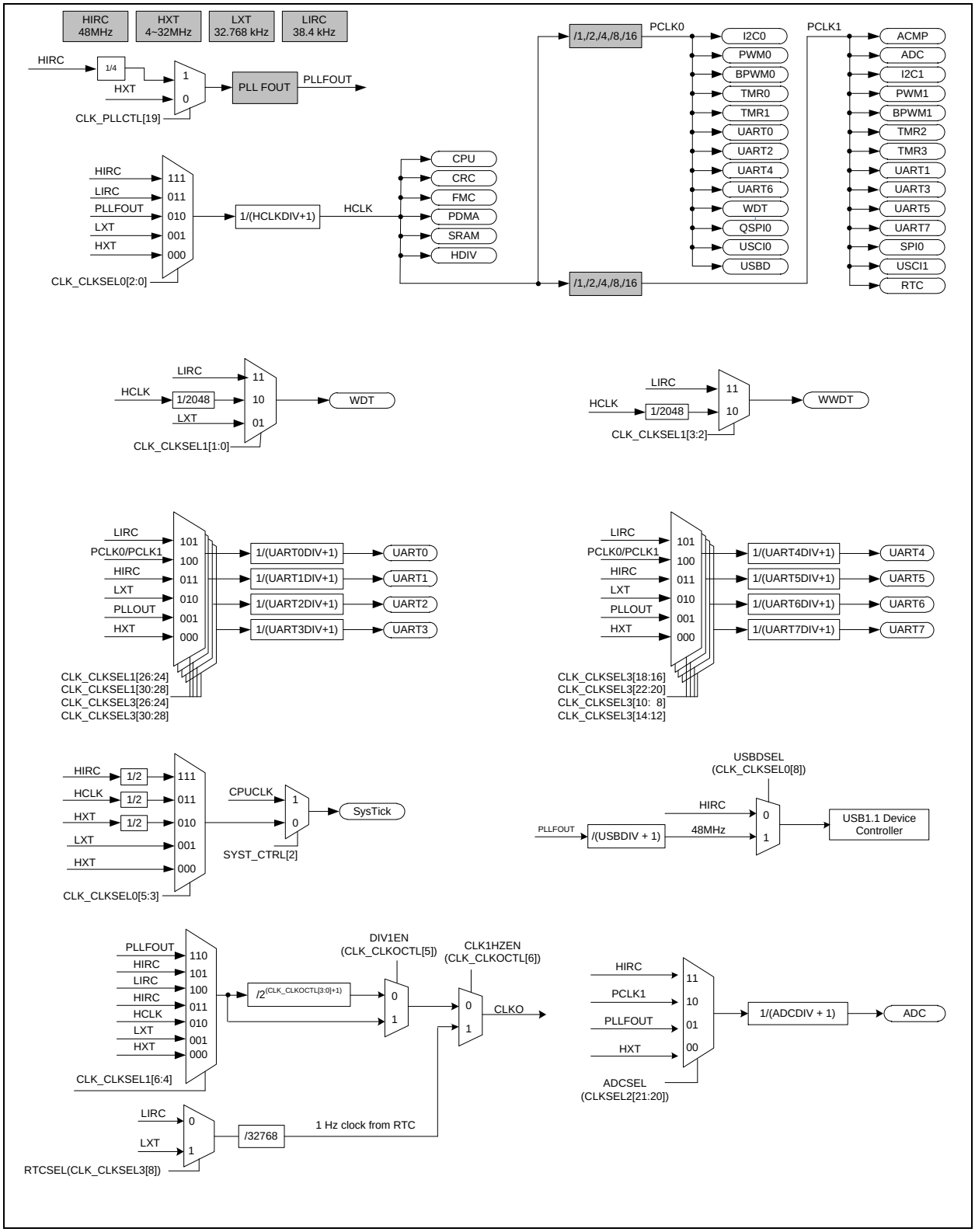


Figure 6.2-1 Clock Generator Global View Diagram (1/2)

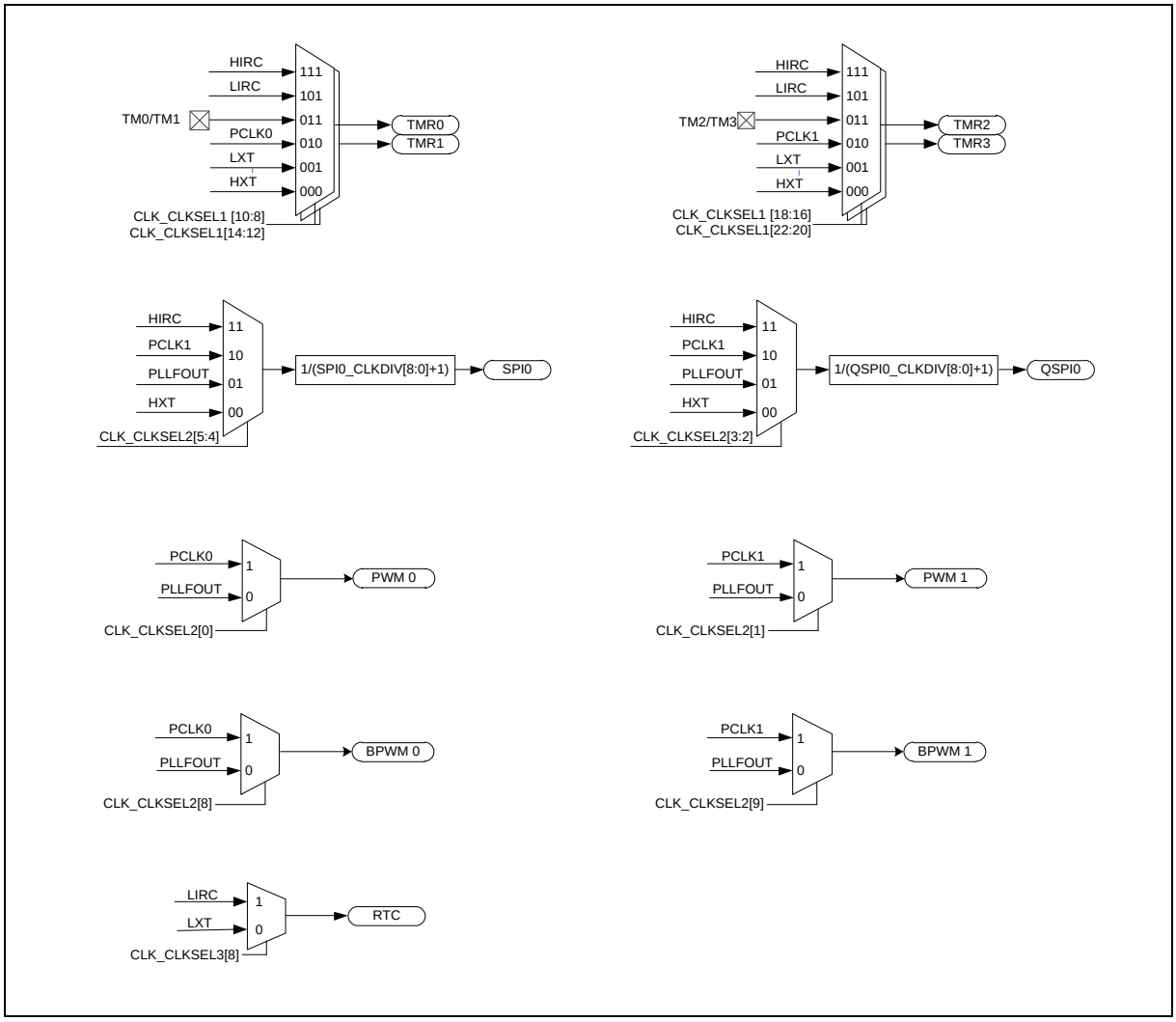


Figure 6.2-2 Clock Generator Global View Diagram (2/2)

6.2.2 Clock Generator

The clock generator consists of 6 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~32 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~32 MHz external high speed crystal (HXT) or 48 MHz internal high speed oscillator (HIRC/4)
- 48 MHz internal high speed RC oscillator (HIRC)
- 38.4 kHz internal low speed RC oscillator (LIRC)

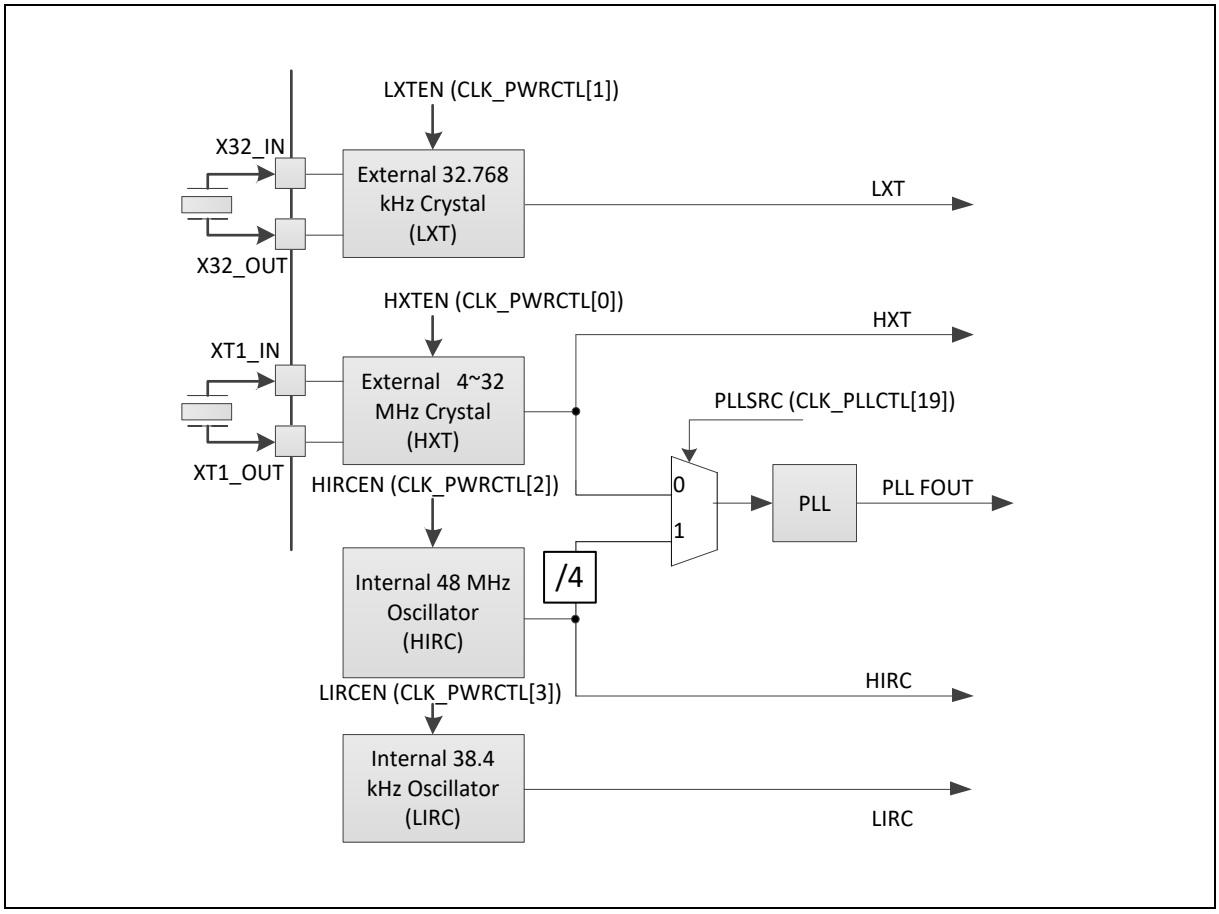


Figure 6.2-3 Clock Generator Block Diagram

6.2.3 System Clock and SysTick Clock

The system clock has 5 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.2-4

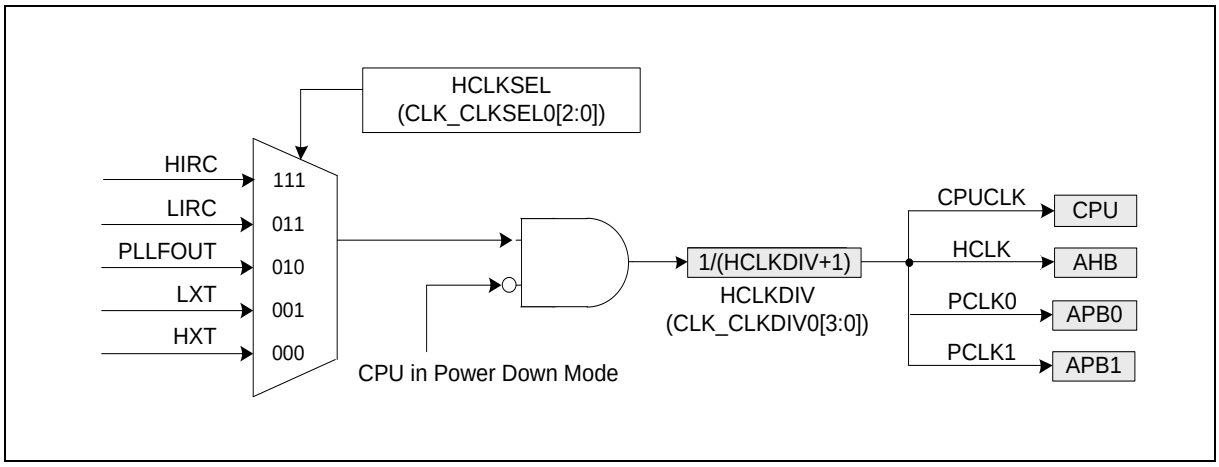


Figure 6.2-4 System Clock Block Diagram

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIEN (CLK_CLKDCTL[5]) is set to 1. User can trying to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

The HXT clock stop detect and system clock switch to HIRC procedure is shown in Figure 6.2-5.

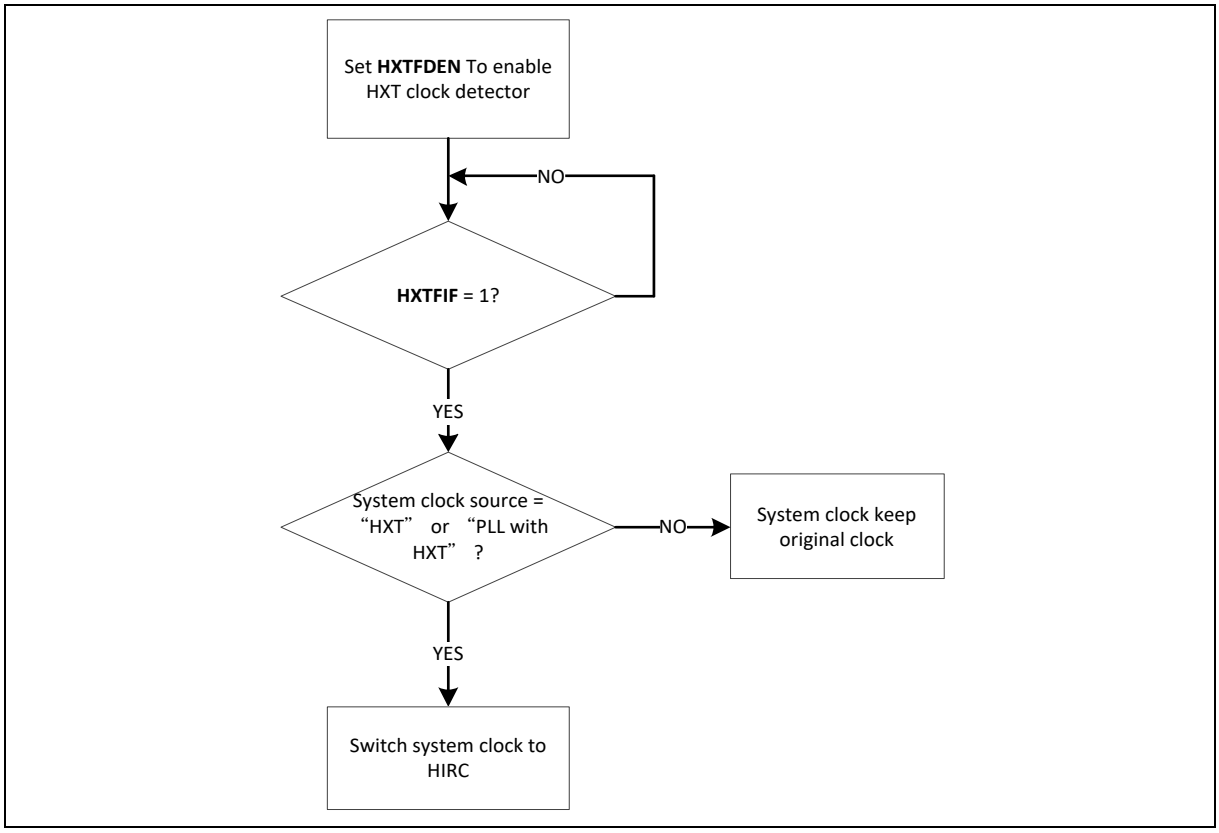


Figure 6.2-5 HXT Stop Protect Procedure

When LXT clock detector is enabled, the system clock will auto switch to LIRC if LXT clock stop being detected when system clock source comes from LXT. If LXT clock stop condition is detected, the LXTFIF (CLK_CLKDSTS[1]) is set to 1 and chip will enter interrupt if LXTFIEN (CLK_CLKDCTL[13]) is set to 1. User can trying to recover LXT by disable LXT and enable LXT again to check if the clock stable bit is set to 1 or not. If LXT clock stable bit is set to 1, it means LXT is recover to oscillate after re-enable action and user can switch system clock to LXT again.

The LXT clock stop detect and system clock switch to LIRC procedure is shown in Figure 6.2-6.

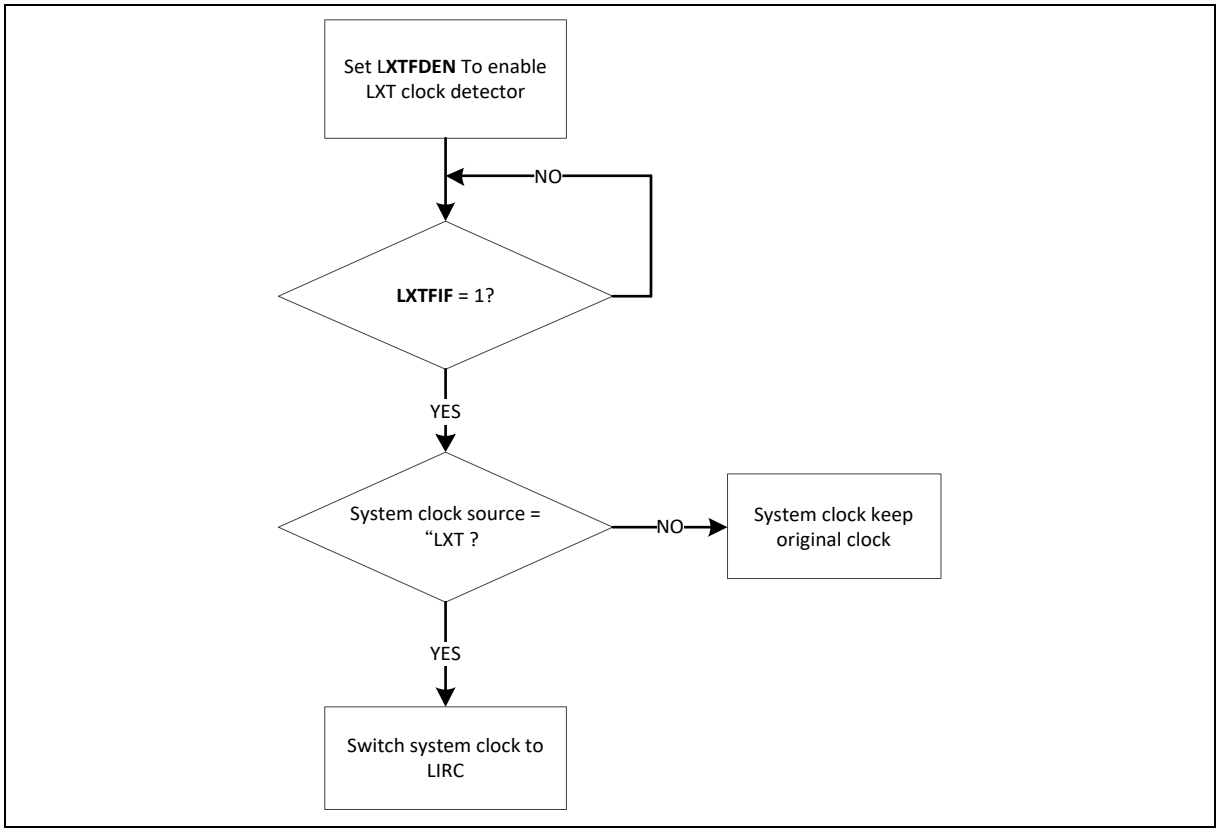


Figure 6.2-6 LXT Stop Protect Procedure

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.2-7.

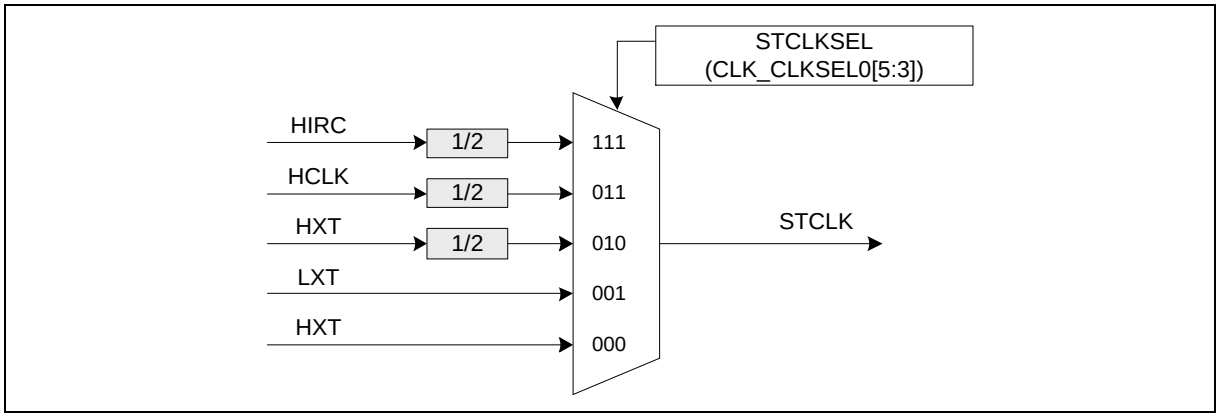


Figure 6.2-7 SysTick Clock Control Block Diagram

6.2.4 Peripherals Clock

The peripherals clock has different clock source switch setting, which depends on the different peripheral. Please refer to the CLK_CLKSELx register description.

6.2.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are

disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For theses clocks, which still keep active, are listed below:

- Clock Generator
  - 38.4 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

6.2.6 Clock Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

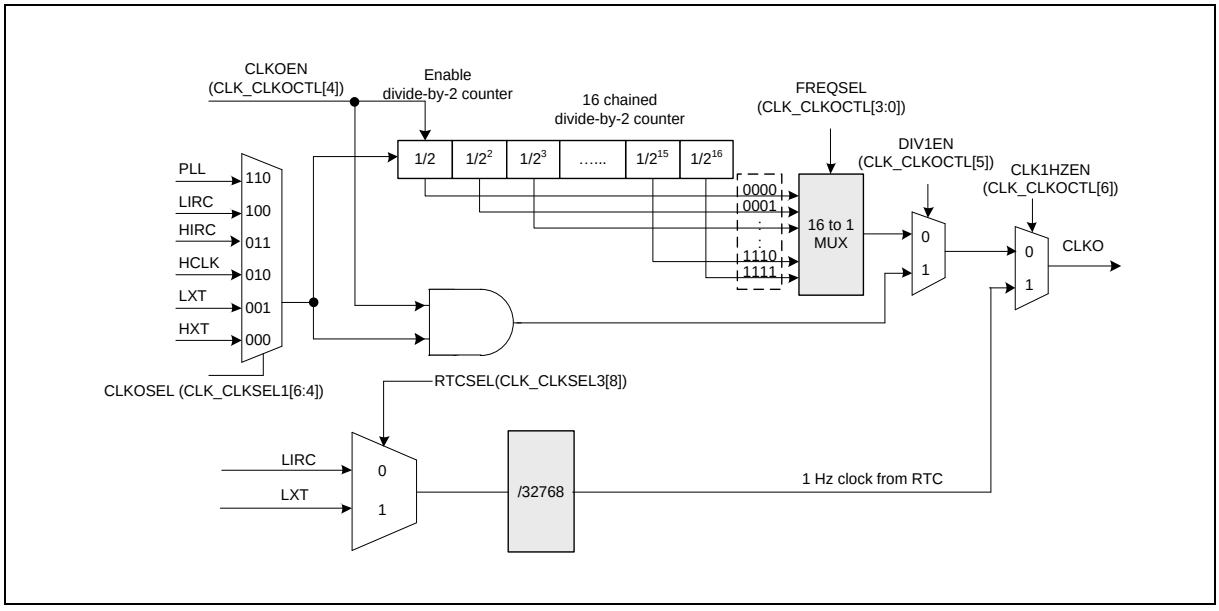


Figure 6.2-8 Clock Output Block Diagram

6.2.7 USB Clock Source

The clock source of USBD is generated from 48 MHz HIRC or programmable PLL output. The generated clocks are shown in Figure 6.2-9.

USBDIV is the clock divider output frequency, the output formula is

(PLLFOUT frequency) / (USBDIV + 1).

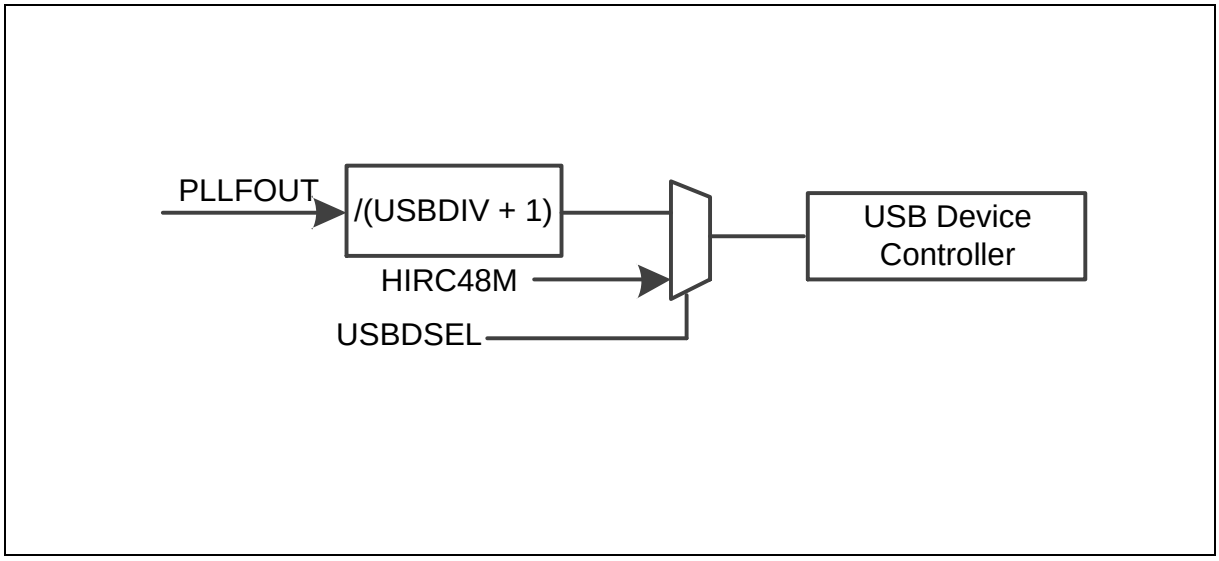


Figure 6.2-9 USBD Clock Source

6.3 System Manager

6.3.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Orginization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.3.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sourcces are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M0 core Only by writing 1 to CPURST (SYS_IPRST0[1])
  - nRESET glitch filter time 32us

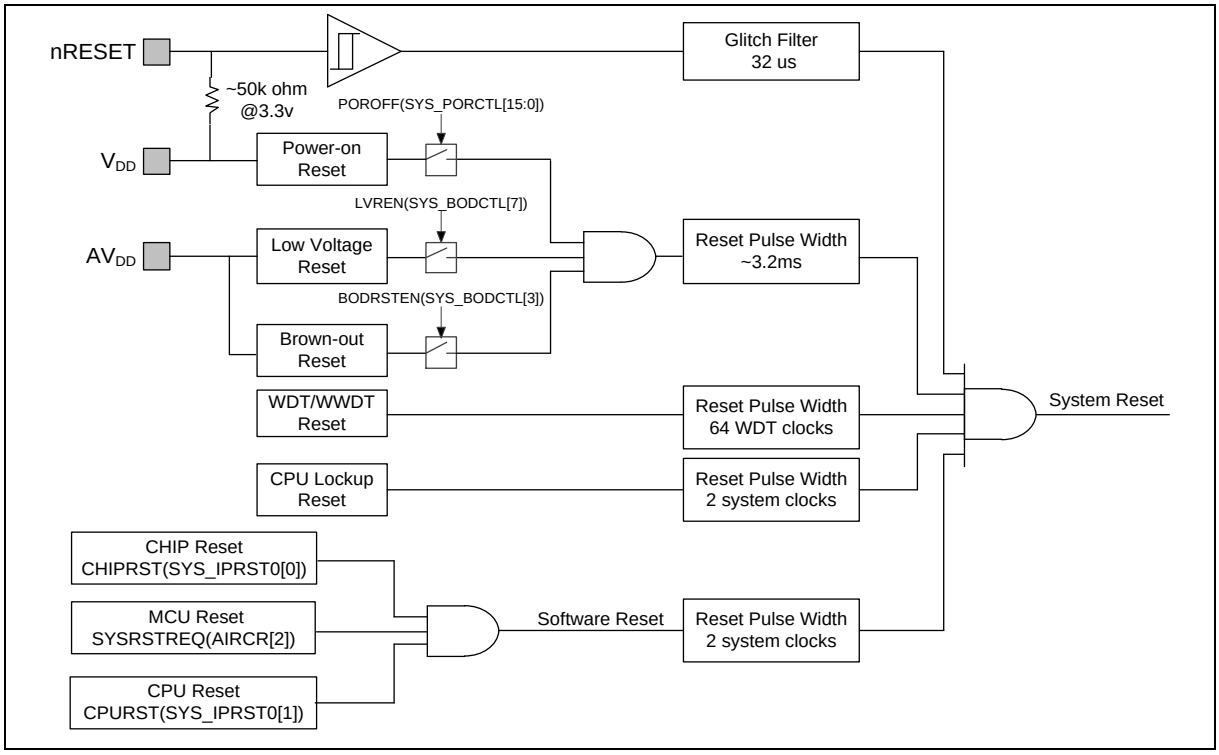


Figure 6.3-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M0 only; the other reset sources will reset Cortex®-M0 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.3-1.

Reset Sources Register	POR	nRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
SYS_RSTSTS	0x001	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[16])									
BODRSTEN (SYS_BODCTL[3])									
HXTEN (CLK_PWRCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
LXTSELXT (CLK_PWRCTL[24])	0x0	-	-	-	-	-	-	-	-
LXTGAIN	0x1	-	-	-	-	-	-	-	-

(CLK_PWRCTL[25:26])									
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
HCLKSEL (CLK_CLKSEL0[2:0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	-	-	-	-	-	-	-	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
PLLSTB (CLK_STATUS[2])	0x0	-	-	-	-	-	-	-	-
HIRCSTB (CLK_STATUS[4])	0x0	-	-	-	-	-	-	-	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDTEN (WDT_CTL[7])									
WDT_CTL except bit 1 and bit 7.	0x0700	0x0700	0x0700	0x0700	0x0700	-	0x0700	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
BS (FMC_ISPCTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
FMC_DFBA	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	Reload from CONFIG1	-	-
CBS (FMC_ISPSTS[2:1))	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
VECMAP (FMC_ISPSTS[23:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value								-

FMC Registers	Reset Value
Note: '-' means that the value of register keeps original setting.	

Table 6.3-1 Reset Value of Registers

6.3.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Table 6.3-2 shows the nRESET reset waveform.

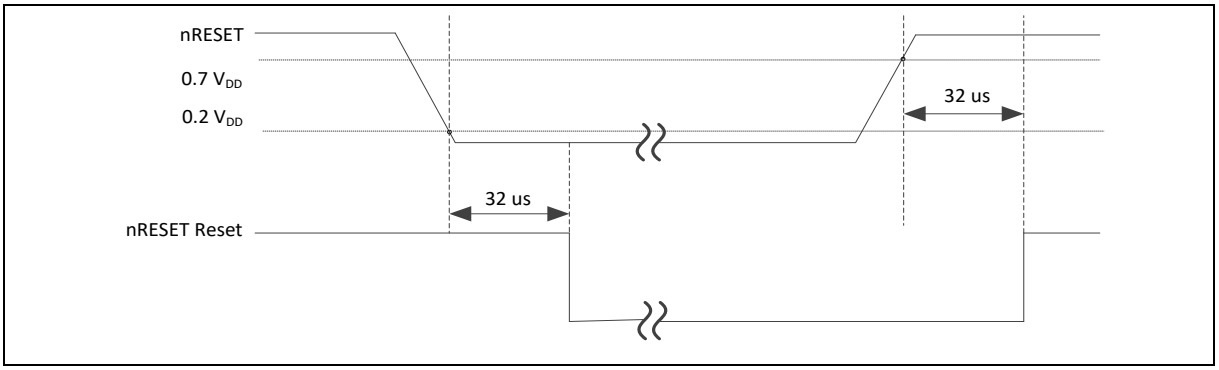


Figure 6.3-2 nRESET Reset Waveform

6.3.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.3-3 shows the power-on reset waveform.

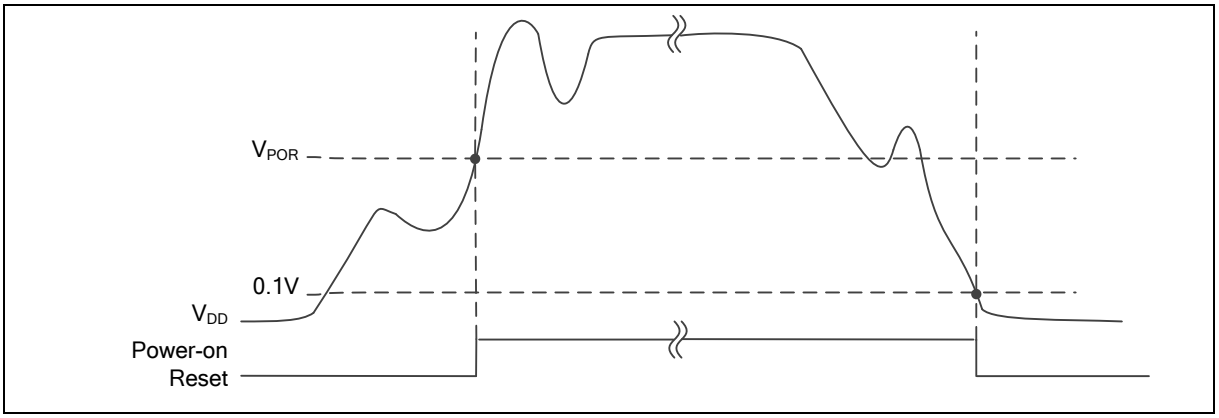


Figure 6.3-3 Power-on Reset (POR) Waveform

6.3.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.3-4 shows the Low Voltage Reset waveform.

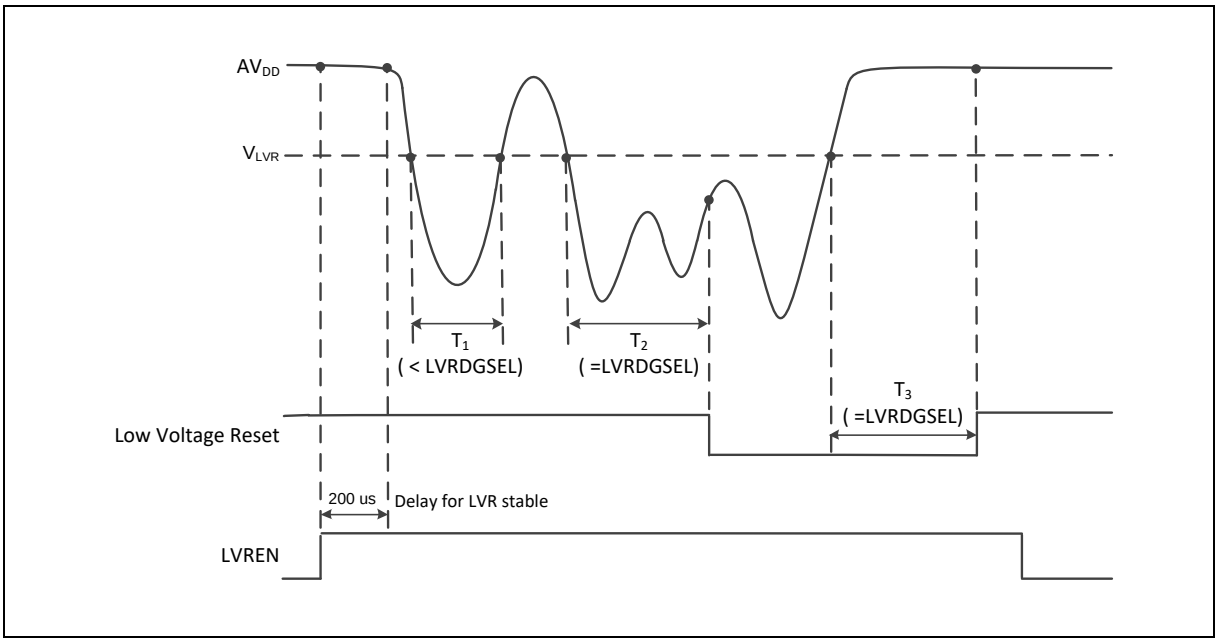


Figure 6.3-4 Low Voltage Reset (LVR) Waveform

6.3.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN and BODVL (SYS_BODCTL[16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.3-5 shows the Brown-out Detector waveform.

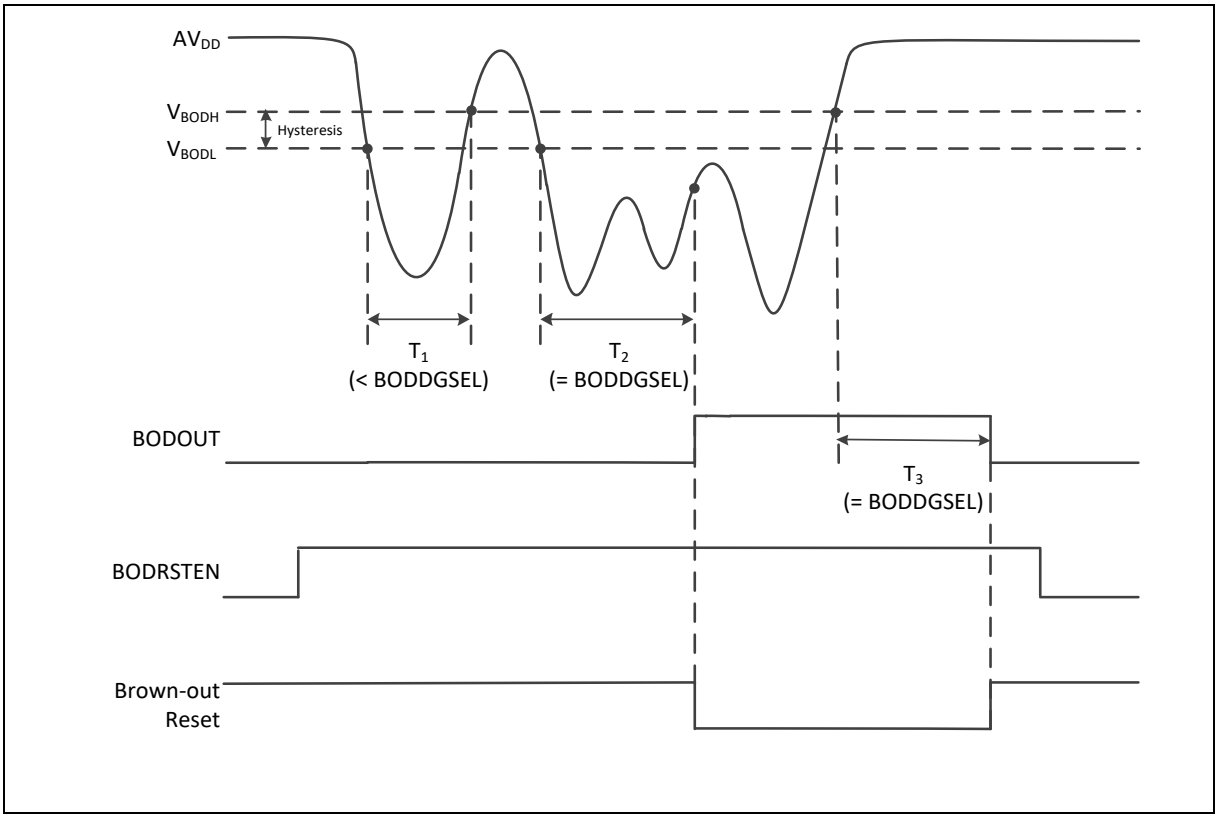


Figure 6.3-5 Brown-out Detector (BOD) Waveform

6.3.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.3.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.3.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M0 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[0]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

6.3.3 System Power Distribution

In this chip, power distribution is divided into three segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver.

The outputs of internal voltage regulators, LDO and V_{DD}, require an external capacitor which should be located close to the corresponding pin. Figure 6.3-6 shows the NuMicro® M031 power distribution.

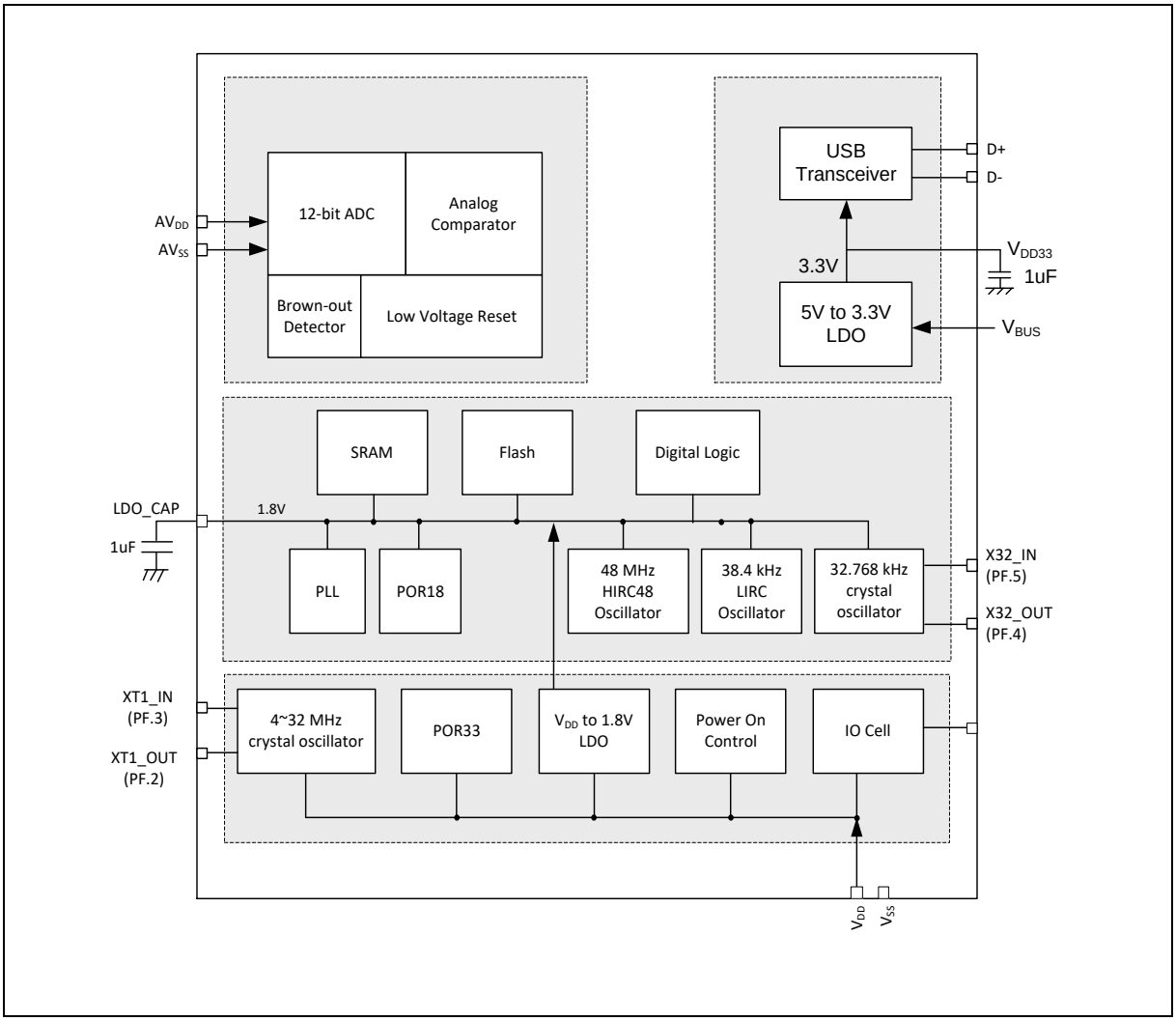


Figure 6.3-6 NuMicro® M031BT Power Distribution Diagram

6.3.4 Power Modes and Wake-up Sources

The M031BT/M032BT Series has power manager unit to support several operating modes for saving power. Table 6.3-2 lists all power modes in the M031BT/M032BT Series .

Mode	CPU Operating Maximum Speed (MHz)	LDO_CAP(V)	Clock Disable
Normal mode	72 MHz at 2.0V-3.6V	1.8	All clocks are disabled by control register.

	48 MHz at 1.8V-3.6V		
Idle mode	CPU enter Sleep mode	1.8	Only CPU clock is disabled.
Power-down mode	CPU enters Power-down mode	1.8	Most clocks are disabled except LIRC/LXT, and only WDT/Timer/UART/RTC peripheral clocks still enable if their clock sources are selected as LIRC/LXT.

Table 6.3-2 Power Mode Table

There are different power mode entry settings and leaving condition for each power mode. Table 6.3-3 shows the entry setting for each power mode. When chip power-on, chip is running in normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCT:[7]) and execute WFI instruction.

Register/Instruction Mode	**SLEEPDEEP (SCR[2])**	**PDEN (CLK_PWRCTL[7])**	**CPU Run WFI Instruction**
Normal mode	0	0	NO
Idle mode (CPU enter Sleep mode)	0	0	YES
Power-down mode (CPU enters Deep Sleep mode)	1	1	YES

Table 6.3-3 Power Mode Difference Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.3-4 lists the available clocks for each power mode.

Power Mode	**Normal Mode**	**Idle Mode**	**Power-Down Mode**
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	WDT, I²C, Timer, UART, BOD, GPIO, EINT, USCI, USBD, ACMP, and RTC
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.3-4 Power Mode Difference Table

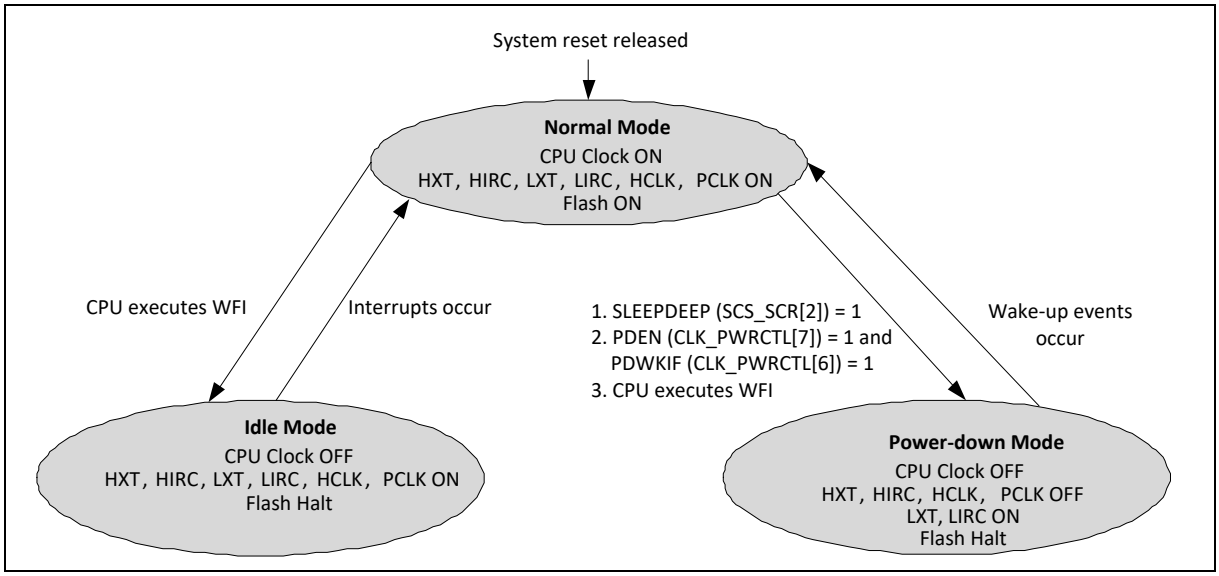


Figure 6.3-7 Power Mode State Machine

1. LXT (32768 Hz XTL) ON or OFF depends on SW setting in normal mode.
2. LIRC (38.4 kHz OSC) ON or OFF depends on SW setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.
5. If UART clock source is selected as LXT and LXT is on.
6. If RTC clock source is selected as LIRC/LXT and LIRC/LXT is on.

	Normal Mode	Idle Mode	Power-Down Mode
HXT (4~32 MHz XTL)	ON	ON	Halt
HIRC48 (48 MHz OSC)	ON	ON	Halt
LXT (32768 Hz XTL)	ON	ON	ON/OFF[1]
LIRC (38.4 kHz OSC)	ON	ON	ON/OFF[2]
PLL	ON/OFF	ON/OFF	Halt
LDO	ON	ON	ON
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON	Halt
GPIO	ON	ON	Halt
PDMA	ON	ON	Halt
TIMER	ON	ON	ON/OFF[3]
PWM	ON	ON	Halt
BPWM	ON	ON	Halt
WDT	ON	ON	ON/OFF[4]
WWDT	ON	ON	Halt
UART	ON	ON	ON/OFF[5]
USCI	ON	ON	Halt
I^2C	ON	ON	Halt
SPI	ON	ON	Halt
QSPI	ON	ON	Halt
USBD	ON	ON	Halt
ADC	ON	ON	Halt
ACMP	ON	ON	Halt
RTC	ON	ON	ON/OFF[6]

Table 6.3-5 Clocks in Power Modes

Wake-up sources in Power-down mode:

WDT, I^2C, Timer, UART, USCI, BOD, GPIO, USBD, ACMP, and RTC.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.3-5 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up	Wake-Up Condition	System Can Enter Power-Down Mode Again Condition*

Source		
BOD	Brown-Out Detector Interrupt	After software writes 1 to clear (SYS_BODCTL[4]).
INT	External Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
TIMER	Timer Interrupt	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
WDT	WDT Interrupt	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
RTC	Alarm Interrupt	After software writes 1 to clear ALMIF (RTC_INTSTS[0]).
	Time Tick Interrupt	After software writes 1 to clear TICKIF (RTC_INTSTS[1]).
UART0/1/4/5	nCTS wake-up	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	Incoming Data wake-up	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
UART2/3/6/7	nCTS wake-up	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	Incoming Data wake-up	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
USCI UART	CTS Toggle	After software writes 1 to clear WKF (UUART_WKSTS[0]).
	Data Toggle	After software writes 1 to clear WKF (UUART_WKSTS[0]).
USCI I^2C	Data toggle	After software writes 1 to clear WKF (UI2C_WKSTS[0]).
	Address match	After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], and then writes 1 to clear WKF (UI2C_WKSTS[0]).
USCI SPI	SS Toggle	After software writes 1 to clear WKF (USPI_WKSTS[0]).
I^2C	Address match	After software writes 1 to clear WKIF (I2C_WKSTS[0]).
USBD	Remote Wake-up	After software writes 1 to clear BUSIF (USBD_INTSTS[0]).
ACMP	Comparator Power-Down Wake-Up Interrupt	After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]).

Table 6.3-6 Condition of Entering Power-down Mode Again

6.3.5 System Memory Map

The NuMicro® M031BT/M032BT Series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown inTable 6.3-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The M031BT/M032BT Series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0007_FFFF	FLASH_BA	FLASH Memory Space (512 Kbytes)
0x2000_0000 – 0x2001_7FFF	SRAM0_BA	SRAM Memory Space (96 Kbytes)

0x6000_0000 – 0x6FFF_FFFF	EXTMEM_BA	External Memory Space (256 Mbytes)
Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers
0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA_BA	Peripheral DMA Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
0x4001_4000 – 0x4001_7FFF	HDIV_BA	Hardware Divider Register
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT_BA	Watchdog Timer Control Registers
0x4004_1000 – 0x4004_1FFF	RTC_BA	RTC Control Registers
0x4004_3000 – 0x4004_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
0x4004_5000 – 0x4004_5FFF	ACMP01_BA	Analog Comparator 0/ 1 Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_8000 – 0x4005_8FFF	PWM0_BA	PWM0 Control Registers
0x4005_9000 – 0x4005_9FFF	PWM1_BA	PWM1 Control Registers
0x4005_A000 – 0x4005_AFFF	BPWM0_BA	BPWM0 Control Registers
0x4005_B000 – 0x4005_BFFF	BPWM1_BA	BPWM1 Control Registers
0x4006_0000 – 0x4006_0FFF	QSPI0_BA	QSPI0 Control Registers
0x4006_1000 – 0x4006_1FFF	SPI0_BA	SPI0 Control Registers
0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers
0x4007_2000 – 0x4007_2FFF	UART2_BA	UART2 Control Registers
0x4007_3000 – 0x4007_3FFF	UART3_BA	UART3 Control Registers
0x4007_4000 – 0x4007_4FFF	UART4_BA	UART4 Control Registers
0x4007_5000 – 0x4007_5FFF	UART5_BA	UART5 Control Registers
0x4007_6000 – 0x4007_6FFF	UART6_BA	UART6 Control Registers
0x4007_7000 – 0x4007_7FFF	UART7_BA	UART7 Control Registers
0x4008_0000 – 0x4008_0FFF	I2C0_BA	I2C0 Control Registers
0x4008_1000 – 0x4008_1FFF	I2C1_BA	I2C1 Control Registers
0x400C_0000 – 0x400C_0FFF	USBD_BA	USB Device Control Register
0x400D_0000 – 0x400D_0FFF	USCI0_BA	USCI0 Control Registers

0x400D_1000 – 0x400D_1FFF	USCI1_BA	USCI1 Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.3-7 Address Space Assignments for On-Chip Controllers

6.3.6 SRAM Memory Organization

The M031BT supports embedded SRAM with total 16 Kbytes size

- Supports total 16 Kbytes SRAM
- Supports byte / half word / word write
- Supports oversize response error

Table 6.3-9 shows the SRAM organization of M031. The address between 0x2000_4000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

Figure 6.3-8 SRAM Memory Organization

6.3.7 SRAM Memory Organization with parity function

The M032BT supports embedded SRAM with total 96 Kbytes size

- Supports total 96 Kbytes SRAM
- Supports parity error check function for SRAM bank0 section 0(32 Kbytes)
- Supports byte / half word / word write
- Supports oversize response error

Table 6.3-9 shows the SRAM organization of M031. The address between 0x2001_8000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses. There are three section in SRAM bank0. The section 0 is addressed to 32 Kbytes with parity function, the section 1 is addressed to 32 Kbytes and the section 2 is addressed to 32 Kbytes. SRAM section 0 has byte parity error check function. When CPU is accessing SRAM section 0, the parity error checking mechanism is dynamic operating. As parity error occured, the PERRIF (SYS_SRAM_STATUS[0]) will be asserted to 1 and the SYS_SRAM_ERRADDR register will recode the address with parity error. Chip will enter interrupt when SRAM parity error occurred if PERRIEN (SYS_SRAM_INTCTL[0]) is set to 1. When SRAM parity error occured, chip will stop detecting SRAM parity error until user writes 1 to clear the PERRIF(SYS_SRAM_STATUS[0]) bit.

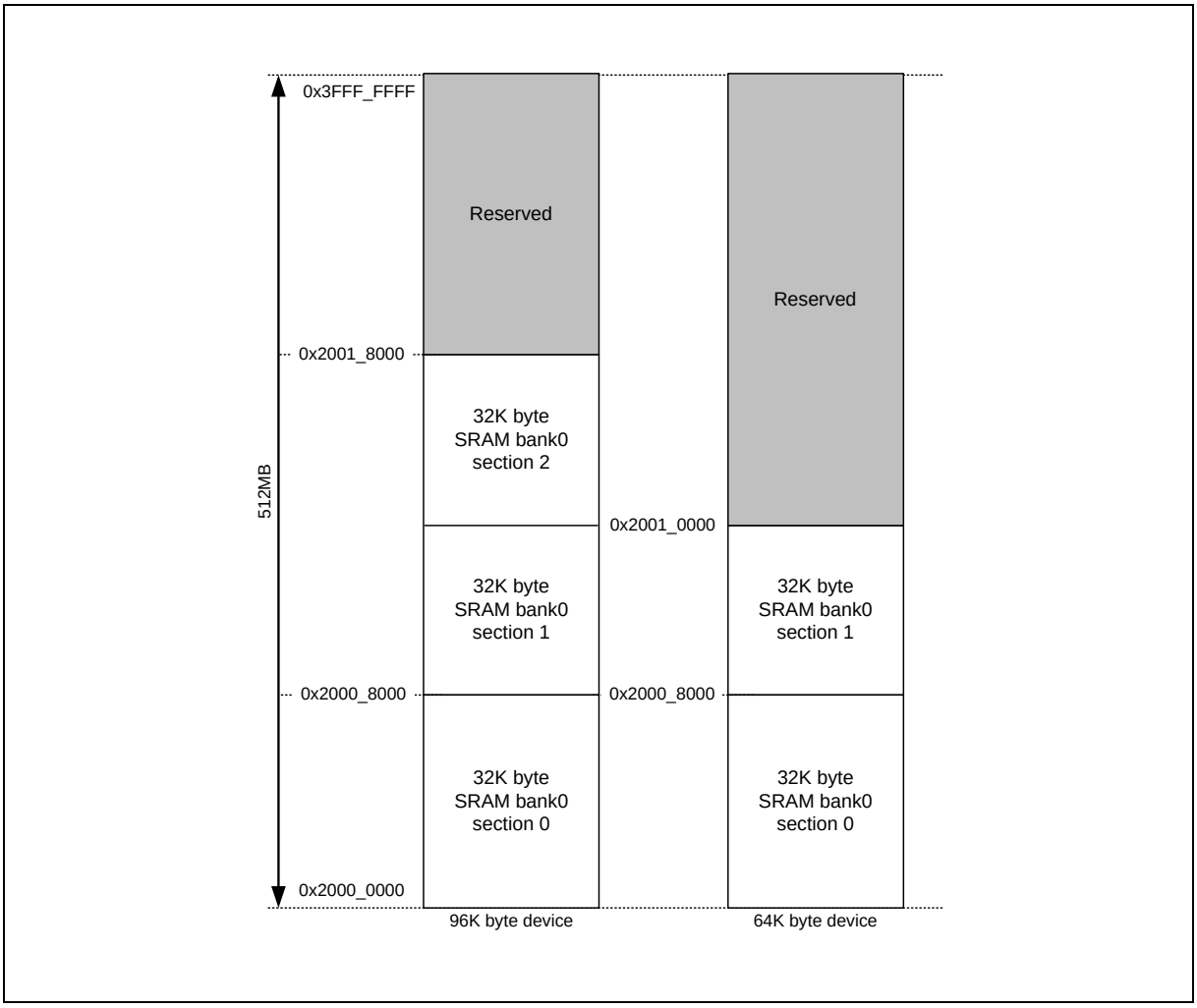


Figure 6.3-10 SRAM Memory Organization

6.3.8 Chip Bus Matrix

The M031BT/M032BT Series supports Bus Matrix to manage the access arbitration between masters. The access arbitration use round-robin algorithm as the bus priority.

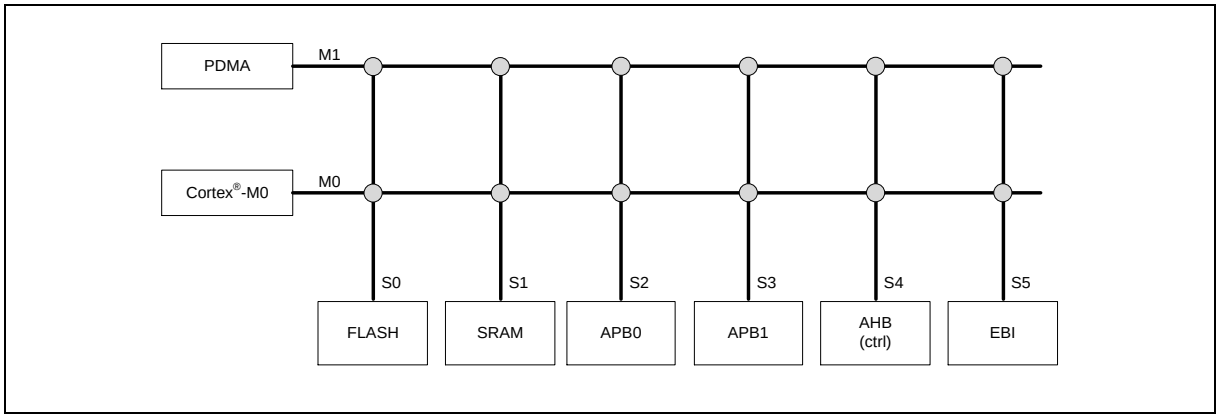


Figure 6.3-9 NuMicro® M031BT/M032BT Bus Matrix Diagram

6.3.9 IRC Auto Trim

This chip supports auto-trim function: the HIRC trim (48 MHz RC oscillator), according to the accurate external 32.768 kHz crystal oscillator or internal USB synchronous mode, automatically gets accurate output frequency, 0.25 % deviation within all temperature ranges.

In HIRC case, the system needs an accurate 48 MHz clock. In such case, if neither using use PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_HIRCTRIMCTL [10] reference clock selection) to “1”, set FREQSEL (SYS_HIRCTRIMCTL [1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_HIRCTRIMSTS[0] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

6.3.10 Register Lock Control

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x4000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence. All proteced control registers are noted “(Write Protect)” and add an note “**Note:** This bit is write protected. Refer to the SYS_REGLCTL register “ in register description field.

Register	Bit	Description
CLK_PWRCTL	[26:25] LXTGAIN	LXT Gain Control Bit (Write Protect)
CLK_PWRCTL	[22:20] HXTGAIN	HXT Gain Control Bit (Write Protect)
CLK_PWRCTL	[7] PDEN	System Power-down Enable (Write Protect)
CLK_PWRCTL	[5] PDWKIEN	Power-down Mode Wake-up Interrupt Enable Bit (Write Protect)
CLK_PWRCTL	[4] PDWKDLY	Enable the Wake-up Delay Counter (Write Protect)
CLK_PWRCTL	[3] LIRCEN	LIRC Enable Bit (Write Protect)
CLK_PWRCTL	[2] HIRCEN	HIRC Enable Bit (Write Protect)
CLK_PWRCTL	[1] LXTEN	LXT Enable Bit (Write Protect)
CLK_PWRCTL	[0] HXTEN	HXT Enable Bit (Write Protect)
CLK_APBCLK0	[0] WDTCKEN	Watchdog Timer Clock Enable Bit (Write Protect)
CLK_CLKSEL0	[8] USBDSEL	USB Device Clock Source Selection (Write Protect)
CLK_CLKSEL0	[5:3] STCLKSEL	Cortex®-M0 SysTick Clock Source Selection (Write Protect)
CLK_CLKSEL0	[2:0] HCLKSEL	HCLK Clock Source Selection (Write Protect)
CLK_CLKSEL1	[3:2] WWDTSEL	Window Watchdog Timer Clock Source Selection (Write Protect)
CLK_CLKSEL1	[1:0] WDTSEL	Watchdog Timer Clock Source Selection (Write Protect)
CLK_PLLCTL	[23] STBSEL	PLL Stable Counter Selection (Write Protect)
CLK_PLLCTL	[19] PLLSRC	PLL Source Clock Selection (Write Protect)
CLK_PLLCTL	[18] OE	PLL OE (FOUT Enable) Pin Control (Write Protect)
CLK_PLLCTL	[17] BP	PLL Bypass Control (Write Protect)
CLK_PLLCTL	[16] PD	Power-down Mode (Write Protect)
CLK_PLLCTL	[15:14] OUTDIV	PLL Output Divider Control (Write Protect)
CLK_PLLCTL	[13:9] INDIV	PLL Input Divider Control (Write Protect)
CLK_PLLCTL	[8:0] FBDIV	PLL Feedback Divider Control (Write Protect)
CLK_CLKDSTS	[8] HXTFQIF	HXT Clock Frequency Range Detector Interrupt Flag (Write Protect)
CLK_CLKDSTS	[1] LXTFIF	LXT Clock Fail Interrupt Flag (Write Protect)
CLK_CLKDSTS	[0] HXTFIF	HXT Clock Fail Interrupt Flag (Write Protect)

SYS_IPRST0	[7] CRCRST	CRC Calculation Controller Reset (Write Protect)
SYS_IPRST0	[4] HDIV_RST	HDIV Controller Reset (Write Protect)
SYS_IPRST0	[2] PDMARST	PDMA Controller Reset (Write Protect)
SYS_IPRST0	[1] CPURST	Processor Core One-shot Reset (Write Protect)
SYS_IPRST0	[0] CHIPRST	Chip One-shot Reset (Write Protect)
SYS_BODCTL	[20] LVRVL	LVR Detector Threshold Voltage Selection (Write Protect)
SYS_BODCTL	[16] BODVL	Brown-out Detector Threshold Voltage Selection (Write Protect)
SYS_BODCTL	[14:12] LVRDGSEL	LVR Output De-glitch Time Select (Write Protect)
SYS_BODCTL	[10:8] BODDGSEL	Brown-out Detector Output De-glitch Time Select (Write Protect)
SYS_BODCTL	[7] LVREN	Low Voltage Reset Enable Bit (Write Protect)
SYS_BODCTL	[5] BODLPM	Brown-out Detector Low Power Mode (Write Protect)
SYS_BODCTL	[3] BODRSTEN	Brown-out Reset Enable Bit (Write Protect)
SYS_BODCTL	[0] BODEN	Brown-out Detector Enable Bit (Write Protect)
SYS_PORCTL	[15:0] POROFF	Power-on Reset Enable Bit (Write Protect)
SYS_SRAM_BISTCTL	[18] SRS2	SRAM Bank0 Section 2 BIST Select (Write Protect)
SYS_SRAM_BISTCTL	[17] SRS1	SRAM Bank0 Section 1 BIST Select (Write Protect)
SYS_SRAM_BISTCTL	[16] SRS0	SRAM Bank0 Section 0 BIST Select (Write Protect)
SYS_SRAM_BISTCTL	[7] PDMABIST	PDMA BIST Enable Bit (Write Protect)
SYS_SRAM_BISTCTL	[4] USBBIST	USB BIST Enable Bit (Write Protect)
SYS_SRAM_BISTCTL	[2] FMCBIST	FMC CACHE BIST Enable Bit (Write Protect)
SYS_SRAM_BISTCTL	[0] SRBIST	SRAM BIST Enable Bit (Write Protect)
SYS_PORDISAN	[15:0] POROFFAN	Power-on Reset Enable Bit (Write Protect)
NMIEN	[15] UART1_INT	UART1 NMI Source Enable (Write Protect)
NMIEN	[14] UART0_INT	UART0 NMI Source Enable (Write Protect)
NMIEN	[13] EINT5	External Interrupt From PB.7, PD.12 or PF.14 Pin NMI Source Enable (Write Protect)
NMIEN	[12] EINT4	External Interrupt From PA.8, PB.6 or PF.15 Pin NMI Source Enable (Write Protect)
NMIEN	[11] EINT3	External Interrupt From PB.2 or PC.7 Pin NMI Source Enable (Write Protect)
NMIEN	[10] EINT2	External Interrupt From PB.3 or PC.6 Pin NMI Source Enable (Write Protect)
NMIEN	[9] EINT1	External Interrupt From PA.7, PB.4 or PD.15 Pin NMI Source Enable (Write Protect)
NMIEN	[8] EINT0	External Interrupt From PA.6 or PB.5 Pin NMI Source Enable (Write Protect)
NMIEN	[6] RTC_INT	RTC NMI Source Enable (Write Protect)
NMIEN	[4] CLKFAIL	Clock Fail Detected and IRC Auto Trim Interrupt NMI Source Enable (Write Protect)

NMIEN	[3] SRAM_PERR	SRAM ParityCheck Error NMI Source Enable (Write Protect)
NMIEN	[2] PWRWU_INT	Power-down Mode Wake-up NMI Source Enable (Write Protect)
NMIEN	[1] IRC_INT	IRC TRIM NMI Source Enable (Write Protect)
NMIEN	[0] BODOUT	BOD NMI Source Enable (Write Protect)
FMC_ISPCTL	[24] INTEN	ISP Interrupt Enabled Bit (Write Protect)
FMC_ISPCTL	[6] ISPFF	ISP Fail Flag (Write Protect)
FMC_ISPCTL	[5] LDUEN	LDROM Update Enable Bit (Write Protect)
FMC_ISPCTL	[4] CFGUEN	CONFIG Update Enable Bit (Write Protect)
FMC_ISPCTL	[3] APUEN	APROM Update Enable Bit (Write Protect)
FMC_ISPCTL	[2] SPUEN	SPROM Update Enable Bit (Write Protect)
FMC_ISPCTL	[1] BS	Boot Selection (Write Protect)
FMC_ISPCTL	[0] ISPEN	ISP Enable Bit (Write Protect)
FMC_ISPTRG	[0] ISPGO	ISP Start Trigger (Write Protect)
FMC_FTCTL	[9] CACHEINV	Flash Cache Invalidation (Write Protect)
FMC_FTCTL	[6:4] FOM	Frequency Optimization Mode (Write Protect)
FMC_ISPSTS	[6] ISPFF	ISP Fail Flag (Write Protect)
TIMER0_CTL	[31] ICEDEBUG	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
TIMER1_CTL	[31] ICEDEBUG	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
TIMER2_CTL	[31] ICEDEBUG	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
TIMER3_CTL	[31] ICEDEBUG	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
WDT_CTL	[31] ICEDEBUG	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
WDT_CTL	[11:8] TOUTSEL	WDT Time-out Interval Selection (Write Protect)
WDT_CTL	[7] WDTEN	WDT Enable Bit (Write Protect)
WDT_CTL	[6] INTEN	WDT Time-out Interrupt Enable Bit (Write Protect)
WDT_CTL	[5] WKF	WDT Time-out Wake-up Flag (Write Protect)
WDT_CTL	[4] WKEN	WDT Time-out Wake-up Function Control (Write Protect)
WDT_CTL	[1] RSTEN	WDT Time-out Reset Enable Bit (Write Protect)
WDT_ALTCTL	[1:0] RSTDSEL	WDT Reset Delay Selection (Write Protect)
BPWM_CTL0	[31] DBGTRIOFF	ICE Debug Mode Acknowledge Disable (Write Protect)
BPWM_CTL0	[30] DBGHALT	ICE Debug Mode Counter Halt (Write Protect)
PWM_CTL0	[31] DBGTRIOFF	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
PWM_CTL0	[30] DBGHALT	ICE Debug Mode Counter Halt (Write Protect)
PWM_DTCTL0_1	[24] DTCKSEL	Dead-time Clock Select (Write Protect)
PWM_DTCTL0_1	[16] DTEN	Enable Dead-time Insertion for PWM Pair (PWM_CH0, PWM_CH1) (PWM_CH2, PWM_CH3) (PWM_CH4, PWM_CH5) (Write Protect)
PWM_DTCTL0_1	[11:0] DTCNT	Dead-time Counter (Write Protect)

PWM_DTCTL2_3	[24] DTCKSEL	Dead-time Clock Select (Write Protect)
PWM_DTCTL2_3	[16] DTEN	Enable Dead-time Insertion for PWM Pair (PWM_CH0, PWM_CH1) (PWM_CH2, PWM_CH3) (PWM_CH4, PWM_CH5) (Write Protect)
PWM_DTCTL2_3	[11:0] DTCNT	Dead-time Counter (Write Protect)
PWM_DTCTL4_5	[24] DTCKSEL	Dead-time Clock Select (Write Protect)
PWM_DTCTL4_5	[16] DTEN	Enable Dead-time Insertion for PWM Pair (PWM_CH0, PWM_CH1) (PWM_CH2, PWM_CH3) (PWM_CH4, PWM_CH5) (Write Protect)
PWM_DTCTL4_5	[11:0] DTCNT	Dead-time Counter (Write Protect)
PWM_BRKCTL0_1	[19:18] BRKAODD	PWM Brake Action Select for Odd Channel (Write Protect)
PWM_BRKCTL0_1	[17:16] BRKAEVEN	PWM Brake Action Select for Even Channel (Write Protect)
PWM_BRKCTL0_1	[15] SYSLBEN	Enable System Fail As Level-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[13] BRKP1LEN	Enable BKP1 Pin As Level-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[12] BRKP0LEN	Enable BKP0 Pin As Level-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[9] CPO1LBEN	Enable ACMP1_O Digital Output As Level-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[8] CPO0LBEN	Enable ACMP0_O Digital Output As Level-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[7] SYSEBEN	Enable System Fail As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[5] BRKP1EEN	Enable PWMx_BRAKE1 Pin As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[4] BRKP0EEN	Enable PWMx_BRAKE0 Pin As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[1] CPO1EBEN	Enable ACMP1_O Digital Output As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[0] CPO0EBEN	Enable ACMP0_O Digital Output As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[19:18] BRKAODD	PWM Brake Action Select for Odd Channel (Write Protect)
PWM_BRKCTL2_3	[17:16] BRKAEVEN	PWM Brake Action Select for Even Channel (Write Protect)
PWM_BRKCTL2_3	[15] SYSLBEN	Enable System Fail As Level-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[13] BRKP1LEN	Enable BKP1 Pin As Level-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[12] BRKP0LEN	Enable BKP0 Pin As Level-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[9] CPO1LBEN	Enable ACMP1_O Digital Output As Level-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[8] CPO0LBEN	Enable ACMP0_O Digital Output As Level-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[7] SYSEBEN	Enable System Fail As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[5] BRKP1EEN	Enable PWMx_BRAKE1 Pin As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[4] BRKP0EEN	Enable PWMx_BRAKE0 Pin As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[1] CPO1EBEN	Enable ACMP1_O Digital Output As Edge-detect Brake Source (Write Protect)

PWM_BRKCTL2_3	[0] CPO0EBEN	Enable ACMP0_O Digital Output As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[19:18] BRKAODD	PWM Brake Action Select for Odd Channel (Write Protect)
PWM_BRKCTL4_5	[17:16] BRKAEVEN	PWM Brake Action Select for Even Channel (Write Protect)
PWM_BRKCTL4_5	[15] SYSLBEN	Enable System Fail As Level-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[13] BRKP1LEN	Enable BKP1 Pin As Level-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[12] BRKP0LEN	Enable BKP0 Pin As Level-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[9] CPO1LBEN	Enable ACMP1_O Digital Output As Level-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[8] CPO0LBEN	Enable ACMP0_O Digital Output As Level-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[7] SYSEBEN	Enable System Fail As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[5] BRKP1EEN	Enable PWMx_BRAKE1 Pin As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[4] BRKP0EEN	Enable PWMx_BRAKE0 Pin As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[1] CPO1EBEN	Enable ACMP1_O Digital Output As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[0] CPO0EBEN	Enable ACMP0_O Digital Output As Edge-detect Brake Source (Write Protect)
PWM_SWBRK	[8+n/2] n=0,2,4 BRKLTRGn	PWM Level Brake Software Trigger (Write Only) (Write Protect)
PWM_SWBRK	[n/2] n=0,2,4 BRKETRGn	PWM Edge Brake Software Trigger (Write Only) (Write Protect)
PWM_INTEN1	[10] BRKLIEN4_5	PWM Level-detect Brake Interrupt Enable for Channel4/5 (Write Protect)
PWM_INTEN1	[9] BRKLIEN2_3	PWM Level-detect Brake Interrupt Enable for Channel2/3 (Write Protect)
PWM_INTEN1	[8] BRKLIEN0_1	PWM Level-detect Brake Interrupt Enable for Channel0/1 (Write Protect)
PWM_INTEN1	[2] BRKEIEN4_5	PWM Edge-detect Brake Interrupt Enable for Channel4/5 (Write Protect)
PWM_INTEN1	[1] BRKEIEN2_3	PWM Edge-detect Brake Interrupt Enable for Channel2/3 (Write Protect)
PWM_INTEN1	[0] BRKEIEN0_1	PWM Edge-detect Brake Interrupt Enable for Channel0/1 (Write Protect)
PWM_INTSTS1	[8+n] n=0,1..5 BRKLIFn	PWM Channel n Level-detect Brake Interrupt Flag (Write Protect)
PWM_INTSTS1	[n] n=0,1..5 BRKEIFn	PWM Channel n Edge-detect Brake Interrupt Flag (Write Protect)
ADC_ADCR	[12] RESET	ADC RESET (Write Protect)

6.3.11 UART0_TXD/USCI0_DAT1 modulation with PWM

This chip supports UART0_TXD/USCI0_DAT1 to modulate with PWM channel. User can set MODPWMSEL(SYS_MODCTL[7:4]) to choose which PWM0 channel to modulate with UART0_TXD/USCI0_DAT1 and set MODEN(SYS_MODCTL[0]) to enable modulation function. User can set TXDINV(UART_LINE[8]) to inverse UART0_TXD or DATOINV(UUART_LINECTL[5]) to inverse USCI0_DAT1 before modulating with PWM.

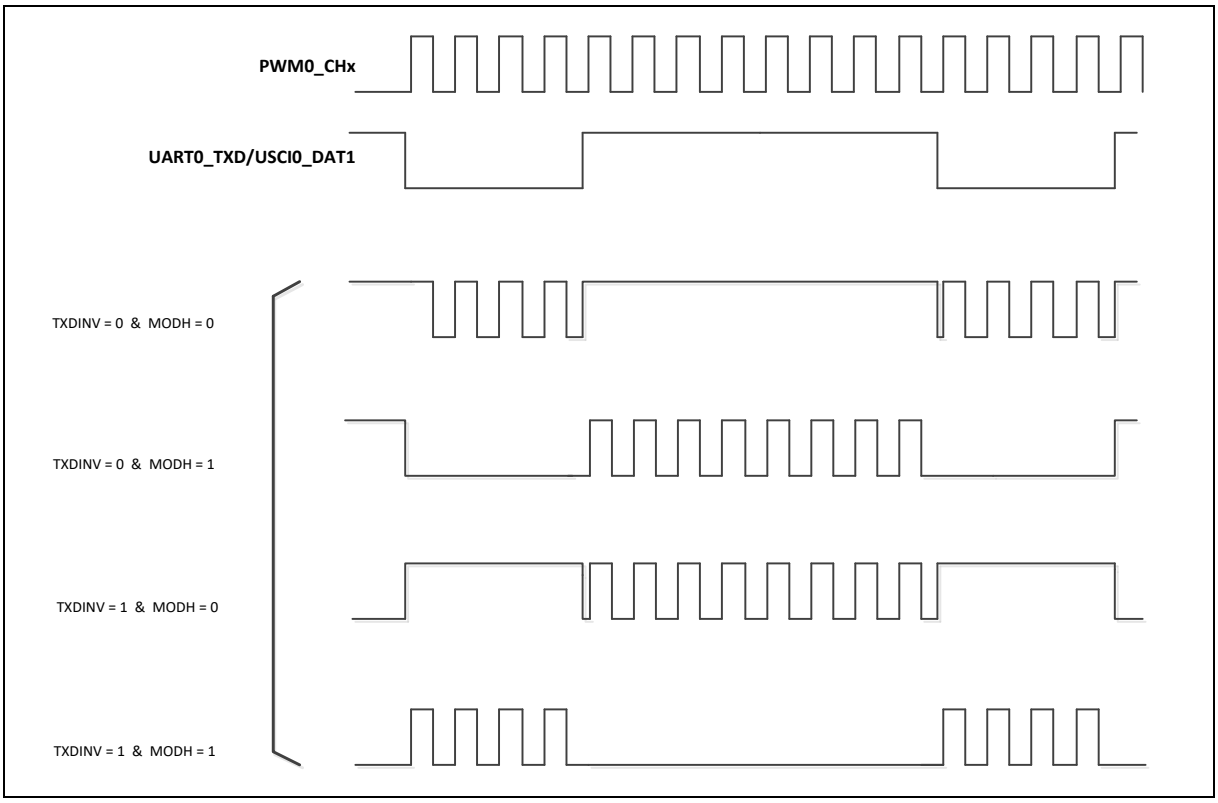


Figure 6.3-11 UART0_TXD/USCI0_DAT1 Modulated with PWM Channel

6.3.12 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “Arm® Cortex®-M0 Technical Reference Manual” and “Arm® v6-M Architecture Reference Manual”.

6.3.12.1 System Timer Control Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
SYST Base Address: **SCS_BA = 0xE000_E000**				
SYST_CTRL	SCS_BA+0x10	R/W	SysTick Control and Status Register	0x0000_0000
SYST_LOAD	SCS_BA+0x14	R/W	SysTick Reload Value Register	0xXXXX_XXXX
SYST_VAL	SCS_BA+0x18	R/W	SysTick Current Value Register	0xXXXX_XXXX

6.3.12.2 System Timer Control Register Description

SysTick Control and Status Register (SYST_CTRL)

Register	Offset	R/W	Description	Reset Value
SYST_CTRL	SCS_BA+0x10	R/W	SysTick Control and Status Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							COUNTFLAG
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					CLKSRC	TICKINT	ENABLE

Bits	Description	
[31:17]	**Reserved**	Reserved.
[16]	**COUNTFLAG**	**System Tick Counter Flag** Returns 1 if timer counted to 0 since last time this register was read. COUNTFLAG is set by a count transition from 1 to 0. COUNTFLAG is cleared on read or by a write to the Current Value register.
[15:3]	**Reserved**	Reserved.
[2]	**CLKSRC**	**System Tick Clock Source Selection** 0 = Clock source is the (optional) external reference clock. 1 = Core clock used for SysTick.
[1]	**TICKINT**	**System Tick Interrupt Enabled** 0 = Counting down to 0 does not cause the SysTick exception to be pended. Software can use COUNTFLAG to determine if a count to zero has occurred. 1 = Counting down to 0 will cause the SysTick exception to be pended. Clearing the SysTick current value register by a register write in software will not cause SysTick to be pended.
[0]	**ENABLE**	**System Tick Counter Enabled** 0 = Counter Disabled. 1 = Counter will operate in a multi-shot manner.

SysTick Reload Value Register (SYST_LOAD)

Register	Offset	R/W	Description	Reset Value
SYST_LOAD	SCS_BA+0x14	R/W	SysTick Reload Value Register	0xXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
RELOAD							
15	14	13	12	11	10	9	8
RELOAD							
7	6	5	4	3	2	1	0
RELOAD							

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:0]	**RELOAD**	**System Tick Reload Value** The value to load into the Current Value register when the counter reaches 0.

SysTick Current Value Register (SYST_VAL)

Register	Offset	R/W	Description	Reset Value
SYST_VAL	SCS_BA+0x18	R/W	SysTick Current Value Register	0xXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
CURRENT							
15	14	13	12	11	10	9	8
CURRENT							
7	6	5	4	3	2	1	0
CURRENT							

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:0]	**CURRENT**	**System Tick Current Value** Current counter value. This is the value of the counter at the time it is sampled. The counter does not provide read-modify-write protection. The register is write-clear. A software write of any value will clear the register to 0.

6.3.13 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor core and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "Arm® Cortex®-M0 Technical Reference Manual" and "Arm® v6-M Architecture Reference Manual".

6.3.13.1 Exception Model and System Interrupt Map

Table 6.3-8 lists the exception model supported by the M031BT/M032BT Series . Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as "0" and the lowest priority is denoted as "3". The default priority of all the user-configurable interrupts is "0". Note that priority "0" is treated as the fourth priority on the system, after three system exceptions "Reset", "NMI" and "Hard Fault".

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable

SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6.3-8 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BODOUT	Brown-Out low voltage detected interrupt
17	1	WDT_INT	Watchdog Timer interrupt
18	2	EINT024	External interrupt fromEINT0,2,4.
19	3	EINT135	External interrupt fromEINT1.3.5
20	4	GPABGH_INT	External interrupt from PA, PB, PG, PH pin
21	5	GPCDEF_INT	External interrupt from PC, PD, PE, PF pin
22	6	PWM0_INT	PWM0 interrupt
23	7	PWM1_INT	PWM1 interrupt
24	8	TMR0_INT	Timer 0 interrupt
25	9	TMR1_INT	Timer 1 interrupt
26	10	TMR2_INT	Timer 2 interrupt
27	11	TMR3_INT	Timer 3 interrupt
28	12	UART02_INT	UART0,2 interrupt
29	13	UART13_INT	UART1,3 interrupt
30	14	SPI0_INT	SPI0 interrupt
31	15	QSPI0_INT	QSPI0 interrupt
32	16	Reserved	Reserved
33	17	UART57_INT	UART5,7 interrupt
34	18	I2C0_INT	I2C0 interrupt
35	19	I2C1_INT	I2C1 interrupt
36	20	BPWM0_INT	BPWM0 interrupt
37	21	BPWM1_INT	BPWM1 interrupt
38	22	USCI01	USCI0,1 interrupt
39	23	USBD_INT	USB device interrupt
40	24	Reserved	Reserved
41	25	ACMP01_INT	ACMP0 and ACMP1 interrupt
42	26	PDMA_INT	PDMA interrupt
43	27	UART46_INT	UART4,6 interrupt

44	28	PWRWU_INT	Clock controller interrupt for chip wake-up from power-down state
45	29	ADC_INT	ADC interrupt
46	30	CLKFAIL	Clock fail detected or IRC Auto Trim interrupt or SRAM parity check error interrupt
47	31	RTC_INT	RTC interrupt

Table 6.3-9 Interrupt Number Table

6.3.13.2 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For Armv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 7.2-10 Vector Figure Format

6.3.13.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not be activated. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.3.13.4 NVIC Control Registers

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
NVIC Base Address: **NVIC_BA = 0xE000_E100**				
NVIC_ISER0	NVIC_BA+0x000	R/W	IRQ0 ~ IRQ31 Set-enable Control Register	0x0000_0000
NVIC_ICER0	NVIC_BA+0x080	R/W	IRQ0 ~ IRQ31 Clear-enable Control Register	0x0000_0000
NVIC_ISPR0	NVIC_BA+0x100	R/W	IRQ0 ~ IRQ31 Set-pending Control Register	0x0000_0000
NVIC_ICPR0	NVIC_BA+0x180	R/W	IRQ0 ~ IRQ31 Clear-pending Control Register	0x0000_0000
NVIC_IABR0	NVIC_BA+0x200	R/W	IRQ0 ~ IRQ31 Active Bit Register	0x0000_0000
NVIC_IPRn **n=0,1..7**	0xE000E400 +0x4*n	R/W	IRQ0 ~ IRQ31 Priority Control Register	0x0000_0000
STIR	0xE000EF00	R/W	Software Trigger Interrupt Registers	0x0000_0000

IRQ0 ~ IRQ31 Set-enable Control Register (NVIC_ISER0)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER0	NVIC_BA+0x000	R/W	IRQ0 ~ IRQ31 Set-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETENA							

Bits	Description	
[31:0]	**SETENA**	**Interrupt Set Enable Bit** The NVIC_ISER0 registers enable interrupts, and show which interrupts are enabled Write Operation: 0 = No effect. 1 = Interrupt Enabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ31 Clear-enable Control Register (NVIC_ICER0)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER0	NVIC_BA+0x080	R/W	IRQ0 ~ IRQ31 Clear-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALENA							

Bits	Description	
[31:0]	**CALENA**	**Interrupt Clear Enable Bit** The NVIC_ICER0 registers disable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Disabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ31 Set-pending Control Register (NVIC_ISPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR0	NVIC_BA+0x100	R/W	IRQ0 ~ IRQ31 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0 registers force interrupts into the pending state, and show which interrupts are pending Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ31 Clear-pending Control Register (NVIC_ICPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR0	NVIC_BA+0x180	R/W	IRQ0 ~ IRQ31 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0 registers remove the pending state from interrupts, and show which interrupts are pending Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ31 Active Bit Register (NVIC_IABR0)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR0	NVIC_BA+0x200	R/W	IRQ0 ~ IRQ31 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0 registers indicate which interrupts are active. 0 = interrupt not active. 1 = interrupt active.

IRQ0 ~ IRQ31 Interrupt Priority Register (NVIC_IPRn)

Register	Offset	R/W	Description	Reset Value
NVIC_IPRn n=0,1..7	0xE000E400 +0x4*n	R/W	IRQ0 ~ IRQ31 Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_4n_3		Reserved					
23	22	21	20	19	18	17	16
PRI_4n_2		Reserved					
15	14	13	12	11	10	9	8
PRI_4n_1		Reserved					
7	6	5	4	3	2	1	0
PRI_4n_0		Reserved					

Bits	Description	
[31:30]	**PRI_4n_3**	**Priority of IRQ_4n+3** "0" denotes the highest priority and "3" denotes the lowest priority
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_4n_2**	**Priority of IRQ_4n+2** "0" denotes the highest priority and "3" denotes the lowest priority
[21:16]	**Reserved**	Reserved.
[15:14]	**PRI_4n_1**	**Priority of IRQ_4n+1** "0" denotes the highest priority and "3" denotes the lowest priority
[13:8]	**Reserved**	Reserved.
[7:6]	**PRI_4n_0**	**Priority of IRQ_4n+0** "0" denotes the highest priority and "3" denotes the lowest priority
[5:0]	**Reserved**	Reserved.

Software Trigger Interrupt Register (STIR)

Register	Offset	R/W	Description	Reset Value
STIR	0xE000EF00	R/W	Software Trigger Interrupt Registers	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							INTID
7	6	5	4	3	2	1	0
INTID							

Bits	Description	
[31:9]	**Reserved**	Reserved.
[8:0]	**INTID**	**Interrupt ID** Write to the STIR To Generate An Interrupt from Software When the USERSETMPEND bit in the SCR is set to 1, unprivileged software can access the STIR Interrupt ID of the interrupt to trigger, in the range 0-31. For example, a value of 0x03 specifies interrupt IRQ3.

6.3.13.5 NMI Control Registers

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
NMI Base Address: **NMI_BA = 0x4000_0300**				
NMIEN	NMI_BA+0x00	R/W	NMI Source Interrupt Enable Register	0x0000_0000
NMISTS	NMI_BA+0x04	R	NMI Source Interrupt Status Register	0x0000_0000

NMI Source Interrupt Enable Register (NMIEN)

Register	Offset	R/W	Description	Reset Value
NMIEN	NMI_BA+0x00	R/W	NMI Source Interrupt Enable Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
UART1_INT	UART0_INT	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
7	6	5	4	3	2	1	0
Reserved	RTC_INT	Reserved	CLKFAIL	SRAM_PERR	PWRWU_INT	IRC_INT	BODOUT

Bits	Description	
[31:16]	**Reserved**	Reserved.
[15]	**UART1_INT**	**UART1 NMI Source Enable (Write Protect)** 0 = UART1 NMI source Disabled. 1 = UART1 NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[14]	**UART0_INT**	**UART0 NMI Source Enable (Write Protect)** 0 = UART0 NMI source Disabled. 1 = UART0 NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[13]	**EINT5**	**External Interrupt From PB.7, PD.12 or PF.14 Pin NMI Source Enable (Write Protect)** 0 = External interrupt from PB.7, PD.12 or PF.14 pin NMI source Disabled. 1 = External interrupt from PB.7, PD.12 or PF.14 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[12]	**EINT4**	**External Interrupt From PA.8, PB.6 or PF.15 Pin NMI Source Enable (Write Protect)** 0 = External interrupt from PA.8, PB.6 or PF.15 pin NMI source Disabled. 1 = External interrupt from PA.8, PB.6 or PF.15 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[11]	**EINT3**	**External Interrupt From PB.2 or PC.7 Pin NMI Source Enable (Write Protect)** 0 = External interrupt from PB.2 or PC.7 pin NMI source Disabled. 1 = External interrupt from PB.2 or PC.7 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[10]	**EINT2**	**External Interrupt From PB.3 or PC.6 Pin NMI Source Enable (Write Protect)** 0 = External interrupt from PB.3 or PC.6 pin NMI source Disabled. 1 = External interrupt from PB.3 or PC.6 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.

[9]	**EINT1**	**External Interrupt From PA.7, PB.4 or PD.15 Pin NMI Source Enable (Write Protect)** 0 = External interrupt from PA.7, PB.4 or PD.15 pin NMI source Disabled. 1 = External interrupt from PA.7, PB.4 or PD.15 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[8]	**EINT0**	**External Interrupt From PA.6 or PB.5 Pin NMI Source Enable (Write Protect)** 0 = External interrupt from PA.6 or PB.5 pin NMI source Disabled. 1 = External interrupt from PA.6 or PB.5 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[7]	**Reserved**	Reserved.
[6]	**RTC_INT**	**RTC NMI Source Enable (Write Protect)** 0 = RTC NMI source Disabled. 1 = RTC NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[5]	**Reserved**	Reserved.
[4]	**CLKFAIL**	**Clock Fail Detected and IRC Auto Trim Interrupt NMI Source Enable (Write Protect)** 0 = Clock fail detected and IRC Auto Trim interrupt NMI source Disabled. 1 = Clock fail detected and IRC Auto Trim interrupt NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[3]	**SRAM_PERR**	**SRAM ParityCheck Error NMI Source Enable (Write Protect)** 0 = SRAM parity check error NMI source Disabled. 1 = SRAM parity check error NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[2]	**PWRWU_INT**	**Power-down Mode Wake-up NMI Source Enable (Write Protect)** 0 = Power-down mode wake-up NMI source Disabled. 1 = Power-down mode wake-up NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[1]	**IRC_INT**	**IRC TRIM NMI Source Enable (Write Protect)** 0 = IRC TRIM NMI source Disabled. 1 = IRC TRIM NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[0]	**BODOUT**	**BOD NMI Source Enable (Write Protect)** 0 = BOD NMI source Disabled. 1 = BOD NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.

NMI Source Interrupt Status Register (NMISTS)

Register	Offset	R/W	Description	Reset Value
NMISTS	NMI_BA+0x04	R	NMI Source Interrupt Status Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
UART1_INT	UART0_INT	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
7	6	5	4	3	2	1	0
Reserved	RTC_INT	Reserved	CLKFAIL	SRAM_PERR	PWRWU_INT	IRC_INT	BODOUT

Bits	Description	
[31:16]	**Reserved**	Reserved.
[15]	**UART1_INT**	**UART1 Interrupt Flag (Read Only)** 0 = UART1 interrupt is deasserted. 1 = UART1 interrupt is asserted.
[14]	**UART0_INT**	**UART0 Interrupt Flag (Read Only)** 0 = UART1 interrupt is deasserted. 1 = UART1 interrupt is asserted.
[13]	**EINT5**	**External Interrupt From PB.7 or PF.14 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PB.7 or PF.14 interrupt is deasserted. 1 = External Interrupt from PB.7 or PF.14 interrupt is asserted.
[12]	**EINT4**	**External Interrupt From PA.8, PB.6 or PF.15 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PA.8, PB.6 or PF.15 interrupt is deasserted. 1 = External Interrupt from PA.8, PB.6 or PF.15 interrupt is asserted.
[11]	**EINT3**	**External Interrupt From PB.2 or PC.7 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PB.2 or PC.7 interrupt is deasserted. 1 = External Interrupt from PB.2 or PC.7 interrupt is asserted.
[10]	**EINT2**	**External Interrupt From PB.3 or PC.6 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PB.3 or PC.6 interrupt is deasserted. 1 = External Interrupt from PB.3 or PC.6 interrupt is asserted.
[9]	**EINT1**	**External Interrupt From PA.7, PB.4 or PD.15 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PA.7, PB.4 or PD.15 interrupt is deasserted. 1 = External Interrupt from PA.7, PB.4 or PD.15 interrupt is asserted.
[8]	**EINT0**	**External Interrupt From PA.6 or PB.5 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PA.6 or PB.5 interrupt is deasserted.

		1 = External Interrupt from PA.6 or PB.5 interrupt is asserted.
[7]	**Reserved**	Reserved.
[6]	**RTC_INT**	**RTC Interrupt Flag (Read Only)** 0 = RTC interrupt is deasserted. 1 = RTC interrupt is asserted.
[5]	**Reserved**	Reserved.
[4]	**CLKFAIL**	**Clock Fail Detected or IRC Auto Trim Interrupt Flag (Read Only)** 0 = Clock fail detected or IRC Auto Trim interrupt is deasserted. 1 = Clock fail detected or IRC Auto Trim interrupt is asserted.
[3]	**SRAM_PERR**	**SRAM ParityCheck Error Interrupt Flag (Read Only)** 0 = SRAM parity check error interrupt is deasserted. 1 = SRAM parity check error interrupt is asserted.
[2]	**PWRWU_INT**	**Power-down Mode Wake-up Interrupt Flag (Read Only)** 0 = Power-down mode wake-up interrupt is deasserted. 1 = Power-down mode wake-up interrupt is asserted.
[1]	**IRC_INT**	**IRC TRIM Interrupt Flag (Read Only)** 0 = HIRC TRIM interrupt is deasserted. 1 = HIRC TRIM interrupt is asserted.
[0]	**BODOUT**	**BOD Interrupt Flag (Read Only)** 0 = BOD interrupt is deasserted. 1 = BOD interrupt is asserted.

6.3.14 System Control Register

The Cortex®-M0 status and operation mode control are managed by System Control Registers. Including CPUID, Cortex®-M0 interrupt priority and Cortex®-M0 power management can be controlled through these system control registers.

For more detailed information, please refer to the "*Arm® Cortex®-M0 Technical Reference Manual*" and "*Arm® v6-M Architecture Reference Manual*".

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
SCR Base Address: **SCS_BA = 0xE000_E000**				
ICSR	SCS_BA+0xD04	R/W	Interrupt Control and State Register	0x0000_0000
VTOR	SCS_BA+0xD08	R/W	Vector Table Offset Register	0x0000_0000
AIRCR	SCS_BA+0xD0C	R/W	Application Interrupt and Reset Control Register	0xFA05_0000
SCR	SCS_BA+0xD10	R/W	System Control Register	0x0000_0000
SHPR1	SCS_BA+0xD18	R/W	System Handler Priority Register 1	0x0000_0000
SHPR2	SCS_BA+0xD1C	R/W	System Handler Priority Register 2	0x0000_0000
SHPR3	SCS_BA+0xD20	R/W	System Handler Priority Register 3	0x0000_0000

Interrupt Control State Register (ICSR)

Register	Offset	R/W	Description	Reset Value
ICSR	SCS_BA+0xD04	R/W	Interrupt Control and State Register	0x0000_0000

31	30	29	28	27	26	25	24
NMIPENDSET	Reserved		PENDSVSET	PENDSVCLR	PENDSTSET	PENDSTCLR	Reserved
23	22	21	20	19	18	17	16
ISRPREEMPT	ISRPENDING	Reserved				VECTPENDING	
15	14	13	12	11	10	9	8
VECTPENDING				RETTOBASE	Reserved		
7	6	5	4	3	2	1	0
Reserved		VECTACTIVE					

Bits	Description	
[31]	**NMIPENDSET**	**NMI Set-pending Bit** Write Operation: 0 = No effect. 1 = Changes NMI exception state to pending. Read Operation: 0 = NMI exception is not pending. 1 = NMI exception is pending. **Note:** Because NMI is the highest-priority exception, normally the processor enters the NMI exception handler as soon as it detects a write of 1 to this bit. Entering the handler then clears this bit to 0. This means a read of this bit by the NMI exception handler returns 1 only if the NMI signal is reasserted while the processor is executing that handler.
[30:29]	**Reserved**	Reserved.
[28]	**PENDSVSET**	**PendSV Set-pending Bit** Write Operation: 0 = No effect. 1 = Changes PendSV exception state to pending. Read Operation: 0 = PendSV exception is not pending. 1 = PendSV exception is pending. **Note:** Writing 1 to this bit is the only way to set the PendSV exception state to pending.
[27]	**PENDSVCLR**	**PendSV Clear-pending Bit** Write Operation: 0 = No effect. 1 = Removes the pending state from the PendSV exception. **Note:** This is a write only bit. To clear the PENDSV bit, you must “write 0 to PENDSVSET and write 1 to PENDSVRTC_CAL” at the same time.

[26]	**PENDSTSET**	**SysTick Exception Set-pending Bit** Write Operation: 0 = No effect. 1 = Changes SysTick exception state to pending. Read Operation: 0 = SysTick exception is not pending. 1 = SysTick exception is pending.
[25]	**PENDSTCLR**	**SysTick Exception Clear-pending Bit** Write Operation: 0 = No effect. 1 = Removes the pending state from the SysTick exception. **Note:** This is a write only bit. To clear the PENDST bit, you must "write 0 to PENDSTSET and write 1 to PENDSTRTC_CAL" at the same time.
[24]	**Reserved**	Reserved.
[23]	**ISRPREEMPT**	**Interrupt Preempt Bit (Read Only)** If set, a pending exception will be serviced on exit from the debug halt state.
[22]	**ISRPENDING**	**Interrupt Pending Flag, Excluding NMI and Faults (Read Only)** 0 = Interrupt not pending. 1 = Interrupt pending.
[21:18]	**Reserved**	Reserved.
[17:12]	**VECTPENDING**	**Number of the Highest Pended Exception** Indicate the Exception Number of the Highest Priority Pending Enabled Exception 0 = no pending exceptions. Nonzero = the exception number of the highest priority pending enabled exception. The value indicated by this field includes the effect of the BASEPRI and FAULTMASK registers, but not any effect of the PRIMASK register.
[11]	**RETTOBASE**	**Preempted Active Exceptions Indicator** Indicate whether There are Preempted Active Exceptions 0 = there are preempted active exceptions to execute. 1 = there are no active exceptions, or the currently-executing exception is the only active exception.
[10:6]	**Reserved**	Reserved.
[5:0]	**VECTACTIVE**	**Number of the Current Active Exception** 0 = Thread mode. Non-zero = The exception number of the currently active exception.

Vector Table Offset Register (VTOR)

Register	Offset	R/W	Description	Reset Value
VTOR	SCS_BA+0xD08	R/W	Vector Table Offset Register	0x0000_0000

31	30	29	28	27	26	25	24
TBLOFF							
23	22	21	20	19	18	17	16
TBLOFF							
15	14	13	12	11	10	9	8
TBLOFF							
7	6	5	4	3	2	1	0
TBLOFF	Reserved						

Bits	Description	
[31:7]	**TBLOFF**	**Table Offset Bits** The vector table address for the selected Security state.
[6:0]	**Reserved**	Reserved.

Application Interrupt and Reset Control Register (AIRCR)

Register	Offset	R/W	Description	Reset Value
AIRCR	SCS_BA+0xD0C	R/W	Application Interrupt and Reset Control Register	0xFA05_0000

31	30	29	28	27	26	25	24
VECTORKEY							
23	22	21	20	19	18	17	16
VECTORKEY							
15	14	13	12	11	10	9	8
ENDIANNESS	Reserved				PRIGROUP		
7	6	5	4	3	2	1	0
Reserved					SYSRESETREQ	VECTCLRACTIVE	VECTRESET

Bits	Description	
[31:16]	**VECTORKEY**	**Register Access Key** When writing this register, this field should be 0x05FA, otherwise the write action will be unpredictable. The VECTORKEY filed is used to prevent accidental write to this register from resetting the system or clearing of the exception status.
[15]	**ENDIANNESS**	**Data Endianness** 0 = Little-endian. 1 = Big-endian.
[14:11]	**Reserved**	Reserved.
[10:8]	**PRIGROUP**	**Interrupt Priority Grouping** This field determines the Split Of Group priority from subpriority,
[7:3]	**Reserved**	Reserved.
[2]	**SYSRESETREQ**	**System Reset Request** Writing This Bit to 1 Will Cause A Reset Signal To Be Asserted To The Chip And Indicate A Reset Is Requested This bit is write only and self-cleared as part of the reset sequence.
[1]	**VECTCLRACTIVE**	**Exception Active Status Clear Bit** Setting This Bit To 1 Will Clears All Active State Information For Fixed And Configurable Exceptions This bit is write only and can only be written when the core is halted. **Note:** It is the debugger's responsibility to re-initialize the stack.
[0]	**VECTRESET**	Reserved.

PRIGROUP	Binary Point	Group Priority Bits	Subpriority Bits	Number Of Group Priorities	Subpriorities
0b000	bxxxxxxx.y	[7:1]	[0]	128	2
0b001	bxxxxxx.yy	[7:2]	[1:0]	64	4
0b010	bxxxxx.yyy	[7:3]	[2:0]	32	8
0b011	bxxxx.yyyy	[7:4]	[3;0]	16	16
0b100	bxxx.yyyyy	[7:5]	[4:0]	8	32
0b101	bxx.yyyyyy	[7:6]	[5:0]	4	64
0b110	bx.yyyyyyy	[7]	[6:0]	2	128
0b111	b.yyyyyyyy	None	[7:0]	1	256

Table 6.3-10 Priority Grouping

System Control Register (SCR)

Register	Offset	R/W	Description	Reset Value
SCR	SCS_BA+0xD10	R/W	System Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved			SEVONPEND	Reserved	SLEEPDEEP	SLEEPONEXIT	Reserved

Bits	Description	
[31:5]	**Reserved**	Reserved.
[4]	**SEVONPEND**	**Send Event on Pending** 0 = Only enabled interrupts or events can wake up the processor, while disabled interrupts are excluded. 1 = Enabled events and all interrupts, including disabled interrupts, can wake up the processor. When an event or interrupt enters pending state, the event signal wakes up the processor from WFE. If the processor is not waiting for an event, the event is registered and affects the next WFE. The processor also wakes up on execution of an SEV instruction or an external event.
[3]	**Reserved**	Reserved.
[2]	**SLEEPDEEP**	**Processor Deep Sleep and Sleep Mode Selection** Control Whether the Processor Uses Sleep Or Deep Sleep as its Low Power Mode. 0 = Sleep. 1 = Deep sleep.
[1]	**SLEEPONEXIT**	**Sleep-on-exit Enable Control** This bit indicate Sleep-On-Exit when Returning from Handler Mode to Thread Mode. 0 = Do not sleep when returning to Thread mode. 1 = Enters sleep, or deep sleep, on return from an ISR to Thread mode. Setting this bit to 1 enables an interrupt driven application to avoid returning to an empty main application.
[0]	**Reserved**	Reserved.

System Handler Priority Register 1 (SHPR1)

Register	Offset	R/W	Description	Reset Value
SHPR1	SCS_BA+0xD18	R/W	System Handler Priority Register 1	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_6							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_5							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_4							

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:16]	**PRI_6**	Priority of system handler 6, UsageFault
[15:8]	**PRI_5**	Priority of system handler 5, BusFault
[7:0]	**PRI_4**	Priority of system handler 4, MemManage

System Handler Priority Register 2 (SHPR2)

Register	Offset	R/W	Description	Reset Value
SHPR2	SCS_BA+0xD1C	R/W	System Handler Priority Register 2	0x0000_0000

31	30	29	28	27	26	25	24
PRI_11		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[31:30]	**PRI_11**	**Priority of System Handler 11 – SVCall** “0” denotes the highest priority and “3” denotes the lowest priority.
[29:0]	**Reserved**	Reserved.

System Handler Priority Register 3 (SHPR3)

Register	Offset	R/W	Description	Reset Value
SHPR3	SCS_BA+0xD20	R/W	System Handler Priority Register 3	0x0000_0000

31	30	29	28	27	26	25	24
PRI_15		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_14		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[31:30]	**PRI_15**	**Priority of System Handler 15 – SysTick** "0" denotes the highest priority and "3" denotes the lowest priority.
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_14**	**Priority of System Handler 14 – PendSV** "0" denotes the highest priority and "3" denotes the lowest priority.

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

This chip is equipped with 64/128/256/512 Kbytes on-chip embedded Flash (the chip with 512 Kbytes consists of two 256 Kbytes BANK0 and BANK1). A User Configuration block is provided for system initialization. A loader ROM (LDROM) is used for In-System-Programming (ISP) function. A security protection ROM (SPROM) can conceal user program. For M032BTxG/I, a 4 Kbytes cache with zero wait cycle is implemented to improve the performance of code/data fetching. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without the chip reset after the embedded Flash is updated.

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

This chip has up to 111 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 111 pins are arranged in 5 ports named as PA, PB, PC, PD, PE, PF, PG and PH. PA and PB has 16 pins on port. PC has 15 pins on port. PD and PE has 16 pins on port. PF has 14 pins on port. PG has 10 pins on port. PH has 8 pins on port. Each of the 111 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (CONFIG0[10]).

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- I/O pin can be configured as interrupt source with edge/level setting
- Input schmitt trigger function
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in input mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the wake-up function

6.6 PDMA Controller (PDMA)

6.6.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 9 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.6.2 Features

- Supports 9 independently configurable channels
- Selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and I^2C, SPI, UART, USCI, ADC, PWM , QSPI and TIMER request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on channel 0 and channel1

6.7 Timer Controller (TMR)

6.7.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.7.2 Features

6.7.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- Supports event counting source from internal USB SOF signal
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports internal capture triggered while internal ACMP output signal and LIRC transition
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, ADC, PDMA, BPWM function
- Supports Inter-Timer trigger mode

6.8 Watchdog Timer (WDT)

6.8.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.8.2 Features

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 416us ~ 27.3 s if WDT_CLK = 38.4 kHz (LIRC).
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT.

6.9 Window Watchdog Timer (WWDT)

6.9.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.9.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.10 Real Time Clock (RTC)

6.10.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

6.10.2 Features

- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK.
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register.
- Supports Leap Year indication in RTC_LEAPYEAR register.
- Supports Day of the Week counter in RTC_WEEKDAY register.
- Frequency of RTC clock source compensate by RTC_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports 1 Hz clock output.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.

6.11 Basic PWM Generator and Capture Timer (BPWM)

6.11.1 Overview

The chip provides two BPWM generators — BPWM0 and BPWM1. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for ADC to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.11.2 Features

6.11.2.1 BPWM Function Features

- Supports maximum clock frequency up to 144 MHz.
- Supports up to two BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger ADC in the following events:
  - BPWM counter matches 0, period value or compared value

6.11.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.12 PWM Generator and Capture Timer (PWM)

6.12.1 Overview

The chip provides two PWM generators — PWM0 and PWM1. Each PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM uses comparator compared with counter to generate events. These events use to generate PWM pulse, interrupt and trigger signal for ADC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, they have difference architecture. In Complementary mode, there are two comparators to generate various PWM pulse with 12-bit dead-time generator. For PWM output control unit, it supports polarity output, independent pin mask and brake functions.

The PWM generator also supports input capture function to latch PWM counter value to the corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

6.12.2 Features

6.12.2.1 PWM Function Features

- Supports maximum clock frequency up to 144 MHz
- Supports up to two PWM modules, each module provides 6 output channels
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channel
  - Dead-time insertion with 12-bit resolution
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution PWM counter
  - Up, down and up-down counter operation type
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
  - Brake source from pin and system safety events (clock failed, Brown-out detection, SRAM parity error and CPU lockup)
  - Noise filter for brake source from pin
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger ADC on the following events:
  - PWM counter matches 0, period value or compared value

6.12.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition

- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for PWM all channels

6.13 UART Interface Controller (UART)

6.13.1 Overview

The chip provides eight channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs Normal Speed UART and supports flow control function. The UART controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, RS-485 and Single-wire function modes and auto-baud rate measuring function.

6.13.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes or 1/1 byte entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function (Only UART0 /UART1 /UART4 /UART5 with Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function)
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - Support 9600 bps for UART_CLK is selected LXT. (Only UART0 /UART1 /UART4 /UART5 with this feature)
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function
- Support Single-wire function mode.

UART Feature	UART0/ UART1/ UART4/ UART5	UART2/ UART3/ UART6/ UART7	USCI-UART
FIFO	16 Bytes	1 Bytes	TX: 1byte

			RX: 2byte
Auto Flow Control (CTS/RTS)	√	√	√
IrDA	√	√	-
LIN	-	-	-
RS-485 Function Mode	√	√	√
nCTS Wake-up	√	√	√
Incoming Data Wake-up	√	√	√
Received Data FIFO reached threshold Wake-up	√	-	-
RS-485 Address Match (AAD mode) Wake-up	√	-	-
Auto-Baud Rate Measurement	√	√	√
STOP Bit Length	1, 1.5, 2 bit	1, 1.5, 2 bit	1, 2 bit
Word Length	5, 6, 7, 8 bits	5, 6, 7, 8 bits	6~13 bits
Even / Odd Parity	√	√	√
Stick Bit	√	√	-
Note: √= Supported			

Table 6.13-1 NuMicro® M031BT/M032BT Series UART Features

6.14 Serial Peripheral Interface (SPI)

6.14.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains one set of SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer.

6.14.2 Features

- SPI Mode
  - Supports one set of SPI controller
  - Supports Master or Slave mode operation
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers which depends on SPI setting of data width
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Master mode up to 16 MHz (when chip works at V_{DD} = 1.8~3.6V)
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
  - Supports PDMA transfer

6.15 Quad Serial Peripheral Interface (QSPI)

6.15.1 Overview

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains one QSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller supports 2-bit Transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O Transfer mode and the controller supports the PDMA function to access the data buffer.

6.15.2 Features

- Supports one QSPI controller
- Supports Master or Slave mode operation
- Master mode up to 24 MHz and Slave mode up to 16 MHz (when chip works at V_{DD} = 1.8~3.6V)
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports receive-only mode

6.16 I²C Serial Interface Controller (I²C)

6.16.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I²C controllers which support Power-down wake-up function.

6.16.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports setup/hold time programmable
- Supports Bus Management (SM/PM compatible) function

Section	Sub-Section	M031BTxD/E	M032BTxG/I
6.16.5 Functional Description	6.16.5.2 Operation Modes - Bus Management (SMBus/PMBus Compatiable) - Device Identification – Slave Address - Bus Protocols - Address Resolution Protocol (ARP) - Received Command and Data acknowledge control - Host Notify Protocol - Bus Management Alert - Packet Error Checking - Time-out - Bus Management Time-out: - Bus Clock Low Time-out: - Bus Idle Detection	-	•
Register Description	I2C Bus Manage Control Register (I2C_BUSCTL)	-	•

Section	Sub-Section	M031BTxD/E	M032BTxG/I
	I2C Bus Management Timer Control Register (I2C_BUSTCTL)	-	•
	I2C Bus Management Status Register (I2C_BUSSTS)	-	•
	I2C Byte Number Register (I2C_PKTSIZE)	-	•
	I2C PEC Value Register (I2C_PKTCRC)	-	•
	I2C Bus Management Timer Register (I2C_BUSTOUT)	-	•
	I2C Clock Low Timer Register (I2C_CLKTOUT)	-	•

Table 6.16-1 I^2C Feature Comparison Table at Different Chip

6.17 USCI - Universal Serial Control Interface Controller (USCI)

6.17.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

6.17.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

6.18 USCI – UART Mode

6.18.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter being independent, frames can start at different points in time for transmission and reception.

The UART controller also provides auto flow control. There are two conditions to wake-up the system.

6.18.2 Features

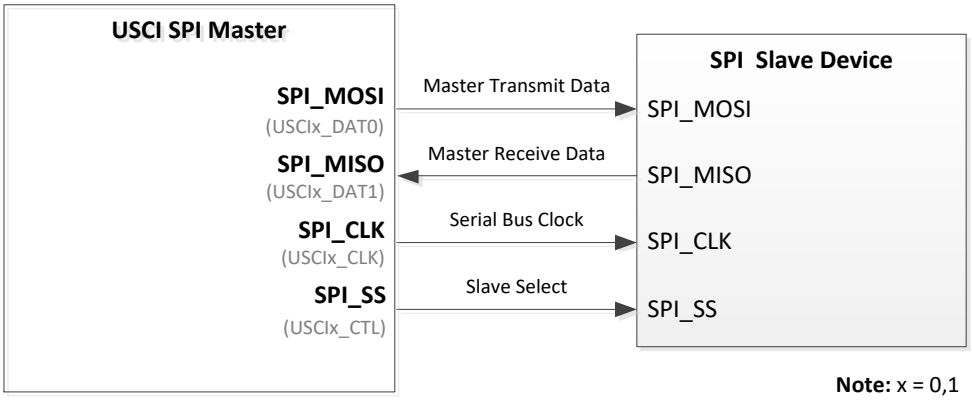
- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-bit Data Transfer (Support 9-bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports PDMA capability
- Supports Wake-up function (Data and nCTS Wakeup Only)

6.19 USCI - SPI Mode

6.19.1 Overview

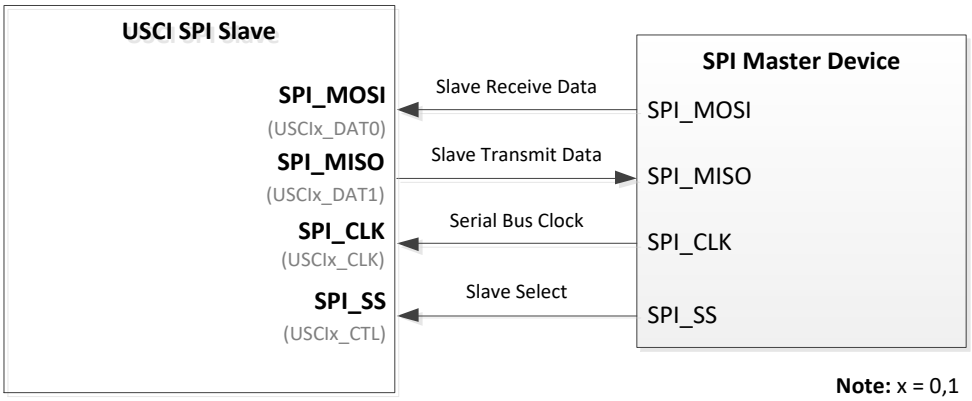
The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1

This SPI protocol can operate as Master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in Master and Slave mode are shown below.



Note: M031BT series doesn't support USCIx_CTL0 pin. User needs to use GPIO as SPI_SS pin.

Figure 6.19-1 SPI Master Mode Application Block Diagram



Note: M031BT series doesn't support USCIx_CTL0 pin, so it only supports SPI slave 3-wire mode.

Figure 6.19-2 SPI Slave Mode Application Block Diagram

6.19.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master = f_{PCLK} / 2, Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload

- Supports MSB first or LSB first transfer sequence
- Supports Word Suspend function
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

6.20 USCI - I²C Mode

6.20.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.20-1 for more detailed I²C BUS Timing.

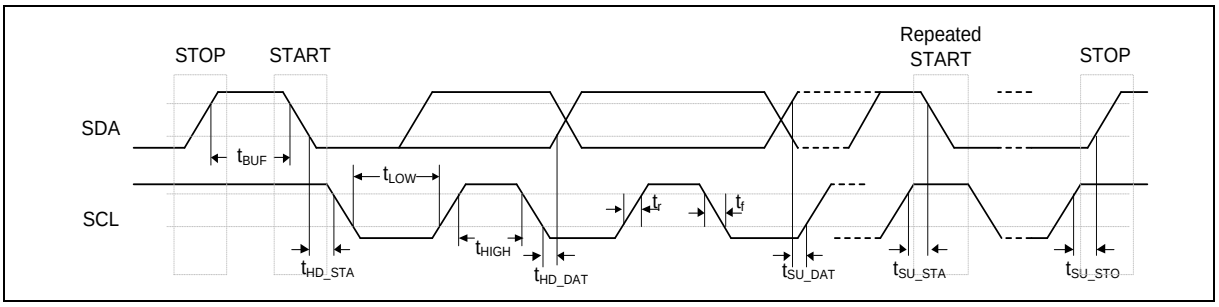


Figure 6.20-1 I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (UI2C_CTL [2:0]) = 100B. When enable this port, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

Note: Pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode .

6.20.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by received 'START' symbol or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

6.21 USB 2.0 Full-Speed Device Controller (USBD)

6.21.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/ isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 512 Bytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEGx).

There are 8 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the no-event-wake-up, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register USBD_EPSTS0 to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disable the SE0 bit, host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to Universal Serial Bus Specification Revision *2.0*.

6.21.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 5 different interrupt events (SOF, NEVWK, VBUSDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3 ms
- Supports 8 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 512 byte buffer size
- Provides remote wake-up capability

6.22 CRC Controller (CRC)

6.22.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

6.22.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

6.23 Hardware Divider (HDIV)

6.23.1 Overview

The hardware divider (HDIV) is useful to the high performance application. The hardware divider is a signed, integer divider with both quotient and remainder outputs.

6.23.2 Features

- Signed (two's complement) integer calculation
- 32-bit dividend with 16-bit divisor calculation capacity
- 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
- Divided by zero warning flag
- Write divisor to trigger calculation

6.24 Analog-to-Digital Converter (ADC)

6.24.1 Overview

The ADC contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with 16 input channels. The A/D converter supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin (STADC), timer0~3 overflow pulse trigger, PWM trigger or BPWM trigger.

6.24.2 Features

- Operating voltage: 1.8V~3.6V.
- Analog input voltage: 0 ~ AV_{DD}.
-
- 12-bit resolution and 10-bit accuracy is guaranteed.
- Up to 16 single-end analog input channels or 8 differential analog input channels.
- Maximum ADC peripheral clock frequency is 34 MHz.
- Up to 2 MSPS sampling rate.
- Scan on enabled channels
- Threshold voltage detection
- Four operation modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software Write 1 to ADST bit
  - External pin (STADC)
  - Timer 0~3 overflow pulse trigger
  - BPWM trigger
  - PWM trigger
- Each conversion result is held in data register of each channel with valid and overrun indicators.
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- Supports extend sample time function (0~255 ADC clock).
- One internal channel from band-gap voltage (V_{BG}).
- One internal channel from internal pull-up/down circuit.
- Supports PDMA transfer mode.
- Supports Calibration mode.

- Supports Floating Detect Function

Note1: ADC sampling rate = (ADC peripheral clock frequency) / (total ADC conversion cycle)

Note2: If the internal channel for band-gap voltage is active, the maximum sampling rate will be 300k SPS.

Note3: The ADC Clock frequency must be slower than or equal to PCLK.

Section	M031BTxD/E	M032BTxG/I
6.25.5.11 PWM trigger	•	•
6.25.5.12 BPWM trigger	-	•
6.25.5.17 Floating Detect Function	-	•

Table 6.24-1 ADC Features Comparison Table

6.25 Analog Comparator Controller (ACMP)

6.25.1 Overview

The chip provides two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

6.25.2 Features

- Analog input voltage range: 0 ~ AV_{DD} (voltage of AV_{DD} pin)
- Supports hysteresis function
- Supports wake-up function
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2, or ACMP0_P3
  - 3 negative sources:
    - ACMP0_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)
- ACMP1 supports
  - 4 multiplexed I/O pins at positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP1_P2, or ACMP1_P3
  - 3 negative sources:
    - ACMP1_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)
- Shares one ACMP interrupt vector for all comparators
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for PWM
- Supports window compare mode and window latch mode
- Supports calibration function

Section	Sub-Section	M031BTxD/E	M032BTxG/I
Function Description	6.26.5.7 Calibration function	-/●	●

Table 6.25-1 Calibration Function Features Comparison Table at Different Chip

6.26 Radio

6.26.1 Overview

This chip is equipped with an RF transceiver for wireless application use. The RF transceiver includes an RF radio and modulator/demodulator. It is fully compliant with the Bluetooth 5.0 standard and also supports proprietary 2.4 GHz protocols.

6.26.2 Features

- Modem with Integrated RF radio for 2.4 GHz Bluetooth communication link
- Compliant with Bluetooth 5 Low Energy Specification
- Supports proprietary 2.4 GHz protocols
- High TX power with low current (+8 dBm, 8 mA)
- Programmable output power from -20 dBm to +8 dBm
- Rx Sensitivity : -94 dBm at 1 Mbps
- Data rate: 1Mbps and 2Mbps
- 32 kHz low speed on-chip RC oscillator with deviation less than ± 500 ppm
- Dedicated 16/32 MHz high speed crystal
- RSSI read-out
- Integrated security engine for real-time processing of the data stream
  - AES-CCM
  - AES-128
  - CRC
- Two power modes for RF transceiver
  - DC-to-DC mode
  - LDO mode
- Five operating modes:
  - Deep Sleep
  - Sleep
  - Standby
  - Receive
  - Transmit

6.27 Peripherals Interconnection

6.27.1 Overview

Some peripherals have interconnections which allow autonomous communication or synchronous action between peripherals without needing to involve the CPU. Peripherals interact without CPU saves CPU resources, reduces power consumption, operates with no software latency and fast responds.

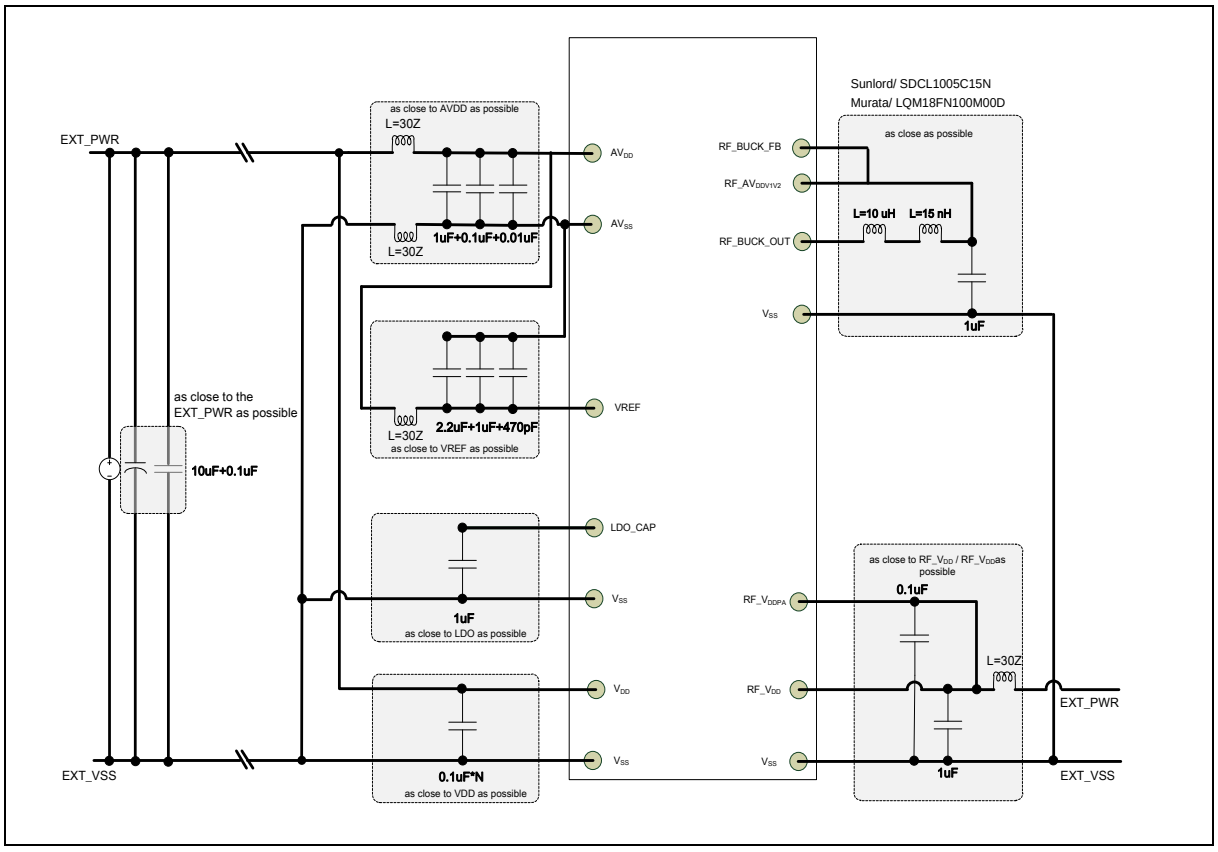
6.27.2 Peripherals Interconnect Matrix table

Source	Destination					
	ADC	HIRC TRIM	BPWM	PWM	Timer	UART/USCI
ACMP	-	-	-	3	6	-
BOD	-	-	-	3	-	-
Clock Fail	-	-	-	3	-	-
CPU Lockup	-	-	-	3	-	-
LIRC	-	-	-	-	6	-
HXT	-	-	-	-	-	
LXT	-	2		-	-	
BPWM	1		4	-	-	-
PWM	1	-	4	4	-	8
Timer	1	-	5	5	7	-
USBD	-	2	-	-	-	-

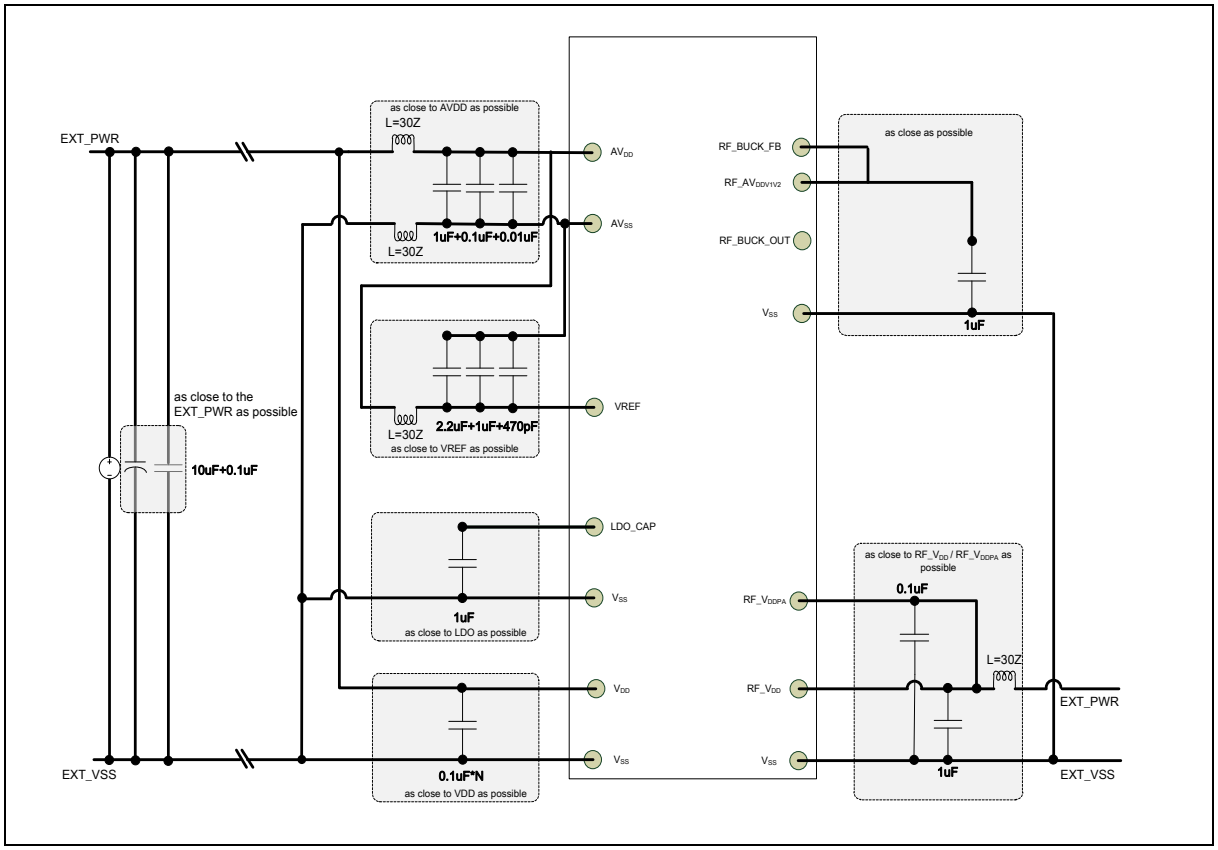
Table 6.27-1 Peripherals Interconnect Matrix table

7 APPLICATION CIRCUIT

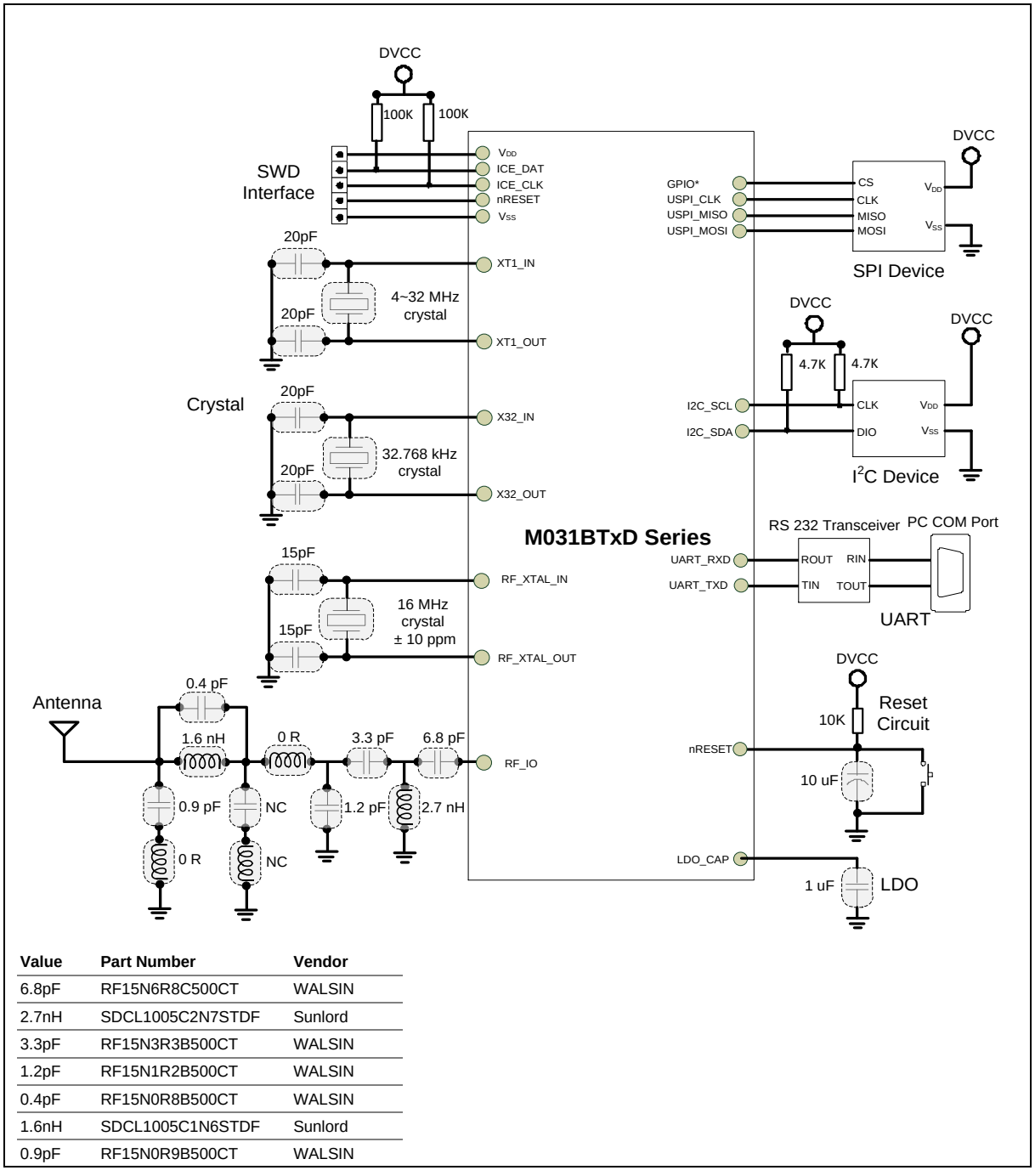
7.1 Power Supply Scheme (DC-to-DC Mode)



7.2 Power Supply Scheme (LDO Mode)



7.3 Peripheral Application Scheme (M031BTxD)



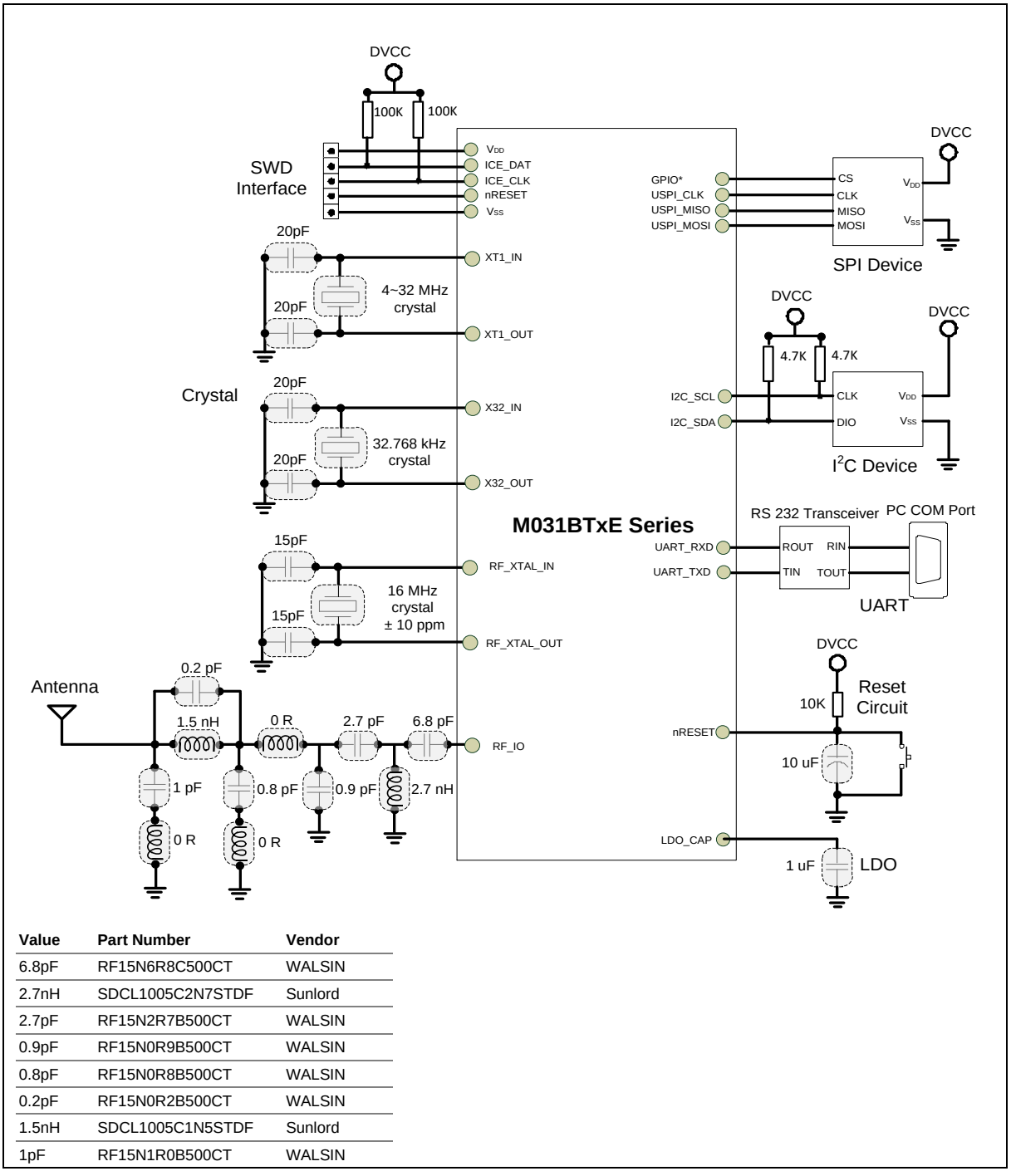
Value	Part Number	Vendor
6.8pF	RF15N6R8C500CT	WALSIN
2.7nH	SDCL1005C2N7STDF	Sunlord
3.3pF	RF15N3R3B500CT	WALSIN
1.2pF	RF15N1R2B500CT	WALSIN
0.4pF	RF15N0R8B500CT	WALSIN
1.6nH	SDCL1005C1N6STDF	Sunlord
0.9pF	RF15N0R9B500CT	WALSIN

Note 1: M031BT series doesn't support USCIx_CTL0 pin. User needs to use GPIO as SPI_SS pin.

Note 2: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 3: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

7.4 Peripheral Application Scheme (M031BTxE)



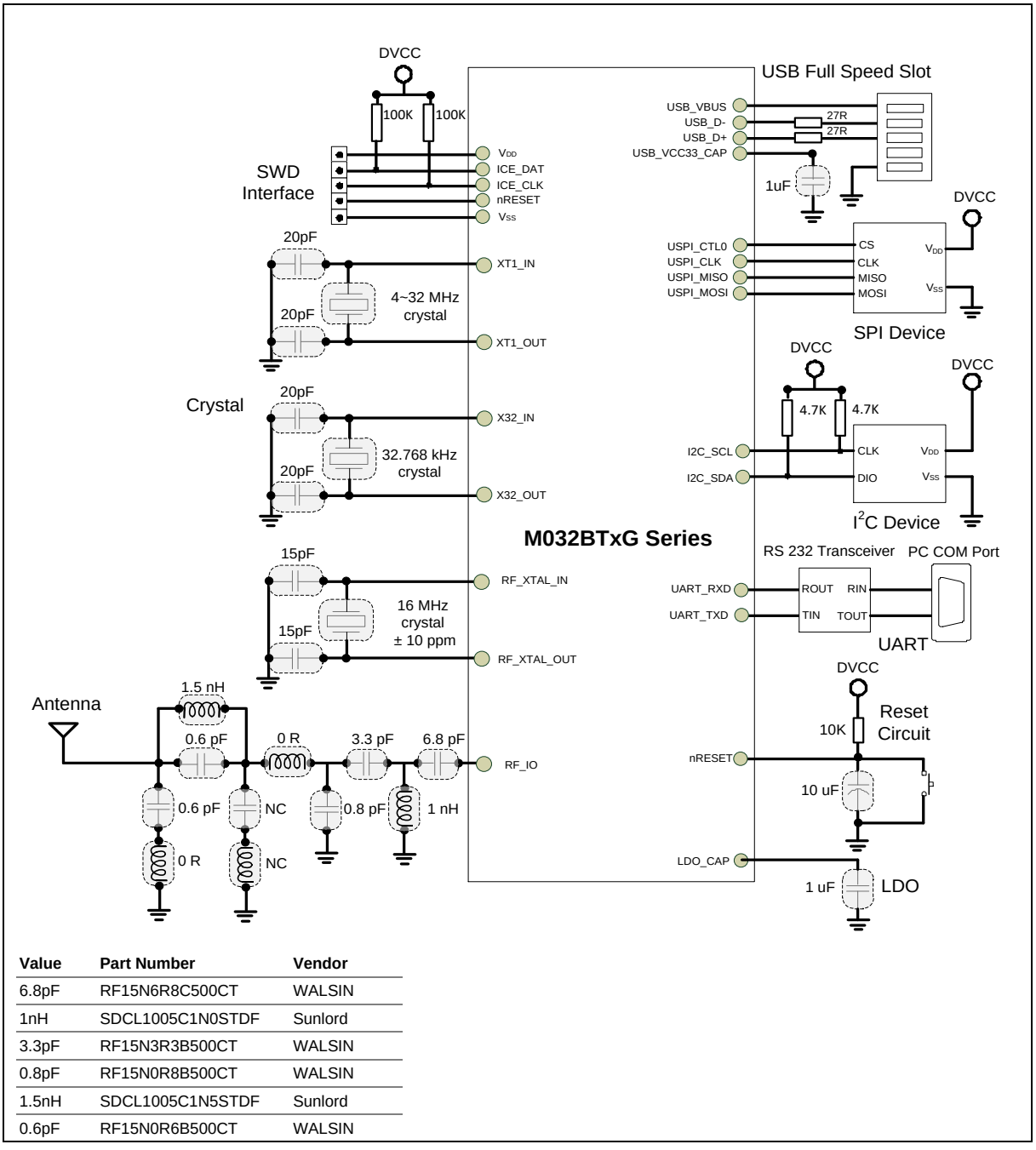
Value	Part Number	Vendor
6.8pF	RF15N6R8C500CT	WALSIN
2.7nH	SDCL1005C2N7STDF	Sunlord
2.7pF	RF15N2R7B500CT	WALSIN
0.9pF	RF15N0R9B500CT	WALSIN
0.8pF	RF15N0R8B500CT	WALSIN
0.2pF	RF15N0R2B500CT	WALSIN
1.5nH	SDCL1005C1N5STDF	Sunlord
1pF	RF15N1R0B500CT	WALSIN

Note 1: M031BT series doesn't support USCIx_CTL0 pin. User needs to use GPIO as SPI_SS pin.

Note 2: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 3: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

7.5 Peripheral Application Scheme (M032BTxG)

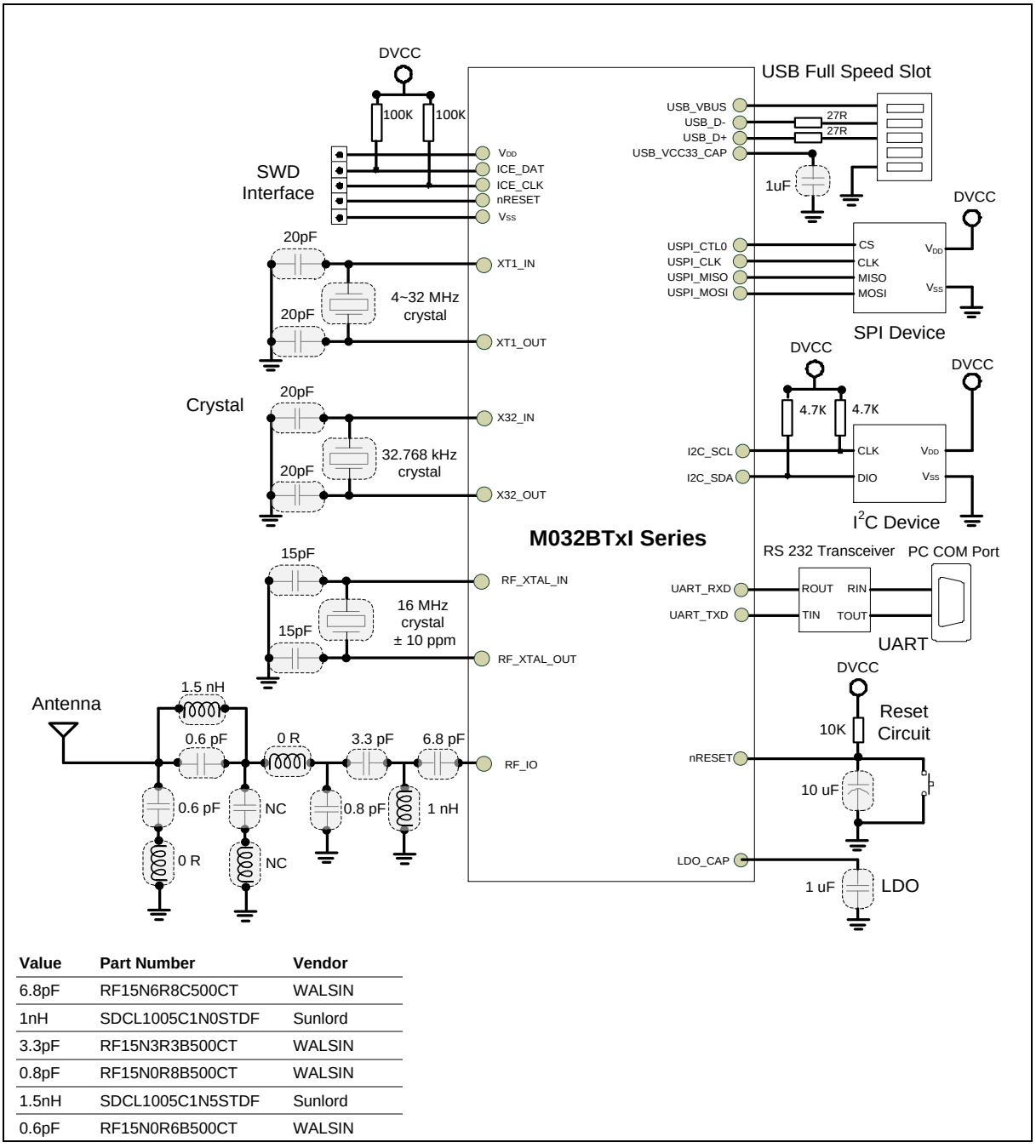


Value	Part Number	Vendor
6.8pF	RF15N6R8C500CT	WALSIN
1nH	SDCL1005C1N0STDF	Sunlord
3.3pF	RF15N3R3B500CT	WALSIN
0.8pF	RF15N0R8B500CT	WALSIN
1.5nH	SDCL1005C1N5STDF	Sunlord
0.6pF	RF15N0R6B500CT	WALSIN

Note 1: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 2: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

7.6 Peripheral Application Scheme (M032BTxI)



Value	Part Number	Vendor
6.8pF	RF15N6R8C500CT	WALSIN
1nH	SDCL1005C1N0STDF	Sunlord
3.3pF	RF15N3R3B500CT	WALSIN
0.8pF	RF15N0R8B500CT	WALSIN
1.5nH	SDCL1005C1N5STDF	Sunlord
0.6pF	RF15N0R6B500CT	WALSIN

Note 1: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 2: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

8 ELECTRICAL CHARACTERISTICS

Please refer to the relative Datasheet for detailed information about the M031BT electrical characteristics.

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	4.0	V
RF_V_{DD}-V_{SS}[*1]	Power supply for RF transceiver	-0.3	4.0	V
ΔV_{DD}	Variations between different power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on 5V-tolerance I/O	V_{SS}-0.3	5.5	V
	Input voltage on any other pin[*2]	V_{SS}-0.3	4.0	V

Note:

1. All main power (V_{DD}, RF_V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.
2. Non 5V-tolerance I/O includes PA.10 ~ 11; PB.0 ~ 15; PF.2, 3, 4, 5; all USB pin and nRESET pin. V_{IN} maximum value must be respected to avoid permanent damage. Refer to Table 8.1-2 for the values of the maximum allowed injected current

Table 8.1-1 Voltage Characteristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	150	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	100	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$ [*3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [*3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>A_{VDD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current Characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (°C)
- θ_{JA} = thermal resistance junction-ambient (°C/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	85	°C
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
	Thermal resistance junction-ambient 48-pin QFN(5x5 mm)	-	37.8	-	°C/Watt
	Thermal resistance junction-ambient 68-pin QFN(8x8 mm)	-	27.5	-	°C/Watt

Note:
1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal Characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-2000	-	+2000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-400	-	+400	
LU[*3]	Pin current for latch-up[*3]	-100	-	+100	mA

Note:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4.

Table 8.1-4 EMC Characteristics for M031BTxD/M031BTxE

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-2000	-	+2000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-250	-	+250	
LU[*3]	Pin current for latch-up[*3]	-100	-	+100	mA

Note:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4.

Table 8.1-5 EMC Characteristics for M032BTxG/M032BTxI

8.1.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
48-pin QFN(5x5 mm) [*1]	MSL 3
68-pin QFN(8x8 mm) [*1]	MSL 3

Note:

1. Determined according to IPC/JEDEC J-STD-020

Table 8.1-6 Package Moisture Sensitivity (MSL)

8.1.6 Soldering Profile

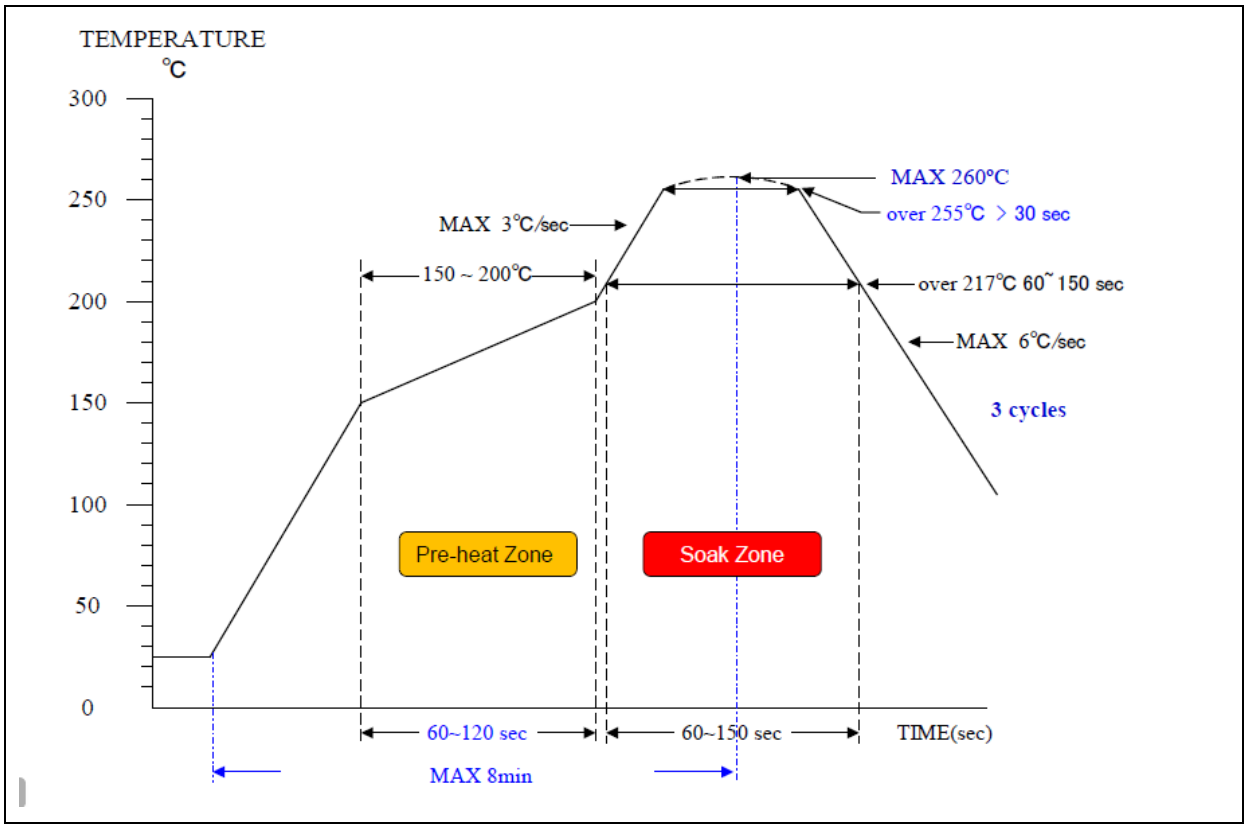


Figure 8.1-1 Soldering Profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217°C to peak)	3°C/sec. max
Preheat temperature 150°C ~200°C	60 sec. to 120 sec.
Temperature maintained above 217°C	60 sec. to 150 sec.
Time with 5°C of actual peak temperature	> 30 sec.
Peak temperature range	260°C
Ramp-down rate	6°C/sec ax.
Time 25°C to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 8.1-7 Soldering Profile

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 1.8 ~ 3.6V, T_A = 25°C, HCLK = 48/72 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	85	°C	
f_{HCLK}	Internal AHB clock frequency	-	-	48	MHz	V_{DD} = 1.8 V~3.6 V
		-	-	72	MHz	V_{DD} = 2.0 V~3.6 V
V_{DD}	Operation voltage	1.8	-	3.6	V	f_{HCLK} up to 48 MHz
		2.0	-	3.6		f_{HCLK} up to 72 MHz
RF_V_{DD}	RF transceiver operation voltage	2.3	-	3.6		DC-to-DC mode
		1.8	-	3.6		LDO mode
RF_V_{DDPA}	RF power amplifier operation voltage	RF_V_{DD}				
RF_AV_{DD1V2}	RF Transceiver 1.2 V voltage	-	1.2	-		
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{REF}	Analog reference voltage	1.8	-	AV_{DD}		$AV_{DD} - V_{REF} < 1.2$ V
V_{LDO}	LDO output voltage	-	1.8	-		
V_{BG}[*4]	Band-gap voltage	1.16	1.23	1.31		
C_{LDO}[*2]	LDO output capacitor on each pin	1				μF
R_{ESR}[*3]	ESR of C_{LDO} output capacitor	0.1	-	10	Ω	
I_{RUSH}[*3]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	150	-	mA	
E_{RUSH}[*3]	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	2.25	-	μC	V_{DD} = 1.8 V, T_A = 85 °C, I_{RUSH} = 150 mA for 15 us

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external 1 μF output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production
4. Based on characterization, not tested in production unless otherwise specified.

Table 8.2-1 General Operating Conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics for M031BTxD/M031BTxE

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 1. 8V ~ 3.6 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK0, 1} = f_{HCLK}$.
- Program run CoreMark® code in Flash.

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]		Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, all peripherals disable	48 MHz	8.8	10.1	10.5	mA
		32 MHz	6.2	7.1	7.6	
		24 MHz	5	5.8	6.0	
		12 MHz	3.6	4.1	4.4	
		4 MHz	2.4	2.8	3.0	
		38.4 kHz	0.105	0.121	0.275	
		32.768 kHz	0.104	0.120	0.273	
	Normal run mode, executed from Flash, all peripherals enable	48 MHz	20	23.0	23.7	
		32 MHz	12.9	14.8	15.5	
		24 MHz	11.2	12.9	13.3	
		12 MHz	6.7	7.7	8.0	
		4 MHz	3.9	4.5	4.7	
		38.4 kHz	0.111	0.128	0.283	
		32.768 kHz	0.110	0.127	0.281	
	Normal run mode, executed from Flash, Timer1/SPI0/PDMA enable	48 MHz	11.4	13.11	13.5	
		32 MHz	7.8	8.97	9.5	
		24 MHz	6.4	7.36	7.7	
		12 MHz	4.2	4.83	5.1	

Note:

1. When analog peripheral blocks such as ADC, ACMP, PLL, HIRC, LIRC, HXT, LXT and RF transceiver are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.
3. The RF transceiver operates in deep sleep mode.

Table 8.3-1 Current Consumption in Normal Run Mode for M031BTxD/M031BTxE

Symbol	Conditions	F_{HCLK}	Typ	Max[*1] [*2]		Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	
I_{DD_IDLE}	Idle mode, all peripherals disable	48 MHz	3.85	4.43	4.68	mA
		32 MHz	3.15	3.62	4.01	
		24 MHz	2.74	3.15	3.36	
		12 MHz	1.83	2.10	2.30	
		4 MHz	1.74	2.00	2.19	
		38.4 kHz	0.098	0.113	0.266	
		32.768 kHz	0.099	0.114	0.267	
	Idle mode, all peripherals enable	48 MHz	15.45	17.77	18.36	
		32 MHz	10.02	11.52	12.15	
		24 MHz	8.81	10.13	10.53	
		12 MHz	5.46	6.28	6.57	
		4 MHz	3.23	3.71	3.94	
		38.4 kHz	0.108	0.124	0.279	
		32.768 kHz	0.107	0.123	0.277	
	Idle mode, Timer1/SPI0/PDMA enable	48 MHz	6.45	7.42	7.73	
		32 MHz	5.83	6.70	7.14	
		24 MHz	5.15	5.92	6.17	
		12 MHz	4.5	5.18	5.39	

Note:

1. When analog peripheral blocks such as ADC, ACMP, PLL, HIRC, LIRC, HXT, LXT and RF transceiver are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.
3. The RF transceiver operates in deep sleep mode.

Table 8.3-2 Current Consumption in Idle Mode for M031BTxD/M031BTxE

Symbol	Test Conditions	LXT[*1] 32.768 kHz	LIRC 38.4 kHz	Typ[*2]	Max[*3][*4]		Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	
I_{DD_PD}	Power-down mode, all peripherals disable	-	-	13	25	355	µA
	Power-down mode, WDT/Timer/UART enable	V	-	15.5	28	365	
	Power-down mode, WDT/Timer/UART enable	-	V	14.5	27	370	
	Power-down mode, WDT use LIRC, UART/Timer use LXT	V	V	16.5	29	380	

Note:

1. Crystal used: AURUM XF66RU000032C0 with a CL of 20 pF for typical values
2. V_{DD} = AV_{DD} = 3.3V, LVR17 enabled, POR disabled and BOD disabled.
3. Based on characterization, not tested in production unless otherwise specified.
4. When analog peripheral blocks such as ADC, ACMP and RF transceiver are ON, an additional power consumption should be considered.
5. Based on characterization, tested in production.
6. The RF transceiver operates in deep sleep mode.

Table 8.3-3 Chip Current Consumption in Power-down Mode for M031BTxD/M031BTxE

8.3.2 Supply Current Characteristics for M032BTxG/M032BTxI

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 1. 8V ~ 3.6 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK0, 1} = f_{HCLK}$.
- Program run CoreMark® code in Flash.

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]		Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, all peripherals disable	72 MHz[*3]	23.7	27.2	28.7	mA
		48 MHz	14.3	16.5	18.2	
		32 MHz	9.0	10.4	12.0	
		24 MHz	7.4	8.5	9.9	
		12 MHz	4.7	5.4	6.8	
		4 MHz	2.4	2.8	4.1	
		38.4 kHz	0.141	0.162	1.430	
		32.768 kHz	0.140	0.161	1.429	
	Normal run mode, executed from Flash, all peripherals enable	72 MHz[*3]	48.5	55.7	55.7	
		48 MHz	29.9	34.4	36.6	
		32 MHz	19.7	22.7	24.7	
		24 MHz	16.1	18.5	20.2	
		12 MHz	9.3	10.7	12.2	
		4 MHz	4.8	5.5	6.9	
		38.4 kHz	0.207	0.238	1.511	
		32.768 kHz	0.204	0.235	1.507	
	Normal run mode, executed from Flash, SPI0/PDMA enable	72 MHz[*3]	26.1	30.0	31.5	
		48 MHz	16.1	18.5	20.2	
		32 MHz	9.8	11.3	12.9	
		24 MHz	8.5	9.8	11.3	

Note:

1. When analog peripheral blocks such as ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.
3. When chip works at V_{DD} = 2.0~3.6V.
4. The RF transceiver operates in deep sleep mode.

Table 8.3-4 Current Consumption in Normal Run Mode for M032BTxG/M032BTxI

Symbol	Conditions	F_{HCLK}	Typ	Max[*1] [*2]		Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	
I_{DD_IDLE}	Idle mode, all peripherals disable	72 MHz[*3]	9.9	11.4	12.6	mA
		48 MHz	3.9	4.5	5.9	
		32 MHz	2.6	3.0	4.3	
		24 MHz	2.7	3.1	4.5	
		12 MHz	2.1	2.4	3.7	
		4 MHz	1.7	2.0	3.3	
		38.4 kHz	0.133	0.153	1.421	
		32.768 kHz	0.133	0.153	1.422	
	Idle mode, all peripherals enable	72 MHz[*3]	32.6	37.5	39.7	
		48 MHz	19.1	21.9	23.8	
		32 MHz	12.5	14.3	16.1	
		24 MHz	10.5	12.1	13.6	
		12 MHz	6.2	7.1	8.5	
		4 MHz	3.3	3.8	5.1	
		38.4 kHz	0.145	0.167	1.438	
		32.768 kHz	0.143	0.164	1.434	
	Idle mode, SPI0/PDMA enable	72 MHz	11.9	13.7	15.0	
		48 MHz	5.3	6.0	7.4	
		32 MHz	3.5	4.0	5.4	
		24 MHz	3.4	3.9	5.3	

Note:

1. When analog peripheral blocks such as ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.
3. When chip works at V_{DD} = 2.0~3.6V.
4. The RF transceiver operates in deep sleep mode.

Table 8.3-5 Current Consumption in Idle Mode for M032BTxG/M032BTxI

Symbol	Test Conditions	LXT[*1] 32.768 kHz	LIRC 38.4 kHz	Typ[*2]	Max[*3][*4]		Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	
I_{DD_PD}	Power-down mode, all peripherals disable	-	-	51.5	61.2 [*5]	1298	µA
	Power-down mode, WDT/Timer/UART enable	V	-	53.1	63.3	1294	
	Power-down mode, WDT/Timer/UART enable	-	V	53.1	63.4	1300	
	Power-down mode, WDT use LIRC, UART/Timer use LXT	V	V	55.1	63.5	1306	

Note:

1. Crystal used: AURUM XF66RU000032C0 with a CL of 20 pF for typical values
2. V_{DD} = AV_{DD} = 3.3V, LVR17 enabled, POR disabled and BOD disabled.
3. Based on characterization, not tested in production unless otherwise specified.
4. When analog peripheral blocks such as ADC and ACMP are ON, an additional power consumption should be considered.
5. Based on characterization, tested in production.
6. The RF transceiver operates in deep sleep mode.

Table 8.3-6 Chip Current Consumption in Power-down Mode for M032BTxG/M032BTxI

8.3.3 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = 3.3 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, f_{HCLK} = 48 MHz, $f_{PCLK0, 1}$ = f_{HCLK}.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

Peripheral	I_{DD}[*1]	Unit
PDMA	0.721	mA
ISP	0.0002	
HDIV	0.135	
CRC	0.119	
SRAM0IDLE	0.122	
WDT/WWDT	0.125	
RTC	0.102	
TMR0	0.332	
TMR1	0.303	
TMR2	0.299	
TMR3	0.292	
CLKO	0.095	
ACMP01[*3]	0.243	
I2C0	0.159	
I2C1	0.122	
QSPI	0.914	
SPI	1.878	
UART0	0.629	
UART1	0.575	
UART2	0.631	
UART3	0.614	
UART4	0.584	
UART5	0.647	
UART6	0.549	
UART7	0.654	
USB FS Device	1.099	
ADC[*2]	0.962	
USCI0	0.638	
USCI1	0.445	

Peripheral	I_{DD}[*1]	Unit
PWM0	1.257	
PWM1	1.26	
BPWM0	0.649	
BPWM1	0.652	
Radio[*4]	0.0004	

Note:

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.
4. The RF transceiver operates in deep sleep mode.

Table 8.3-7 Peripheral Current Consumption

8.3.4 RF Supply Current Characteristics

Tast condition: DC-to-DC Mode, T_A= 25 °C, RF_V_{DD} = 3.3V, RF_V_{DDPA} = 3.3V, V_{DD} = 3.3 V and AV_{DD} = 3.3 V.

Symbol	Parameter	Min	Typ[*1] [*2]	Max	Unit	Test Conditions
$I_{RF_DeepSleep}$	Deep Sleep		0.4		µA	
I_{RF_Sleep}	Sleep		0.7		µA	
$I_{RF_Standby}$	Standby		1.3		mA	
I_{RF_RX}	Radio RX		6.5		mA	1 Mbps, 37- byte packets
			6.8		mA	2 Mbps, 37- byte packets
$I_{RF_TX+0dBm}$	Radio TX		11.2		mA	1 Mbps, 37- byte packets
			6.6		mA	2 Mbps, 37- byte packets
$I_{RF_TX+4dBm}$	Radio TX		12.4		mA	1 Mbps, 37- byte packets
			7.2		mA	2 Mbps, 37- byte packets
$I_{RF_TX+4dBm}$	Radio TX		13.4		mA	1 Mbps, 37- byte packets
			7.8		mA	2 Mbps, 37- byte packets
$I_{RF_TX+8dBm}$	Radio TX		14.7		mA	1 Mbps, 37- byte packets
			8.5		mA	2 Mbps, 37- byte packets

Note:

1. Guaranteed by characterization results, not tested in production.
2. The measured current value from RF_VDD only includes the average current of the RF transceiver in Direct Test Mode.

Table 8.3-8 RF DC Characteristics

8.3.5 RF Operating Mode Switching Times

The switching times given in Table 8.3-9 is measured on a switching phase with a with a 48 MHz HIRC.

From \ To	Deep Sleep	Sleep	Standby	Receive	Transmit
Deep Sleep	-	X	3 ms	X	X
Sleep	X	-	3 ms	X	X
Standby	1 ms	1 ms	-	100 µs	100 µs
Receive	X	X	0 µs	-	X
Transmit	X	X	0 µs	X	-

Note:

1. X: not allowed

Table 8.3-9 RF Operating Mode Switching Times

8.3.6 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.3-10 is measured on a wakeup phase with a 48 MHz HIRC oscillator.

Symbol	Parameter	Typ	Max	Unit
t_{WU_IDLE}	Wakeup from IDLE mode	5	6	cycles
t_{WU_NPD}[*1][*2]	Wakeup from normal power down mode	12	25	µs

Note:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first

Table 8.3-10 Low-power Mode Wakeup Timings

8.3.7 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} except 5V-tolenece I/O should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current , but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative injection	Positive injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	0	mA	Injected current on nReset pins
		-0	0		Injected current on PF2~PF5, and PB0~PB15 for analog input function
		-5	NA		Injected current on any other 5V-tolerance I/O

Table 8.3-11 I/O Current Injection Characteristics

8.3.8 I/O DC Characteristics

8.3.8.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage	0	-	$0.3*V_{DD}$	V	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	$0.2*V_{DD}$	-	V	
I_{LK}[*2]	Input leakage current	-1		1	µA	$V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode
		-1		1		$V_{DD} < V_{IN} < 5$ V, Open-drain or input only mode on any other 5v tolerance pins

R_{PU}[*1] [*3]	Pull up resistor	-	45	-	kΩ	V_{DD} = 3.3 V, Quasi mode
		-	120	-		V_{DD} = 1.8 V, Quasi mode

Note:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.
3. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up resistors must be disabled. Leakage could be higher than the maximum value, if positive current is injected on adjacent pins

Table 8.3-12 I/O Input Characteristics

8.3.8.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[*1] [*2]	Source current for quasi-bidirectional mode and high level	-25.5	-28	-31	μA	V_{DD} = 3.3 V V_{IN}=(V_{DD}-0.4) V
		-19	-22	-24	μA	V_{DD} = 2.5 V V_{IN}=(V_{DD}-0.4) V
		-10.5	-13	-16	μA	V_{DD} = 1.8 V V_{IN}=(V_{DD}-0.4) V
	Source current for push-pull mode and high level	-8	-10	-15	mA	V_{DD} = 3.3 V V_{IN}=(V_{DD}-0.4) V
		-6	-8	-13	mA	V_{DD} = 2.5 V V_{IN}=(V_{DD}-0.4) V
		-3.5	-5.5	-10.5	mA	V_{DD} = 1.8 V V_{IN}=(V_{DD}-0.4) V
I_{SK}[*1] [*2]	Sink current for push-pull mode and low level	7.5	9	14.5	mA	V_{DD} = 3.3 V V_{IN}= 0.4 V
		6	7.5	13	mA	V_{DD} = 2.5 V V_{IN}= 0.4 V
		3.5	5	10.5	mA	V_{DD} = 1.8 V V_{IN}= 0.4 V
C_{IO}[*1]	I/O pin capacitance	-	5	-	pF	

Note:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.3-13 I/O Output Characteristics

8.3.8.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}[*1]	Internal nRESET pull up resistor	-	45	-	KΩ	V_{DD} = 3.3 V
		-	120	-		V_{DD} = 1.8 V
t_{FR}[*1]	nRESET input filtered pulse time	-	32	-	μs	Normal run and Idle mode
		75	-	155		Power down mode

Note:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-14 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC)

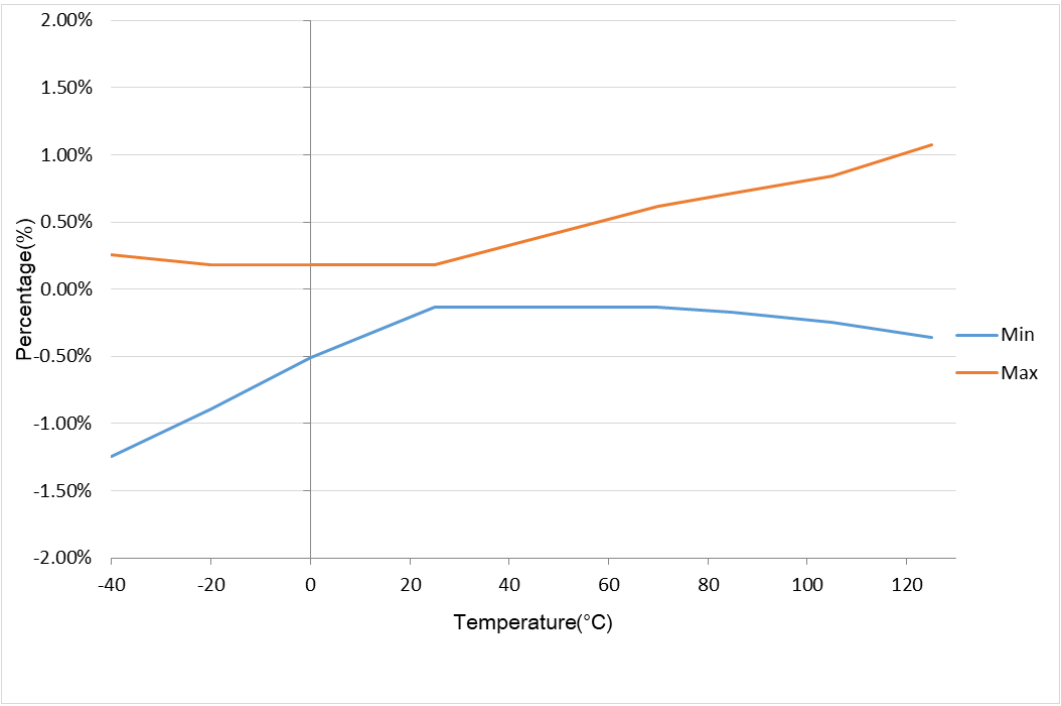
The 48 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	1.8	-	3.6	V	
f_{HRC}	Oscillator frequnecy	47.52	48	48.48	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[*1]	-	2[*1]	%	T_A = -40°C ~ +85 °C, V_{DD} = 1.8 ~ 3.6V
I_{HRC}[*1]	Operating current	-	1655	-	µA	
T_S[*2]	Stable time	-	11	15	µs	T_A = -40°C ~ +85 °C, V_{DD} = 1.8 ~ 3.6V

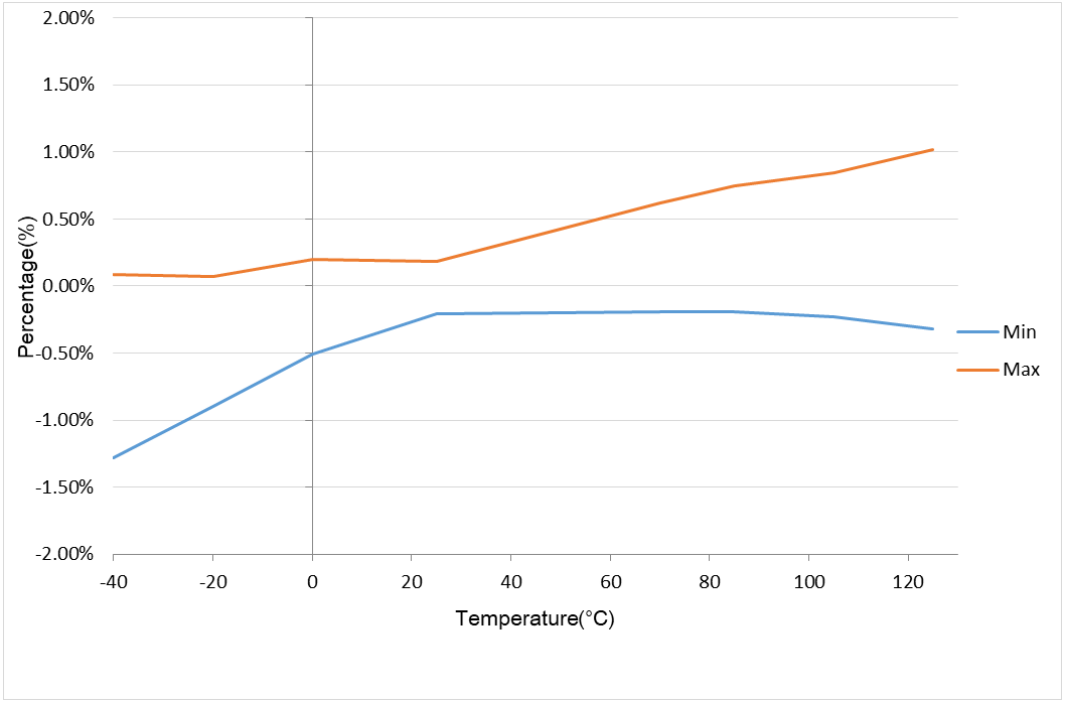
Note:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

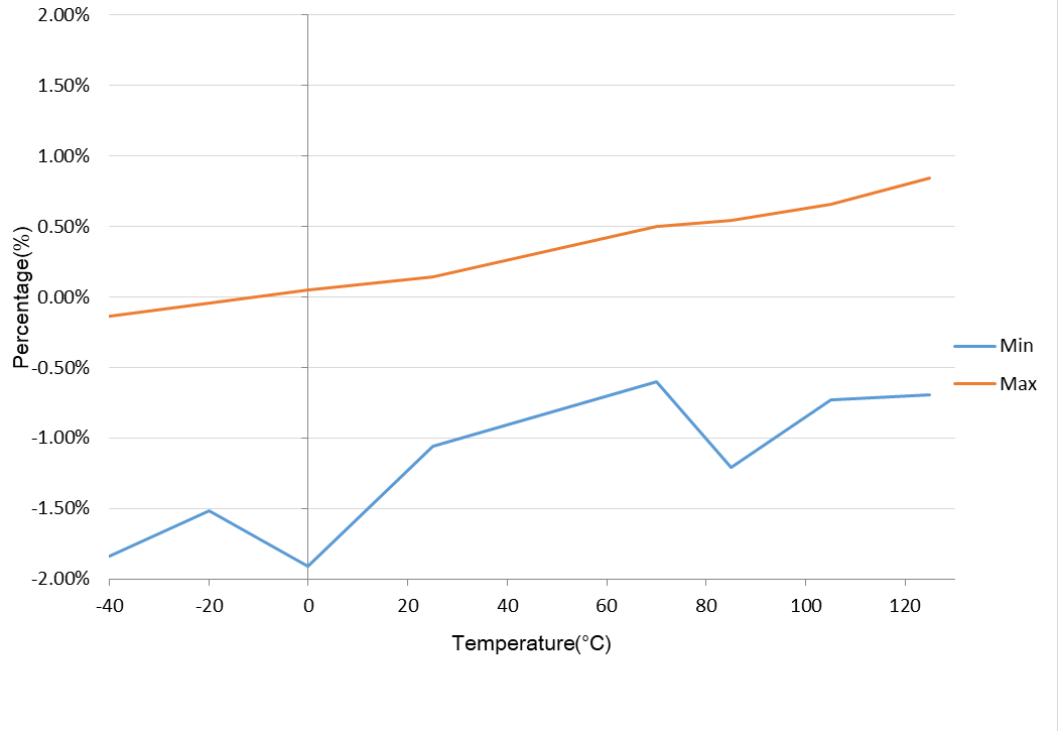
Table 8.4-1 48 MHz Internal High Speed RC Oscillator(HIRC) Characteristics



(a) Test condition: V_{DD}=3.6 V, Temp = -40~125℃



(b) Test condition: V_{DD}=2.7 V, Temp = -40~125℃



(c) Test condition: V_{DD}=1.8 V, Temp = -40~125℃

Note:

1. The graph is a statistical result using a limited number of samples. For the actual characteristic range, please refer to Table 8.4-1.

Figure 8.4-1 HIRC vs. Temperature

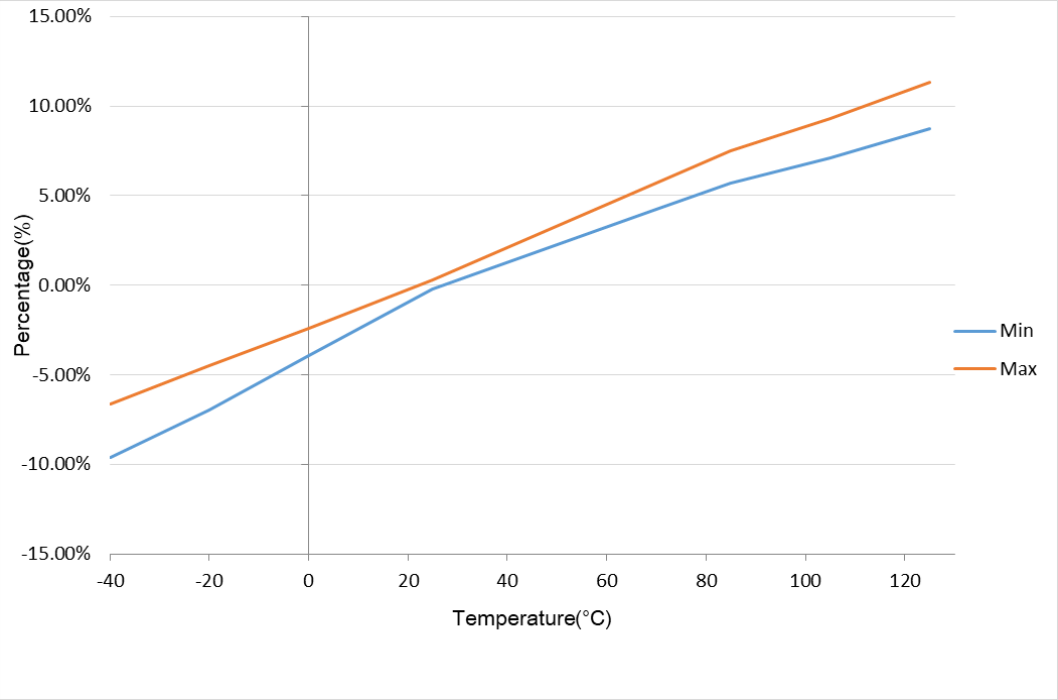
8.4.2 38.4 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.8	-	3.6	V	
F_{LRC} [*2]	Oscillator frequnecy	38.016	38.4	38.784	kHz	
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-15	-	15	%	T_A=-40~85 °C V_{DD}=1.8V~3.6V Without software calibration
I_{LRC}	Operating current	-	1	-	μA	V_{DD} = 3.3V
T_S	Stable time	-	500	-	μs	T_A=-40~85 °C V_{DD}=1.8V~3.6V

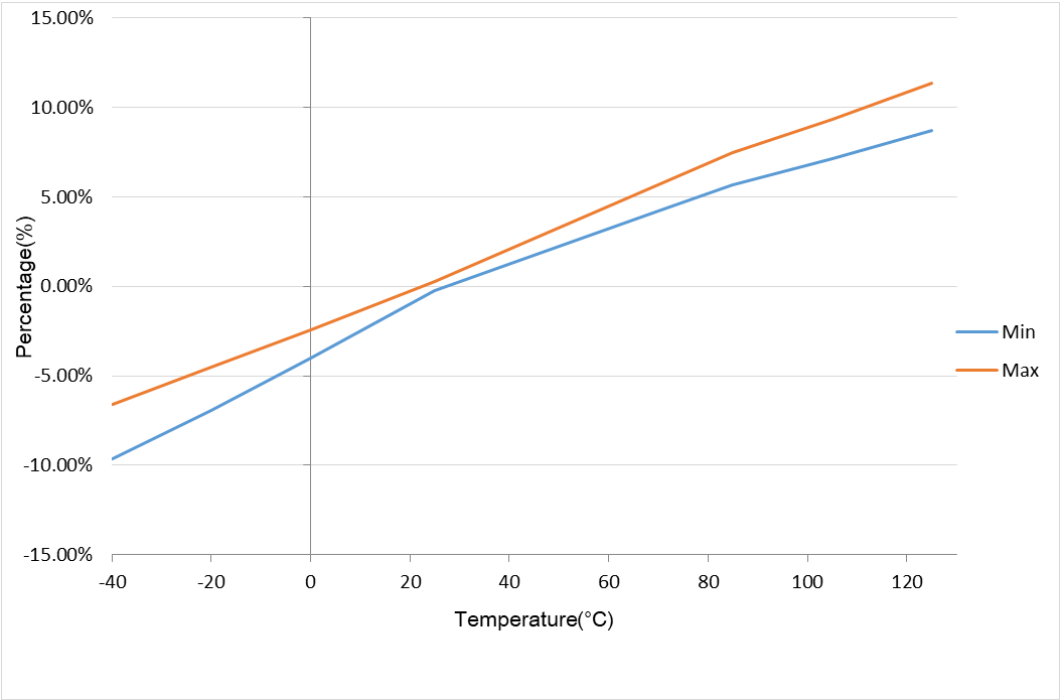
Note:

1. Guaranteed by characterization, not tested in production.
2. The 38.4 kHz low speed RC oscillator can be calibrated by user.
3. Guaranteed by design.

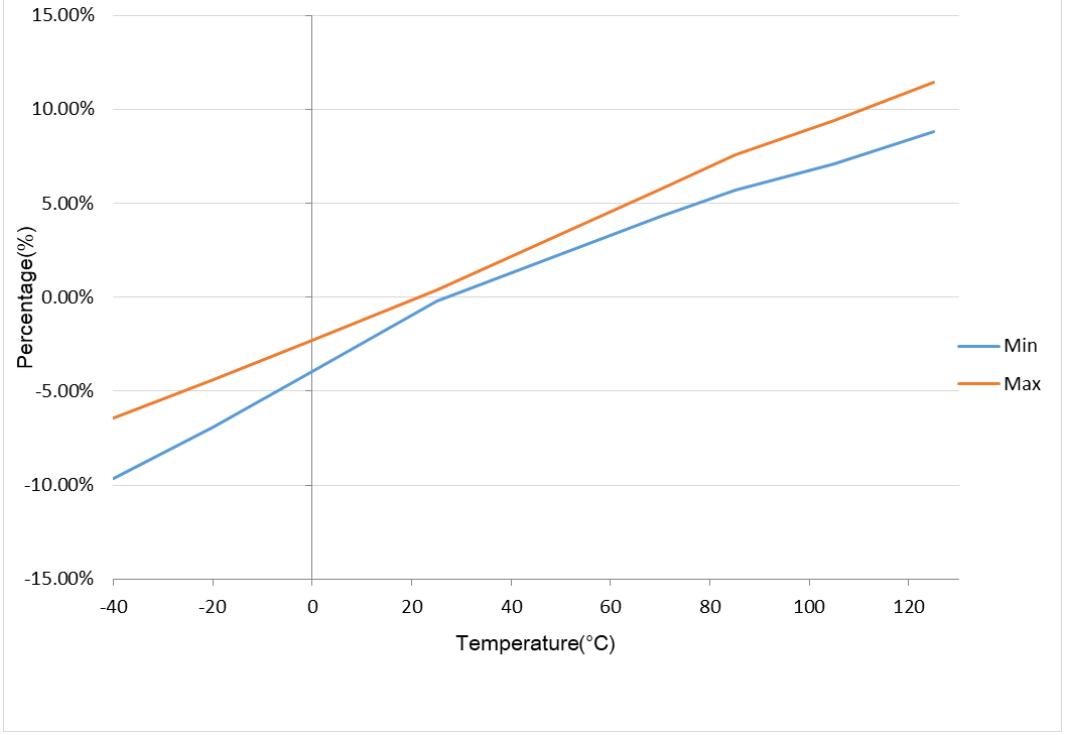
Table 8.4-2 38.4 kHz Internal Low Speed RC Oscillator(LIRC) characteristics



(a) Test condition: V_{DD}=3.6 V, Temp = -40~125℃



(b) Test condition: V_{DD}=2.7 V, Temp = -40~125℃



(c) Test condition: V_{DD}=1.8 V, Temp = -40~125℃

Note:

1. The graph is a statistical result using a limited number of samples. For the actual characteristic range, please refer to Table 8.4-2.

Figure 8.4-2 LIRC vs. Temperature

8.4.3 32 kHz Internal RF Low Speed RC Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
F_{RF_LRC}	Oscillator frequnecy		32		kHz	
F_{CAL}	Frequency Accuracy	-	500	-	ppm	T_A= 25°C
F_{TC}	Temperature Coefficient	-	200	-	ppm/°C	
T_S	Stable time	-	300	-	μs	

Note:

1. Guaranteed by characterization, not tested in production.

Table 8.4-3 32 kHz Internal RF Low Speed RC Oscillator Characteristics

8.4.4 External 16/32 MHz RF High Speed Crystal characteristics

The RF high-speed external clock can be supplied with a 16 or 32 MHz crystal oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the RF_XTAL_IN and RF_ XTAL_OUT pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
f_{RF_XT}	Oscillator frequency		16		MHz	
	Frequency Tolerance	-50	-	50	ppm	T_A= 25°C
Rs	Equivalent Series Resistance (ESR)		100		ohm	
	Drive Level			0.1	mW	
	Load Capacitance		9		pF	
	Frequency vs. Temperature	-20		20	ppm	T_A= -20 ~ +85°C
	Aging	-3		3	ppm/year	

Note:
1. Guaranteed by characterization, not tested in production.

Table 8.4-4 External 16 MHz RF High Speed Crystal Characteristics

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
f_{RF_XT}	Oscillator frequency		32		MHz	
	Frequency Tolerance	-50	-	50	ppm	T_A= 25°C
	Equivalent Series Resistance (ESR)		60		ohm	
	Drive Level			0.1	mW	
	Load Capacitance		10		pF	
	Frequency vs. Temperature	-20		20	ppm	T_A= -20 ~ +85°C
	Aging	-3		3	ppm/year	

Note:
1. Guaranteed by characterization, not tested in production.

Table 8.4-5 External 32 MHz RF High Speed Crystal Characteristics

8.4.4.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 25 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (3 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
16 MHz	10 ~ 25 pF	10 ~ 25 pF	without
32 MHz	10 ~ 25 pF	10 ~ 25 pF	without

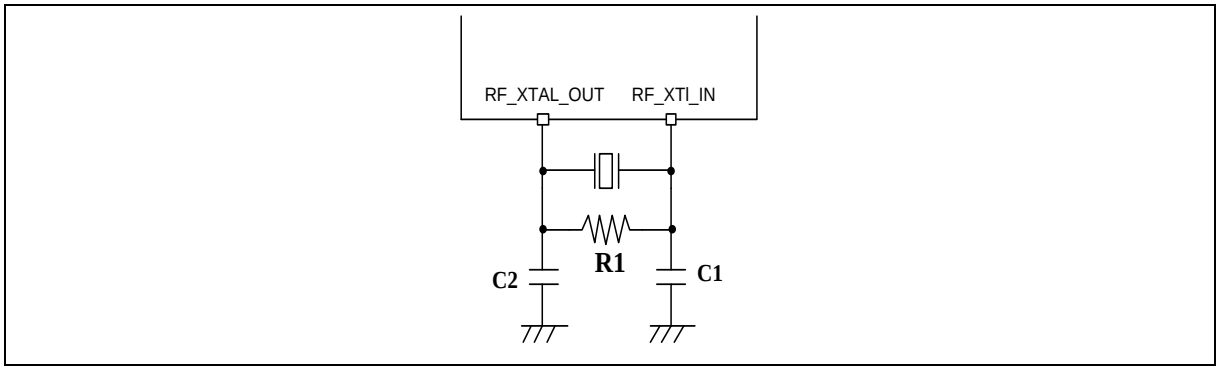


Figure 8.4-3 Typical Crystal Application Circuit

8.4.6 External 4~32 MHz High Speed Crystal/Ceramic Resonator (HXT) characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.8	-	3.6	V	
R_f	Internal feedback resister	-	200	-	kΩ	
f_{HXT}	Oscillator frequency	4	-	32	MHz	
I_{HXT}	Current consumption	-	120	200	μA	4 MHz, Gain = L0
			170	300		8 MHz, Gain = L1
		-	250	450		12 MHz, Gain = L2
		-	350	600		16 Mhz, Gain = L3
			500	850		24 MHz, Gain = L4
		-	650	1100		32 MHz, Gain = L7
T_S	Stable time	-	1700	2200	μs	4 MHz, Gain = L0
			900	1100		8 MHz, Gain = L1
		-	600	740		12 MHz, Gain = L2
		-	450	650		16 Mhz, Gain = L3
		-	400	600		24 MHz, Gain = L4
		-	350	550		32 MHz, Gain = L7
Du_{HXT}	Duty cycle	40	-	60	%	
Vpp	Peak-to-peak amplitude	-	1	-	V	

Note:

1. Guaranteed by characterization, not tested in production.

Table 8.4-6 External 4~32 MHz High Speed Crystal (HXT) Oscillator

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
Rs	Equivalent series resisotr(ESR)	-	-	150	Ω	Crystal @4 MHz
		-	-	50		Crystal @12 MHz
		-	-	40		Crystal @16 MHz
		-	-	40		Crystal @24 MHz
		-	-	40		Crystal @32 MHz

Note:

1. Guaranteed by characterization, not tested in production.
2. Safety factor (S_f) must be higher than 5 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain should be increased.

$$S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$$

R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) and is not suitable for mass production.

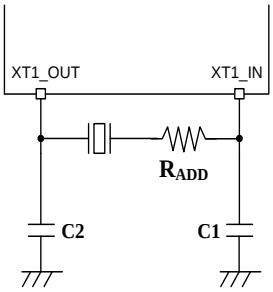


Table 8.4-7 External 4~32 MHz High Speed Crystal Characteristics

8.4.6.2 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 25 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
4 MHz ~ 32 MHz	10 ~ 25 pF	10 ~ 25 pF	without

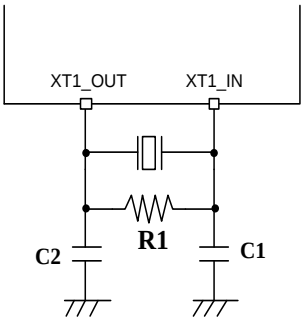
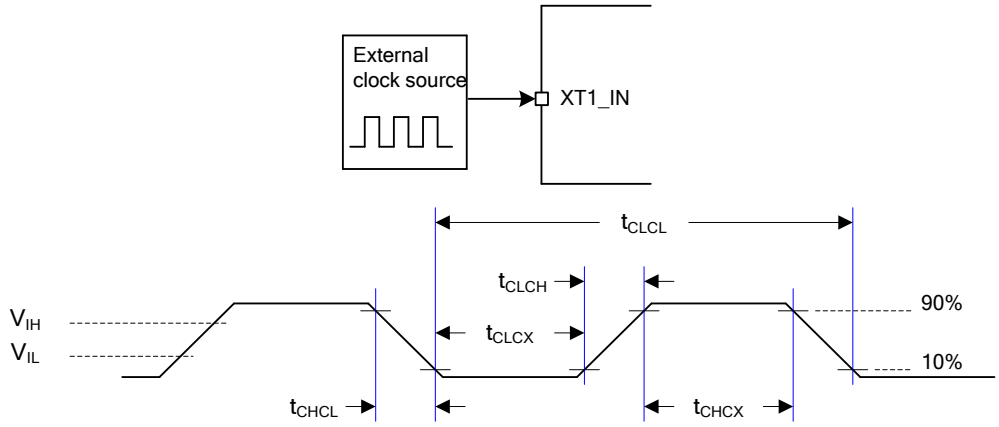


Figure 8.4-4 Typical Crystal Application Circuit

8.4.7 External 4~32 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	1	-	32	MHz	
t_{CHCX}	Clock high time	8	-	-	ns	
t_{CLCX}	Clock low time	8	-	-	ns	
t_{CLCH}	Clock rise time	-	-	10	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	ns	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Note:

1. Guaranteed by characterization, not tested in production.

Table 8.4-8 External 4~32 MHz High Speed Clock Input Signal

8.4.8 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operation voltage	1.8	-	3.6	V	
T_{LXT}	Temperature range	-40	-	85	°C	
R_f	Internal feedback resistor	-	6.5	-	MΩ	
F_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Current consumption	-	1.5	6	μA	ESR=35 kΩ, Gain = L1
		-	2	6		ESR=70 kΩ, Gain = L2
Ts_{LXT}	Stable time	-	500	900	ms	
Du_{LXT}	Duty cycle	30	-	70	%	
V_{pp}	Peak-to-peak amplitude	TBD	500	-	mV	

Note:
1. Guaranteed by characterization, not tested in production.

Table 8.4-9 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalnet Series Resisotr(ESR)	-	35	70	kΩ	Crystal @32.768 kHz

Table 8.4-10 External 32.768 kHz Low Speed Crystal Characteristics

8.4.8.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 70 KΩ	20 pF	20 pF	without

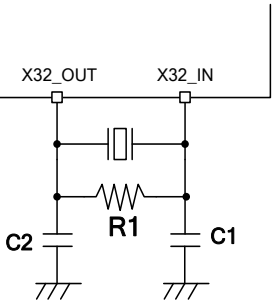
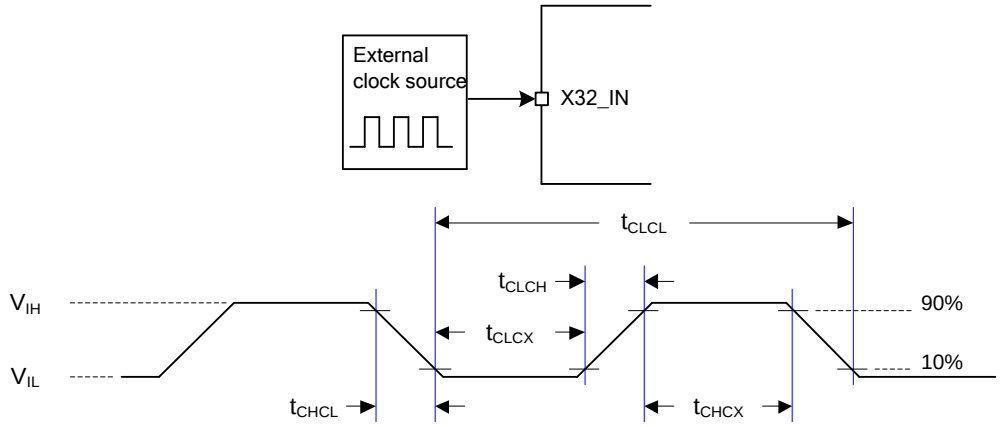


Figure 8.4-5 Typical 32.768 kHz Crystal Application Circuit

8.4.9 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{LXT}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	ns	
t_{CLCX}	Clock low time	450	-	-	ns	
t_{CLCH}	Clock rise time	-	-	50	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	ns	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	40	-	60	%	
Xin_VIH	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
Xin_VIL	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Note:

1. Guaranteed by design, not tested in production

Table 8.4-11 External 32.768 kHz Low Speed Clock Input Signal

8.4.10 PLL Characteristics

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
f_{PLL_in}	PLL input clock	3.2	-	32	MHz	
f_{PLL_OUT}	PLL multiplier output clock	50	-	96	MHz	
f_{PLL_REF}	PLL reference clock	0.8	-	8	MHz	
f_{PLL_VCO}	PLL voltage controlled oscillator	200	-	500	MHz	
T_L	PLL locking time	-	-	500	µs	
Jitter[*2]	Cycle-to-cycle Jitter	-	200	350	ps	
I_{DD}	Power consumption	-	3.1	5	mA	V_{DD} =3.3V @ f_{PLL_OUT} = 96 MHz

Note:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production

Table 8.4-12 PLL Characteristics

8.4.11 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Output high (90%) to low level (10%) fall time	-	5.5	ns	C_L = 30 pF, V_{DD} >= 2.7 V
		-	3		C_L = 10 pF, V_{DD} >= 2.7 V
		-	8.5		C_L = 30 pF, V_{DD} >= 1.8 V
		-	4.5		C_L = 10 pF, V_{DD} >= 1.8 V
$t_{r(IO)out}$	Output low (10%) to high level (90%) rise time	-	5.5	ns	C_L = 30 pF, V_{DD} >= 2.7 V
		-	3		C_L = 10 pF, V_{DD} >= 2.7 V
		-	8.5		C_L = 30 pF, V_{DD} >= 1.8 V
		-	4.5		C_L = 10 pF, V_{DD} >= 1.8 V
$f_{max(IO)out}$[*3]	I/O maximum frequency	-	60	MHz	C_L = 30 pF, V_{DD} >= 2.7 V
		-	110		C_L = 10 pF, V_{DD} >= 2.7 V
		-	40		C_L = 30 pF, V_{DD} >= 1.8 V
		-	75		C_L = 10 pF, V_{DD} >= 1.8 V
I_{DIO}[*4]	I/O dynamic current consumption	2.77	-	mA	C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		1.19	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		0.69	-		C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz
		0.3	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz

Note:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 8.4-13 I/O AC Characteristics

8.5 Analog Characteristics

8.5.1 LDO

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Power supply	1.8	-	3.6	V	
V_{LDO}	Output voltage	-	1.8	-	V	
T_A	Temperature	-40	-	85	°C	

Note

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1μF capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

8.5.2 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	-	20	30	μA	AV_{DD} = 3.6V
I_{LVR}[*1]	LVR operating current	-	2	3.6		AV_{DD} = 3.6V
I_{BOD}[*1]	BOD operating current	-	3	5.5		AV_{DD} = 3.6V
V_{POR}	POR reset voltage	1.35	1.5	1.65	V	-
V_{LVR}	LVR reset voltage	1.6	1.7	1.8		
V_{BOD}	BOD brown-out detect voltage	1.8	2.0	2.2		BODVL = 0
		2.3	2.5	2.7		BODVL = 1
T_{LVR_SU}[*1]	LVR startup time	-	200	-	μs	-
T_{LVR_RE}[*1]	LVR respond time	-	16	-		-
T_{BOD_SU}[*1]	BOD startup time	-	1000	-		-
T_{BOD_RE}[*1]	BOD respond time	-	120	-		-
R_{VDDR}[*1]	V_{DD} rise time rate	10	-	-	μs/V	POR Enabled
R_{VDDF}[*1]	V_{DD} fall time rate	10	-	-		POR Enabled
		80	-	-		LVR Enabled
		250	-	-		BOD 2.0V Enabled
		150	-	-		BOD 2.5V Enabled

Note:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.5-1 Reset and Power Control Unit

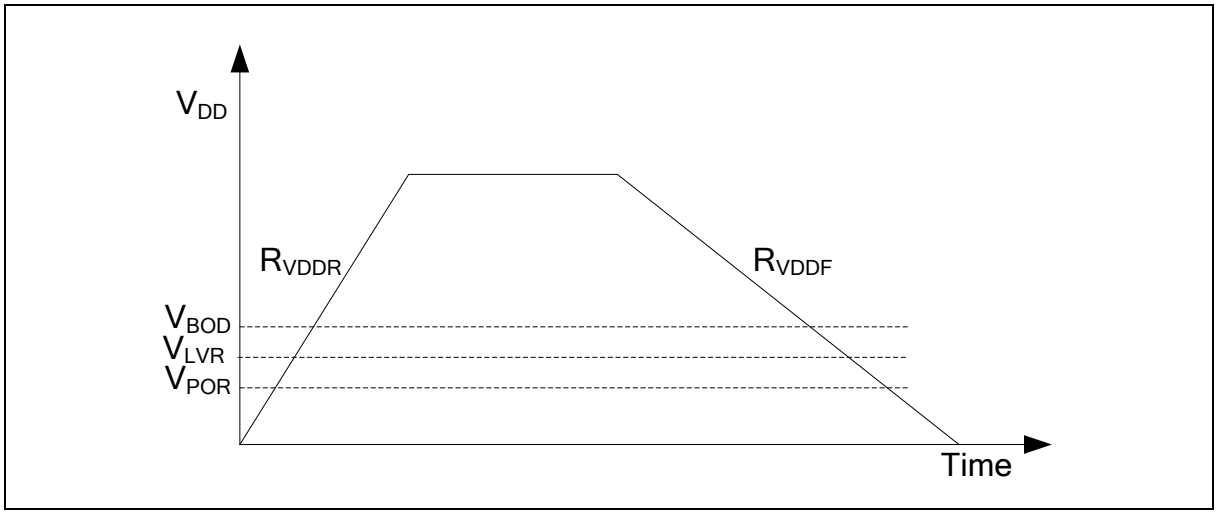


Figure 8.5-1 Power Ramp Up/Down Condition

8.5.3 12-bit SAR ADC

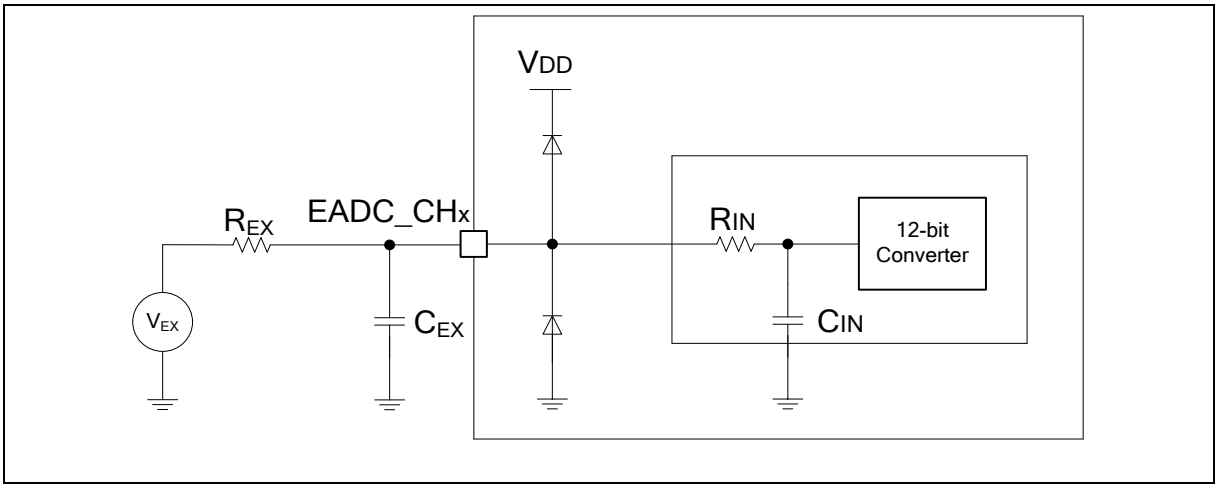
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	85	°C	
AV_{DD}	Analog operating voltage	1.8	-	3.6	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	1.8	-	AV_{DD}	V	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
V_{CM}	Common-Mode Input Range	$V_{REF}/2$			V	Full differential input
I_{ADC}[*1]	Operating current (AV_{DD} + V_{REF} current)	-	-	355	µA	$AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V F_{ADC} = 34 MHz $T_{CONV} = 17 * T_{ADC}$
N_R	Resolution	12			Bit	
F_{ADC}[*1] $1/T_{ADC}$	ADC Clock frequency	4	-	34	MHz	
T_{SMP}	Sampling Time	1	-	256	$1/F_{ADC}$	T_{SMP} = (EXTSMPT(ADC_ESMPCTL[7:0]) + 1) * T_{ADC}
T_{CONV}	Conversion time	17	-	272	$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 16 * T_{ADC}$
F_{SPS}[*1]	Sampling Rate	0.236	-	2	MSPS	$F_{SPS} = F_{ADC} / T_{CONV}$ EXTSMPT(ADC_ESMPCTL[7:0]) = 0
T_{EN}	Enable to ready time	20	-	-	µs	
INL[*1]	Integral Non-Linearity Error	-2	-	+2	LSB	$V_{REF} = AV_{DD}$,
DNL[*1]	Differential Non-Linearity Error	-1	-	+2	LSB	$V_{REF} = AV_{DD}$,
E_G[*1]	Gain error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$,
E_O[*1]$_T$	Offset error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$,
E_A[*1]	Absolute Error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$,
ENOB[*1]	Effective number of bits	-	-	TBD	bits	F_{ADC} = 34 MHz $AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V Input Frequency = 20 kHz T_A = 25 °C
SINAD[*1]	Signal-to-noise and distortion ratio	-	-	TBD	dB	
SNR[*1]	Signal-to-noise ratio	-	-	TBD		
THD[*1]	Total harmonic distortion	-	-	TBD		
C_{IN}[*1]	Internal Capacitance	-	2.9	-	pF	
R_{IN}[*1]	Internal Switch Resistance	-	-	2	kΩ	
R_{EX}[*1]	External input impedance	-	-	50	kΩ	

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions

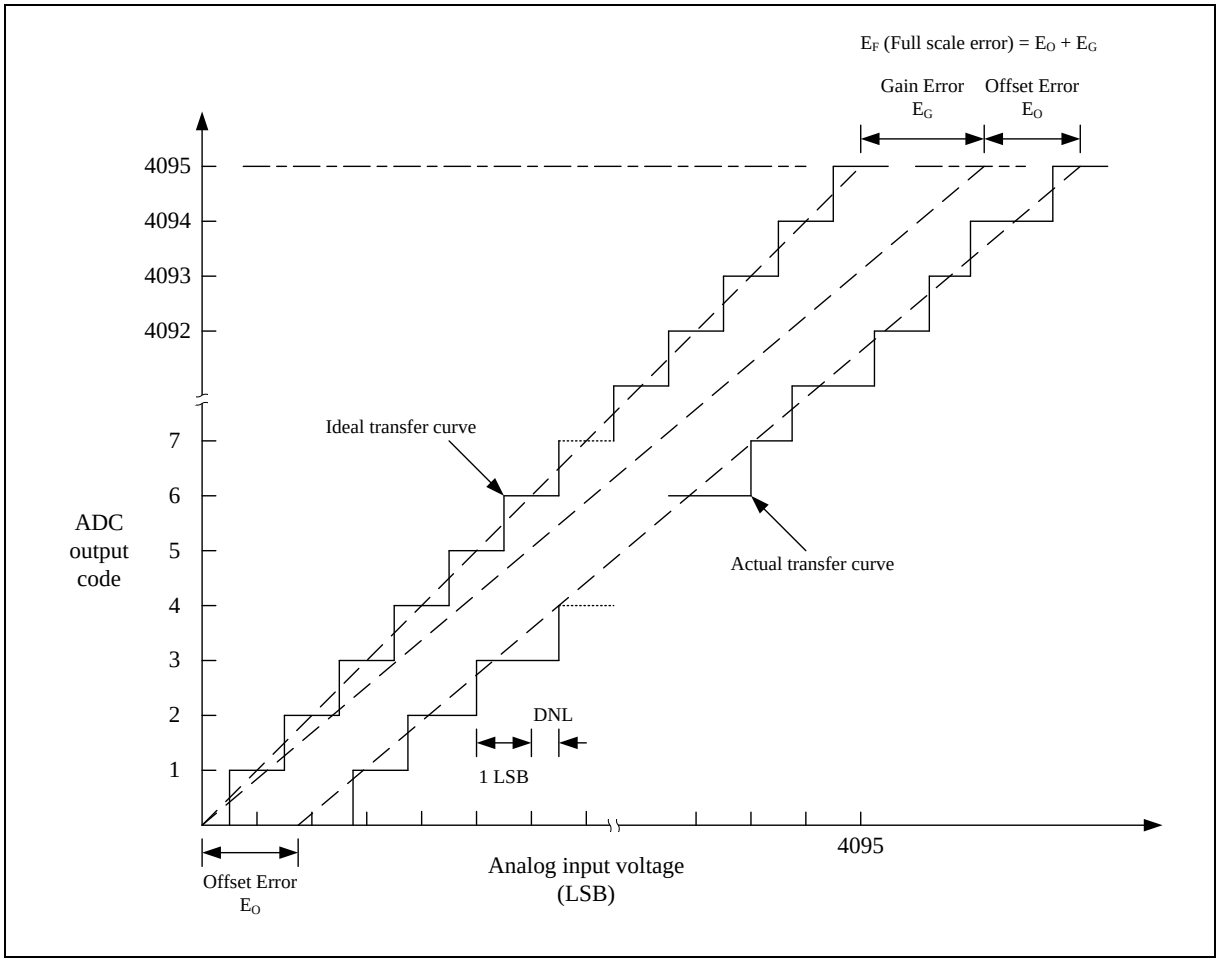
Note:

1. Guaranteed by characterization result, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} = \frac{k}{f_{ADC} \times C_{IN} \times \ln(2^{N+2})} - R_{IN}$$



Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.4 Analog Comparator Controller (ACMP)

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
AV_{DD}	Analog supply voltage	1.8	-	3.6	V	V_{DD} = AV_{DD}
T_A	Temperature	-40	-	85	˚C	
I_{DD}	Operating current	-	30	45	μA	
V_{CM}[*2]	Input common mode voltage range	0.35	1/2 AV_{DD}	AV_{DD} -0.3		
V_{DI}[*2]	Differential input voltage sensitivity	10	20	-	mV	Hysteresis disable
V_{offset}[*2]	Input offset voltage	-	10	20	mV	Hysteresis disable,
V_{hys}[*2]	Hysteresis window	40	90	140	mV	
A_v[*1]	DC voltage Gain	45	65	75	dB	
T_d[*2]	Propagation delay	-	-	400	nS	
T_{Setup}[*2]	Setup time	-	-	4	uS	
A_{CRV}[*2]	CRV output voltage	-5	-	5	%	AV_{DD} x (1/6+CRVCTL/24)
R_{CRV}[*2]	Unit resistor value	-	4.2	-	kΩ	
T_{SETUP_CRV}[*2]	Setup time	-	-	350	μS	CRV output voltage settle to ±5%
I_{DD_CRV}[*2]	Operating current	-	30	45	μA	

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

Table 8.5-2 ACMP Characteristics

8.5.5 RF Characteristics

8.5.5.1 Transmitter Characteristics

Tast condition: T_A= 25 °C, RF_V_{DD} = 3.3V, RF_V_{DDPA} = 3.3V, V_{DD} = 3.3 V and AV_{DD} = 3.3 V.

Symbol	Parameter	Values			Unit	Condition
		Min	Typ	Max		
P_{OUT}	RF Output Power	-20	-	8	dBm	M031BTxD/M031BTxE
		-20	-	6	dBm	M032BTxG/M032BTxI
$F_{OPERATING}$	Operating Frequency	2.4		2.5	GHz	
ΔF	Frequency Drift		< ± 50		kHz	1 Mbps data rate
			< ± 50		kHz	2 Mbps data rate
$F_{\Delta F}$	Frequency Drift Rate		< ± 20		kHz /50μs	1 Mbps & 2 Mbps data rates
Δf1	Average Frequency Deviation (data pattern = 111000…)	225	260	275	kHz	1 Mbps data rate
		450	500	550	kHz	2 Mbps data rate
Δf2	Instantaneous Deviation (data pattern = 10101010…)	185			kHz	1 Mbps data rate
		370			kHz	2 Mbps data rate
Δf2 / Δf1	Deviation Ratio	80			%	1 Mbps data rate
		80			%	2 Mbps data rate
	Spectrum Mask with Adjacent Channel Offset: ± 2 MHz		-20		dBc	1 Mbps data rate
	Spectrum Mask with Adjacent Channel Offset: ≥ 3 MHz		-30		dBc	1 Mbps data rate
	Spectrum Mask with Adjacent Channel Offset: ± 4 MHz		-20		dBc	2 Mbps data rate
	Spectrum Mask with Adjacent Channel Offset: ± 5 MHz		-20		dBc	2 Mbps data rate
	Spectrum Mask with Adjacent Channel Offset: ± 6 MHz		-30		dBc	2 Mbps data rate

Table 8.5-3 RF Transmitter Characteristics

8.5.5.2 Receiver Characteristics

Tast condition: T_A= 25 °C, RF_V_{DD} = 3.3V, RF_V_{DDPA} = 3.3V, V_{DD} = 3.3 V and AV_{DD} = 3.3 V.

Symbol	Parameter	Values			Unit	Condition
		Min	Typ	Max		
	RF Sensitivity, NF = 6 dB, +1.2VDC core supply		-94		dBm	1 Mbps data rate, M031BTxD/M031BTxE
			-91		dBm	2 Mbps data rate, M031BTxD/M031BTxE
			-93		dBm	1 Mbps data rate, M032BTxG/M032BTxI
			-90		dBm	2 Mbps data rate, M032BTxG/M032BTxI
C/I $_{CO-CHANNEL}$	Carrier-to-Interference:		8		dB	1 Mbps data rate
	Co-Channel Selectivity		9		dB	2 Mbps data rate
C/I $_{-1\ MHz}$	Carrier-to-Interference:		-5		dB	1 Mbps data rate
	- 1 MHz Adjacent Channel Selectivity					
C/I $_{+1\ MHz}$	Carrier-to-Interference:		-9		dB	1 Mbps data rate
	+ 1 MHz Adjacent Channel Selectivity					
C/I $_{-2\ MHz}$	Carrier-to-Interference:		-36		dB	1 Mbps data rate
	- 2 MHz Adjacent Channel Selectivity		-3		dB	2 Mbps data rate
C/I $_{+2\ MHz}$	Carrier-to-Interference:		-26		dB	1 Mbps data rate
	+ 2 MHz Adjacent Channel Selectivity		-8		dB	2 Mbps data rate
C/I $_{-3\ MHz}$	Carrier-to-Interference:		-40		dB	1 Mbps data rate
	- 3 MHz Adjacent Channel Selectivity					
C/I $_{+3\ MHz}$	Carrier-to-Interference:		-38		dB	1 Mbps data rate
	+ 3 MHz Adjacent Channel Selectivity					
C/I $_{-4\ MHz}$	Carrier-to-Interference:		-34		dB	2 Mbps data rate
	- 4 MHz Adjacent Channel Selectivity					
C/I $_{+4MHz}$	Carrier-to-Interference:		-25		dB	2 Mbps data rate
	+ 4 MHz Adjacent Channel Selectivity					
C/I $_{-6\ MHz}$	Carrier-to-Interference:		-42		dB	2 Mbps data rate
	- 6 MHz Adjacent Channel Selectivity					
C/I $_{+6\ MHz}$	Carrier-to-Interference:		-37		dB	2 Mbps data rate
	+ 6 MHz Adjacent Channel Selectivity					
C/I $_{IMAGE}$	Carrier-to-Interference:		-26		dB	1 Mbps data rate
	Image Channel Selectivity		-25		dB	2 Mbps data rate
C/I $_{IMAGE1\ MHz}$	Carrier-to-Interference:		-38		dB	1 Mbps data rate
	Image 1 MHz Adjacent Channel Selectivity		-37		dB	2 Mbps data rate
IM	Intermodulation Interferer Level		-31		dBm	1 Mbps data rate

Symbol	Parameter	Values			Unit	Condition
		Min	Typ	Max		
			-31		dBm	2 Mbps data rate
OOB	Out-of-band Blocking: Interferer		-15		dBm	1 Mbps data rate
30 MHz, 2000 MHz	30 MHz ≤ f ≤ 2000 MHz		-15		dBm	2 Mbps data rate
OOB	Out-of-band Blocking: Interferer		-20		dBm	1 Mbps data rate
2000 MHz, 2399 MHz	2003 MHz ≤ f ≤ 2399 MHz		-20		dBm	2 Mbps data rate
OOB	Out-of-band Blocking: Interferer		-20		dBm	1 Mbps data rate
2484 MHz, 2997 MHz	2484 MHz ≤ f ≤ 2997 MHz		-20		dBm	2 Mbps data rate
OOB	Out-of-band Blocking: Interferer		-20		dBm	1 Mbps data rate
2997 MHz, 6 GHz	2997 MHz ≤ f ≤ 6 GHz		-20		dBm	2 Mbps data rate
OOB	Out-of-band Blocking: Interferer		-10		dBm	1 Mbps data rate
6 GHz, 12.75 GHz	6 GHz ≤ f ≤ 12.75 GHz		-10		dBm	2 Mbps data rate

Table 8.5-4 RF Receiver Characteristics

8.6 Communications Characteristics

8.6.1 QSPI/SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	16	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 25 pF
		-	-	16		1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 25 pF
F_{SPICLK} $1/ T_{SPICLK}$	QSPI clock frequency	-	-	24	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 25 pF
		-	-	24		1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 25 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{DS}	Data input setup time	2	-	-	ns	
t_{DH}	Data input hold time	4	-	-	ns	
t_V	Data output valid time	-	-	5	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 25 pF
		-	-	8.5	ns	1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 25 pF

Note:

1. Guaranteed by design.

Table 8.6-1 QSPI/SPI Master Mode Characteristics

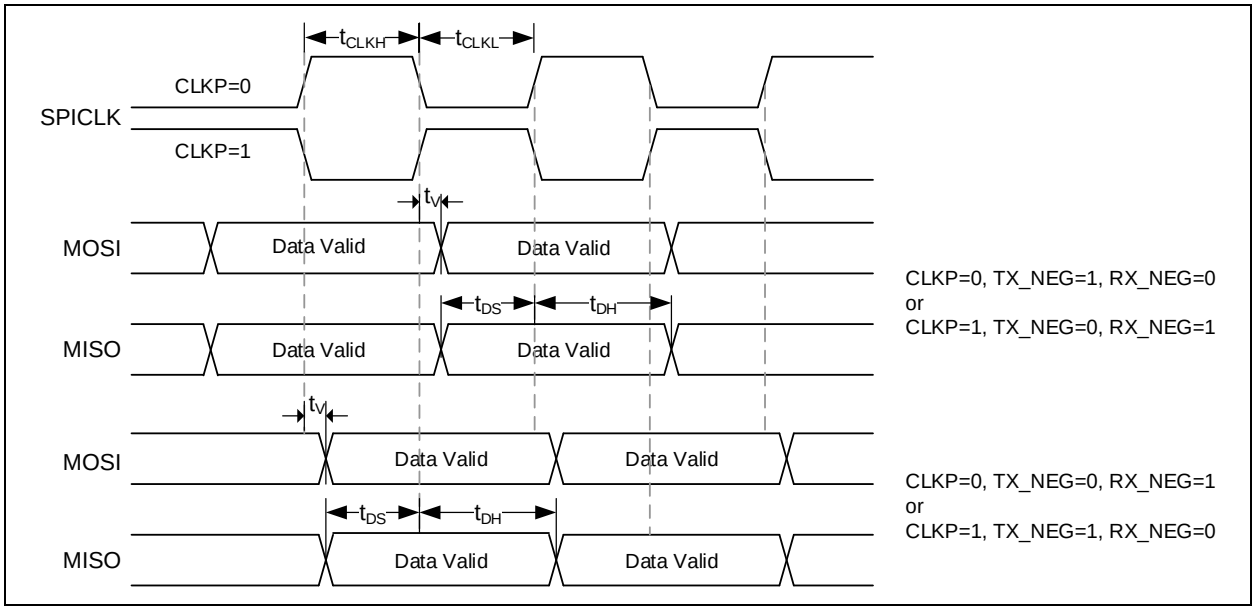


Figure 8.6-1 QSPI/SPI Master Mode Timing Diagram

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	QSPI clock frequency	-	-	16	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
		-	-	16		1.8 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
		1 T_{SPICLK} + 3ns	-	-		1.8 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns	
t_{DS}	Data input setup time	1.5	-	-	ns	
t_{DH}	Data input hold time	3.5	-	-	ns	
t_V	Data output valid time	-	-	17.5	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
		-	-	25		1.8 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-2 QSPI Slave Mode Characteristics

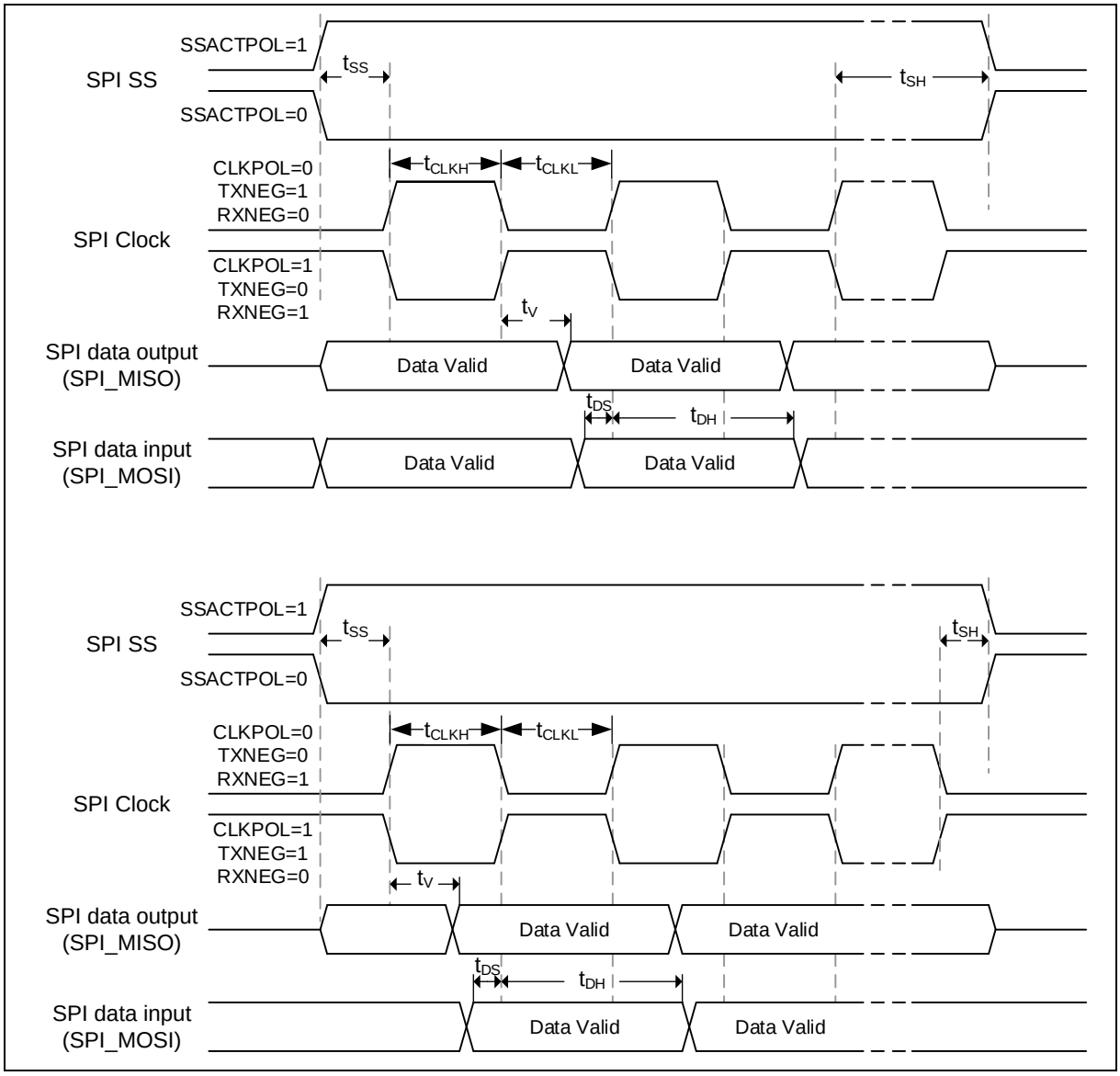


Figure 8.6-2 QSPI Slave Mode Timing Diagram

8.6.2 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μs
t_{HIGH}	SCL high period	4	-	0.6	-	μs
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μs
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μs
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μs
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μs
$t_{SU;DAT}$	Data setup time	250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μs
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	ns
t_f	SCL/SDA fall time	-	300	-	300	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-3 I²C Characteristics

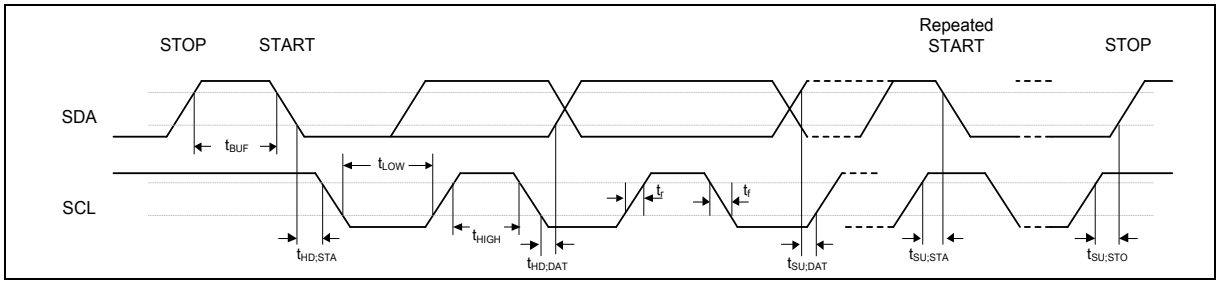


Figure 8.6-3 I²C Timing Diagram

8.6.3 USCI - SPI Dynamic Characteristics

Symbol	Parameter	Min [*1]	Typ	Max[*1]	Unit	Test Conditions
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	24	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	24		1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{DS}	Data input setup time	2	-	-	ns	
t_{DH}	Data input hold time	4	-	-	ns	
t_V	Data output valid time	-	-	5	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	8.5	ns	1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-4 USCI-SPI Master Mode Characteristics

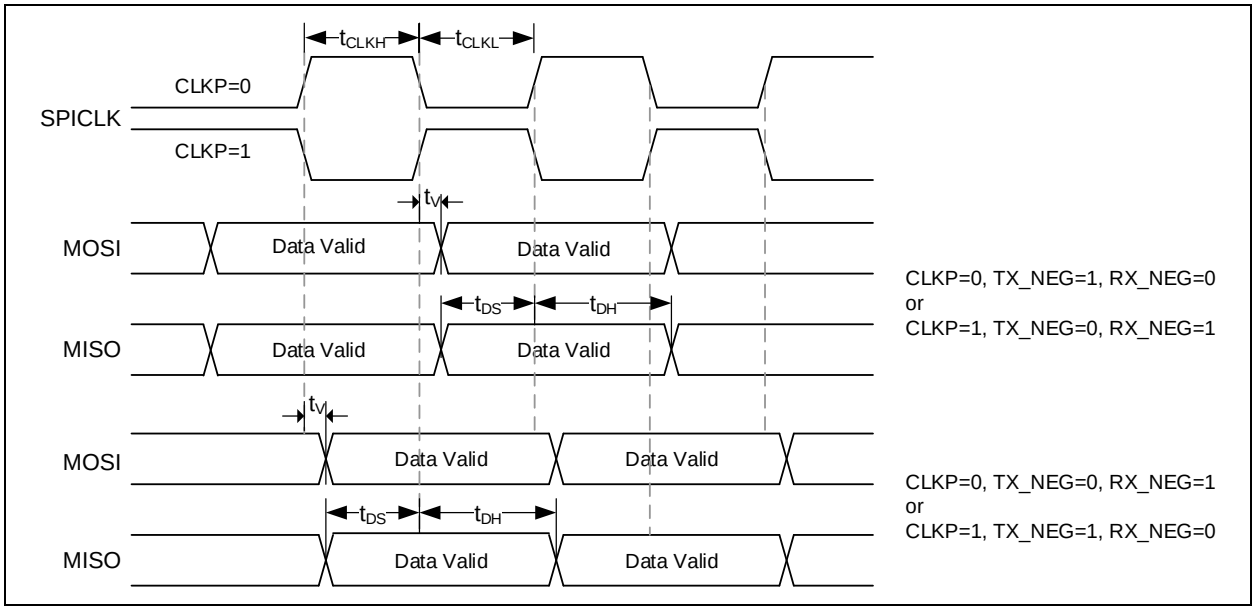


Figure 8.6-4 USCI-SPI Master Mode Timing Diagram

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	7	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	7		1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		1 T_{SPICLK} + 3ns	-	-		1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns	
t_{DS}	Data input setup time	2	-	-	ns	
t_{DH}	Data input hold time	4	-	-	ns	
t_V	Data output valid time	-	-	65	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	70		1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-5 USCI-SPI Slave Mode Characteristics

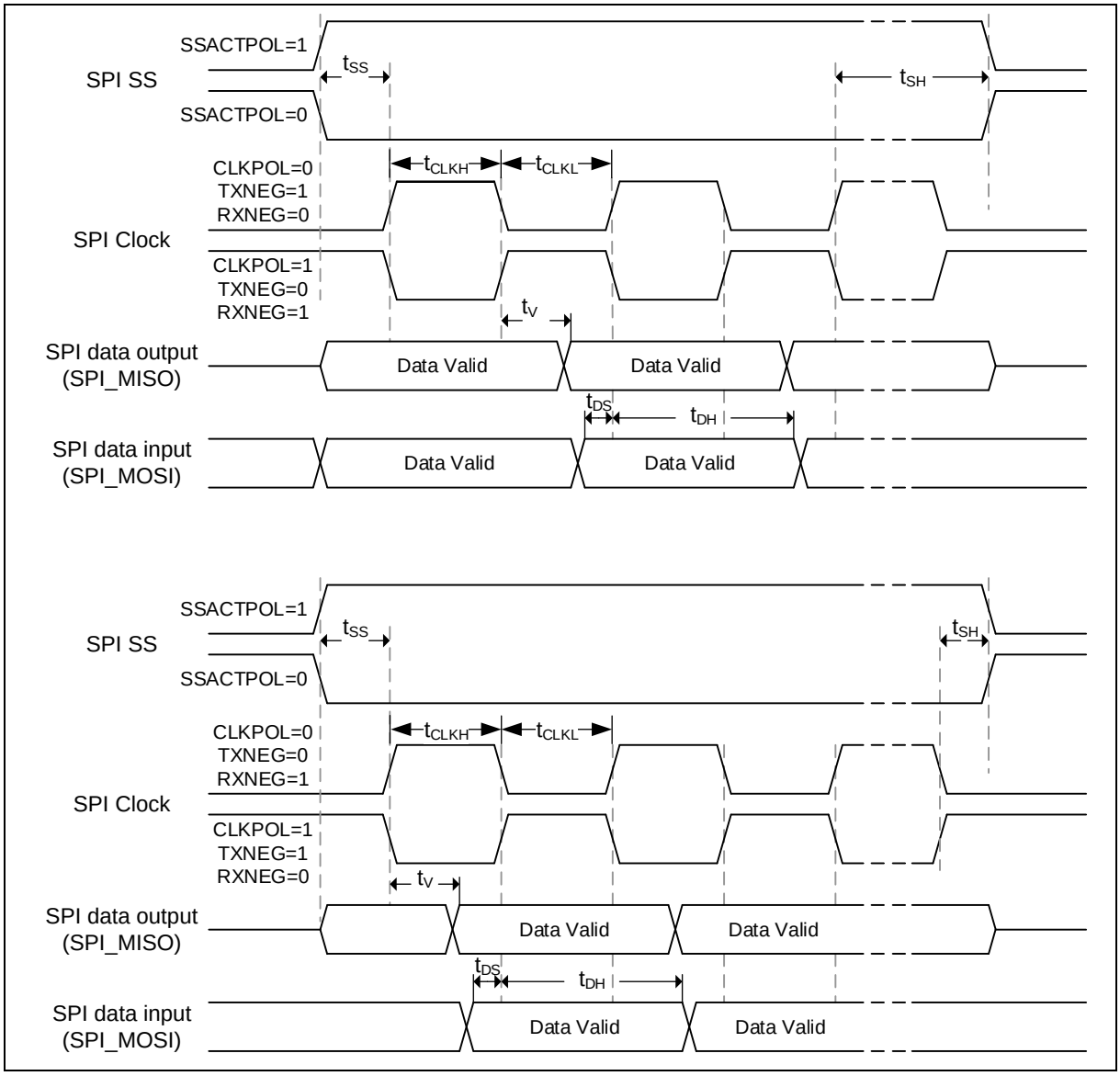


Figure 8.6-5 USCI-SPI Slave Mode Timing Diagram

8.6.4 USCI-I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	µs
t_{HIGH}	SCL high period	4	-	0.6	-	µs
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	µs
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	µs
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	µs
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	µs
$t_{SU;DAT}$	Data setup time	250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	µs
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	ns
t_f	SCL/SDA fall time	-	300	-	300	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-6 USCI-I²C Characteristics

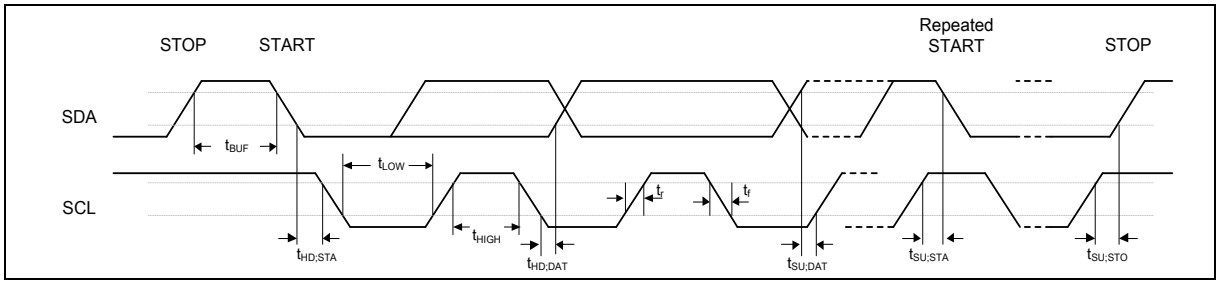


Figure 8.6-6 USCI-I²C Timing Diagram

8.6.5 USB Characteristics

8.6.5.1 USB Full-Speed Characteristics

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{BUS}	USB full speed transceiver operating voltage	4.4		5.25	V	
V_{DD33}[*2]	USB Internal power regulator output	3.0	3.3	3.6	V	
V_{IH}	Input high (driven)	2.0	-	-	V	-
V_{IL}	Input low	-	-	0.8	V	-
V_{DI}	Differential input sensitivity	0.2	-	-	V	|(USB_D+) - (USB_D-)|
V_{CM}	Differential common-mode range	0.8	-	2.5	V	Includes V_{DI} range
V_{SE}	Single-ended receiver threshold	0.8	-	2.0	V	-
	Receiver hysteresis	-	200	-	mV	-
V_{OL}	Output low (driven)	0	-	0.3	V	-
V_{OH}	Output high (driven)	2.8	-	3.6	V	-
V_{CRS}	Output signal cross voltage	1.3	-	2.0	V	-
R_{PU}	Pull-up resistor	1.19	-	1.9	kΩ	-
V_{TRM}	Termination voltage for upstream port pull-up (RPU)	3.0	-	3.6	V	
Z_{DRV}[*3]	Driver output resistance	-	10	-	Ω	Steady state drive
C_{IN}	Transceiver capacitance	-	-	26	pF	Pin to GND

Note:

1. Guaranteed by characterization result, not tested in production.
2. To ensure stability, an external 1 μF output capacitor, 1uF external capacitor must be connected between the USB_VDD33_CAP pin and the closest GND pin of the device.
3. USB_D+ and USB_D- must be connected with series resistors to fit USB Full-speed spec request (28 ~ 44Ω).

Table 8.6-7 USB Full-Speed Characteristics

8.6.5.2 USB Full-Speed PHY characteristics

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
T_{FR}	rise time	4	-	20	ns	C_L=50 pF
T_{FF}	fall time	4	-	20	ns	C_L=50 pF
T_{FRFF}	rise and fall time matching	90	-	111.11	%	$T_{FRFF} = T_{FR}/T_{FF}$

Note:

1. Guaranteed by characterization result, not tested in production.

Table 8.6-8 USB Full-Speed PHY Characteristics

8.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

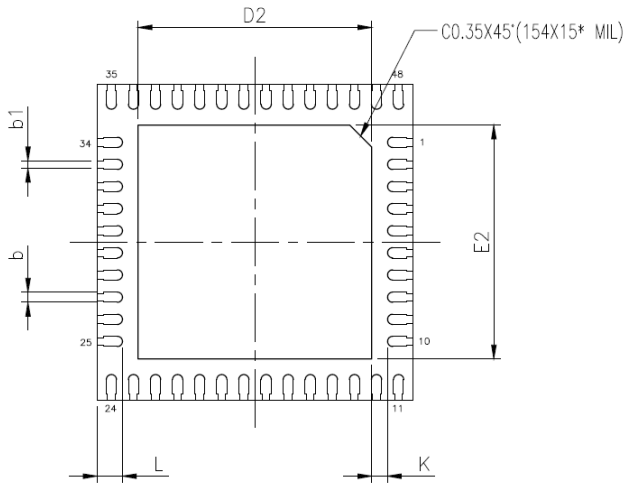
Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_{ERASE}	Page erase time	-	20	-	ms	
T_{PROG}	Program time	-	60	-	µs	
I_{DD1}	Read current	-	7	-	mA	
I_{DD2}	Program current	-	8	-	mA	
I_{DD3}	Erase current	-	12	-	mA	
N_{ENDUR}	Endurance	20,000	-		cycles[1]	T_J = -40°C~85°C
T_{RET}	Data retention	65	-	-	year	20 kcycle[2] T_J = 55°C
		10	-	-	year	20 kcycle[2] T_J = 85°C

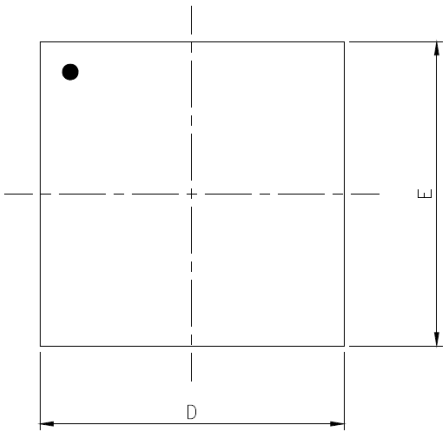
Note:

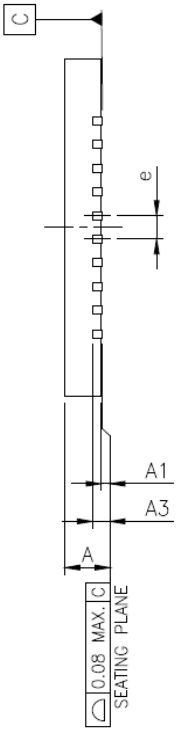
1. Number of program/erase cycles.
2. Guaranteed by design.

9 PACKAGE DIMENSIONS

9.1 QFN 48-pin (5X5x0.9 mm Pitch:0.35 mm)



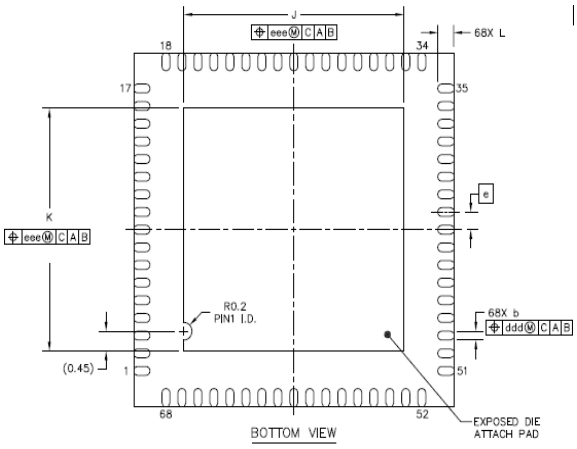


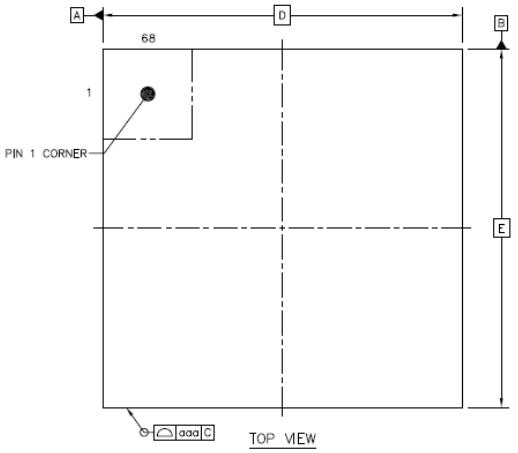


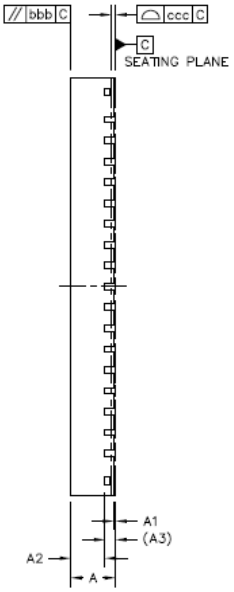
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.13	0.18	0.23
b1	0.07	0.12	0.17
D		5.00 BSC	
E		5.00 BSC	
e		0.35 BSC	
K	0.20	—	—

PAD SIZE	D2			E2			L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
154X15* MIL	3.65	3.70	3.75	3.65	3.70	3.75	0.35	0.40	0.45

9.2 QFN 68-pin (8X8x0.9 mm Pitch:0.4 mm)







		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	5.4	5.5	5.6
	Y	K	5.4	5.5	5.6
LEAD LENGTH		L	0.3	0.4	0.5
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
ADC	Enhanced Analog-to-Digital Converter
EBI	External Bus Interface
EMAC	Ethernet MAC Controller
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12 MHz Internal High Speed RC Oscillator
HXT	4~32 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	38.4 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation

QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Description
2020.07.21	1.00	Initial version.
2020.08.18	1.01	Updated Multi-function Pin Diagram in section 4.1.3.1.
2021.12.15	2.00	Added new part numbers for M032BTxI / M032BTxG and updated the description of the new part numbers.
2022.03.21	2.01	Revised M032BTAG8AN & M032BTAIAAN part number typo error in section 3.2.2.

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Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

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