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3.2 Gbps Transimpedance Amplifier with AGC

M02013

Low-power, high-sensitivity 3.2 Gbps transimpedance amplifier fabricated in a sub-micro CMOS process

The M02013 is a transimpedance amplifier (TIA) with automatic gain control (AGC) manufactured in a sub-micron, CMOS process. The AGC allows more than 25 dB of dynamic range, providing a low-cost solution for longer-reach 3.2 Gbps ATM/SONET systems.

For optimum system performance, the M02013 die should be mounted with a silicon or InGaAs PIN photodetector inside a lensed TO-Can or other optical sub-assembly.

The M02013 reverse biases the PIN by approximately 1.8 volts to optimise performance. A replica of the average photodiode current is available at the MON pad for alignment and 'LOSS of SIGNAL' monitoring.

Transimpedance Amplifier (TIA)

The TIA consists of a high gain single-ended CMOS amplifier with a feedback resistor. The feedback creates a virtual earth low impedance at the input, and virtually all of the input current passes through the feedback resistor, defining the voltage at the output. Advanced CMOS design techniques are employed to maintain the stability of this stage across all input conditions. Single-ended amplifiers have inherently poor power supply noise rejection. For this reason, an on-chip low dropout linear regulator has been incorporated into the design to give excellent noise rejection up to several MHz. Higher frequency power supply noise is removed by the external 470 pF decoupling capacitor connected to PINK.

The circuit is designed for PIN photodiodes in the “grounded cathode” configuration with the anode connected to the input of the TIA and the cathode connected to AC ground, such as the provided PINK terminal. Reverse DC bias is applied to reduce the photodiode capacitance. Avalanche photodiodes can be connected externally to a higher voltage.

Automatic Gain Control (AGC)

The M02013 has been designed to operate over the input range of +3 dBm to –23 dBm @ 3.2 Gbps and –24 dBm @ 2.5 Gbps. This represents a ratio of 1:300, whereas the acceptable dynamic range of the output is only 1:30 which implies a compression of 10:1 in the transimpedance. The design uses a MOS transistor operating in the triode region as a “voltage controlled resistor” to achieve the transimpedance variation.

KEY FEATURES

- Typical -23 dBm sensitivity, +3 dBm saturation at 3.2 Gbps
- Typical differential transimpedance: 10kΩ
- Differential output
- Operates with +3.3V supply
- Monitor output
- AGC provides dynamic range of more than 25 dB

Another feature of the AGC is that it only operates on signals greater than –17.5 dBm (@ 0.9 A/W). This knee in the gain response is important when setting “signal detect” functions in the following post amplifier. It also aids in active photodiode alignment.

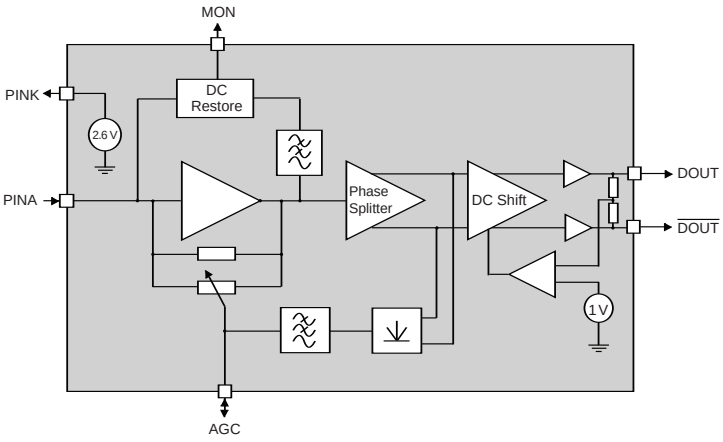
The AGC pad allows the AGC to be disabled during photodiode alignment by grounding the pad through a low impedance. The AGC control voltage can be monitored during normal operation at this pad by a high impedance (>10 MΩ) circuit.

Output Stage

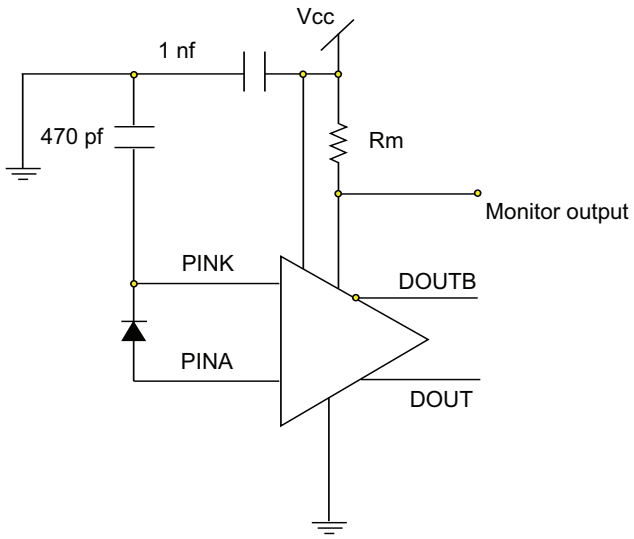
The signal from the TIA enters a phase splitter followed by a DC-shift stage and a pair of voltage follower outputs. These are designed to drive a differential (100Ω) load. They are stable for driving capacitive loads, such as interstage filters. Each output has its own GND pad, all four GND pads on the chip should be connected for proper operation. Since the M02013 exhibits rapid roll-off (3 pole), simple external filtering is sufficient.

Monitor O/P

High impedance O/P sinks replicate average photodiode current for monitoring purposes.



M02013 Block Diagram



Recommended Circuit

Product Highlights

Applications

- ATM/SDH/SONET
- OC-48 with FEC
- L4 Modules
- 2x Fiber Channel

Ordering Information

- M02013-A3: wafle pack (WP)
- M02013-QSPBG: quarter wafer

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