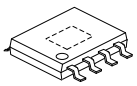
0.8V REFERENCE ULTRA LOW DROPOUT LINEAR REGULATOR



HSOP-8

■ DESCRIPTION

The UTC **LXXLD70** is a typical LDO with the features of very low dropout voltage as low as 0.15V at output current 7.0A.

For normal operation, two supply voltages are necessary. One called control voltage from other equipment can shutdown the output voltage and it should pull and hold the voltage of EN pin less than 0.3V. Another one is the main supply voltage whose purpose is for main power conversion, to keep the power dissipation low, and to make the dropout voltage lower.

Internally, in the UTC **LXXLD70**, there're many functions which can be seen in the block figure to prevent the IC from being damaged. Internal Power-On-Reset (POR) circuit can control the two supply voltages to prevent fault operations of the circuit; the thermal shutdown circuit is able to protect the device from over thermal operation, and a current limit function will keep the device work safely under current over-loads.

The UTC **LXXLD70** can be used as an ideal to provide well supply voltage in the applications, such as front-side-bus termination on motherboard, NB applications, front side bus V_{TT} (1.2V/7.0A) and note book PC applications.

■ FEATURES

* Low Dropout V_D= 0.15V (typ.) @ I_{OUT}=7.0A
* Low ESR Output Capacitor
* V_{REF}=0.8V
* ±1.5% over Line, Load and Temperature Output Accuracy
* Fast Transient Response
* Output Voltage Adjustable through External Resistors
* POR (Power-On-Reset) controlling V_{CNTL} and V_{IN}
* With internal Soft-Start
* Internal Current Limit Protection
* Internal Under Voltage Protection
* Hysteretic Thermal Shutdown
* With Power-OK Output (with a Delay Time)
* For Standby or Suspend Mode: Shutdown

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
LXXLD70L-SH2-R	LXXLD70G-SH2-R	HSOP-8	Tape Reel
LXXLD70L-SH2-T	LXXLD70G-SH2-T	HSOP-8	Tube

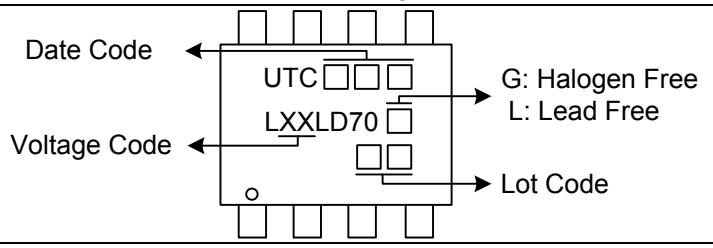
Note: XX: Output Voltage, refer to Marking Information.

LXXLD70L-SH2-R

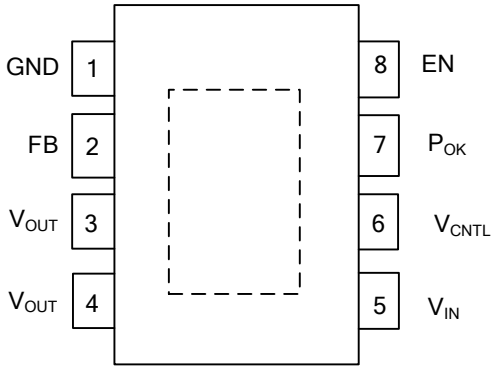
(1) Packing Type	(1) R: Tape Reel, T: Tube
(2) Package Type	(2) SH2: HSOP-8
(3) Lead Free	(3) G: Halogen Free, L: Lead Free
(4) Output Voltage Code	(4) XX: refer to Marking Information

Copyright © 2011 Unisonic Technologies Co., Ltd

■ MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING
HSOP-8	AD : ADJ	

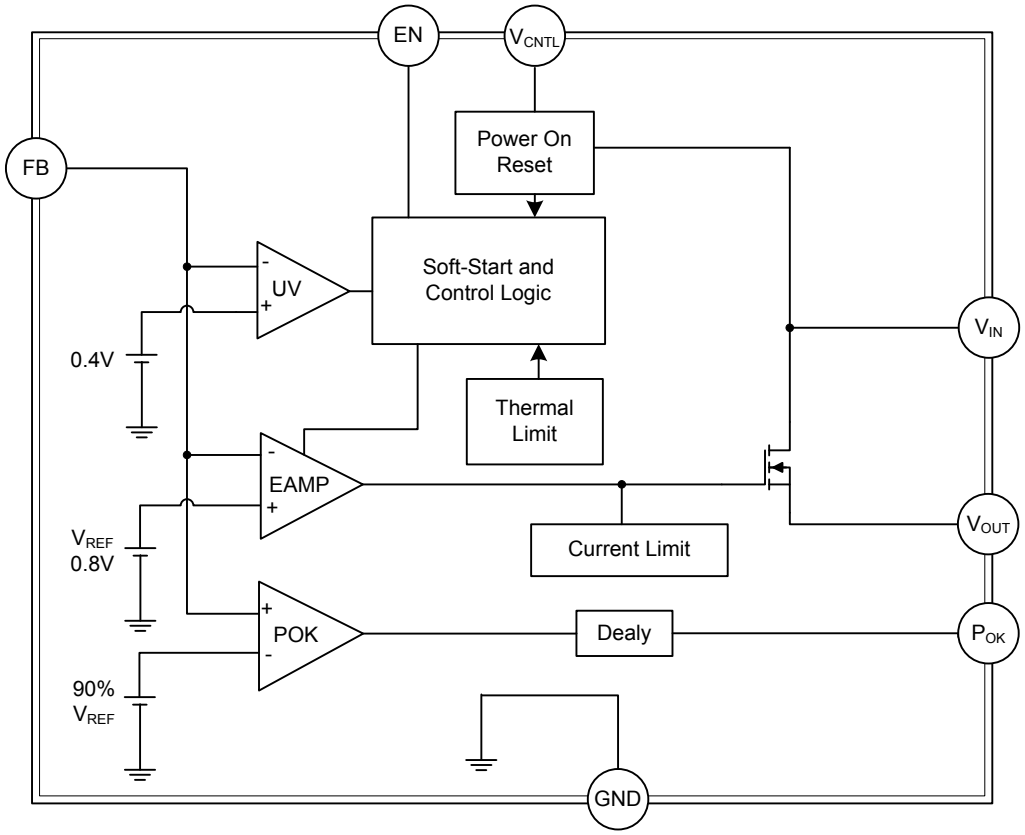
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground pin.
2	FB	There's an external resistor divider connected to this pin which is necessary to give the feedback voltage to the regulator. The external circuit is combined as the follow: between V_{OUT} and FB is R1(connected with a bypass capacitor which can improve the load transient response),and between FB and ground is R2.The value of R2 and R1 are recommended between 100Ω~10kΩ.So the output voltage is equals: $V_{OUT}=0.8\cdot(1+\frac{R1}{R2})(V)$
3	V_{OUT}	The output voltage pin of the regulator. There should be set an output capacitor to compensate for closed-loop and also to improve transient responses. It's necessary to connect Pin 3 and Pin 4 together by wide tracks.
4	V_{OUT}	
5	V_{IN}	This pin is the main supply input. It's necessary to connect the Exposed Pad and V_{IN} together for lower dropout voltage. Monitoring this pin's voltage can reset Power-On.
6	V_{CNTL}	Power input pin of the control circuitry. Connecting this pin to a +5V (recommended) supply voltage provides the bias for the control circuitry. The voltage at this pin is monitored for Power-On Reset purpose.
7	P_{OK}	Output pin for Power-OK signal output. Being an open drain output, through senescing FB voltage, this pin can show the users the output voltage's states. That's this pin will be low under any of these two situations: the rising FB voltage is not above the V_{POK} threshold; the falling FB voltage is below the V_{PNOK} threshold. That indicates the output voltage is not ready for users.
8	EN	Input Enable control pin. The output voltage can be shut down when this pin is below 0.3V. This pin's voltage can be set higher than V_{CNTL} voltage by an internal 10μA current source, and then the regulator will begin working normally.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (V_{CNTL} to GND)	V_{CNTL}	-0.3 ~ +7	V
Supply Voltage (V_{IN} to GND)	V_{IN}	-0.3 ~ +3.9	V
EN and FB to GND	$V_{I/O}$	-0.3 ~ V_{CNTL}+0.3	V
POK to GND Voltage	V_{POK}	-0.3 ~ +7	V
Power Dissipation	P_D	3	W
Lead Soldering Temperature, 10 Seconds	T_{SDR}	260	°C
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient in Free Air (Note 1)	θ_{JA}	38	°C/W
Junction to Case (Note 2)	θ_{JC}	14	°C/W

Notes: 1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of HSOP-8 is soldered directly on the PCB.
2. The Thermal Pad Temperature is measured on the PCB copper area connected to the thermal pad of package.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
VCNTL Supply Voltage	V_{CNTL}	4.5 ~ 6	V
VIN Supply Voltage	V_{IN}	1.0 ~ 3.5	V
Output Voltage , V_{CNTL}=5.0±5%	V_{OUT}	0.8 ~ V_{IN}-0.2	V
Output Current	I_{OUT}	0 ~ 7	A
Junction Temperature	T_J	+125	°C

■ ELECTRICAL CHARACTERISTICS

(Refer to the typical application circuit. These specifications apply over, V_{CNTL}=5V, V_{IN}=1.25V, V_{OUT}=1.05V and T_A=-40 ~ 85°C, unless otherwise specified. Typical values are at T_A=25°C).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{CNTL} Supply Current	I_{VCNTL}	EN=V_{CNTL}, V_{FB} is well regulated	0.4	1.0	2.0	mA
V_{CNTL} Shutdown Current	I_{SD}	EN=GND		280	380	μA
POWER-ON-RESET (POR)						
Rising V_{CNTL} POR Threshold		V_{CNTL} Rising	2.7	2.9	3.1	V
V_{CNTL} POR Hysteresis				0.4		V
Rising V_{IN} POR Threshold		V_{IN} Rising	0.8	0.9	1.0	
V_{IN} POR Hysteresis				0.5		V
OUTPUT VOLTAGE						
Reference Voltage	V_{REF}	FB=V_{OUT}		0.8		V
Output Voltage Accuracy		I_{OUT}=0~7A, T_J=-40 ~ 125°C	-1.5		+1.5	%
Line Regulation		V_{CNTL}=4.5 ~ 6V	-1.5		+1.5	mV/V
Load Regulation		I_{OUT}=0 ~ 7A		0.06	0.15	%
DROPOUT VOLTAGES						
V_{IN}-to-V_{OUT} Dropout Voltage	V_{DROP}	I_{OUT}=7A, V_{CNTL}=5V, T_J=25°C		0.11	0.14	V
		I_{OUT}=7A, V_{CNTL}=5V, T_J=-40~125°C			0.2	V
PROTECTIONS						
Current-Limit Level	I_{LIM}	V_{CNTL}=5V, T_J=25°C	8	10	12	A
		V_{CNTL}=5V, T_J=-40~125°C	7.2			A
Thermal Shutdown Temperature	T_{SD}	T_J Rising		150		°C
Thermal Shutdown Hysteresis				50		°C
Under-Voltage Threshold		V_{FB} Falling		0.4		V
ENABLE AND SOFT-START						
EN Logic High Threshold Voltage		V_{EN} Rising	0.3	0.4	0.5	V
EN Hysteresis				30		mV
EN Pull-High Current		EN=GND		10		μA
Soft-Start Interval	T_{SS}			2		ms
POWER-OK AND DELAY						
P_{OK} Threshold Voltage for Power OK	V_{POK}	V_{FB} Rising	90%	92%	94%	V_{REF}
P_{OK} Threshold Voltage for Power Not OK	V_{PNOK}	V_{FB} Falling	79%	81%	83%	V_{REF}
P_{OK} Pull-Low Voltage		P_{OK} Sinks 5mA		0.25	0.4	V
P_{OK} Delay Time	T_{DELAY}		1	3	10	ms

■ APPLICATION INFORMATION

1. Power Sequencing

When there's no main voltage applied at V_{IN}, it is suggested not to apply a voltage to V_{OUT} for a long time. Because the internal parasitic diode (between V_{OUT} to V_{IN}) will conduct and dissipate power, there's no protection.

2. Output Capacitor

A proper output capacitor to maintain stability and improve transient response over temperature and current is necessary. Proper ESR (equivalent series resistance) and capacitance of the output capacitor should be selected properly for stability of the normal operation and good load transient response.

Many kinds of capacitors can be used as an output capacitor, such as ultra-low-ESR capacitors (like ceramic chip capacitors), low-ESR bulk capacitors (like solid Tantalum, POSCap, and Aluminum electrolytic capacitors). And also the value of the output capacitors' can be increased without limit.

In the applications with large stepping load current, the low-ESR bulk capacitors are normally recommended.

Decoupling ceramic capacitors are recommended to be placed at the load and ground pins very closely and also the impedance of the layout must be minimized.

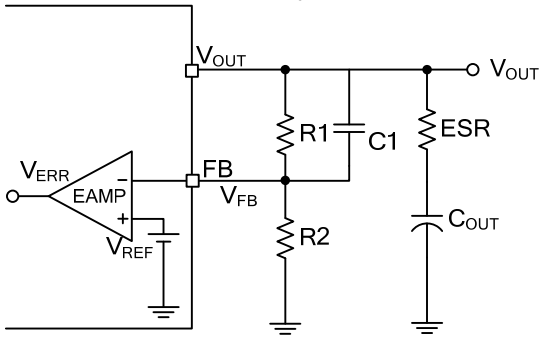
3. Input Capacitor

In order to prevent the input rail from dropping, the proper input capacitor to supply current surge during stepping load transients is required. Because the limited slew rate of the surge currents, more parasitic inductance needs more input capacitance.

Ultra-low-ESR capacitors (>100mF, ESR<300mW) is recommended for the input capacitor.

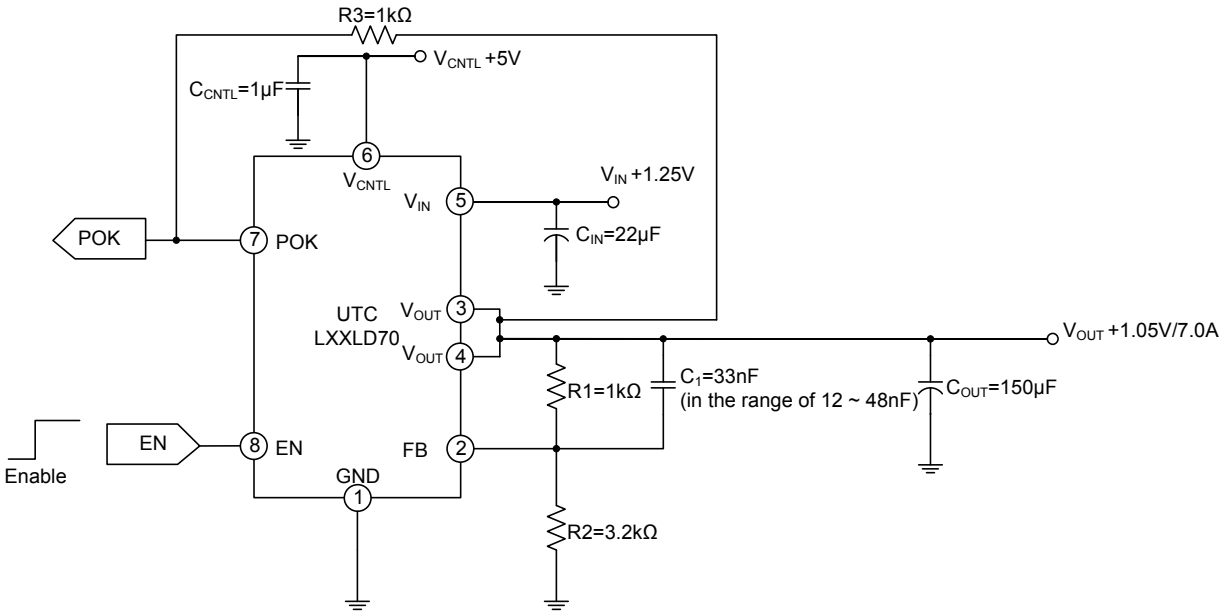
4. Feedback Network

The following figure shows the feedback network between V_{OUT} GND and FB pins. Working with the internal error amplifier, the feedback network can provide proper frequency response for the UTC **LXXLD70**.

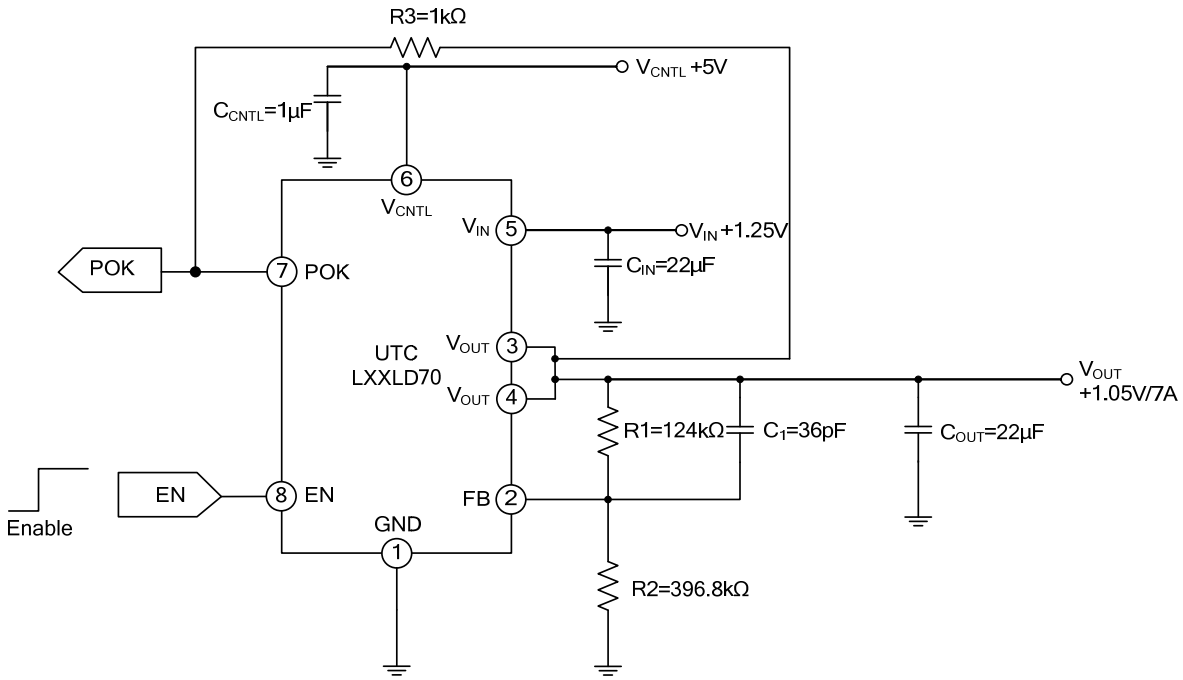


■ TYPICAL APPLICATION CIRCUITS

1. Using an Output Capacitor with ESR≥18mΩ



2. Using an MLCC as the Output Capacitor



C_{OUT} (μF)	V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C1 (pF)
22	1.2	120	240	36
	1.5	120	137.14	39
	1.8	105	184	39
44	1.05	240	768	39
	1.2	187	374	47
	1.5	180	205.71	47
	1.8	162	129.6	47

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.