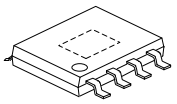
LXXLD50

CMOS IC

0.8V REFERENCE ULTRA LOW DROPOUT LINEAR REGULATOR



HSOP-8

■ DESCRIPTION

The UTC **LXXLD50** is a 5A ultra low dropout linear regulator providing designers with well supply voltage for applications of NB and front-side-bus termination on motherboards.

A control voltage for the circuitry and a main supply voltage for power conversion are needed as supply voltages to reduce power dissipation and provide extremely low dropout.

The UTC **LXXLD50** contains some function circuits. A Power-On-Reset (POR) circuit monitors both supply voltages to prevent undesired operations. A thermal shutdown and current limit circuits prevent this device from being damaged due to thermal and current over-loads. A POK indicates the output status with a pre-set time delay. It can control other converter for power sequence. The UTC **LXXLD50** can be enabled by other power system. Pulling and holding the EN pin below 0.3V shuts off the output.

The UTC **LXXLD50** is ideal for applications,such as front side bus VTT (1.2V/5A), note book PC applications, and motherboard applications.

■ FEATURES

* Low Dropout V_D=0.2V(Typ.)@ I_{OUT}=5A
* Low ESR Output Capacitor
* V_{REF}=0.8V
* High Output Accuracy : ±1.5% Over Line, Load and Temperature
* Fast Transient Response
* 1.2V, 1.5V, 1.8V, 2.5V Output Options by Connecting ADJ to GND and Output Voltage can be Adjusted by External Resistors
* Power-On-Reset Monitoring both Supply Voltages (V_{CNTL} and V_{IN} Pins)
* Protection function: Internal Soft-Start
  Current-Limit Protection
  Under-Voltage Protection
  Thermal Shutdown with Hysteresis
  Over-Voltage Protection
* Power-OK Output with a Delay Time
* Shutdown for Standby or Suspend Mode
* Lead Free Available (RoHS Compliant)

■ ORDERING INFORMATION

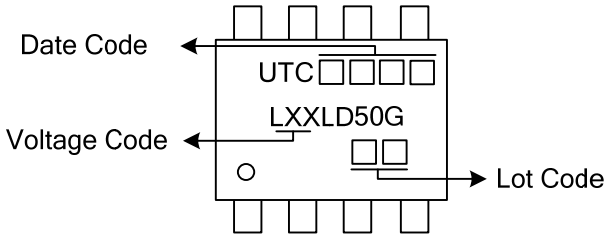
Ordering Number		Package	Packing
Lead Free	Halogen Free		
LXXLD50L-SH2-R	LXXLD50G-SH2-R	HSOP-8	Tape Reel

Note: xx: Output Voltage, refer to Marking Information.

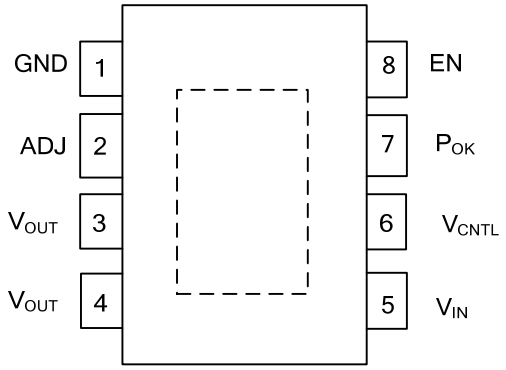
LXXLD50L-SH2-R (1) Packing Type (2) Package Type (3) Lead Free (4) Output Voltage Code	(1) R: Tape Reel (2) SH2: HSOP-8 (3) G: Halogen Free, Lead Free (4) xx: refer to Marking Information

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■ MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING
HSOP-8	25 : 2.5V AD: ADJ	

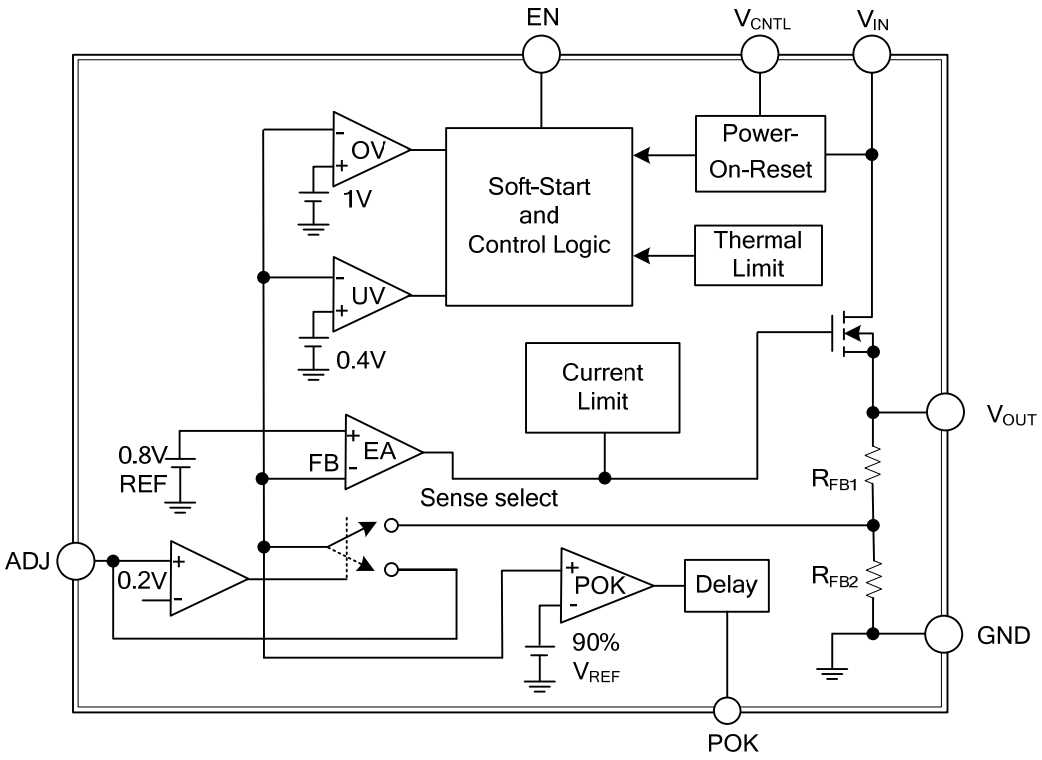
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground pin of the circuitry. All voltage levels are measured with respect to this pin.
2	ADJ	This pin, when grounded, sets the output voltage by the internal feedback resistors; If external feedback resistors are used, the output voltage will be V_{OUT}=0.8· (1+R1/R2) (V) where R1 is connected from VOUT to ADJ with Kelvin sensing and R2 is connected from ADJ to GND. A bypass capacitor may be connected with R1in parallel to improve load transient response. The recommended R2 and R1 are in the range of 100~10kΩ.
3	V_{OUT}	Output of the regulator. Please connect Pin 3 and 4 together using wide tracks. It is necessary to connect a output capacitor with this pin for closed-loop compensation and improving transient responses.
4	V_{OUT}	
5	V_{IN}	Main supply input pins for power conversions. The Exposed Pad provide a very low impedance input path for the main supply voltage. Please tie the Exposed Pad and VIN Pin (Pin 8) together to reduce the dropout voltage. The voltage at this pins is monitored for Power-On Reset purpose.
6	V_{CNTL}	Power input pin of the control circuitry. Connecting this pin to a +5V (recommended) supply voltage provides the bias for the control circuitry. The voltage at this pin is monitored for Power-On Reset purpose.
7	P_{OK}	Power-OK signal output pin. This pin is an open-drain output used to indicate status of output voltage by sensing FB voltage. This pin is pulled low when the rising FB voltage is not above the VPOK threshold or the falling FB voltage is below the VPNOK threshold, indicating the output is not OK.
8	EN	Enable control pin. Pulling and holding this pin below 0.3V shuts down the output. When re-enabled, the IC undergoes a new soft-start cycle . Left this pin open, an internal current source 10mA pulls this pin up to V_{CNTL} voltage, enabling the regulator.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
VCNTL Supply Voltage (V_{CNTL} to GND)	V_{CNTL}	-0.3 ~ 7	V
VIN Supply Voltage (V_{IN} to GND)	V_{IN}	-0.3 ~ 3.3	V
EN and FB to GND	$V_{I/O}$	-0.3 ~ V_{CNTL}+0.3	V
POK to GND	V_{POK}	-0.3 ~ 7	V
Average Power Dissipation	P_D	3	W
Peak Power Dissipation (<20mS)	P_{PEAK}	20	W
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-65 ~ 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	40	°C/W

Note: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of SOP-8-P is soldered directly on the PCB.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	RATINGS	UNIT
V_{CNTL} Supply Voltage		V_{CNTL}	3.1 ~ 6	V
V_{IN} Supply Voltage		V_{IN}	1.1 ~ 3.3	V
Output Voltage	V_{CNTL}=3.3±5%	V_{OUT}	0.8 ~ 1.2	V
	V_{CNTL}=5.0±5%		+0.8 ~ V_{IN}-0.2	V
V_{OUT} Output Current		I_{OUT}	0 ~ 6	A
Operating Junction Temperature		T_J	-25 ~ 125	°C

■ ELECTRICAL CHARACTERISTICS

(Refer to the typical application circuit. These specifications apply over, V_{CNTL} = 5V, V_{IN} = 1.5V, V_{OUT} = 1.2V or V_{IN} = 1.8V, V_{OUT} = 1.5V or V_{IN} = 2.1V, V_{OUT} = 1.8V or V_{IN} = 2.8V, V_{OUT} = 2.5V and T_A = 0 ~ 70°C, unless otherwise specified. Typical values refer to T_A = 25°C.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{CNTL} Supply Current	I_{CNTL}	EN = V_{CNTL},	0.4	1	8	mA
V_{CNTL} Shutdown Current	I_{SD}	EN = GND		200	380	μA
POWER-ON-RESET						
V_{CNTL} POR Threshold		V_{CNTL} Rising	2.7	2.9	3.1	V
V_{CNTL} POR Hysteresis				0.4		V
V_{IN} POR Threshold		V_{IN} Rising	0.8	0.9	1.0	
V_{IN} POR Hysteresis				0.5		V
OUTPUT VOLTAGE						
Reference Voltage	V_{REF}	ADJ =V_{OUT}		0.8		V
Output Voltage Accuracy		I_{OUT}=0A ~ 5A, T_J= -25 ~125°C	-1.5		+1.5	%
Line Regulation		V_{CNTL}=3.3 ~ 5.5V		0.06	0.3	%
Load Regulation		I_{OUT}=0A ~ 5A		0.06	0.15	%
DROPOUT VOLTAGE						
Dropout Voltage		I_{OUT} = 5A, V_{CNTL}=5V, T_J= 25°C		0.2	0.25	V
		I_{OUT} = 5A, V_{CNTL}=5V, T_J= -50~125°C			0.3	V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION						
Current Limit	I_{LIMIT}	V_{CNTL}=5V, T_J= 25°C	7	8	9	A
		V_{CNTL}=5V, T_J= -25 ~ 125°C	6			A
		V_{CNTL}=3.3V, T_J= 25°C	6.3	6.7	8.8	A
		V_{CNTL}=3.3V, T_J= -25 ~ 125°C	6			A
Thermal Shutdown Temperature	T_{SD}	T_J Rising		150		°C
Thermal Shutdown Hysteresis				25		°C
Under-Voltage Threshold		ADJ Falling		0.4		V
Over-Voltage Threshold	V_{OVP}/V_{normal}	Output Voltage up regulation voltage		125		%
ENABLE AND SOFT-START						
EN Logic High Threshold Voltage		V_{EN} Rising	0.3	0.4	0.5	V
EN Hysteresis				30		mV
EN Pin Pull-Up Current		EN=GND		10		μA
Soft-Start Interval	T_{SS}			1.2		ms
POWER OK AND DELAY						
P_{OK} Threshold Voltage for Power OK	V_{POK}	V_{ADJ} Rising	90%	92%	94%	V_{REF}
P_{OK} Threshold Voltage for Power Not OK	V_{PNOK}	V_{ADJ} Falling	79%	81%	83%	V_{REF}
P_{OK} Low Voltage		POK sinks 5mA		0.2	0.4	V
P_{OK} Delay Time	T_{DELAY}		1	1.5	10	mS
ADJ						
Adjust Pin threshold			0.1	0.2	0.4	V

■ FUNCTIONAL DESCRIPTION

Power-On-Reset

A POR (Power-On-Reset) circuit is designed to monitor the two supply voltages at V_{CNTL} pin and V_{IN} pin to avoid the unexpected operations. During powering on process, the POR circuit would initiate a soft-start process after the two supply voltages above their rising POR threshold voltages. The POR function also pulls low the P_{OK} pin regardless the output voltage when the voltage at V_{CNTL} pin drops below its falling POR threshold.

Internal Soft-Start

The built-in soft-start circuit controls rise rate of the output voltage to limit the current surge at start-up. The soft-start interval is approximately 1.2mS (TYP.).

Output Voltage Regulation

The error amplifier compares a temperature-compensated 0.8V reference with the feedback voltage, which is characterized with high bandwidth and DC gain to provide fast transient response and less load regulation.

The output voltage can be adjusted by an output NMOS to get the preset voltage. The difference which is amplified by the error amplifier provides load current from V_{IN} pin to V_{OUT} pin.

Current-Limit

The current-limit protection circuit is used to protect this device against the maximum current, which occurs in overload or short-circuit conditions. For the UTC **LXXLD50**, the current is monitored through the output NMOS.

Under-Voltage Protection (UVP)

The UTC **LXXLD50** monitors the voltage on internal feed back signal after soft-start process is finished. Thus, the Under-Voltage circuit is inactive during soft-start. When the voltage on FB signal goes below the under-voltage threshold, the UVP circuit shuts off the output immediately. Last for a period, this device starts a new soft-start to regulate output.

Over-Voltage Protection (OVP)

The UTC **LXXLD50** monitors the output voltage. When the voltage on V_{OUT} pin goes high beyond normal regulation voltage by 25%, the OVP circuit shuts off the output immediately. After a while, the **LXXLD50** starts a new soft-start to regulate output.

Thermal Shutdown

The thermal shutdown protection circuit is designed to prevent the junction temperature beyond a certain value. If the junction temperature becomes higher than +150°C, the output NMOS is turned off through a thermal sensor, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 25°C, resulting in a pulsed output during continuous thermal overload conditions.

The average junction temperature is reduced by the 25°C hysteresis during continuous thermal overload conditions, making this device use longer. Also, the power dissipation should be externally limited to ensure junction temperature under +125°C during normal operation.

Enable Control

If the EN pin is applied to a logic low signal (V_{EN}< 0.3V), the output would be shut down. Following a shutdown, a logic high signal re-enables the output through initiation of a new soft-start cycle. Left open, this pin is pulled up by an internal current source (10μA Typical) to enable operation. For a low cost-effectiveness, an external transistor is not required.

Power-OK and Delay

For the UTC **LXXLD50**, the Power-OK circuit indicates the status of the output voltage by monitoring the internal feedback voltage (V_{FB}). When the feedback voltage becomes equal to the rising Power-OK threshold (V_{POK}), an internal delay function starts to perform a delay time. At the end of the delay time, the IC shuts off the internal NMOS of the POK to indicate the output is OK. When the feedback voltage becomes equal to the falling Power-OK threshold (V_{PNOK}), the IC immediately turns on the NMOS of the P_{OK} to indicate the output is not OK without a delay time.

■ APPLICATION INFORMATION

Power Sequencing

Less consideration could be taken into the power sequencing of V_{IN} and V_{CNTL}. But do not apply a voltage to V_{OUT} for a long time when the main voltage applied at V_{IN} is not present. The reason is the internal parasitic diode from V_{OUT} to V_{IN} conducts and dissipates power without protections due to the forward-voltage.

Output Capacitor

For the maximum device performance and improving system stability, transient response over temperature and current, a well-suitable output capacitor is needed. The selected output capacitor should be qualified perfect ESR (equivalent series resistance) and capacitor value for a better system stability and load transient.

The UTC **LXXLD50** is designed with a programmable feedback compensation adjusted by an external feedback network for the use of wide ranges of ESR and capacitance in all applications. The output capacitors can be ultra-low-ESR capacitors, such as ceramic chip capacitors; low-ESR bulk capacitors, such as solid Tantalum, POSCap, and Aluminum electrolytic capacitors, and their values can be increased without limit.

During load transients, the output capacitors, depending on the stepping amplitude and slew rate of load current, are used to reduce the slew rate of the current seen by the UTC **LXXLD50** and help the device to minimize the variations of output voltage for good transient response. Therefore, low-ESR bulk capacitors are universally to be expected for the applications with large stepping load current.

In addition, decoupling ceramic capacitors must be located to the load and GND as close as possible and the layout's impedance should be maintained minimum.

Input Capacitor

The input capacitors should be chosen properly due to supply current to protect the input rail against dropping during stepping load transients. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN pin limit the slew rate of the surge currents. More parasitic inductance needs more input capacitance. More capacitance reduces the variations of the V_{IN} pin voltage.

For the UTC **LXXLD50**, input capacitors with low-ESR are not needed. Ultra-low-ESR capacitors (such as ceramic chip capacitors) are good options, and an aluminum electrolytic capacitor (>100μF, ESR <300mΩ) is recommended as the input capacitor.

Feedback Network

In the following, the feedback network between V_{OUT}, GND and FB pins is shown in Figure 1. It works with the internal error amplifier to provide proper frequency response for the linear regulator.

As seen in Figure 1, the ESR is the equivalent series resistance of the output capacitor. The C_{OUT} is ideal capacitance in the output capacitor. The V_{OUT} is the setting of the output voltage.

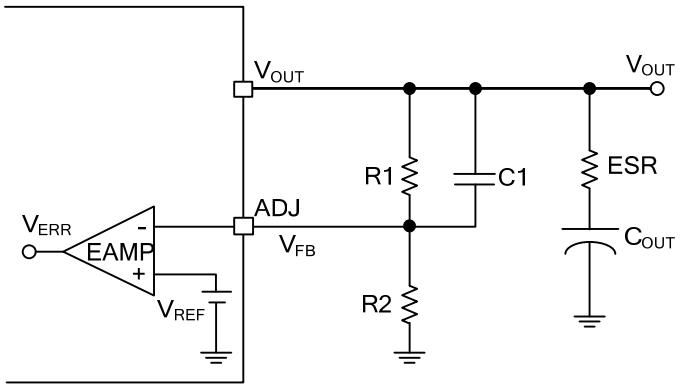
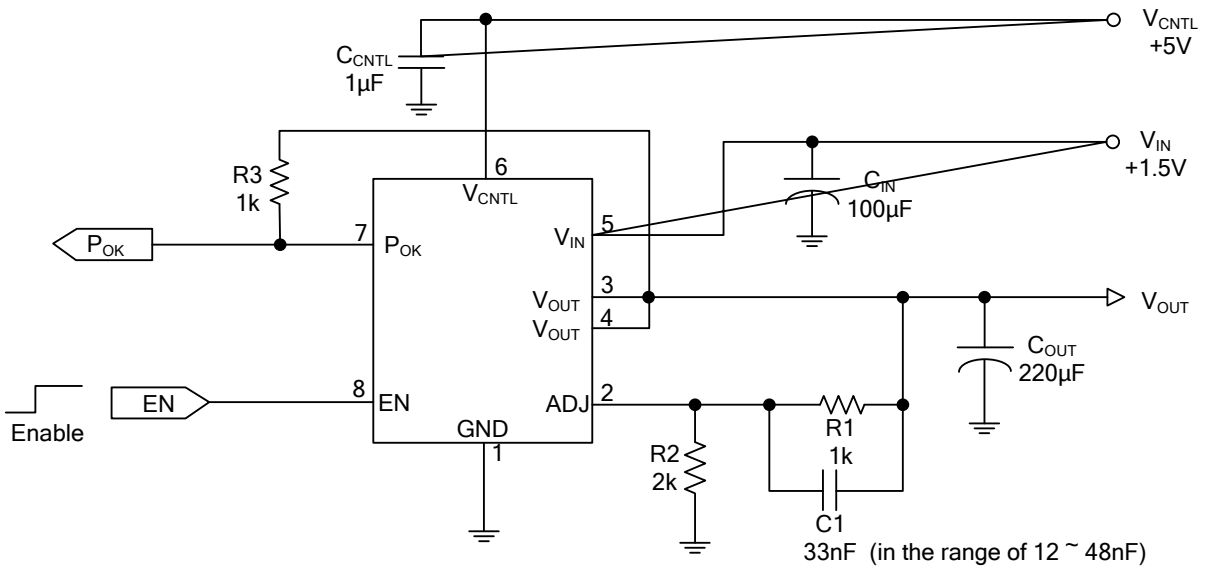


Figure 1.

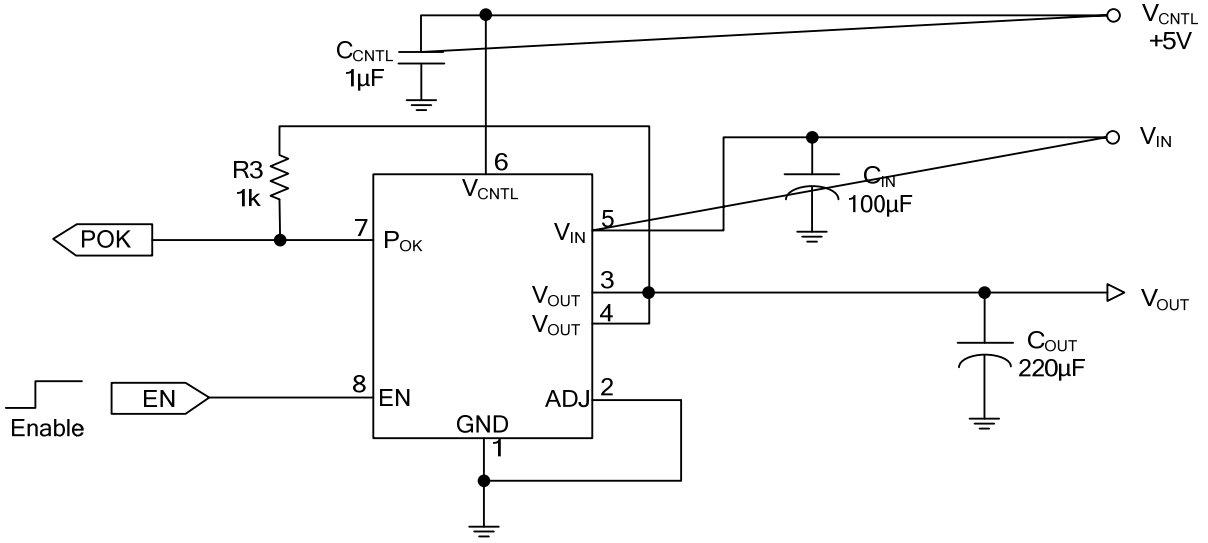
■ TYPICAL APPLICATION CIRCUIT

1. Using an Output Capacitor with ESR≥18mΩ

ADJ Mode



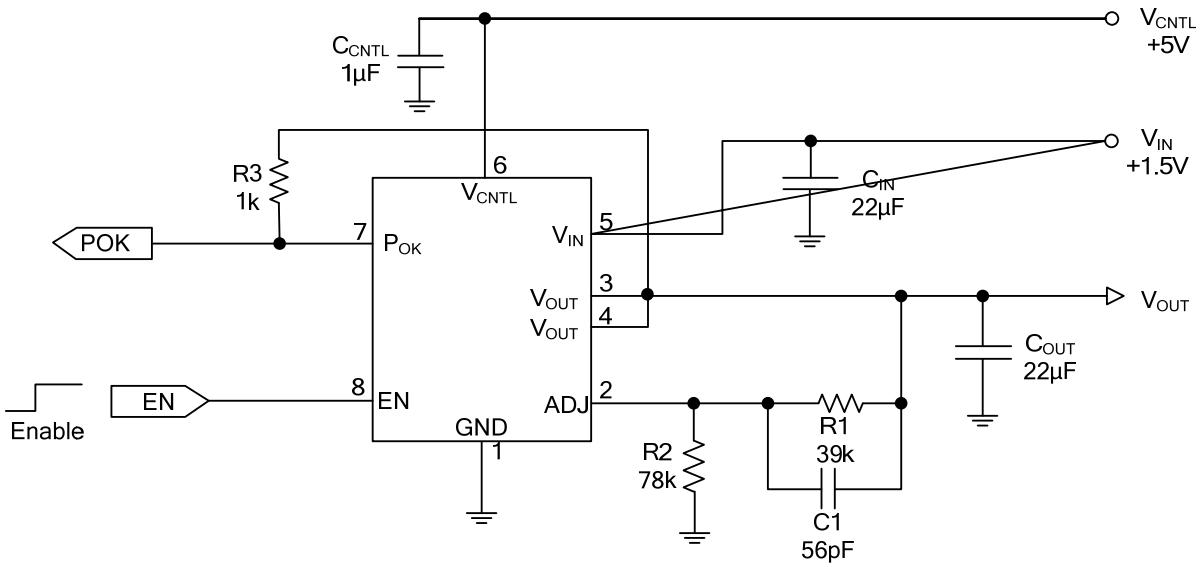
Fixed Voltage Mode



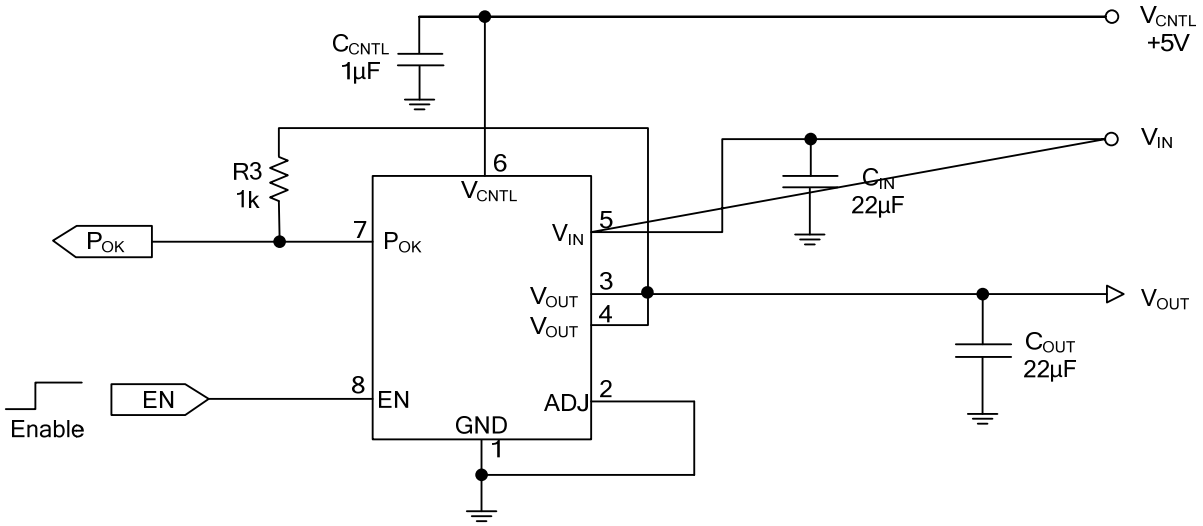
■ TYPICAL APPLICATION CIRCUIT (Cont.)

2. Using an MLCC as the Output Capacitor

ADJ Mode



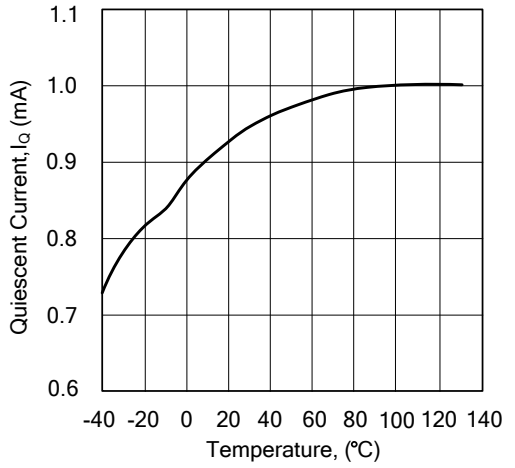
Fixed Voltage Mode



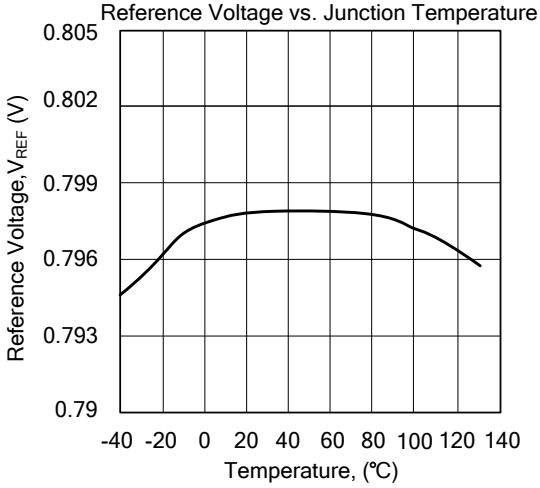
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C1 (pF)
1.05	43	137.6	47
1.5	27	30.86	82
1.8	15	12	150

■ TYPICAL CHARACTERISTICS

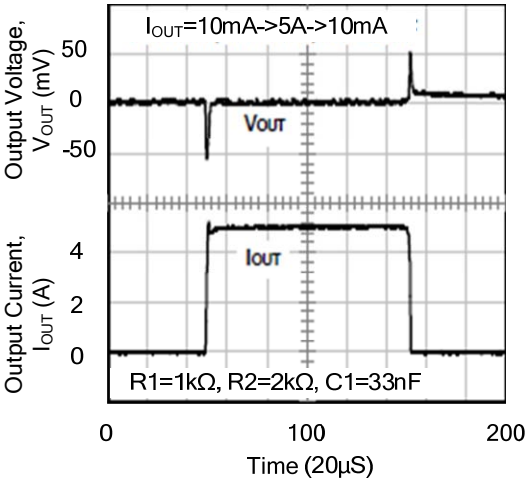
V_{CNTL} Supply Current vs. Junction Temperature



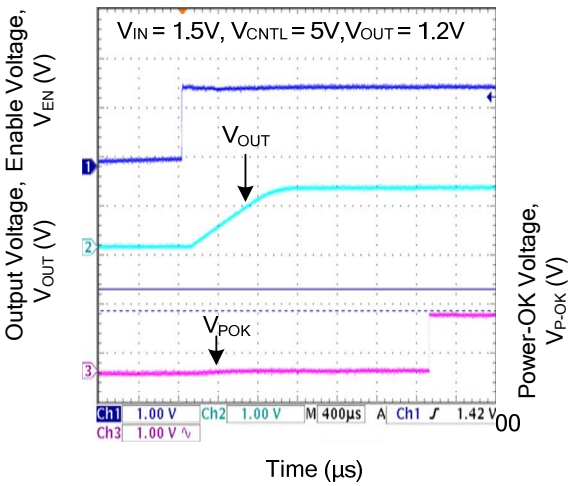
Reference Voltage vs. Junction Temperature



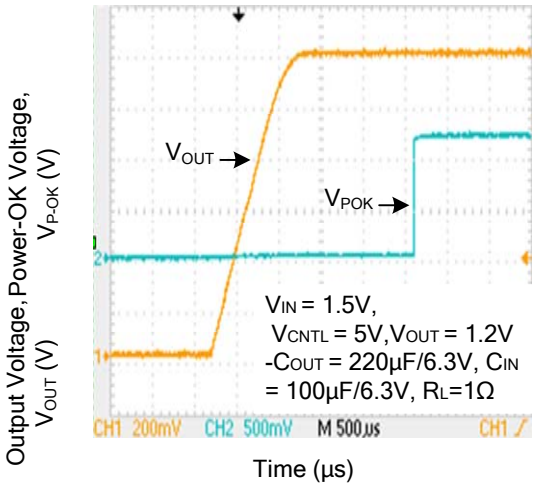
Load Transient



Enable



POK Delay



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