LXT300Z/LXT301Z

Advanced T1/E1 Short-Haul Transceivers

General Description

The LXT300Z and LXT301Z are fully integrated transceivers for both North American 1.544 Mbps (T1) and International 2.048 Mbps (E1) applications. They are pin and functionally compatible with standard LXT300/301 devices, with some circuit enhancements.

The LXT300Z provides receive jitter attenuation starting at 3 Hz, and is microprocessor controllable through a serial interface. The LXT301Z is pin compatible, but does not provide jitter attenuation or a serial interface. An advanced transmit driver architecture provides constant low output impedance for both marks and spaces, for improved Bit Error Rate performance over various cable network configurations. Both transceivers offer a variety of diagnostic features including transmit and receive monitoring. Clock inputs may be derived from an on-chip crystal oscillator or from digital inputs. They use an advanced double-poly, double-metal CMOS process and require only a single 5-volt power supply.

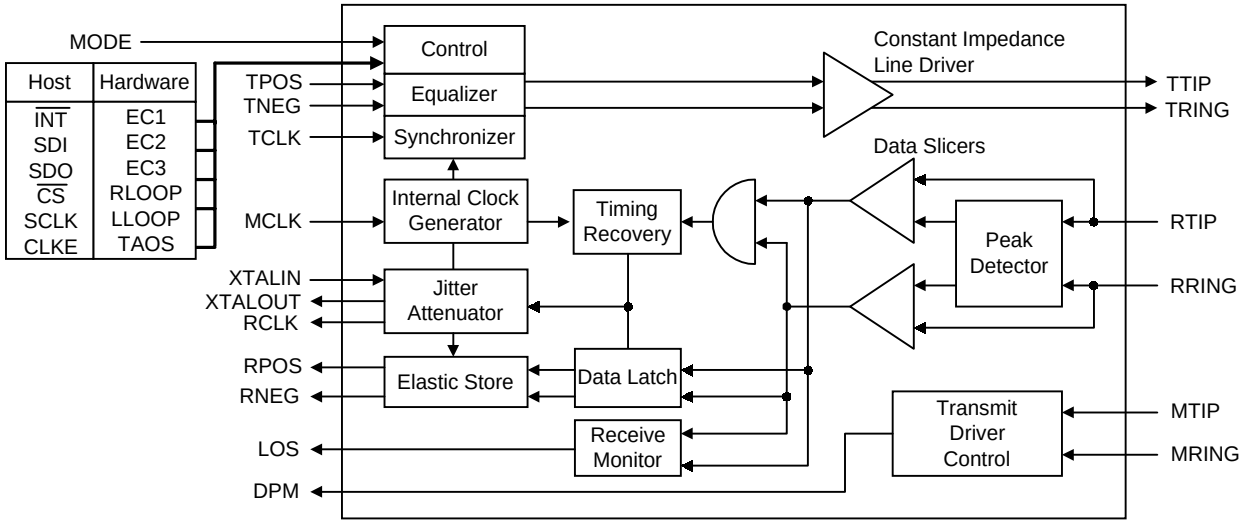
Applications

- PCM/Voice Channel Banks
- Data Channel Bank/Concentrator
- T1/E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High-speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

Features

- Data recovery and clock recovery functions
- Receive jitter attenuation starting at 3 Hz exceeds AT&T Pub 62411, Pub 43801, Pub 43802, ITU G.703, and ITU G.823 (LXT300Z only)
- Line driver with constant low mark and space impedance (3 Ω typical)
- Minimum receive signal of 500 mV
- Adaptive and selectable (E1/DSX-1) slicer levels for improved SNR
- Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft
- Local and remote loopback functions
- Digital Transmit Driver Monitor
- Digital Receive Monitor with Loss of Signal (LOS) output and first mark reset
- Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Microprocessor controllable (LXT300Z only)
- Compatible with most popular PCM framers
- Available in 28-pin DIP or PLCC

LXT300Z Block Diagram



PIN ASSIGNMENTS & SIGNAL DESCRIPTIONS

Figure 1: Pin Assignments

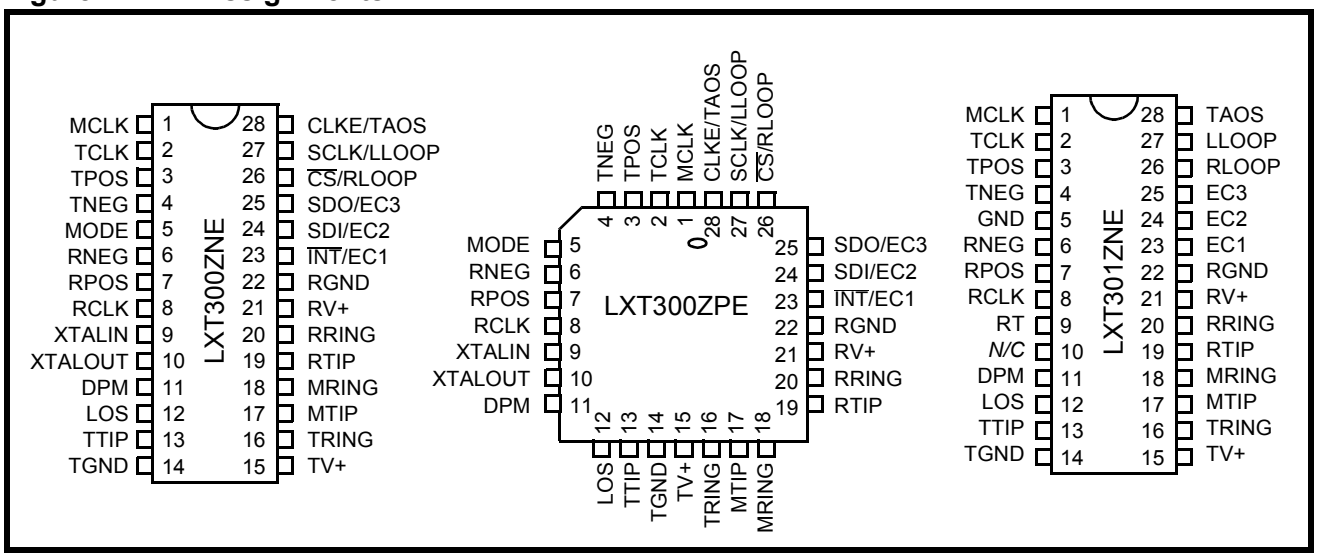


Table 1: Pin Descriptions

Pin #	Sym	I/O[1]	Description
1	MCLK	DI	**Master Clock.** A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. *LXT300Z Only: If MCLK is not applied, this pin should be grounded.*
2	TCLK	DI	**Transmit Clock.** Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK. If TCLK is grounded, the output drivers enter a high-Z state, except during Remote Loopback.
3	TPOS	DI	**Transmit Positive Data.** Input for positive pulse to be transmitted on the twisted-pair line.
4	TNEG	DI	**Transmit Negative Data.** Input for negative pulse to be transmitted on the twisted-pair line.
5	MODE	DI	**Mode Select *(LXT300z)*.** Setting MODE High puts the LXT300Z in the Host Mode. In the Host Mode, the serial interface is used to control the LXT300Z and determine its status. Setting MODE Low puts the LXT300Z in the Hardware (H/W) mode. In the Hardware Mode, the serial interface is disabled and hard-wired pins are used to control configuration and report status.
	GND	S	**Ground *(LXT301Z)*.** Tie to Ground.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
6	RNEG	DO	**Receive Negative Data; Receive Positive Data.** Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). Both outputs are stable and valid on the rising edge of RCLK. *LXT300Z only: In the Host Mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware Mode both outputs are stable and valid on the rising edge of RCLK.*
7	RPOS	DO	
8	RCLK	DO	**Recovered Clock.** This is the clock recovered from the signal received at RTIP and RRING.
9	XTALIN	AI	**Crystal Input; Crystal Output *(LXT300Z).*** An external crystal operating at four times the bit rate (6.176 MHz for DSX-1, 8.192 MHz for E1 applications with an 18.7 pF load) is required to enable the jitter attenuation function of the LXT300Z. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and floating the XTALOUT pin.
10	XTALOUT	AO	
9	RT	AI	**Receive Termination *(LXT301Z).*** Connect to RV+ through a 1 k Ω resistor.
10	N/C	–	**No Connection *(LXT301Z).***
11	DPM	DO	**Driver Performance Monitor.** DPM goes High when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ±2 clock periods. DPM remains High until a signal is detected.
12	LOS	DO	**Loss of Signal.** LOS goes High when 175 consecutive spaces have been detected. LOS returns Low when a mark is detected.
13	TTIP	AO	**Transmit Tip; Transmit Ring.** Differential Driver Outputs. These outputs are designed to drive a 25 Ω load. The transmitter will drive 100 Ω shielded twisted-pair cable through a 1:2 step-up transformer without additional components. To drive 75 Ω coaxial cable, two 2.2 Ω resistors are required in series with the transformer.
16	TRING	AO	
14	TGND	S	**Transmit Ground.** Ground return for the transmit drivers power supply TV+.
15	TV+	S	**Transmit Power Supply.** +5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3 V.
17	MTIP	AI	**Monitor Tip; Monitor Ring.** These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another LXT300Z or LXT301Z on the board.
18	MRING	AI	
19	RTIP	AI	**Receive Tip; Receive Ring.** The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG and RCLK pins.
20	RRING	AI	
21	RV+	S	**Receive Power Supply.** +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	S	**Receive Ground.** Ground return for power supply RV+.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
23	$\overline{\text{INT}}$	DO	**Interrupt *(Host Mode)*.** This *LXT300Z Host Mode* output goes Low to flag the host processor when LOS or DPM go active. $\overline{\text{INT}}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{\text{INT}}$ is reset by clearing the respective register bit (LOS and/or DPM).
	EC1	DI	**Equalizer Control 1 *(H/W Mode)*.** The signal applied at this pin in the *LXT300Z Hardware Mode and LXT301Z* is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
24	SDI	DI	**Serial Data In *(Host Mode)*.** The serial data input stream is applied to this pin when the *LXT300Z* operates in the *Host Mode.* SDI is sampled on the rising edge of SCLK.
	EC2	DI	**Equalizer Control 2 *(H/W Mode)*.** The signal applied at this pin in the *LXT300Z Hardware Mode and LXT301Z* is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
25	SDO	DO	**Serial Data Out *(Host Mode)*.** The serial data from the on-chip register is output on this pin in the *LXT300Z Host Mode.* If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{\text{CS}}$ is High.
	EC3	DI	**Equalizer Control 3 *(H/W Mode)*.** The signal applied at this pin in the *LXT300Z Hardware Mode and LXT301Z* is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
26	$\overline{\text{CS}}$	DI	**Chip Select *(Host Mode)*.** This input is used to access the serial interface in the *LXT300Z Host Mode.* For each read or write operation, $\overline{\text{CS}}$ must transition from High to Low, and remain Low.
	RLOOP	DI	**Remote Loopback *(H/W Mode)*.** This input controls loopback functions in the *LXT300Z Hardware Mode and LXT301Z.* Setting RLOOP High enables the Remote Loopback mode. Setting both RLOOP and LLOOP High causes a Reset.
27	SCLK	DI	**Serial Clock *(Host Mode)*.** This clock is used in the *LXT300Z Host Mode* to write data to or read data from the serial interface registers.
	LLOOP	DI	**Local Loopback *(H/W Mode)*.** This input controls loopback functions in the *LXT300Z Hardware Mode and LXT301Z.* Setting LLOOP High enables the Local Loopback Mode.
28	CLKE	DI	**Clock Edge *(Host Mode)*.** Setting CLKE High causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is Low, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	DI	**Transmit All Ones *(H/W Mode)*.** When High, TAOS causes the *LXT300Z (Hardware Mode) and LXT301Z* to transmit a continuous stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

FUNCTIONAL DESCRIPTION

The LXT300Z and LXT301Z are fully integrated PCM transceivers for both 1.544 Mbps (DSX-1) and 2.048 Mbps (E1) applications. Both transceivers allow full-duplex transmission of digital data over existing twisted-pair installations. The first page of this data sheet shows a simplified block diagram of the LXT300Z; Figure 2 shows the LXT301Z. The LXT301Z is similar to the LXT300Z, but does not incorporate the Jitter Attenuator and associated Elastic Store, or the serial interface port.

The LXT300Z and LXT301Z transceivers each interface with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

Power Requirements

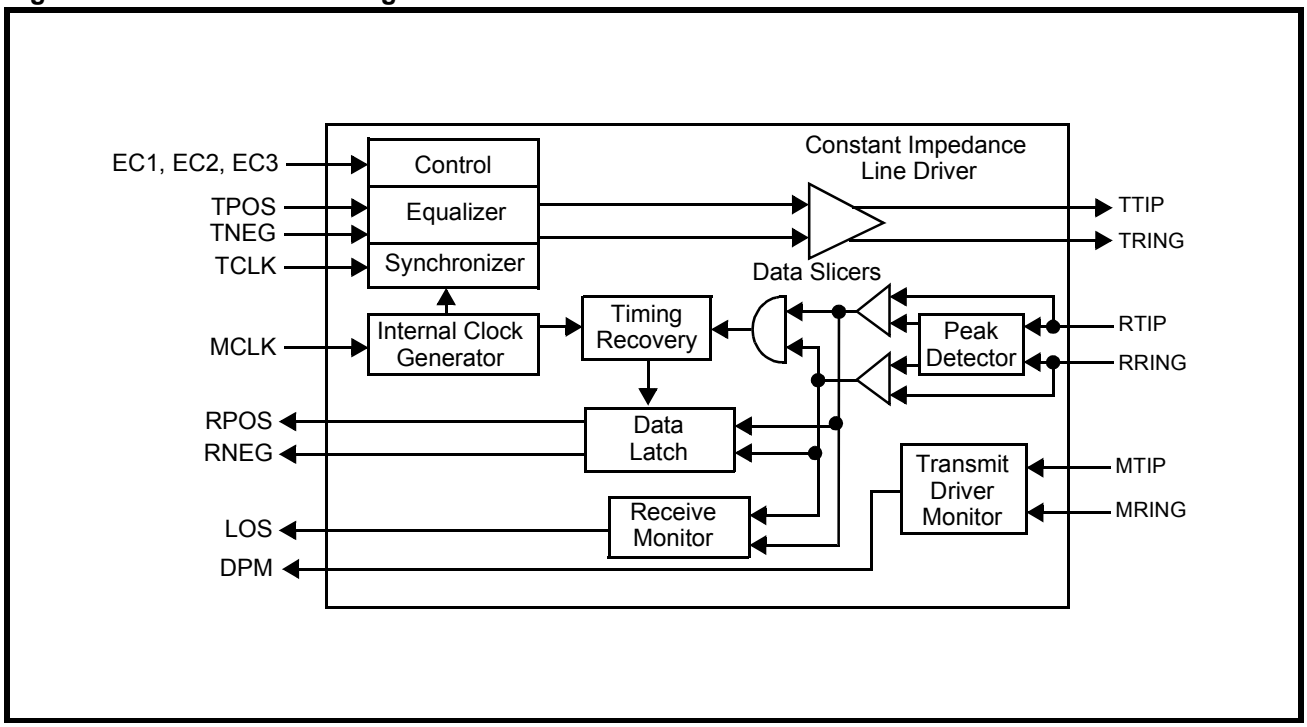
The LXT300Z and LXT301Z are low-power CMOS devices. Each operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± .3V of each other, and decoupled to their respective grounds separately. Refer to Application Information for typical decoupling circuitry. Isolation between the transmit and receive circuits is provided internally.

Reset Operation *(LXT300Z and LXT301Z)*

Upon power up, the transceiver is held static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. MCLK provides the receiver reference for the LXT301Z. The crystal oscillator provides the receiver reference in the LXT300Z. If the LXT300Z crystal oscillator is grounded, MCLK is used as the receiver reference clock.

The transceiver can also be reset from the Host or Hardware Mode. In Host Mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware Mode, reset is commanded by holding RLOOP and LLOOP High simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and then begins calibration.

Figure 2: LXT301Z Block Diagram



Receiver

The LXT300Z and LXT301Z receivers are identical except for the Jitter Attenuator and Elastic Store. The following discussion applies to both transceivers except where noted.

The signal is received from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to the Test Specifications section for receiver timing.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (determined by Equalizer Control inputs EC1~EC3 ≠ 000) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (EC inputs = 000) the threshold is set to 50%.

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB). Regardless of received signal level, the peak detectors are held above a minimum level of 300 mV to provide immunity from impulsive noise. (During LOS, RPOS and RNEG are squelched if the received input signal drops to 300 mV.)

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. *In the LXT300Z only, recovered clock signals are supplied to the jitter attenuator and the data latch. The recovered data is passed to the elastic store where it is buffered and synchronized with the dejittered recovered clock (RCLK).* The data and clock recovery circuits have an input jitter tolerance significantly better than required by Pub 62411.

Receive (Loss of Signal) Monitor

The receive monitor generates a Loss of Signal (LOS) output upon receipt of 175 consecutive zeros (spaces). The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes High, and the RCLK output is replaced with the MCLK. LOS is reset when the first mark is received.

(*In the LXT300Z only, if MCLK is not supplied the RCLK output will be replaced with the centered crystal clock.*)

Jitter Attenuation (LXT300Z Only)

In the LXT300Z only, recovered clock signals are supplied to the jitter attenuator and the data latch. The recovered data is passed to the elastic store where it is buffered and synchronized with the dejittered recovered clock (RCLK). Jitter attenuation of the LXT300Z clock and data outputs (see Figure 4) is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Application Information for crystal specifications. The ES is a 32 x 2-bit register. Recovered data is clocked into the ES with the recovered clock signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the receive path.

Transmitter

The transmitter circuits in the LXT300Z and LXT301Z are identical. The following discussion applies to both models. Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 2. Refer to the Test Specifications section for master and transmit clock timing characteristics. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Equalizer Control signals are hard-wired to the LXT301Z.

LXT300Z Only: Equalizer Control signals may be hard-wired in the Hardware Mode, or input as part of the serial data stream (SDI) in the Host Mode.

Pulses can be shaped for either 1.544 or 2.048 Mbps applications. DSX-1 applications with 1.544 Mbps pulses can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The LXT300Z and LXT301Z also match FCC specifications for CSU applications. Pulses at 2.048 Mbps can drive coaxial or shielded twisted-pair lines using appropriate resistors in line with the output transformer.

Driver Performance Monitor

The transceiver incorporates an advanced Driver Performance Monitor (DPM) in parallel with the TTIP and TRING at the output transformer. The DPM circuitry uses four comparators and a 150 ns pulse discriminator to filter glitches. The DPM output level goes high upon detection of 63 consecutive zeros, and is cleared when a one is detected on the transmit line, or when a reset command is received. The DPM output also goes High to indicate a ground on TTIP or TRING. A ground fault induced DPM flag is automatically cleared when the ground condition is corrected (chip reset is not required).

Line Code

The LXT300Z and LXT301Z transmit data as a 50% AMI line code as shown in Figure 3. Power consumption is reduced by activating the AMI line driver only to transmit a mark. The output driver is disabled during transmission of a space.

Operating Modes

The LXT300Z and LXT301Z transceivers can be controlled through hard-wired pins (Hardware Mode). Both transceivers can also be commanded to operate in one of several diagnostic modes.

LXT300Z Only: The LXT300Z can be controlled by a microprocessor through a serial interface (Host Mode). The mode of operation is set by the MODE pin logic level.

Host Mode Operation (LXT300Z Only)

To allow a host microprocessor to access and control the LXT300Z through the serial interface, MODE is set to 1. The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/Address byte and an 8-bit Data byte. Figure 4 shows the serial interface data structure and relative timing.

The Host Mode provides a latched Interrupt output ($\overline{\text{INT}}$) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte. Host Mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as listed in Table 3.

The LXT300Z serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The LXT300Z contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select ($\overline{\text{CS}}$) input to transition from High to Low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 4 lists serial data output bit combinations for each status. Serial data I/O timing characteristics are shown in the Test Specifications section.

Hardware Mode Operation *(LXT300Z and LXT301Z)*

In Hardware Mode the transceiver is accessed and controlled through individual pins. With the exception of the $\overline{\text{INT}}$ and CLKE functions, Hardware Mode provides all the functions provided in the Host Mode. In the Hardware Mode RPOS and RNEG outputs are valid on the rising edge of RCLK. The LXT301Z operates in Hardware Mode at all times.

LXT300Z Only: To operate in Hardware Mode, MODE must be set Low. Equalizer Control signals (EC1 through EC3) are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host Mode.

Figure 3: 50% AMI Coding

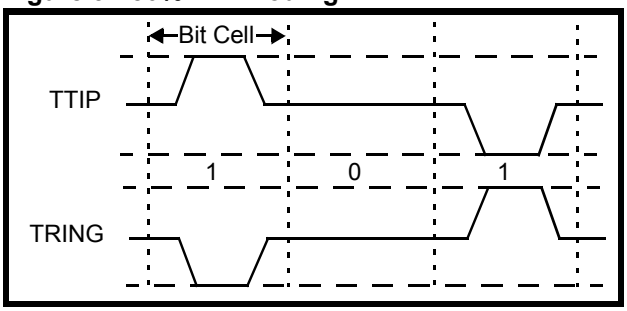


Table 2: LXT300Z Serial Data Output Bits
(See Figure 4)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS is active.
0	1	0	Local Loopback is active.
0	1	1	TAOS and Local Loopback are active.
1	0	0	Remote Loopback is active.
1	0	1	DPM has changed state since last Clear DPM occurred.
1	1	0	LOS has changed state since last Clear LOS occurred.
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred.

Table 3: Valid CLKE Settings

CLKE	Output	Clock	Valid Edge
Low	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
High	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising

Table 4: Equalizer Control Inputs

EC3	EC2	EC1	Line Length[1]	Cable Loss[2]	Application	Bit Rate
0	1	1	0 ~ 133 ft ABAM	0.6 dB	DSX-1	1.544 Mbps
1	0	0	133 ~ 266 ft ABAM	1.2 dB		
1	0	1	266 ~ 399 ft ABAM	1.8 dB		
1	1	0	399 ~ 533 ft ABAM	2.4 dB		
1	1	1	533 ~ 655 ft ABAM	3.0 dB		
0	0	0	ITU Recommendation G.703		E1	2.048 Mbps
0	1	0	FCC Part 68, Option A		CSU	1.544 Mbps

1. Line length from transceiver to DSX-1 cross-connect point.
2. Maximum cable loss at 772 kHz.

Diagnostic Mode Operation

Transmit All Ones

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of ones when the TAOS mode is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback.

Remote Loopback

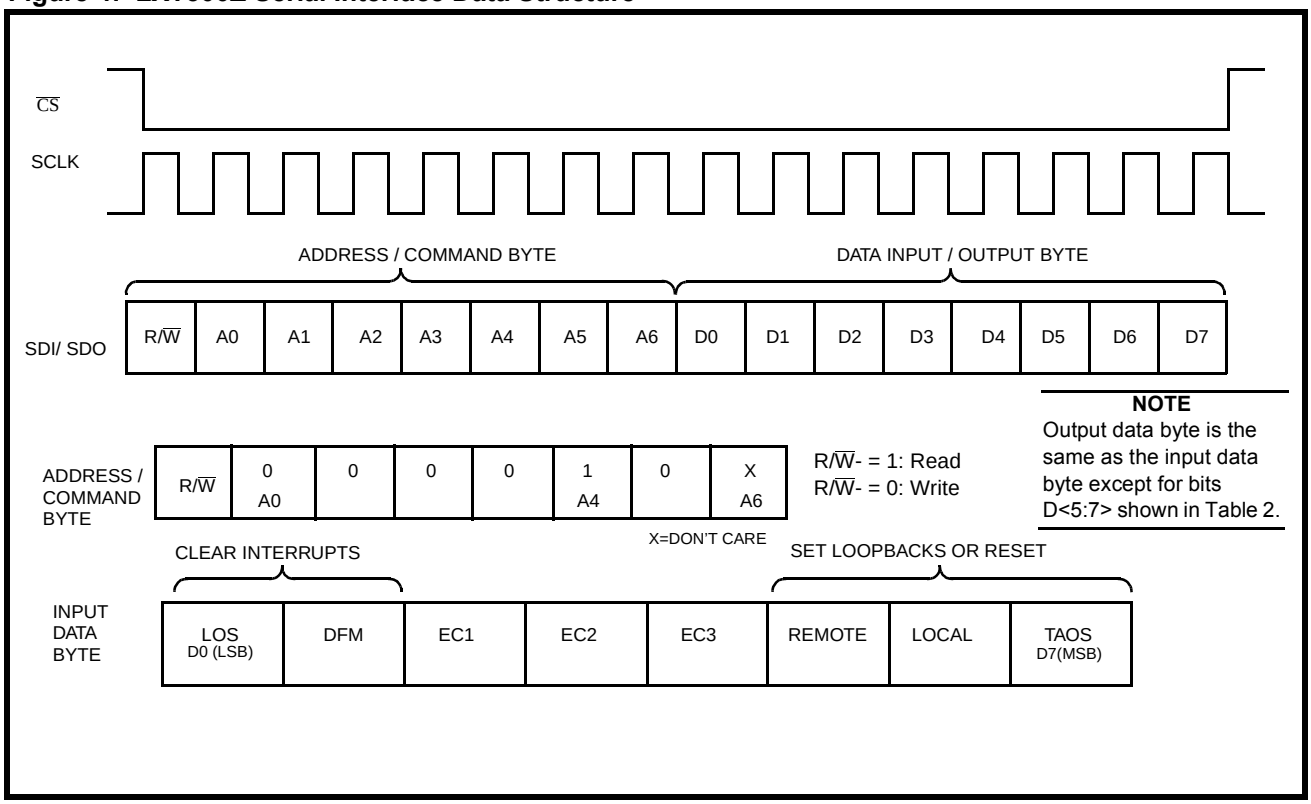
In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

Local Loopback

In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK) through the Rx jitter attenuator. The transmitter circuits are unaffected by the LLOOP command. The TPOS and TNEG inputs (or a stream of ones if the TAOS command is active) will be transmitted normally.

LXT300Z Only: When used in this mode with a crystal, the transceiver can be used as a stand-alone jitter attenuator.

Figure 4: LXT300Z Serial Interface Data Structure

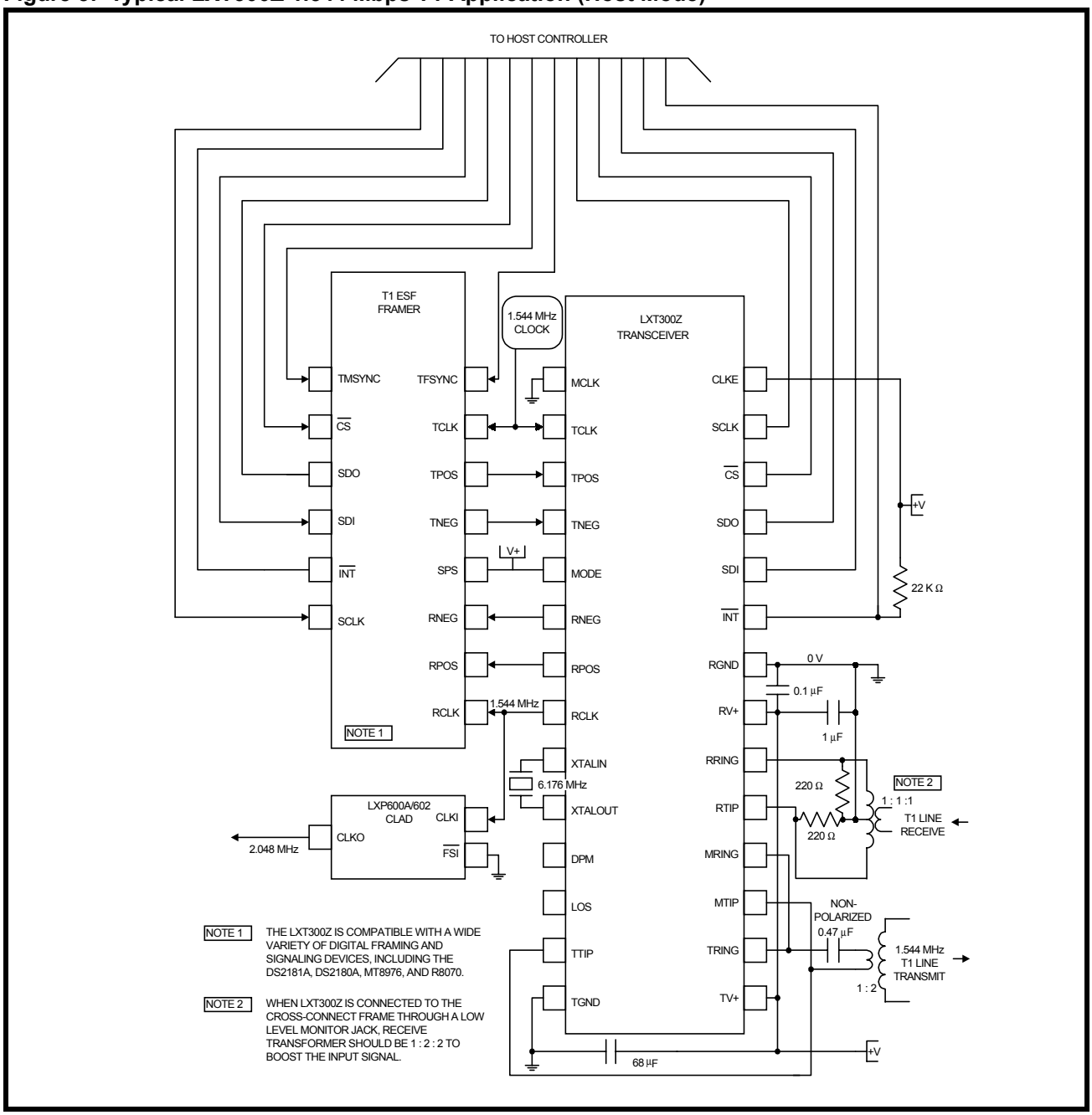


APPLICATION INFORMATION

LXT300Z Host Mode 1.544 Mbps T1 Interface Application

Figure 5 is a typical 1.544 Mbps T1 application. The LXT300Z is shown in the Host Mode with a typical T1/ESF framer providing the digital interface with the host controller. Both devices are controlled through the serial interface. An LXP600A Clock Adapter (CLAD) provides the 2.048 MHz system backplane clock, locked to the recovered 1.544 MHz clock signal. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (68 µF on the transmit side, 1.0 µF and 0.1 µF on the receive side).

Figure 5: Typical LXT300Z 1.544 Mbps T1 Application (Host Mode)



LXT300Z Hardware Mode E1 Interface Application

Figure 6 is a typical 2.048 Mbps E1 application. The LXT300Z is shown in Hardware Mode with a typical E1/CRC4 framer. Resistors are installed in line with the transmit transformer for loading a 75 Ω coaxial cable. The in-line resistors are not required for transmission on 120 Ω shielded twisted-pair lines. As in the T1 application Figure 5, this configuration is illustrated with a crystal in place to enable the LXT300Z Jitter Attenuation Loop, and a single power supply bus. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function

Figure 6: Typical LXT300Z 75 Ω E1 Application (Hardware Mode)

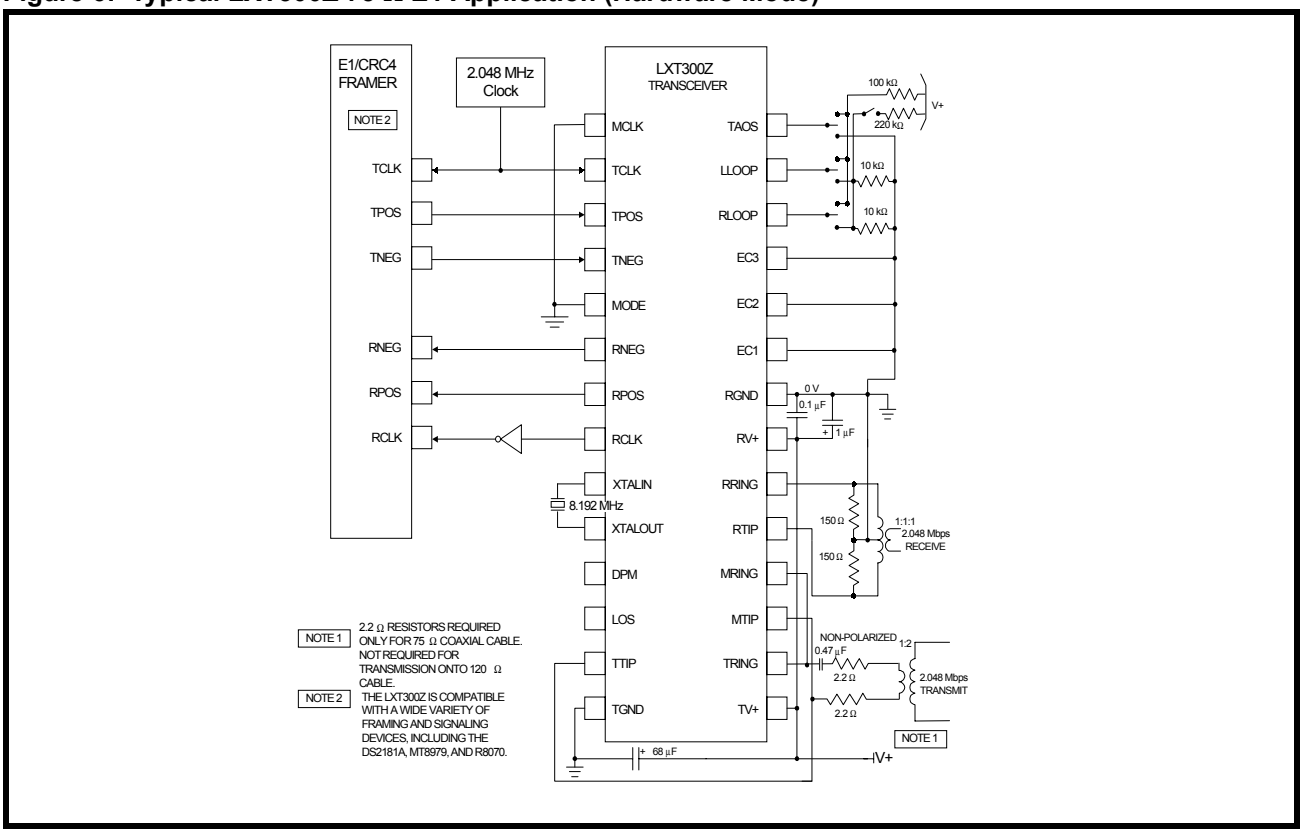


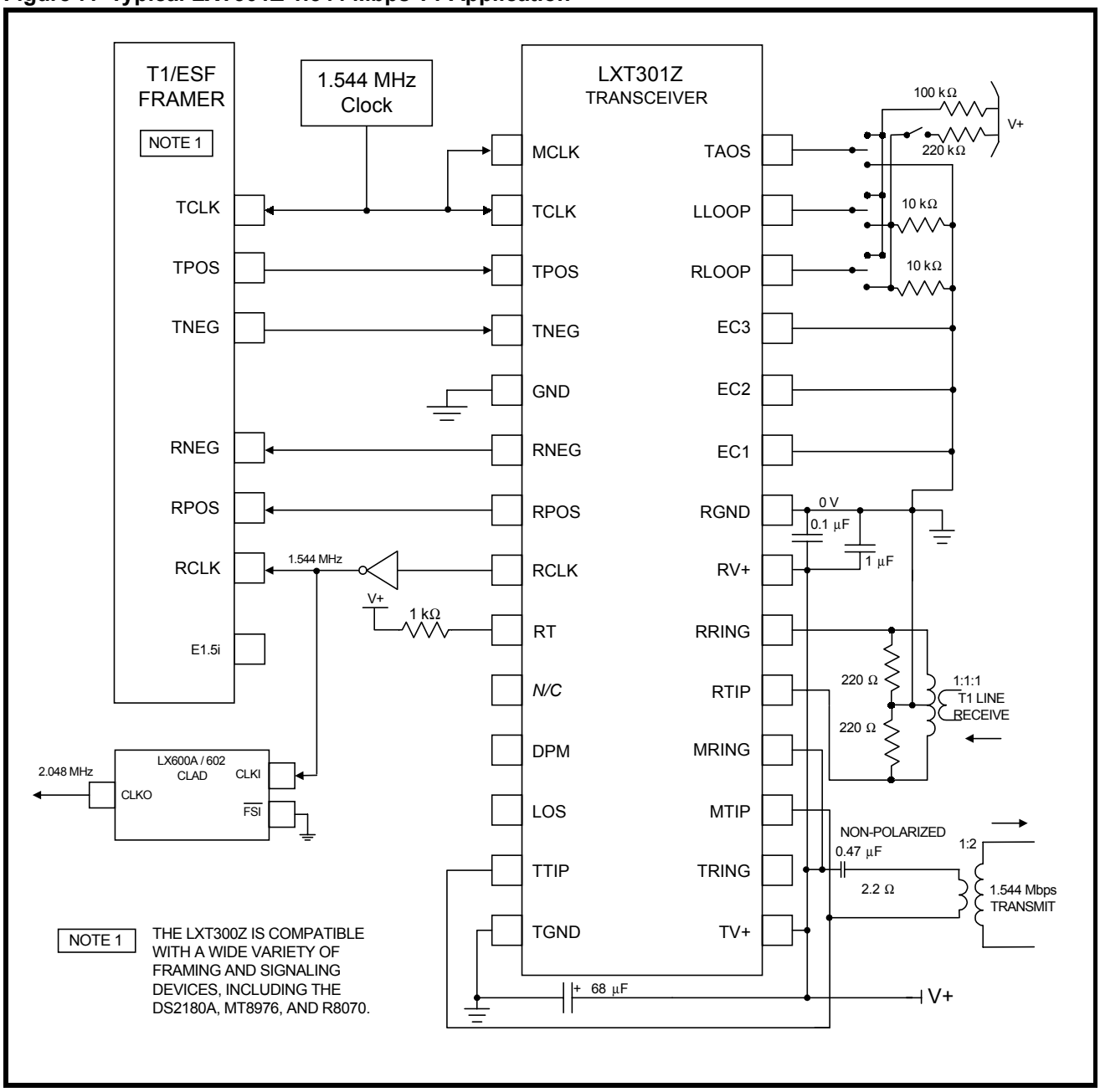
Table 5: LXT300Z Crystal Specifications (External)

Parameter	T1	E1
Frequency	6.176 MHz	8.192 MHz
Frequency stability	± 20 ppm @ 25 °C ± 25 ppm from -40 °C to 85 °C (Ref 25 °C reading)	± 20 ppm @ 25 °C ± 25 ppm from -40 °C to +85 °C (Ref 25 °C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm	CL = 11 pF to 18.7 pF, +ΔF = 95 to 115 ppm CL = 18.7 pF to 34 pF, -ΔF = 95 to 115 ppm
Effective series resistance	40 Ω Maximum	30 Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical	HC49 (R3W),C_O = 7 pF maximum C_M = 17 fF typical

LXT301Z 1.544 Mbps T1 Interface Application

Figure 7 is a typical 1.544 Mbps T1 application of the LXT301Z. The LXT301Z is shown with a typical T1/ESF framer. An LXP600A Clock Adapter (CLAD) provides the 2.048 MHz system backplane clock, locked to the recovered 1.544 MHz clock signal. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (68 µF on the transmit side, 1.0 µF and 0.1 µF on the receive side).

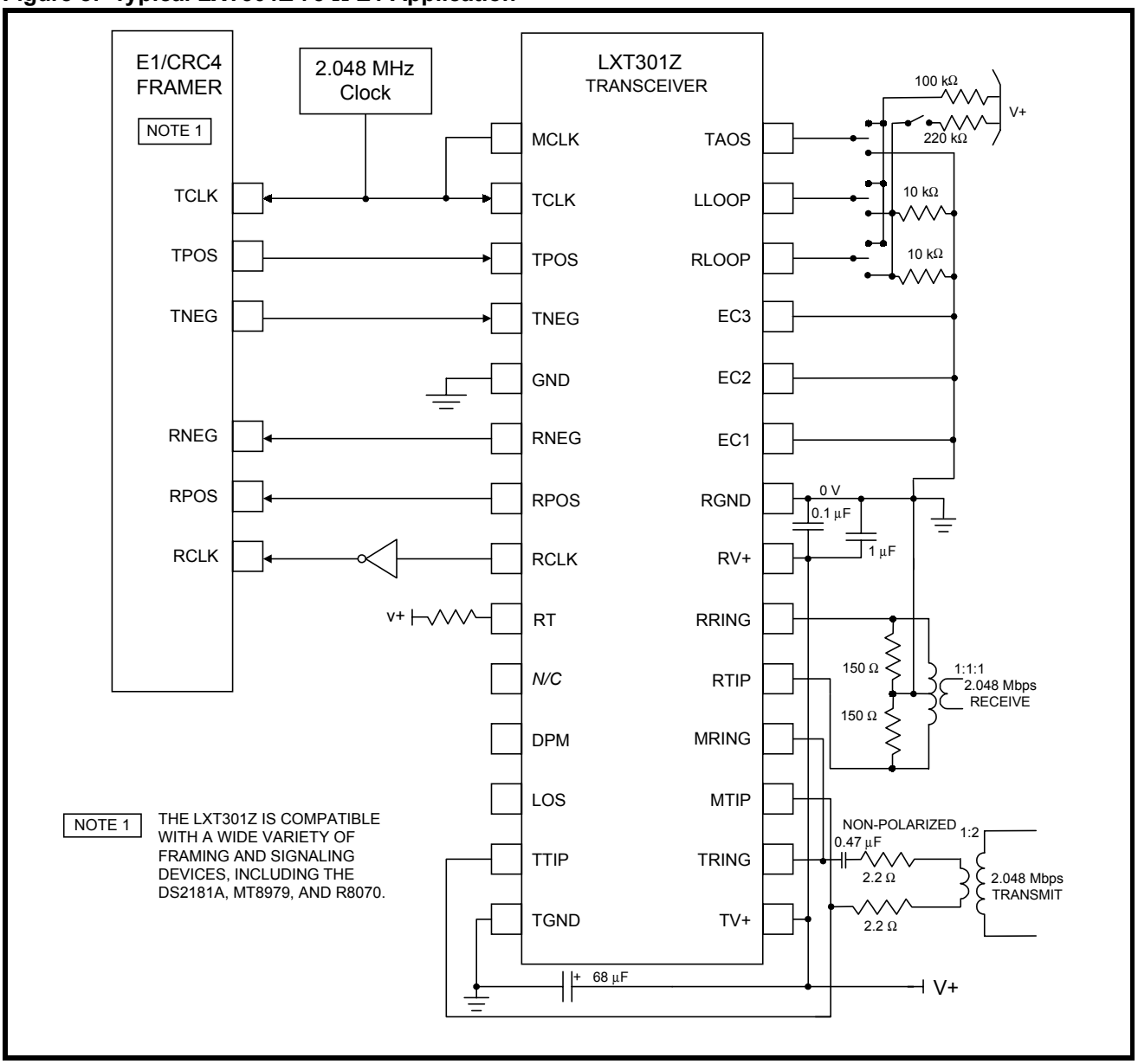
Figure 7: Typical LXT301Z 1.544 Mbps T1 Application



LXT301Z 2.048 Mbps E1 Interface Application

Figure 8 is a typical 2.048 Mbps E1 application of the LXT301Z. The LXT301Z is shown with a typical E1/CRC4 framer. Resistors are installed in line with the transmit transformer for loading a 75 Ω coaxial cable. The in-line resistors are not required for transmission on 120 Ω shielded twisted-pair lines. As in the T1 application Figure 7, this configuration is illustrated with a single power supply bus. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function.

Figure 8: Typical LXT301Z 75 Ω E1 Application



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 6 through 13 and Figures 11 through 15 represent the performance specifications of the LXT300Z/LXT301Z and are guaranteed by test, except where noted by design.

Table 6: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	RV+, TV+	-0.3	6.0	V
Input voltage, any pin[1]	V_{IN}	RGND - 0.3	RV+ + 0.3	V
Input current, any pin[2]	I_{IN}	-10	10	mA
Storage temperature	T_{STG}	-65	150	°C

CAUTION

Operations at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

1. Excluding RTIP and RRING which must stay between -6V and (RV+ + 0.3) V.
2. Transient currents of up to 100 mA will not cause SCR latch up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

Table 7: Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
DC supply[1]	RV+, TV+	4.75	5.0	5.25	V
Ambient operating temperature	T_A	-40	25	85	° C

1. TV+ must not exceed RV+ by more than 0.3 V.

Table 8: Electrical Characteristics (Under Recommended Operating Conditions)

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
High level input voltage[1,2] (pins 1-5, 10, 23-28)	V_{IH}	2.0	–	–	V	
Low level input voltage[1,2] (pins 1-5, 10, 23-28)	V_{IL}	–	–	0.8	V	
High level output voltage[1,2](pins 6-8, 11, 12, 23, 25)	V_{OH}	2.4	–	–	V	I_{OUT} = -400 µA
Low level output voltage[1,2] (pins 6-8, 11, 12, 23, 25)	V_{OL}	–	–	0.4	V	I_{OUT} = 1.6 mA
Input leakage current (pins 1-5, and 23-28)	I_{LL}	-10	–	+10	µA	
Input leakage current (pins 9, 17, and 18)	I_{LL}	-50	–	+50	µA	
Three-state leakage current[1] (pin 25)	I_{3L}	-10	–	+10	µA	
Total power dissipation[3]	P_D	–	–	700	mW	100% ones density & maximum line length @ 5.25 V

1. Functionality of pins 23 and 25 depends on mode. See Host/Hardware Mode descriptions.
2. Output drivers will output CMOS logic levels into CMOS loads.
3. Power dissipation while driving a 25 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

Table 9: Analog Characteristics (Under Recommended Operating Conditions)

Parameter		Min	Typ[1]	Max	Units	Test Conditions
AMI output pulse amplitudes	DSX-1	2.4	3.0	3.6	V	measured at the DSX
	E1 (120 Ω)	2.7	3.0	3.3	V	measured at line side
	E1 (75 Ω)	2.14	2.37	2.6	V	@ 772 kHz
Transmit amplitude variation with supply			1	2.5	%	
Recommended output load at TTIP and TRING		–	25	–	Ω	RTIP to RRING
Driver output impedance[2]		–	3	10	Ω	@ 10 kHz
Jitter added by the transmitter[3]	10 Hz - 8 kHz[2]	–	–	0.01	UI	
	8 kHz - 40 kHz	–	–	0.025	UI	
	10 Hz - 40 kHz	–	–	0.025	UI	
	Broad Band	–	–	0.05	UI	
Output power levels[2] DS1 2 kHz BW	@ 772 kHz	12.6	–	17.9	dB**m**	
	@ 1544 kHz[5]	-29.0	–	–	dB	
Positive to negative pulse imbalance		–	–	0.5	dB	
Sensitivity below DSX[6] (0 dB = 2.4 V)		13.6	–	–	dB	
		500	–	–	mV	
Receiver input impedance		–	40	–	kΩ	
Loss of Signal threshold		–	0.3	–	V	
Data decision threshold	DSX-1	63	70	77	% peak	
	E1	43	50	57	% peak	
Allowable consecutive zeros before LOS		160	175	190	–	
Input jitter tolerance	10 Hz	–	1200	–	UI	
	775 Hz	14	–	–	UI	
	10 kHz - 100 kHz	0.4	–	–	UI	
Jitter attenuation curve corner frequency[4]		–	3	–	Hz	
Jitter attenuation		–	50	–	db	
Jitter attenuation tolerance before FIFO Overflow[2]		28	–	–	UI	

1. Typical values are measured at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Not production tested but guaranteed by design and other correlation methods.
3. Input signal to TCLK is jitter-free.
4. Circuit attenuates jitter at 20 dB/decade above the corner frequency.
5. Referenced to power in 2 kHz band.
6. With a maximum of 6 dB of cable attenuation.

Figure 9: LXT300Z Rx Jitter Tolerance (Typical)

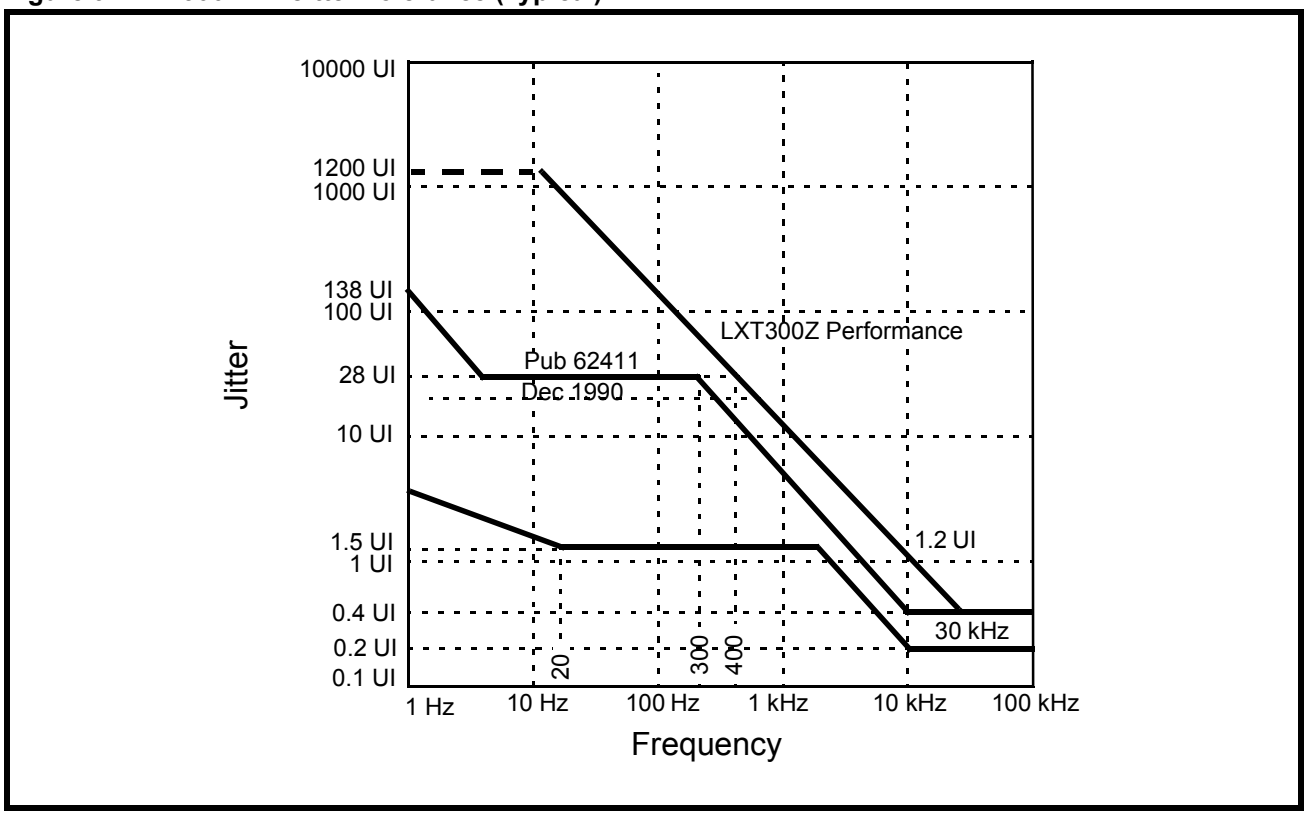


Figure 10: LXT300Z Rx Jitter Transfer Performance (Typical)

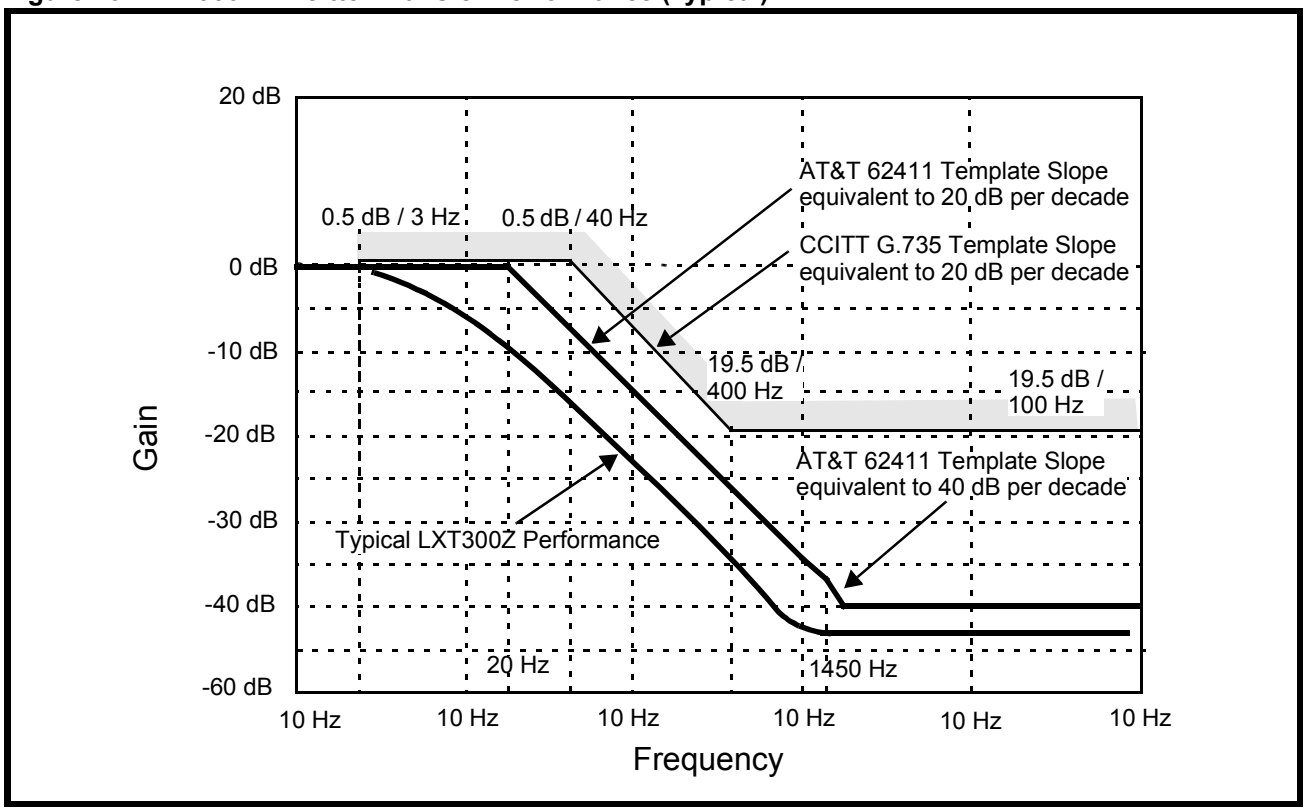


Table 10: **LXT300Z Receiver Timing Characteristics** (See Figure 11)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Receive clock duty cycle		RCLKd	40	-	60	%	
Receive clock pulse width[2]	DSX-1	t_{PW}	–	324	–	ns	
	E1	t_{PW}	–	244	–	ns	
RPOS/RNEG to RCLK rising setup time	DSX-1	t_{SUR}	–	274	–	ns	
	E1	t_{SUR}	–	194	–	ns	
RCLK rising to RPOS/RNEG hold time	DSX-1	t_{HR}	–	274	–	ns	
	E1	t_{HR}	–	194	–	ns	

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 11: LXT300Z Receive Clock Timing Diagram

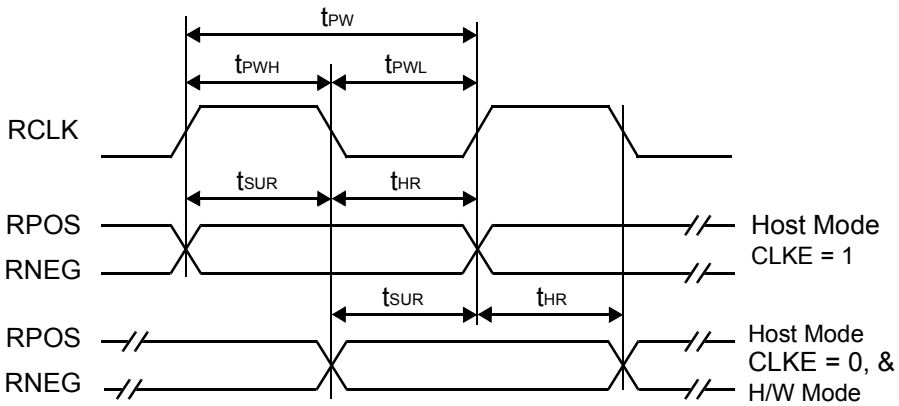


Table 11: LXT301Z Receive Timing Characteristics (See Figure 12)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Receive clock duty cycle[2]	DSX-1	RCLKd	40	50	60	%	
	E1	RCLKd	40	50	60	%	
Receive clock pulse width[2]	DSX-1	t_{PW}	594	648	702	ns	
	E1	t_{PW}	447	488	529	ns	
Receive clock pulse width high	DSX-1	t_{PWH}	–	324	–	ns	
	E1	t_{PWH}	–	244	–	ns	
Receive clock pulse width low	DSX-1	t_{PWL}	270	324	378	ns	
	E1	t_{PWL}	203	244	285	ns	
RPOS/RNEG to RCLK rising setup time	DSX-1	t_{SUR}	50	270	–	ns	
	E1	t_{SUR}	50	203	–	ns	
RCLK rising to RPOS/RNEG hold time	DSX-1	t_{HR}	50	270	–	ns	
	E1	t_{HR}	50	203	–	ns	

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.544 MHz, 0.2 UI clock displacement for 2.048 MHz).

Figure 12: LXT301Z Receive Clock Timing Diagram

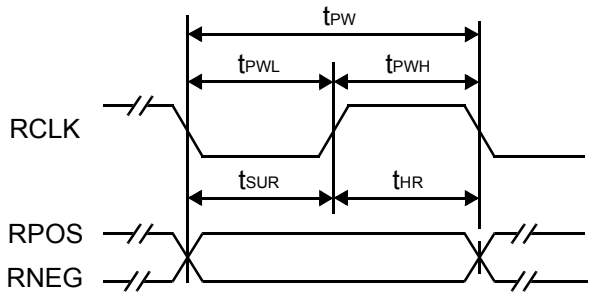


Table 12: LXT300Z/301Z Master Clock and Transmit Timing Characteristics (See Figure 13)

Parameter		Sym	Min	Typ[1]	Max	Units
Master clock frequency	DSX-1	MCLK	–	1.544	–	MHz
	E1	MCLK	–	2.048	–	MHz
Master clock tolerance		MCLKt	–	±100	–	ppm
Master clock duty cycle		MCLKd	40	–	60	%
Crystal frequency *(LXT300Z only)*	DSX-1	fc	–	6.176	–	MHz
	E1	fc	–	8.192	–	MHz
Transmit clock frequency	DSX-1	TCLK	–	1.544	–	MHz
	E1	TCLK	–	2.048	–	MHz
Transmit clock tolerance		TCLKt	–	±50	–	ppm
Transmit clock duty cycle		TCLKd	10	–	90	%
TPOS/TNEG to TCLK setup time		t_{SUT}	25	–	–	ns
TCLK to TPOS/TNEG hold time		t_{HT}	25	–	–	ns

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Not production tested but guaranteed by design and other correlation methods.

Figure 13: LXT300Z/301Z Transmit Clock Timing Diagram

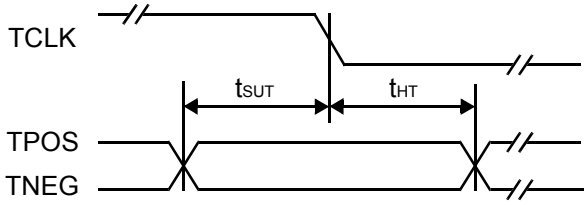


Table 13: LXT300Z Serial I/O Timing Characteristics (See Figures 14 and 15)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	t_{RF}	–	–	100	ns	Load 1.6 mA, 50 pF
SDI to SCLK setup time	t_{DC}	50	–	–	ns	
SCLK to SDI hold time	t_{CDH}	50	–	–	ns	
SCLK low time	t_{CL}	240	–	–	ns	
SCLK high time	t_{CH}	240	–	–	ns	
SCLK rise and fall time	t_R, t_F	–	–	50	ns	
$\overline{CS}$ to SCLK setup time	t_{CC}	50	–	–	ns	
SCLK to $\overline{CS}$ hold time	t_{CCH}	50	–	–	ns	
$\overline{CS}$ inactive time	t_{CWH}	250	–	–	ns	
SCLK to SDO valid	t_{CDV}	–	–	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high Z	t_{CDZ}	–	100	–	ns	

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 14: LXT300Z Serial Data Input Timing Diagram

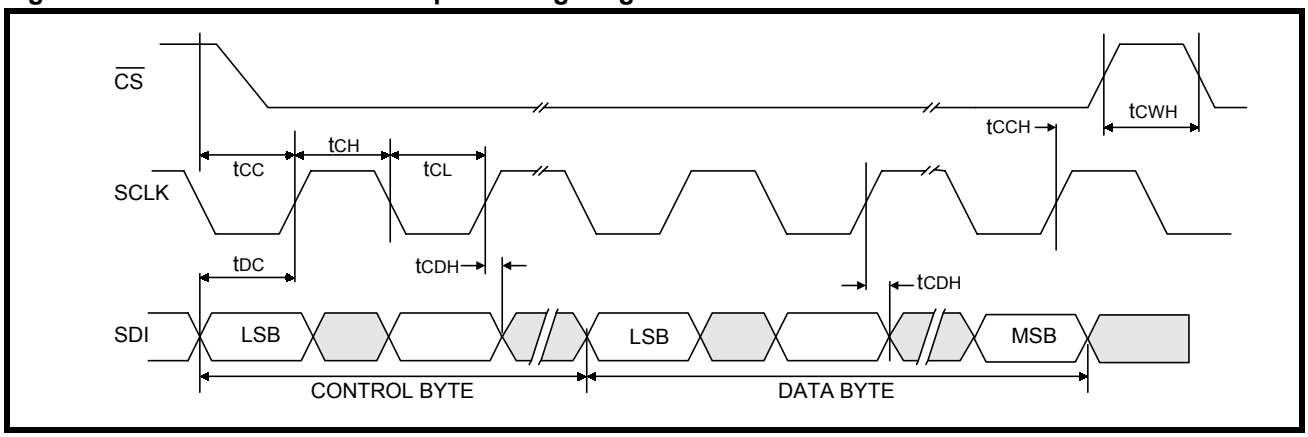


Figure 15: LXT300Z Serial Data Output Timing Diagram

