LX5255

9-Line LVD SCSI Terminator

PRODUCTION DATA SHEET

DESCRIPTION

The LX5255 is a Low Voltage Differential (LVD) terminator designed to comply with the LVD termination specification in the SPI-4 document. The LX5255 is specifically designed for LVD only applications. Because the LX5255 supports only LVD, it has lower output capacitance than multimode terminators such as the LX5250.

The LX5255 utilizes an industry standard LVD architecture. The individual high bandwidth drivers maximize channel separation, reduce channel-to-channel noise and cross talk to insure Ultra320 performance.

When the LX5255 is enabled, the Differential Sense (DIFSENS) pin supplies a voltage between 1.2V and 1.4V. In application, the terminator DIFFB input is connected to the system DIFSENS line. If there are no single ended or High Voltage Differential (HVD) devices attached to the system, the LVD output will be enabled. If the DIFSENS line is LOW, indicating a single ended device, the LX5255 output will be HiZ. If the DIFSENS line is HIGH, indicating a HVD device, the LX5255 output will be HiZ.

The LX5255 has a TTL compatible sleep/disable mode. Applying a logic HIGH to the DISC pin puts the LX5255 in sleep mode. During sleep mode, power dissipation is reduced to a meager 5µA while also placing all outputs and the DIFSENS function in a HiZ state.

KEY FEATURES

- Compliant with SPI-2 (Ultra2), SPI-3 (Ultra160), and SPI-4 (Ultra320)
- 2.5pF Maximum Disabled Output Capacitance
- Fast Response, No External Capacitors Required
- 5µA Supply Current in Disconnect Mode
- 30mA Supply During Normal Operation
- Logic Command Disconnects All Termination Lines
- DIFSENS Line Driver
- Current Limit and Thermal Protection
- Pin Compatible With Unitrode UCC5640

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

TYPICAL APPLICATION



LX5255 Typical Application

PACKAGE ORDER INFO

T_A (°C)	PW Plastic TSSOP 24-Pin RoHS Compliant / Pb-free Transition DC: 0442
0 to 70	**LX5255CPW**

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX5255CPW-TR)

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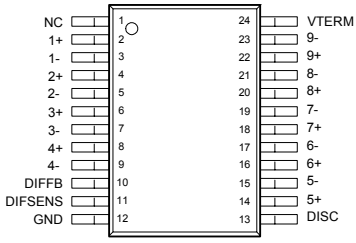
LX5255

ABSOLUTE MAXIMUM RATINGS

Term Power (V_{TERM}).....-0.3V to 7V
Signal Line Voltage.....-0.3V to 7V
Differential Voltage.....-0.3V to 7V
Operating Junction Temperature..... 150°C
Storage Temperature Range.....-65°C to 150°C
Peak Package Solder Reflow Temperature (40 second maximum exposure) . 260°C (+0, -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

PACKAGE PIN OUT



PW PACKAGE
(Top View)
NC – No Internal Connection

RoHS / Pb-free 100% Matte Tin Lead Finish

THERMAL DATA

PW **24L TSSOP**

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	100°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow. θ_{JA} can vary significantly depending on mounting technique. (See Application Notes Section: Thermal considerations)

DIFFB/POWER UP/POWER DOWN FUNCTION TABLE

DISC	DIFFB	Outputs		Quiescent Current
		Status	Type	
L	L < 0.5V	Disable	HI-Z	8mA
L	0.7V to 1.9V	Enable	LVD	30mA
L	H > 2.4V	Disable	HI-Z	8mA
H or Open	X	Disable	HI-Z	10µA

RECOMMENDED MAX OPERATING CONDITIONS

Parameter	Symbol	LX5255			Units
		Min	Typ	Max	
VTerm	V_{TERM}	2.7		5.25	V
Signal Line Voltage		0		5.0	V
Disconnect Input Voltage		0		V_{TERM}	V
Operating Junction Temperature	T_J	0		70	°C

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature 0°C ≤ T_A ≤ 70°C, VTerm = 3.3V, and DISCONNECT = 0V.

Parameter	Symbol	Test Conditions	LX5255 Min	LX5255 Typ	LX5255 Max	Units
LVD Terminator Section						
VTerm Supply Current	I_{CC}	All term lines open		30	35	mA
		DISCONNECT > 2.0V		5	20	µA
Common Mode Voltage	V_{CM}		1.125	1.25	1.375	V
Offset Voltage (Note 1)	V_{OS}	Open circuit between (-) and (+) terminals	100	112	125	mV
Differential Terminator Impedance	Z_D	V_{OUT} Differential = -1V to +1V	100	105	110	Ω
Common Mode Impedance	Z_{CM}	0.5V to 2V	110	150	190	Ω
Output Capacitance (Note 2)	C_O	DISCONNECT > 2.0V			3	pF
Mode Change Delay	t_{DF}	DIFSENS = 1.4V to 0V	100	115	300	ms
DIFSENS Section						
DIFSENS Output Voltage	V_{DIFF}		1.2	1.3	1.4	V
DIFSENS Output Source Current	I_{DIFF}	DIFSENS = 0V	5		15	mA
DIFSENS Sink Current	$I_{SINK(DIFF)}$	V_{TERM} = 2.75V	20		200	µA
Disconnect Section						
Disconnect Threshold	V_{TH}		0.8		2.0	V
Input Current	I_{IH}	DISCONNECT = 0V			10	µA

Note 1: Open Circuit failsafe voltage.
Note 2: Guaranteed by design.

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BLOCK DIAGRAM

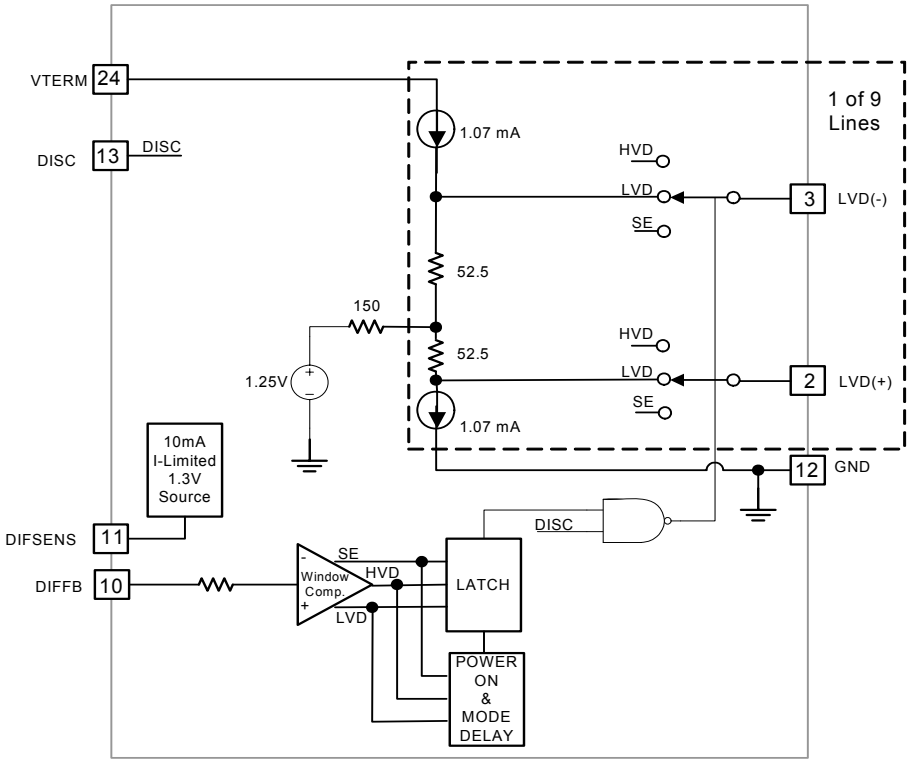


Figure 1 – LX5255CPW Block Diagram

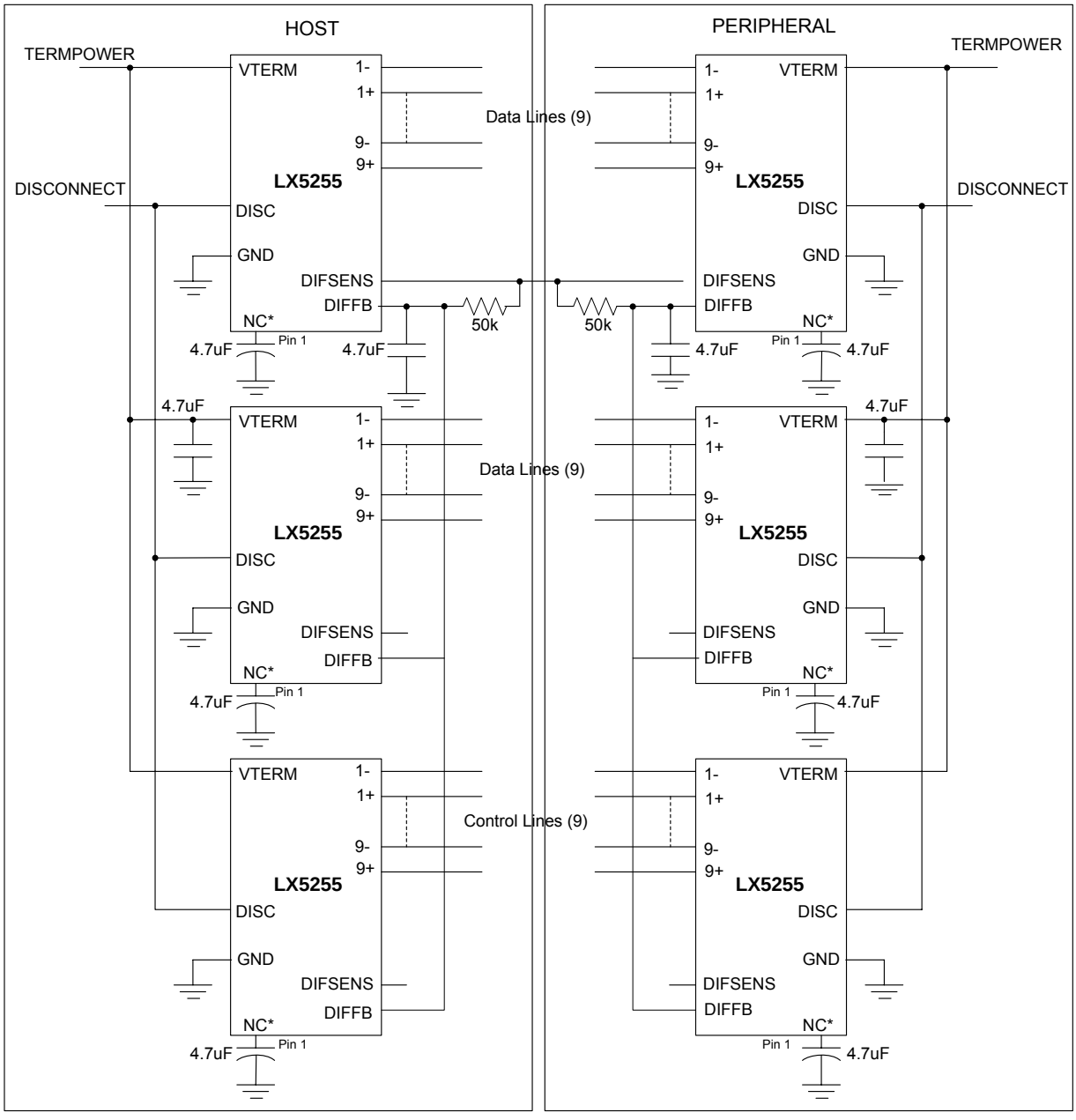
FUNCTIONAL PIN DESCRIPTION

PIN NAME	DESCRIPTION
1-, 2-, 3-, 4-, 5-, 6-, 7-, 8-, 9-	Negative signal termination lines for LVD mode.
1+, 2+, 3+, 4+, 5+, 6+, 7+, 8+, 9+	Positive signal termination lines for LVD mode.
V_{TERM}	Power supply pin for terminator. Connect to SCSI bus VTERM. Must be decoupled by one 4.7µF low-ESR capacitor for every three terminator devices. It is absolutely necessary to connect this pin to the decoupling capacitor through a very low impedance (big traces to PCB). Keeping distances very short from the decoupling capacitors is somewhat layout dependent and some applications may benefit from high frequency decoupling with 0.1µF capacitors at V_{TERM} pin.
DISC	Enables/Disables terminator. See Power Down Function Table for logic levels.
GND	Terminator ground pin. Connect to ground.
DIFSENS	Differential sense pin connected to system DIFFSENS line. Drives the SCSI bus DIFSENS line to 1.3V.
DIFFB	Used to detect the SCSI bus mode (SE, LVD or HVD). Should be connected to a 4.7uF capacitor to GND, and a 50KΩ resistor to the DIFFSENS pin (see Figure 2 on page 5).

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APPLICATION



* The capacitor on Pin 1 can be placed on the LX5255PCW to be pin compatible with other devices. This capacitor is not required.

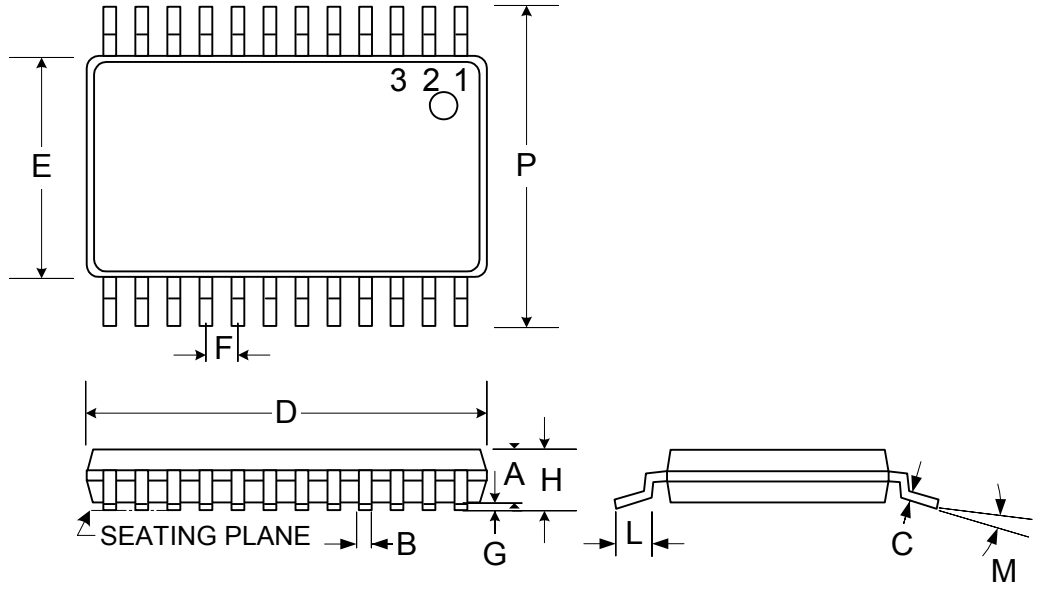
Figure 2 – Suggested Microsemi LX5255 Universal Application Schematic

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MECHANICAL DRAWINGS

PW 24-Pin Thin Small Shrink Outline (TSSOP)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.85	0.95	0.033	0.037
B	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	7.70	7.90	0.303	0.311
E	4.30	4.50	0.169	0.177
F	0.65 BSC		0.025 BSC	
G	0.05	0.15	0.002	0.005
H	–	1.10	–	.0433
L	0.50	0.75	0.020	0.030
M	0°	8°	0°	8°
P	6.25	6.55	0.246	0.256
*LC	–	0.10	–	0.004

* Lead Coplanarity

Note:
1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

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