

LVC and LV ***Low-Voltage CMOS Logic***

Data Book

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INTRODUCTION

The Texas Instruments (TI™) low-voltage logic families provide a variety of devices for users transitioning from 5-V to 3.3-V logic. LVC and LV, both low-voltage CMOS logic families, are just two of TI's wide range of 3.3-V logic solutions.

LVC is TI's answer to designers' 3.3-V *price/performance* needs. With 5-V *tolerance*[†], typical propagation delays of 3.8 ns (*maximum t_{pd} of 6.3 ns*), and 24-mA *output drive* current, LVC is the low-voltage solution that designers often need. With almost 60 devices available and more planned, LVC gives designers the options they need to maximize bus-interface performance.

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LVC and LV are supported in a wide variety of packages, including SOIC, SSOP, TSSOP, and TVSOP. See the specific device data sheets for packaging options.

With a wide range of devices, benchmark service, support, and delivery, TI is the number 1 supplier of standard low-voltage logic worldwide.

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For a complete listing of all TI logic products, please order our Logic Selection Guide (literature number SDYU001) by calling our literature response center at 1-800-477-8924.

[†] All LVC devices in this data book are 5-V tolerant on the inputs. The bidirectional octals and Widebus™ devices are also 5-V tolerant on the outputs.

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

operating conditions and characteristics (in sequence by letter symbols)

C_i	Input capacitance The internal capacitance at an input of the device
C_{io}	Input/output capacitance Input-to-output internal capacitance; transcapacitance
C_o	Output capacitance The internal capacitance at an output of the device
C_{pd}	Power dissipation capacitance Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$
f_{max}	Maximum clock frequency The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification
I_{CC}	Supply current The current into* the V _{CC} supply terminal of an integrated circuit
ΔI_{CC}	Supply current change The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V _{CC}
I_{CEX}	Output high leakage current The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition V _O = 5.5 V
I_{I(hold)}	Input hold current Input current that holds the input at the previous state when the driving device goes to a high-impedance state
I_{IH}	High-level input current The current into* an input when a high-level voltage is applied to that input
I_{IL}	Low-level input current The current into* an input when a low-level voltage is applied to that input
I_{off}	Input/output power-off leakage current The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and V _{CC} = 0 V
I_{OH}	High-level output current The current into* an output with input conditions applied that, according to the product specification, establishes a high level at the output

*Current out of a terminal is given as a negative value.

GLOSSARY

SYMBOLS, TERMS, AND DEFINITIONS

I_{OL}	Low-level output current The current into* an output with input conditions applied that, according to the product specification, establishes a low level at the output
I_{OZ}	Off-state (high-impedance-state) output current (of a 3-state output) I_{OZ} The current that flows through the output gates when the device is in the high-impedance state I_{OZPU} The current that flows into or out of the output stage when the device is being powered up from the high-impedance state I_{OZPD} The current that flows into or out of the output stage when the device is being powered down from the high-impedance state
t_a	Access time The time interval between the application of a specified input pulse and the availability of valid signals at an output
t_c	Clock cycle time Clock cycle time is $1/f_{max}$.
t_{dis}	Disable time (of a 3-state or open-collector output) The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ} . Open-collector outputs change only if they are low at the time of disabling, so $t_{dis} = t_{PLH}$.
t_{en}	Enable time (of a 3-state or open-collector output) The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low) NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{OE}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL} . Open-collector outputs change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHL}$.
t_h	Hold time The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected. 2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.
t_{pd}	Propagation delay time The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or t_{PLH})
t_{PHL}	Propagation delay time, high-to-low level output The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

*Current out of a terminal is given as a negative value.

t_{PHZ}	Disable time (of a 3-state output) from high level The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state
t_{PLH}	Propagation delay time, low-to-high level output The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level
t_{PLZ}	Disable time (of a 3-state output) from low level The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state
t_{PZH}	Enable time (of a 3-state output) to high level The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level
t_{PZL}	Enable time (of a 3-state output) to low level The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level
t_{sk(o)}	Output skew The difference between any two propagation delay times when a single switching input or multiple inputs switching simultaneously cause multiple outputs to switch, as observed across all switching output. This parameter is used to describe the fanout capability of a clock driver and is of concern when making decisions on clock buffering and distribution networks.
t_{su}	Setup time The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected. 2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is to be expected.
t_w	Pulse duration (width) The time interval between specified reference points on the leading and trailing edges of the pulse waveform
Δt/Δv	Input voltage transition rate The input transition rise or fall rate corresponding to the change in signal amplitude with time
Δt/ΔV_{CC}	Power supply power-up rate The power-up ramp rate corresponds to the transition rate of the supply voltage when the device is being powered up.
V_{IH}	High-level input voltage An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

GLOSSARY SYMBOLS, TERMS, AND DEFINITIONS

V_{IL} Low-level input voltage

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{OH} High-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a high level at the output

V_{OL} Low-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a low level at the output

V_{IT+} Positive-going input threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{IT-}

V_{IT-} Negative-going input threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{IT+}

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . . h	=	the level of steady-state inputs A through H, respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
	=	one high-level pulse
	=	one low-level pulse
Toggle	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0 , or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse,  or , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

EXPLANATION OF FUNCTION TABLES

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register.

FUNCTION TABLE													
INPUTS									OUTPUTS				
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	H	H	H	H	H	QAn	QBn	QCn
H	L	H	↑	X	L	L	L	L	L	L	QAn	QBn	QCn
H	H	L	↑	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	↑	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs occurs while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A is at output Q_A, data entered at B is at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D, respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

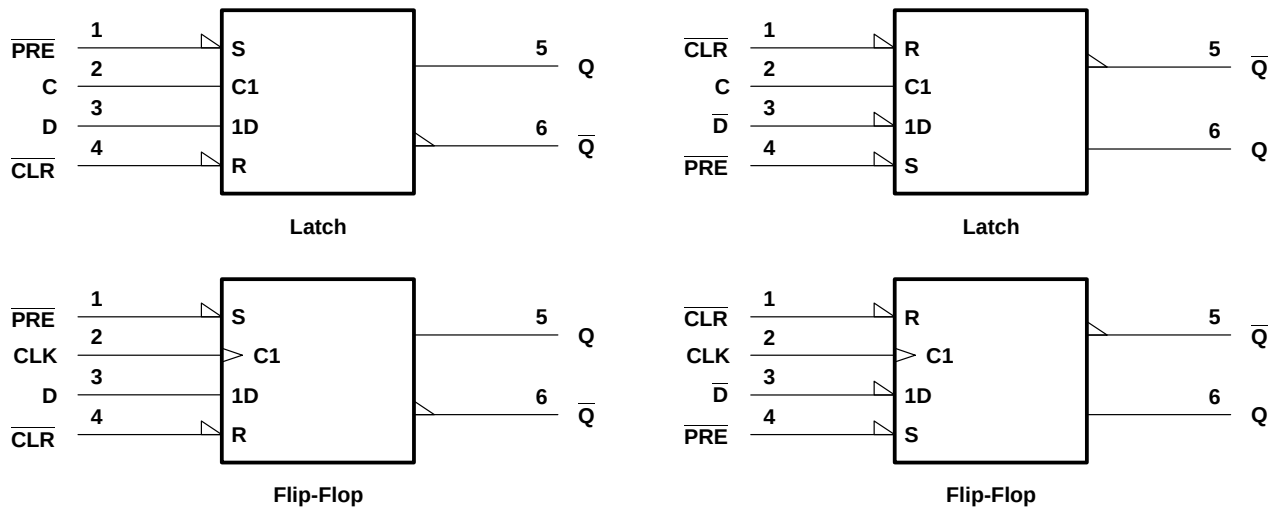
The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

The function table functional tests do not reflect all possible combinations or sequential modes.

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\bar{Q}$. An input that causes a Q output to go high or a $\bar{Q}$ output to go low is called preset (PRE). An input that causes a $\bar{Q}$ output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names ($\overline{\text{PRE}}$ and $\overline{\text{CLR}}$) if they are active low.

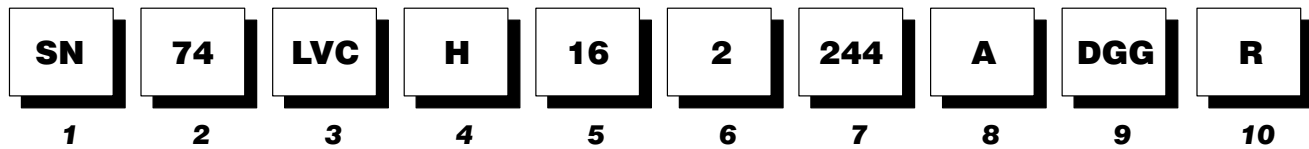
The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\bar{D}$ and $\bar{Q}$.

In some applications, it may be advantageous to redesignate the data input from D to $\bar{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and $\bar{Q}$ exchange names, the preset and clear pins also exchange names. The polarity indicators ($\triangle$) on $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or $\bar{D}$), Q, and $\bar{Q}$. Pin 5 (Q or $\bar{Q}$) is still in phase with the data input (D or $\bar{D}$); their active levels change together.

Example:



1 Standard Prefix

Example: SNJ – Conforms to MIL-PRF-38535 (QML)

2 Temperature Range

Examples: 54 – Military
74 – Commercial

3 Family

Examples: Blank – Transistor-Transistor Logic
ABT – Advanced BiCMOS Technology
ABTE – Advanced BiCMOS Technology/
Enhanced Transceiver Logic
AC/ACT – Advanced CMOS Logic
AHC/AHCT – Advanced High-Speed CMOS Logic
ALB – Advanced Low-Voltage BiCMOS
ALS – Advanced Low-Power Schottky Logic
ALVC – Advanced Low-Voltage CMOS Technology
AS – Advanced Schottky Logic
BCT – BiCMOS Bus-Interface Technology
CBT – Crossbar Technology
CBTLV – Low-Voltage Crossbar Technology
F – F Logic
FB – Backplane Transceiver Logic/Futurebus+
GTL – Gunning Transceiver Logic
HC/HCT – High-Speed CMOS Logic
HSTL – High-Speed Transceiver Logic
LS – Low-Power Schottky Logic
LV – Low-Voltage CMOS Technology
LVC – Low-Voltage CMOS Technology
LVT – Low-Voltage BiCMOS Technology
S – Schottky Logic
SSTL – Stub Series-Terminated Logic

4 Special Features

Examples: Blank = No Special Features
D – Level-Shifting Diode (CBTD)
H – Bus Hold (ALVCH)
R – Damping Resistor on Inputs/Outputs (LVCR)
S – Schottky Clamping Diode (CBTS)

5 Bit Width

Examples: Blank = Gates, MSI, and Octals
1G – Single Gate
8 – Octal IEEE 1149.1 (JTAG)
16 – Widebus™ (16, 18, and 20 bit)
18 – Widebus IEEE 1149.1 (JTAG)
32 – Widebus+™ (32 and 36 bit)

6 Options

Examples: Blank = No Options
2 – Series-Damping Resistor on Outputs
4 – Level Shifter
25 – 25-Ω Line Driver

7 Function

Examples: 244 – Noninverting Buffer/Driver
374 – D-Type Flip-Flop
573 – D-Type Transparent Latch
640 – Inverting Transceiver

8 Device Revision

Examples: Blank = No Revision
Letter Designator A–Z

9 Packages

Examples: D, DW – Small-Outline Integrated Circuit (SOIC)
DB, DL – Shrink Small-Outline Package (SSOP)
DBB, DGV – Thin Very Small-Outline Package (TVSOP)
DBQ – Quarter-Size Outline Package (QSOP)
DBV, DCK – Small-Outline Transistor Package (SOT)
DGG, PW – Thin Shrink Small-Outline Package (TSSOP)
FK – Leadless Ceramic Chip Carrier (LCCC)
FN – Plastic Leaded Chip Carrier (PLCC)
GB – Ceramic Pin Grid Array (CPGA)
HFP, HS, HT, HV – Ceramic Quad Flat Package (CQFP)
J, JT – Ceramic Dual-In-Line Package (CDIP)
N, NP, NT – Plastic Dual-In-Line Package (PDIP)
PAG, PAH, PCA, PCB, PM, PN, PZ –
Thin Quad Flat Package (TQFP)
PH, PQ, RC – Quad Flat Package (QFP)
W, WA, WD – Ceramic Flat Package (CFP)

10 Tape and Reel

All new or changed devices in the DB and PW package types include the R designation for reeled product. Existing products designated as LE presently maintain that designation, but will be converted to R in the future.

Nomenclature Examples:

For an Existing Device – SN74LVTxxxDBLE

For a New or Changed Device – SN74LVTxxxADBR

LE – Left Embossed (valid for DB and PW packages only)

R – Standard (valid for all surface-mount packages except existing DB and PW devices)

There is no difference between LE and R designated products, with respect to the carrier tape, cover tape, or reels used.

NOTIFICATION OF PACKAGE NOMENCLATURE ALIAS (for Standard Linear and Logic device names of greater than 18 characters)

TI is converting from its current order-entry system to a more advanced system. This conversion requires modifications, both internal and external, to TI's current business processes. This new system will ultimately provide significant improvements to all facets of TI's business – from production, to order entry, to logistics. One change required is a limitation of TI part numbers to no more than 18 characters in length. Based on customer inputs, Standard Linear and Logic determined the least disruptive implementations as outlined below:

1. Package alias

TI will use a package alias to denote specific package types for devices currently exceeding 18 characters in length. Table 1 shows a mapping of package codes to an alias single-character representation.

Table 1

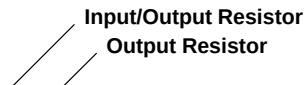
CURRENT PACKAGE CODE	ALIAS
DL	L
DGG/DBB	G
DGV	V
DLR	LR – tape/reel packing
DGGR/DBBR	GR – tape/reel packing
DGVR	VR – tape/reel packing

Current: SN74 ALVCH 162269A DGGR

New: SN74 ALVCH 162269A GR

2. Resistor-option nomenclature

For devices greater than 18 characters with input and output resistors, TI will adopt a simplified nomenclature to designate the resistor option. This will eliminate the redundant 2 (designating output resistors) when the part number also contains an R (designating input/output resistors).



Current: SN74 ALVCH R 16 2 245 A

New: SN74 ALVCH R 16 245 A

There is no change to the device or data-sheet electrical parameters. The packages involved and the changes in nomenclature are noted in Table 1.

These nomenclature changes are being gradually implemented. The first customer-visible conversions for TI logic devices will be made to data sheets. Over the next few months, TI logic data sheets will be updated. Please note that these changes in device nomenclature in no way reflect a change in device performance or process characteristics.

General Information	1
LVC Gates and MSI	2
LVC Octals	3
LVC Widebus™	4
LVC 3.3-V to 5-V Translators and Cable Drivers	5
LV Gates and MSI	6
LV Octals	7
Application Reports	8
Mechanical Data	9

Contents			Page
SN54LVC00A	SN74LVC00A	Quadruple 2-Input Positive-NAND Gates	2-3
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SN54LVC04A	SN74LVC04A	Hex Inverters	2-19
	SN74LVCU04A	Hex Inverter	2-27
SN54LVC06A	SN74LVC06A	Hex Inverter Buffers/Drivers With Open-Drain Outputs	2-35
SN54LVC07A	SN74LVC07A	Hex Buffers/Drivers With Open-Drain Outputs	2-43
SN54LVC08A	SN74LVC08A	Quadruple 2-Input Positive-AND Gates	2-51
	SN74LVC10A	Triple 3-Input Positive-NAND Gate	2-59
SN54LVC14A	SN74LVC14A	Hex Schmitt-Trigger Inverters	2-67
SN54LVC32A	SN74LVC32A	Quadruple 2-Input Positive-OR Gates	2-75
SN54LVC74A	SN74LVC74A	Dual Positive-Edge-Triggered D-Type Flip-Flops With Clear and Preset	2-83
SN54LVC86A	SN74LVC86A	Quadruple 2-Input Exclusive-OR Gates	2-91
	SN74LVC112A	Dual Negative-Edge-Triggered J-K Flip-Flop With Clear and Preset	2-99
	SN74LVC125A	Quadruple Bus Buffer Gate With 3-State Outputs	2-107
	SN74LVC126A	Quadruple Bus Buffer Gate With 3-State Outputs	2-115
	SN74LVC137A	3-Line to 8-Line Decoder/Demultiplexer With Address Latches	2-123
SN54LVC138A	SN74LVC138A	3-Line to 8-Line Decoders/Demultiplexers	2-131
	SN74LVC139A	Dual 2-Line to 4-Line Decoder/Demultiplexer	2-139
	SN74LVC157A	Quadruple 2-Line to 1-Line Data Selector/Multiplexer	2-147
	SN74LVC158A	Quadruple 2-Line to 1-Line Data Selector/Multiplexer	2-155
	SN74LVC257A	Quadruple 2-Line to 1-Line Data Selector/Multiplexer With 3-State Outputs	2-163
	SN74LVC258A	Quadruple 2-Line to 1-Line Data Selector/Multiplexer With 3-State Outputs	2-171

SN54LVC00A, SN74LVC00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and DIPs (J)

description

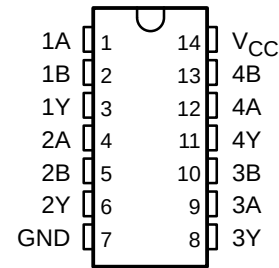
The SN54LVC00A quadruple 2-input positive-NAND gate is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC00A quadruple 2-input positive-NAND gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The 'LVC00A devices perform the Boolean function $Y = A \bullet B$ or $Y = \overline{A + B}$ in positive logic.

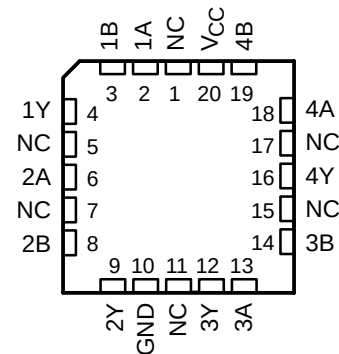
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC00A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC00A is characterized for operation from -40°C to 85°C .

SN54LVC00A ... J OR W PACKAGE
SN74LVC00A ... D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LVC00A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



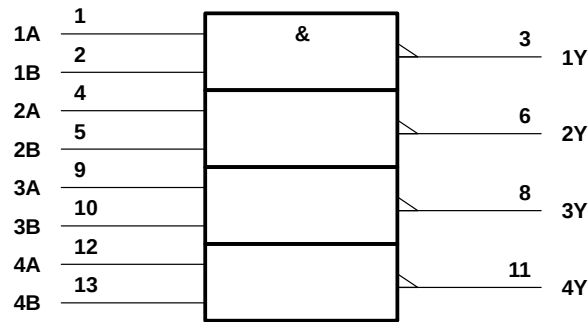
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVC00A, SN74LVC00A
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, PW, and W packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LVC00A, SN74LVC00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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recommended operating conditions (see Note 4)

			SN54LVC00A		SN74LVC00A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			0.7		
		V _{CC} = 2.7 V to 3.6 V		0.8	0.8		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V			–4		mA
		V _{CC} = 2.3 V			–8		
		V _{CC} = 2.7 V		–12	–12		
		V _{CC} = 3 V		–24	–24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V			4		mA
		V _{CC} = 2.3 V			8		
		V _{CC} = 2.7 V		12	12		
		V _{CC} = 3 V		24	24		
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVC00A, SN74LVC00A

QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC00A			SN74LVC00A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V				V _{CC} –0.2			V
		2.7 V to 3.6 V	V _{CC} –0.2						
	I _{OH} = –4 mA	1.65 V				1.2			
	I _{OH} = –8 mA	2.3 V				1.7			
	I _{OH} = –12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
	I _{OH} = –24 mA	3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.2			V
		2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA	1.65 V				0.45			
	I _{OL} = 8 mA	2.3 V				0.7			
	I _{OL} = 12 mA	2.7 V	0.4			0.4			
	I _{OL} = 24 mA	3 V	0.55			0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			10			μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND	3.3 V	5			5			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC00A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	5.1		1	4.3	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC00A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	‡	‡	‡	‡	5.1		1	4.3	ns
t _{sk(o)} [§]									1		ns

‡ This information was not available at the time of publication.

§ Skew between any two outputs of the same package switching in the same direction



SN54LVC00A, SN74LVC00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

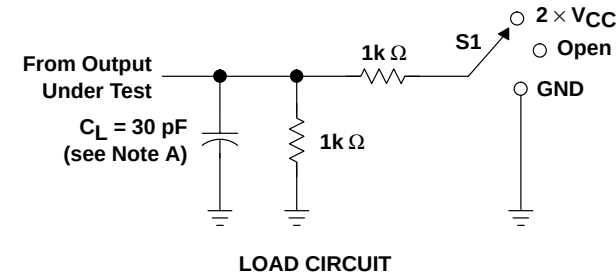
SCAS279G – JANUARY 1993 – REVISED JUNE 1998

operating characteristics, $T_A = 25^\circ\text{C}$

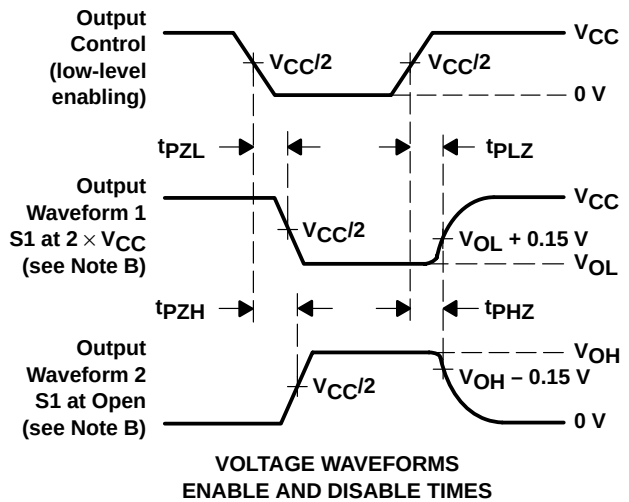
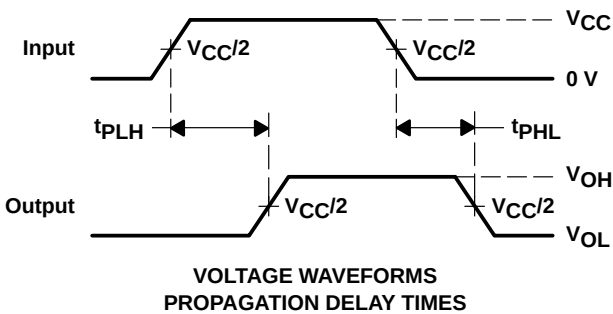
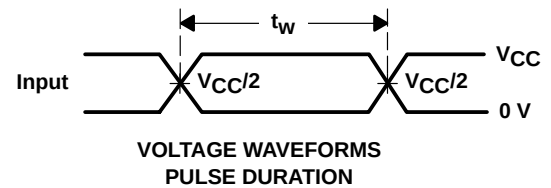
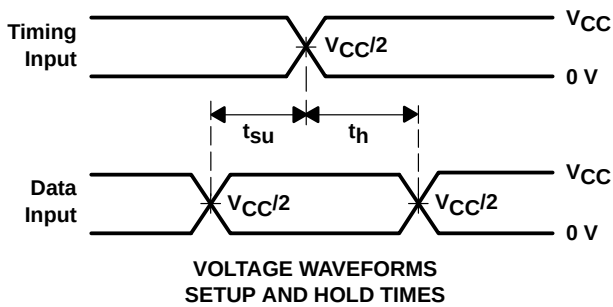
PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
		TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per gate	$f = 10\text{ MHz}$	†	†	9.5	pF

† This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZH}	$2 \times V_{CC}$
t_{PHZ}/t_{PHZ}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

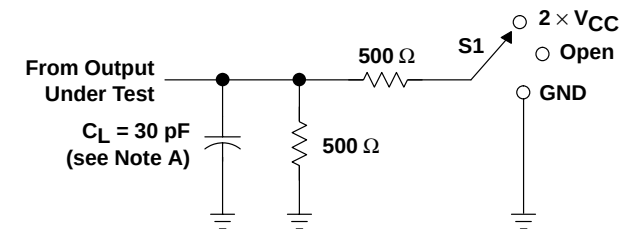


SN54LVC00A, SN74LVC00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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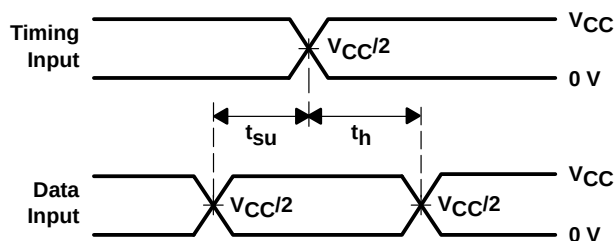
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

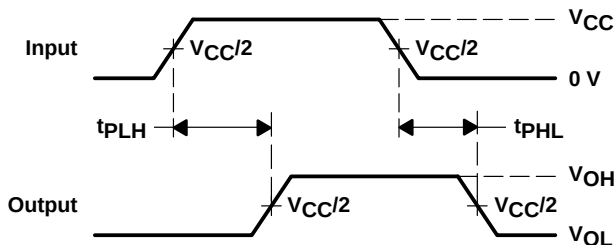


LOAD CIRCUIT

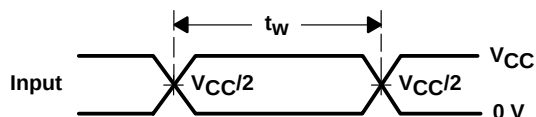
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



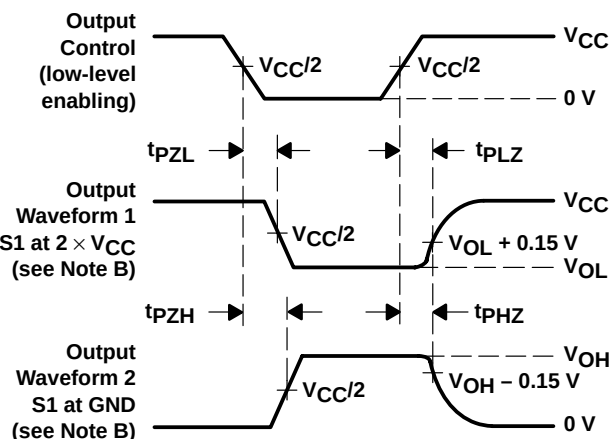
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



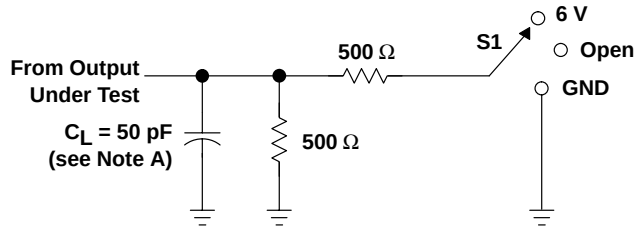
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

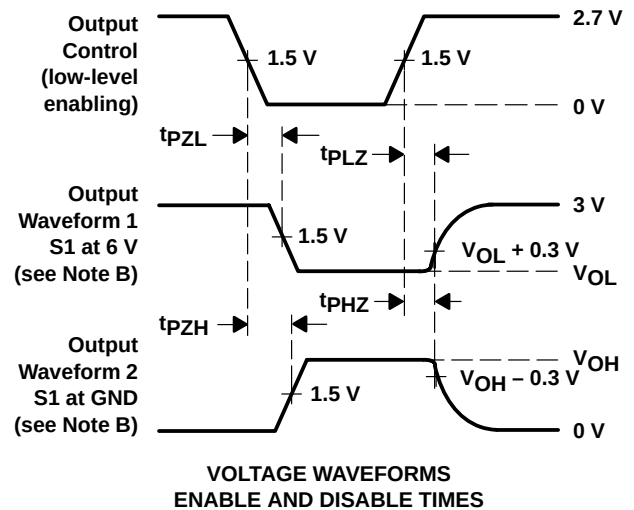
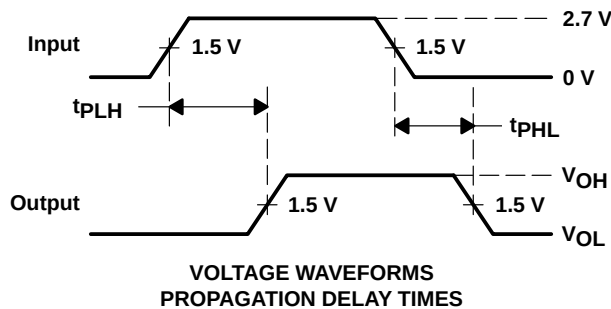
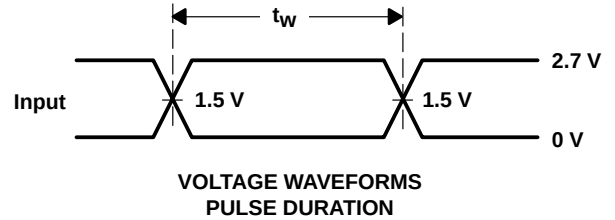
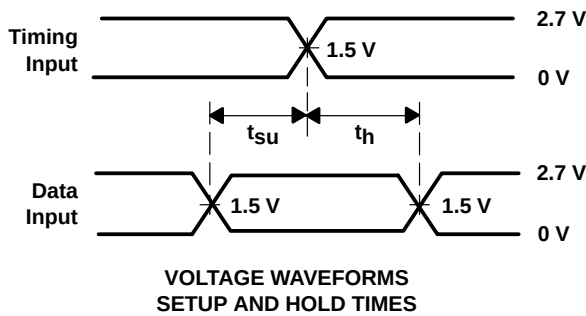
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC02A, SN74LVC02A QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCAS280H – JANUARY 1993 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W), Chip Carriers (FK), and DIPs (J)

description

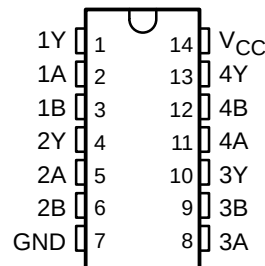
The SN54LVC02A quadruple 2-input positive-NOR gate is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC02A quadruple 2-input positive-NOR gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The 'LVC02A devices perform the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

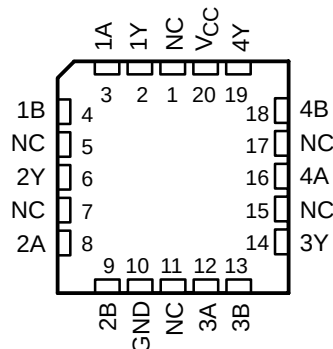
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC02A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC02A is characterized for operation from -40°C to 85°C .

SN54LVC02A ... J OR W PACKAGE
SN74LVC02A ... D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LVC02A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

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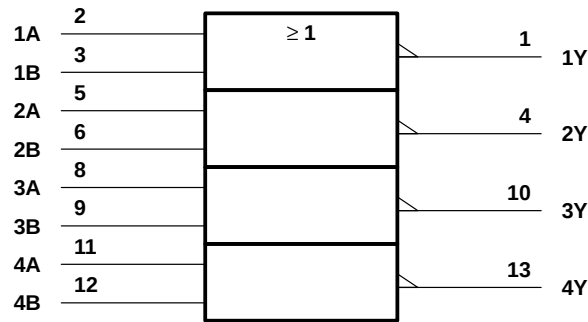
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVC02A, SN74LVC02A
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCAS280H – JANUARY 1993 – REVISED JUNE 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, PW, and W packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply-voltage range, V_{CC}	–0.5 V to 6.5 V
Input-voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output-voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LVC02A, SN74LVC02A QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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recommended operating conditions (see Note 4)

			SN54LVC02A		SN74LVC02A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			0.7		
		V _{CC} = 2.7 V to 3.6 V		0.8	0.8		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V			–4		mA
		V _{CC} = 2.3 V			–8		
		V _{CC} = 2.7 V		–12	–12		
		V _{CC} = 3 V		–24	–24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V			4		mA
		V _{CC} = 2.3 V			8		
		V _{CC} = 2.7 V		12	12		
		V _{CC} = 3 V		24	24		
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVC02A, SN74LVC02A

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC02A		SN74LVC02A		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V			V _{CC} –0.2		V	
		2.7 V to 3.6 V	V _{CC} –0.2					
	I _{OH} = –4 mA	1.65 V			1.2			
	I _{OH} = –8 mA	2.3 V			1.7			
	I _{OH} = –12 mA	2.7 V	2.2			2.2		
		3 V	2.4			2.4		
I _{OH} = –24 mA	3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2		V	
		2.7 V to 3.6 V	0.2					
	I _{OL} = 4 mA	1.65 V			0.45			
	I _{OL} = 8 mA	2.3 V			0.7			
	I _{OL} = 12 mA	2.7 V	0.4		0.4			
	I _{OL} = 24 mA	3 V	0.55		0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5		±5		μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10		10		μA	
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500		500		μA	
C _i	V _I = V _{CC} or GND	3.3 V	5		5		pF	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC02A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	5.4		1	4.4	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC02A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	‡	‡	‡	‡	5.4		1	4.4	ns
t _{sk(0)} [§]									1		ns

‡ This information was not available at the time of publication.

§ Skew between any two outputs of the same package switching in the same direction



SN54LVC02A, SN74LVC02A QUADRUPLE 2-INPUT POSITIVE-NOR GATES

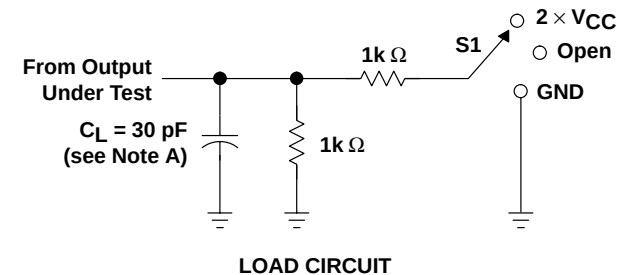
SCAS280H – JANUARY 1993 – REVISED JUNE 1998

operating characteristics, $T_A = 25^\circ\text{C}$

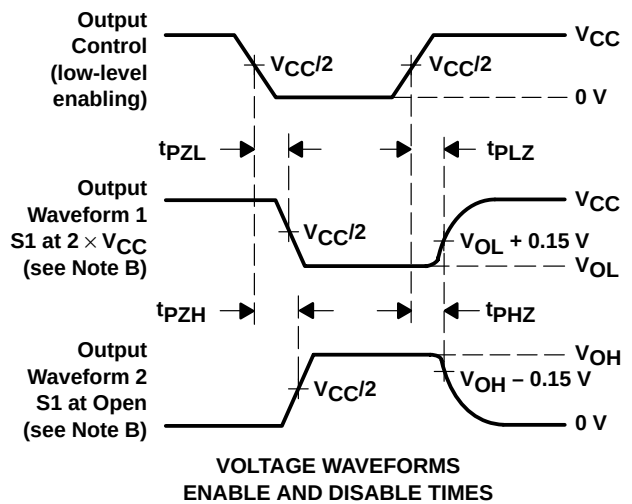
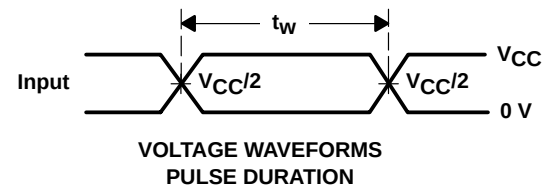
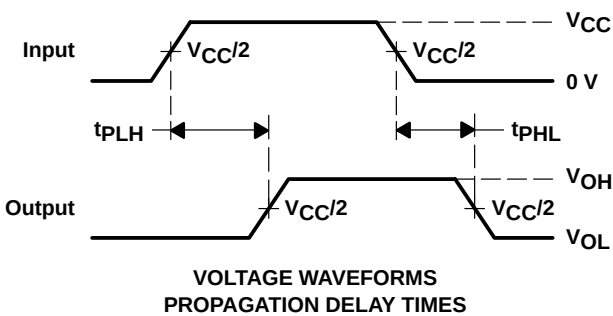
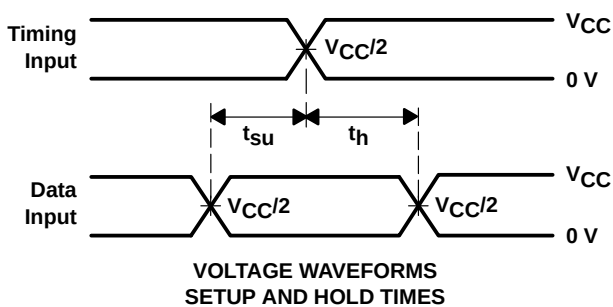
PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
		TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per gate	$f = 10\text{ MHz}$	†	†	9.5	pF

† This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	Open



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

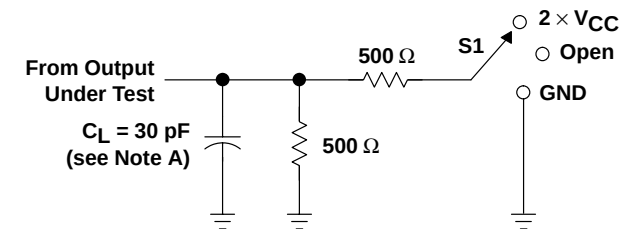


SN54LVC02A, SN74LVC02A QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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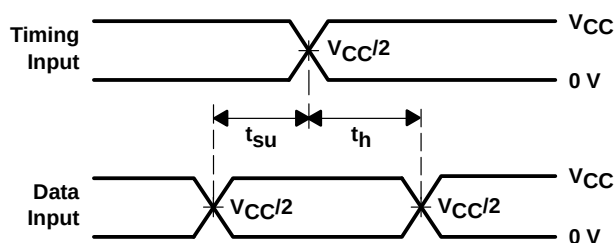
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

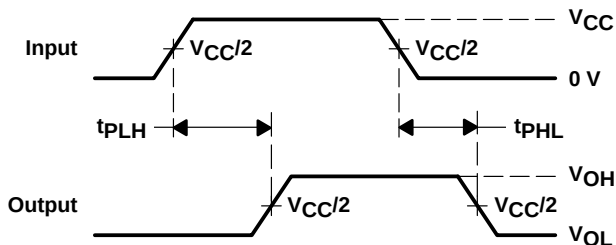


LOAD CIRCUIT

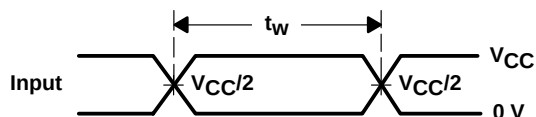
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



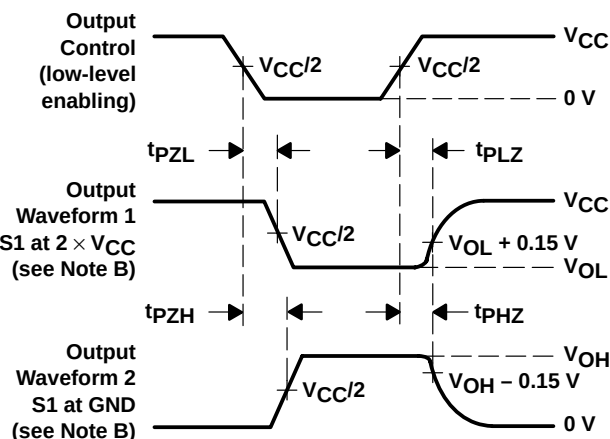
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



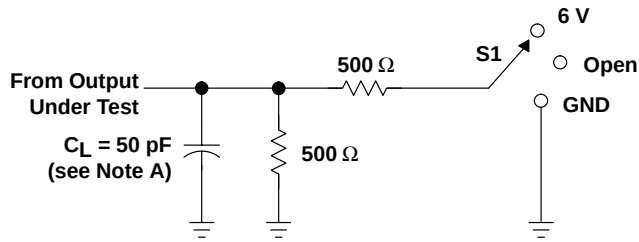
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

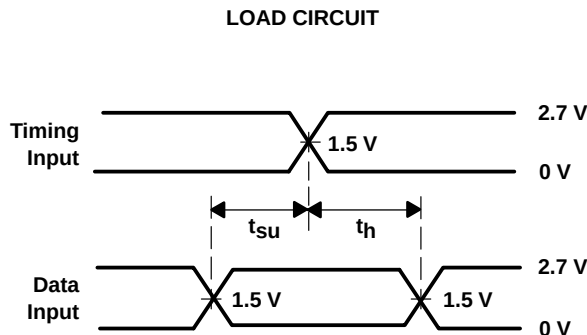
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V}$ AND $3.3 \text{ V} \pm 0.3 \text{ V}$

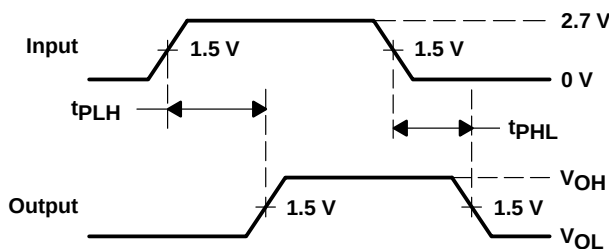


LOAD CIRCUIT

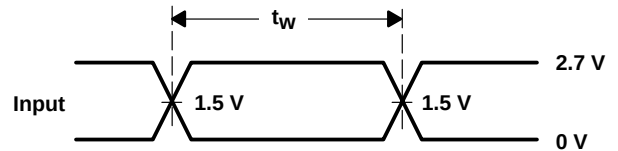
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



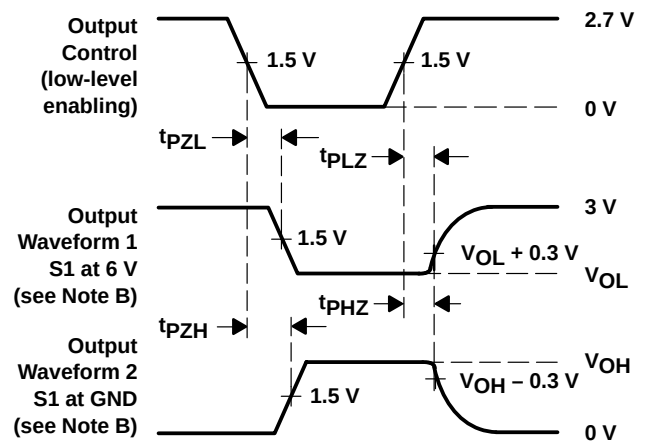
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC04A, SN74LVC04A HEX INVERTERS

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- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Inputs Accept Voltages to 5.5 V**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, and Ceramic Chip Carriers (FK)**

description

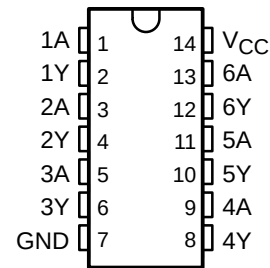
The SN54LVC04A hex inverter contains six independent inverters designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC04A hex inverter contains six independent inverters designed for 1.65-V to 3.6-V V_{CC} operation.

The 'LVC04A devices perform the Boolean function $Y = \overline{A}$.

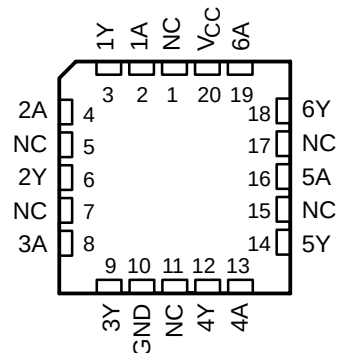
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC04A is characterized for operation over the full military temperature range from -55°C to 125°C . The SN74LVC04A is characterized for operation from -40°C to 85°C .

SN54LVC04A ... J OR W PACKAGE
SN74LVC04A ... D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LVC04A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



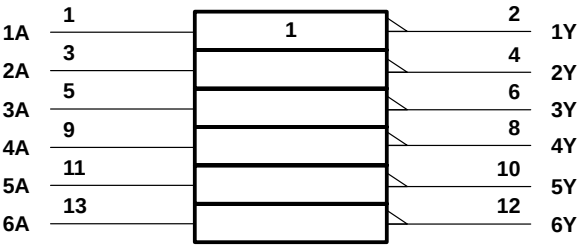
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

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SN54LVC04A, SN74LVC04A
HEX INVERTERS

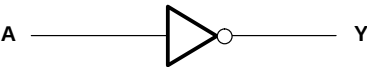
SCAS281H – JANUARY 1993 – REVISED JUNE 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, PW, and W packages.

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LVC04A, SN74LVC04A HEX INVERTERS

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recommended operating conditions (see Note 4)

			SN54LVC04A		SN74LVC04A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			0.7		
		V _{CC} = 2.7 V to 3.6 V		0.8	0.8		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V			–4		mA
		V _{CC} = 2.3 V			–8		
		V _{CC} = 2.7 V		–12	–12		
		V _{CC} = 3 V		–24	–24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V			4		mA
		V _{CC} = 2.3 V			8		
		V _{CC} = 2.7 V		12	12		
		V _{CC} = 3 V		24	24		
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVC04A, SN74LVC04A HEX INVERTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC04A			SN74LVC04A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V				V _{CC} –0.2			V
		2.7 V to 3.6 V	V _{CC} –0.2						
	I _{OH} = –4 mA	1.65 V				1.2			
	I _{OH} = –8 mA	2.3 V				1.7			
	I _{OH} = –12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
	I _{OH} = –24 mA	3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.2			V
		2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA	1.65 V				0.45			
	I _{OL} = 8 mA	2.3 V				0.7			
	I _{OL} = 12 mA	2.7 V	0.4			0.4			
	I _{OL} = 24 mA	3 V	0.55			0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			10			μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND	3.3 V	5			5			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC04A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A	Y	5.5		0.5	4.5	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC04A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	‡	‡	‡	‡	5.5		1	4.5	ns
t _{sk(o)} [§]									1		ns

‡ This information was not available at the time of publication.

§ Skew between any two outputs of the same package switching in the same direction

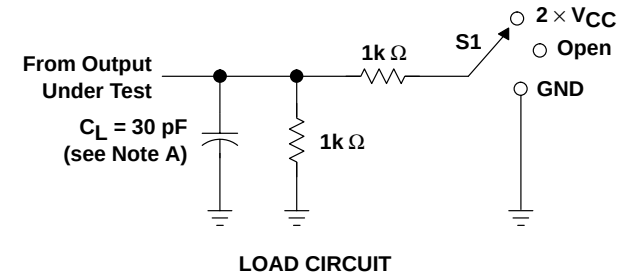


operating characteristics, $T_A = 25^\circ\text{C}$

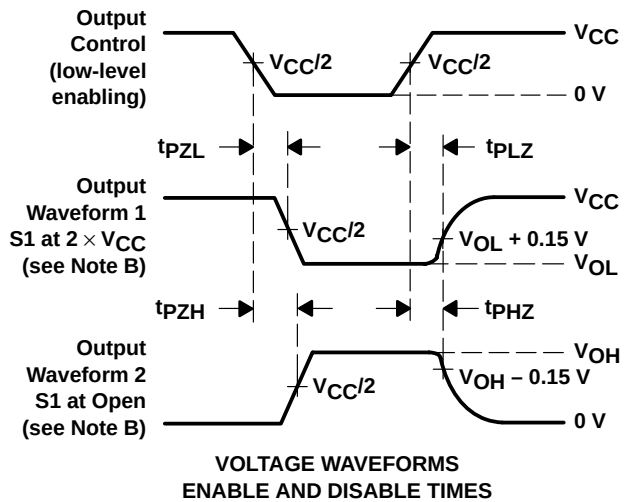
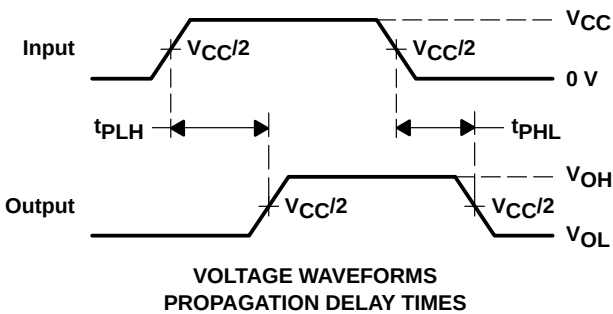
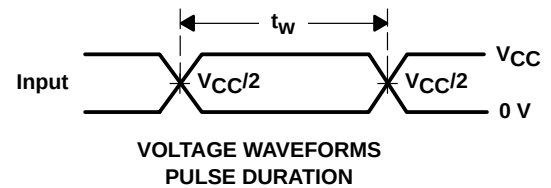
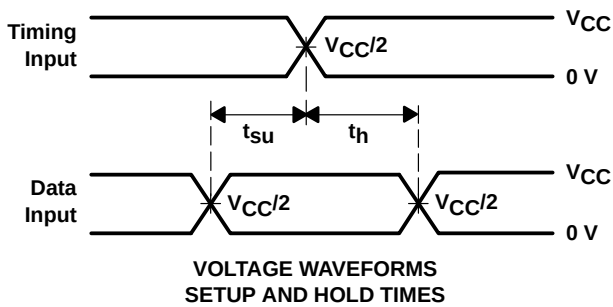
PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
		TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per inverter	$f = 10\text{ MHz}$	†	†	8	pF

† This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZH}	2 × V_{CC}
t_{PHZ}/t_{PHZ}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 0\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZH} and t_{PHZ} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

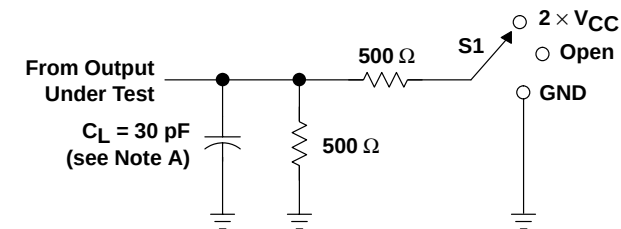
Figure 1. Load Circuit and Voltage Waveforms

SN54LVC04A, SN74LVC04A HEX INVERTERS

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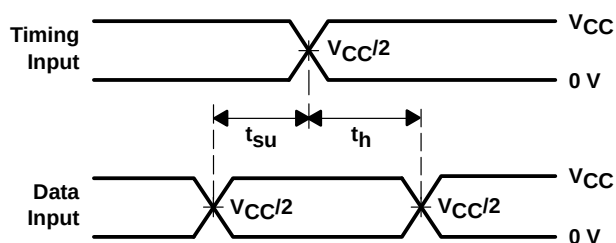
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

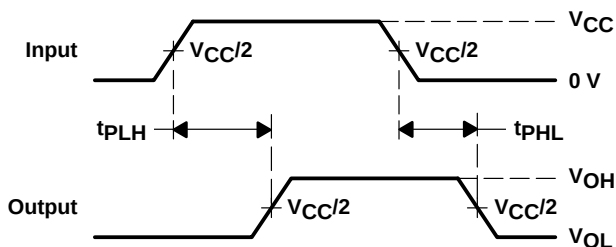


LOAD CIRCUIT

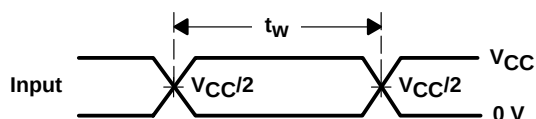
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



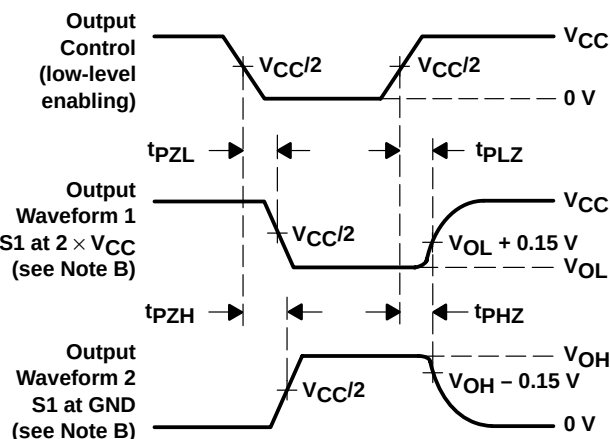
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



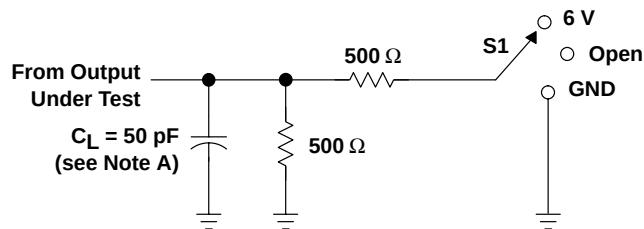
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

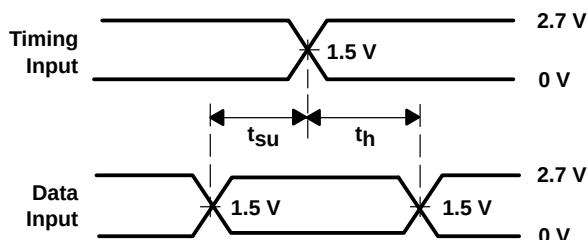
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

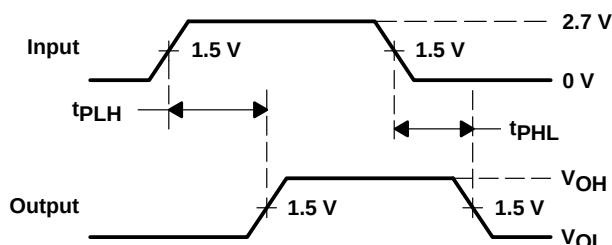


LOAD CIRCUIT

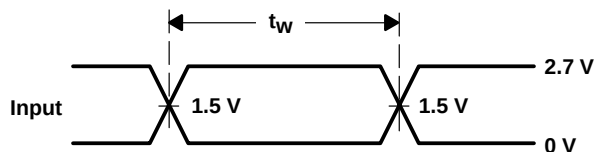
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



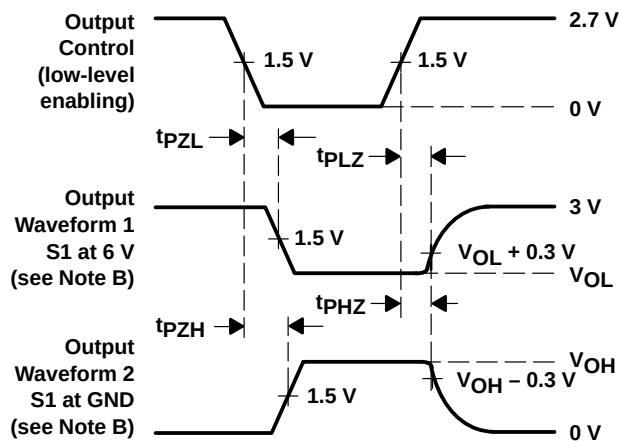
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



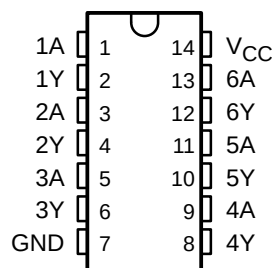
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Inputs Accept Voltages to 5.5 V**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

**D, DB, OR PW PACKAGE
(TOP VIEW)**



description

This hex inverter is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCU04A contains six independent inverters with unbuffered outputs, and performs the Boolean function $Y = \bar{A}$.

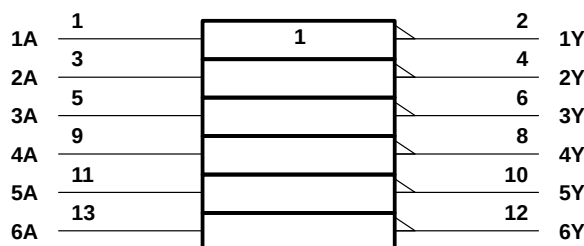
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVCU04A is characterized for operation from -40°C to 85°C .

**FUNCTION TABLE
(each inverter)**

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



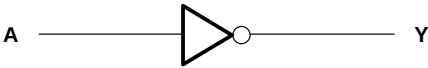
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SN74LVCU04A
HEX INVERTER

SCAS282F – JANUARY 1993 – REVISED JUNE 1998

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	$V_{CC} = 1.65\text{ V}$	1.32		V
		$V_{CC} = 2.3\text{ V}$	1.84		
		$V_{CC} = 2.7\text{ V}$	2.16		
		$V_{CC} = 3\text{ V}$	2.4		
		$V_{CC} = 3.6\text{ V}$	2.88		
V_{IL}	Low-level input voltage	$V_{CC} = 1.65\text{ V}$		0.4	V
		$V_{CC} = 2.3\text{ V}$		0.5	
		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$		0.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65\text{ V}$		–4	mA
		$V_{CC} = 2.3\text{ V}$		–8	
		$V_{CC} = 2.7\text{ V}$		–12	
		$V_{CC} = 3\text{ V}$		–24	
I_{OL}	Low-level output current	$V_{CC} = 1.65\text{ V}$		4	mA
		$V_{CC} = 2.3\text{ V}$		8	
		$V_{CC} = 2.7\text{ V}$		12	
		$V_{CC} = 3\text{ V}$		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP [†]	MAX	UNIT
V_{OH}	$I_{OH} = -100\text{ }\mu\text{A}$	1.65 V to 3.6 V	$V_{CC}-0.2$			V
	$I_{OH} = -4\text{ mA}$, $V_{IL} = 0.4\text{ V}$	1.65 V	1.2			
	$I_{OH} = -8\text{ mA}$, $V_{IL} = 0.5\text{ V}$	2.3 V	1.7			
	$I_{OH} = -12\text{ mA}$, $V_{IL} = 0.65\text{ V}$	2.7 V	2.2			
		3 V	2.4			
	$I_{OH} = -24\text{ mA}$	3 V	2.2			
V_{OL}	$I_{OL} = 100\text{ }\mu\text{A}$	1.65 V to 3.6 V			0.2	V
	$I_{OL} = 4\text{ mA}$, $V_{IH} = 1.32\text{ V}$	1.65 V			0.45	
	$I_{OL} = 8\text{ mA}$, $V_{IH} = 1.84\text{ V}$	2.3 V			0.7	
	$I_{OL} = 12\text{ mA}$, $V_{IH} = 2.16\text{ V}$	2.7 V			0.4	
	$I_{OL} = 24\text{ mA}$, $V_{IH} = 2.4\text{ V}$	3 V			0.55	
I_I	$V_I = 5.5\text{ V or GND}$	3.6 V			±5	μA
I_{CC}	$V_I = V_{CC}\text{ or GND}$, $I_O = 0$	3.6 V			10	μA
ΔI_{CC}	One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$	2.7 V to 3.6 V			500	μA
C_i	$V_I = V_{CC}\text{ or GND}$	3.3 V		5		pF

[†] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

SN74LVCU04A

HEX INVERTER

SCAS282F – JANUARY 1993 – REVISED JUNE 1998

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	†	†	†	†	4.7		1	3.8	ns
t _{sk(o)} ‡									1		ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

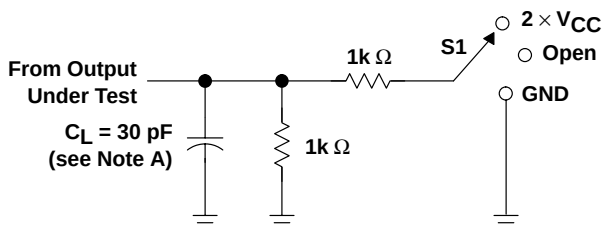
PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
		TYP	TYP	TYP	
C _{pd} Power dissipation capacitance per inverter	f = 10 MHz	†	†	5	pF

† This information was not available at the time of publication.



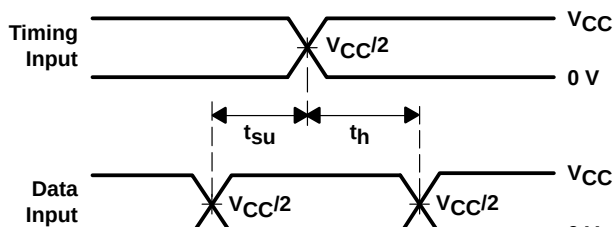
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

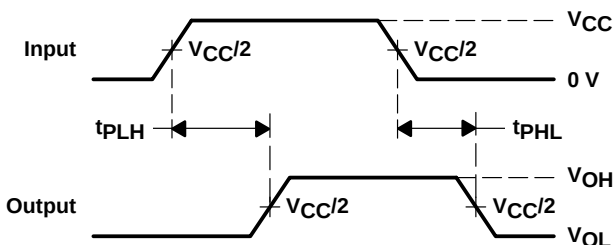


LOAD CIRCUIT

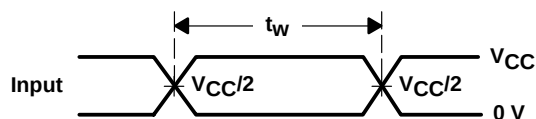
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHZ}	Open



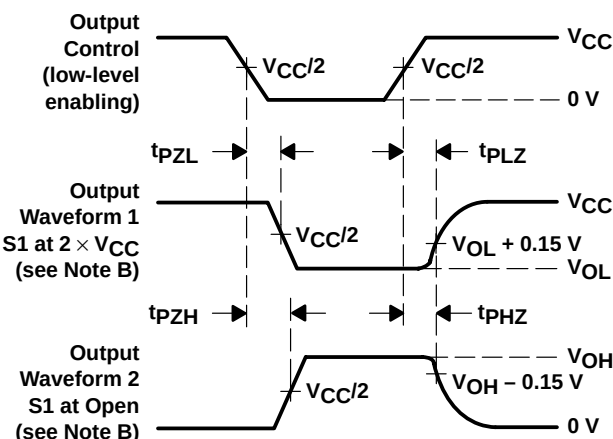
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

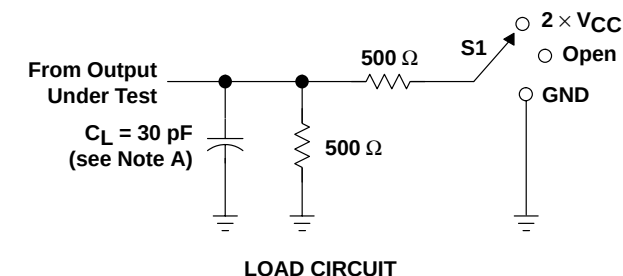
Figure 1. Load Circuit and Voltage Waveforms

SN74LVCU04A HEX INVERTER

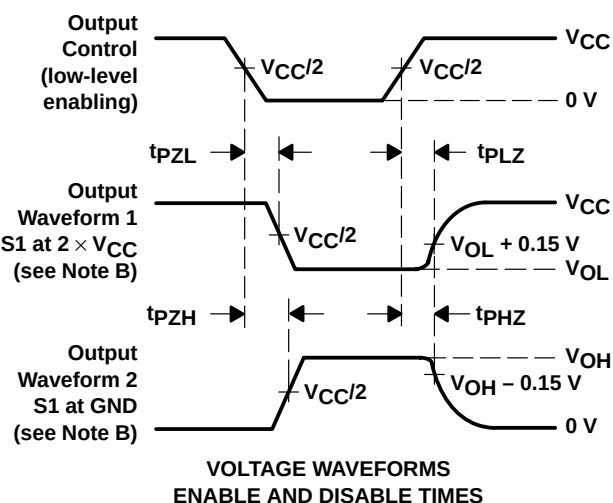
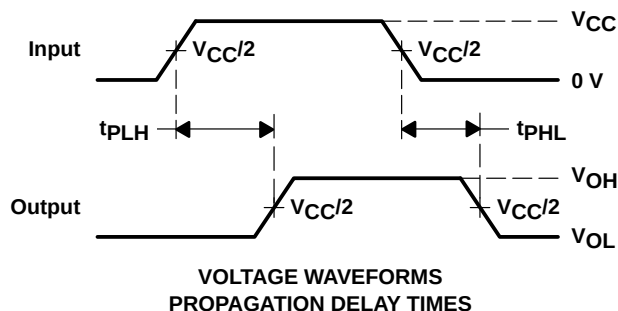
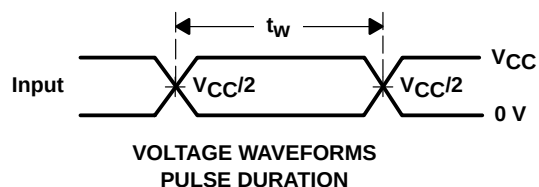
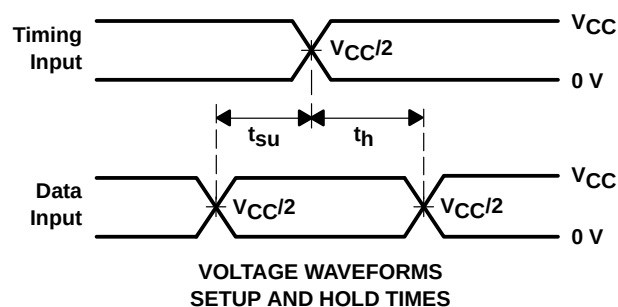
SCAS282F – JANUARY 1993 – REVISED JUNE 1998

PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND

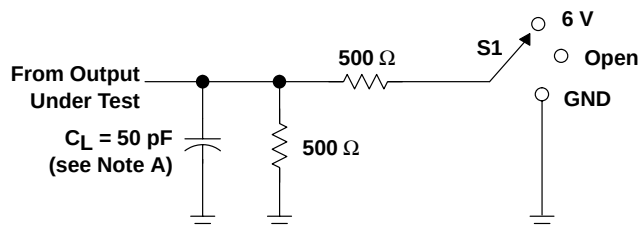


- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

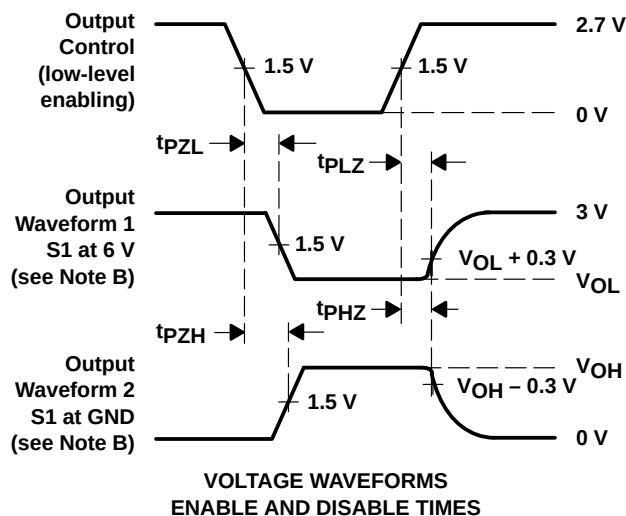
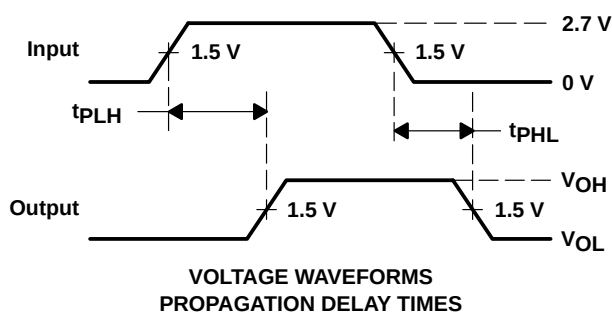
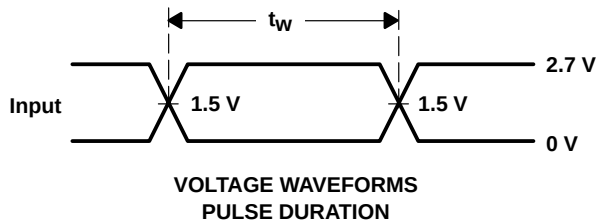
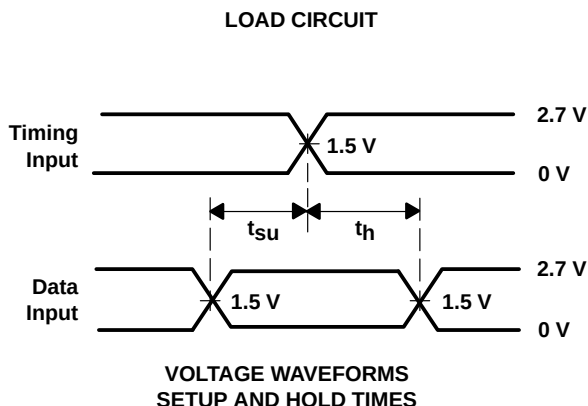
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC06A, SN74LVC06A HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

SCAS596C – OCTOBER 1997 – REVISED JULY 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Inputs and Open-Drain Outputs Accept Voltages up to 5.5 V**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (D), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and DIPs (J)**

description

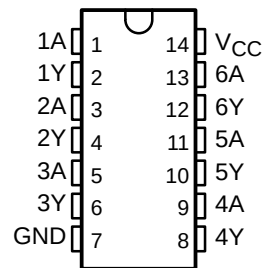
These hex inverter buffers/drivers are designed for 1.65-V to 3.6-V V_{CC} operation.

The outputs of the 'LVC06A devices are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

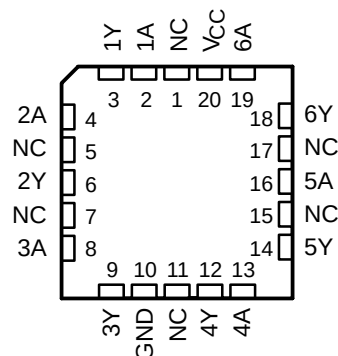
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC06A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC06A is characterized for operation from -40°C to 85°C .

SN54LVC06A . . . J OR W PACKAGE
SN74LVC06A . . . D, DGV, OR PW PACKAGE
(TOP VIEW)



SN54LVC06A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

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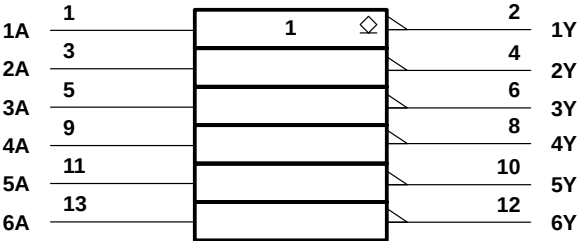
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SN54LVC06A, SN74LVC06A HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

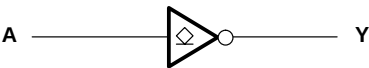
SCAS596C – OCTOBER 1997 – REVISED JULY 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for the D, DGV, and PW packages.

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O	–0.5 V to 6.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	127°C/W
DGV package	182°C/W
PW package	170°C/W
Storage temperature range, T_{Stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51.

SN54LVC06A, SN74LVC06A HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

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recommended operating conditions (see Note 4)

			SN54LVC06A		SN74LVC06A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		0.8		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	5.5	0	5.5	V
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		4		mA
		V _{CC} = 2.3 V	8		8		
		V _{CC} = 2.7 V	12		12		
		V _{CC} = 3 V	24		24		
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC06A			SN74LVC06A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V			0.2			0.2	V
	I _{OL} = 4 mA	1.65 V			0.45			0.45	
	I _{OL} = 8 mA	2.3 V			0.7			0.7	
	I _{OL} = 12 mA	2.7 V			0.4			0.4	
	I _{OL} = 24 mA	3 V			0.55			0.55	
I _I	V _I = 5.5 V or GND	3.6 V			±5			±5	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			10			10	µA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500			500	µA
C _i	V _I = V _{CC} or GND	3.3 V			5			5	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC06A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1.4	3.9	1	3.1	3.9		1	3.7	ns

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SN54LVC06A, SN74LVC06A
HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-DRAIN OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC06A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1.4	3.9	1	3.1	3.9		1	3.7	ns

operating characteristics, $T_A = 25^\circ\text{C}$

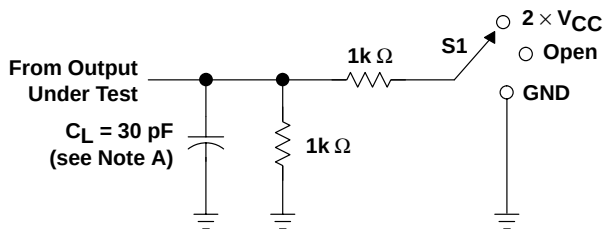
PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per buffer/driver	$f = 10\text{ MHz}$	2.1	2.3	2.5	pF

SN54LVC06A, SN74LVC06A HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

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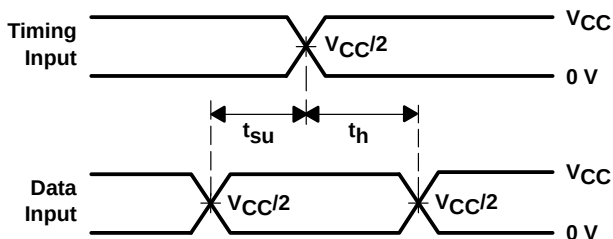
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$$

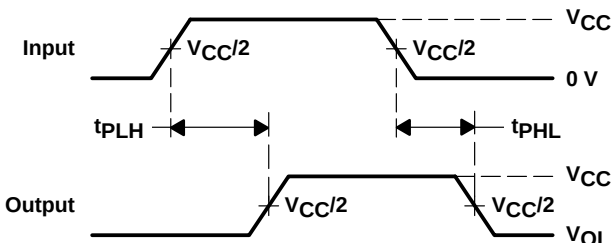


LOAD CIRCUIT

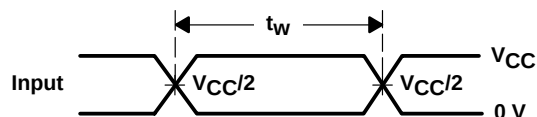
TEST	S1
t_{pZL} (see Note F)	$2 \times V_{CC}$
t_{pLZ} (see Note G)	$2 \times V_{CC}$
t_{PHZ}/t_{PHZ}	$2 \times V_{CC}$



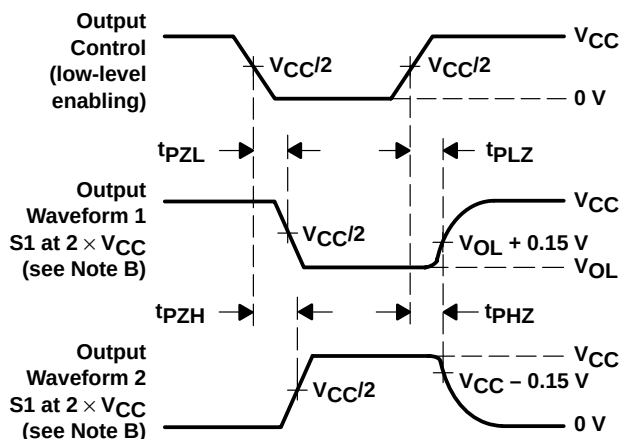
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pd} .
 - t_{pZL} is measured at $V_{CC}/2$.
 - t_{pLZ} is measured at $V_{OL} + 0.15\text{ V}$.

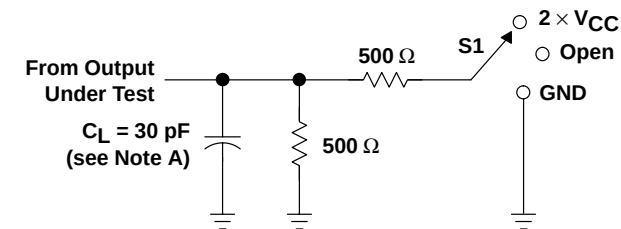
Figure 1. Load Circuit and Voltage Waveforms

SN54LVC06A, SN74LVC06A HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

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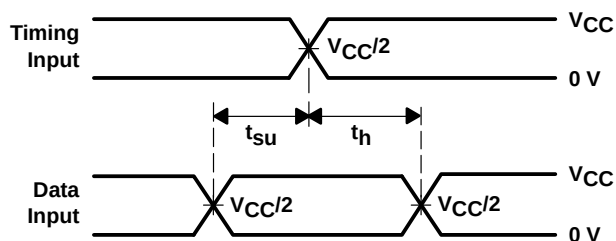
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

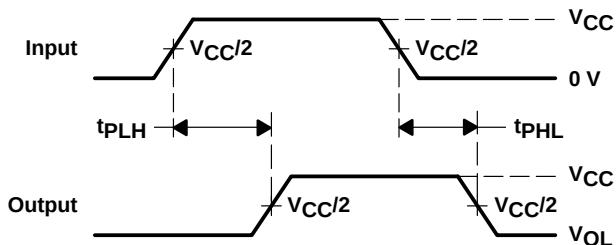


LOAD CIRCUIT

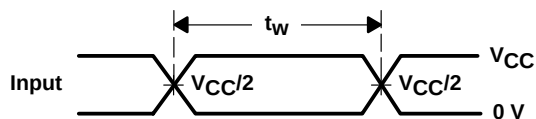
TEST	S1
t_{pZL} (see Note F)	$2 \times V_{CC}$
t_{pLZ} (see Note G)	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	$2 \times V_{CC}$



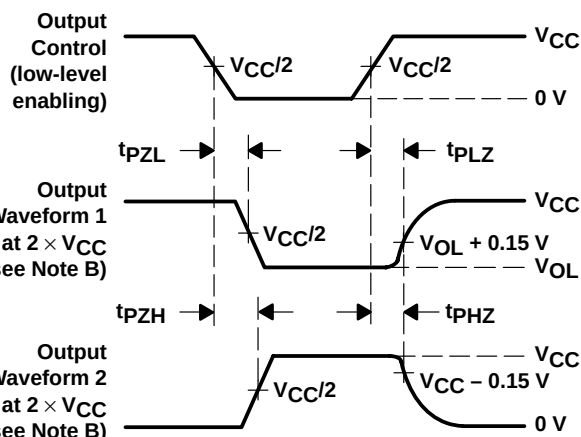
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



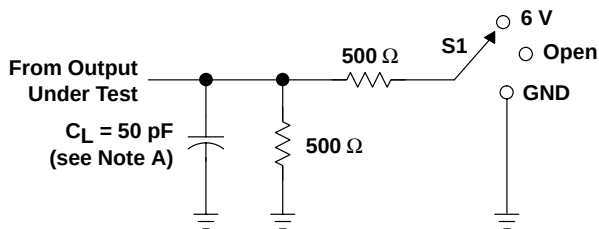
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pd} .
 - t_{pZL} is measured at $V_{CC}/2$.
 - t_{pLZ} is measured at $V_{OL} + 0.15 \text{ V}$.

Figure 2. Load Circuit and Voltage Waveforms

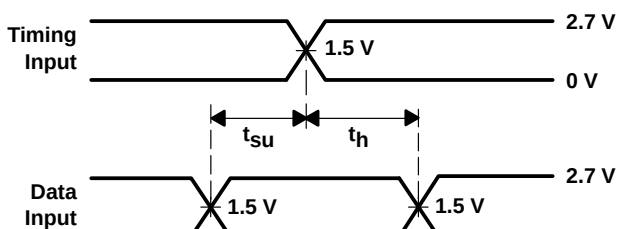
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.7 \text{ AND } 3.3 \text{ V} \pm 0.3 \text{ V}$$

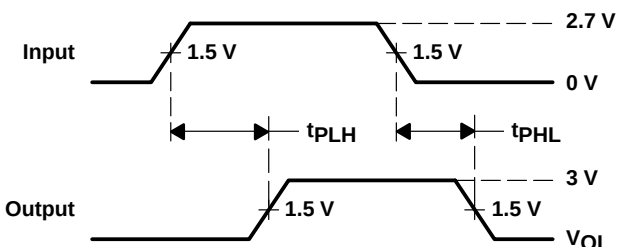


LOAD CIRCUIT

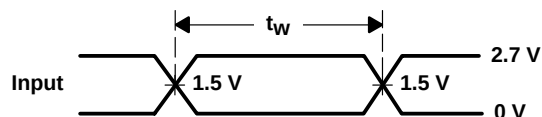
TEST	S1
t_{pZL} (see Note F)	6 V
t_{pLZ} (see Note G)	6 V
t_{PHZ}/t_{PHZ}	6 V



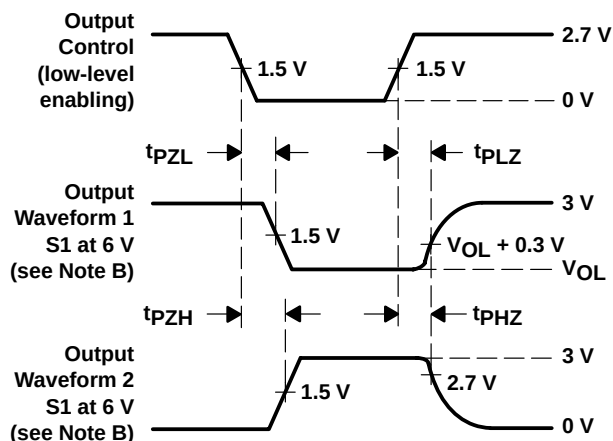
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pd} .
- F. t_{pZL} is measured at 1.5 V.
- G. t_{pLZ} is measured at $V_{OL} + 0.3 \text{ V}$.

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC07A, SN74LVC07A HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

SCAS595F – OCTOBER 1997 – REVISED JULY 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Inputs and Open-Drain Outputs Accept Voltages Up to 5.5 V**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (D), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW) Packages, and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and DIPs (J)**

description

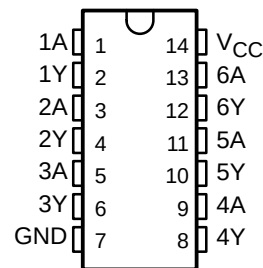
These hex buffers/drivers are designed for 1.65-V to 5.5-V V_{CC} operation.

The outputs of the 'LVC07A devices are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

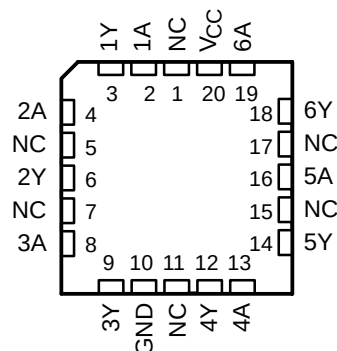
Inputs can be driven from 1.8-V, 2.5-V, 3.3-V (LVTTTL), or 5-V (CMOS) devices. This feature allows the use of these devices as translators in a mixed-system environment.

The SN54LVC07A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC07A is characterized for operation from -40°C to 85°C .

SN54LVC07A . . . J OR W PACKAGE
SN74LVC07A . . . D, DGV, OR PW PACKAGE
(TOP VIEW)



SN54LVC07A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each buffer/driver)

INPUT A	OUTPUT Y
H	H
L	L

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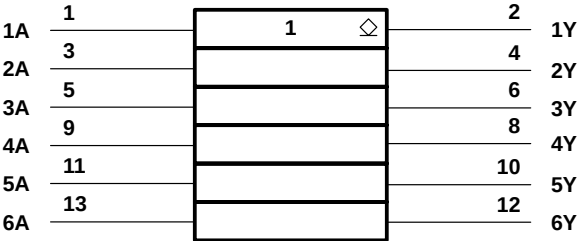
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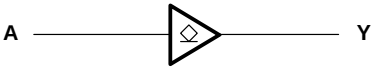
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DGV, J, PW, and W packages.

logic diagram, each buffer/driver (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O	–0.5 V to 6.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	127°C/W
DGV package	182°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

SN54LVC07A, SN74LVC07A HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

SCAS595F – OCTOBER 1997 – REVISED JULY 1998

recommended operating conditions (see Note 3)

			SN54LVC07A		SN74LVC07A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		1.65	5.5	1.65	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		0.8		
		V _{CC} = 4.5 V to 5.5 V	0.3 × V _{CC}		0.3 × V _{CC}		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	5.5	0	5.5	V
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		4		mA
		V _{CC} = 2.3 V	12		12		
		V _{CC} = 2.7 V	12		12		
		V _{CC} = 3 V	24		24		
		V _{CC} = 4.5 V	24		24		
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC07A			SN74LVC07A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OL}	I _{OL} = 100 μA	1.65 V to 5.5 V	0.2			0.2			V
	I _{OL} = 4 mA	1.65 V	0.45			0.45			
	I _{OL} = 12 mA	2.3 V	0.7			0.7			
		2.7 V	0.4			0.4			
	I _{OL} = 24 mA	3 V	0.55			0.55			
		4.5 V							
I _I	V _I = 5.5 V or GND	3.6 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			10			μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND	3.3 V	5			5			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC07A										UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1	3.5	1	2.8	3		1	2.9	1	2.6	ns

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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SN54LVC07A, SN74LVC07A
HEX BUFFERS/DRIVERS
WITH OPEN-DRAIN OUTPUTS

SCAS595F – OCTOBER 1997 – REVISED JULY 1998

switching characteristics over recommended operating free-air temperature range, (unless otherwise noted) (see Figures 1 through 4)

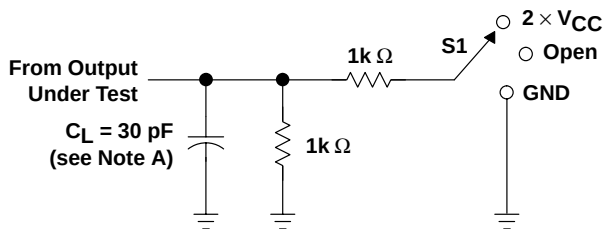
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC07A										UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1	3.5	1	2.8	3		1	2.9	1	2.6	ns

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per buffer/driver	$f = 10\text{ MHz}$	1.8	2	2.5	3.78	pF

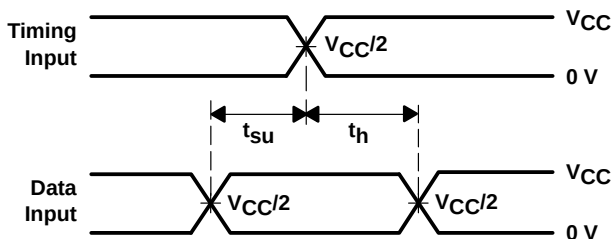
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$$

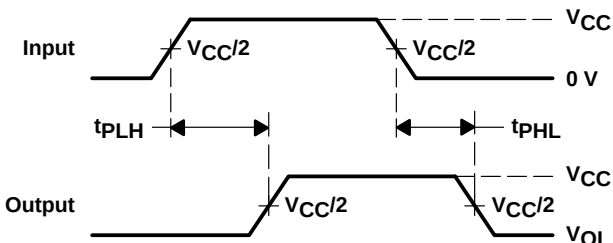


LOAD CIRCUIT

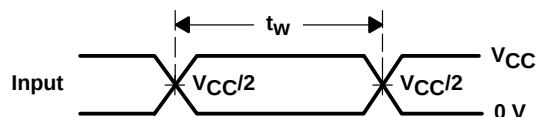
TEST	S1
t_{PZL} (see Note F)	2 $\times V_{CC}$
t_{PLZ} (see Note G)	2 $\times V_{CC}$
t_{PHZ}/t_{PHL}	2 $\times V_{CC}$



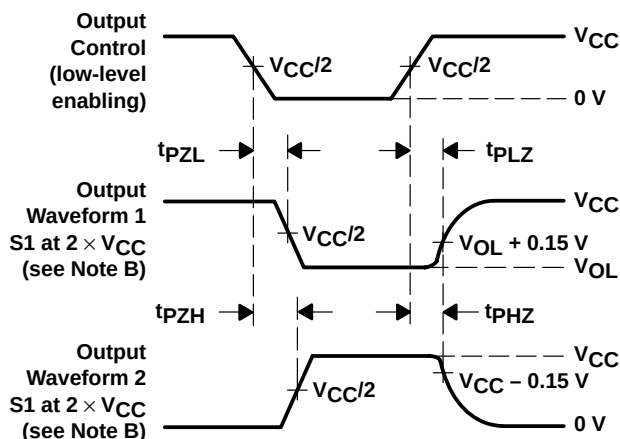
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
- F. t_{PZL} is measured at $V_{CC}/2$.
- G. t_{PLZ} is measured at $V_{OL} + 0.15\text{ V}$.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVC07A, SN74LVC07A

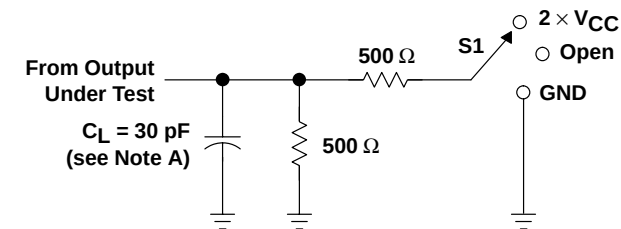
HEX BUFFERS/DRIVERS

WITH OPEN-DRAIN OUTPUTS

SCAS595F – OCTOBER 1997 – REVISED JULY 1998

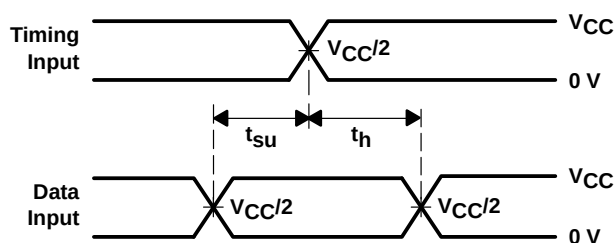
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

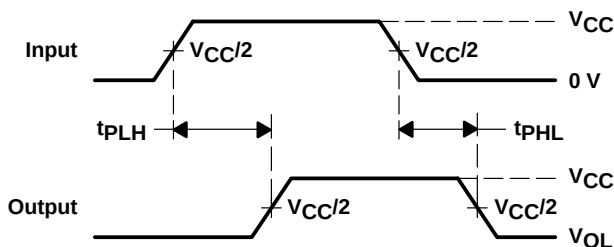


LOAD CIRCUIT

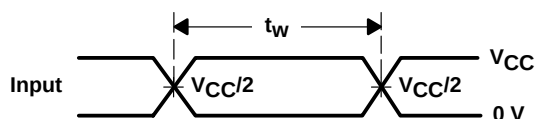
TEST	S1
t_{pZL} (see Note F)	2 $\times V_{CC}$
t_{pLZ} (see Note G)	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	2 $\times V_{CC}$



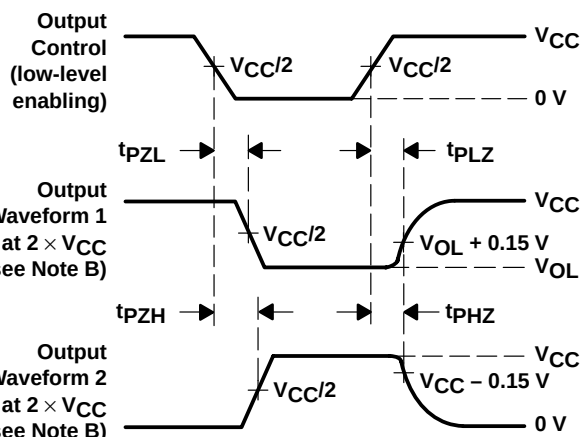
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



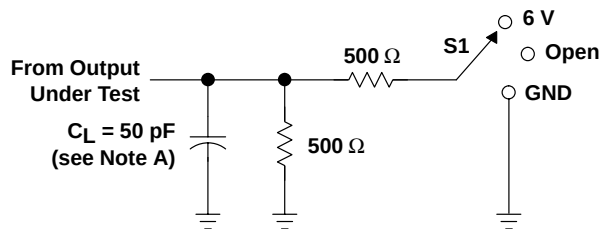
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pd} .
 - t_{pZL} is measured at $V_{CC}/2$.
 - t_{pLZ} is measured at $V_{OL} + 0.15 \text{ V}$.

Figure 2. Load Circuit and Voltage Waveforms

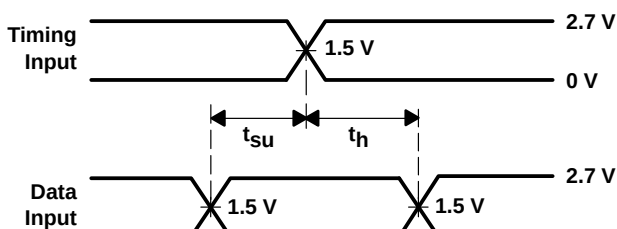
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.7 \text{ AND } 3.3 \text{ V} \pm 0.3 \text{ V}$$

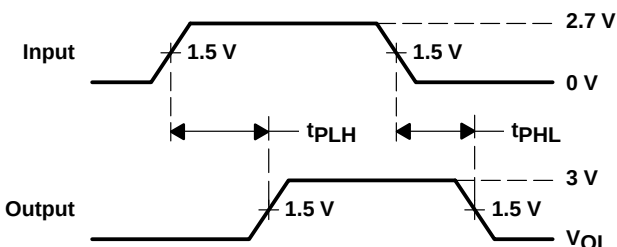


LOAD CIRCUIT

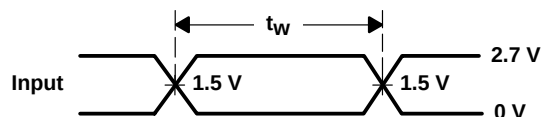
TEST	S1
t_{pZL} (see Note F)	6 V
t_{pLZ} (see Note G)	6 V
t_{PHZ}/t_{PH}	6 V



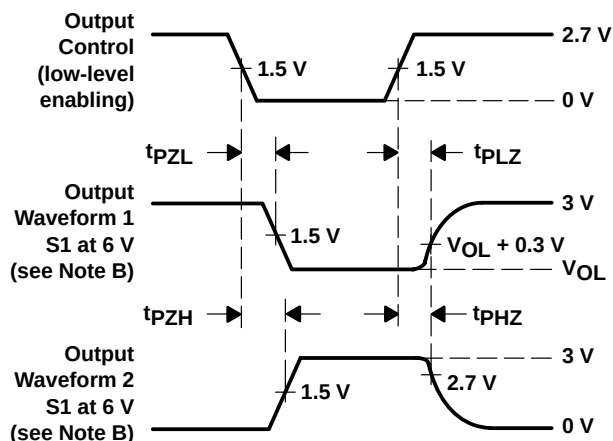
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pd} .
- F. t_{pZL} is measured at 1.5 V.
- G. t_{pLZ} is measured at $V_{OL} + 0.3 \text{ V}$.

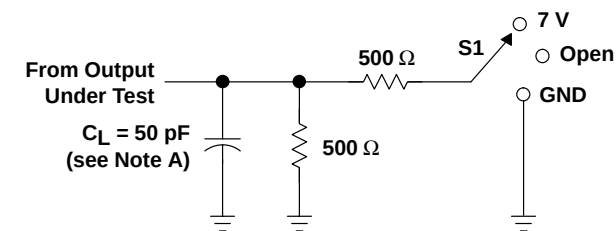
Figure 3. Load Circuit and Voltage Waveforms

SN54LVC07A, SN74LVC07A HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

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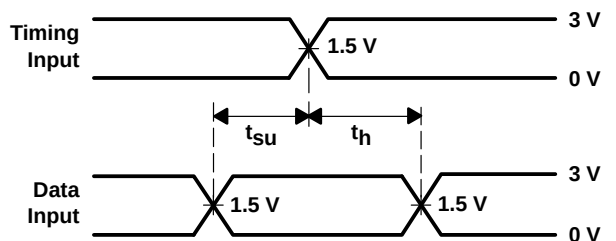
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$$

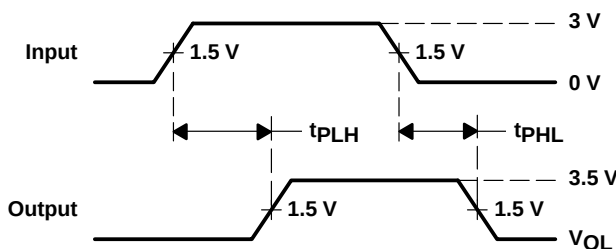


LOAD CIRCUIT

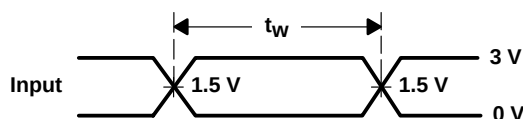
TEST	S1
t_{pZL} (see Note F)	7 V
t_{pLZ} (see Note G)	7 V
t_{PHZ}/t_{PHL}	7 V



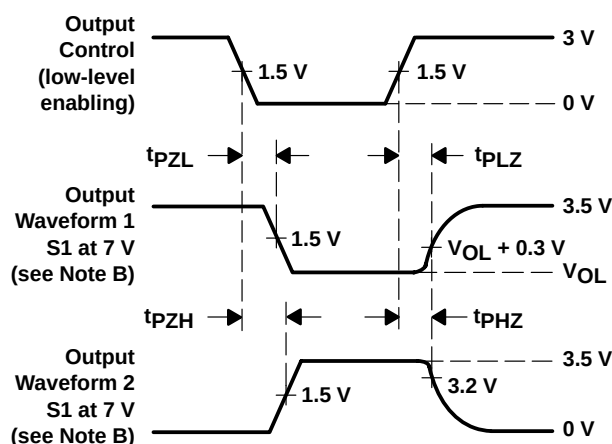
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pd} .
 - F. t_{pZL} is measured at 1.5 V.
 - G. t_{pLZ} is measured at $V_{OL} + 0.3\text{ V}$.

Figure 4. Load Circuit and Voltage Waveforms

SN54LVC08A, SN74LVC08A QUADRUPLE 2-INPUT POSITIVE-AND GATES

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flat (W) Packages, and DIPs (J)

description

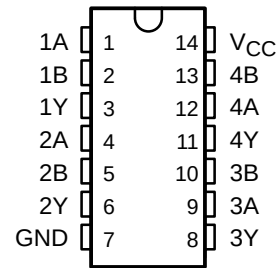
The SN54LVC08A quadruple 2-input positive-AND gate is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC08A quadruple 2-input positive-AND gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The 'LVC08A devices perform the Boolean function $Y = A \cdot B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

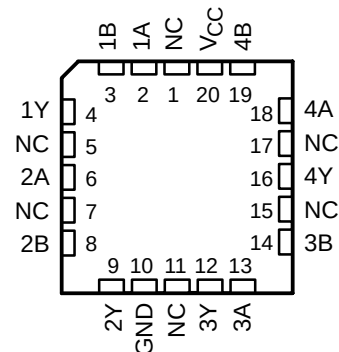
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC08A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC08A is characterized for operation from -40°C to 85°C .

SN54LVC08A . . . J OR W PACKAGE
SN74LVC08A . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LVC08A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



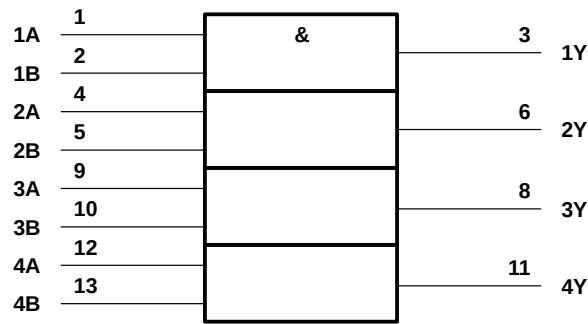
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVC08A, SN74LVC08A
QUADRUPLE 2-INPUT POSITIVE-AND GATES

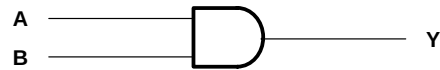
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, PW, and W packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	127°C/W
DB package	158°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LVC08A, SN74LVC08A QUADRUPLE 2-INPUT POSITIVE-AND GATES

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recommended operating conditions (see Note 4)

			SN54LVC08A		SN74LVC08A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			0.7		
		V _{CC} = 2.7 V to 3.6 V		0.8	0.8		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V			–4		mA
		V _{CC} = 2.3 V			–8		
		V _{CC} = 2.7 V		–12	–12		
		V _{CC} = 3 V		–24	–24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V			4		mA
		V _{CC} = 2.3 V			8		
		V _{CC} = 2.7 V		12	12		
		V _{CC} = 3 V		24	24		
Δt/Δv	Input transition rise or fall rate		0	8	0	8	ns/V
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVC08A, SN74LVC08A

QUADRUPLE 2-INPUT POSITIVE-AND GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC08A			SN74LVC08A			UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{OH}	I _{OH} = −100 μA	1.65 V to 3.6 V				V _{CC} −0.2			V	
		2.7 V to 3.6 V	V _{CC} −0.2							
	I _{OH} = −4 mA	1.65 V				1.2				
	I _{OH} = −8 mA	2.3 V				1.7				
	I _{OH} = −12 mA	2.7 V	2.2				2.2			
		3 V	2.4				2.4			
	I _{OH} = −24 mA	3 V	2.2				2.2			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.2			V	
		2.7 V to 3.6 V	0.2							
	I _{OL} = 4 mA	1.65 V				0.45				
	I _{OL} = 8 mA	2.3 V				0.7				
	I _{OL} = 12 mA	2.7 V	0.4			0.4				
	I _{OL} = 24 mA	3 V	0.55			0.55				
I _I	V _I = 5.5 V or GND	3.6 V	±5			±5			μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			10			μA	
ΔI _{CC}	One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500			μA	
C _i	V _I = V _{CC} or GND	3.3 V	5			5			pF	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC08A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	4.8		1	4.1	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC08A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	1	9.8	1	6.9	4.8		1	4.1	ns
t _{sk(o)} [‡]									1		ns

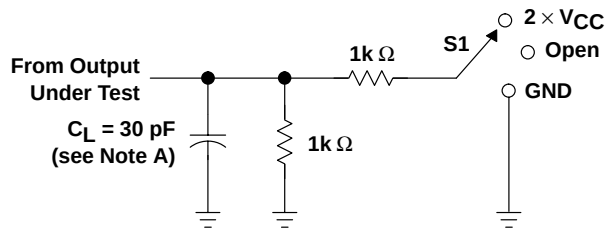
‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per gate	f = 10 MHz	7	9.8	10	pF

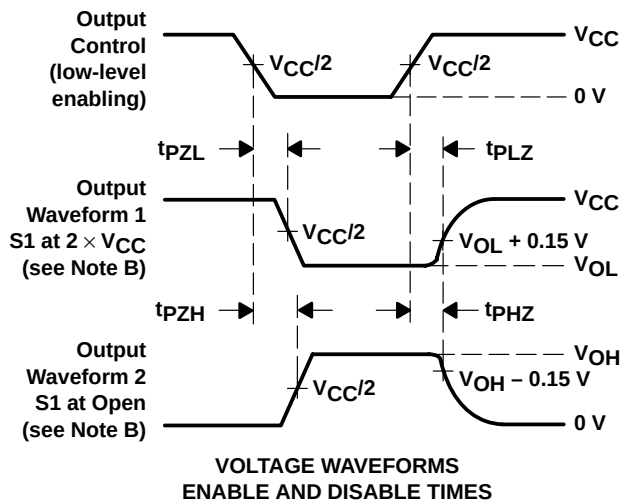
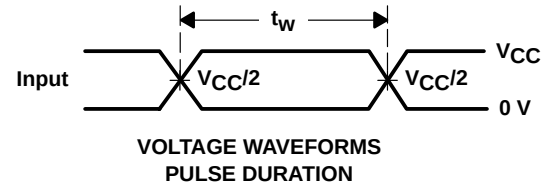
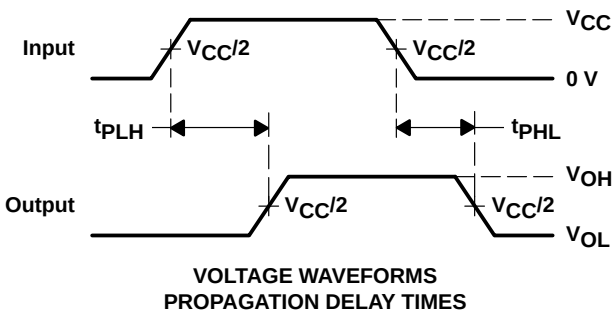
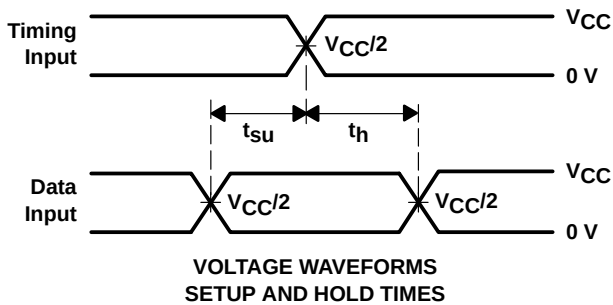


PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

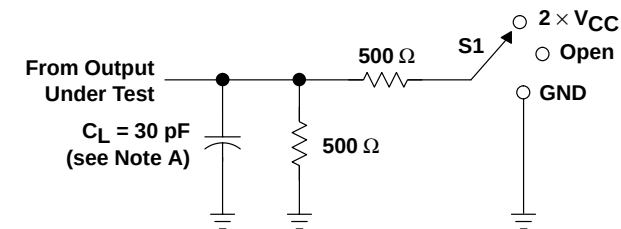
Figure 1. Load Circuit and Voltage Waveforms

SN54LVC08A, SN74LVC08A QUADRUPLE 2-INPUT POSITIVE-AND GATES

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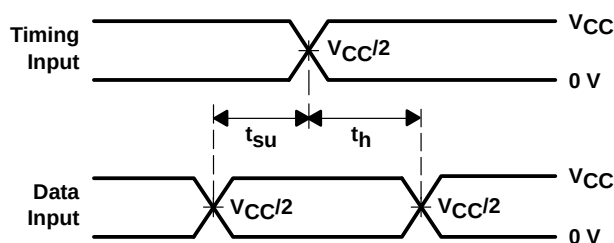
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

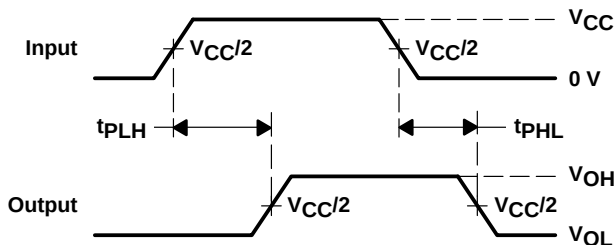


LOAD CIRCUIT

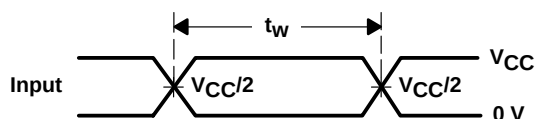
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



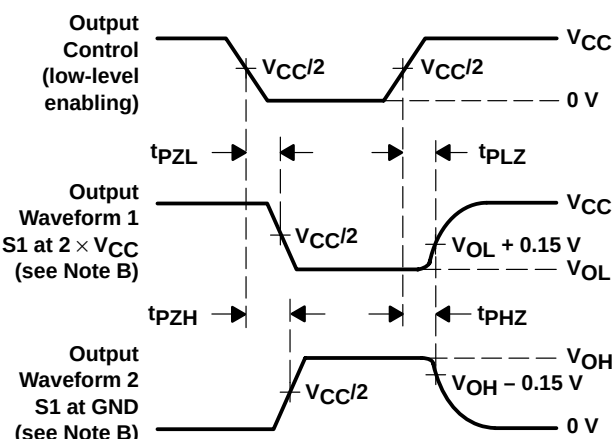
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

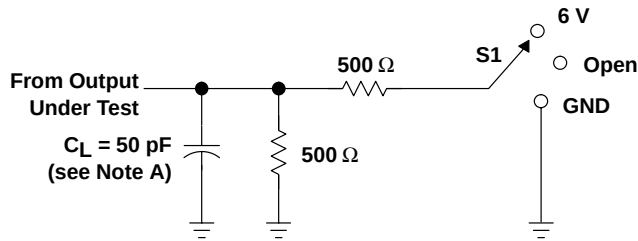


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

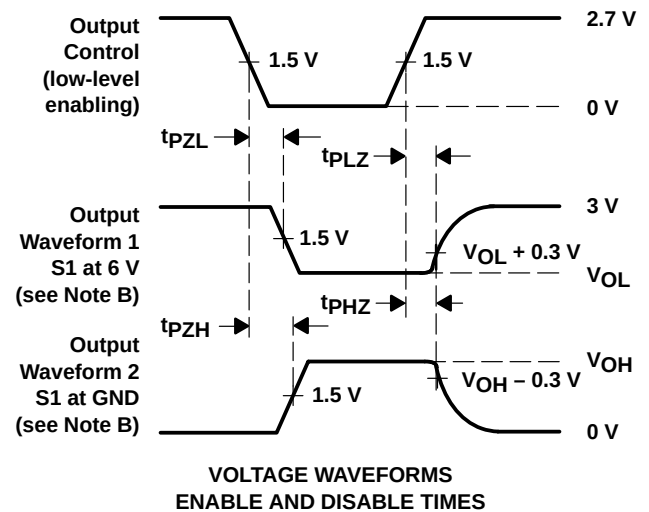
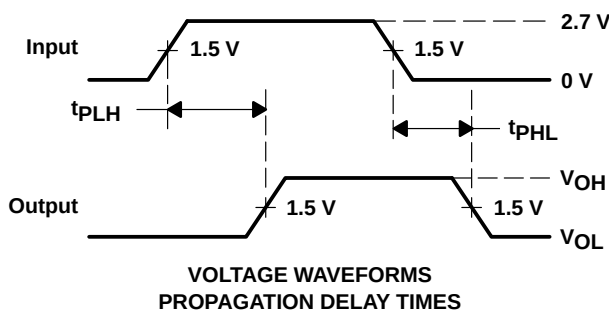
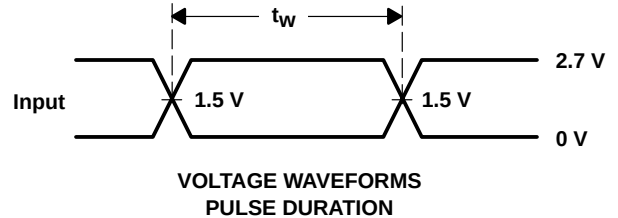
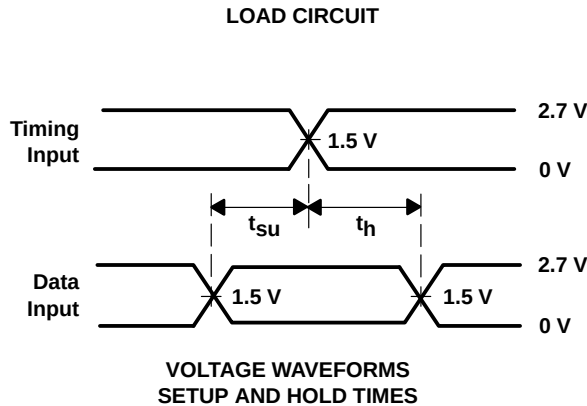
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

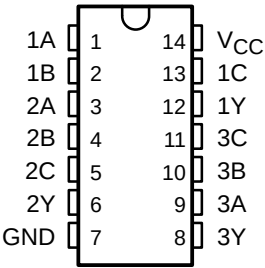
SN74LVC10A

TRIPLE 3-INPUT POSITIVE-NAND GATE

SCAS284F – JANUARY 1993 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^{\circ}\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^{\circ}\text{C}$**
- **Inputs Accept Voltages to 5.5 V**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This triple 3-input positive-NAND gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC10A performs the Boolean function $Y = \overline{A \bullet B \bullet C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC10A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each gate)

INPUTS			OUTPUT Y
A	B	C	
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



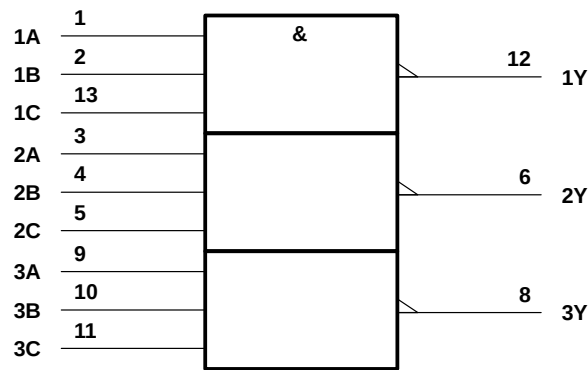
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SN74LVC10A
TRIPLE 3-INPUT POSITIVE-NAND GATE

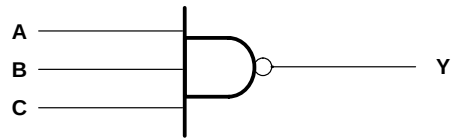
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN74LVC10A

TRIPLE 3-INPUT POSITIVE-NAND GATE

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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	−4		mA
		V _{CC} = 2.3 V	−8		
		V _{CC} = 2.7 V	−12		
		V _{CC} = 3 V	−24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		mA
		V _{CC} = 2.3 V	8		
		V _{CC} = 2.7 V	12		
		V _{CC} = 3 V	24		
T _A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V	V _{CC} –0.2		V	
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
I _{OH} = –24 mA	3 V	2.2				
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V	0.2		V	
	I _{OL} = 4 mA	1.65 V	0.45			
	I _{OL} = 8 mA	2.3 V	0.7			
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5		μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10		μA	
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500		μA	
C _i	V _I = V _{CC} or GND	3.3 V	5		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



SN74LVC10A

TRIPLE 3-INPUT POSITIVE-NAND GATE

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	†	†	†	†	5.8		1	4.9	ns
t _{sk(o)} ‡									1		ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

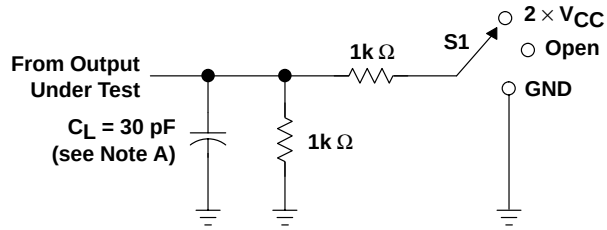
PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
		TYP	TYP	TYP	
C _{pd} Power dissipation capacitance per gate	f = 10 MHz	†	†	11	pF

† This information was not available at the time of publication.



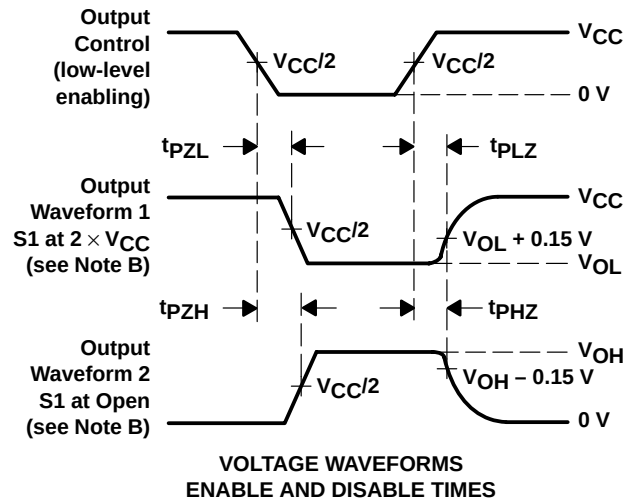
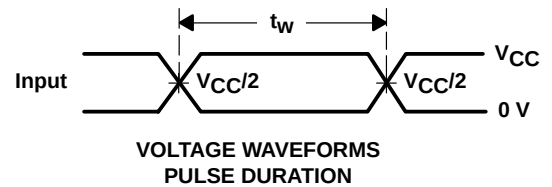
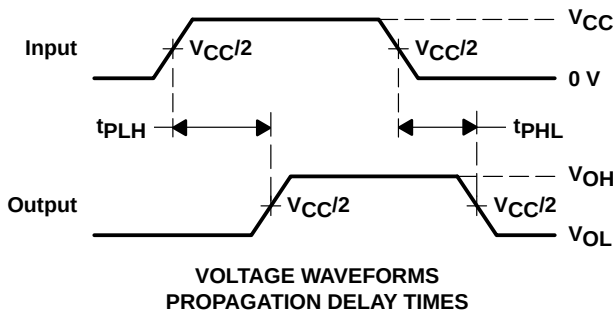
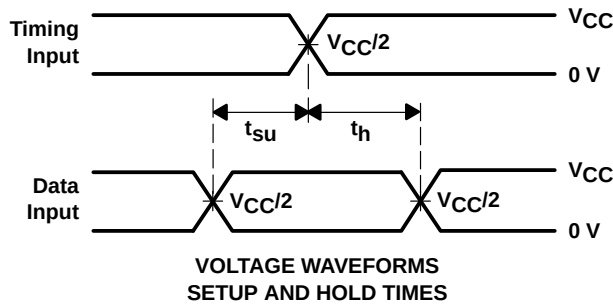
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

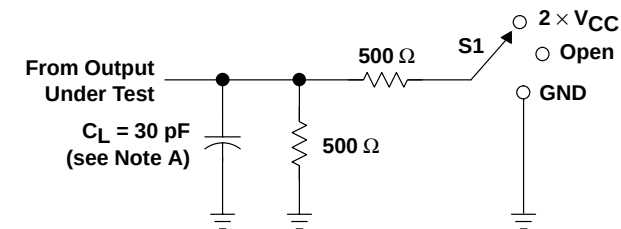
SN74LVC10A

TRIPLE 3-INPUT POSITIVE-NAND GATE

SCAS284F – JANUARY 1993 – REVISED JUNE 1998

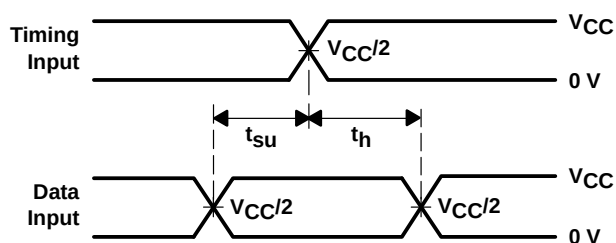
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

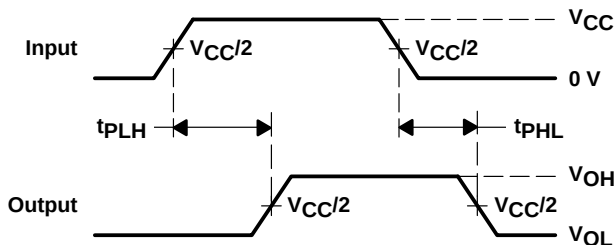


LOAD CIRCUIT

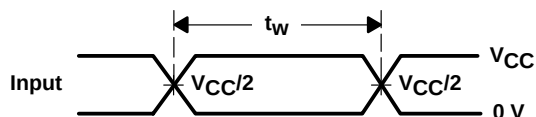
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



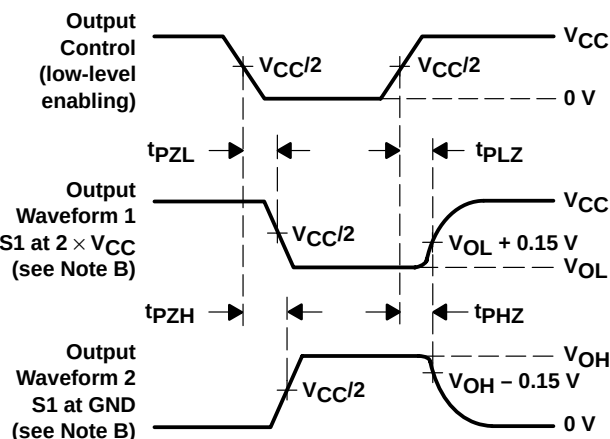
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



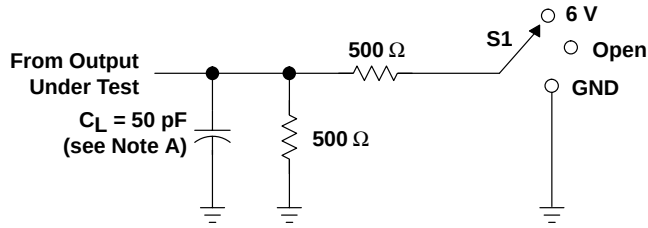
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

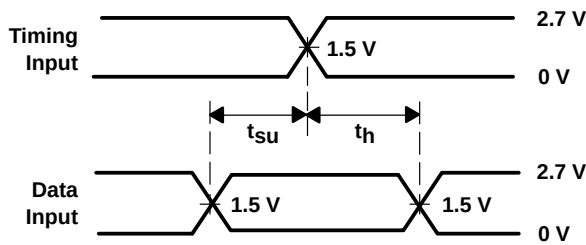
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

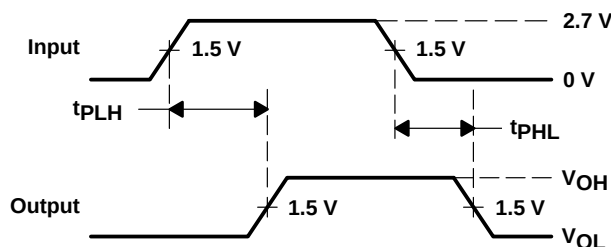


LOAD CIRCUIT

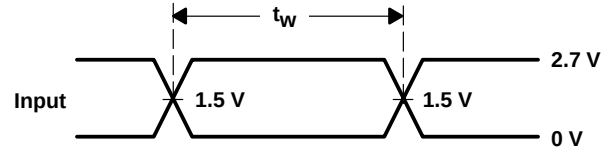
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



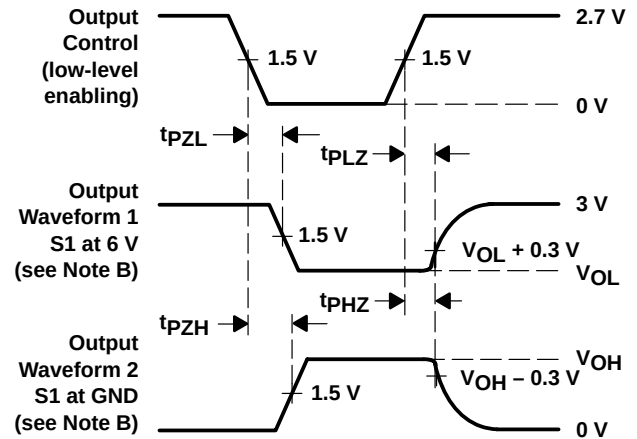
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC14A, SN74LVC14A HEX SCHMITT-TRIGGER INVERTERS

SCAS285H – MARCH 1993 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

description

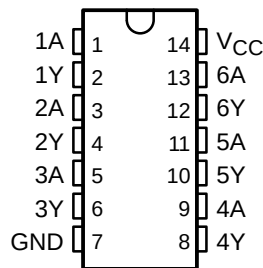
The SN54LVC14A hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC14A hex Schmitt-trigger inverter is designed for 1.65-V to 3.6-V V_{CC} operation.

The devices contain six independent inverters, and perform the Boolean function $Y = \bar{A}$.

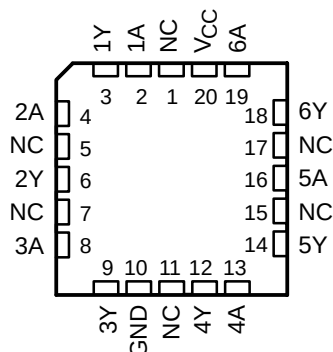
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC14A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC14A is characterized for operation from -40°C to 85°C .

SN54LVC14A . . . J OR W PACKAGE
SN74LVC14A . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LVC14 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

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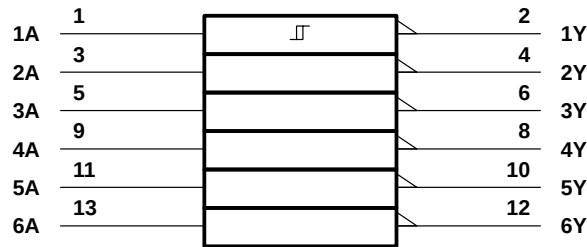
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVC14A, SN74LVC14A
HEX SCHMITT-TRIGGER INVERTERS

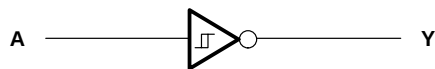
SCAS285H – MARCH 1993 – REVISED JUNE 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LVC14A, SN74LVC14A HEX SCHMITT-TRIGGER INVERTERS

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recommended operating conditions (see Note 4)

			SN54LVC14A		SN74LVC14A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			0.7		
		V _{CC} = 2.7 V to 3.6 V		0.8	0.8		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V			–4		mA
		V _{CC} = 2.3 V			–8		
		V _{CC} = 2.7 V		–12	–12		
		V _{CC} = 3 V		–24	–24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V			4		mA
		V _{CC} = 2.3 V			8		
		V _{CC} = 2.7 V		12	12		
		V _{CC} = 3 V		24	24		
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVC14A, SN74LVC14A HEX SCHMITT-TRIGGER INVERTERS

SCAS285H – MARCH 1993 – REVISED JUNE 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC14A			SN74LVC14A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{T+} Positive-going threshold		2.7 V	0.8		2	0.8		2	V
		3 V	0.8		2	0.8		2	
		3.6 V	0.8		2	0.8		2	
V _{T–} Negative-going threshold		2.7 V	0.4		1.4	0.4		1.4	V
		3 V	0.6		1.5	0.6		1.5	
		3.6 V	0.8		1.8	0.8		1.8	
ΔV _T Hysteresis (V _{T+} – V _{T–})		2.7 V	0.3		1.1	0.3		1.1	V
		3 V	0.3		1.2	0.3		1.2	
		3.6 V	0.3		1.2	0.3		1.2	
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V				V _{CC} –0.2			V
		2.7 V to 3.6 V	V _{CC} –0.2						
	I _{OH} = –4 mA	1.65 V				1.2			
	I _{OH} = –8 mA	2.3 V				1.7			
	I _{OH} = –12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
	I _{OH} = –24 mA	3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.2			V
		2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA	1.65 V				0.45			
	I _{OL} = 8 mA	2.3 V				0.7			
	I _{OL} = 12 mA	2.7 V	0.4			0.4			
	I _{OL} = 24 mA	3 V	0.55			0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			10			μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND	3.3 V	5			5			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC14A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A	Y	7.5		1	6.4	ns



SN54LVC14A, SN74LVC14A HEX SCHMITT-TRIGGER INVERTERS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC14A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	†	†	†	†	7.5	1	6.4	ns	
t _{sk(o)} [‡]								1		ns	

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
		TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per inverter	$f = 10\text{ MHz}$	†	†	7	pF

† This information was not available at the time of publication.

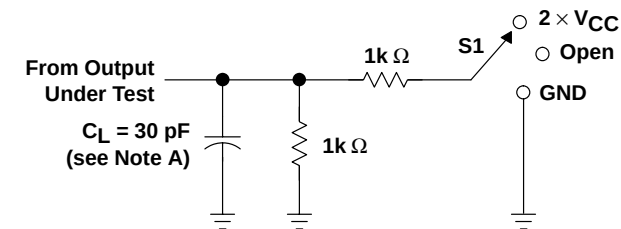


SN54LVC14A, SN74LVC14A HEX SCHMITT-TRIGGER INVERTERS

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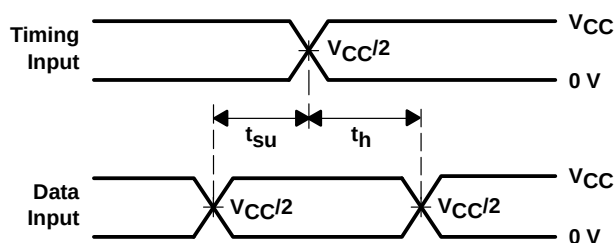
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

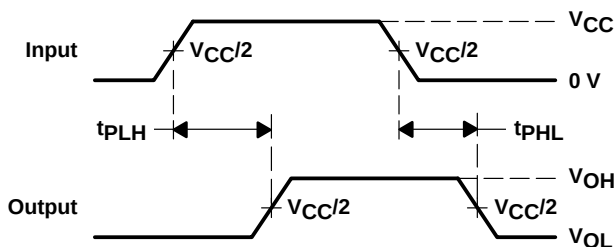


LOAD CIRCUIT

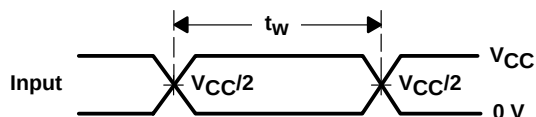
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



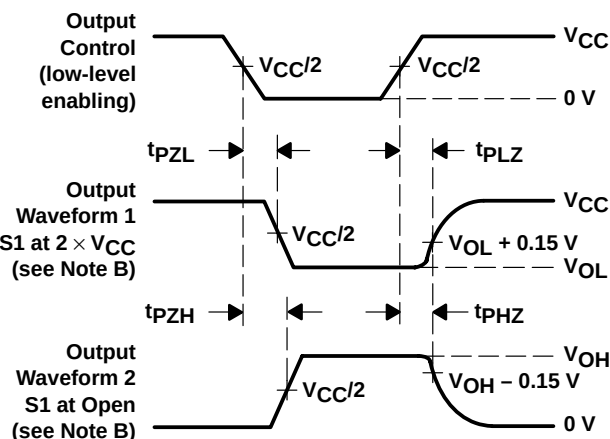
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



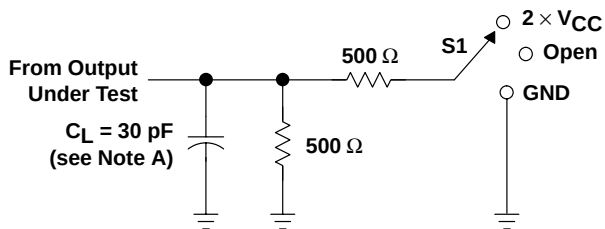
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

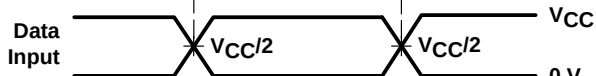
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

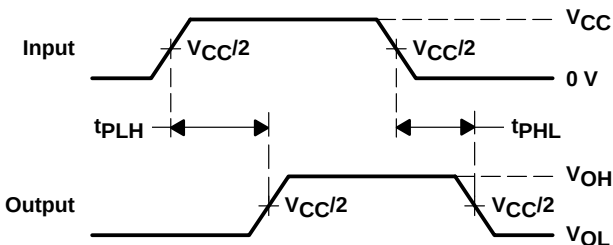


LOAD CIRCUIT

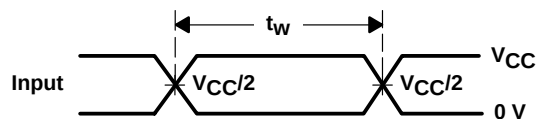
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PHZ}	GND



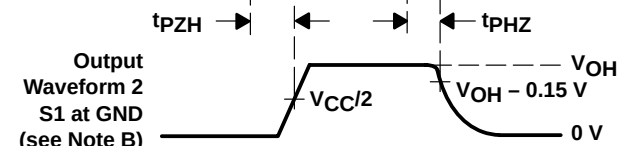
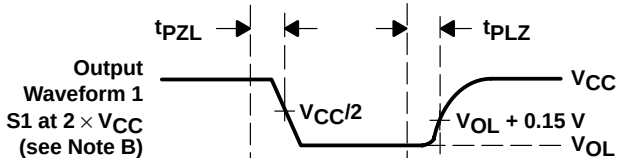
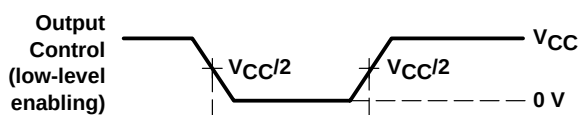
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

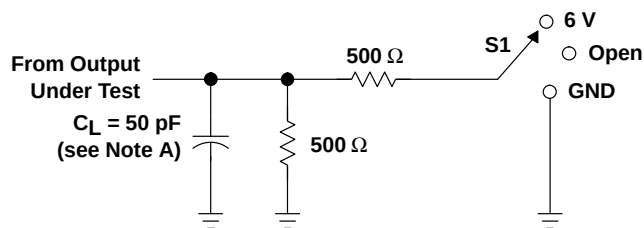
Figure 2. Load Circuit and Voltage Waveforms

SN54LVC14A, SN74LVC14A HEX SCHMITT-TRIGGER INVERTERS

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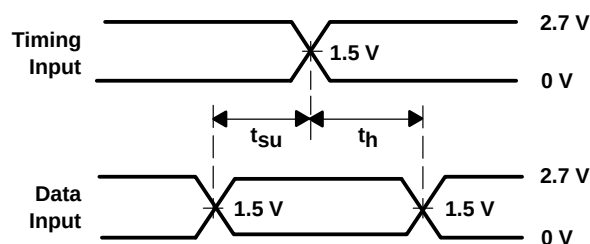
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$

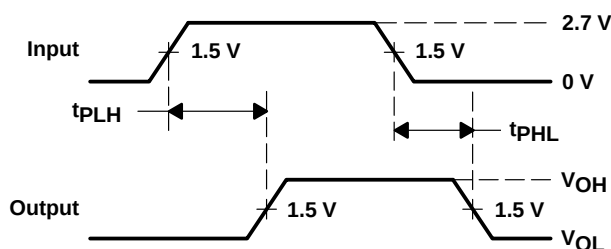


LOAD CIRCUIT

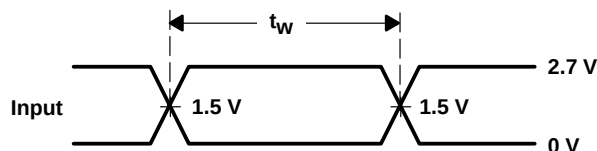
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



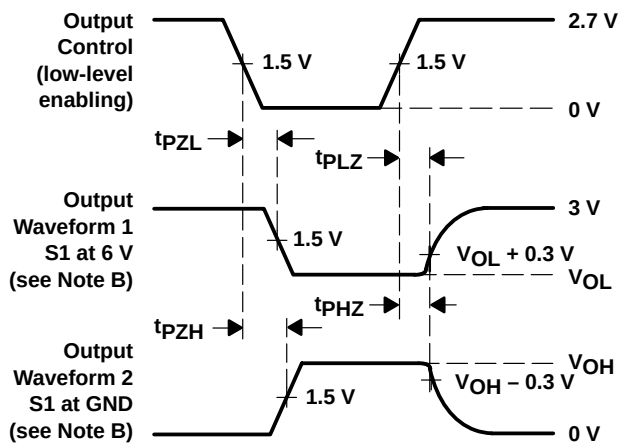
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC32A, SN74LVC32A QUADRUPL 2-INPUT POSITIVE-OR GATES

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Inputs Accept Voltages to 5.5 V**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and DIPs (J)**

description

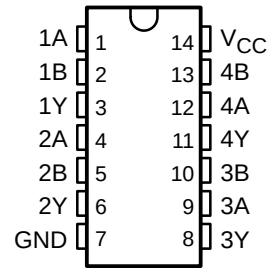
The SN54LVC32A quadruple 2-input positive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC32A quadruple 2-input positive-OR gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The 'LVC32A devices perform the Boolean function $Y = A + B$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

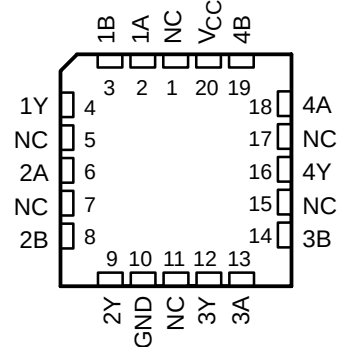
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC32A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC32A is characterized for operation from -40°C to 85°C .

SN54LVC32A . . . J OR W PACKAGE
SN74LVC32A . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LVC32A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT Y
A	B	
H	X	H
X	H	H
L	L	L

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



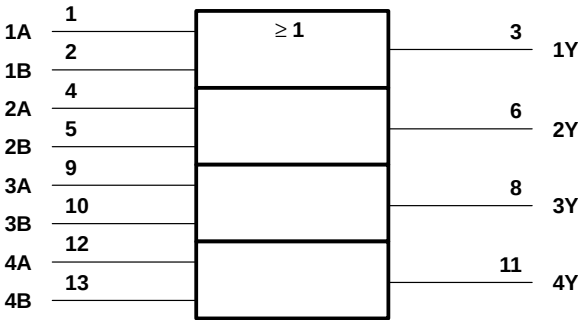
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVC32A, SN74LVC32A QUADRUPLE 2-INPUT POSITIVE-OR GATES

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, PW, and W packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	127°C/W
DB package	158°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LVC32A, SN74LVC32A QUADRUPLE 2-INPUT POSITIVE-OR GATES

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recommended operating conditions (see Note 4)

			SN54LVC32A		SN74LVC32A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			0.7		
		V _{CC} = 2.7 V to 3.6 V		0.8	0.8		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V			–4		mA
		V _{CC} = 2.3 V			–8		
		V _{CC} = 2.7 V		–12	–12		
		V _{CC} = 3 V		–24	–24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V			4		mA
		V _{CC} = 2.3 V			8		
		V _{CC} = 2.7 V		12	12		
		V _{CC} = 3 V		24	24		
Δt/Δv	Input transition rise or fall rate		0	7	0	7	ns/V
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVC32A, SN74LVC32A

QUADRUPLE 2-INPUT POSITIVE-OR GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC32A			SN74LVC32A			UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V				V _{CC} –0.2			V	
		2.7 V to 3.6 V	V _{CC} –0.2							
	I _{OH} = –4 mA	1.65 V				1.2				
	I _{OH} = –8 mA	2.3 V				1.7				
	I _{OH} = –12 mA	2.7 V	2.2				2.2			
		3 V	2.4				2.4			
	I _{OH} = –24 mA	3 V	2.2				2.2			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.2			V	
		2.7 V to 3.6 V	0.2							
	I _{OL} = 4 mA	1.65 V				0.45				
	I _{OL} = 8 mA	2.3 V				0.7				
	I _{OL} = 12 mA	2.7 V	0.4			0.4				
	I _{OL} = 24 mA	3 V	0.55			0.55				
I _I	V _I = 5.5 V or GND	3.6 V	±5			±5			μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			10			μA	
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500			μA	
C _i	V _I = V _{CC} or GND	3.3 V	5			5			pF	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC32A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	4.4		1	3.8	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC32A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	1	8.7	1	5.4	4.4		1.5	3.8	ns
t _{sk(o)} [‡]									1		ns

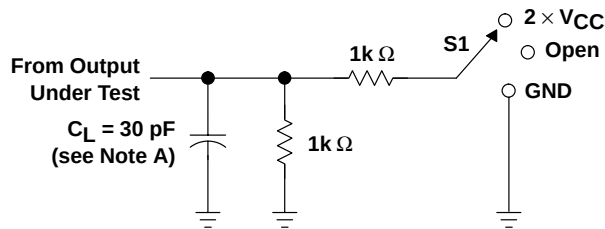
‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per gate	f = 10 MHz	7.5	10.6	12.5	pF

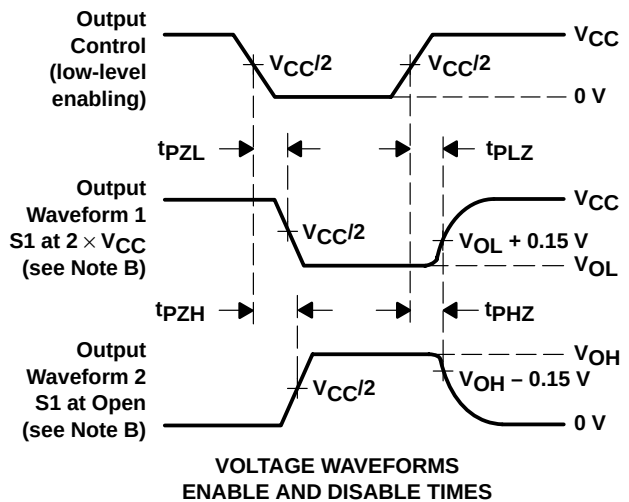
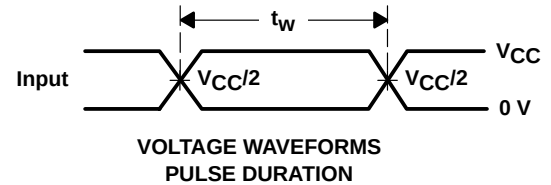
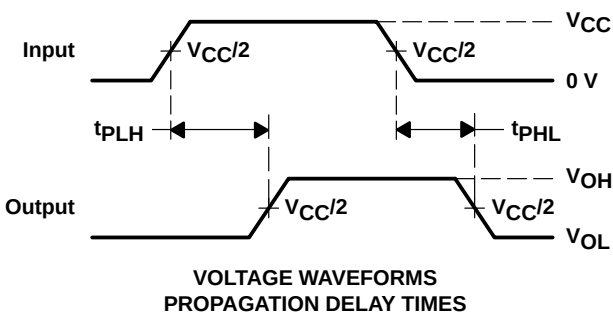
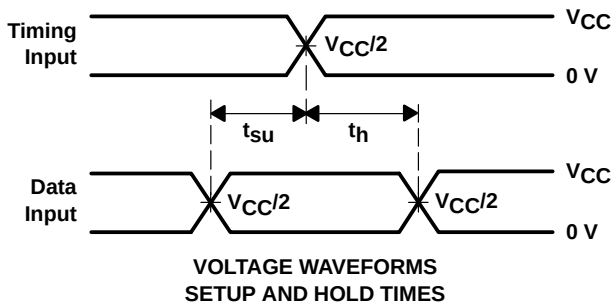


PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	Open



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

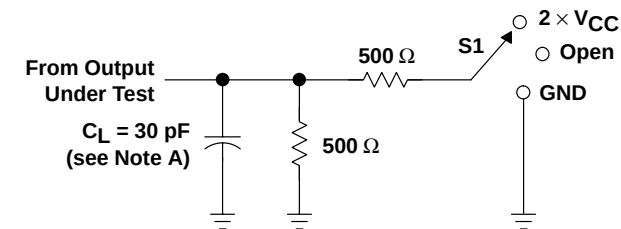
Figure 1. Load Circuit and Voltage Waveforms

SN54LVC32A, SN74LVC32A QUADRUPLE 2-INPUT POSITIVE-OR GATES

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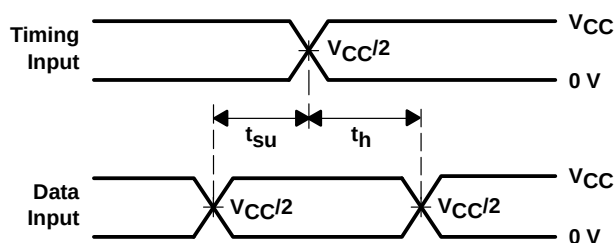
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

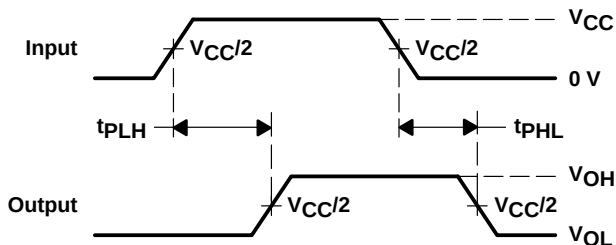


LOAD CIRCUIT

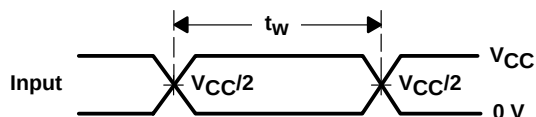
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



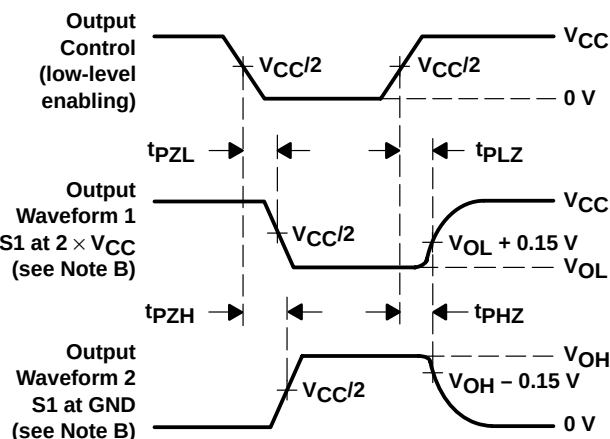
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

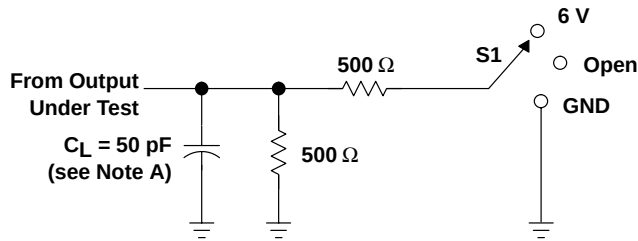


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

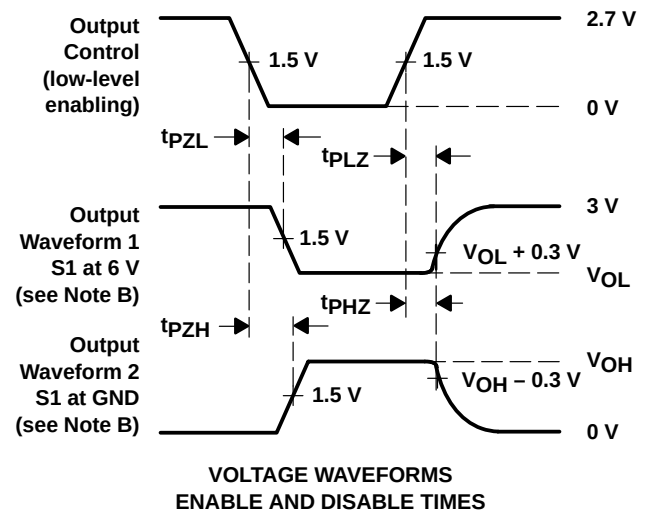
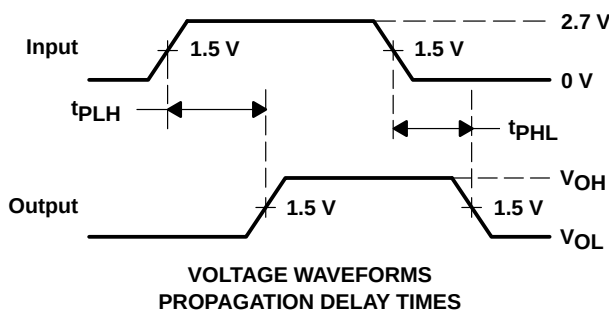
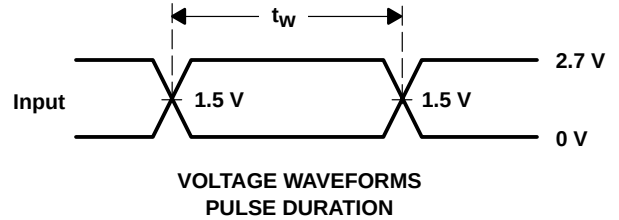
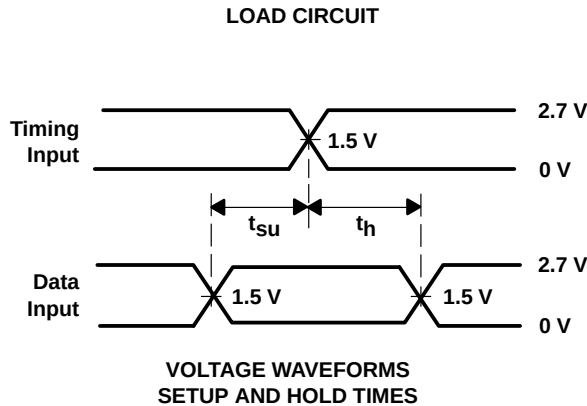
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC74A, SN74LVC74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Inputs Accept Voltages to 5.5 V**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and DIPs (J)**

description

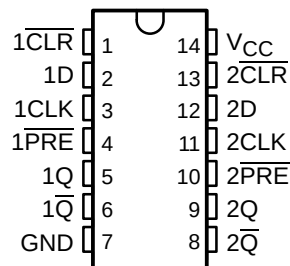
The SN54LVC74A dual positive-edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC74A dual positive-edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

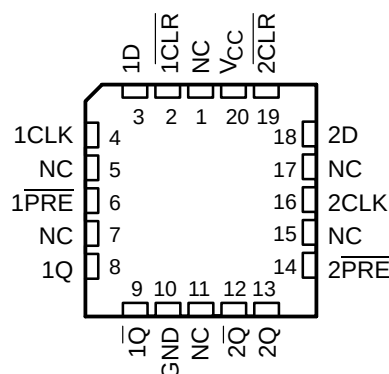
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC74A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC74A is characterized for operation from -40°C to 85°C .

SN54LVC74A ... J OR W PACKAGE
SN74LVC74A ... D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LVC74A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVC74A, SN74LVC74A

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH CLEAR AND PRESET

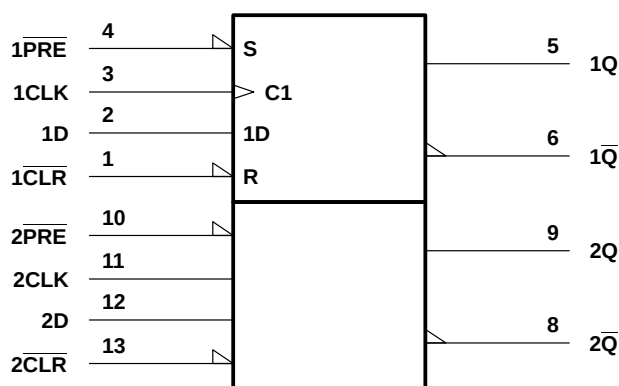
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FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H [†]	H [†]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	$\overline{\text{Q}}_0$

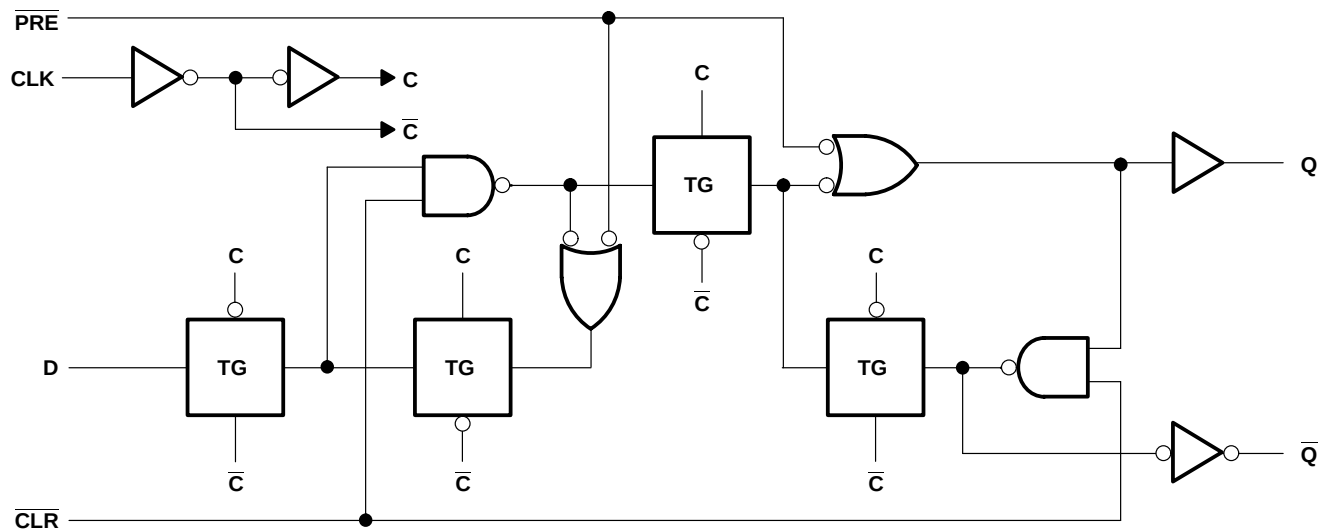
[†] This configuration is unstable; that is, it does not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

logic symbol[‡]



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, PW, and W packages.

logic diagram, each flip-flop (positive logic)



SN54LVC74A, SN74LVC74A

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply-voltage range, V_{CC}	–0.5 V to 6.5 V
Input-voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output-voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	127°C/W
DB package	158°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVC74A		SN74LVC74A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	Operating	2	3.6	1.65	3.6	V
	Data retention only	1.5		1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V			1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V			0.7		
	$V_{CC} = 2.7$ V to 3.6 V		0.8	0.8		
V_I Input voltage		0	5.5	0	5.5	V
V_O Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current	$V_{CC} = 1.65$ V				–4	mA
	$V_{CC} = 2.3$ V				–8	
	$V_{CC} = 2.7$ V		–12		–12	
	$V_{CC} = 3$ V		–24		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V				4	mA
	$V_{CC} = 2.3$ V				8	
	$V_{CC} = 2.7$ V		12		12	
	$V_{CC} = 3$ V		24		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	0	10	ns/V
T_A Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVC74A, SN74LVC74A

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH CLEAR AND PRESET

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC74A			SN74LVC74A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V				V _{CC} –0.2			V
		2.7 V to 3.6 V	V _{CC} –0.2						
	I _{OH} = –4 mA	1.65 V				1.2			
	I _{OH} = –8 mA	2.3 V				1.7			
	I _{OH} = –12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
	I _{OH} = –24 mA	3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.2			V
		2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA	1.65 V				0.45			
	I _{OL} = 8 mA	2.3 V				0.7			
	I _{OL} = 12 mA	2.7 V	0.4			0.4			
	I _{OL} = 24 mA	3 V	0.55			0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			10			μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND	3.3 V	5			5			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

			SN54LVC74A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		83		100		MHz
t _w	Pulse duration		PRE or CLR low		3.3		ns
			CLK high or low		3.3		
t _{su}	Setup time before CLK↑		Data		3		ns
			PRE or CLR inactive		2		
t _h	Hold time, data after CLK↑		1		1		ns



SN54LVC74A, SN74LVC74A

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			SN74LVC74A								UNIT
			$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		†		†		83		100		MHz
t _w	Pulse duration	PRE or CLR low	†		†		3.3		3.3		ns
		CLK high or low	†		†		3.3		3.3		
t _{su}	Setup time before CLK↑	Data	†		†		3.4		3		ns
		PRE or CLR inactive	†		†		2.2		2		
t _h	Hold time, data after CLK↑		†		†		1		0		ns

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC74A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
f _{max}			83		100		MHz
t _{pd}	CLK	Q or $\overline{Q}$	6		1	5.2	ns
	$\overline{\text{PRE}}$ or CLR		6.4		1	5.4	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC74A								UNIT	
			$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f _{max}			†		†			83		100		MHz
t _{pd}	CLK	Q or $\overline{Q}$	†	†	†	†		6		1	5.2	ns
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$		†	†	†	†		6.4		1	5.4	
t _{sk(o)} [‡]										1		ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per flip-flop	f = 10 MHz	†	†	27	pF

† This information was not available at the time of publication.

SN54LVC74A, SN74LVC74A

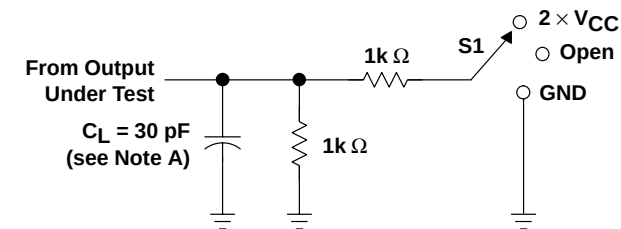
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH CLEAR AND PRESET

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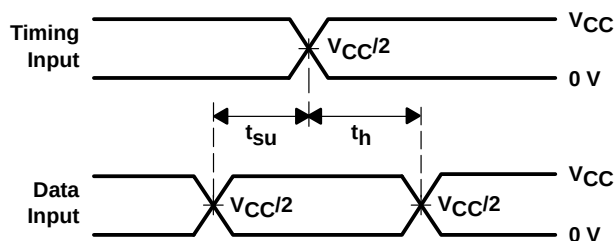
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

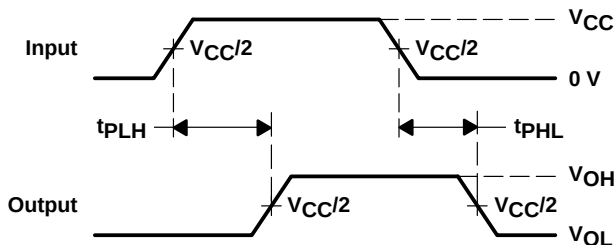


LOAD CIRCUIT

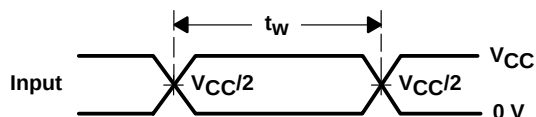
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



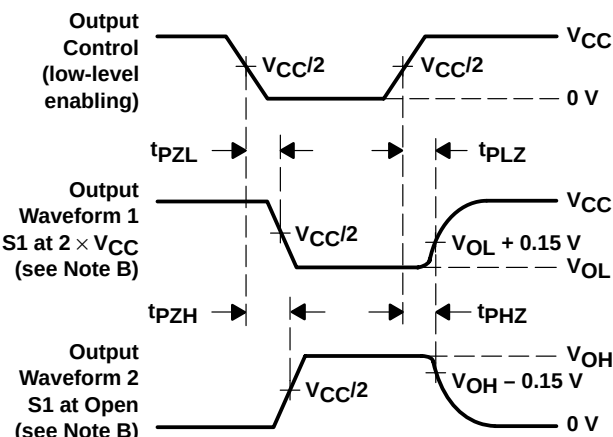
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

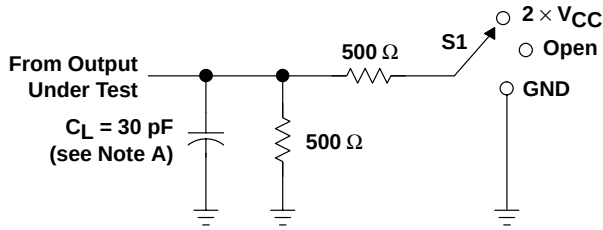
Figure 1. Load Circuit and Voltage Waveforms

SN54LVC74A, SN74LVC74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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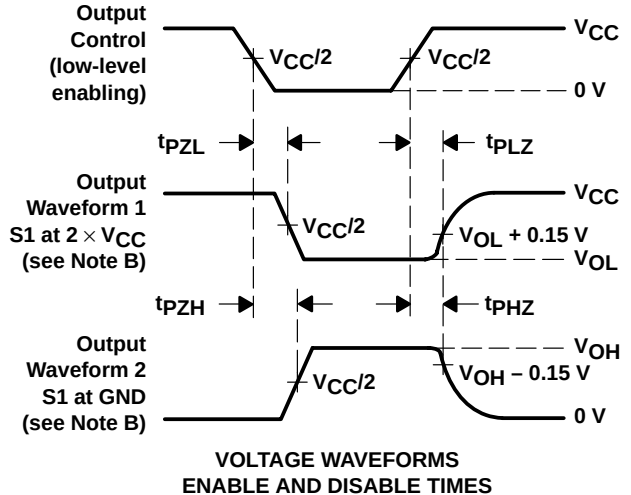
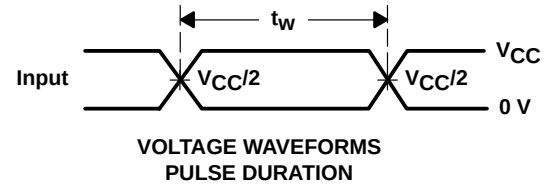
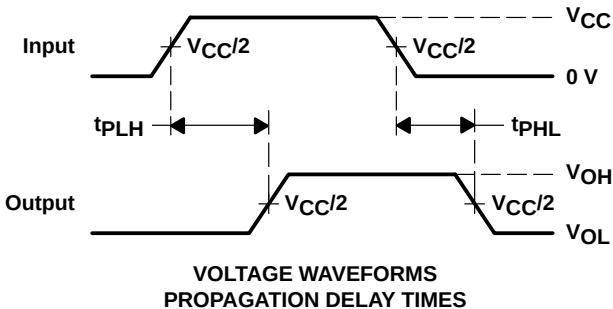
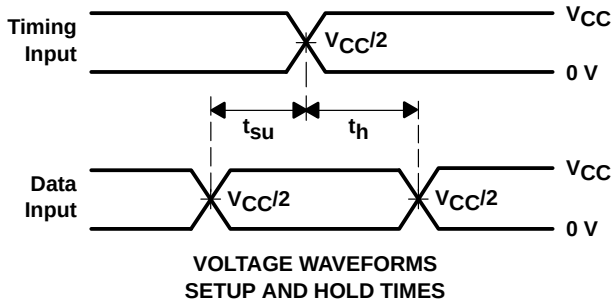
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN54LVC74A, SN74LVC74A

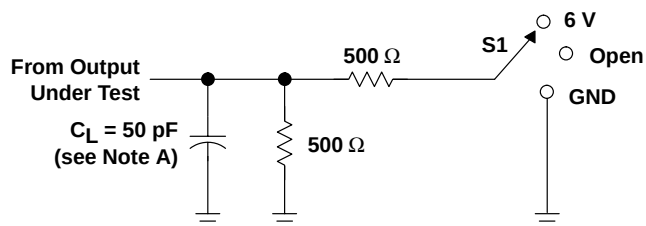
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH CLEAR AND PRESET

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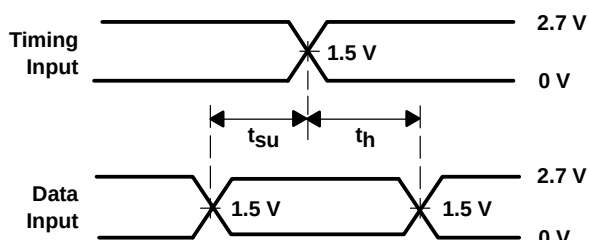
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$

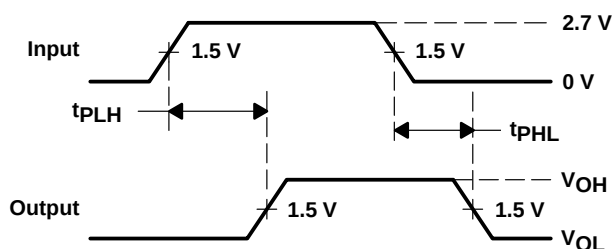


LOAD CIRCUIT

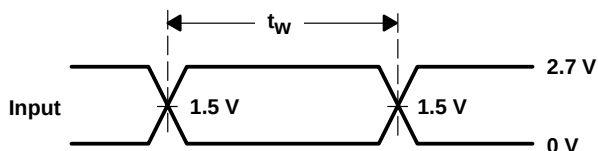
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



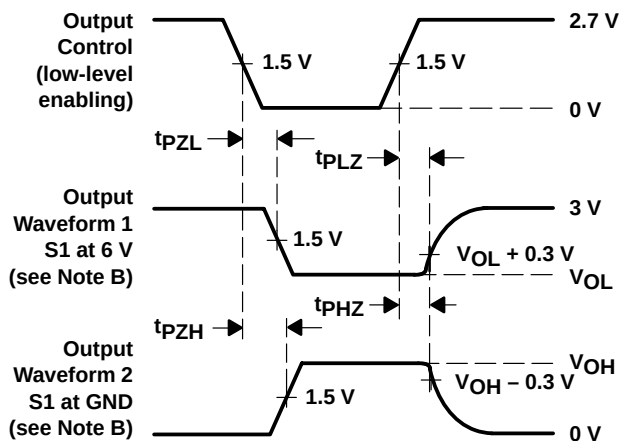
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC86A, SN74LVC86A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Package, Ceramic Chip Carriers (FK), and DIPs (J)

description

The SN54LVC86A quadruple 2-input exclusive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC86A quadruple 2-input exclusive-OR gate is designed for 1.65-V to 3.6-V V_{CC} operation.

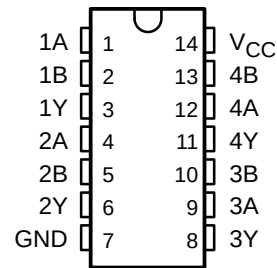
The 'LVC86A devices perform the Boolean function $Y = A \oplus B$ or $Y = \bar{A}B + A\bar{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

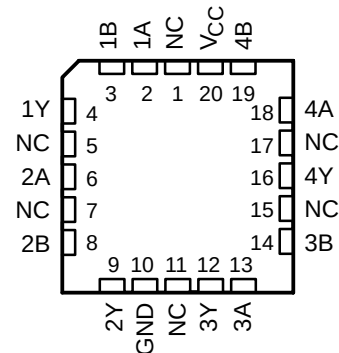
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC86A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC86A is characterized for operation from -40°C to 85°C .

SN54LVC86A . . . J OR W PACKAGE
SN74LVC86A . . . D, DB, DGV, OR PW PACKAGE
(TOP VIEW)



SN54LVC86A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



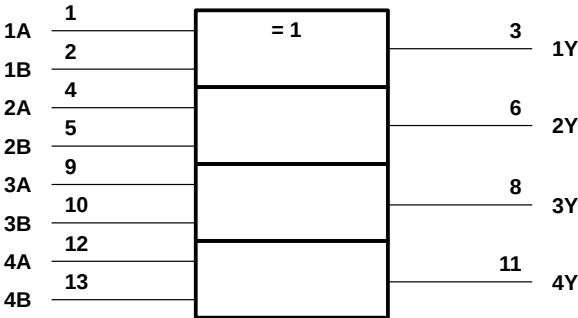
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVC86A, SN74LVC86A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

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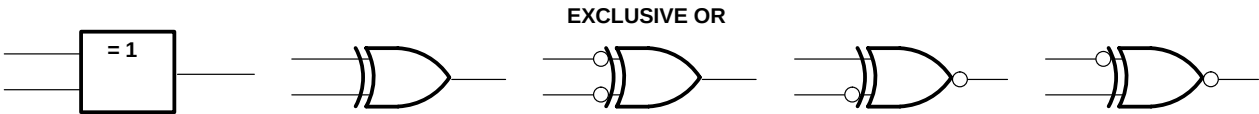
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, PW, and W packages.

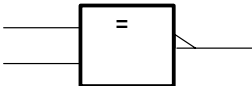
exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These five equivalent exclusive-OR symbols are valid for an SN74LVC86A gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



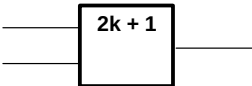
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LVC86A, SN74LVC86A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

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recommended operating conditions (see Note 4)

			SN54LVC86A		SN74LVC86A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		0.8		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V			−4		mA
		V _{CC} = 2.3 V			−8		
		V _{CC} = 2.7 V	−12		−12		
		V _{CC} = 3 V	−24		−24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V			4		mA
		V _{CC} = 2.3 V			8		
		V _{CC} = 2.7 V	12		12		
		V _{CC} = 3 V	24		24		
Δt/Δv	Input transition rise or fall rate		0	9	0	9	ns/V
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVC86A, SN74LVC86A

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC86A			SN74LVC86A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V				V _{CC} –0.2			V
		2.7 V to 3.6 V	V _{CC} –0.2						
	I _{OH} = –4 mA	1.65 V				1.2			
	I _{OH} = –8 mA	2.3 V				1.7			
	I _{OH} = –12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
	I _{OH} = –24 mA	3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.2			V
		2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA	1.65 V				0.45			
	I _{OL} = 8 mA	2.3 V				0.7			
	I _{OL} = 12 mA	2.7 V	0.4			0.4			
	I _{OL} = 24 mA	3 V	0.55			0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			10			μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND	3.3 V	5			5			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC86A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A	Y	5.6		1	4.6	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC86A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	‡	‡	‡	‡	5.6		1	4.6	ns
t _{sk(0)} [§]									1		ns

‡ This information was not available at the time of publication.

§ Skew between any two outputs of the same package switching in the same direction



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PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per gate	f = 10 MHz	†	†	8.5	pF

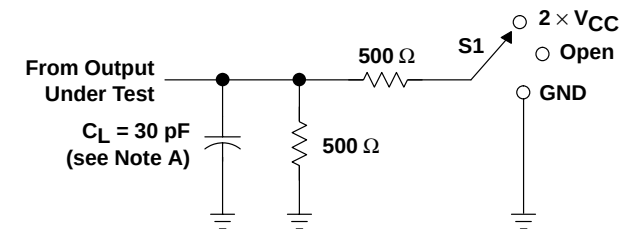
2-95

SN54LVC86A, SN74LVC86A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

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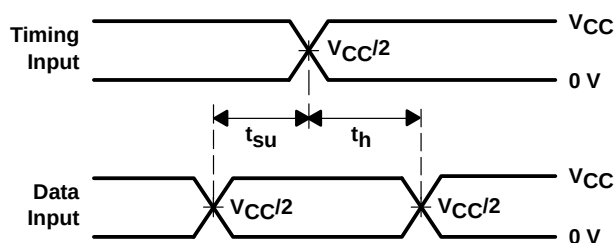
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

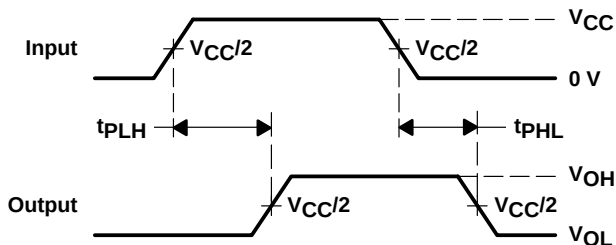


LOAD CIRCUIT

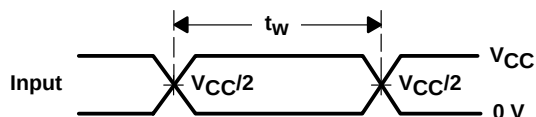
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



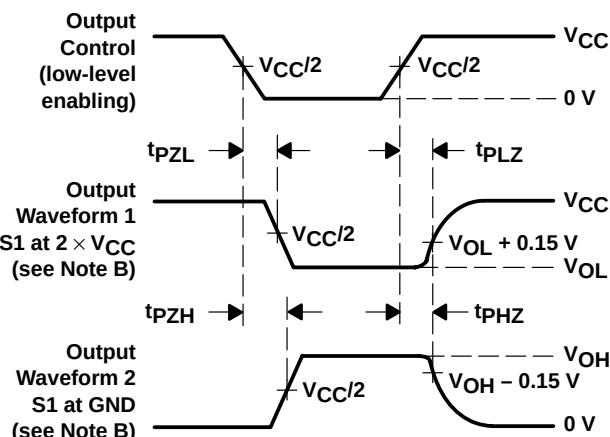
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



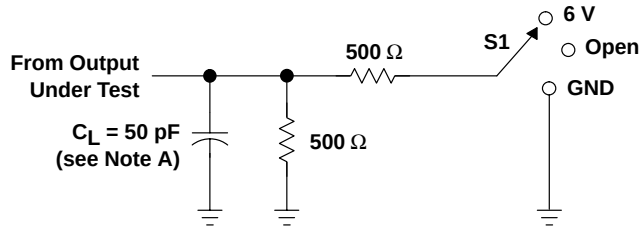
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

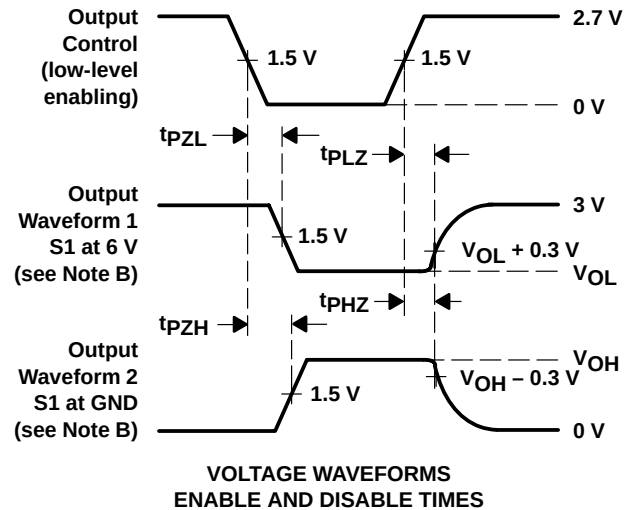
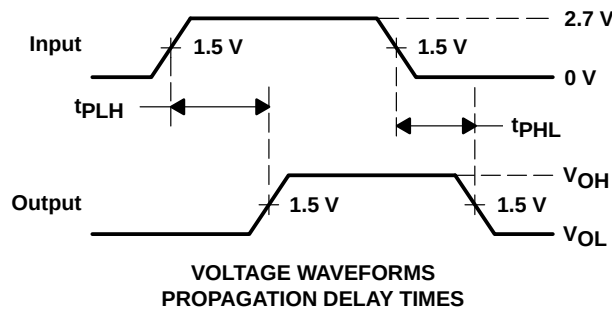
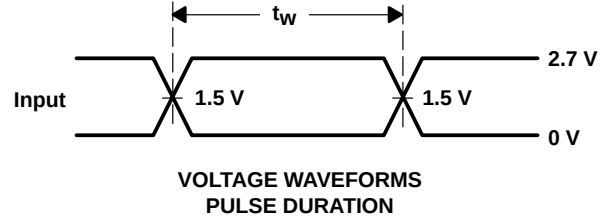
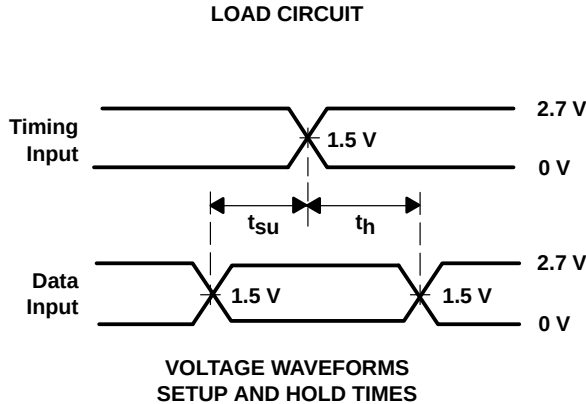
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

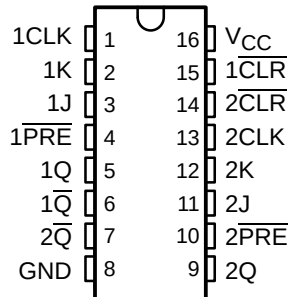
SN74LVC112A

DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

SCAS289F – JANUARY 1993 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Inputs Accept Voltages to 5.5 V**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

**D, DB, OR PW PACKAGE
(TOP VIEW)**



description

This dual negative-edge-triggered J-K flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the J and K inputs meeting the setup time requirements is transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and K inputs can be changed without affecting the levels at the outputs. The SN74LVC112A can perform as a toggle flip-flop by tying J and K high.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC112A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	K	Q	$\overline{\text{Q}}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	$H^\dagger$	$H^\dagger$
H	H	$\downarrow$	L	L	Q_0	$\overline{Q}_0$
H	H	$\downarrow$	H	L	H	L
H	H	$\downarrow$	L	H	L	H
H	H	$\downarrow$	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

† The output levels in this configuration may not meet the minimum levels for V_{OH} . Furthermore, this configuration is unstable; that is, it does not persist when either $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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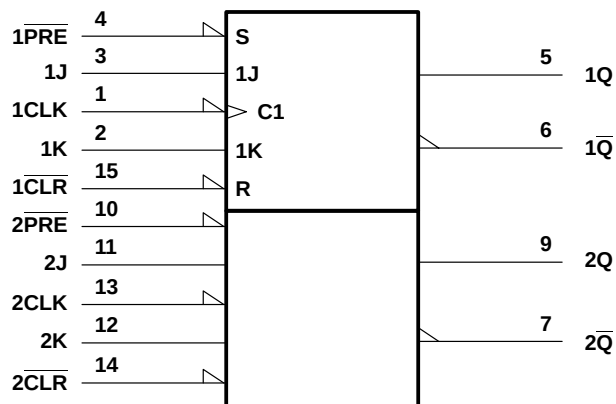
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SN74LVC112A

DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

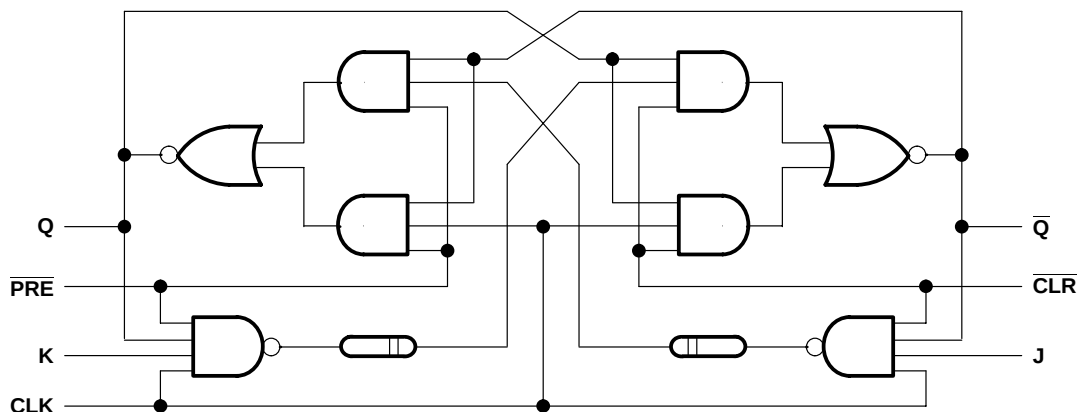
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)



SN74LVC112A

DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage		0	V_{CC}	V
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74LVC112A

DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP

WITH CLEAR AND PRESET

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V	V _{CC} –0.2			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
	I _{OL} = 4 mA	1.65 V			0.45	
	I _{OL} = 8 mA	2.3 V			0.7	
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = 5.5 V or GND	3.6 V			±5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			10	μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μA
C _i	V _I = V _{CC} or GND	3.3 V			4.5	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		‡		‡		150		150		MHz
t _w	Pulse duration, CLK high or low		‡		‡		3.3		3.3		ns
t _{su}	Setup time	Data before CLK↓	‡		‡		2.3		3.1		ns
		PRE or CLR inactive	‡		‡		1.1		2.4		
t _h	Hold time, data after CLK↓		‡		‡		0.7		2.5		ns

‡ This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	TYP	MAX	
f _{max}			‡		‡		150		150			MHz
t _{pd}	CLR or PRE	Q or $\bar{Q}$	‡	‡	‡	‡	5.5		1	3.4	4.8	ns
	CLK		‡	‡	‡	‡	7.1		1	3.5	5.9	

‡ This information was not available at the time of publication.



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DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

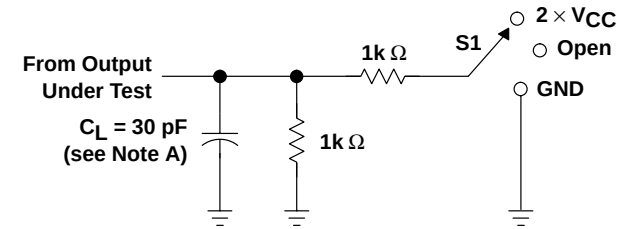
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operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
		TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per flip-flop	$f = 10\text{ MHz}$	†	†	24	pF

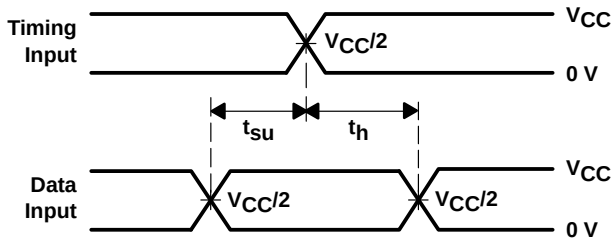
† This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$

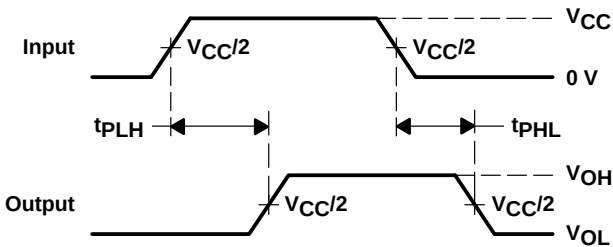


LOAD CIRCUIT

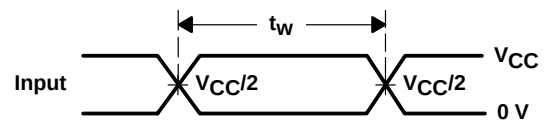
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



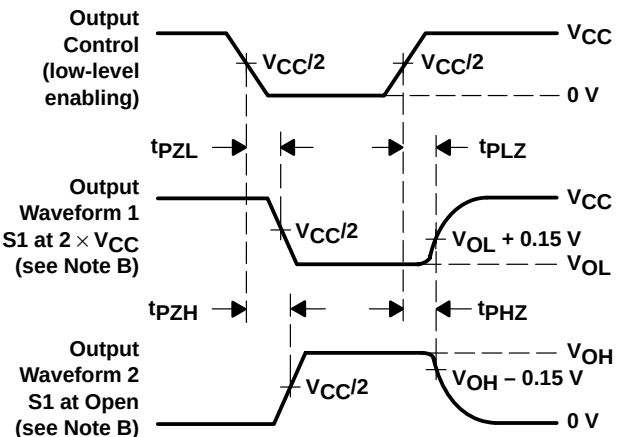
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



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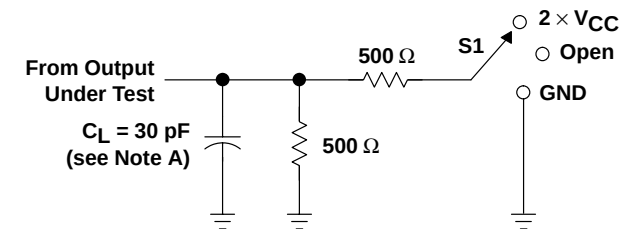
DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP

WITH CLEAR AND PRESET

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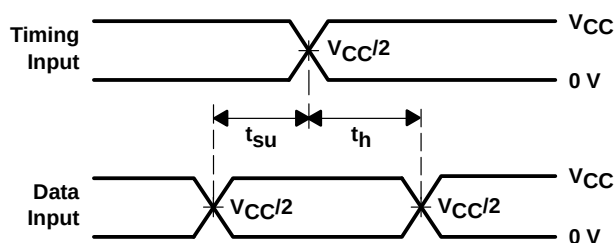
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

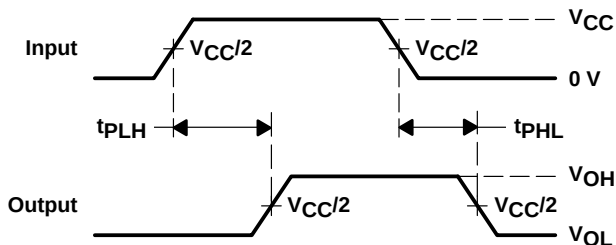


LOAD CIRCUIT

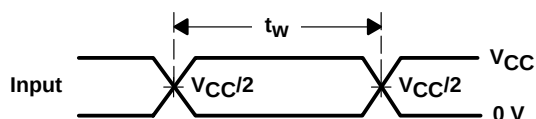
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



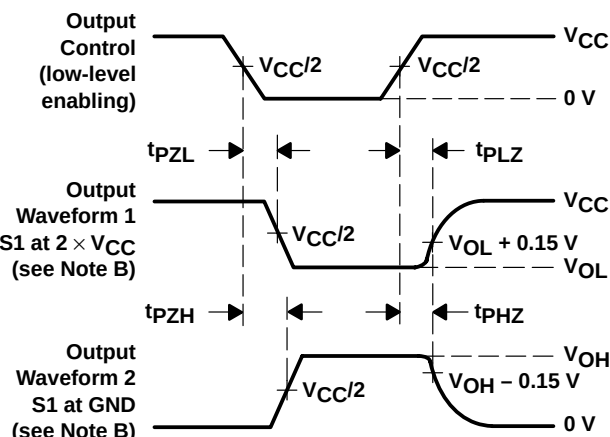
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

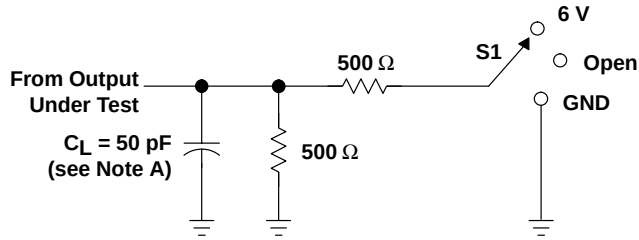
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DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

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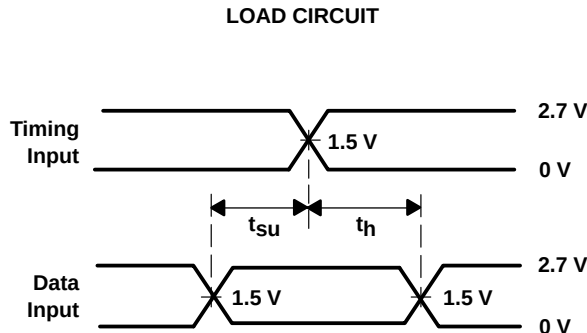
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$

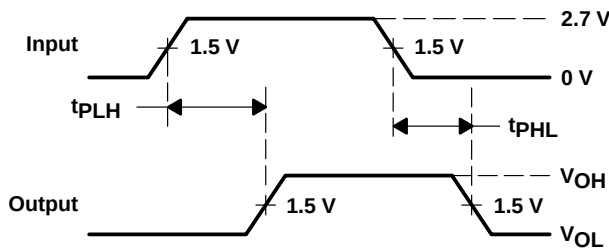


LOAD CIRCUIT

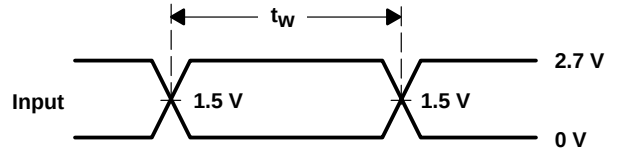
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



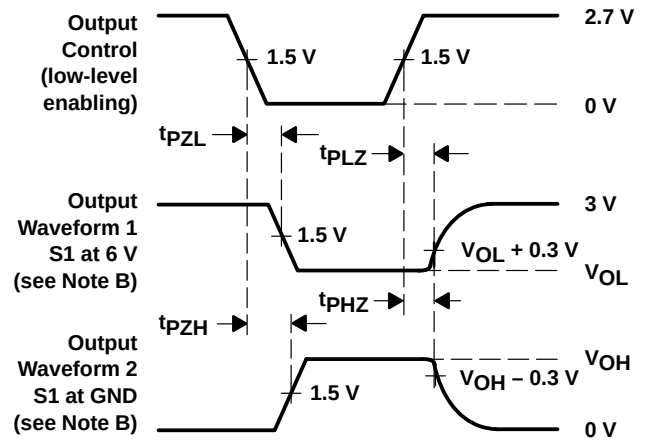
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

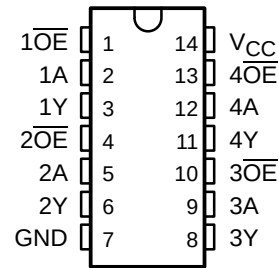
Figure 3. Load Circuit and Voltage Waveforms

SN74LVC125A QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple bus buffer gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC125A features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC125A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



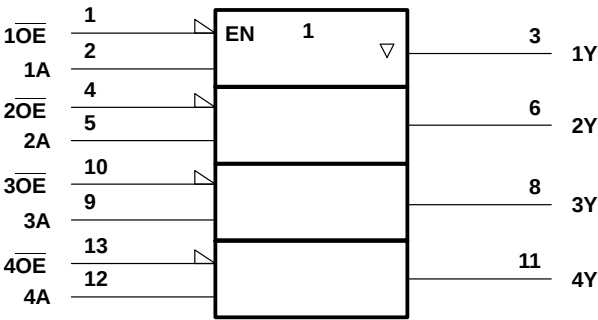
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SN74LVC125A
QUADRUPLE BUS BUFFER GATE
WITH 3-STATE OUTPUTS

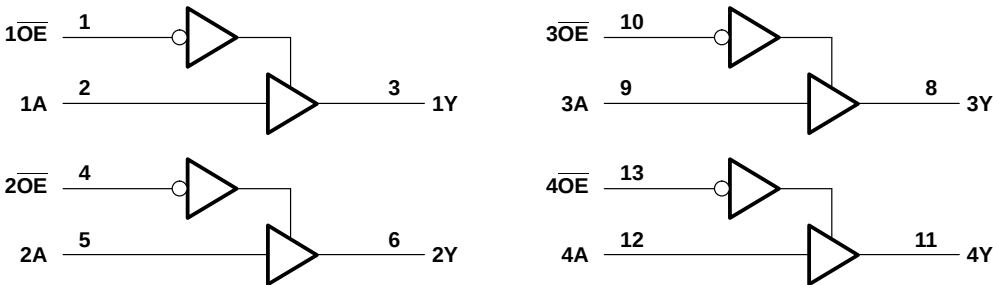
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	127°C/W
DB package	158°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stressratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

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QUADRUPLE BUS BUFFER GATE
WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	−4		mA
		V _{CC} = 2.3 V	−8		
		V _{CC} = 2.7 V	−12		
		V _{CC} = 3 V	−24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		mA
		V _{CC} = 2.3 V	8		
		V _{CC} = 2.7 V	12		
		V _{CC} = 3 V	24		
Δt/Δv	Input transition rise or fall rate		0	8	ns/V
T _A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = −100 μA	1.65 V to 3.6 V	V _{CC} −0.2			V
	I _{OH} = −4 mA	1.65 V	1.2			
	I _{OH} = −8 mA	2.3 V	1.7			
	I _{OH} = −12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = −24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
	I _{OL} = 4 mA	1.65 V			0.45	
	I _{OL} = 8 mA	2.3 V			0.7	
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = 5.5 V or GND	3.6 V			±5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			10	μA
ΔI _{CC}	One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μA
C _i	V _I = V _{CC} or GND	3.3 V			5	pF

[†] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.



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QUADRUPLE BUS BUFFER GATE

WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1	12.3	1	6.3	5.5		1	4.8	ns
t_{en}	$\overline{OE}$	Y	1	14.3	1	7.4	6.6		1	5.4	ns
t_{dis}	$\overline{OE}$	Y	1	11.1	1	5.6	5		1	4.6	ns
$t_{sk(o)}^{\dagger}$									1		ns

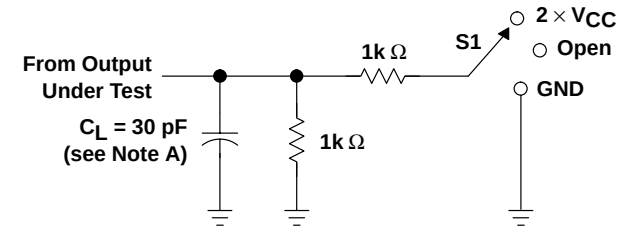
[†] Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per gate	$f = 10\text{ MHz}$	7.4	11.3	15	pF

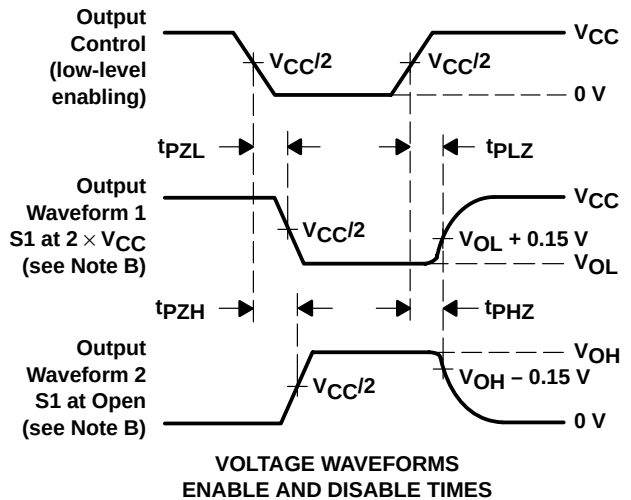
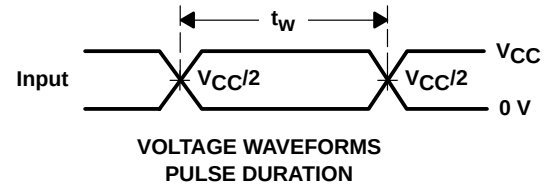
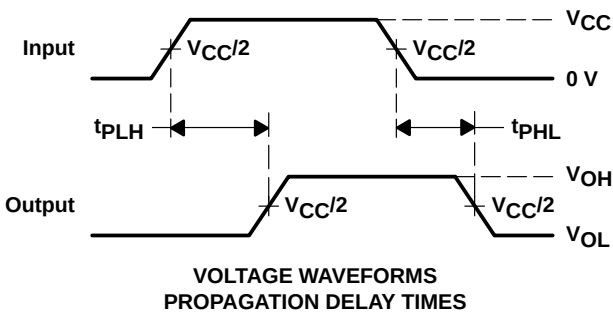
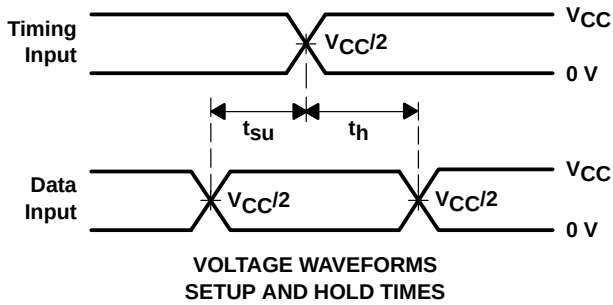


PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC125A

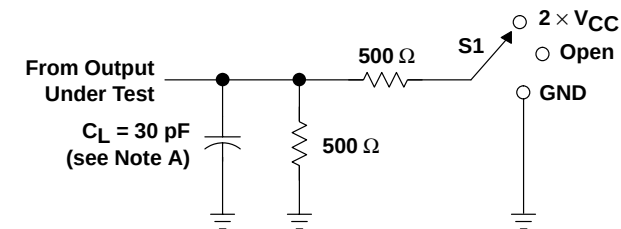
QUADRUPLE BUS BUFFER GATE

WITH 3-STATE OUTPUTS

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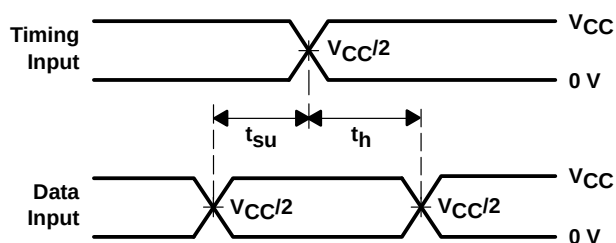
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

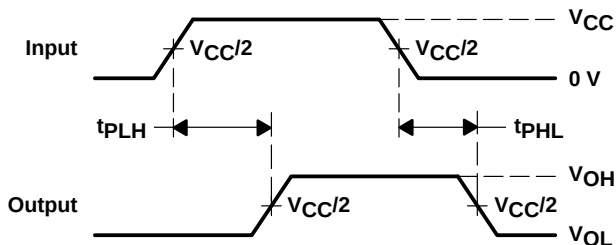


LOAD CIRCUIT

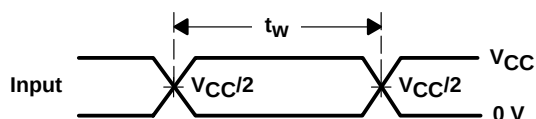
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



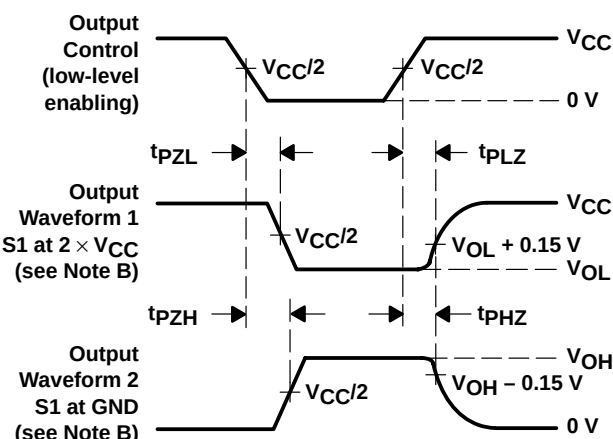
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

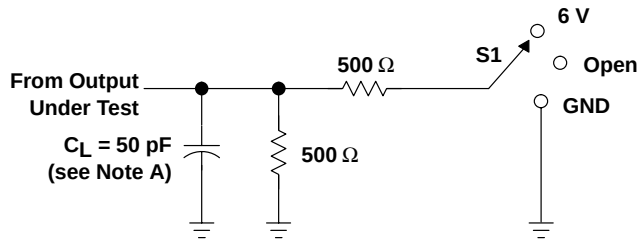


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

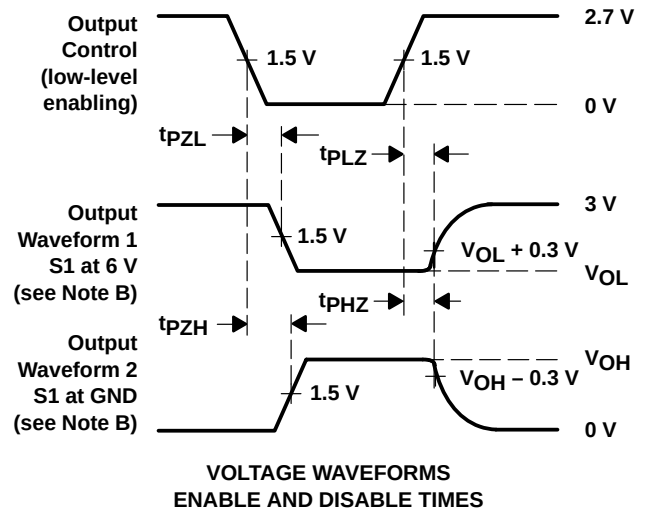
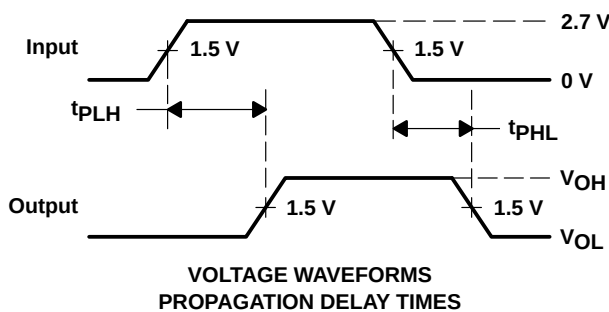
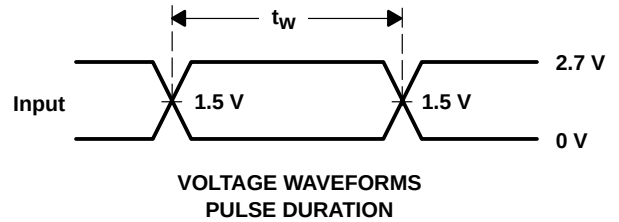
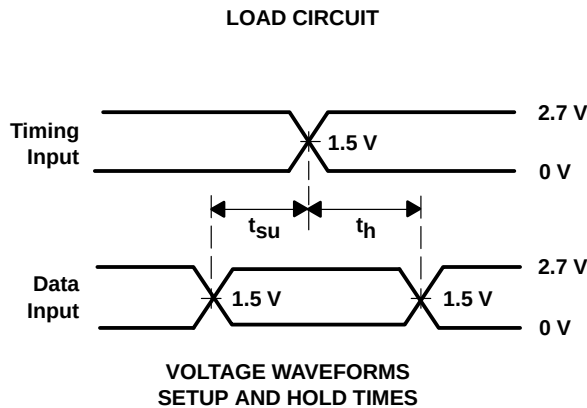
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

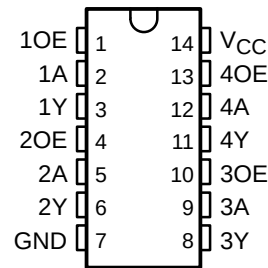
Figure 3. Load Circuit and Voltage Waveforms

SN74LVC126A QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

**D, DB, OR PW PACKAGE
(TOP VIEW)**



description

This quadruple bus buffer gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC126A features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC126A is characterized for operation from -40°C to 85°C .

**FUNCTION TABLE
(each buffer)**

INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	X	Z

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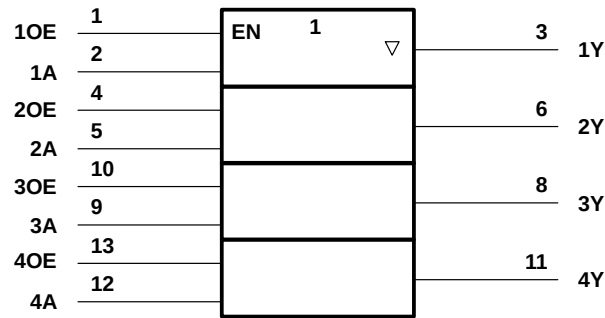
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SN74LVC126A
QUADRUPLE BUS BUFFER GATE
WITH 3-STATE OUTPUTS

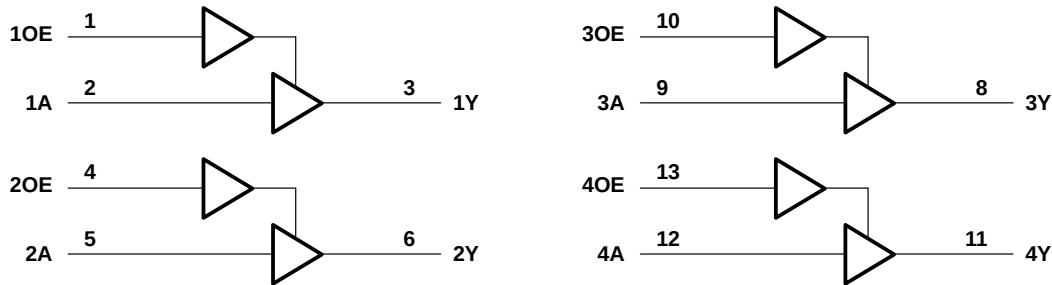
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN74LVC126A
QUADRUPLE BUS BUFFER GATE
WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	−4		mA
		V _{CC} = 2.3 V	−8		
		V _{CC} = 2.7 V	−12		
		V _{CC} = 3 V	−24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		mA
		V _{CC} = 2.3 V	8		
		V _{CC} = 2.7 V	12		
		V _{CC} = 3 V	24		
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T _A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = −100 μA	1.65 V to 3.6 V	V _{CC} −0.2		V	
	I _{OH} = −4 mA	1.65 V	1.2			
	I _{OH} = −8 mA	2.3 V	1.7			
	I _{OH} = −12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = −24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V	0.2		V	
	I _{OL} = 4 mA	1.65 V	0.45			
	I _{OL} = 8 mA	2.3 V	0.7			
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5		μA	
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±10		μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10		μA	
ΔI _{CC}	One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500		μA	
C _i	V _I = V _{CC} or GND	3.3 V	4.5		pF	
C _O	V _O = V _{CC} or GND	3.3 V	7		pF	

[†] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.



SN74LVC126A

QUADRUPLE BUS BUFFER GATE

WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	†	†	†	†	5.2		1	4.7	ns
t_{en}	OE	Y	†	†	†	†	6.3		1	5.7	ns
t_{dis}	OE	Y	†	†	†	†	6.7		1.3	6	ns
$t_{sk(o)}^{\ddagger}$									1		ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction.

operating characteristics, $T_A = 25^\circ\text{C}$

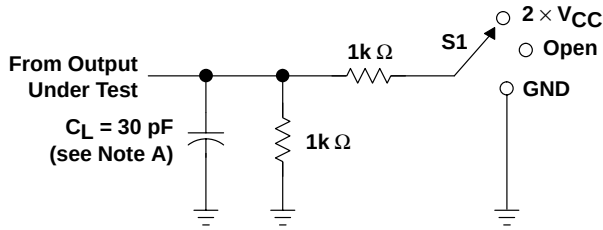
PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per gate	Outputs enabled	f = 10 MHz	†	†	22	pF
		Outputs disabled		†	†	4	

† This information was not available at the time of publication.



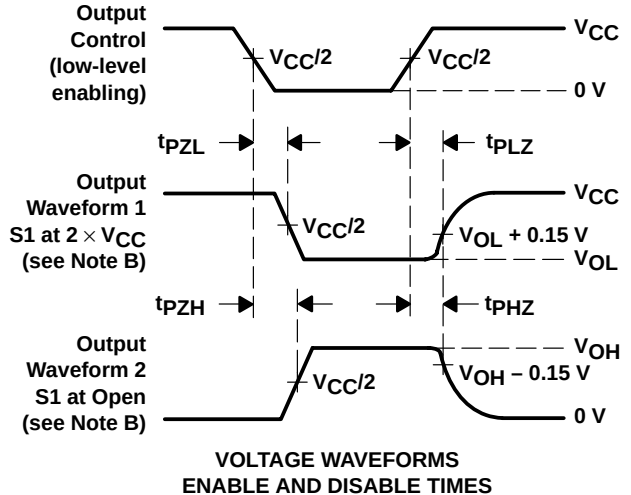
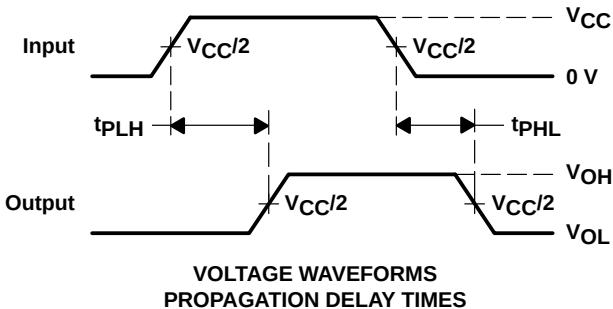
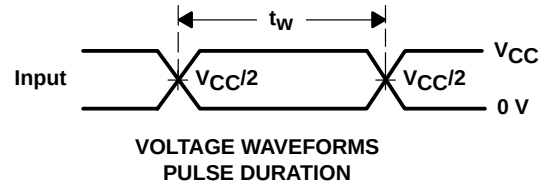
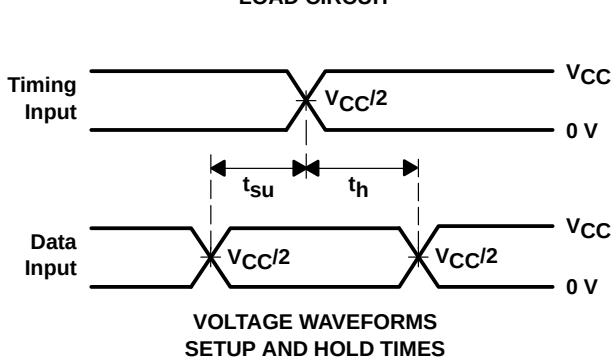
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC126A

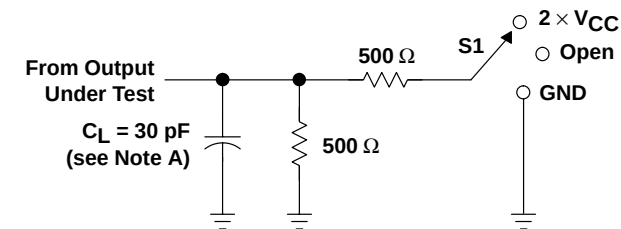
QUADRUPLE BUS BUFFER GATE

WITH 3-STATE OUTPUTS

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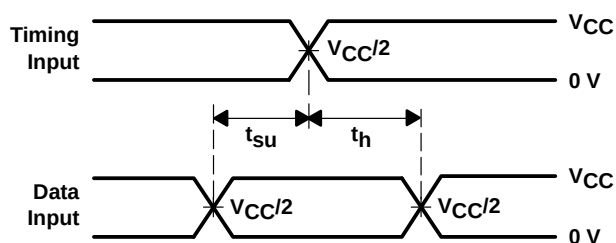
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

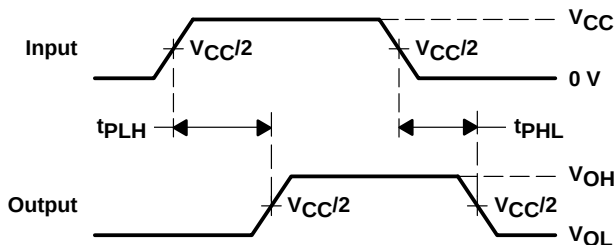


LOAD CIRCUIT

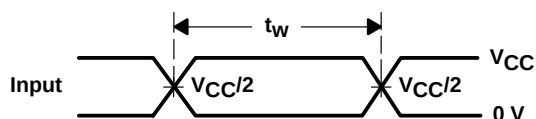
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



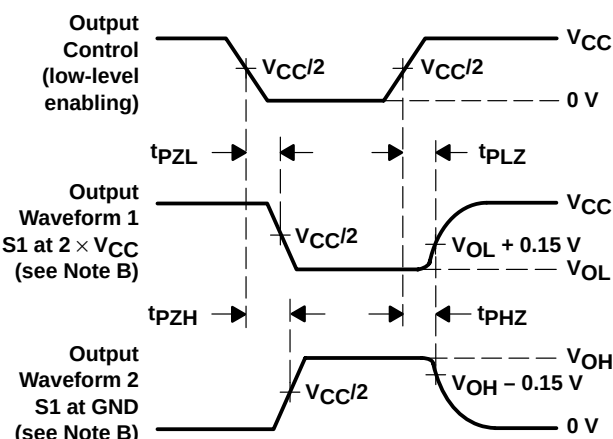
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



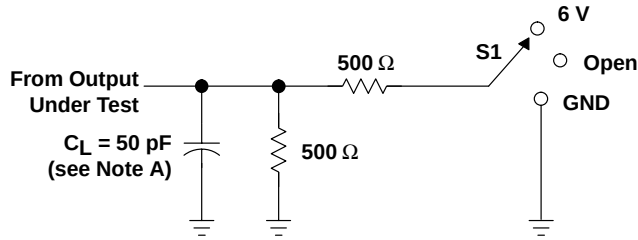
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

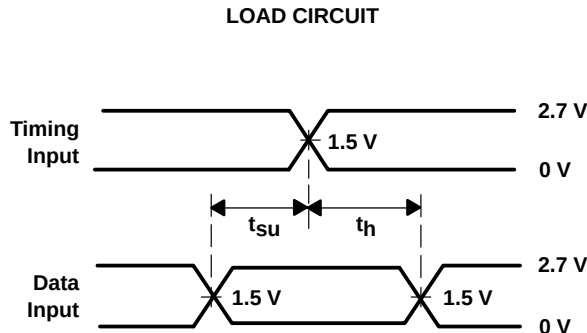
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$

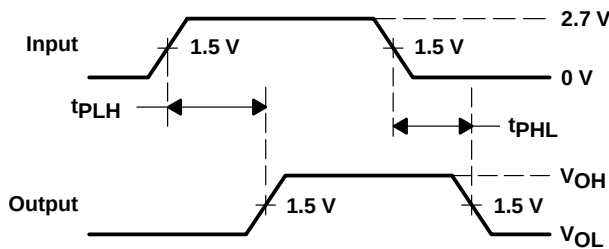


LOAD CIRCUIT

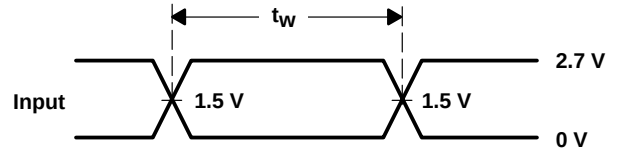
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



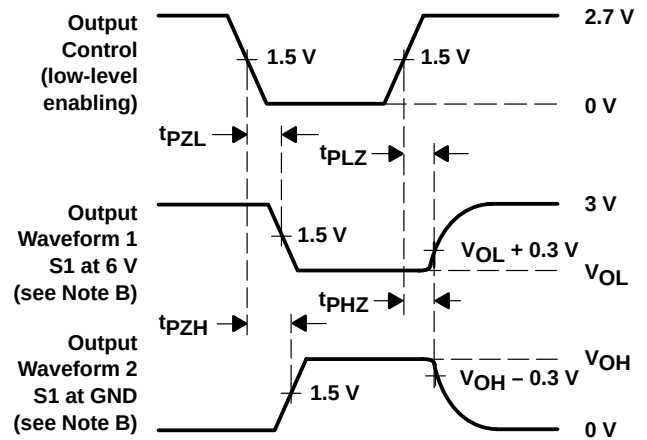
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

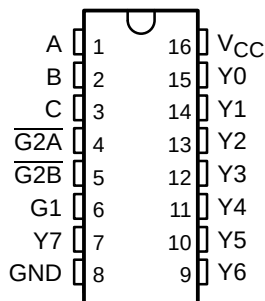
SN74LVC137A

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This 3-line to 8-line decoder/demultiplexer with latches on three address inputs is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC137A is designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

When the latch-enable ($\overline{G2A}$) input is low, the SN74LVC137A acts as a decoder/demultiplexer. When $\overline{G2A}$ transitions from low to high, the address present at the inputs (A, B, and C) is stored in the latches. Further address changes are ignored, provided $\overline{G2A}$ remains high. The output-enable (G1 and $\overline{G2B}$) inputs control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{G2B}$ is high.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC137A is characterized for operation from -40°C to 85°C .

PRODUCT PREVIEW

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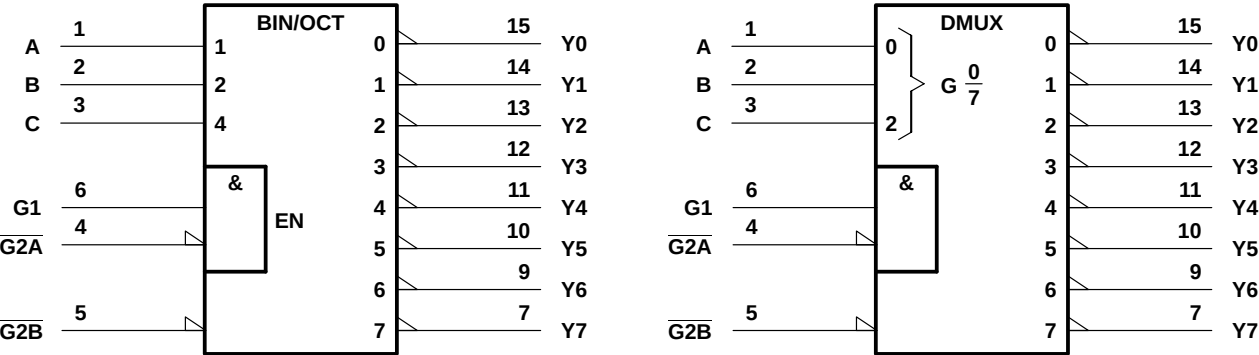
SN74LVC137A
3-LINE TO 8-LINE DECODER/DEMULTIPLEXER
WITH ADDRESS LATCHES

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FUNCTION TABLE

INPUTS						OUTPUTS							
LATCH ENABLE	OUTPUT ENABLE		SELECT										
G2A	G1	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Outputs corresponding to stored address = L; all other outputs = H							

logic symbols (alternatives)[†]



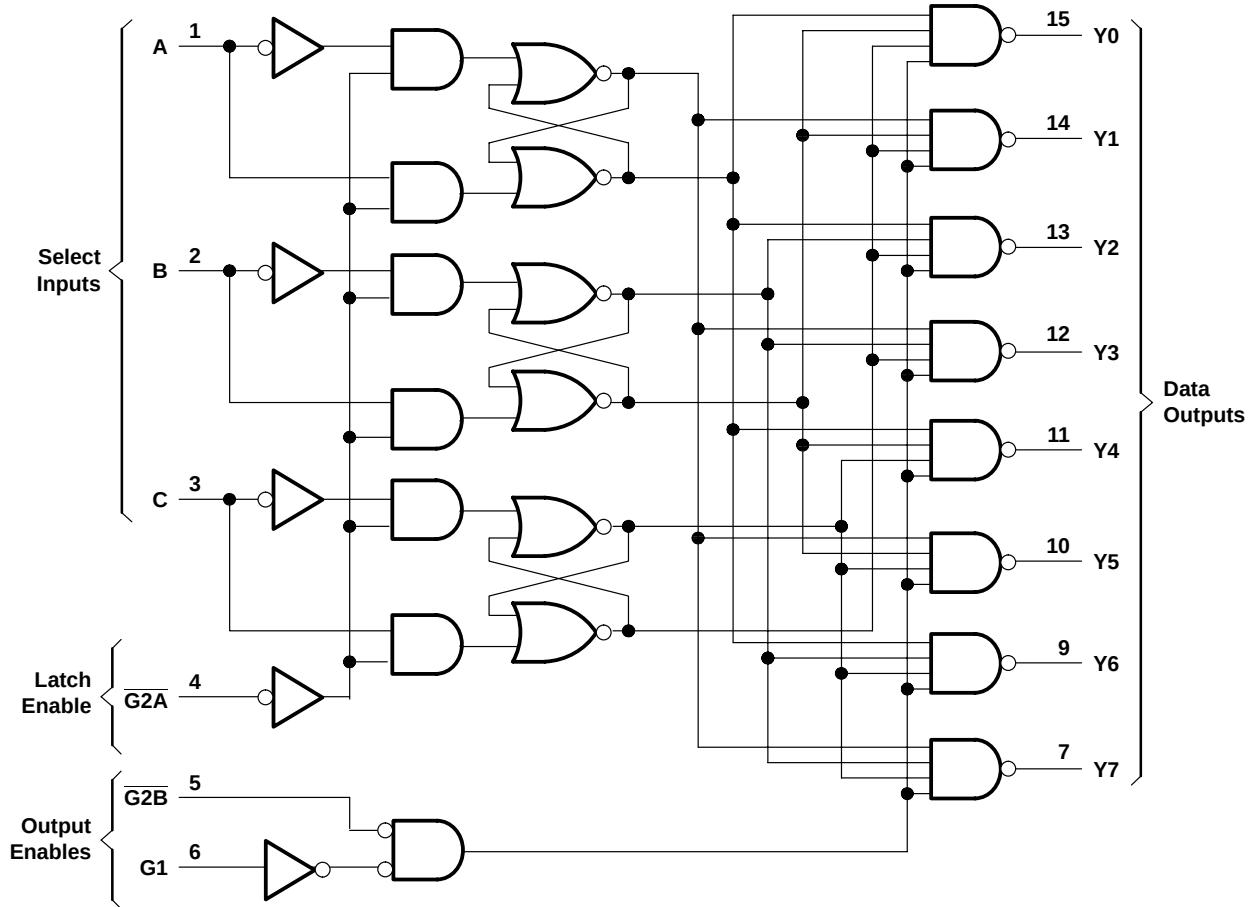
[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LVC137A

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	113°C/W
DB package	131°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

PRODUCT PREVIEW



SN74LVC137A 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7		
	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7		
	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0.8		
V_I Input voltage		0	5.5	V
V_O Output voltage		0	V_{CC}	V
I_{OH} High-level output current	$V_{CC} = 1.65\text{ V}$		–4	mA
	$V_{CC} = 2.3\text{ V}$		–8	
	$V_{CC} = 2.7\text{ V}$		–12	
	$V_{CC} = 3\text{ V}$		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65\text{ V}$		4	mA
	$V_{CC} = 2.3\text{ V}$		8	
	$V_{CC} = 2.7\text{ V}$		12	
	$V_{CC} = 3\text{ V}$		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP [†]	MAX	UNIT
V_{OH}	$I_{OH} = -100\text{ }\mu\text{A}$	1.65 V to 3.6 V	$V_{CC}-0.2$			V
	$I_{OH} = -4\text{ mA}$	1.65 V	1.2			
	$I_{OH} = -8\text{ mA}$	2.3 V	1.7			
	$I_{OH} = -12\text{ mA}$	2.7 V	2.2			
		3 V	2.4			
	$I_{OH} = -24\text{ mA}$	3 V	2.2			
V_{OL}	$I_{OL} = 100\text{ }\mu\text{A}$	1.65 V to 3.6 V			0.2	V
	$I_{OL} = 4\text{ mA}$	1.65 V			0.45	
	$I_{OL} = 8\text{ mA}$	2.3 V			0.7	
	$I_{OL} = 12\text{ mA}$	2.7 V			0.4	
	$I_{OL} = 24\text{ mA}$	3 V			0.55	
I_I	$V_I = 5.5\text{ V or GND}$	3.6 V			± 5	μA
I_{CC}	$V_I = V_{CC}\text{ or GND, } I_O = 0$	3.6 V			10	μA
ΔI_{CC}	One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$	2.7 V to 3.6 V			500	μA
C_i	$V_I = V_{CC}\text{ or GND}$	3.3 V				pF
C_o	$V_O = V_{CC}\text{ or GND}$	3.3 V				pF

[†] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.



SN74LVC137A
3-LINE TO 8-LINE DECODER/DEMULTIPLEXER
WITH ADDRESS LATCHES

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B or C	Y									ns
	$\overline{G2A}$ or $\overline{G2B}$										
	G1										
$t_{sk(o)}^{\dagger}$											ns

[†] Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$				pF

PRODUCT PREVIEW



SN74LVC137A

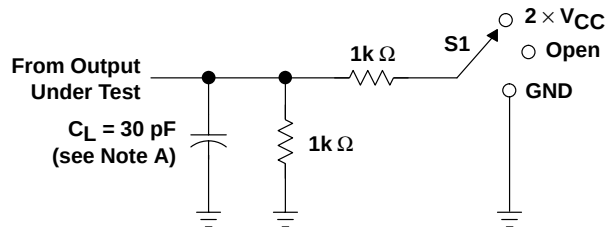
3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

WITH ADDRESS LATCHES

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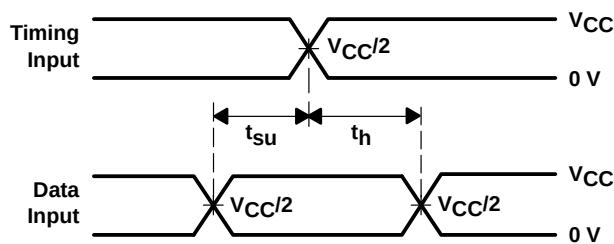
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

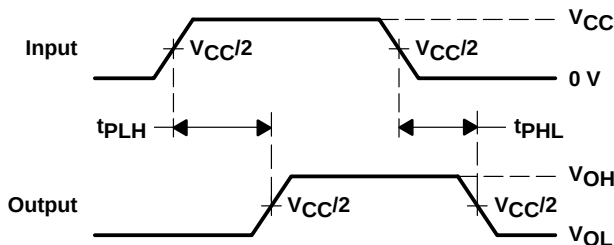


LOAD CIRCUIT

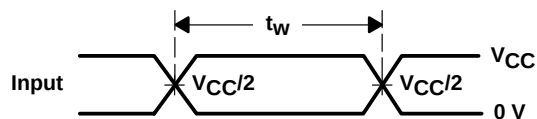
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



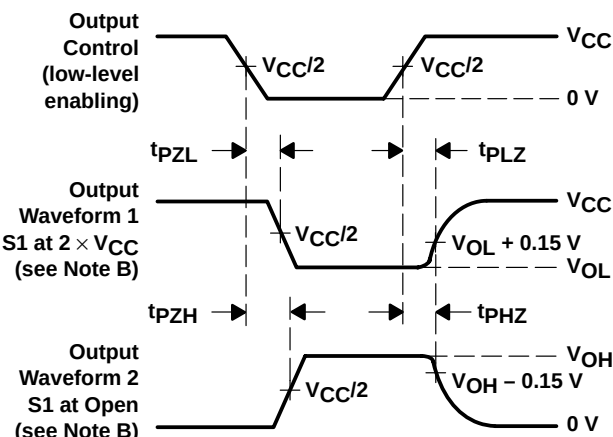
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

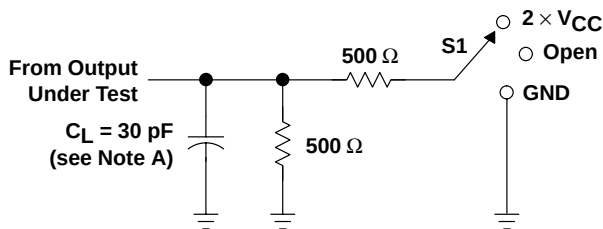
SN74LVC137A

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

SCAS340E – MARCH 1994 – REVISED JUNE 1998

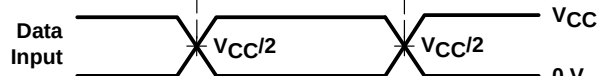
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

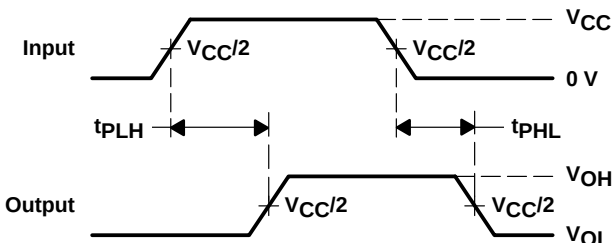


LOAD CIRCUIT

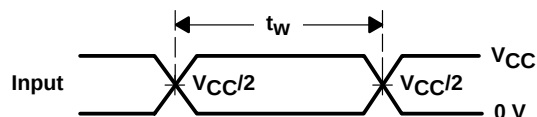
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



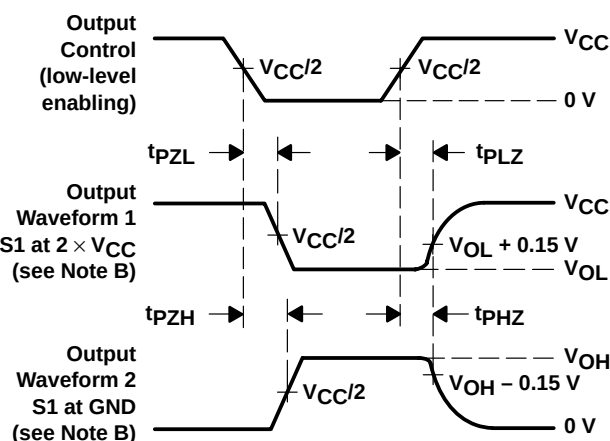
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

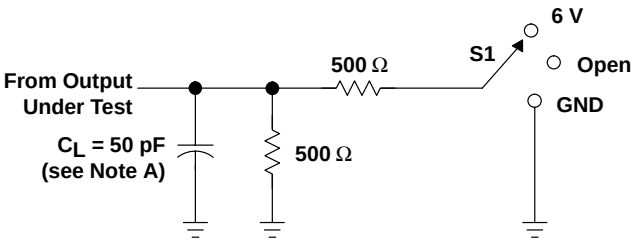
Figure 2. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SN74LVC137A
3-LINE TO 8-LINE DECODER/DEMULTIPLEXER
WITH ADDRESS LATCHES

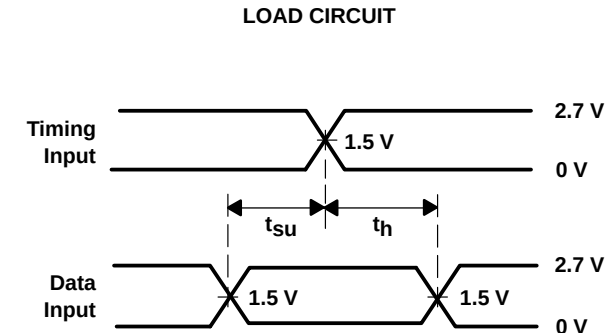
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PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

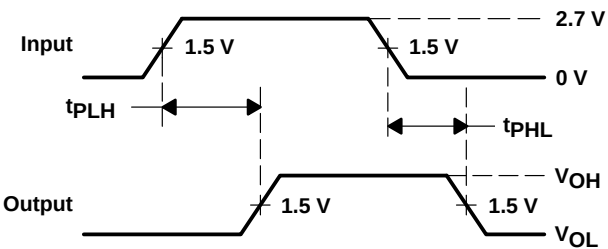


LOAD CIRCUIT

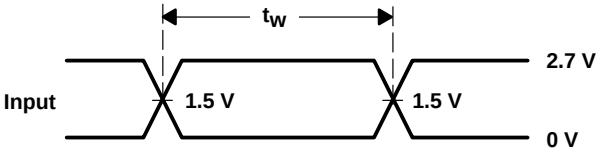
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



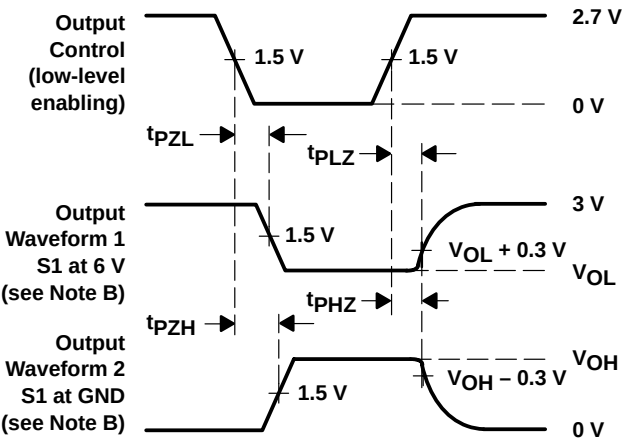
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC138A, SN74LVC138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Inputs Accept Voltages to 5.5 V**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flat (W) Package, and DIPs (J)**

description

The SN54LVC138A 3-line to 8-line decoder/demultiplexer is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC138A 3-line to 8-line decoder/demultiplexer is designed for 1.65-V to 3.6-V V_{CC} operation.

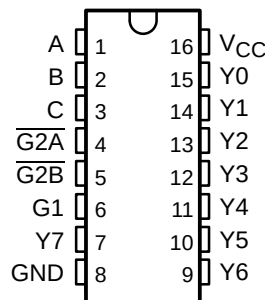
The 'LVC138A devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low enable inputs and one active-high enable input reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

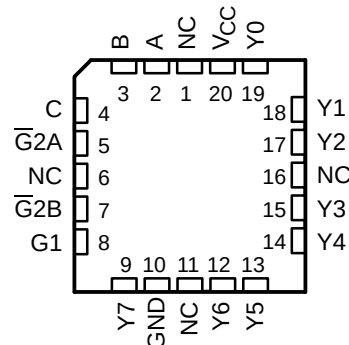
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC138A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC138A is characterized for operation from -40°C to 85°C .

SN54LVC138A . . . J OR W PACKAGE
SN74LVC138A . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LVC138A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

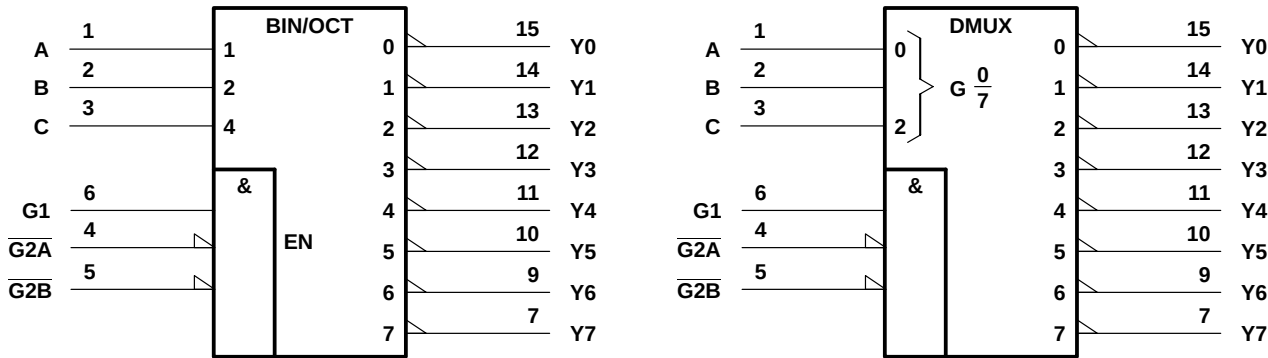
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3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

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FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

logic symbols (alternatives)[†]

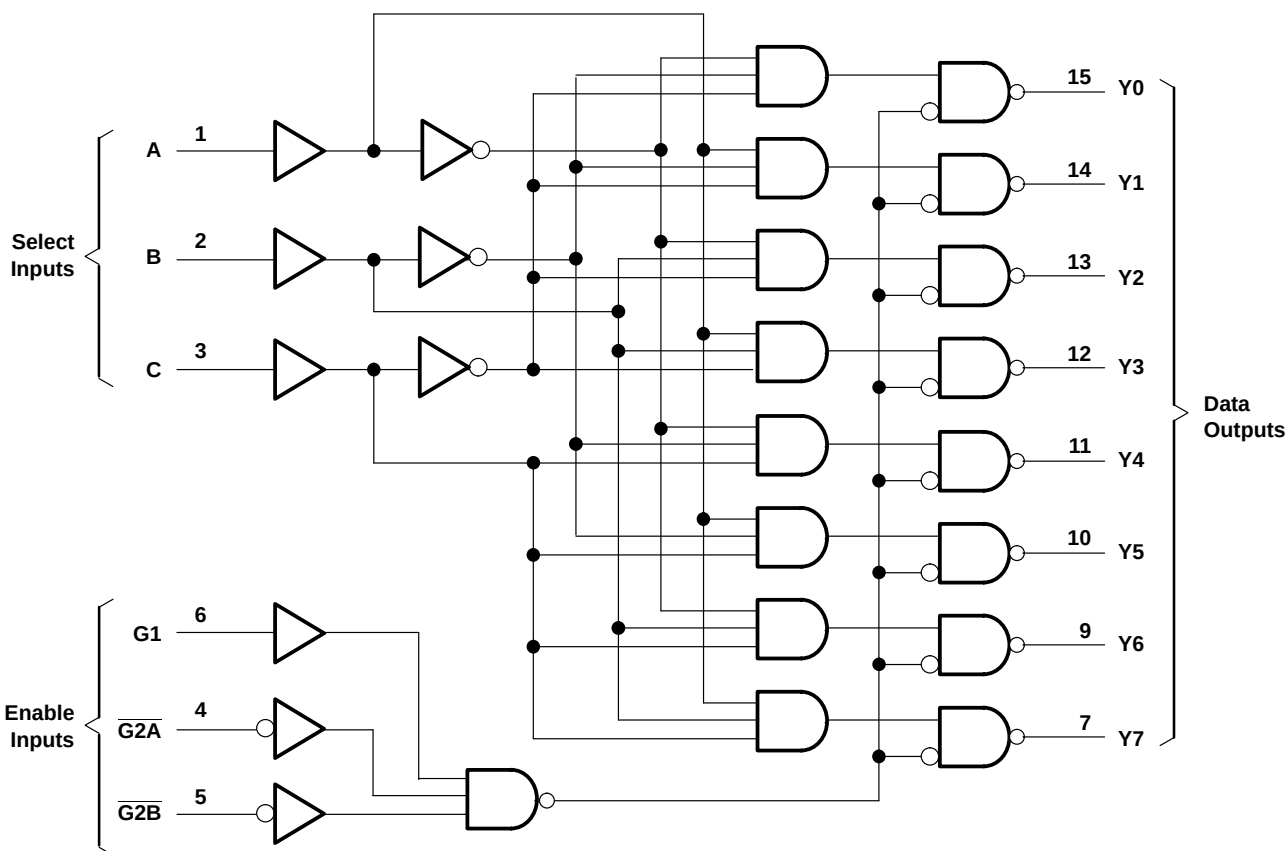


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, PW, and W packages.

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logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LVC138A, SN74LVC138A

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

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recommended operating conditions (see Note 4)

		SN54LVC138A		SN74LVC138A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC} Supply voltage	Operating	2	3.6	1.65	3.6	V
	Data retention only	1.5		1.5		
V _{IH} High-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.65 × V _{CC}		V
	V _{CC} = 2.3 V to 2.7 V			1.7		
	V _{CC} = 2.7 V to 3.6 V	2		2		
V _{IL} Low-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.35 × V _{CC}		V
	V _{CC} = 2.3 V to 2.7 V			0.7		
	V _{CC} = 2.7 V to 3.6 V		0.8	0.8		
V _I Input voltage		0	5.5	0	5.5	V
V _O Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH} High-level output current	V _{CC} = 1.65 V			–4		mA
	V _{CC} = 2.3 V			–8		
	V _{CC} = 2.7 V		–12	–12		
	V _{CC} = 3 V		–24	–24		
I _{OL} Low-level output current	V _{CC} = 1.65 V			4		mA
	V _{CC} = 2.3 V			8		
	V _{CC} = 2.7 V		12	12		
	V _{CC} = 3 V		24	24		
Δt/Δv Input transition rise or fall rate		0	10	0	10	ns/V
T _A Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC138A			SN74LVC138A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V				V _{CC} –0.2			V
		2.7 V to 3.6 V	V _{CC} –0.2						
	I _{OH} = –4 mA	1.65 V				1.2			
	I _{OH} = –8 mA	2.3 V				1.7			
	I _{OH} = –12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
	I _{OH} = –24 mA	3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.2			V
		2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA	1.65 V				0.45			
	I _{OL} = 8 mA	2.3 V				0.7			
	I _{OL} = 12 mA	2.7 V	0.4			0.4			
	I _{OL} = 24 mA	3 V	0.55			0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			10			μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND	3.3 V	5			5			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC138A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A or B or C	Y	7.9		1	6.7	ns
	G2A or G2B		7.4		1	6.5	
	G1		6.4		1	5.8	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC138A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B or C	Y	‡	‡	‡	‡	7.9	1	6.7	ns	
	G2A or G2B		‡	‡	‡	‡	7.4	1	6.5		
	G1		‡	‡	‡	‡	6.4	1	5.8		
t _{sk(o)} [§]								1	ns		

‡ This information was not available at the time of publication.

§ Skew between any two outputs of the same package switching in the same direction



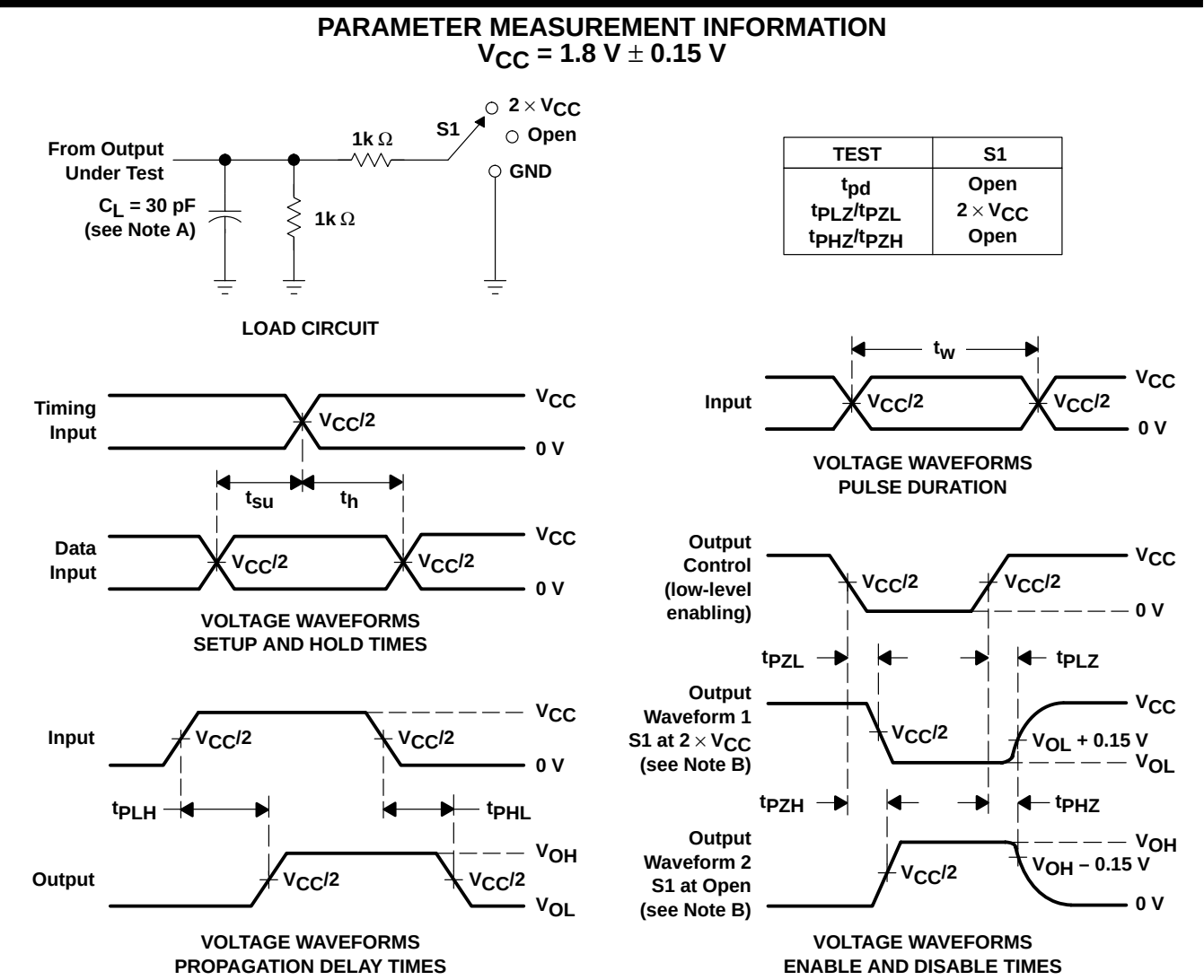
SN54LVC138A, SN74LVC138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

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operating characteristics, $T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
		TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	$f = 10\text{ MHz}$	†	†	27	pF

† This information was not available at the time of publication.

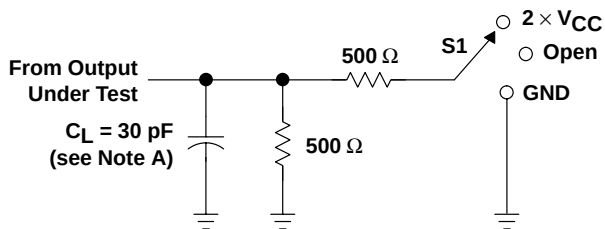


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

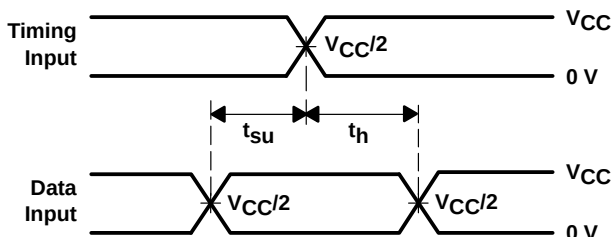
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

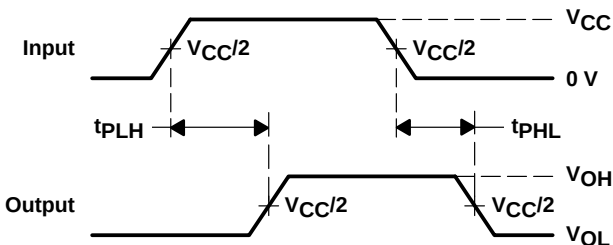


LOAD CIRCUIT

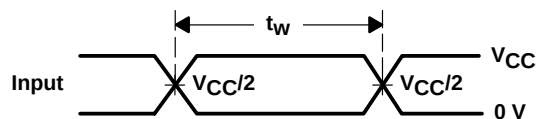
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHZ}	GND



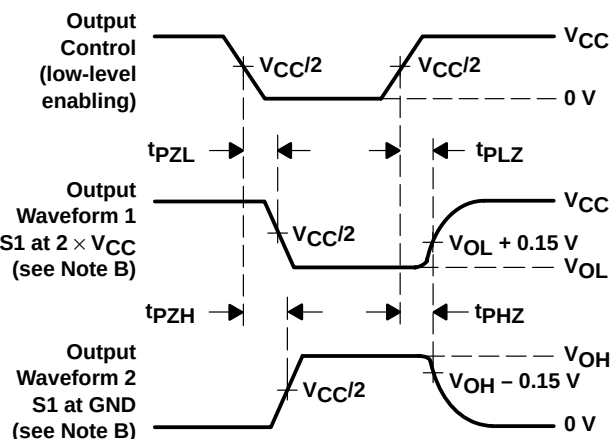
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

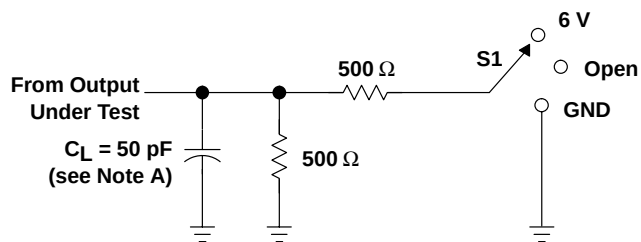
SN54LVC138A, SN74LVC138A

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

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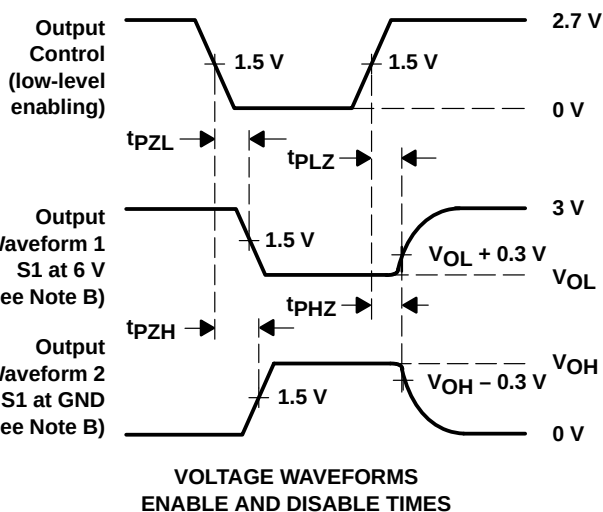
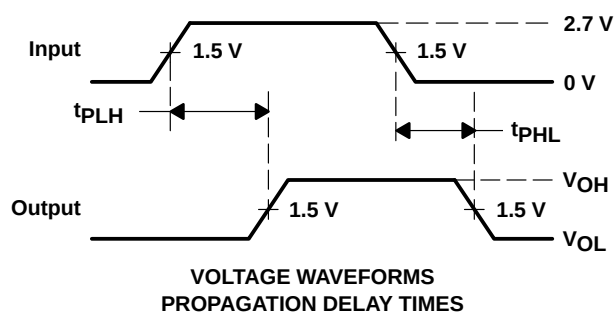
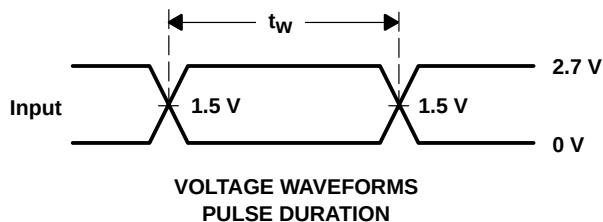
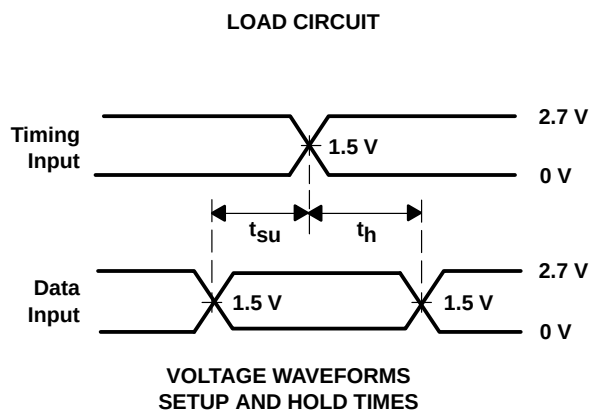
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

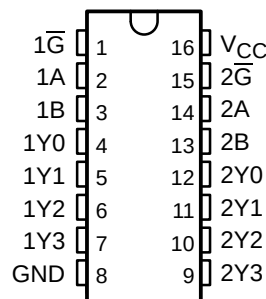
SN74LVC139A

DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

SCAS341F – MARCH 1994 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Inputs Accept Voltages to 5.5 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This dual 2-line to 4-line decoder/demultiplexer is designed for 1.65-V to 3.6-V V_{CC} operation.

The device comprises two individual 2-line to 4-line decoders in a single package. The active-low enable ($\overline{G}$) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC139A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each decoder/demultiplexer)

INPUTS			OUTPUTS			
$\overline{G}$	SELECT					
	B	A	Y3	Y2	Y1	Y0
L	L	L	H	H	H	L
L	L	H	H	H	L	H
L	H	L	H	L	H	H
L	H	H	L	H	H	H
H	X	X	H	H	H	H

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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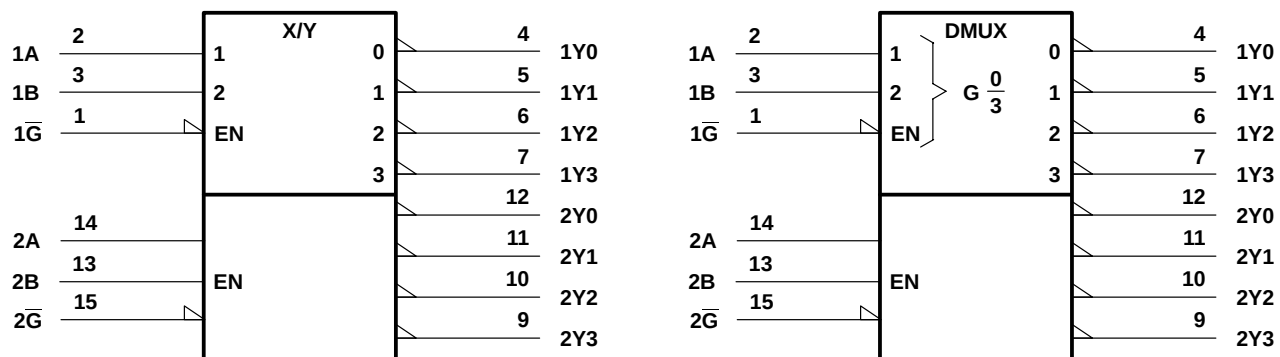
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SN74LVC139A

DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

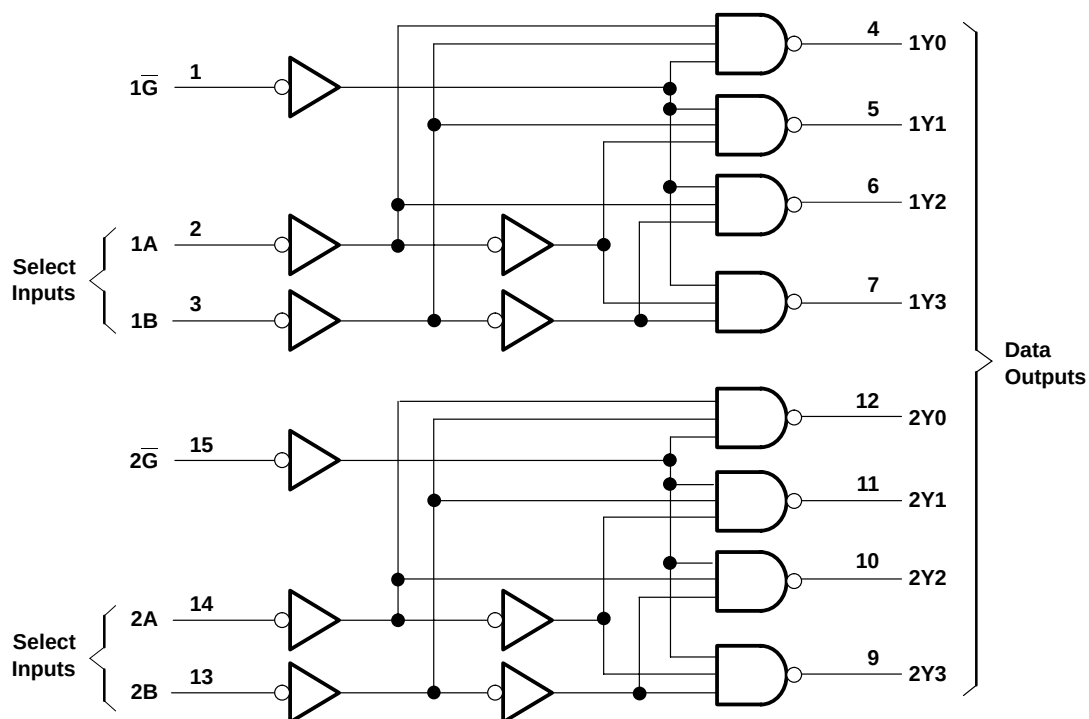
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logic symbols (alternatives)[†]



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC139A

DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage		0	V_{CC}	V
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 4 mA	1.65 V	0.45			
	I _{OL} = 8 mA	2.3 V	0.7			
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5			µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			µA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			µA
C _i	V _I = V _{CC} or GND	3.3 V	5			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	‡	‡	‡	‡	7.3		1	6.2	ns
	$\overline{G}$		‡	‡	‡	‡	5.2		1	4.7	
t _{sk(o)} [§]									1		ns

[‡] This information was not available at the time of publication.

[§] Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

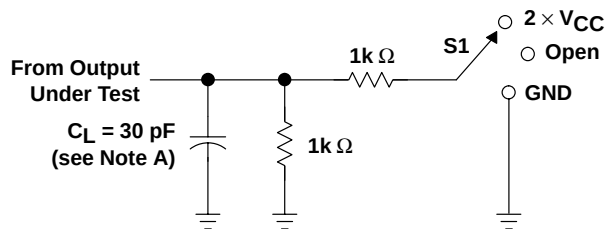
PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
		TYP	TYP	TYP	
C _{pd} Power dissipation capacitance	f = 10 MHz	‡	‡	30.5	pF

[‡] This information was not available at the time of publication.



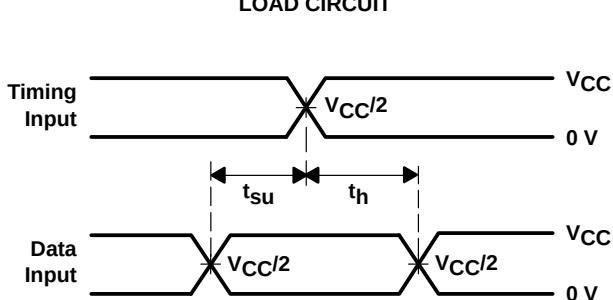
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

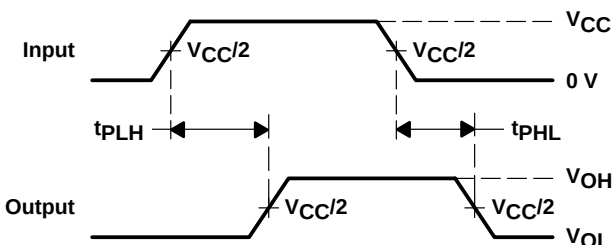


LOAD CIRCUIT

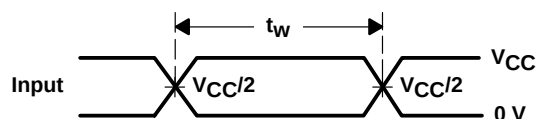
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



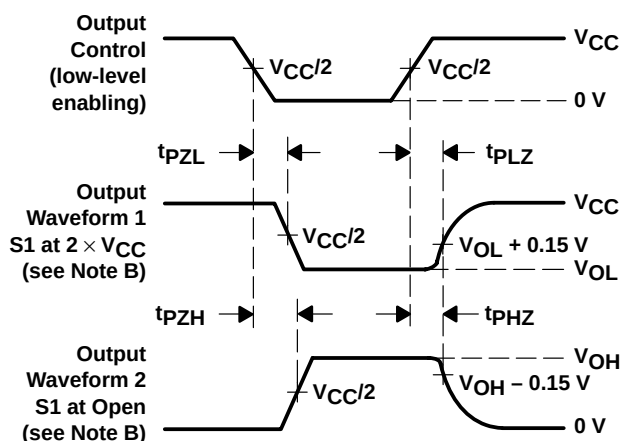
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

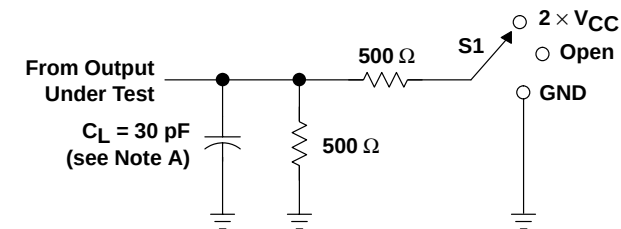
SN74LVC139A

DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

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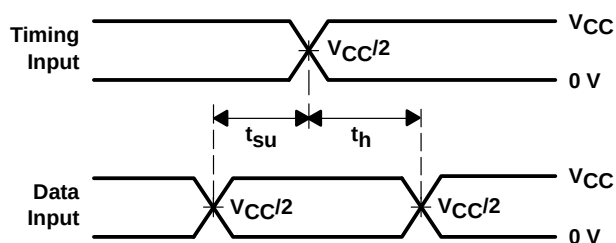
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

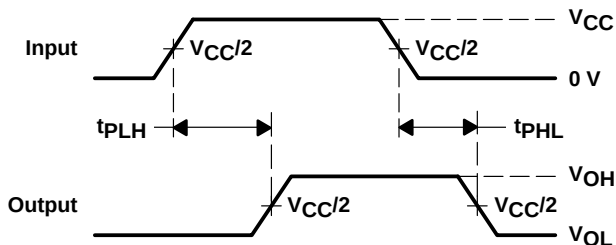


LOAD CIRCUIT

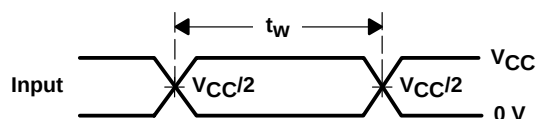
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



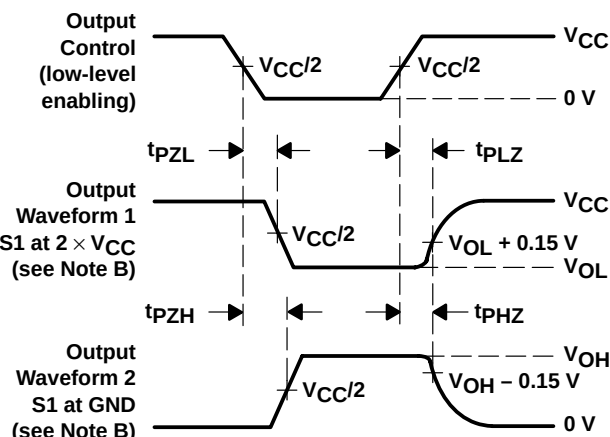
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



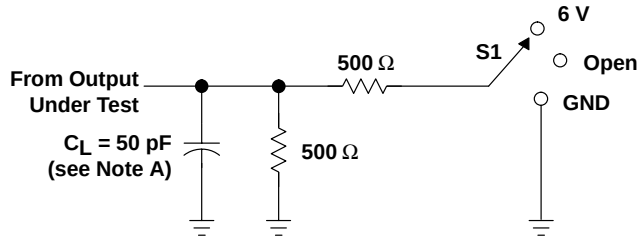
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

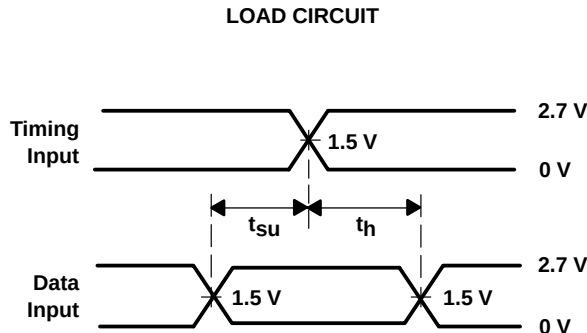
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

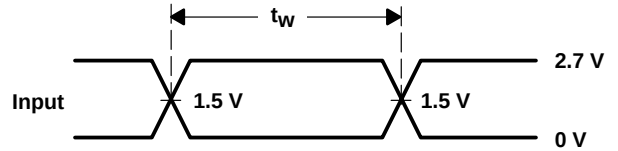


LOAD CIRCUIT

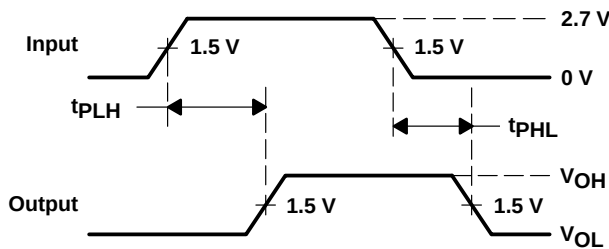
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



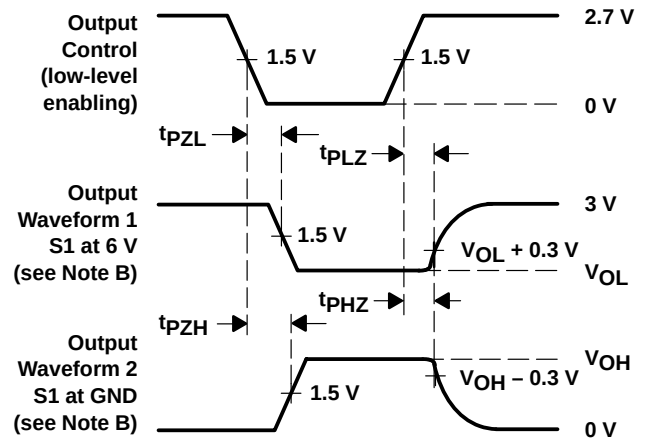
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

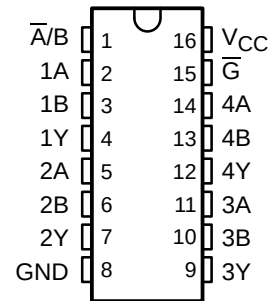
SN74LVC157A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SCAS292F – JANUARY 1993 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC157A features a common strobe ($\overline{G}$) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The device provides true data.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC157A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS				OUTPUT Y
$\overline{G}$	$\overline{A/B}$	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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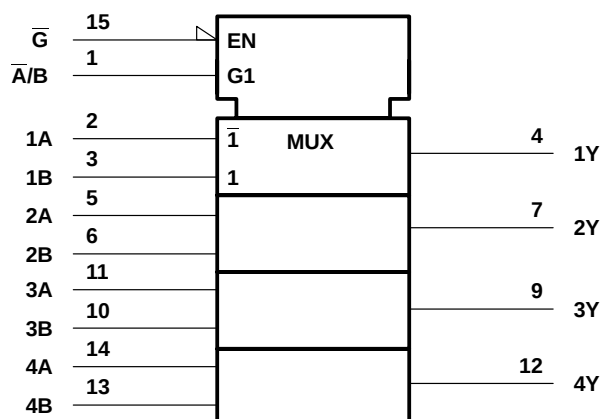
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SN74LVC157A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

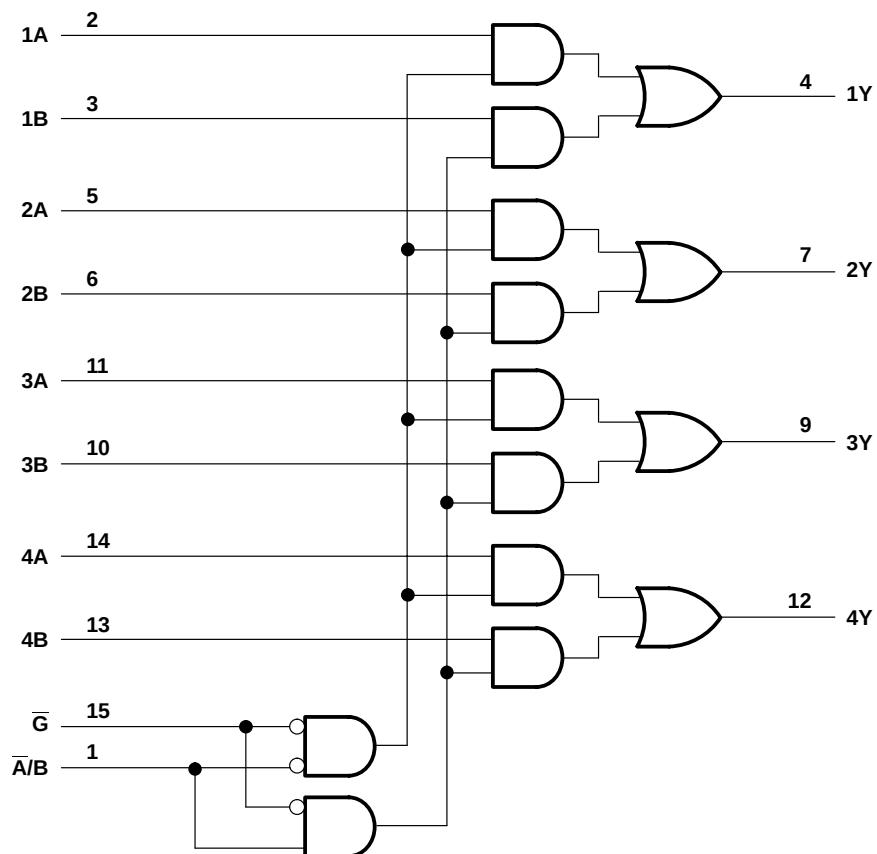
SCAS292F – JANUARY 1993 – REVISED JUNE 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC157A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SCAS292F – JANUARY 1993 – REVISED JUNE 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage		0	V_{CC}	V
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 4 mA	1.65 V	0.45			
	I _{OL} = 8 mA	2.3 V	0.7			
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5			µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			µA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			µA
C _i	V _I = V _{CC} or GND	3.3 V	5			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	‡	‡	‡	‡	5.9		1	5.2	ns
	$\overline{A/B}$		‡	‡	‡	‡	8.1		1	6.8	
	$\overline{G}$		‡	‡	‡	‡	7.8		1	6.5	
t _{sk(o)} [§]										1	ns

[‡] This information was not available at the time of publication.

[§] Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
		TYP	TYP	TYP	
C _{pd} Power dissipation capacitance	f = 10 MHz	‡	‡	16	pF

[‡] This information was not available at the time of publication.

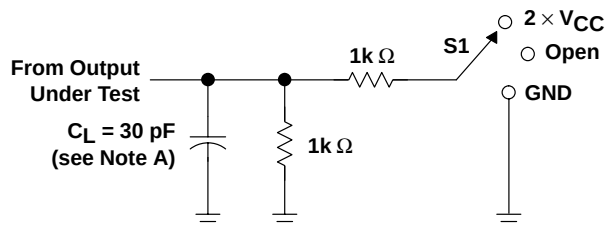


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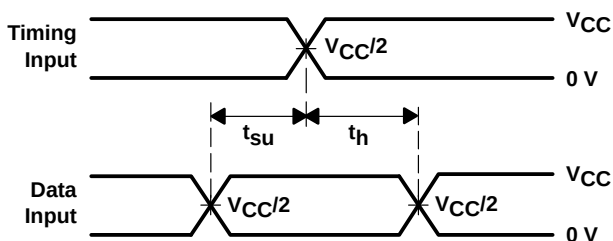
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

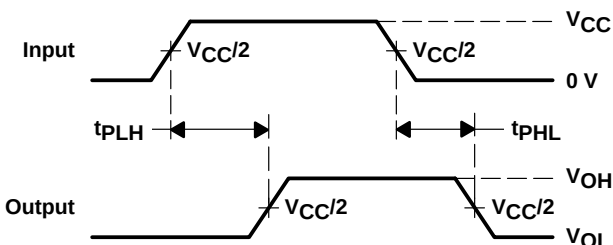


LOAD CIRCUIT

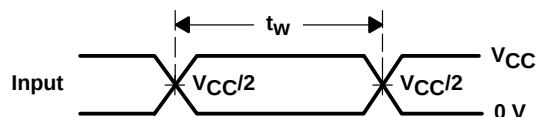
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



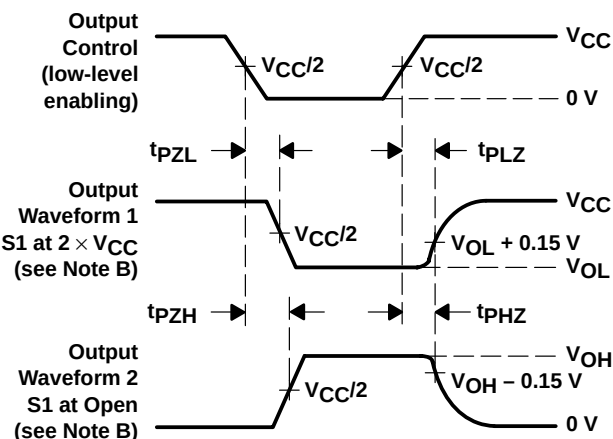
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

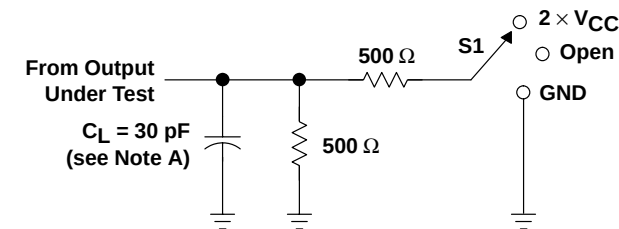
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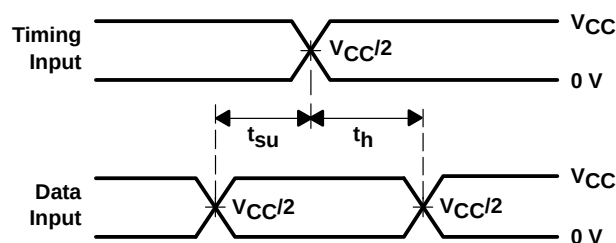
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

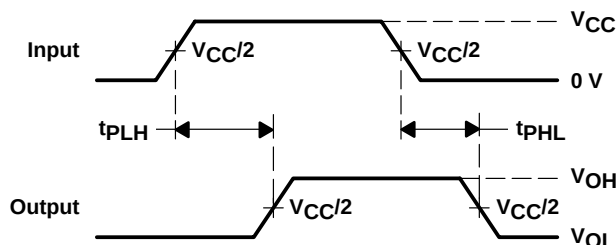


LOAD CIRCUIT

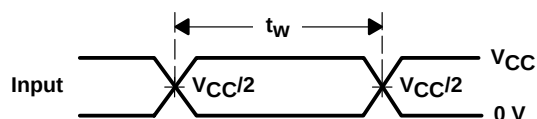
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



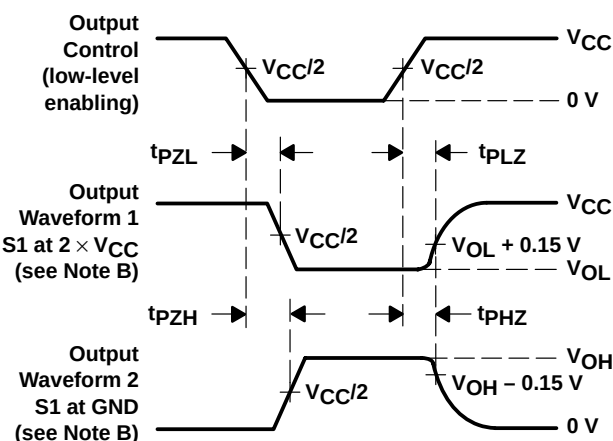
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

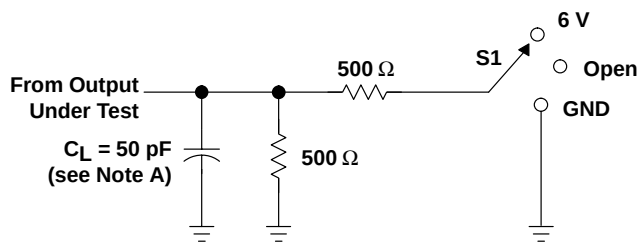
Figure 2. Load Circuit and Voltage Waveforms

SN74LVC157A QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

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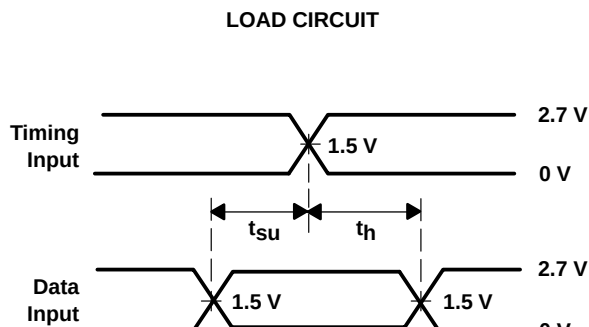
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$

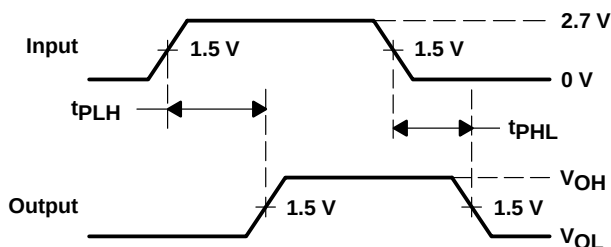


LOAD CIRCUIT

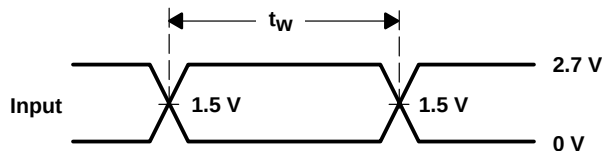
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



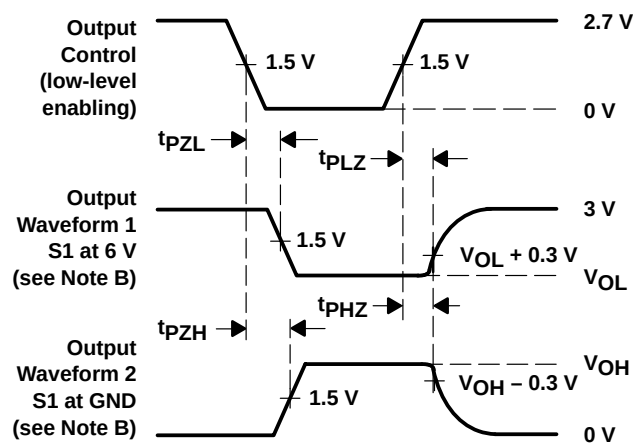
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

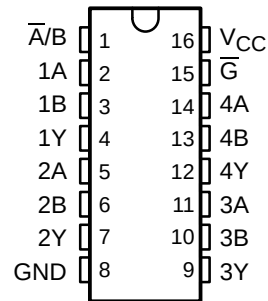
SN74LVC158A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC158A features a direct strobe ($\overline{G}$) input. When the strobe is high, all outputs are high. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The SN74LVC158A provides inverted data.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices in a mixed 3.3-V/5-V system environment.

The SN74LVC158A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS				OUTPUT Y
$\overline{G}$	$\overline{A/B}$	A	B	
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

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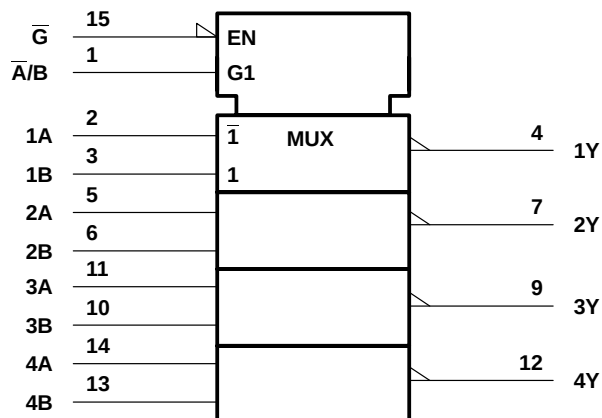
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QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

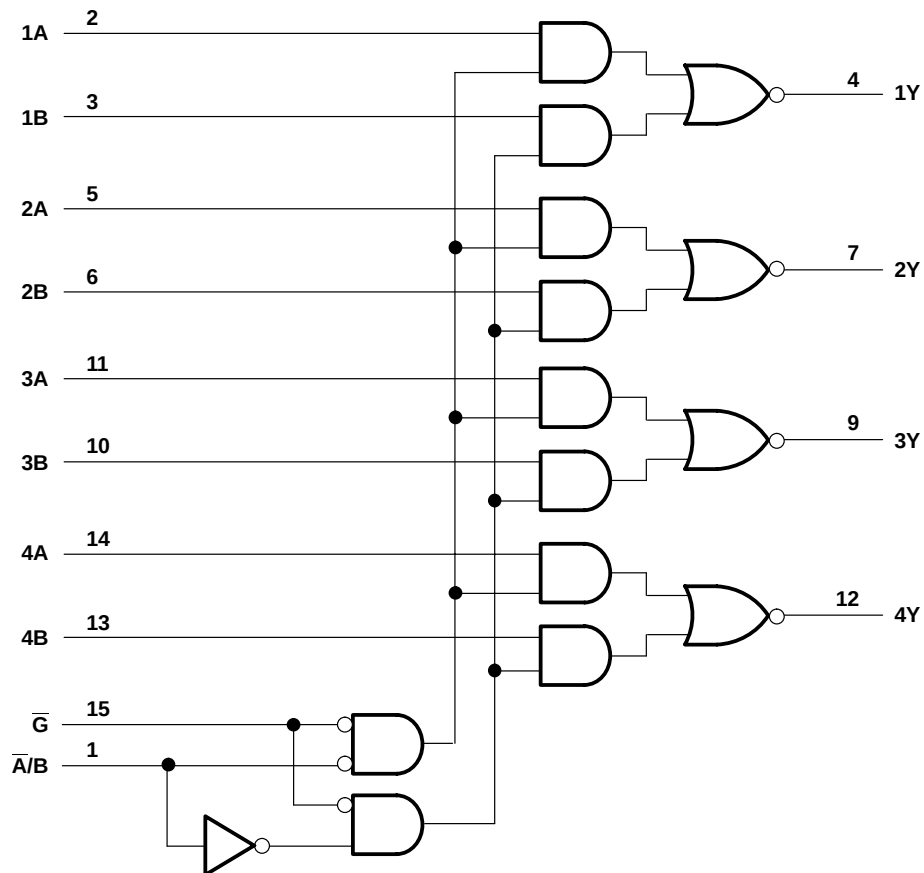
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage		0	V_{CC}	V
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V	V _{CC} –0.2			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
	I _{OL} = 4 mA	1.65 V			0.45	
	I _{OL} = 8 mA	2.3 V			0.7	
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = 5.5 V or GND	3.6 V			±5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			10	μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μA
C _i	V _I = V _{CC} or GND	3.3 V				pF
C _o	V _O = V _{CC} or GND	3.3 V				pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y									ns
	A/B										
	$\overline{G}$										
t _{sk(o)} [‡]											ns

[‡] Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

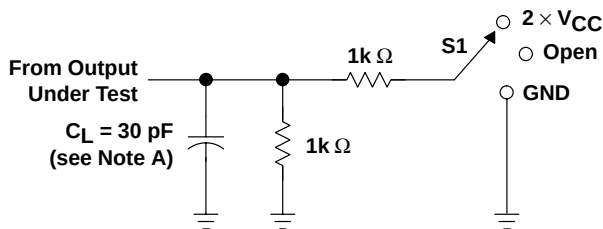
PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
		TYP	TYP	TYP	
C _{pd} Power dissipation capacitance	f = 10 MHz				pF

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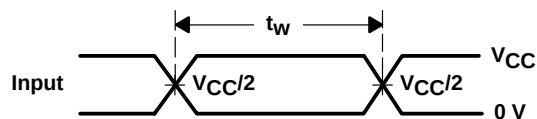
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

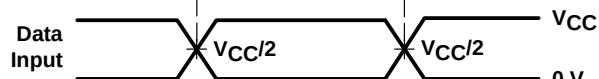


LOAD CIRCUIT

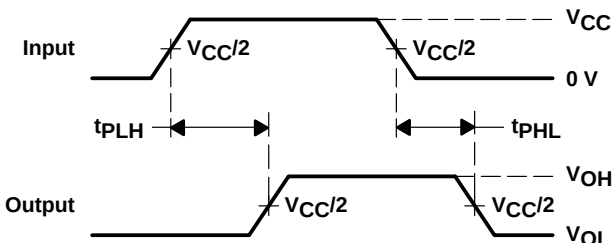
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



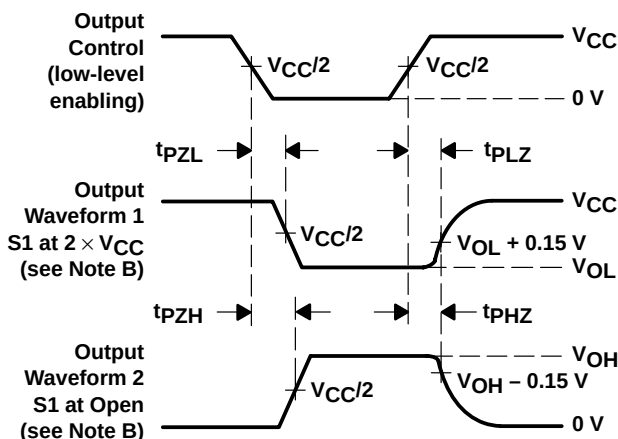
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

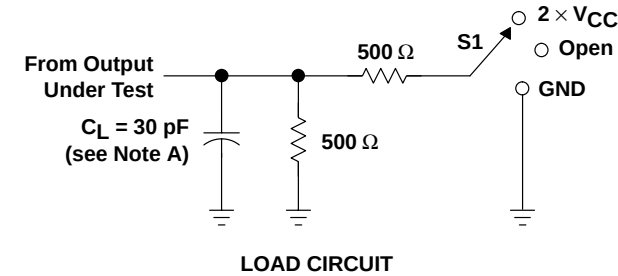
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

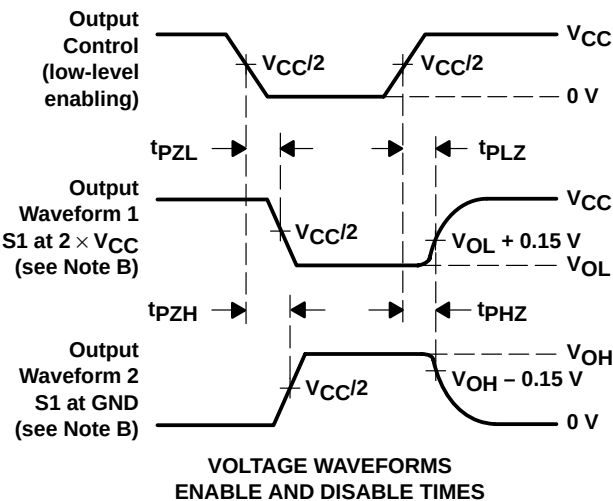
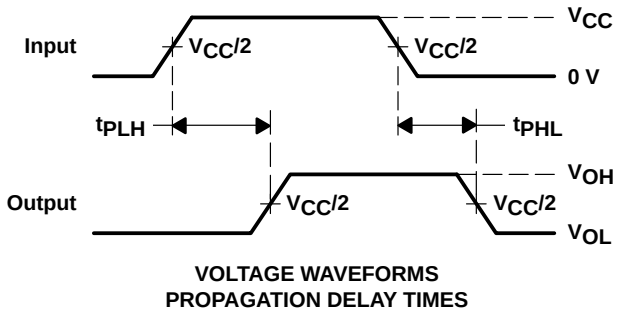
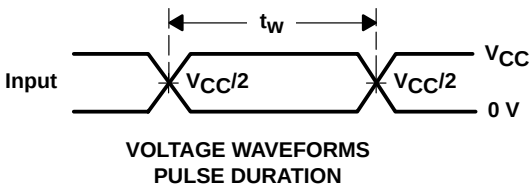
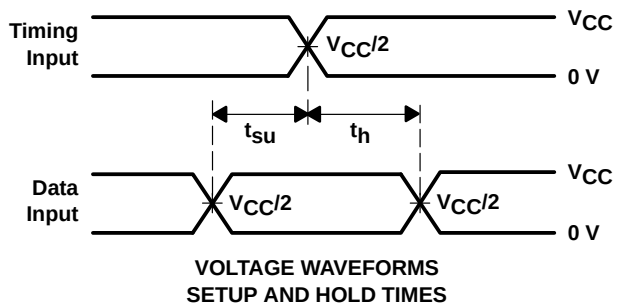
SN74LVC158A QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SCAS342F – MARCH 1994 – REVISED JUNE 1998

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

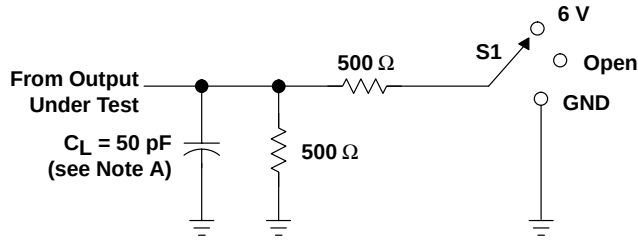
Figure 2. Load Circuit and Voltage Waveforms

SN74LVC158A QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SCAS342F – MARCH 1994 – REVISED JUNE 1998

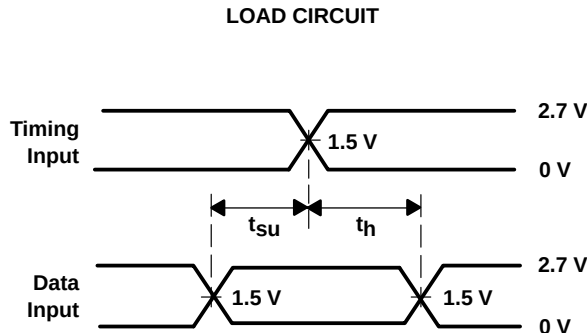
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$

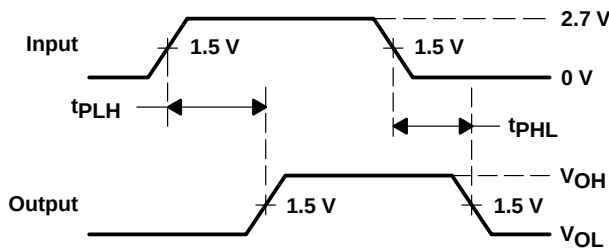


LOAD CIRCUIT

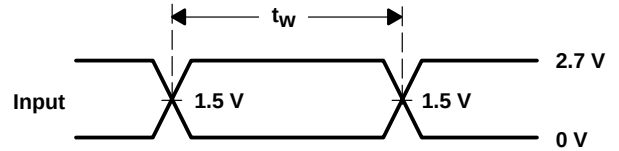
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



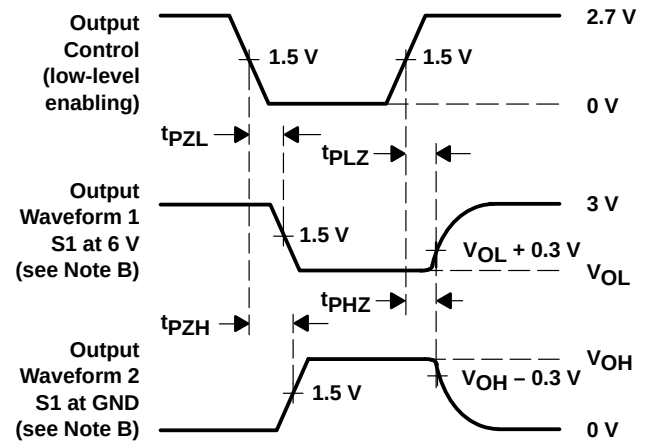
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

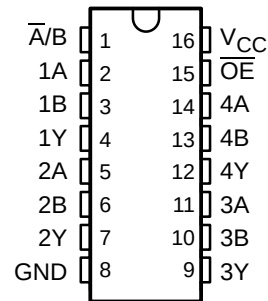
SN74LVC257A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

**D, DB, OR PW PACKAGE
(TOP VIEW)**



description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC257A is designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at a high logic level.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC257A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS				OUTPUT Y
$\overline{OE}$	A/B	A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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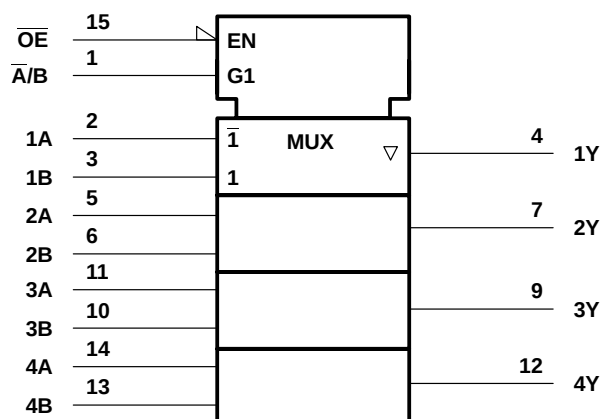
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SN74LVC257A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

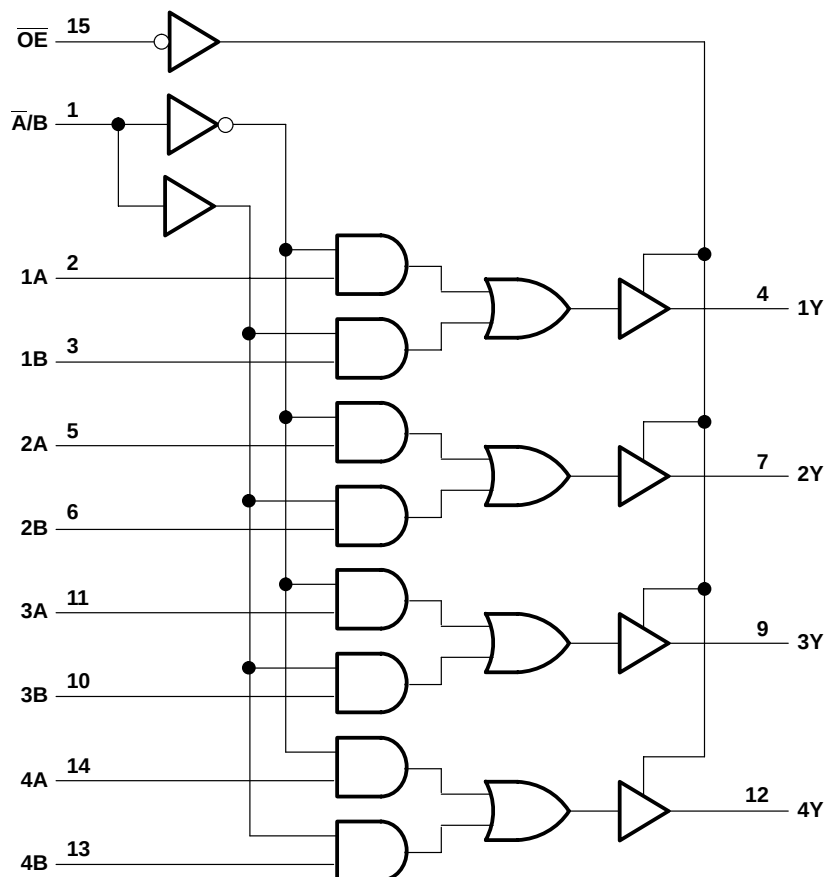
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC257A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage		0	V_{CC}	V
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V	V _{CC} –0.2			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
I _{OH} = –24 mA	3 V	2.2				
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
	I _{OL} = 4 mA	1.65 V			0.45	
	I _{OL} = 8 mA	2.3 V			0.7	
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = 5.5 V or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			10	μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μA
C _i	V _I = V _{CC} or GND	3.3 V	5			pF
C _O	V _O = V _{CC} or GND	3.3 V	5			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	‡	‡	‡	‡	5.4		1	4.6	ns
	$\overline{A/B}$		‡	‡	‡	‡	7.5		1	6.4	
t _{en}	$\overline{OE}$	Y	‡	‡	‡	‡	6.7		1	5.6	ns
t _{dis}	$\overline{OE}$	Y	‡	‡	‡	‡	4.7		1	4.3	ns
t _{sk(o)} [§]									1		ns

‡ This information was not available at the time of publication.

§ Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
		TYP	TYP	TYP	
C _{pd} Power dissipation capacitance	f = 10 MHz	‡	‡	15.5	pF

‡ This information was not available at the time of publication.



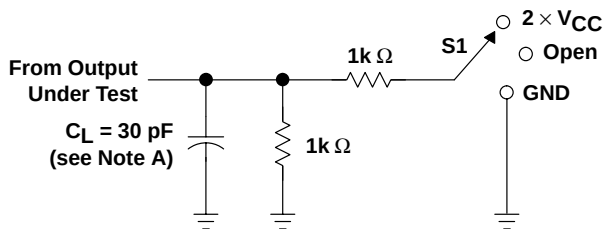
SN74LVC257A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

SCAS294F – JANUARY 1993 – REVISED JUNE 1998

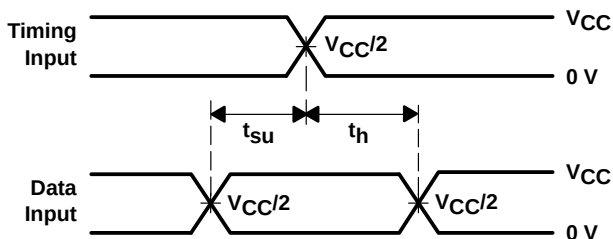
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

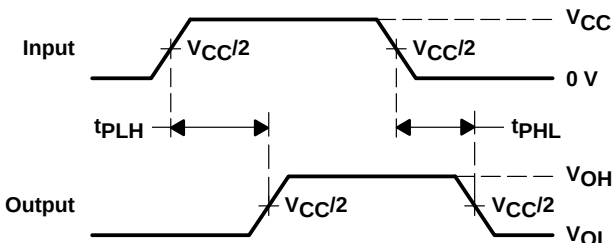


LOAD CIRCUIT

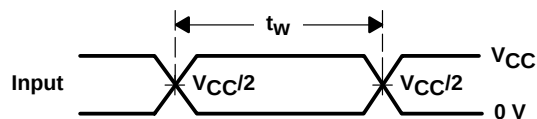
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



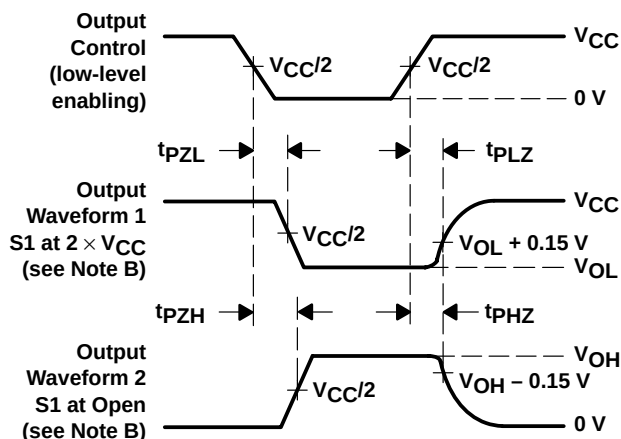
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC257A

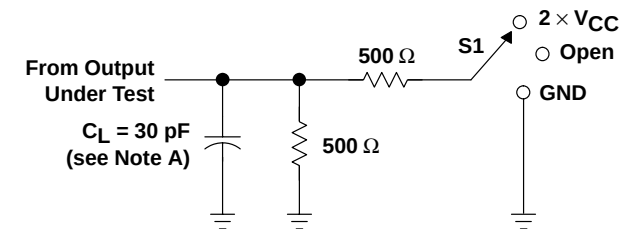
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

WITH 3-STATE OUTPUTS

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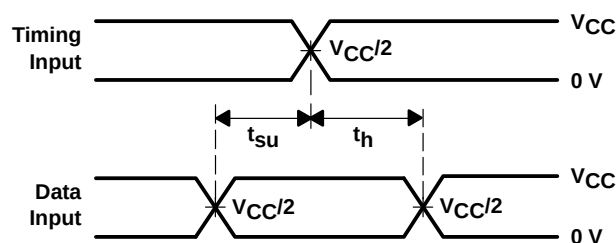
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

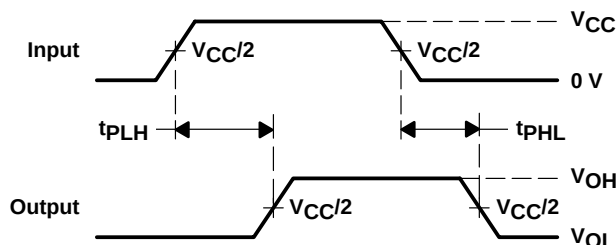


LOAD CIRCUIT

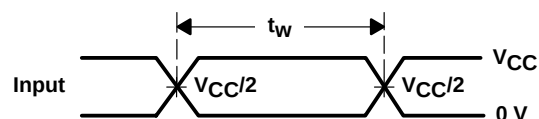
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



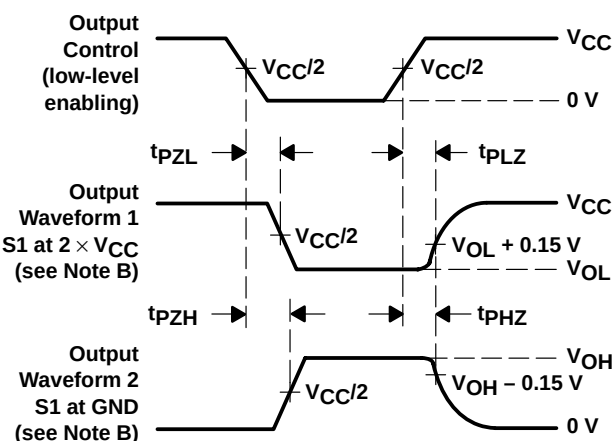
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

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 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

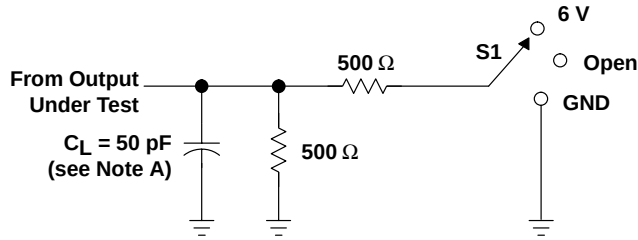
SN74LVC257A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

SCAS294F – JANUARY 1993 – REVISED JUNE 1998

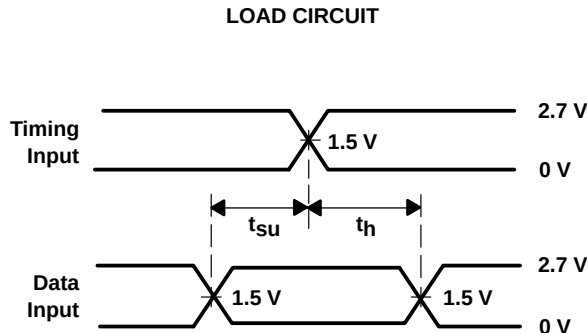
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

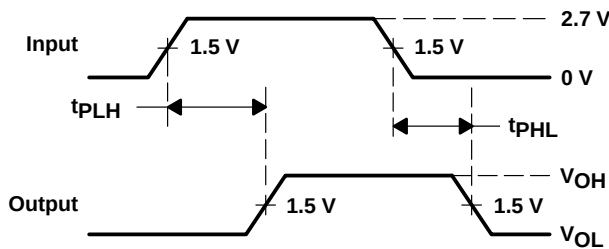


LOAD CIRCUIT

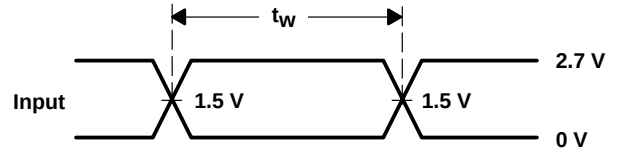
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



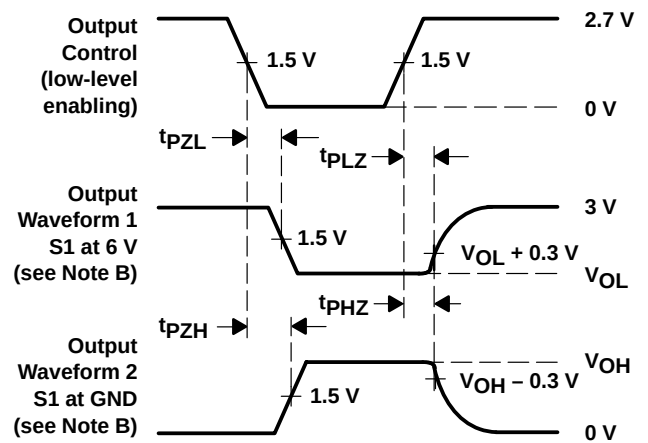
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

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 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

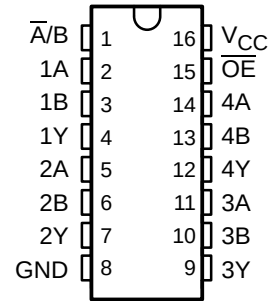
Figure 3. Load Circuit and Voltage Waveforms

SN74LVC258A QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

SCAS345F – MARCH 1994 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC258A is designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at a high logic level.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC258A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS				OUTPUT Y
$\overline{OE}$	A/B	A	B	
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

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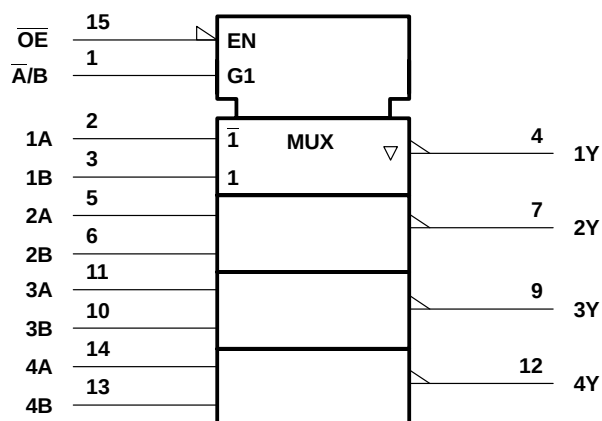
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SN74LVC258A QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

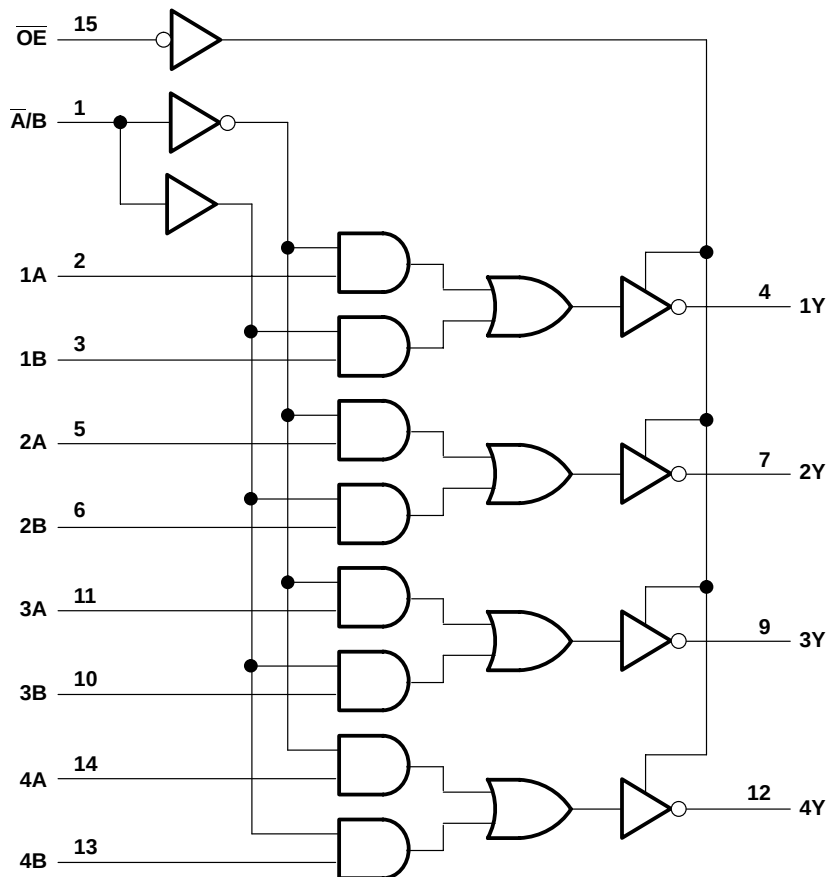
SCAS345F – MARCH 1994 – REVISED JUNE 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC258A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

SCAS345F – MARCH 1994 – REVISED JUNE 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage		0	V_{CC}	V
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW



SN74LVC258A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 4 mA	1.65 V	0.45			
	I _{OL} = 8 mA	2.3 V	0.7			
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5			µA
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±10			µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			µA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			µA
C _i	V _I = V _{CC} or GND	3.3 V				pF
C _o	V _O = V _{CC} or GND	3.3 V				pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y									ns
	$\overline{A/B}$										
t _{en}	$\overline{OE}$	Y									ns
t _{dis}	$\overline{OE}$	Y									ns
t _{sk(o)} [‡]											ns

[‡] Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
		TYP	TYP	TYP	
C _{pd} Power dissipation capacitance	f = 10 MHz				pF



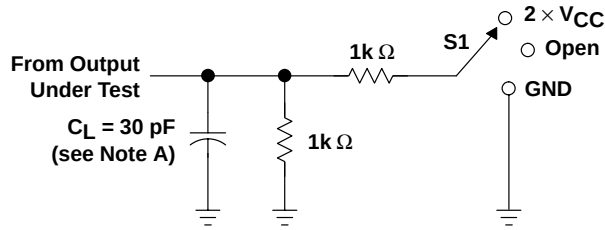
SN74LVC258A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

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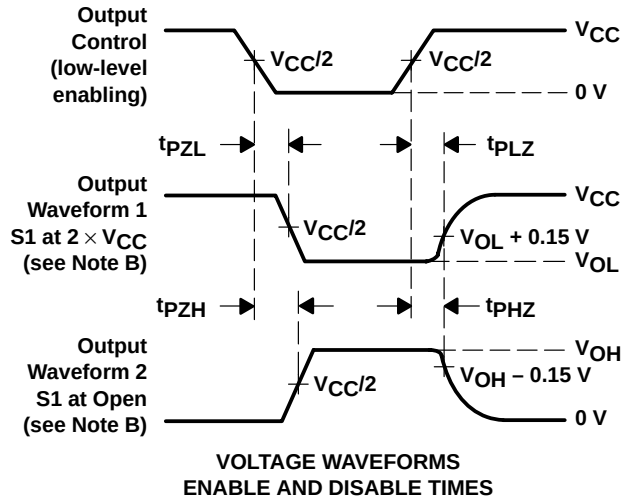
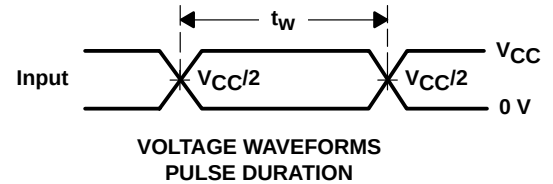
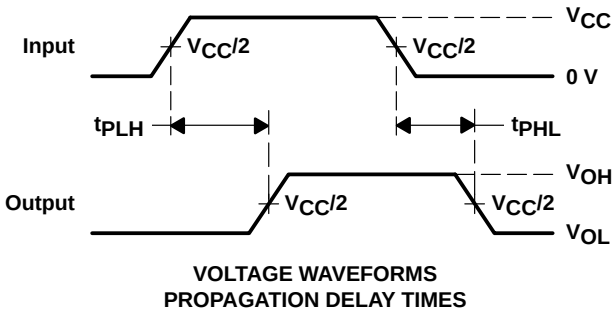
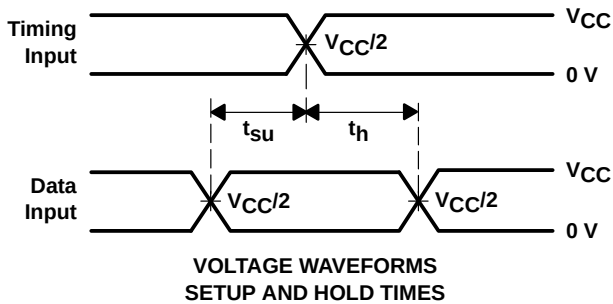
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PHZ}	Open



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SN74LVC258A

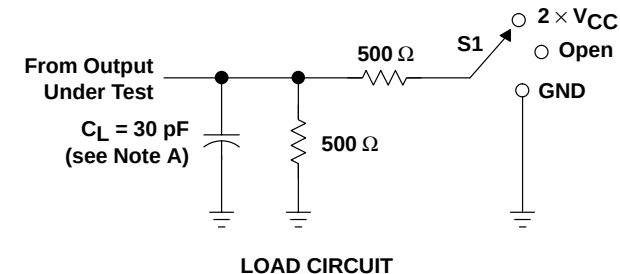
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

WITH 3-STATE OUTPUTS

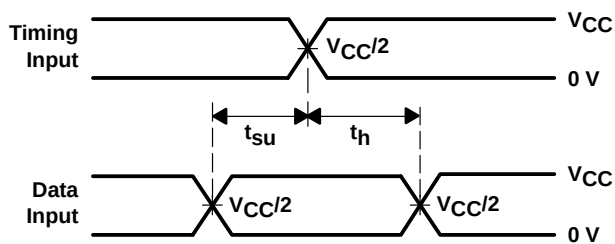
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PARAMETER MEASUREMENT INFORMATION

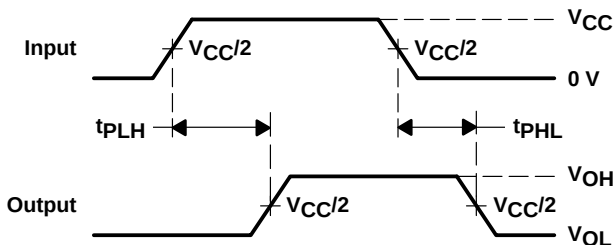
$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



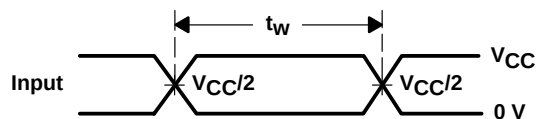
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



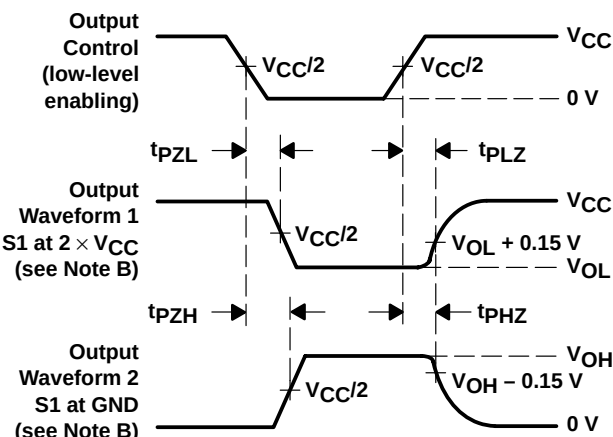
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

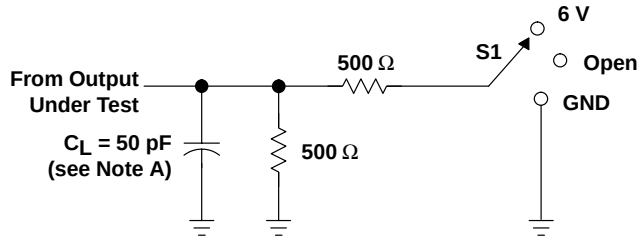
SN74LVC258A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

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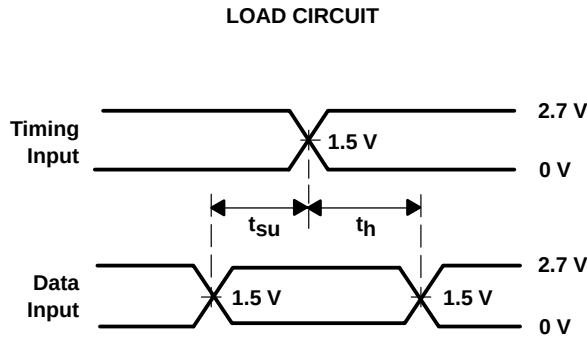
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$

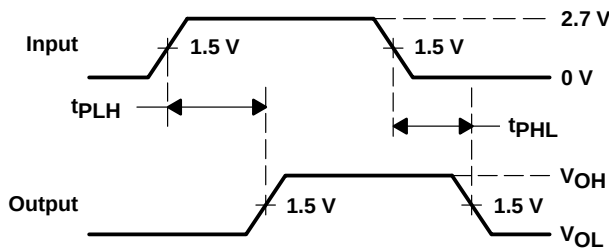


LOAD CIRCUIT

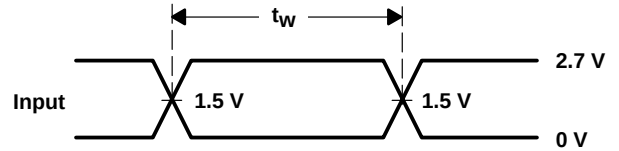
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



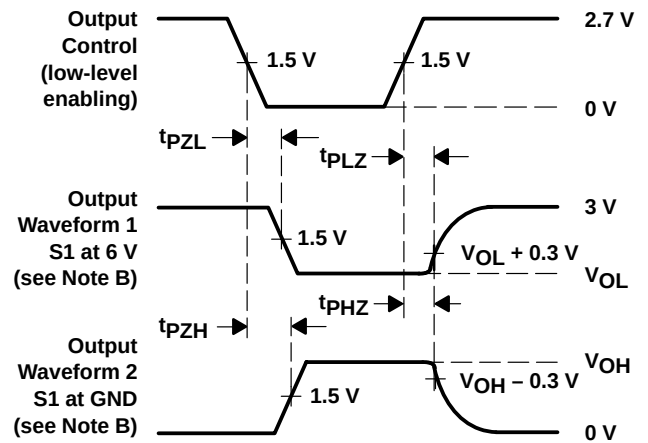
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

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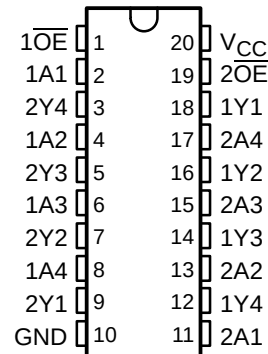
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SN74LVC240A OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Power Off Disables Outputs, Permitting Live Insertion
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC240A is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

This device is organized as two 4-bit buffers/drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC240A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	L
L	L	H
H	X	Z

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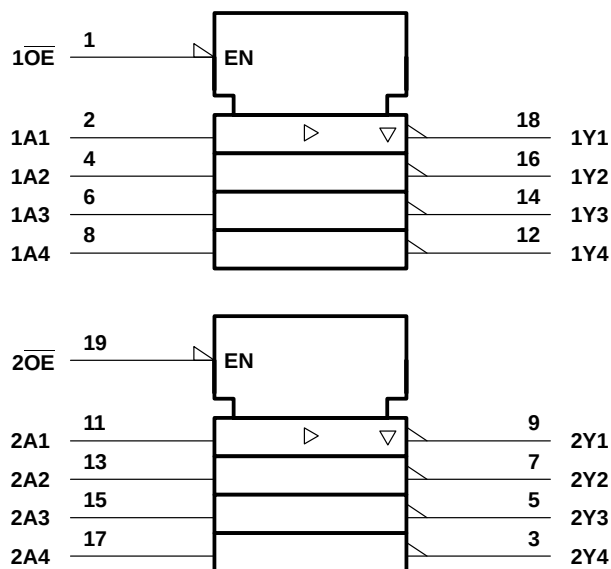
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OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

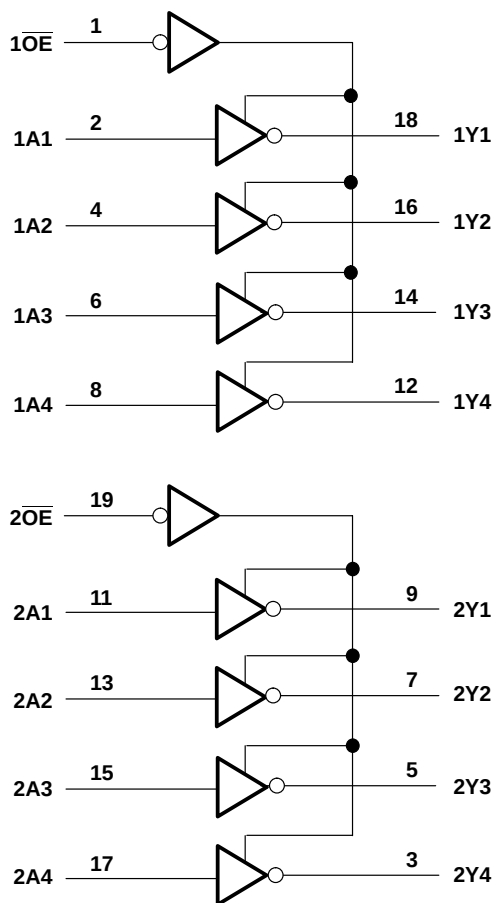
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logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC240A

OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65 3.6	V
		Data retention only	1.5	
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 2.7 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 2.7 V to 3.6 V	0.8	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	High or low state	0 V _{CC}	V
		3 state	0 5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V	–4	mA
		V _{CC} = 2.3 V	–8	
		V _{CC} = 2.7 V	–12	
		V _{CC} = 3 V	–24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4	mA
		V _{CC} = 2.3 V	8	
		V _{CC} = 2.7 V	12	
		V _{CC} = 3 V	24	
Δt/Δv	Input transition rise or fall rate	0	6	ns/V
T _A	Operating free-air temperature	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74LVC240A

OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = −100 μA		1.65 V to 3.6 V	V _{CC} −0.2		V	
	I _{OH} = −4 mA		1.65 V	1.2			
	I _{OH} = −8 mA		2.3 V	1.7			
	I _{OH} = −12 mA		2.7 V	2.2			
			3 V	2.4			
	I _{OH} = −24 mA		3 V	2.2			
V _{OL}	I _{OL} = 100 μA		1.65 V to 3.6 V	0.2		V	
	I _{OL} = 4 mA		1.65 V	0.45			
	I _{OL} = 8 mA		2.3 V	0.7			
	I _{OL} = 12 mA		2.7 V	0.4			
	I _{OL} = 24 mA		3 V	0.55			
I _I	V _I = 0 to 5.5 V		3.6 V	±5		μA	
I _{off}	V _I or V _O = 5.5 V		0	±10		μA	
I _{OZ}	V _O = 0 to 5.5 V		3.6 V	±10		μA	
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	10		μA	
	3.6 V ≤ V _I ≤ 5.5 V [‡]			10			
ΔI _{CC}	One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V	500		μA	
C _i	V _I = V _{CC} or GND		3.3 V	4		pF	
C _O	V _O = V _{CC} or GND		3.3 V	5.5		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	§	§	§	§	7.5		1.3	6.5	ns
t _{en}	$\overline{\text{OE}}$	Y	§	§	§	§	9		1.1	8	ns
t _{dis}	$\overline{\text{OE}}$	Y	§	§	§	§	8		1.4	7	ns
t _{sk(o)} [¶]									1		ns

§ This information was not available at the time of publication.

¶ Skew between any two outputs of the same package switching in the same direction

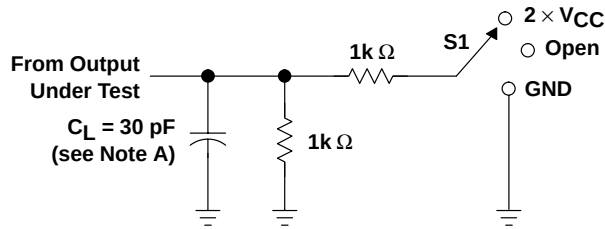
operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	§	§	32	pF
		Outputs disabled		§	§	3	

§ This information was not available at the time of publication.

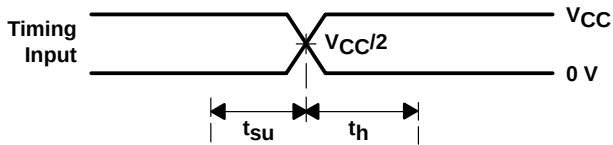


PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$

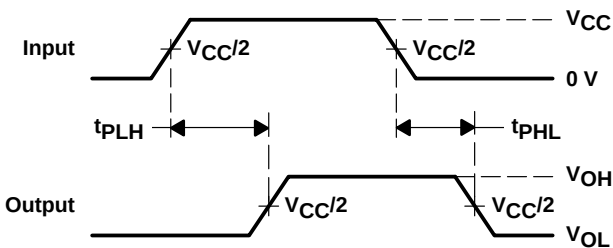


LOAD CIRCUIT

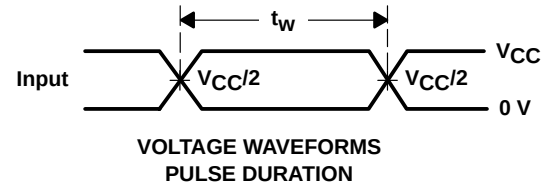
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



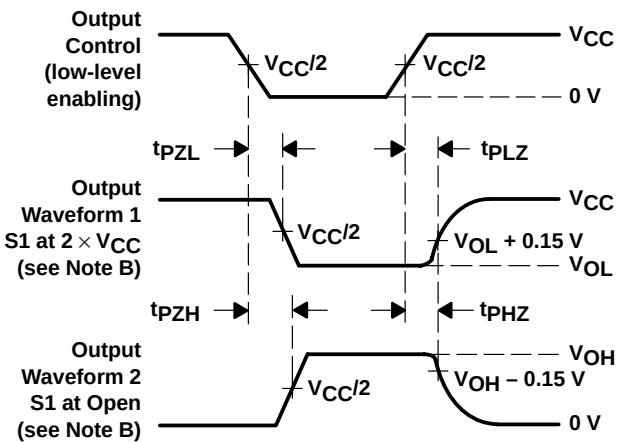
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC240A

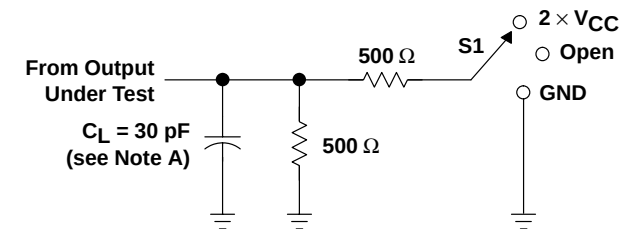
OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

SCAS293F – JANUARY 1993 – REVISED JUNE 1998

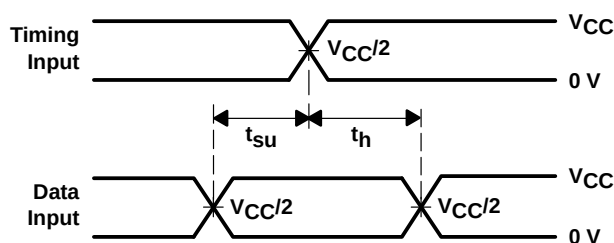
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

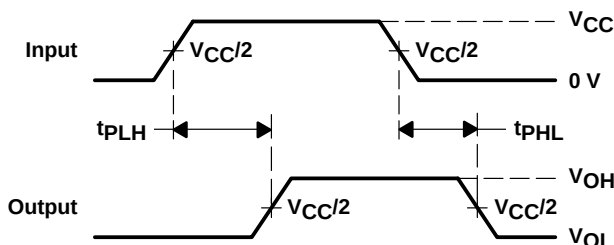


LOAD CIRCUIT

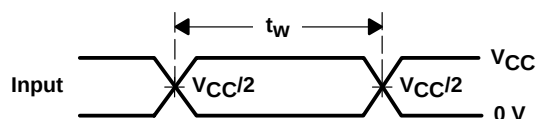
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



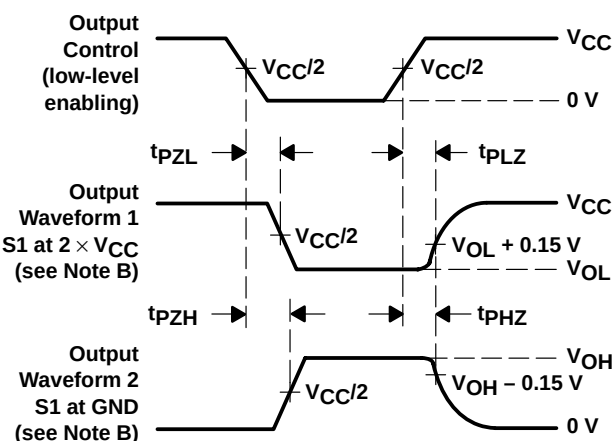
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



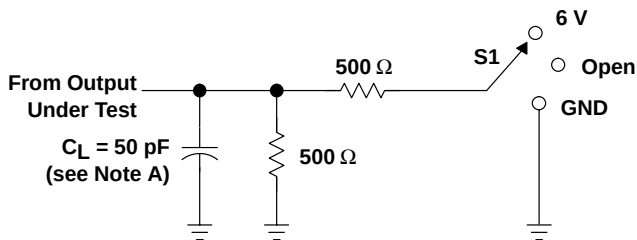
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

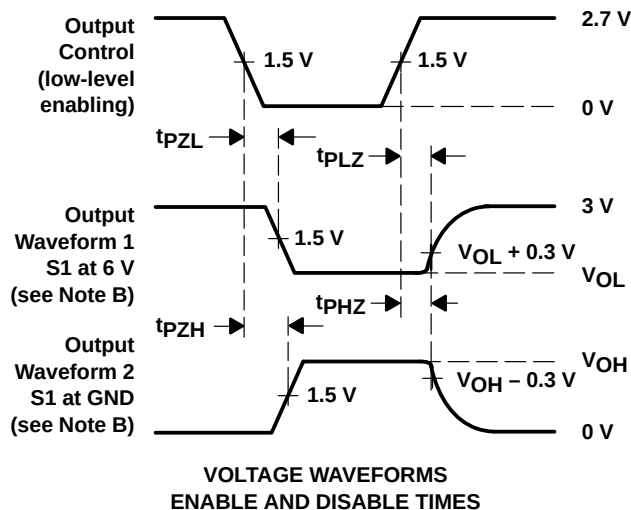
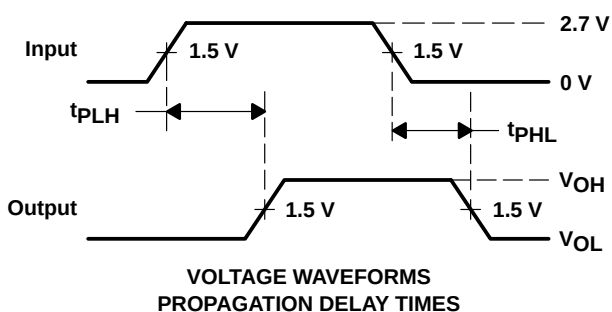
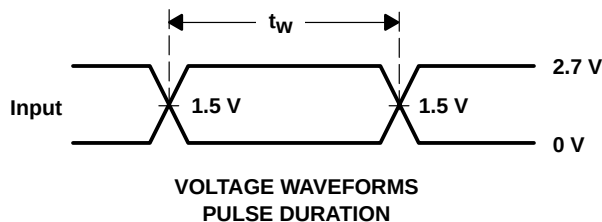
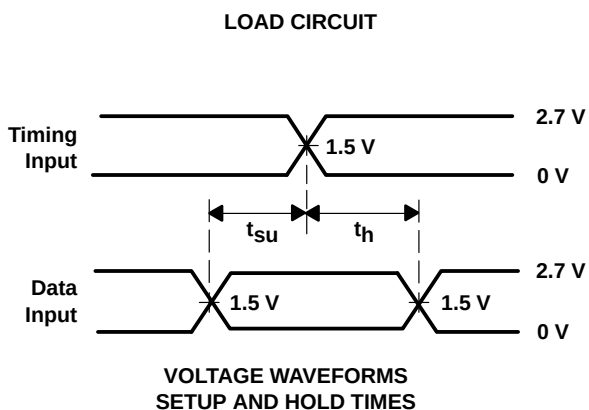
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

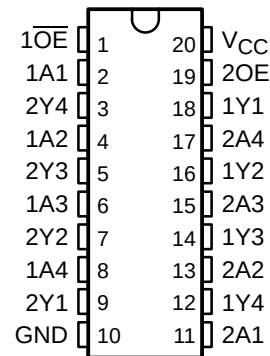
Figure 3. Load Circuit and Voltage Waveforms

SN74LVC241A OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS343E – MARCH 1994 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/line driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC241A is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the 'LVC240A and 'LVC244A, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{OE}$ (active-low output-enable) inputs, and complementary OE and $\overline{OE}$ inputs.

The SN74LVC241A is organized as two 4-bit line drivers with separate output-enable ($\overline{1OE}$, 2OE) inputs. When $\overline{1OE}$ is low or 2OE is high, the device passes data from the A inputs to the Y outputs. When $\overline{1OE}$ is high or 2OE is low, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking or the current-sourcing capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC241A is characterized for operation from -40°C to 85°C .

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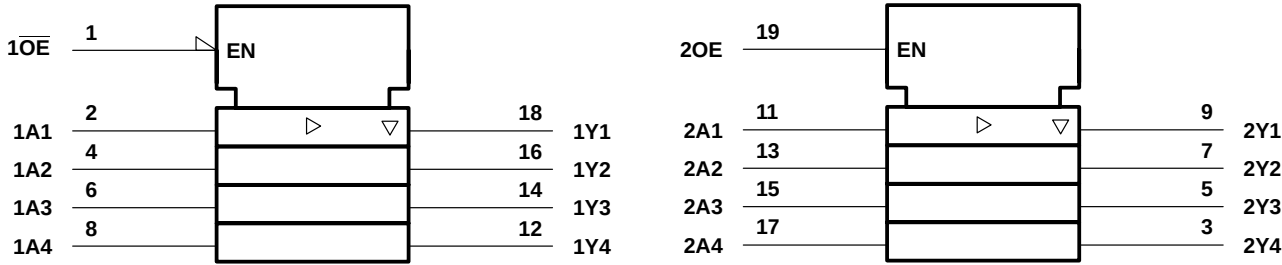
SN74LVC241A
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS
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FUNCTION TABLES

INPUTS		OUTPUT 1Y
1OE	1A	
L	H	H
L	L	L
H	X	Z

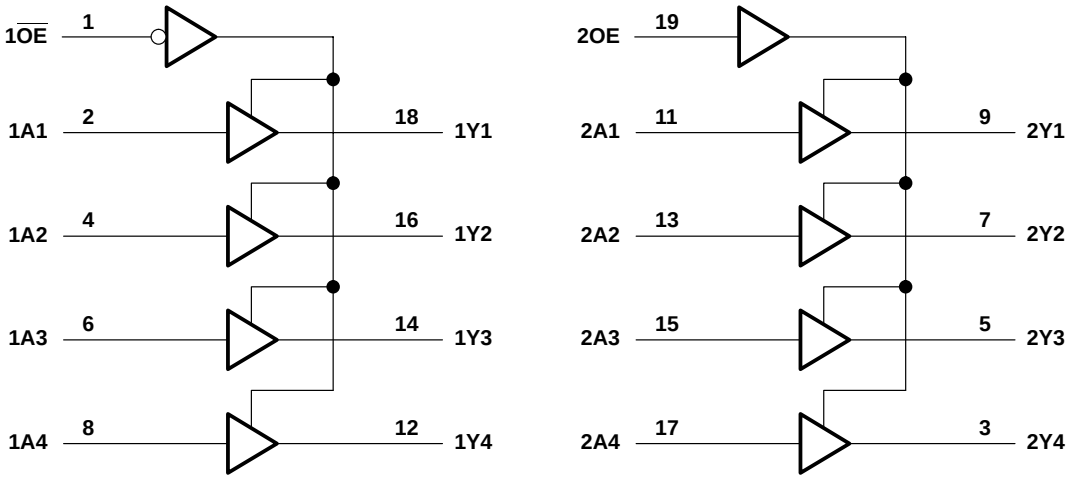
INPUTS		OUTPUT 2Y
2OE	2A	
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC241A

OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OH} = –100 μA		1.65 V to 3.6 V	V _{CC} –0.2		V	
	I _{OH} = –4 mA		1.65 V	1.2			
	I _{OH} = –8 mA		2.3 V	1.7			
	I _{OH} = –12 mA		2.7 V	2.2			
			3 V	2.4			
	I _{OH} = –24 mA		3 V	2.2			
V _{OL}	I _{OL} = 100 μA		1.65 V to 3.6 V	0.2		V	
	I _{OL} = 4 mA		1.65 V	0.45			
	I _{OL} = 8 mA		2.3 V	0.7			
	I _{OL} = 12 mA		2.7 V	0.4			
	I _{OL} = 24 mA		3 V	0.55			
	I _I	V _I = 0 to 5.5 V		3.6 V	±5		μA
I _{off}	V _I or V _O = 5.5 V		0	±10		μA	
I _{OZ}	V _O = 0 to 5.5 V		3.6 V	±10		μA	
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	10		μA	
	3.6 V ≤ V _I ≤ 5.5 V‡			10			
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V	500		μA	
C _i	V _I = V _{CC} or GND		3.3 V			pF	
C _O	V _O = V _{CC} or GND		3.3 V			pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y									ns
t _{en}	OE or OE	Y									ns
t _{dis}	OE or OE	Y									ns

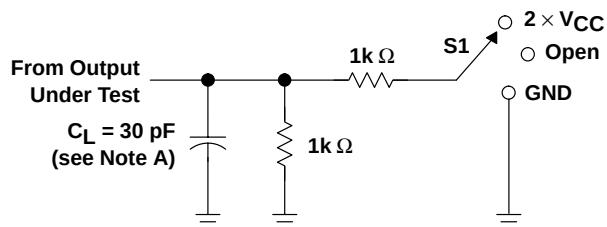
operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz				pF
		Outputs disabled					



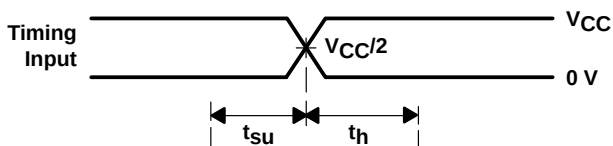
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

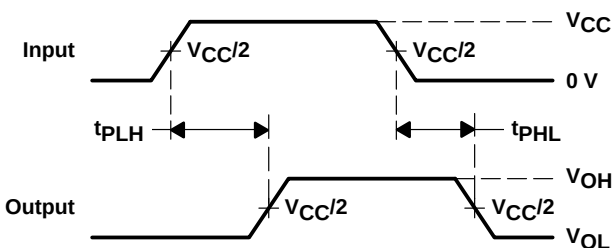


LOAD CIRCUIT

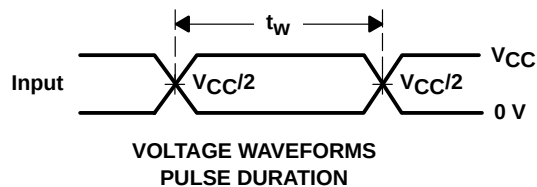
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



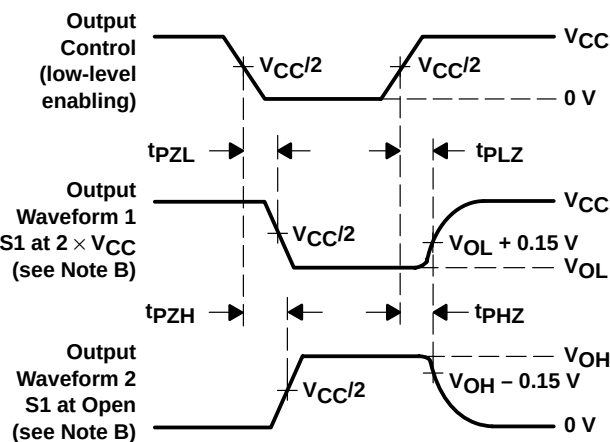
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC241A

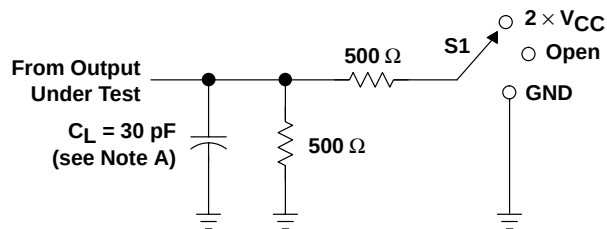
OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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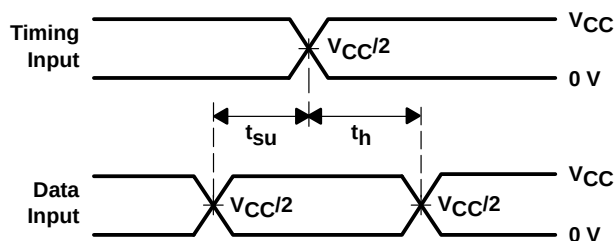
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

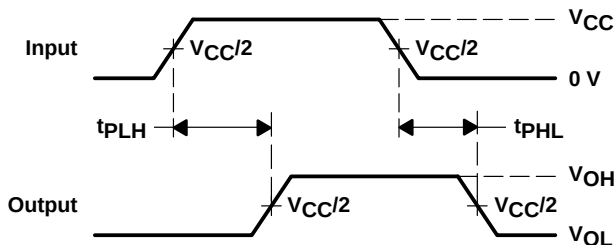


LOAD CIRCUIT

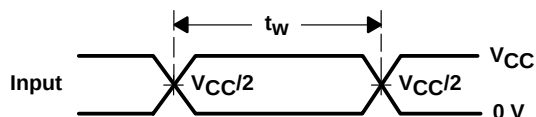
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



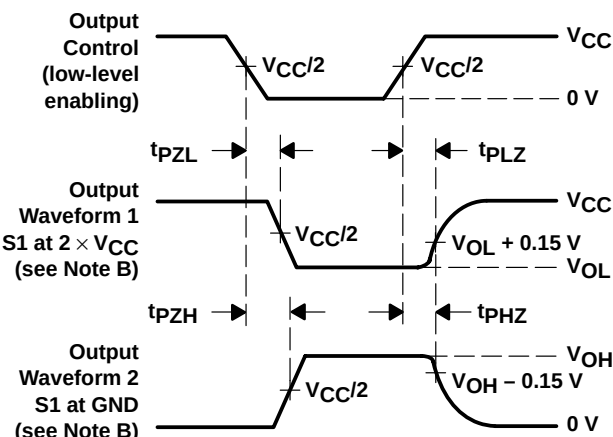
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



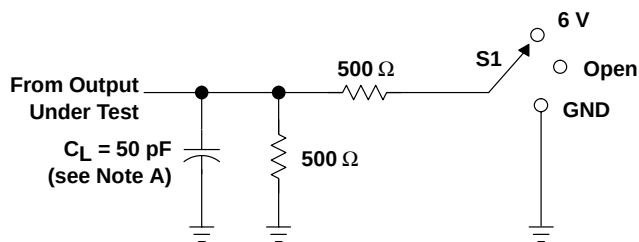
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

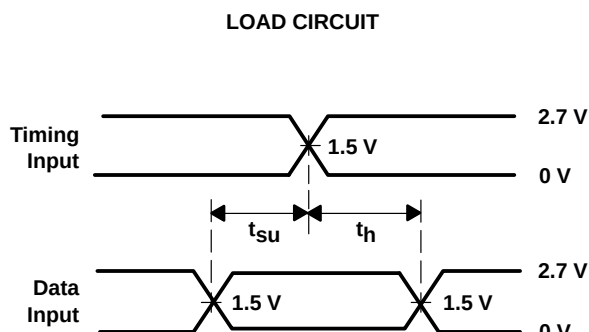
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$

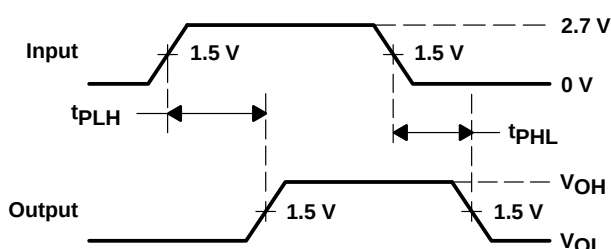


LOAD CIRCUIT

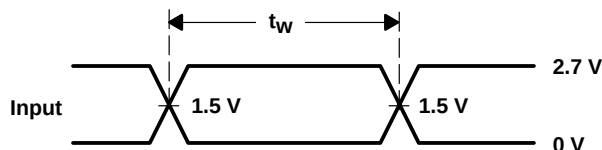
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



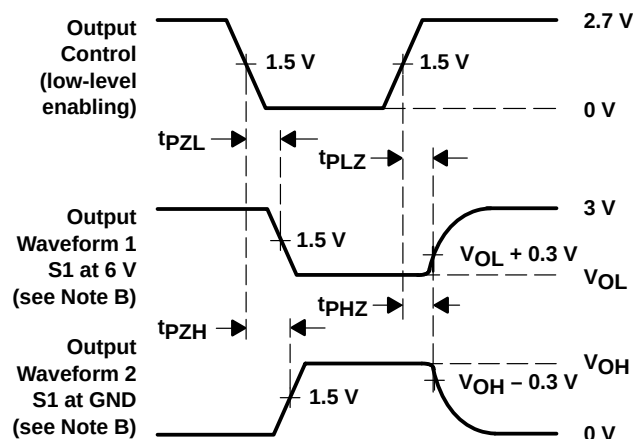
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

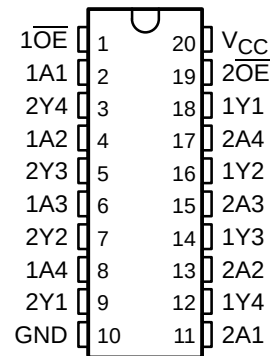
Figure 3. Load Circuit and Voltage Waveforms

SN74LVC244A OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS414I – NOVEMBER 1992 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Package Options Include Shrink Small-Outline (DB), Plastic Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/line driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC244A is organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC244A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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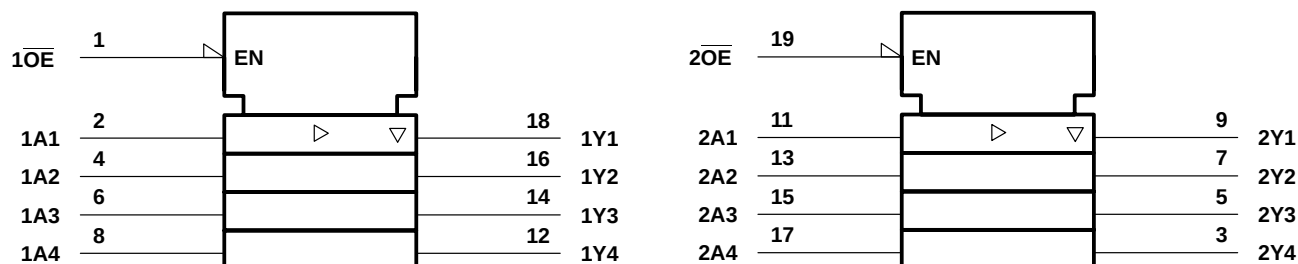
SN74LVC244A

OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

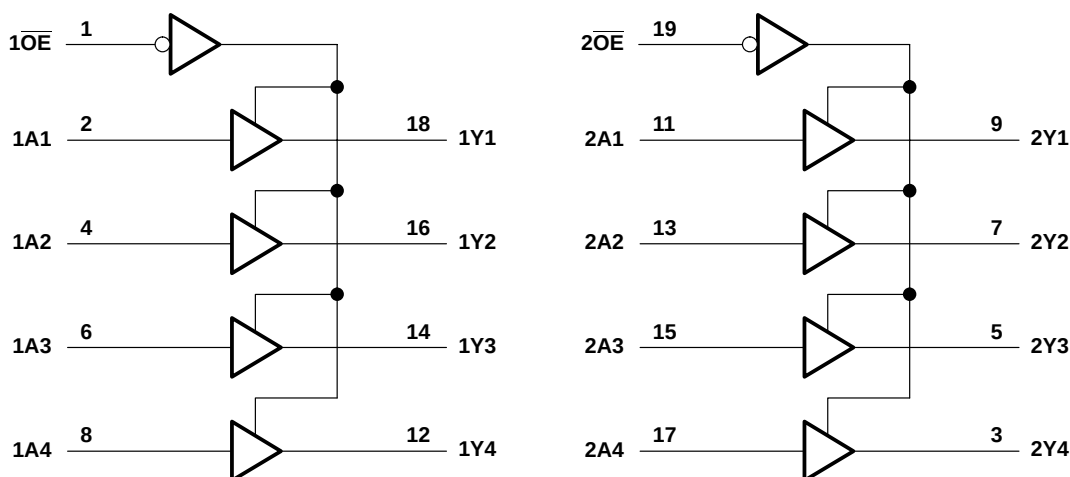
SCAS414I – NOVEMBER 1992 – REVISED JUNE 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	
DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.



SN74LVC244A
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCAS414I – NOVEMBER 1992 – REVISED JUNE 1998

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage		0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	V
		3 state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V	−4		mA
		V _{CC} = 2.3 V	−8		
		V _{CC} = 2.7 V	−12		
		V _{CC} = 3 V	−24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		mA
		V _{CC} = 2.3 V	8		
		V _{CC} = 2.7 V	12		
		V _{CC} = 3 V	24		
T _A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC244A

OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

SCAS414I – NOVEMBER 1992 – REVISED JUNE 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = −100 μA		1.65 V to 3.6 V	V _{CC} −0.2			V
	I _{OH} = −4 mA		1.65 V	1.2			
	I _{OH} = −8 mA		2.3 V	1.7			
	I _{OH} = −12 mA		2.7 V	2.2			
			3 V	2.4			
	I _{OH} = −24 mA		3 V	2.2			
V _{OL}	I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	V
	I _{OL} = 4 mA		1.65 V			0.45	
	I _{OL} = 8 mA		2.3 V			0.7	
	I _{OL} = 12 mA		2.7 V			0.4	
	I _{OL} = 24 mA		3 V			0.55	
I _I	V _I = 0 to 5.5 V		3.6 V			±5	μA
I _{off}	V _I or V _O = 5.5 V		0			±10	μA
I _{OZ}	V _O = 0 to 5.5 V		3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND		3.6 V			10	μA
	3.6 V ≤ V _I ≤ 5.5 V [‡]					10	
ΔI _{CC}	One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V			500	μA
C _i	V _I = V _{CC} or GND		3.3 V			4	pF
C ₀	V _O = V _{CC} or GND		3.3 V			5.5	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	§	§	§	§	6.9		1.5	5.9	ns
t _{en}	$\overline{\text{OE}}$	Y	§	§	§	§	8.6		1.5	7.6	ns
t _{dis}	$\overline{\text{OE}}$	Y	§	§	§	§	6.8		1.5	6.5	ns

§ This information was not available at the time of publication.

operating characteristics, T_A = 25°C

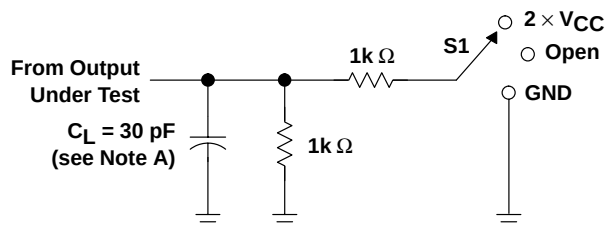
PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	§	§	44	pF
		Outputs disabled		§	§	2	

§ This information was not available at the time of publication.



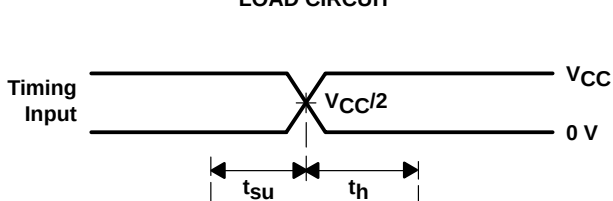
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

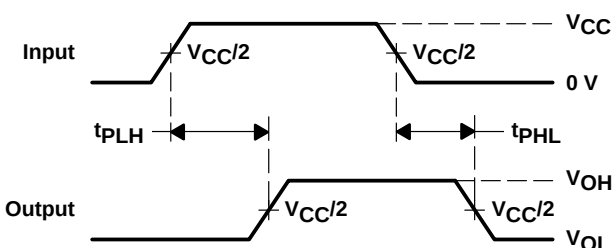


LOAD CIRCUIT

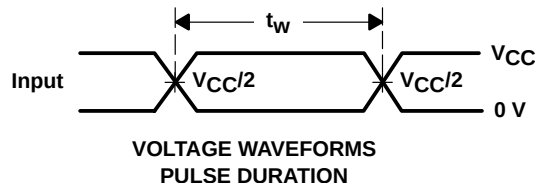
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



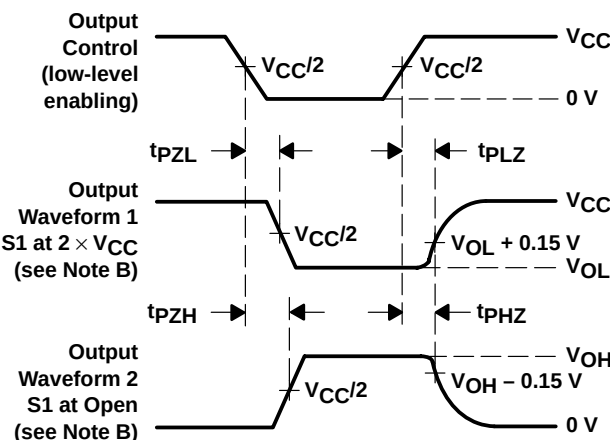
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC244A

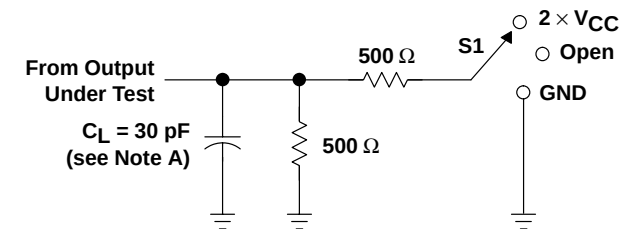
OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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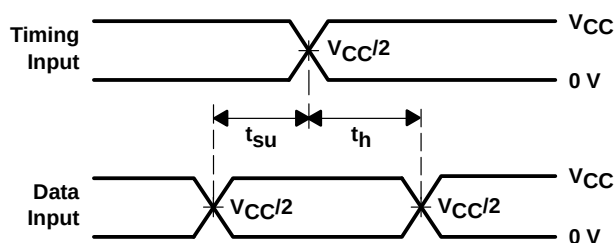
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

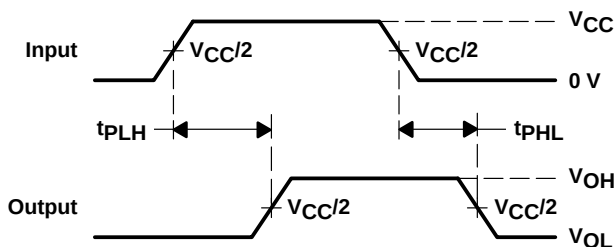


LOAD CIRCUIT

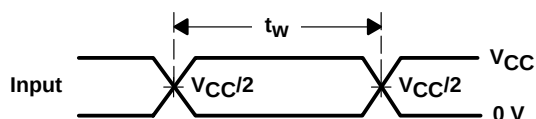
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



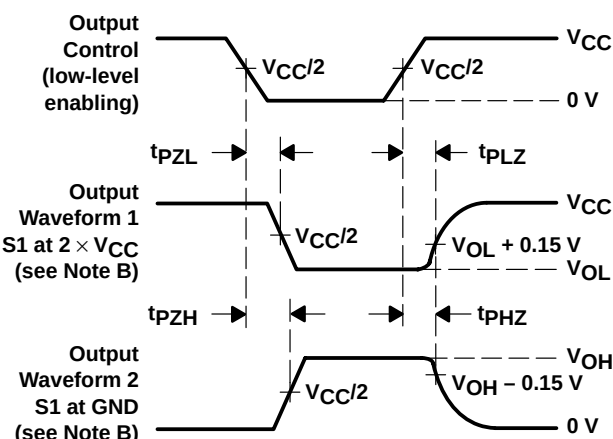
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

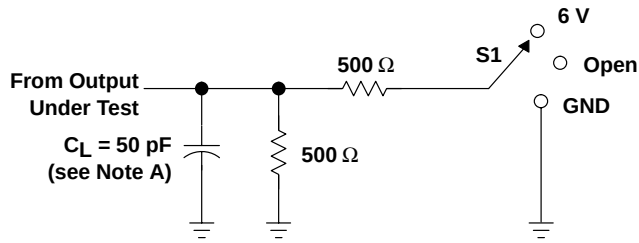


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

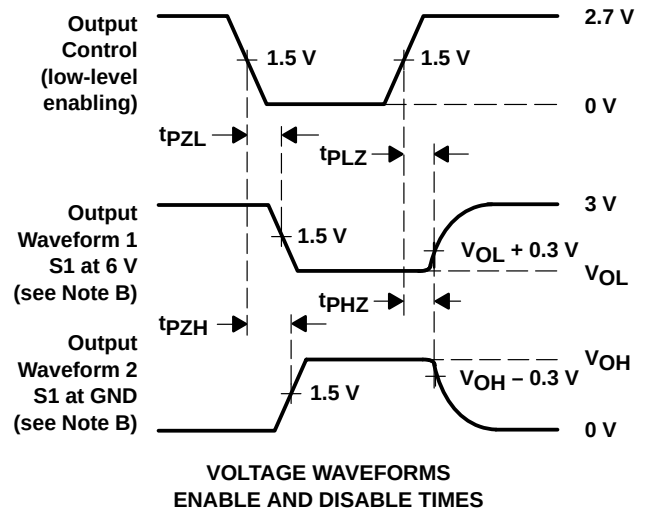
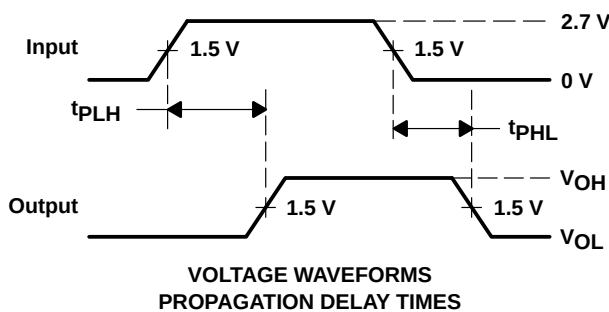
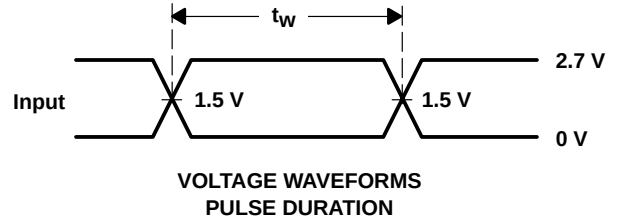
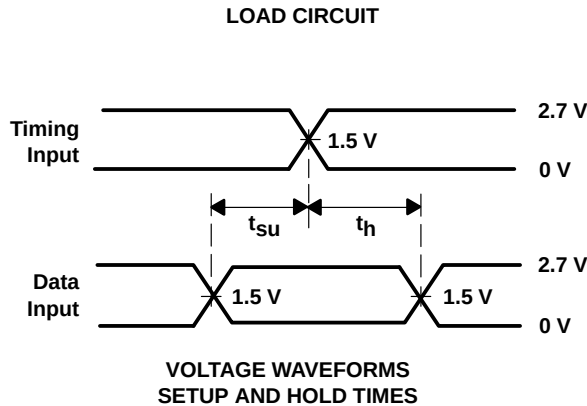
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

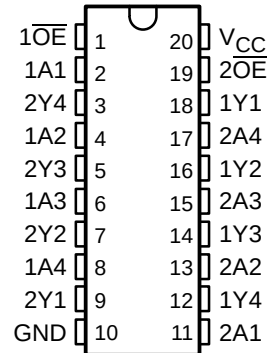
Figure 3. Load Circuit and Voltage Waveforms

SN54LVCH244A, SN74LVCH244A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

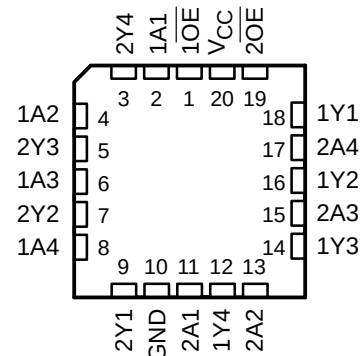
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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Package, Ceramic Chip Carriers (FK), and DIPs (J)

SN54LVCH244A . . . J OR W PACKAGE
SN74LVCH244A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVCH244A . . . FK PACKAGE
(TOP VIEW)



description

The SN54LVCH244A octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVCH244A octal buffer/line driver is designed for 1.65-V to 3.6-V V_{CC} operation.

These devices are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, these devices pass data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVCH244A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVCH244A is characterized for operation from -40°C to 85°C .

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

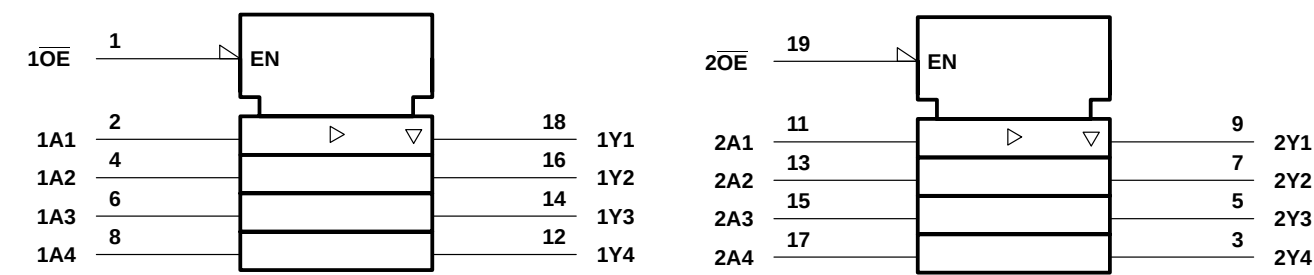
SN54LVCH244A, SN74LVCH244A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each buffer)

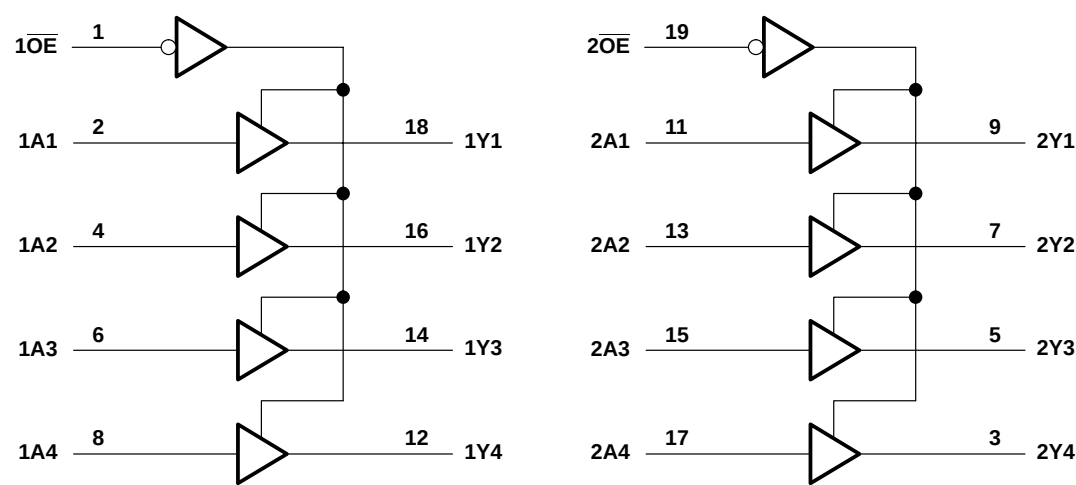
INPUTS		OUTPUT Y
OE	A	
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVCH244A, SN74LVCH244A

OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVCH244A		SN74LVCH244A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	Operating		2	3.6	1.65	3.6	V
	Data retention only		1.5		1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V				$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V				1.7		
	$V_{CC} = 2.7$ V to 3.6 V		2		2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V				$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V				0.7		
	$V_{CC} = 2.7$ V to 3.6 V			0.8	0.8		
V_I Input voltage			0	5.5	0	5.5	V
V_O Output voltage	High or low state		0	V_{CC}	0	V_{CC}	V
	3 state		0	5.5	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V				–4		mA
	$V_{CC} = 2.3$ V				–8		
	$V_{CC} = 2.7$ V			–12	–12		
	$V_{CC} = 3$ V			–24	–24		
I_{OL} Low-level output current	$V_{CC} = 1.65$ V				4		mA
	$V_{CC} = 2.3$ V				8		
	$V_{CC} = 2.7$ V			12	12		
	$V_{CC} = 3$ V			24	24		
$\Delta t/\Delta v$ Input transition rise or fall rate			0	10	0	10	ns/V
T_A Operating free-air temperature			–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVCH244A, SN74LVCH244A

OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCES009G – JULY 1995 - REVISED JUNE 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	SN54LVCH244A			SN74LVCH244A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OH}	I _{OH} = –100 μA		1.65 V to 3.6 V				V _{CC} –0.2			V
			2.7 V to 3.6 V	V _{CC} –0.2						
	I _{OH} = –4 mA		1.65 V				1.2			
	I _{OH} = –8 mA		2.3 V				1.7			
	I _{OH} = –12 mA		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	I _{OH} = –24 mA		3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA		1.65 V to 3.6 V				0.2			V
			2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA		1.65 V				0.45			
	I _{OL} = 8 mA		2.3 V				0.7			
	I _{OL} = 12 mA		2.7 V	0.4			0.4			
	I _{OL} = 24 mA		3 V	0.55			0.55			
I _I	V _I = 0 to 5.5 V		3.6 V	±5			±5			μA
I _{off}	V _I or V _O = 5.5 V		0				±10			μA
I _{I(hold)}	V _I = 0.58 V		1.65 V				‡			μA
	V _I = 1.07 V						‡			
	V _I = 0.7 V		2.3 V				45			
	V _I = 1.7 V						–45			
I _{I(hold)}	V _I = 0.8 V		3 V	75			75			μA
	V _I = 2 V			–75			–75			
	V _I = 0 to 3.6 V [§]		3.6 V	±500			±500			
I _{OZ}	V _O = 0 to 5.5 V		3.6 V	±15			±10			μA
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	10			10			μA
	3.6 V ≤ V _I ≤ 5.5 V [¶]			10			10			
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND		3.3 V	4 12			4			pF
C _O	V _O = V _{CC} or GND		3.3 V	5.5 12			5.5			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This information was not available at the time of publication.

[§] This is the bus-hold maximum dynamic current required to switch the input from one state to another.

[¶] This applies in the disabled state only.

SN54LVCH244A, SN74LVCH244A
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVCH244A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A	Y	7.5		1	6.5	ns
t _{en}	$\overline{OE}$	Y	9		1	8	ns
t _{dis}	$\overline{OE}$	Y	8		1	7	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVCH244A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	†	†	†	†	6.9		1.5	5.9	ns
t _{en}	$\overline{OE}$	Y	†	†	†	†	8.6		1	7.6	ns
t _{dis}	$\overline{OE}$	Y	†	†	†	†	6.8		1.5	5.8	ns

† This information was not available at the time of publication.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	$f = 10\text{ MHz}$	†	†	47	pF
		Outputs disabled		†	†	2	

† This information was not available at the time of publication.

SN54LVCH244A, SN74LVCH244A

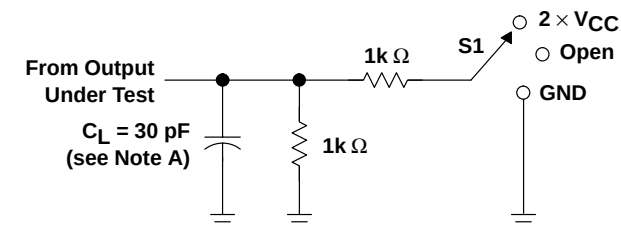
OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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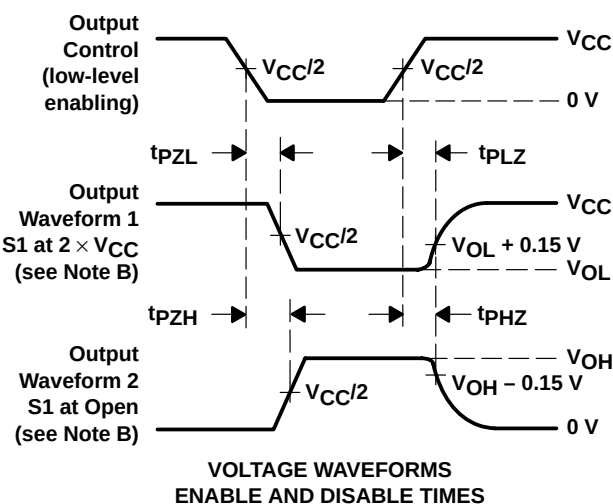
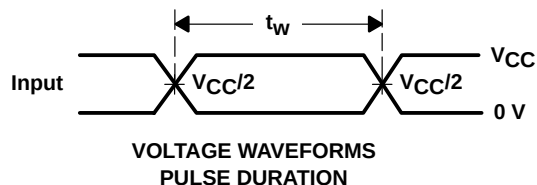
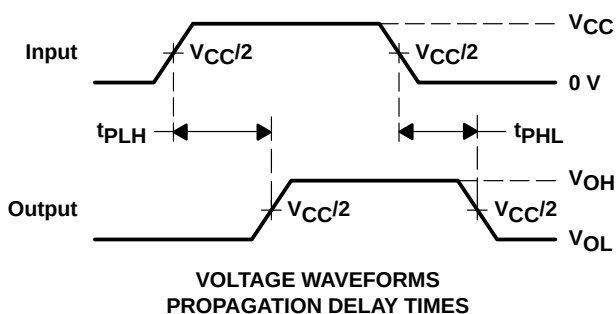
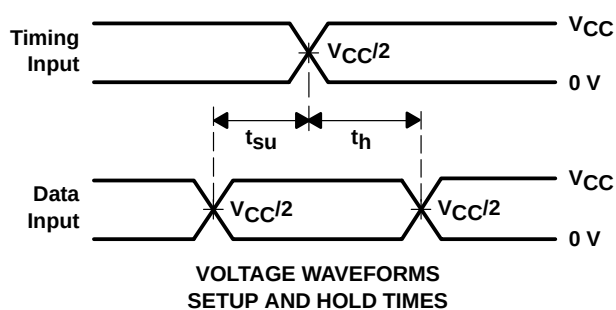
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	Open

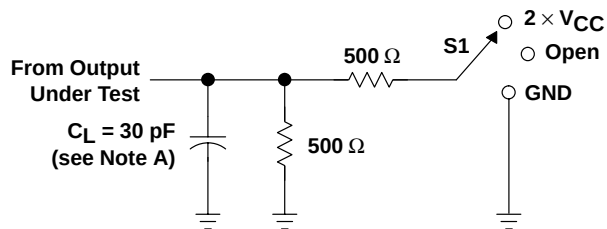


- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

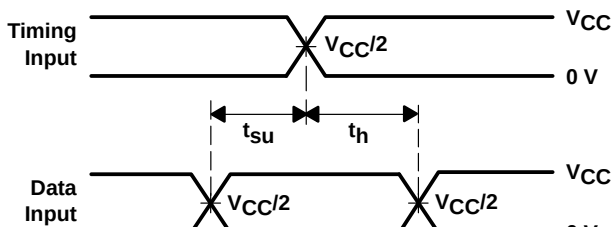
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

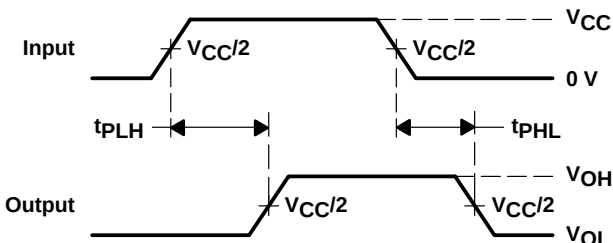


LOAD CIRCUIT

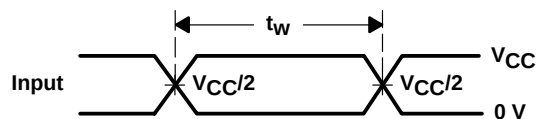
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



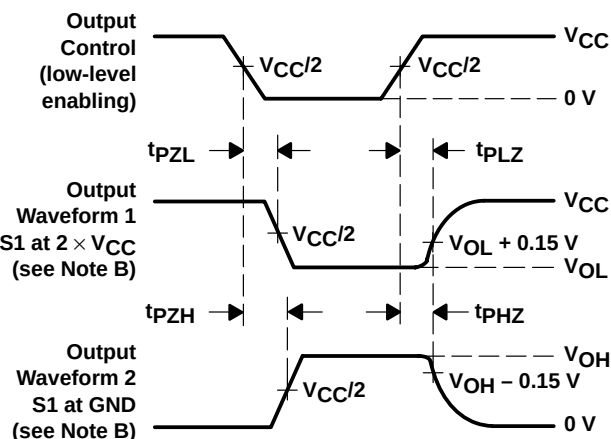
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN54LVCH244A, SN74LVCH244A

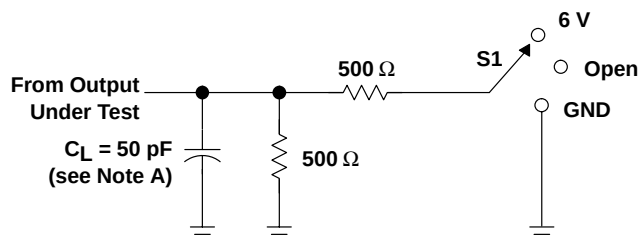
OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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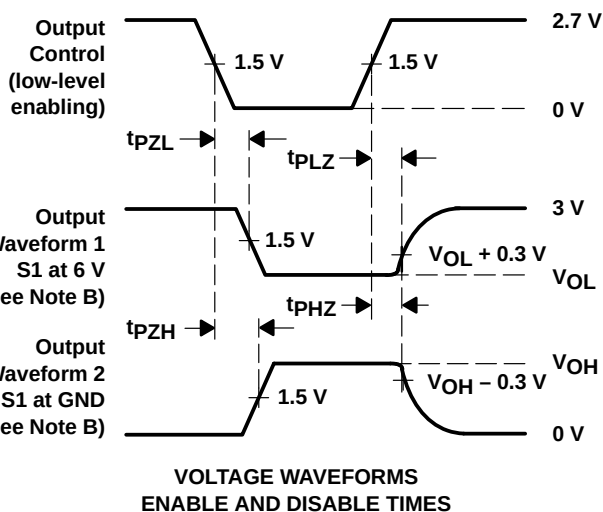
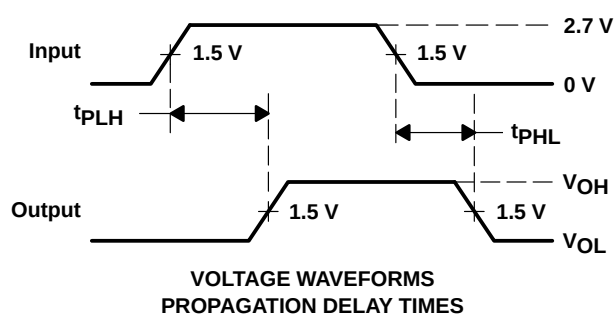
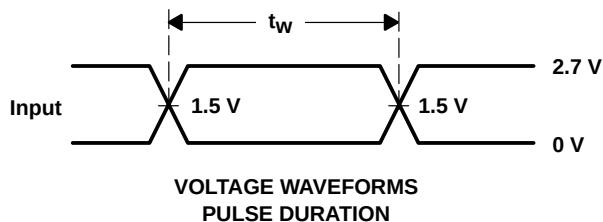
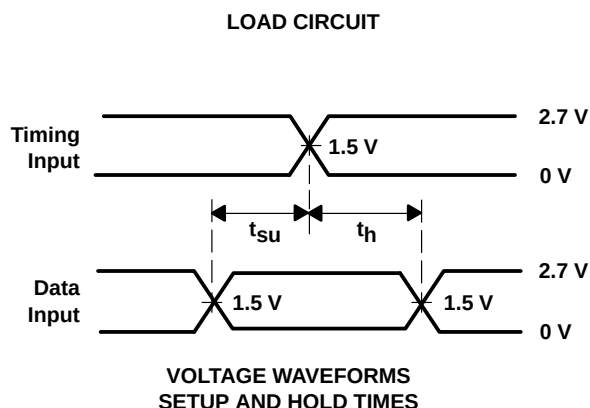
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

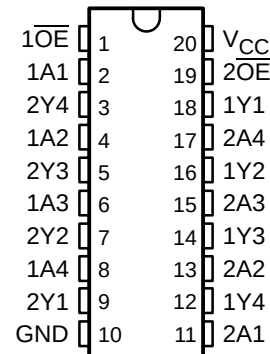
Figure 3. Load Circuit and Voltage Waveforms

SN74LVC2244A OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/line driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC2244A is organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC2244A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Z

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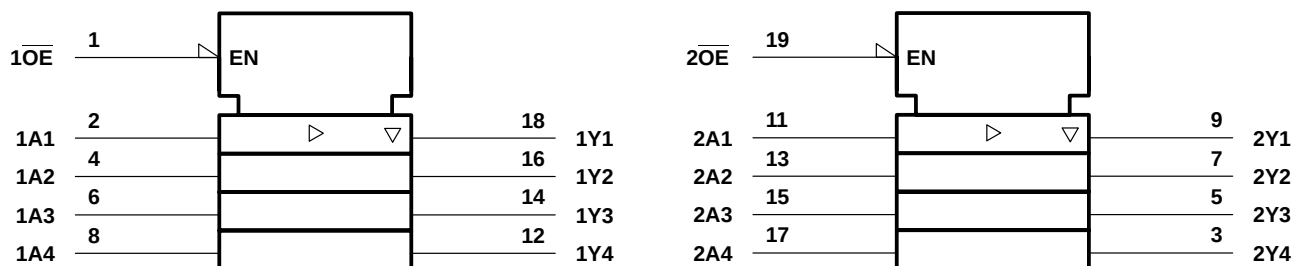
SN74LVC2244A

OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

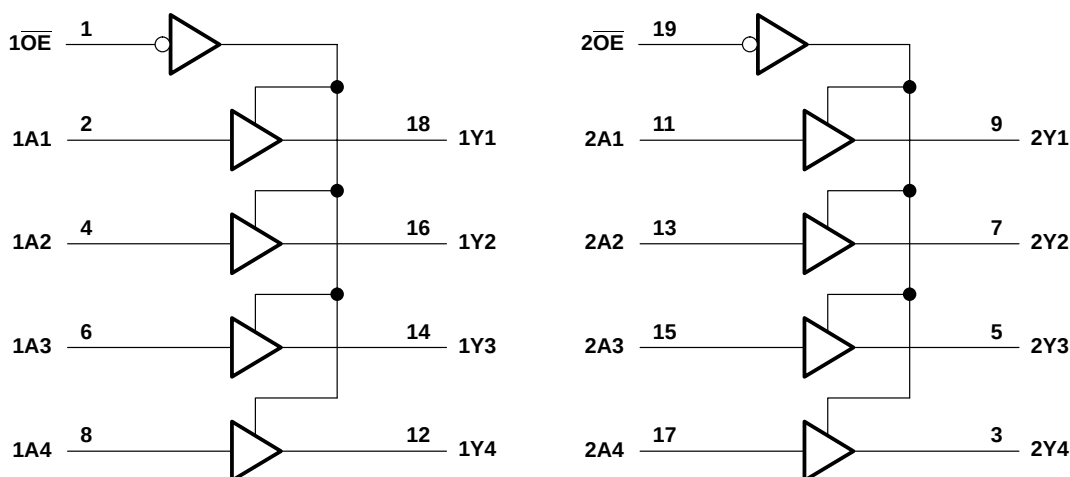
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

SN74LVC2244A
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	High or low state	0	V _{CC}	V
		3 state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V	−2		mA
		V _{CC} = 2.3 V	−4		
		V _{CC} = 2.7 V	−8		
		V _{CC} = 3 V	−12		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	2		mA
		V _{CC} = 2.3 V	4		
		V _{CC} = 2.7 V	8		
		V _{CC} = 3 V	12		
Δt/Δv	Input transition rise or fall rate	0	10	ns/V	
T _A	Operating free-air temperature	−40	85	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC2244A

OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} – 0.2			V
	I _{OH} = –2 mA	1.65 V	1.2			
	I _{OH} = –4 mA	2.3 V	1.7			
		2.7 V	2.2			
	I _{OH} = –6 mA	3 V	2.4			
	I _{OH} = –8 mA	2.7 V	2			
	I _{OH} = –12 mA	3 V	2			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 2 mA	1.65 V	0.45			
	I _{OL} = 4 mA	2.3 V	0.7			
		2.7 V	0.4			
	I _{OL} = 6 mA	3 V	0.55			
	I _{OL} = 8 mA	2.7 V	0.6			
	I _{OL} = 12 mA	3 V	0.8			
I _I	V _I = 0 to 5.5 V	3.6 V	±5			µA
I _{off}	V _I or V _O = 5.5 V	0	±10			µA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V	±10			µA
I _{CC}	V _I = V _{CC} or GND	3.6 V	10			µA
	3.6 V ≤ V _I ≤ 5.5 V [‡]		10			
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			µA
C _i	V _I = V _{CC} or GND	3.3 V	4			pF
C _O	V _O = V _{CC} or GND	3.3 V	5.5			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	§	§	§	§	6.4		1.5	5.5	ns
t _{en}	$\overline{\text{OE}}$	Y	§	§	§	§	8.1		1	7.1	ns
t _{dis}	$\overline{\text{OE}}$	Y	§	§	§	§	7.3		1.5	6.8	ns

§ This information was not available at the time of publication.

operating characteristics, T_A = 25°C

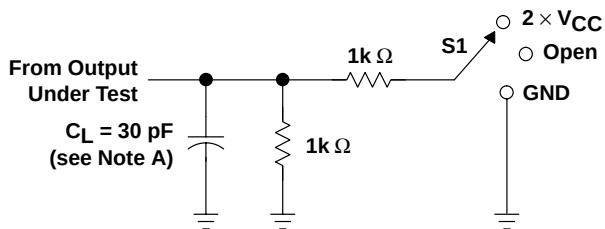
PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	§	§	46	pF
		Outputs disabled		§	§	2	

§ This information was not available at the time of publication.



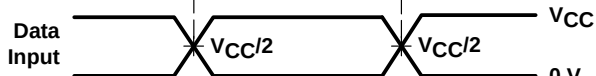
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

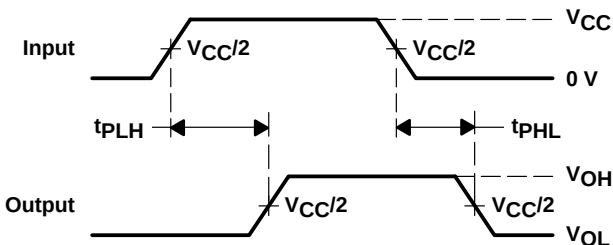


LOAD CIRCUIT

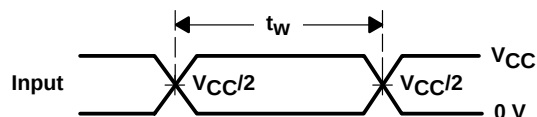
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



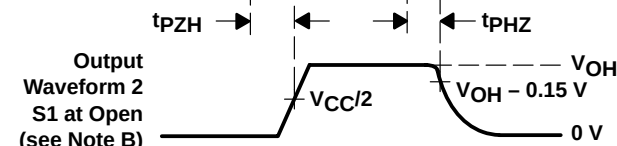
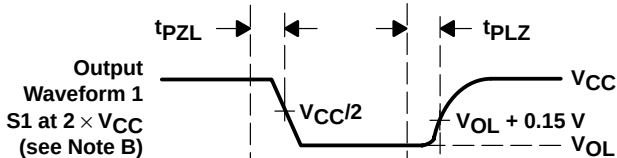
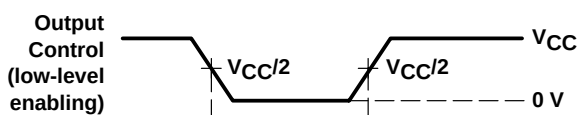
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC2244A

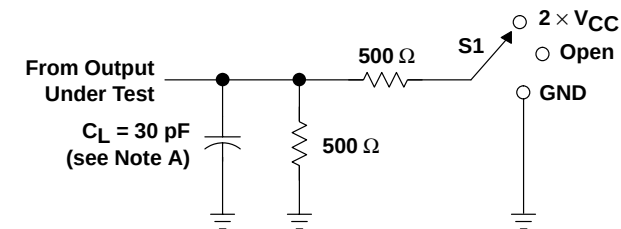
OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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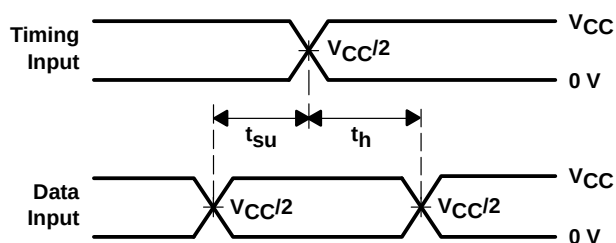
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

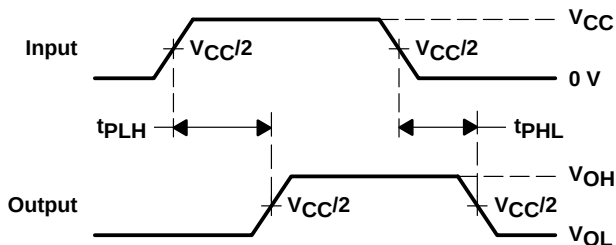


LOAD CIRCUIT

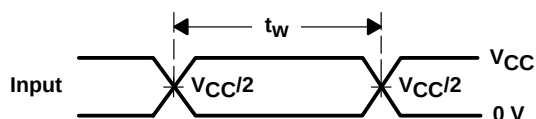
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



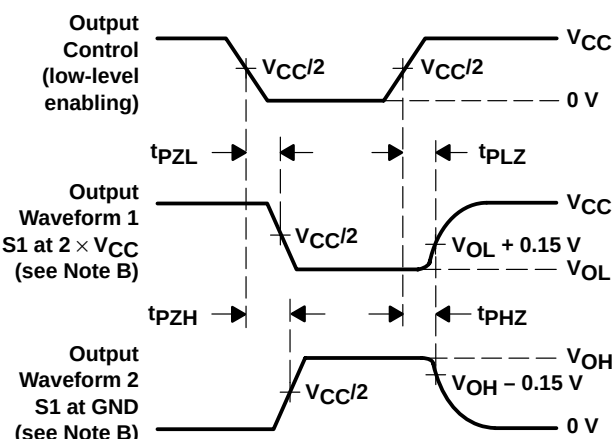
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



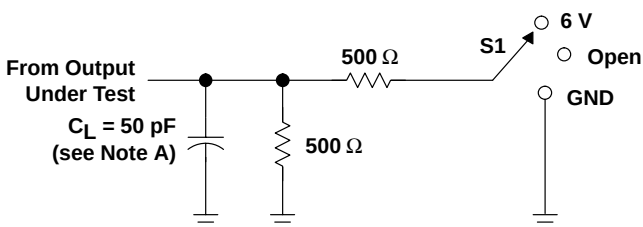
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

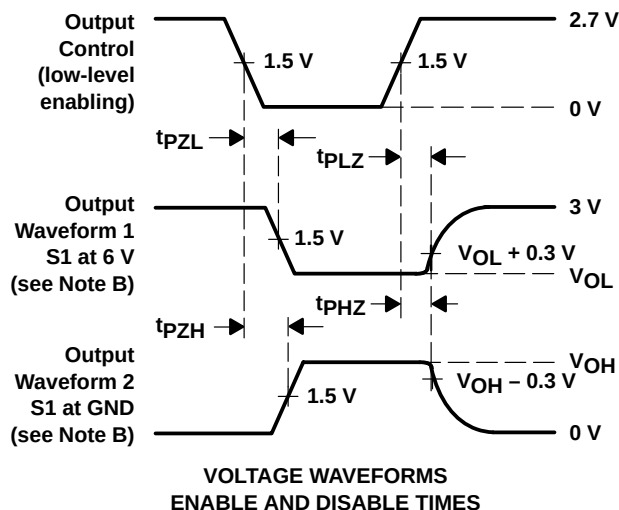
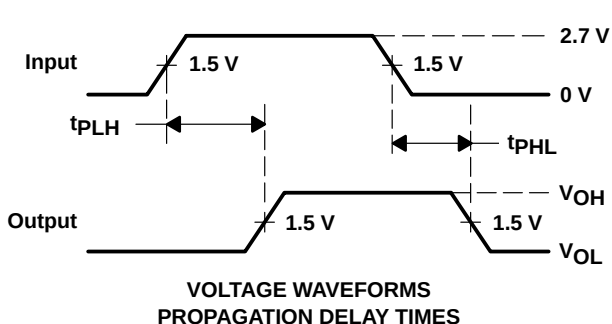
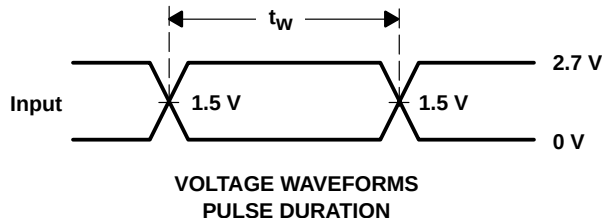
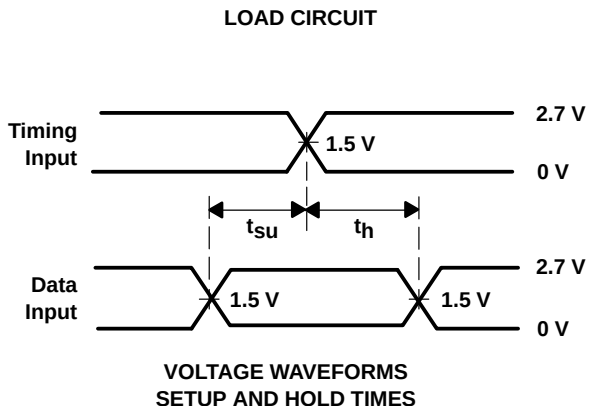
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

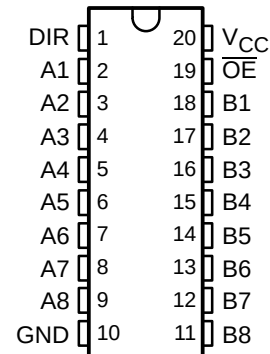
Figure 3. Load Circuit and Voltage Waveforms

SN74LVC245A OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS218I – JANUARY 1993 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Power Off Disables Outputs, Permitting Live Insertion
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC245A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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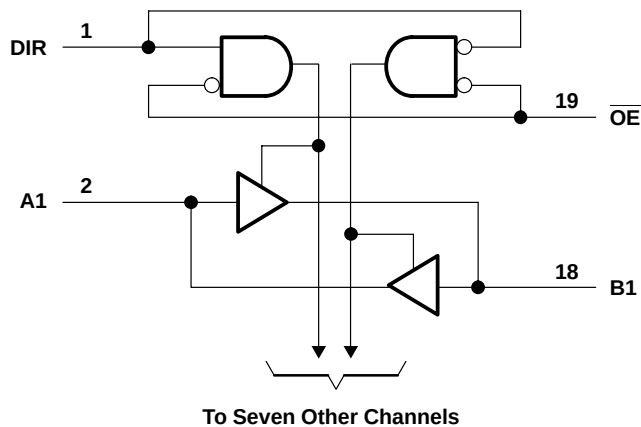
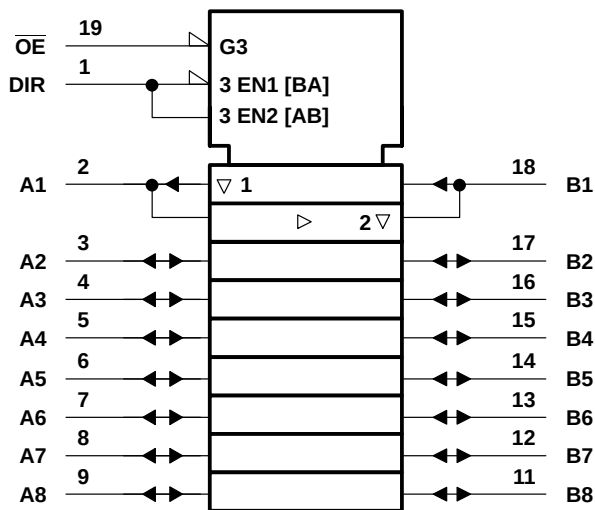
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SN74LVC245A

OCTAL BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCAS218I – JANUARY 1993 – REVISED JUNE 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I : (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74LVC245A

OCTAL BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}		I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
		I _{OH} = –4 mA	1.65 V	1.2			
		I _{OH} = –8 mA	2.3 V	1.7			
		I _{OH} = –12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = –24 mA	3 V	2.2			
V _{OL}		I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
		I _{OL} = 4 mA	1.65 V	0.45			
		I _{OL} = 8 mA	2.3 V	0.7			
		I _{OL} = 12 mA	2.7 V	0.4			
		I _{OL} = 24 mA	3 V	0.55			
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V	±5			µA
I _{off}		V _I or V _O = 5.5 V	0	±10			µA
I _{OZ} [‡]		V _O = 0 to 5.5 V	3.6 V	±10			µA
I _{CC}		V _I = V _{CC} or GND	3.6 V	10			µA
		3.6 V ≤ V _I ≤ 5.5 V [§]		10			
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	4			pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V	5.5			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	¶	¶	¶	¶	7.3		1.5	6.3	ns
t _{en}	$\overline{\text{OE}}$	A or B	¶	¶	¶	¶	9.5		1.5	8.5	ns
t _{dis}	$\overline{\text{OE}}$	A or B	¶	¶	¶	¶	8.5		1.7	7.5	ns
t _{sk(o)} [#]									1		ns

¶ This information was not available at the time of publication.

[#] Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

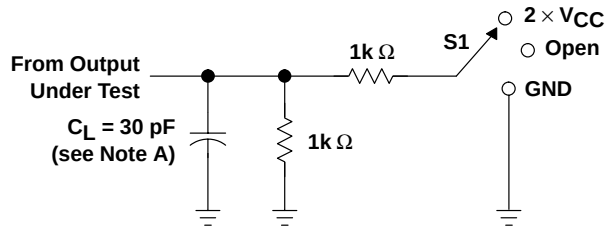
PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	¶	¶	45	pF
		Outputs disabled	¶	¶	2	

¶ This information was not available at the time of publication.



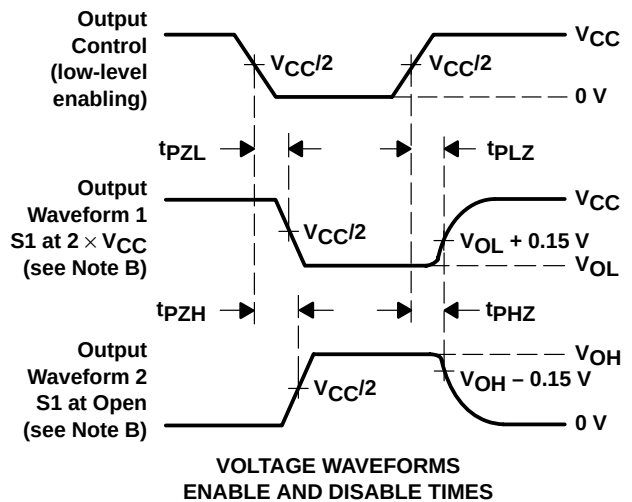
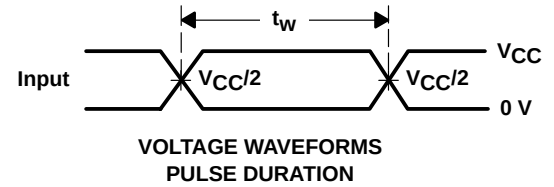
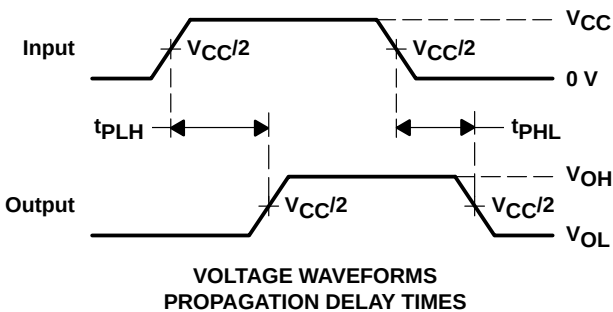
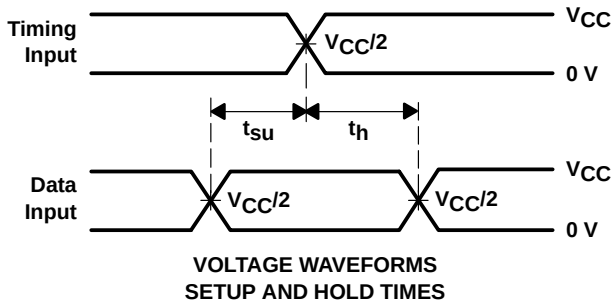
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC245A

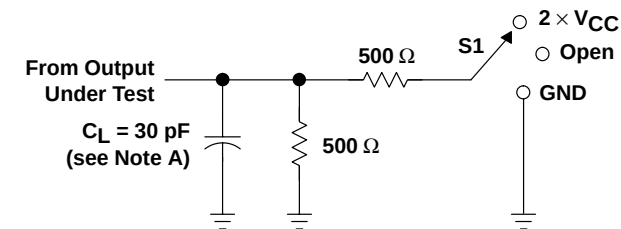
OCTAL BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCAS2181 – JANUARY 1993 – REVISED JUNE 1998

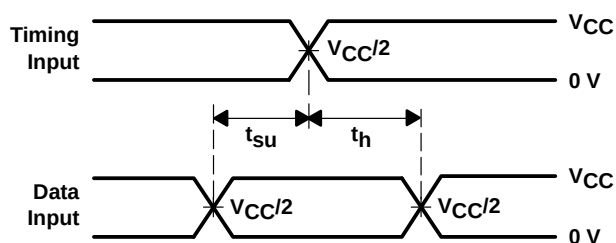
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

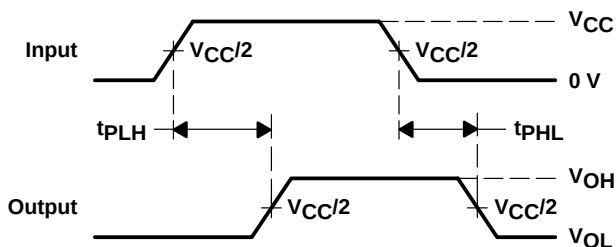


LOAD CIRCUIT

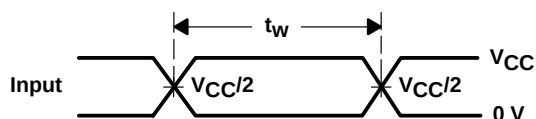
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



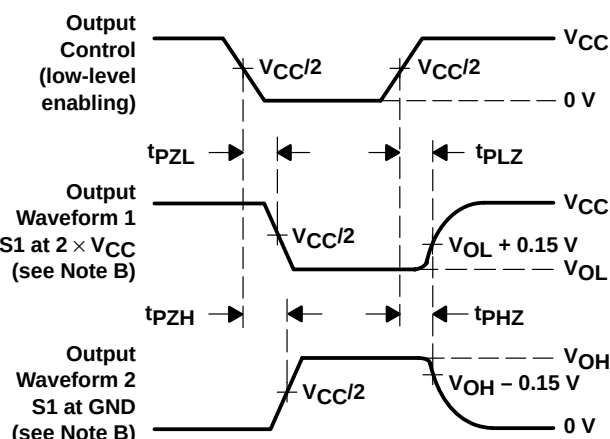
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

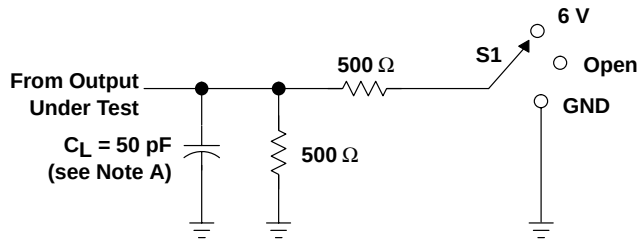


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

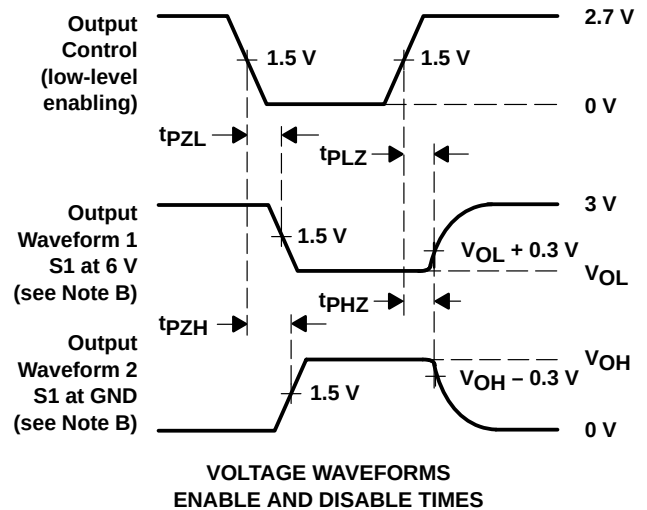
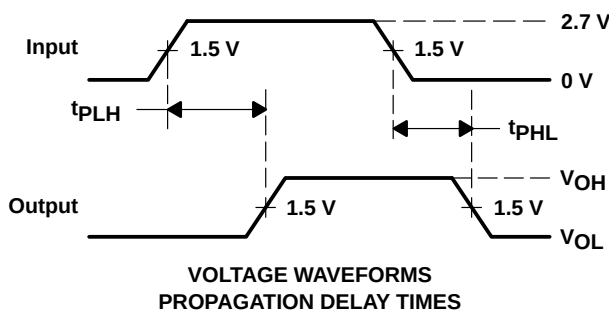
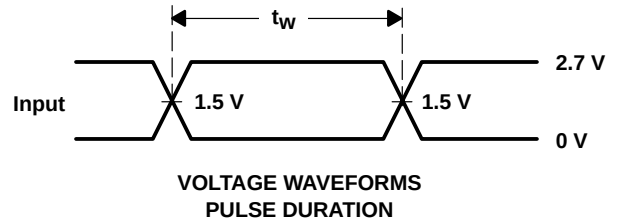
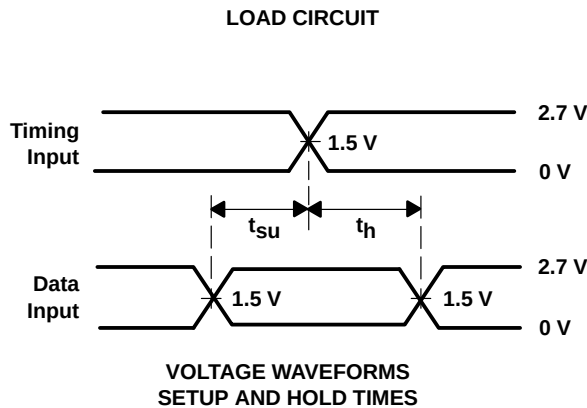
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

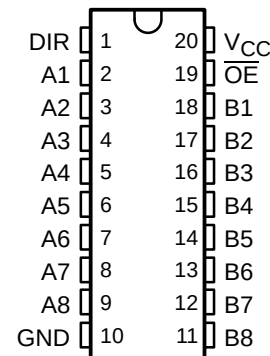
Figure 3. Load Circuit and Voltage Waveforms

SN74LVCR2245A OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS581D – NOVEMBER 1996 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- All Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCR2245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

All outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVCR2245A is characterized for operation from -40°C to 85°C .

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN74LVCR2245A

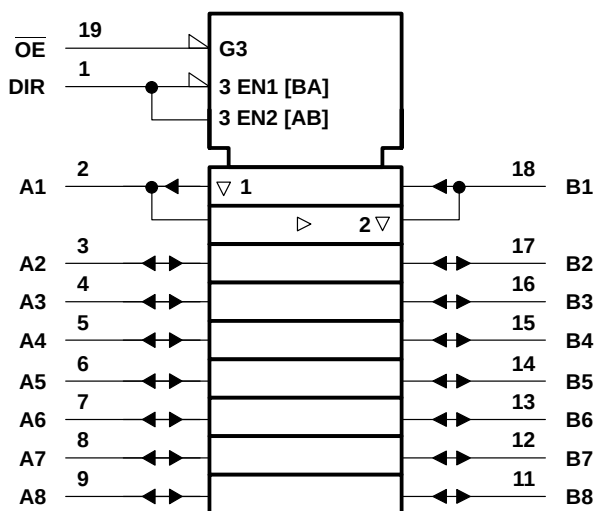
OCTAL BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCAS581D – NOVEMBER 1996 – REVISED JUNE 1998

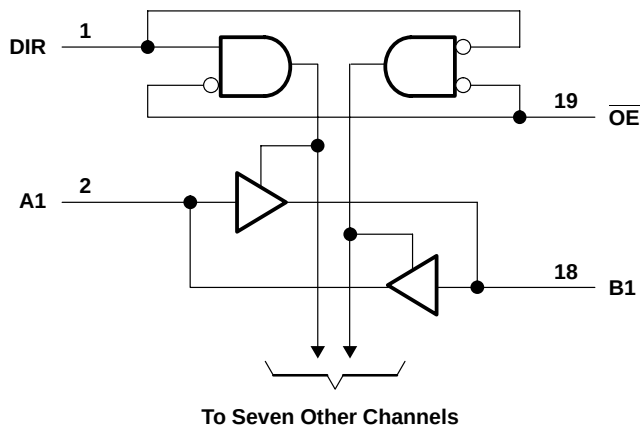
FUNCTION TABLE

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol[†]

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVCR2245A

OCTAL BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I : (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–2	mA
	$V_{CC} = 2.3$ V		–4	
	$V_{CC} = 2.7$ V		–8	
	$V_{CC} = 3$ V		–12	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		2	mA
	$V_{CC} = 2.3$ V		4	
	$V_{CC} = 2.7$ V		8	
	$V_{CC} = 3$ V		12	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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OCTAL BUS TRANSCEIVER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}		I _{OH} = −100 μA	1.65 V to 3.6 V	V _{CC} −0.2			V
		I _{OH} = −2 mA	1.65 V	1.2			
		I _{OH} = −4 mA	2.3 V	1.7			
			2.7 V	2.2			
		I _{OH} = −6 mA	3 V	2.4			
		I _{OH} = −8 mA	2.7 V	2			
		I _{OH} = −12 mA	3 V	2			
V _{OL}		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
		I _{OL} = 2 mA	1.65 V			0.45	
		I _{OL} = 4 mA	2.3 V			0.7	
			2.7 V			0.4	
		I _{OL} = 6 mA	3 V			0.55	
		I _{OL} = 8 mA	2.7 V			0.6	
		I _{OL} = 12 mA	3 V			0.8	
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V			±5	μA
I _{off}		V _I or V _O = 5.5 V	0			±10	μA
I _{OZ} [‡]		V _O = 0 to 5.5 V	3.6 V			±10	μA
I _{CC}		V _I = V _{CC} or GND,	3.6 V			10	μA
		3.6 V ≤ V _I ≤ 5.5 V [§]				10	
ΔI _{CC}		One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V			4	pF
C _{i0}	A or B ports	V _O = V _{CC} or GND	3.3 V			5.5	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	¶	¶	¶	¶	7.3		1.5	6.3	ns
t _{en}	$\overline{OE}$	A or B	¶	¶	¶	¶	9.5		1.5	8.2	ns
t _{dis}	$\overline{OE}$	A or B	¶	¶	¶	¶	8.5		1.7	7.8	ns
t _{sk(o)} [#]										1	ns

¶ This information was not available at the time of publication.

[#] Skew between any two outputs of the same package switching in the same direction



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WITH 3-STATE OUTPUTS

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operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	$f = 10\text{ MHz}$	†	†	48	pF
	Outputs disabled		†	†	4	

† This information was not available at the time of publication.

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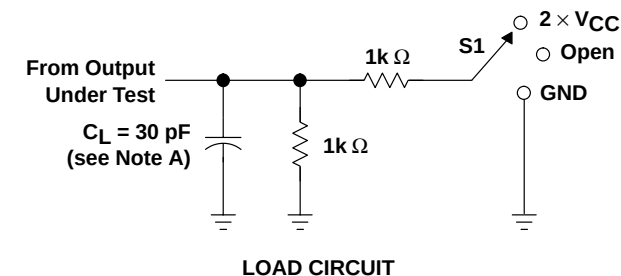
OCTAL BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

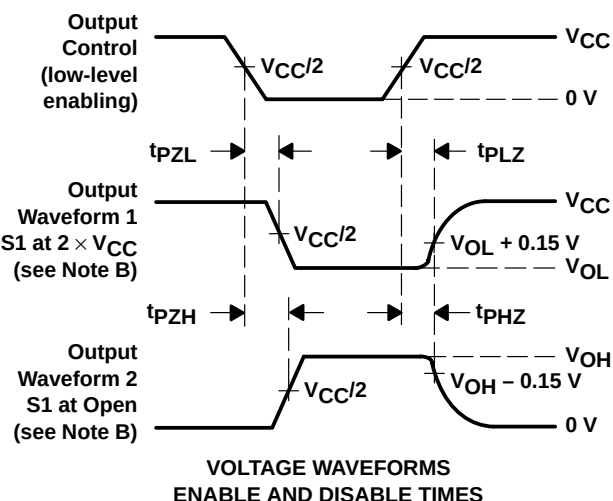
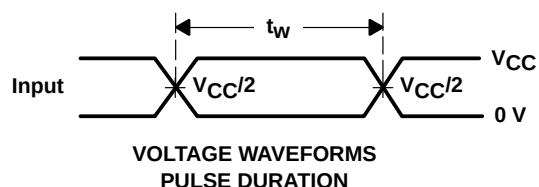
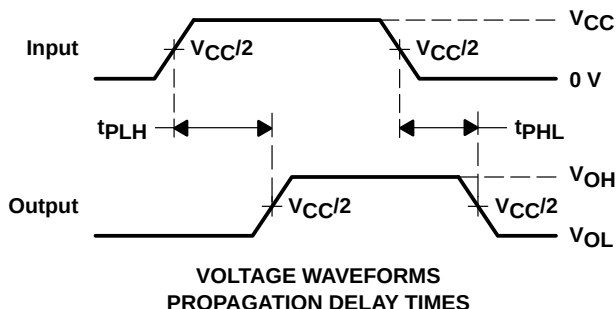
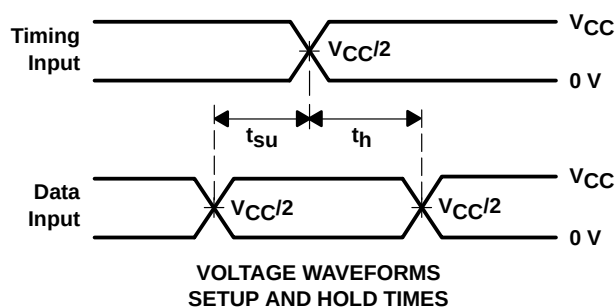
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PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open

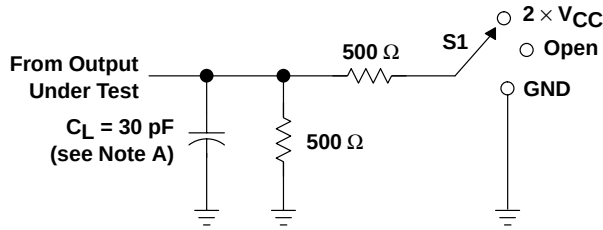


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

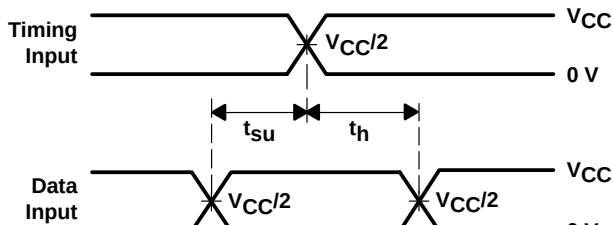
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

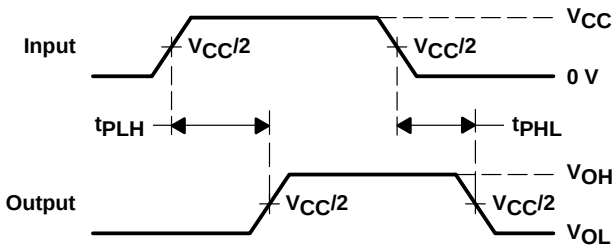


LOAD CIRCUIT

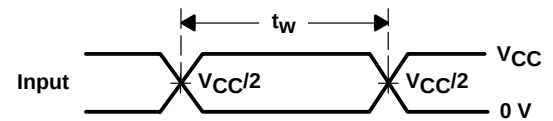
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



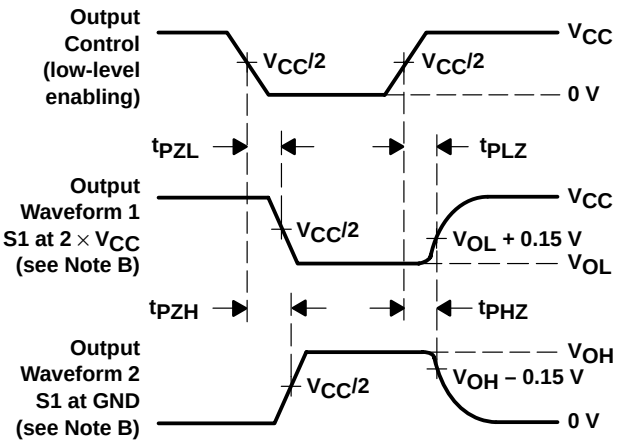
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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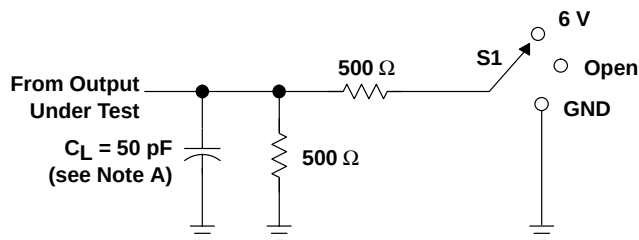
OCTAL BUS TRANSCEIVER

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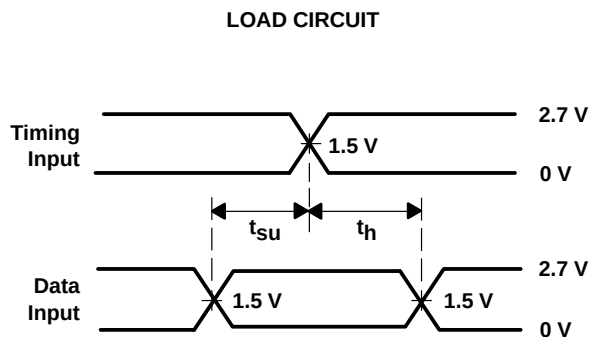
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$

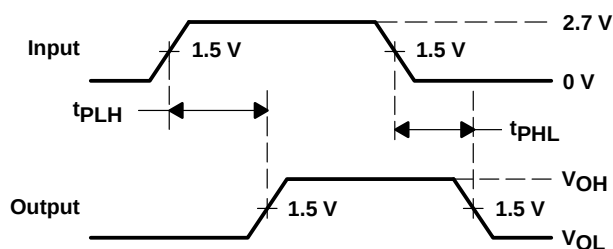


LOAD CIRCUIT

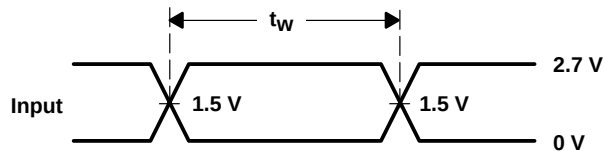
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



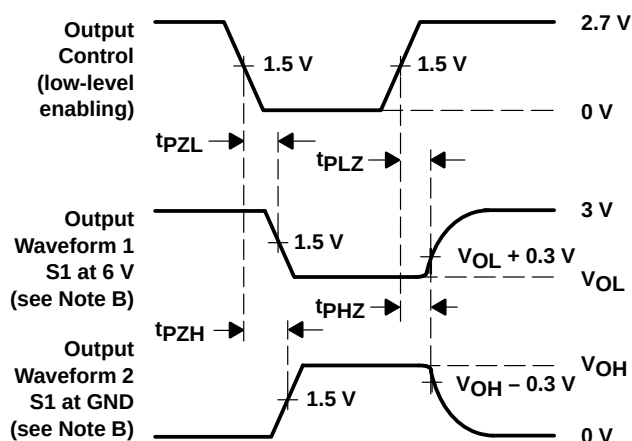
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

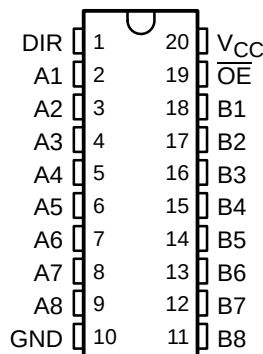
Figure 3. Load Circuit and Voltage Waveforms

SN54LVCH245A, SN74LVCH245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

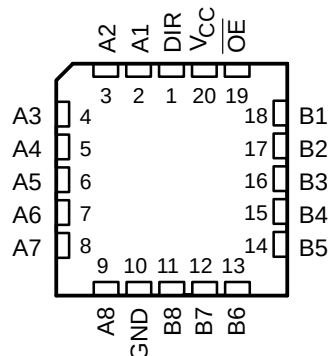
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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Package, Ceramic Chip Carriers (FK), and DIPs (J)

SN54LVCH245A . . . J OR W PACKAGE
SN74LVCH245A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVCH245A . . . FK PACKAGE
(TOP VIEW)



description

The SN54LVCH245A octal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVCH245A octal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

These devices are designed for asynchronous communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVCH245A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVCH245A is characterized for operation from -40°C to 85°C .

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

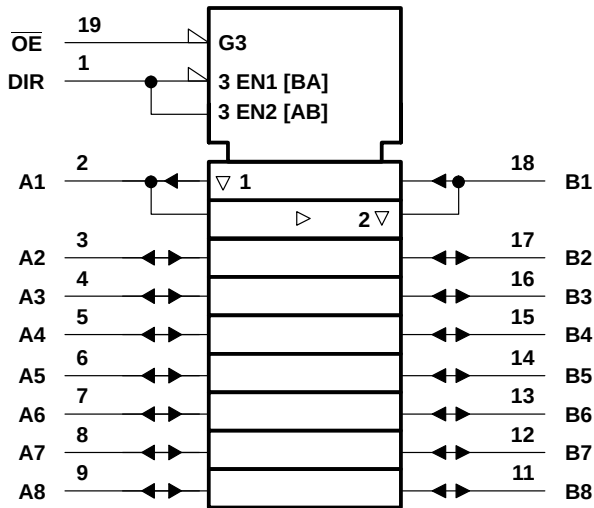
SN54LVCH245A, SN74LVCH245A
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

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FUNCTION TABLE

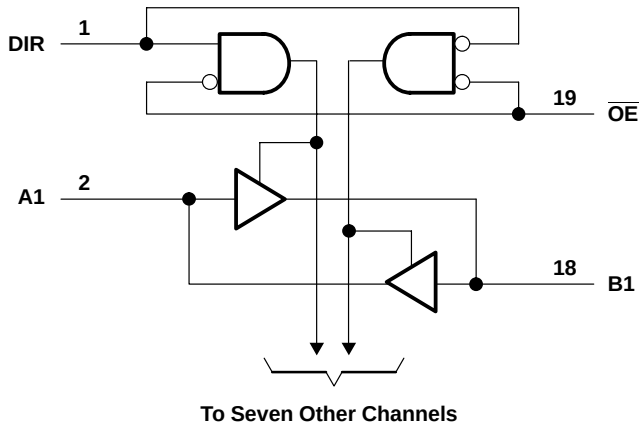
INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I : (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVCH245A		SN74LVCH245A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	Operating		2	3.6	1.65	3.6	V
	Data retention only		1.5		1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V				$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V				1.7		
	$V_{CC} = 2.7$ V to 3.6 V		2		2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V				$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V				0.7		
	$V_{CC} = 2.7$ V to 3.6 V			0.8	0.8		
V_I Input voltage			0	5.5	0	5.5	V
V_O Output voltage	High or low state		0	V_{CC}	0	V_{CC}	V
	3 state		0	5.5	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V				–4		mA
	$V_{CC} = 2.3$ V				–8		
	$V_{CC} = 2.7$ V			–12	–12		
	$V_{CC} = 3$ V			–24	–24		
I_{OL} Low-level output current	$V_{CC} = 1.65$ V				4		mA
	$V_{CC} = 2.3$ V				8		
	$V_{CC} = 2.7$ V			12	12		
	$V_{CC} = 3$ V			24	24		
$\Delta t/\Delta v$ Input transition rise or fall rate			0	10	0	10	ns/V
T_A Operating free-air temperature			–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	SN54LVCH245A			SN74LVCH245A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V				V _{CC} –0.2			V	
		2.7 V to 3.6 V	V _{CC} –0.2							
	I _{OH} = –4 mA	1.65 V				1.2				
	I _{OH} = –8 mA	2.3 V				1.7				
	I _{OH} = –12 mA	2.7 V	2.2			2.2				
		3 V	2.4			2.4				
I _{OH} = –24 mA		3 V	2.2			2.2				
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.2			V	
		2.7 V to 3.6 V	0.2							
	I _{OL} = 4 mA	1.65 V				0.45				
	I _{OL} = 8 mA	2.3 V				0.7				
	I _{OL} = 12 mA	2.7 V	0.4			0.4				
	I _{OL} = 24 mA	3 V	0.55			0.55				
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V	±5			±5			μA
I _{off}		V _I or V _O = 5.5 V	0				±10			μA
I _I (hold)	V _I = 0.58 V		1.65 V				‡			μA
	V _I = 1.07 V						‡			
	V _I = 0.7 V		2.3 V				45			
	V _I = 1.7 V						–45			
	V _I = 0.8 V		3 V	75			75			
	V _I = 2 V			–75			–75			
	V _I = 0 to 3.6 V [§]		3.6 V	±500			±500			
I _{OZ} [¶]		V _O = 0 to 5.5 V	3.6 V	±15			±10			μA
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	10			10			μA
	3.6 V ≤ V _I ≤ 5.5 V [#]			10			10			
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500			μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	4 12			4			pF
C _{i0}	A or B ports	V _O = V _{CC} or GND	3.3 V	5.5 12			5.5			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This information was not available at the time of publication.

§ This is the bus-hold maximum dynamic current required to switch the input from one state to another.

¶ For I/O ports, the parameter I_{OZ} includes the input leakage current.

This applies in the disabled state only.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVCH245A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	8		1	7	ns
t _{en}	$\overline{OE}$	A or B	9.5		1	8.5	ns
t _{djs}	$\overline{OE}$	A or B	8.5		1	7.5	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVCH245A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	†	†	†	†	7.3		1.5	6.3	ns
t _{en}	$\overline{OE}$	A or B	†	†	†	†	9.5		1.5	8.5	ns
t _{dis}	$\overline{OE}$	A or B	†	†	†	†	8.5		1.7	7.5	ns
t _{sk(o)} [‡]									1		ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$f = 10\text{ MHz}$	†	†	47	pF
		Outputs disabled		†	†	2	

† This information was not available at the time of publication.

SN54LVCH245A, SN74LVCH245A

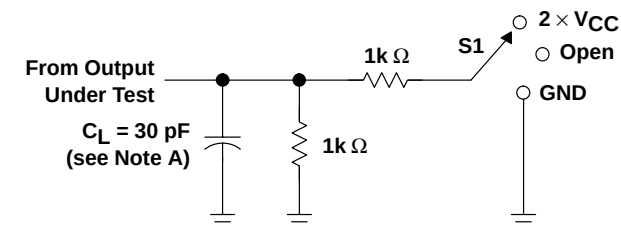
OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCES008F – JULY 1995 - REVISED JUNE 1998

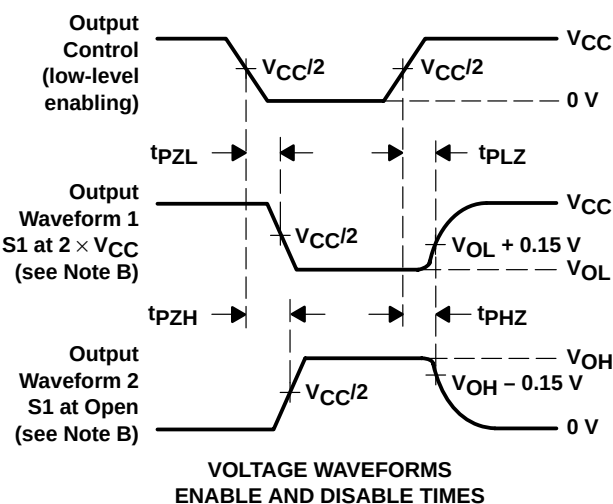
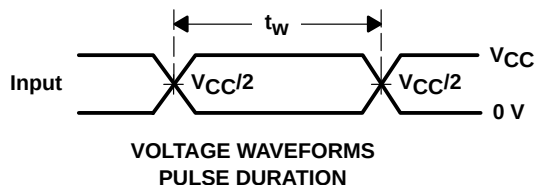
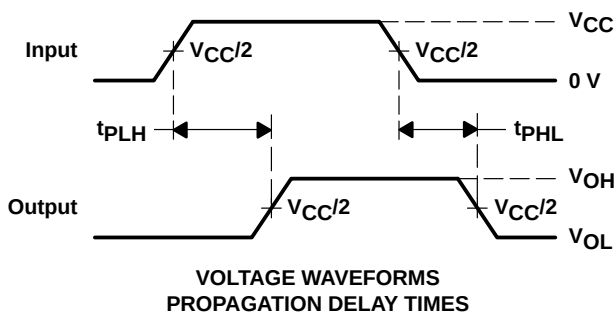
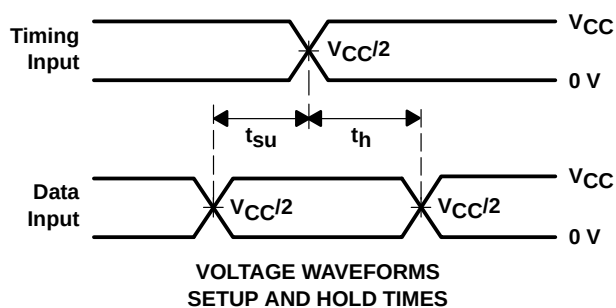
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	Open

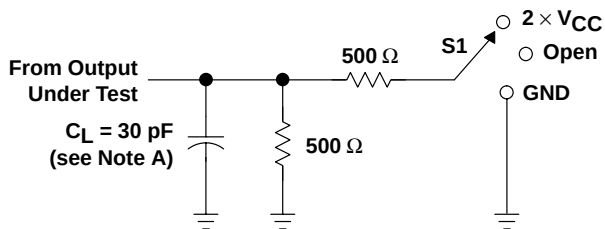


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

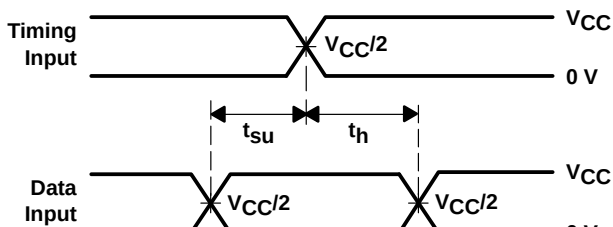
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

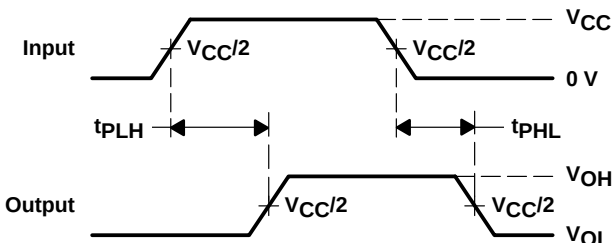


LOAD CIRCUIT

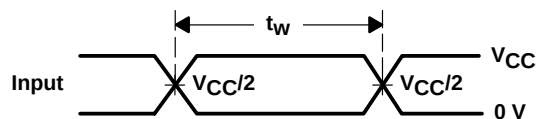
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



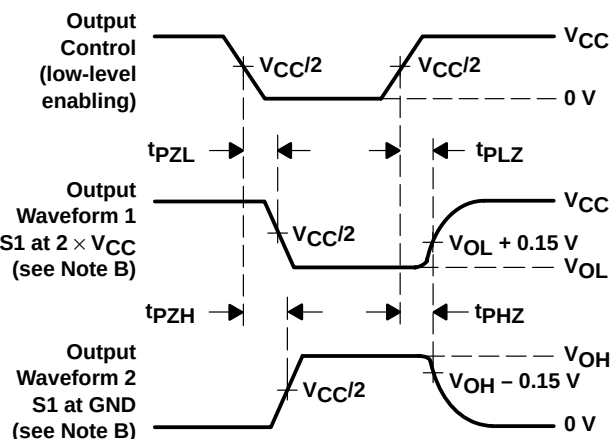
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN54LVCH245A, SN74LVCH245A

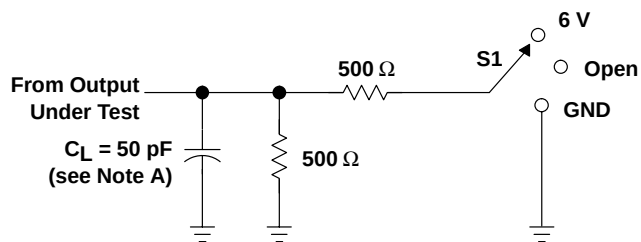
OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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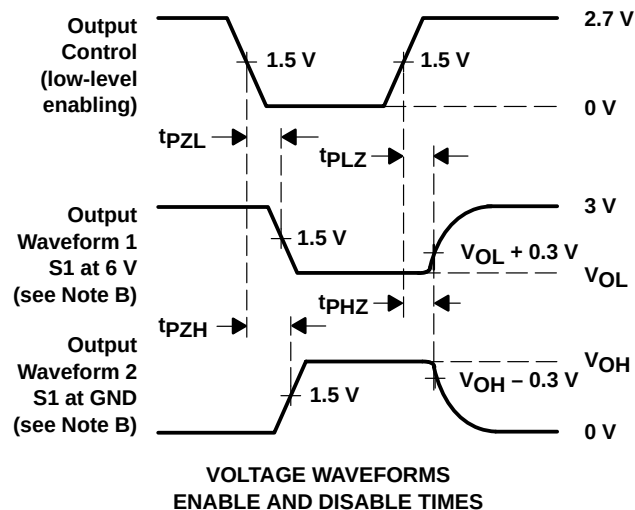
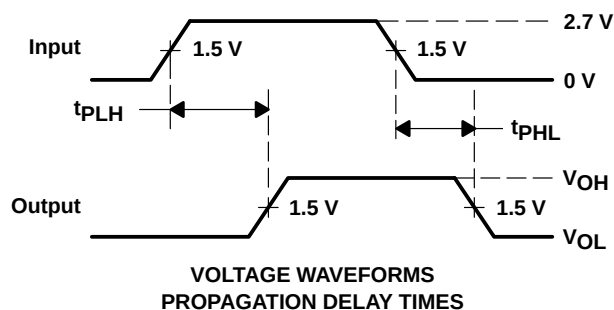
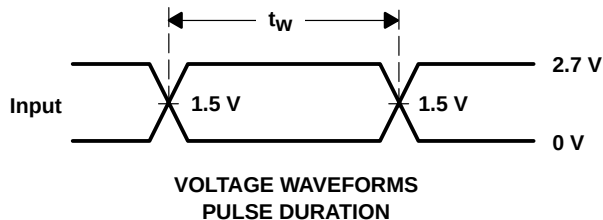
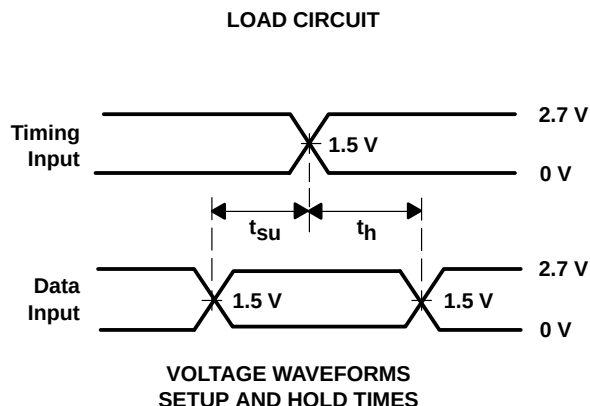
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC373A, SN74LVC373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and DIPs (J)

description

The SN54LVC373A octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC373A octal transparent D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

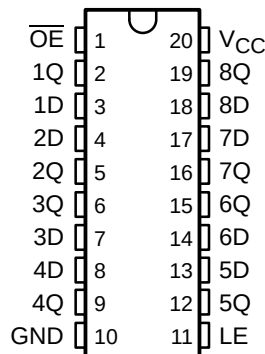
$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

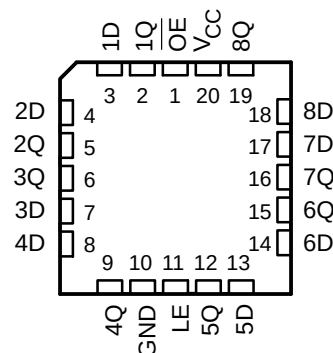
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVC373A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC373A is characterized for operation from -40°C to 85°C .

SN54LVC373A . . . J OR W PACKAGE
SN74LVC373A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVC373A . . . FK PACKAGE
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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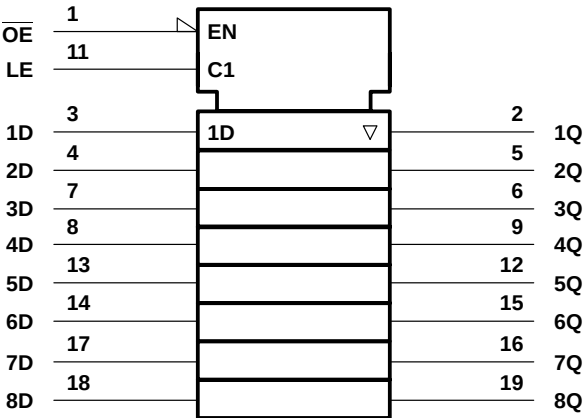
SN54LVC373A, SN74LVC373A
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each latch)

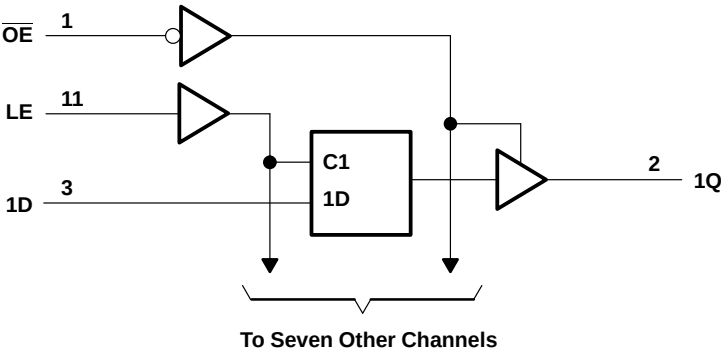
INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVC373A, SN74LVC373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVC373A		SN74LVC373A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	Operating		2	3.6	1.65	3.6	V
	Data retention only		1.5		1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V				$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V				1.7		
	$V_{CC} = 2.7$ V to 3.6 V		2		2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V				$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V				0.7		
	$V_{CC} = 2.7$ V to 3.6 V			0.8	0.8		
V_I Input voltage			0	5.5	0	5.5	V
V_O Output voltage	High or low state		0	V_{CC}	0	V_{CC}	V
	3 state		0	5.5	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V				–4		mA
	$V_{CC} = 2.3$ V				–8		
	$V_{CC} = 2.7$ V			–12	–12		
	$V_{CC} = 3$ V			–24	–24		
I_{OL} Low-level output current	$V_{CC} = 1.65$ V				4		mA
	$V_{CC} = 2.3$ V				8		
	$V_{CC} = 2.7$ V			12	12		
	$V_{CC} = 3$ V			24	24		
$\Delta t/\Delta v$ Input transition rise or fall rate			0	10	0	10	ns/V
T_A Operating free-air temperature			–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVC373A, SN74LVC373A

OCTAL TRANSPARENT D-TYPE LATCHES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	SN54LVC373A			SN74LVC373A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OH}	I _{OH} = –100 μA		1.65 V to 3.6 V				V _{CC} –0.2			V
			2.7 V to 3.6 V	V _{CC} –0.2						
	I _{OH} = –4 mA		1.65 V				1.2			
	I _{OH} = –8 mA		2.3 V				1.7			
	I _{OH} = –12 mA		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	I _{OH} = –24 mA		3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA		1.65 V to 3.6 V				0.2			V
			2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA		1.65 V				0.45			
	I _{OL} = 8 mA		2.3 V				0.7			
	I _{OL} = 12 mA		2.7 V	0.4			0.4			
	I _{OL} = 24 mA		3 V	0.55			0.55			
I _I	V _I = 0 to 5.5 V		3.6 V	±5			±5			μA
I _{off}	V _I or V _O = 5.5 V		0				±10			μA
I _{OZ}	V _O = 0 to 5.5 V		3.6 V	±15			±10			μA
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	10			10			μA
	3.6 V ≤ V _I ≤ 5.5 V‡			10			10			
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND		3.3 V	4	12	4			pF	
C _O	V _O = V _{CC} or GND		3.3 V	5.5	12	5.5			pF	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

		SN54LVC373A				UNIT
		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high	3.3		3.3		ns
t _{SU}	Setup time, data before LE↓	2		2		ns
t _H	Hold time, data after LE↓	2		2		ns



SN54LVC373A, SN74LVC373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		SN74LVC373A								UNIT
		$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high	†		†		3.3		3.3		ns
t _{su}	Setup time, data before LE↓	†		†		2		2		ns
t _h	Hold time, data after LE↓	†		†		1.5		1.5		ns

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC373A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	D	Q	8.5		1	7.5	ns
	LE		9.5		1	8.5	
t _{en}	OE	Q	8.7		1	7.7	ns
t _{djs}	OE	Q	8		0.5	7	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC373A								UNIT
			$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	†	†	†	†	7.8	1.5	6.8	ns	
	LE		†	†	†	†	8.2	2	7.6		
t_{en}	$\overline{OE}$	Q	†	†	†	†	8.7	1.5	7.7	ns	
t_{dis}	$\overline{OE}$	Q	†	†	†	†	7.6	1.5	7	ns	
$t_{sk(o)}^{\ddagger}$									1	ns	

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	$f = 10\text{ MHz}$	†	†	46	pF
		Outputs disabled		†	†	3	

† This information was not available at the time of publication.

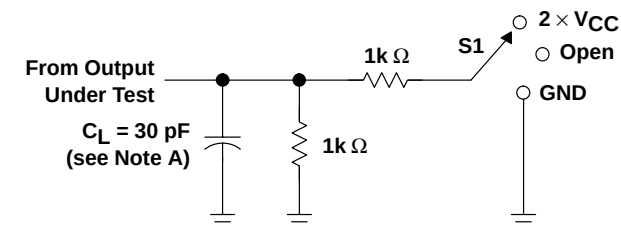


SN54LVC373A, SN74LVC373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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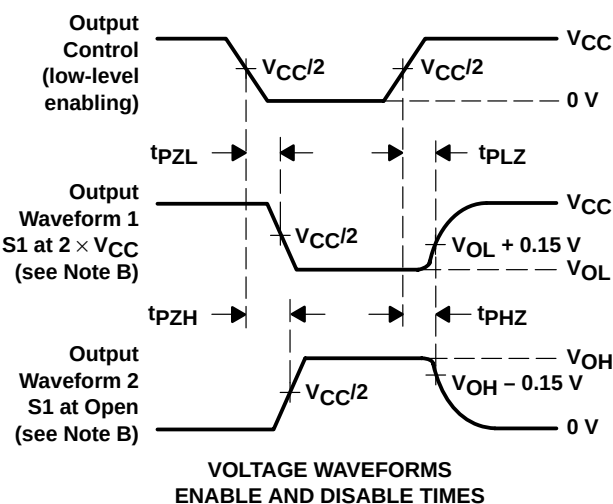
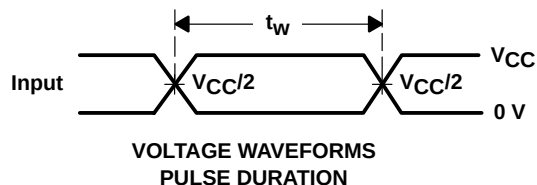
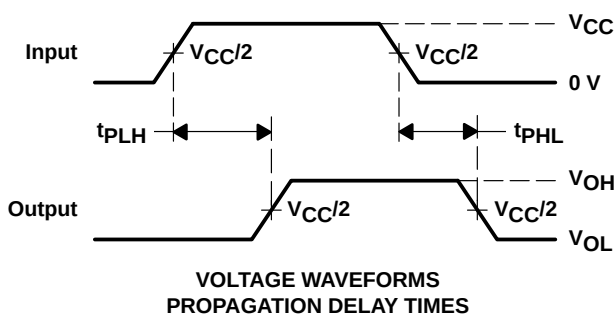
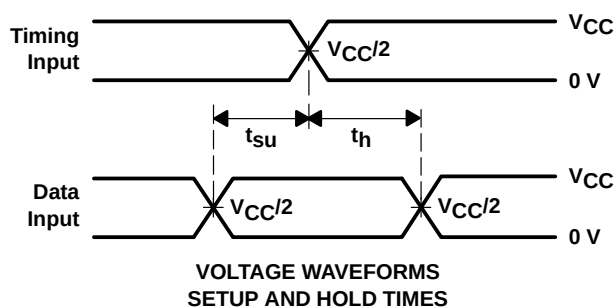
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHZ}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

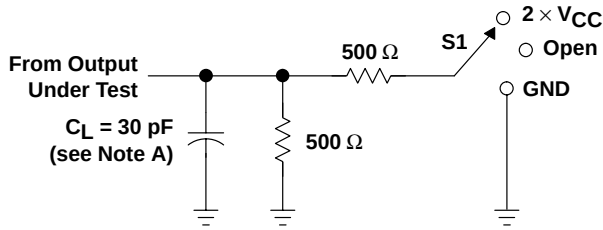
Figure 1. Load Circuit and Voltage Waveforms

SN54LVC373A, SN74LVC373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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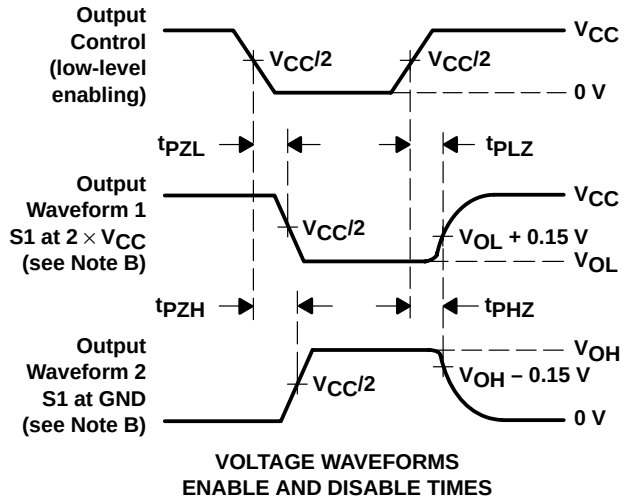
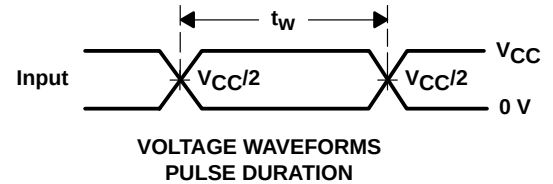
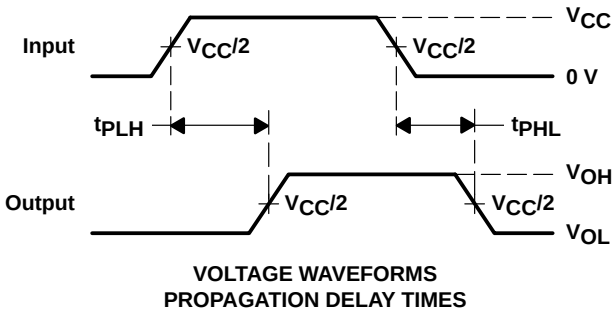
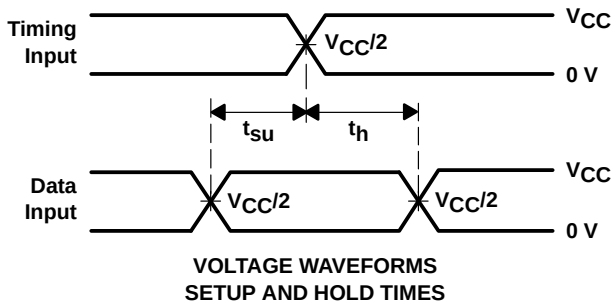
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHZ}	GND



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN54LVC373A, SN74LVC373A

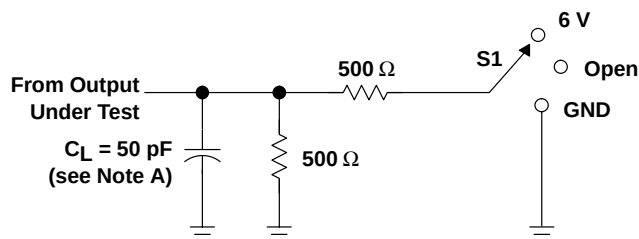
OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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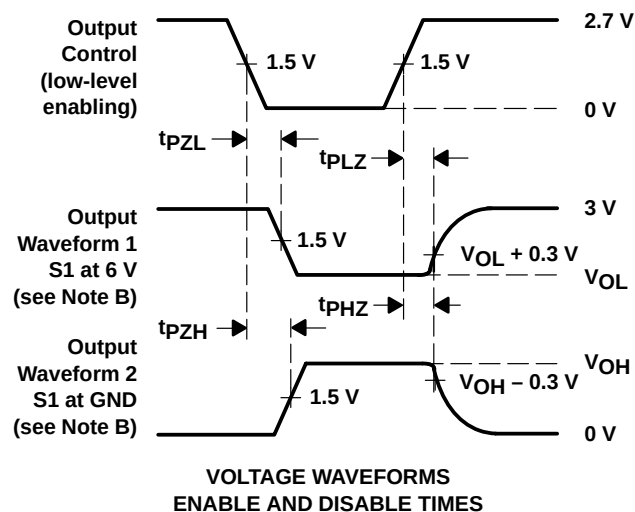
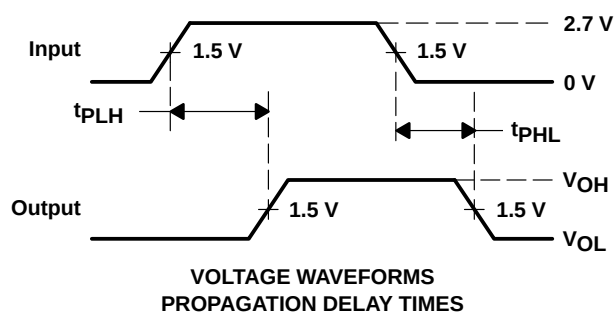
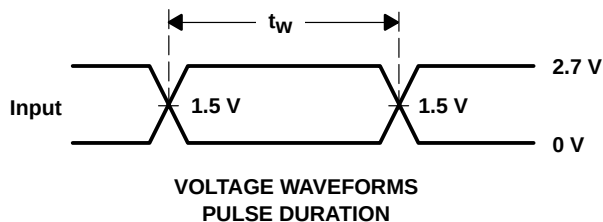
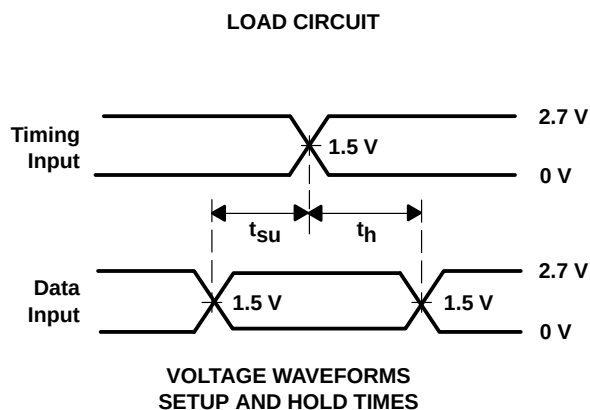
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC374A, SN74LVC374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Inputs/Outputs, Permitting Live Insertion
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and DIPs (J)

description

The SN54LVC374A octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC374A octal edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

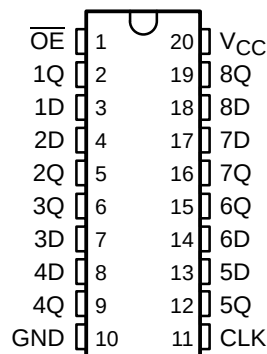
On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

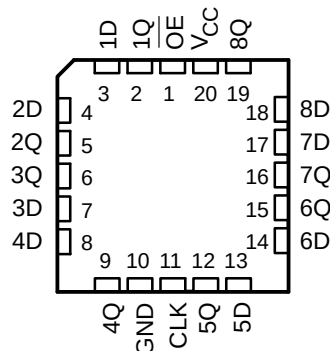
$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

SN54LVC374A . . . J OR W PACKAGE
SN74LVC374A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVC374A . . . FK PACKAGE
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVC374A, SN74LVC374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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description (continued)

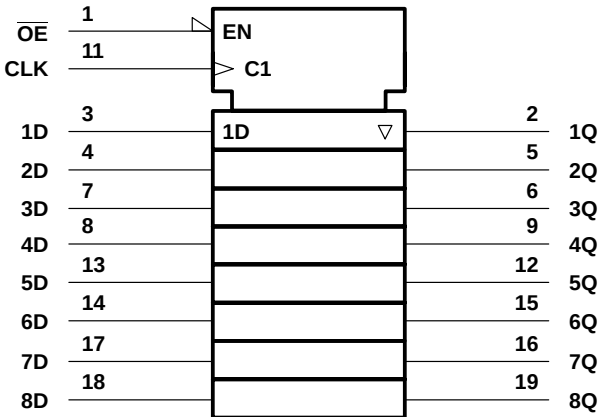
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVC374A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC374A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each flip-flop)

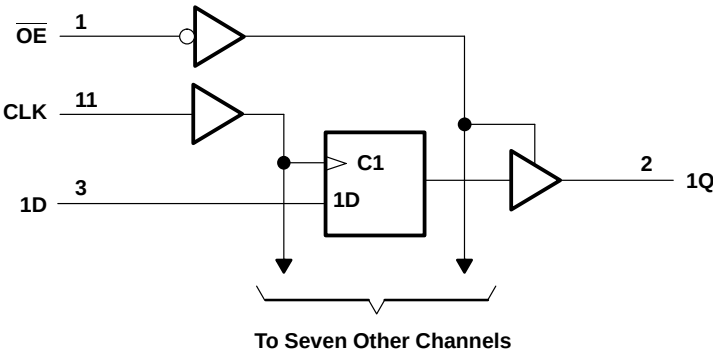
INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVC374A, SN74LVC374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVC374A		SN74LVC374A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	Operating		2	3.6	1.65	3.6	V
	Data retention only		1.5		1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V				$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V				1.7		
	$V_{CC} = 2.7$ V to 3.6 V		2		2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V				$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V				0.7		
	$V_{CC} = 2.7$ V to 3.6 V			0.8	0.8		
V_I Input voltage			0	5.5	0	5.5	V
V_O Output voltage	High or low state		0	V_{CC}	0	V_{CC}	V
	3 state		0	5.5	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V				–4		mA
	$V_{CC} = 2.3$ V				–8		
	$V_{CC} = 2.7$ V			–12	–12		
	$V_{CC} = 3$ V			–24	–24		
I_{OL} Low-level output current	$V_{CC} = 1.65$ V				4		mA
	$V_{CC} = 2.3$ V				8		
	$V_{CC} = 2.7$ V			12	12		
	$V_{CC} = 3$ V			24	24		
$\Delta t/\Delta v$ Input transition rise or fall rate			0	10	0	10	ns/V
T_A Operating free-air temperature			–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	SN54LVC374A			SN74LVC374A			UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V _{OH}	I _{OH} = −100 μA		1.65 V to 3.6 V				V _{CC} −0.2			V
			2.7 V to 3.6 V	V _{CC} −0.2						
	I _{OH} = −4 mA		1.65 V				1.2			
	I _{OH} = −8 mA		2.3 V				1.7			
	I _{OH} = −12 mA		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	I _{OH} = −24 mA		3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA		1.65 V to 3.6 V				0.2			V
			2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA		1.65 V				0.45			
	I _{OL} = 8 mA		2.3 V				0.7			
	I _{OL} = 12 mA		2.7 V	0.4			0.4			
	I _{OL} = 24 mA		3 V	0.55			0.55			
I _I	V _I = 0 to 5.5 V		3.6 V	±5			±5			μA
I _{off}	V _I or V _O = 5.5 V		0				±10			μA
I _{OZ}	V _O = 0 to 5.5 V		3.6 V	±15			±10			μA
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	10			10			μA
	3.6 V ≤ V _I ≤ 5.5 V [‡]			10			10			
ΔI _{CC}	One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND		3.3 V	4	12	4			pF	
C _o	V _O = V _{CC} or GND		3.3 V	5.5	12	5.5			pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

		SN54LVC374A				UNIT
		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	80		100		MHz
t _w	Pulse duration, CLK high or low	3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	2		2		ns
t _h	Hold time, data after CLK↑	1.5		1.5		ns



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		SN74LVC374A								UNIT
		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	†		†		80		100		MHz
t _w	Pulse duration, CLK high or low	†		†		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	†		†		2		2		ns
t _h	Hold time, data after CLK↑	†		†		1.5		1.5		ns

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC374A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
f _{max}			80		100		MHz
t _{pd}	CLK	Q	9.5		1	8.5	ns
t _{en}	OE	Q	9.5		1	8.5	ns
t _{dis}	OE	Q	8		1	7	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC374A								UNIT
			$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		†		80		100		MHz
t _{pd}	CLK	Q	†	†	†	†	8.1		1.5	7	ns
t _{en}	$\overline{\text{OE}}$	Q	†	†	†	†	8.5		1.5	7.5	ns
t _{dis}	$\overline{\text{OE}}$	Q	†	†	†	†	7.1		1.5	6.5	ns
t _{sk(0)} [‡]										1	ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	$f = 10\text{ MHz}$	†	†	54.5	pF
		Outputs disabled		†	†	13.5	

† This information was not available at the time of publication.

SN54LVC374A, SN74LVC374A

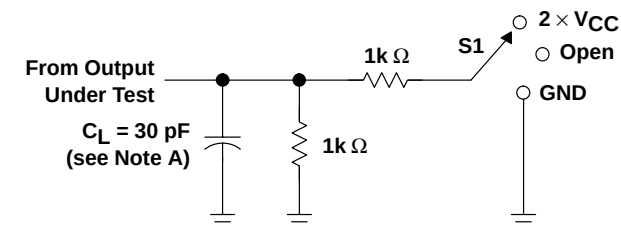
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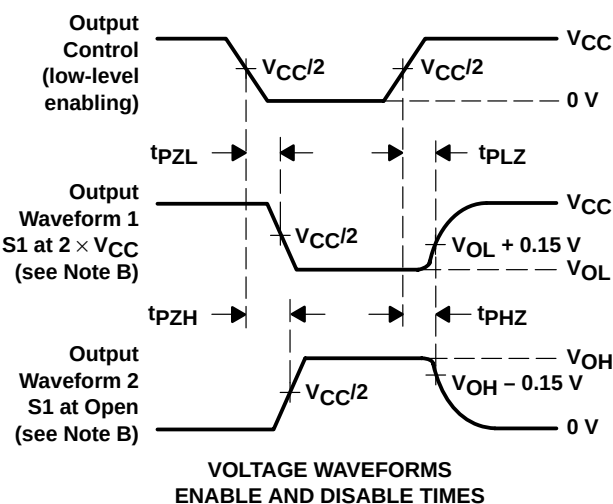
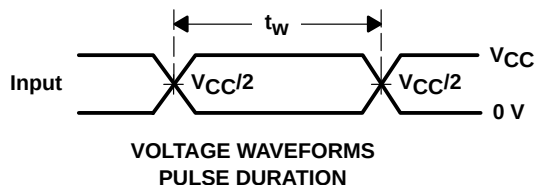
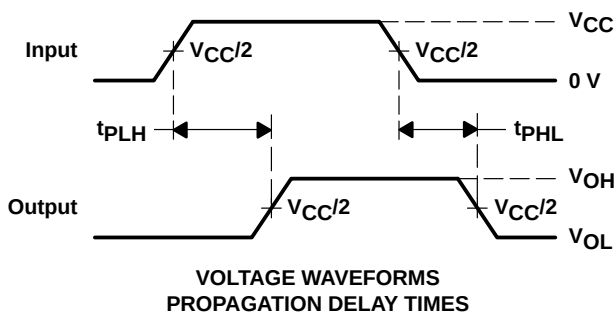
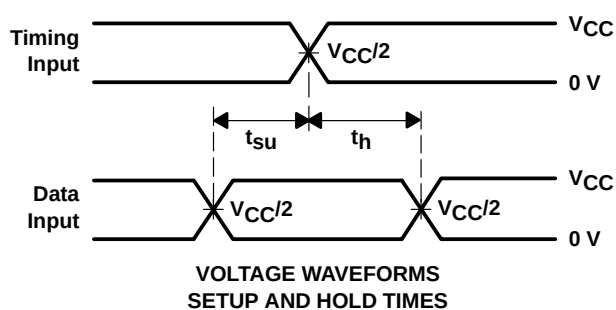
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PHZ}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

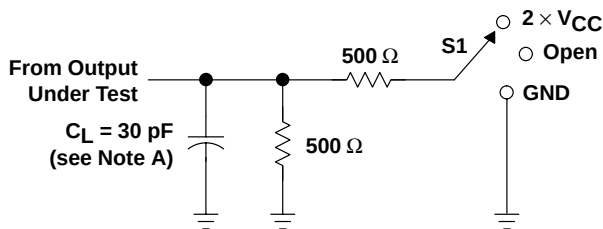
Figure 1. Load Circuit and Voltage Waveforms

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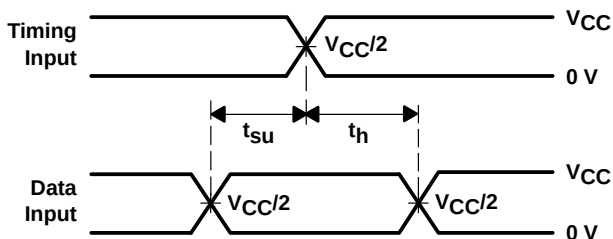
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

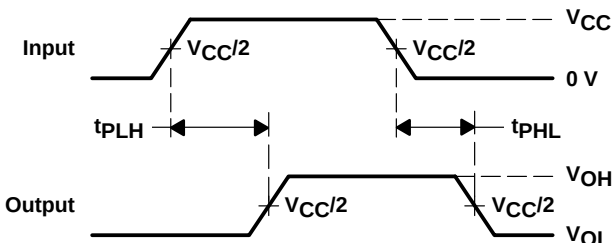


LOAD CIRCUIT

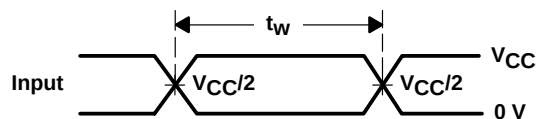
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



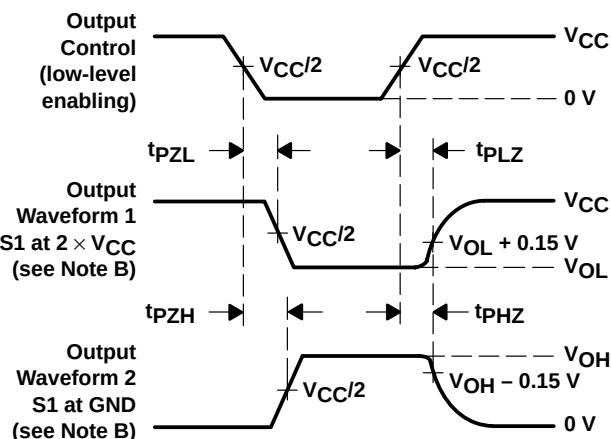
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN54LVC374A, SN74LVC374A

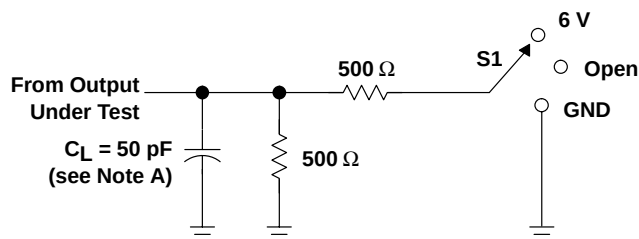
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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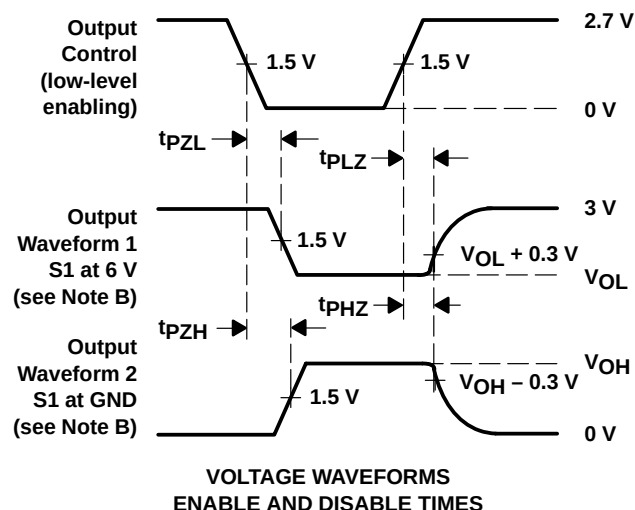
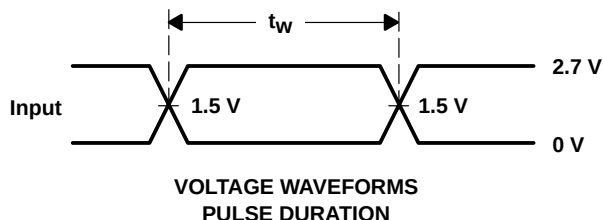
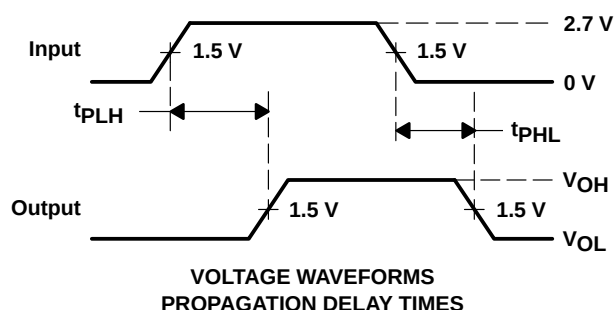
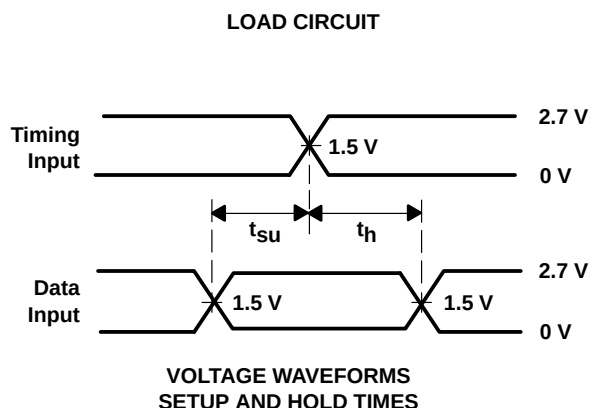
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC540A, SN74LVC540A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and DIPs (J)

description

The SN54LVC540A octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC540A octal buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

These devices are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package that facilitate printed circuit board layout.

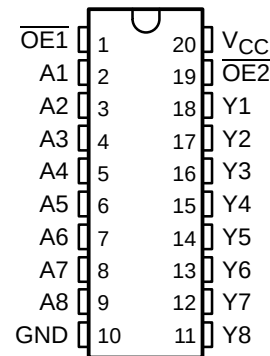
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

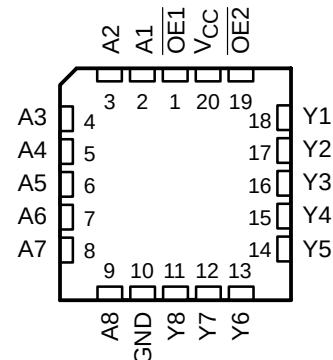
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVC540A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC540A is characterized for operation from -40°C to 85°C .

SN54LVC540A . . . J OR W PACKAGE
SN74LVC540A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVC540A . . . FK PACKAGE
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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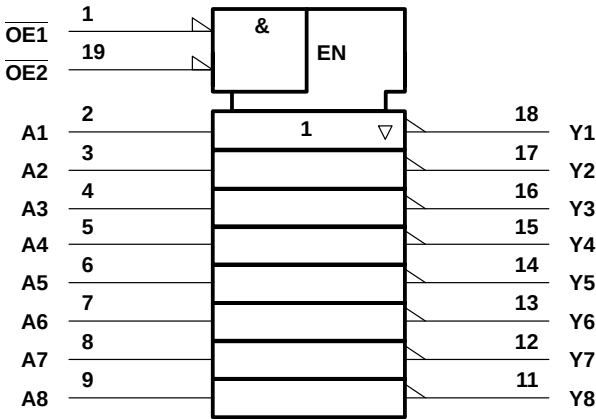
SN54LVC540A, SN74LVC540A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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FUNCTION TABLE

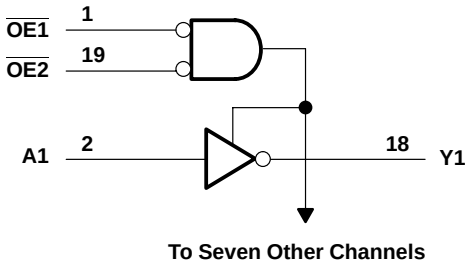
INPUTS			OUTPUT Y
OE1	OE2	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVC540A, SN74LVC540A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVC540A		SN74LVC540A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	Operating		2	3.6	1.65	3.6	V
	Data retention only		1.5		1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V				$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V				1.7		
	$V_{CC} = 2.7$ V to 3.6 V		2		2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V				$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V				0.7		
	$V_{CC} = 2.7$ V to 3.6 V			0.8	0.8		
V_I Input voltage			0	5.5	0	5.5	V
V_O Output voltage	High or low state		0	V_{CC}	0	V_{CC}	V
	3 state		0	5.5	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V				–4		mA
	$V_{CC} = 2.3$ V				–8		
	$V_{CC} = 2.7$ V			–12	–12		
	$V_{CC} = 3$ V			–24	–24		
I_{OL} Low-level output current	$V_{CC} = 1.65$ V				4		mA
	$V_{CC} = 2.3$ V				8		
	$V_{CC} = 2.7$ V			12	12		
	$V_{CC} = 3$ V			24	24		
T_A Operating free-air temperature			–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVC540A, SN74LVC540A

OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	SN54LVC540A			SN74LVC540A			UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V _{OH}	I _{OH} = −100 μA		1.65 V to 3.6 V				V _{CC} −0.2			V
			2.7 V to 3.6 V	V _{CC} −0.2						
	I _{OH} = −4 mA		1.65 V				1.2			
	I _{OH} = −8 mA		2.3 V				1.7			
	I _{OH} = −12 mA		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	I _{OH} = −24 mA		3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA		1.65 V to 3.6 V				0.2			V
			2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA		1.65 V				0.45			
	I _{OL} = 8 mA		2.3 V				0.7			
	I _{OL} = 12 mA		2.7 V	0.4			0.4			
	I _{OL} = 24 mA		3 V	0.55			0.55			
I _I	V _I = 0 to 5.5 V		3.6 V	±5			±5			μA
I _{off}	V _I or V _O = 5.5 V		0				±10			μA
I _{OZ}	V _O = 0 to 5.5 V		3.6 V	±15			±10			μA
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	10			10			μA
	3.6 V ≤ V _I ≤ 5.5 V [‡]			10			10			
ΔI _{CC}	One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND		3.3 V	4			4			pF
C _O	V _O = V _{CC} or GND		3.3 V	5.5			5.5			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC540A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A	Y	7.1		1	5.3	ns
t _{en}	$\overline{OE}$	Y	8		1	6.6	ns
t _{dis}	$\overline{OE}$	Y	8.2		1	7.4	ns



SN54LVC540A, SN74LVC540A
OCTAL BUFFERS/DRIVERS
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC540A								UNIT
			$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	†	†	†	†	7.1	1.4	5.3	ns	
t _{en}	$\overline{OE}$	Y	†	†	†	†	8	1.1	6.6	ns	
t _{dis}	$\overline{OE}$	Y	†	†	†	†	8.2	1.8	7.4	ns	
t _{sk(o)} [‡]								1		ns	

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	$f = 10\text{ MHz}$	†	†	31	pF
		Outputs disabled		†	†	3	

† This information was not available at the time of publication.

SN54LVC540A, SN74LVC540A

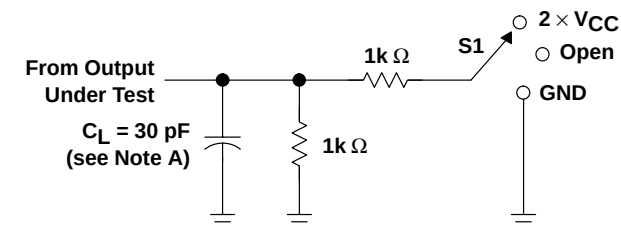
OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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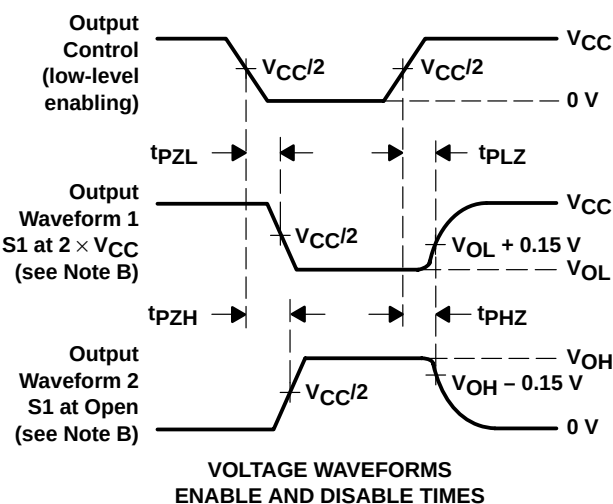
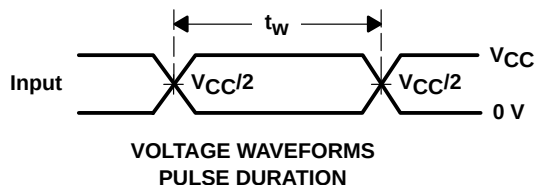
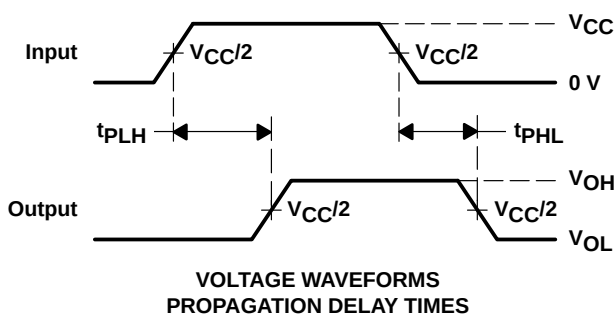
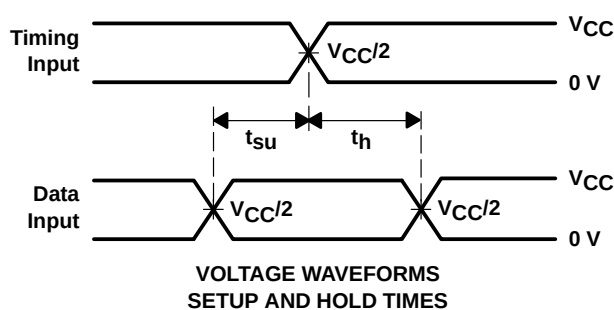
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	Open

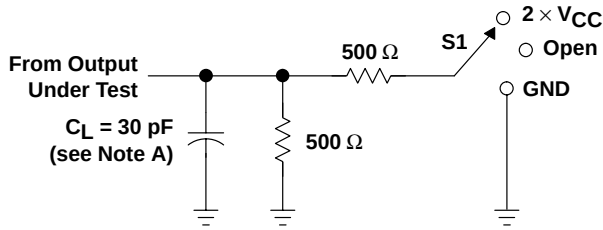


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

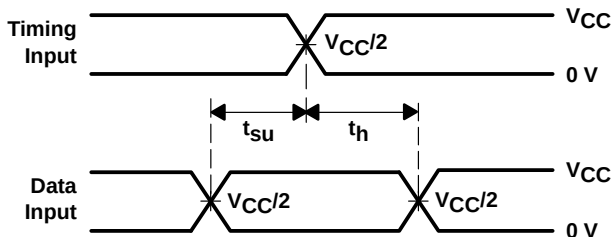
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

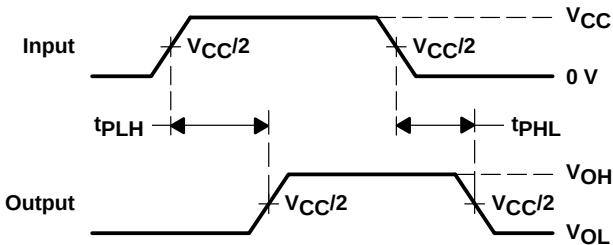


LOAD CIRCUIT

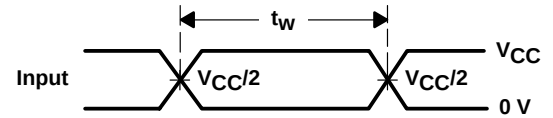
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



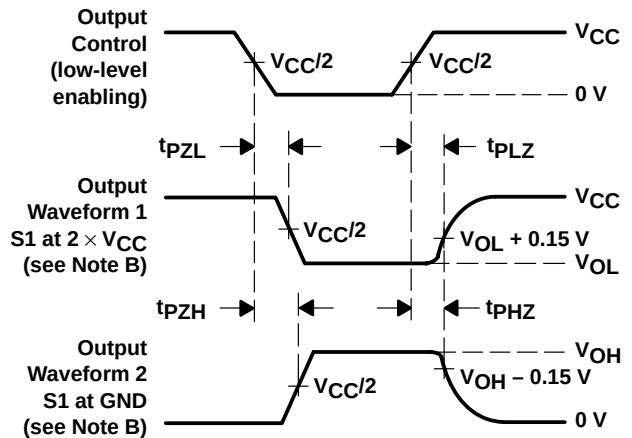
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

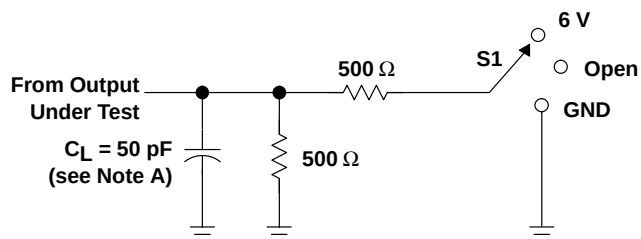
- NOTES:
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 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN54LVC540A, SN74LVC540A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

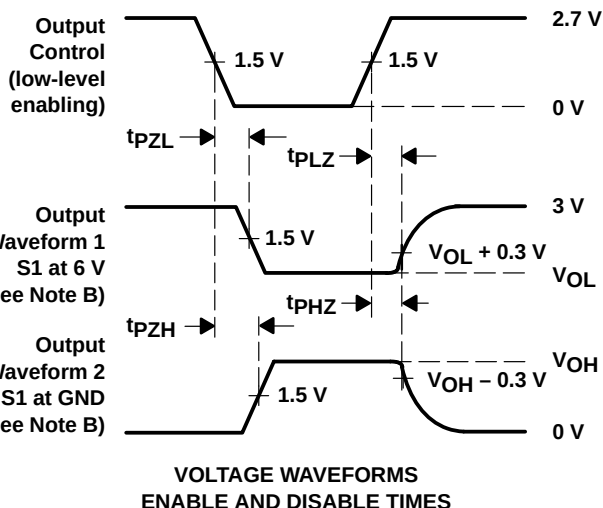
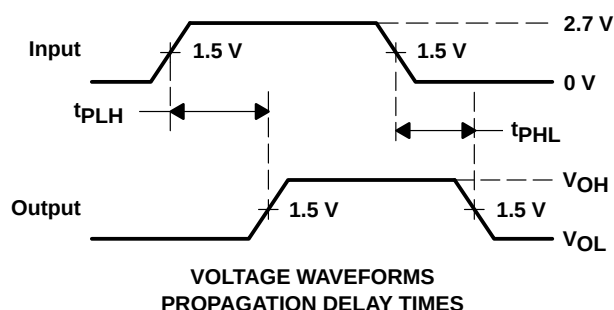
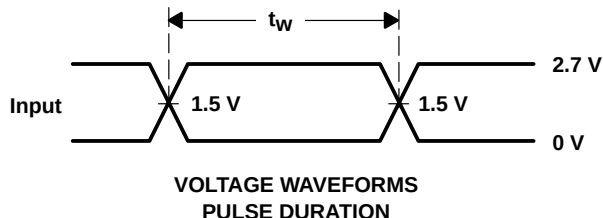
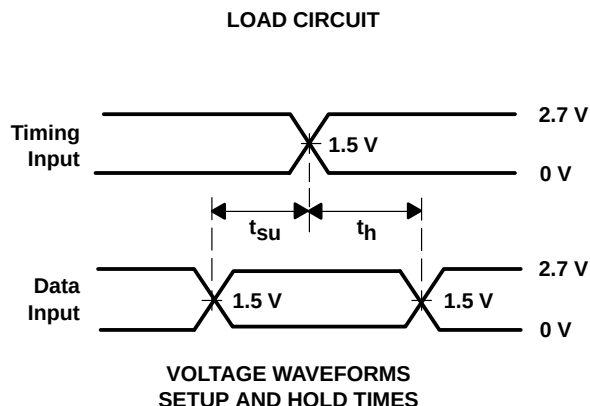
SCAS297H – JANUARY 1993 – REVISED JUNE 1998

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
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 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC541A, SN74LVC541A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and DIPs (J)**

description

The SN54LVC541A octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC541A octal buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The 'LVC541A devices are ideal for driving bus lines or buffering memory address registers.

These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

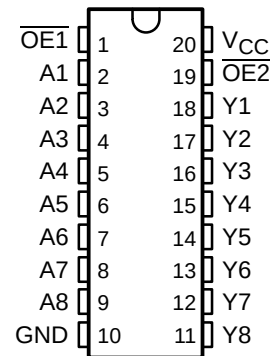
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

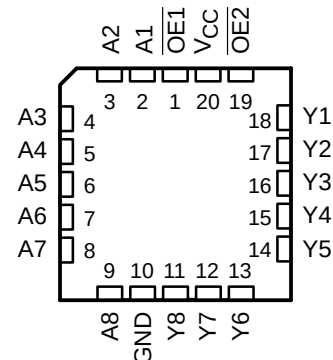
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC541A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC541A is characterized for operation from -40°C to 85°C .

SN54LVC541A . . . J OR W PACKAGE
SN74LVC541A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVC541A . . . FK PACKAGE
(TOP VIEW)



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INPUTS			OUTPUT Y
OE1	OE2	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

The diagram shows a 2-to-1 multiplexer at the top, followed by a 1-to-8 decoder. The multiplexer's output is connected to the decoder's input. The decoder's outputs are labeled 18 through 8, which correspond to outputs Y1 through Y8.

Logic diagram for the Y1 output of the 74VHC163. The diagram shows an AND gate with inputs OE1 (pin 1) and OE2 (pin 19). The output of the AND gate is connected to a bus line labeled 18, which is also the output Y1. This bus line is also connected to a buffer (triangle symbol) with input A1 (pin 2). The output of the buffer is also connected to the bus line 18. A downward arrow from the bus line 18 indicates it is connected to seven other channels.

SN54LVC541A, SN74LVC541A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVC541A		SN74LVC541A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3$ V to 2.7 V			1.7		
		$V_{CC} = 2.7$ V to 3.6 V	2		2		
V_{IL}	Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.35 \times V_{CC}$		V
		$V_{CC} = 2.3$ V to 2.7 V			0.7		
		$V_{CC} = 2.7$ V to 3.6 V		0.8	0.8		
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3 state	0	5.5	0	5.5	
I_{OH}	High-level output current	$V_{CC} = 1.65$ V				–4	mA
		$V_{CC} = 2.3$ V				–8	
		$V_{CC} = 2.7$ V		–12		–12	
		$V_{CC} = 3$ V		–24		–24	
I_{OL}	Low-level output current	$V_{CC} = 1.65$ V				4	mA
		$V_{CC} = 2.3$ V				8	
		$V_{CC} = 2.7$ V		12		12	
		$V_{CC} = 3$ V		24		24	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	SN54LVC541A			SN74LVC541A			UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V _{OH}	I _{OH} = −100 μA		1.65 V to 3.6 V				V _{CC} −0.2			V
			2.7 V to 3.6 V	V _{CC} −0.2						
	I _{OH} = −4 mA		1.65 V				1.2			
	I _{OH} = −8 mA		2.3 V				1.7			
	I _{OH} = −12 mA		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	I _{OH} = −24 mA		3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA		1.65 V to 3.6 V				0.2			V
			2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA		1.65 V				0.45			
	I _{OL} = 8 mA		2.3 V				0.7			
	I _{OL} = 12 mA		2.7 V	0.4			0.4			
	I _{OL} = 24 mA		3 V	0.55			0.55			
I _I	V _I = 0 to 5.5 V		3.6 V	±5			±5			μA
I _{off}	V _I or V _O = 5.5 V		0				±10			μA
I _{OZ}	V _O = 0 to 5.5 V		3.6 V	±15			±10			μA
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	10			10			μA
	3.6 V ≤ V _I ≤ 5.5 V [‡]			10			10			
ΔI _{CC}	One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND		3.3 V	4			4			pF
C _o	V _O = V _{CC} or GND		3.3 V	5.5			5.5			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC541A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A	Y	5.6		1	5.1	ns
t _{en}	$\overline{\text{OE}}$	Y	7.5		1	7	ns
t _{dis}	$\overline{\text{OE}}$	Y	7.7		1	7	ns



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC541A								UNIT
			$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	†	†	†	†	5.6		1.5	5.1	ns
t _{en}	$\overline{OE}$	Y	†	†	†	†	7.5		1.5	7	ns
t _{dis}	$\overline{OE}$	Y	†	†	†	†	7.7		1.5	7	ns
t _{sk(o)} [‡]									1		ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	$f = 10\text{ MHz}$	†	†	33	pF
		Outputs disabled		†	†	2	

† This information was not available at the time of publication.

SN54LVC541A, SN74LVC541A

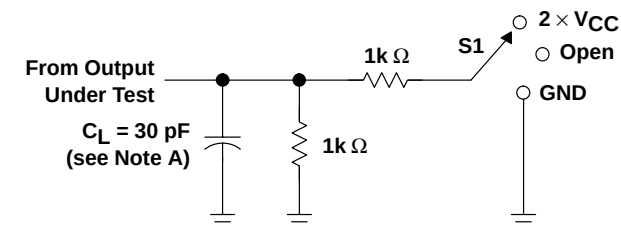
OCTAL BUFFERS/DRIVERS

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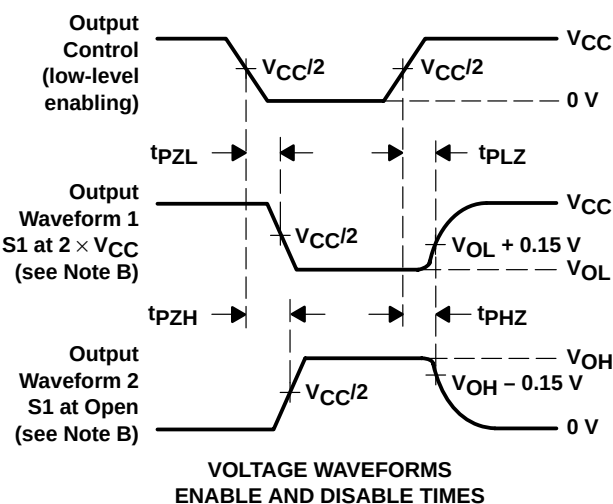
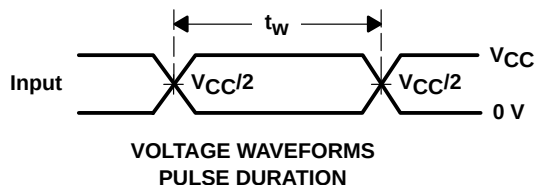
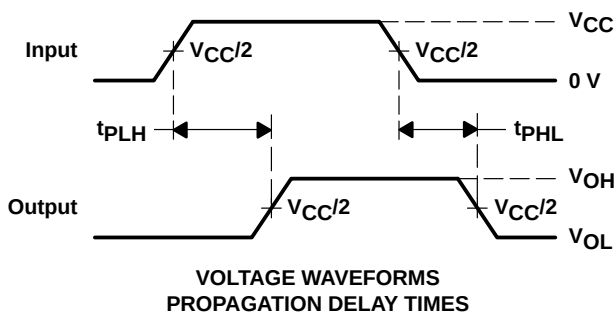
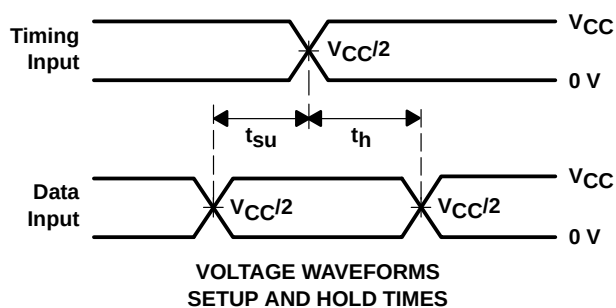
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	Open

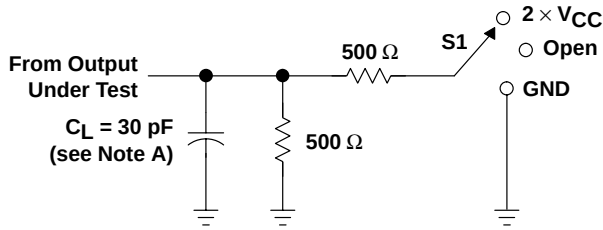


- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

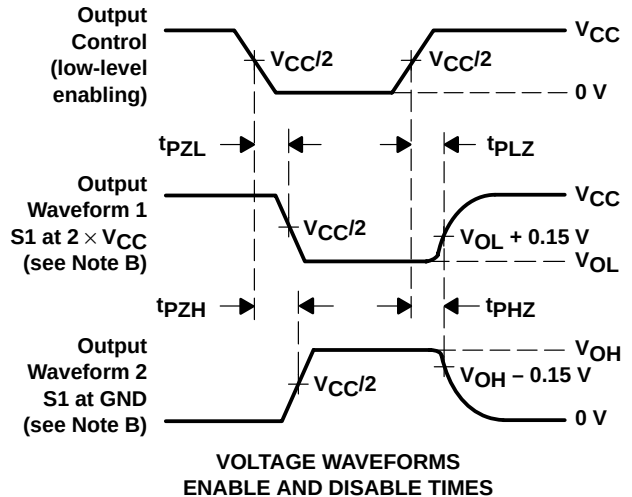
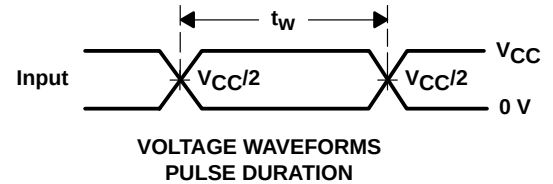
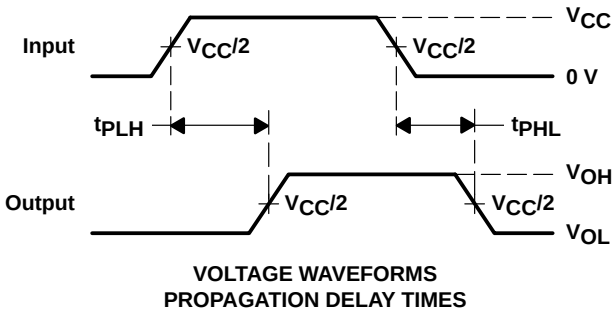
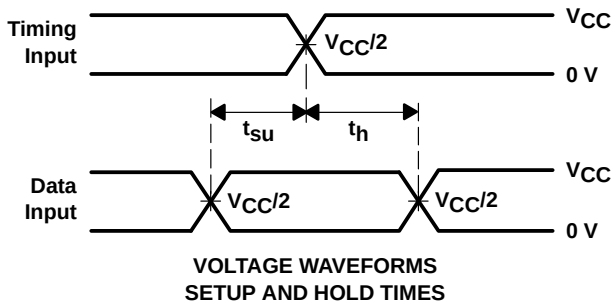
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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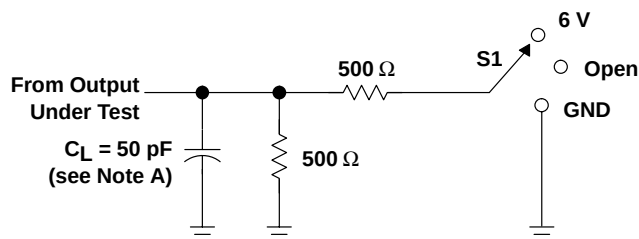
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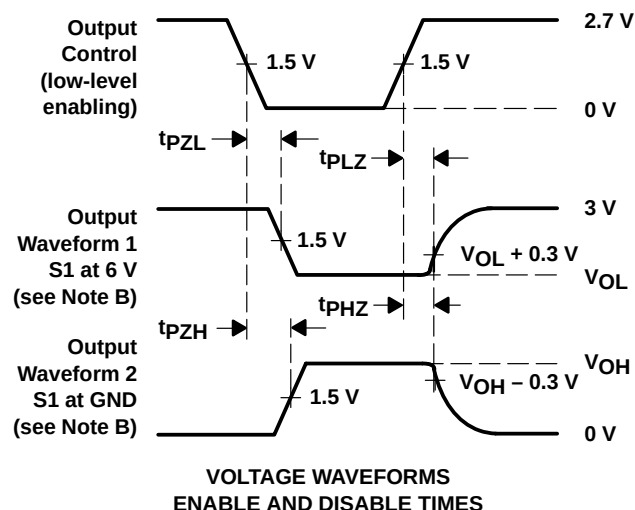
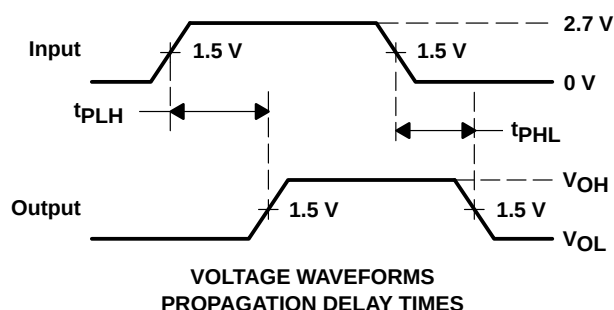
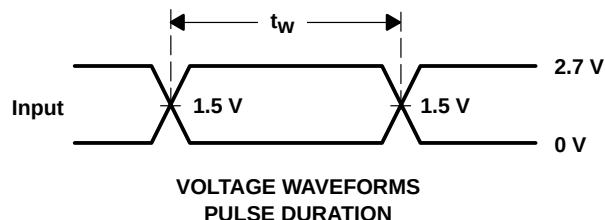
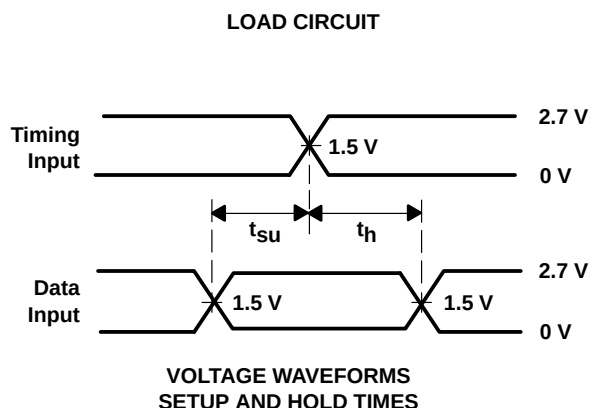
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

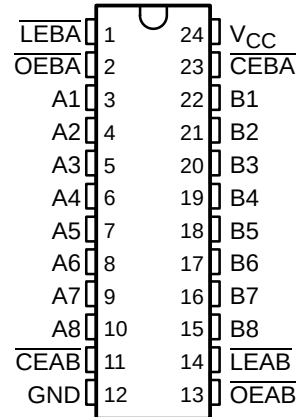
Figure 3. Load Circuit and Voltage Waveforms

SN74LVC543A OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

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- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal registered transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC543A contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ places the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow for B to A is similar to that of A to B, but uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC543A is characterized for operation from -40°C to 85°C .

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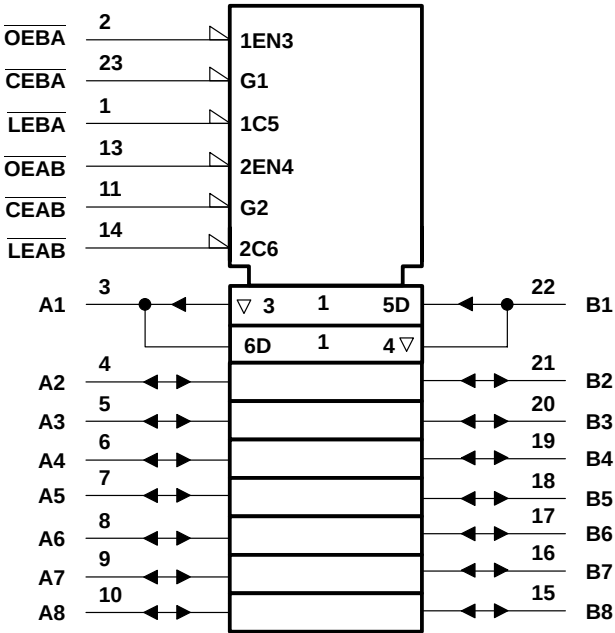
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FUNCTION TABLE†				
INPUTS				OUTPUT B
CEAB	LEAB	OEAB	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B ₀ ‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.
‡ Output level before the indicated steady-state input conditions were established

logic symbols§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7		
	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		0.7	
	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65\text{ V}$		–4	mA
	$V_{CC} = 2.3\text{ V}$		–8	
	$V_{CC} = 2.7\text{ V}$		–12	
	$V_{CC} = 3\text{ V}$		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65\text{ V}$		4	mA
	$V_{CC} = 2.3\text{ V}$		8	
	$V_{CC} = 2.7\text{ V}$		12	
	$V_{CC} = 3\text{ V}$		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}		I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
		I _{OH} = –4 mA	1.65 V	1.2			
		I _{OH} = –8 mA	2.3 V	1.7			
		I _{OH} = –12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = –24 mA	3 V	2.2			
V _{OL}		I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
		I _{OL} = 4 mA	1.65 V	0.45			
		I _{OL} = 8 mA	2.3 V	0.7			
		I _{OL} = 12 mA	2.7 V	0.4			
		I _{OL} = 24 mA	3 V	0.55			
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V	±5			µA
I _{off}		V _I or V _O = 5.5 V	0	±10			µA
I _{OZ} [‡]		V _O = 0 to 5.5 V	3.6 V	±10			µA
I _{CC}		V _I = V _{CC} or GND	3.6 V	10			µA
		3.6 V ≤ V _I ≤ 5.5 V [§]		10			
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	4.5			pF
C _{iO}	A or B ports	V _O = V _{CC} or GND	3.3 V	7.5			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	¶		¶		3.3		3.3		ns
t _{su}	Setup time, data before $\overline{LE}\uparrow$ or $\overline{CE}\uparrow$	¶		¶		1.6		1.6		ns
t _h	Hold time, data after $\overline{LE}\uparrow$ or $\overline{CE}\uparrow$	¶		¶		2.1		2.1		ns

¶ This information was not available at the time of publication.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	†	†	†	†	8		1	7	ns
	$\overline{LE}$		†	†	†	†	9.5		1.2	8.5	
t_{en}	$\overline{OE}$	A or B	†	†	†	†	9.2		1.3	7.7	ns
	$\overline{CE}$		†	†	†	†	9.3		1.3	8	
t_{dis}	$\overline{OE}$	A or B	†	†	†	†	7.5		1	7	ns
	$\overline{CE}$		†	†	†	†	7.5		1	7	

† This information was not available at the time of publication.

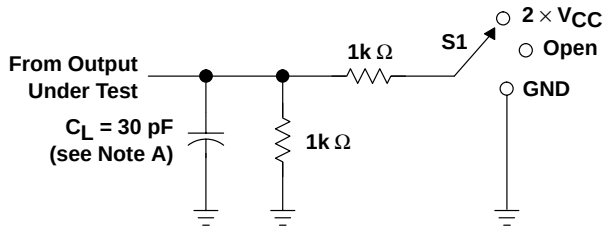
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$f = 10\text{ MHz}$	†	†	49	pF
		Outputs disabled		†	†	6	

† This information was not available at the time of publication.

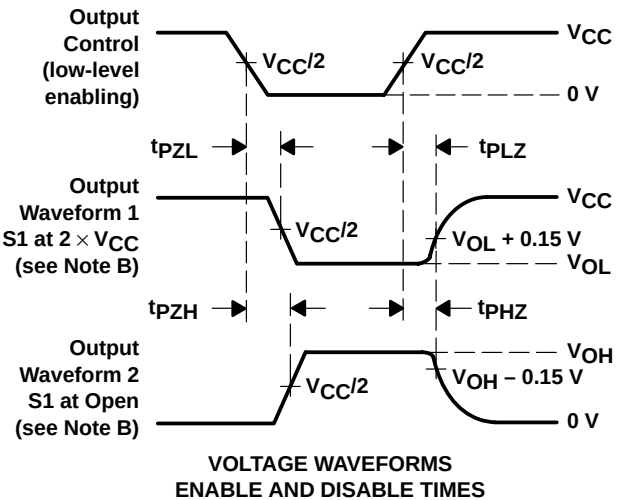
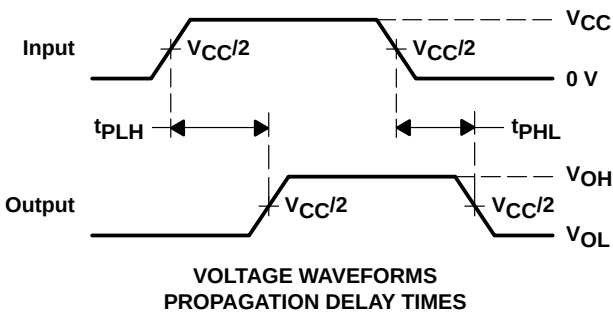
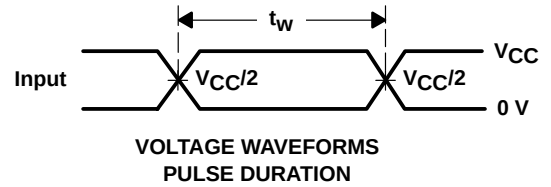
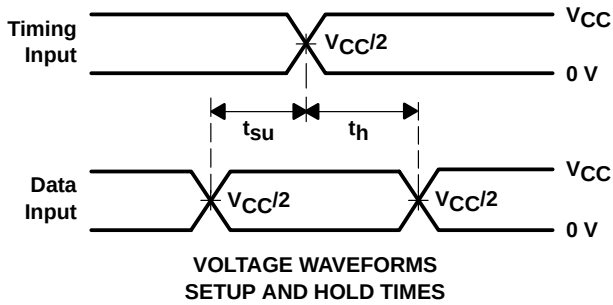
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC543A

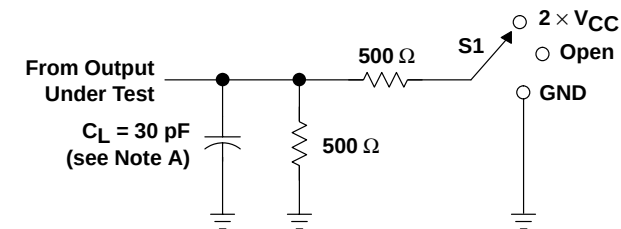
OCTAL REGISTERED TRANSCEIVER

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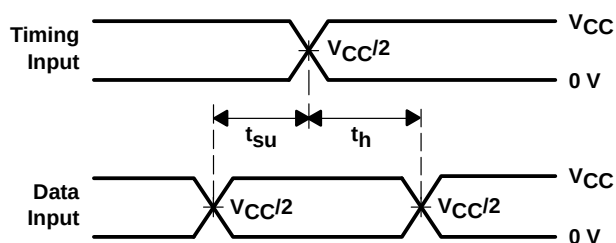
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

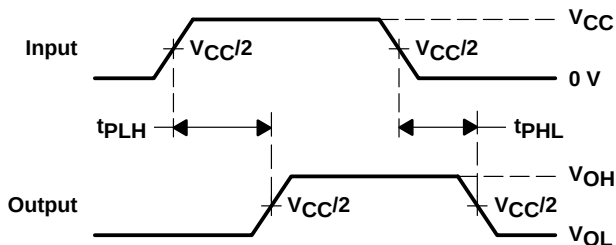


LOAD CIRCUIT

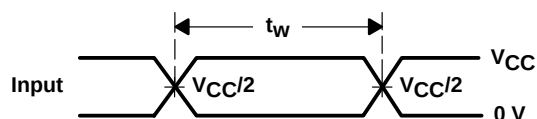
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



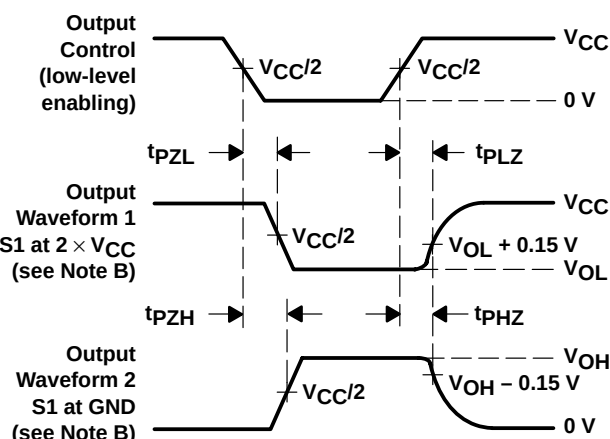
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

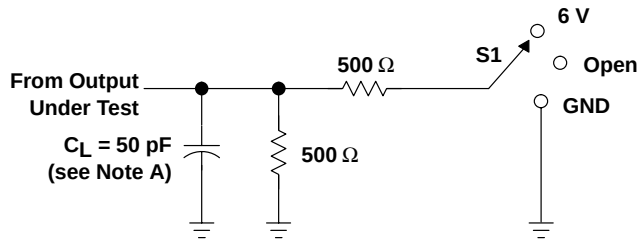


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

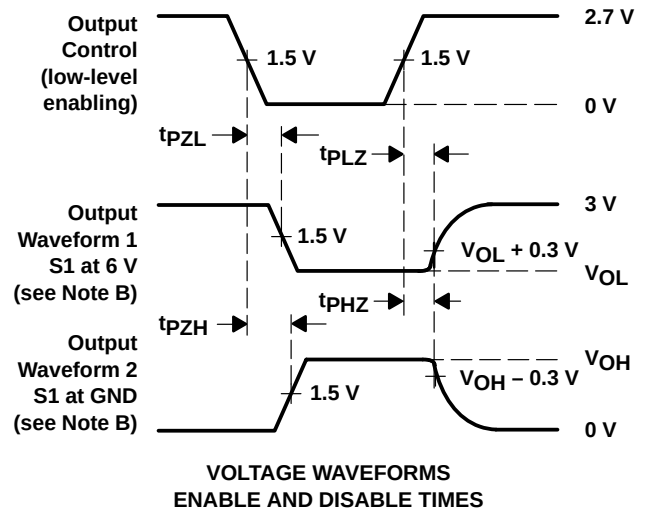
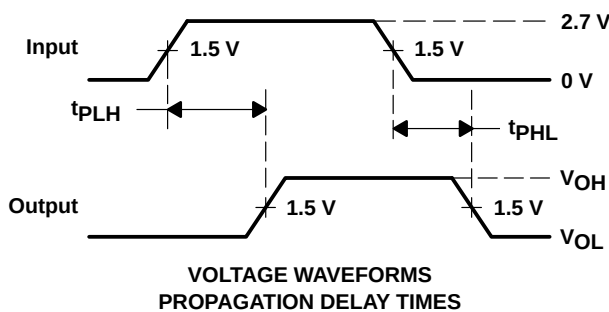
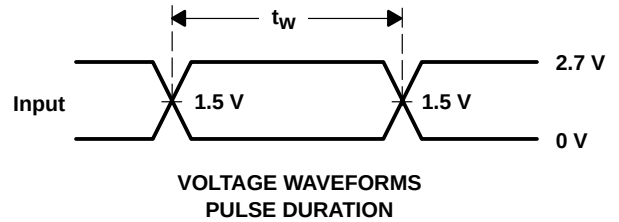
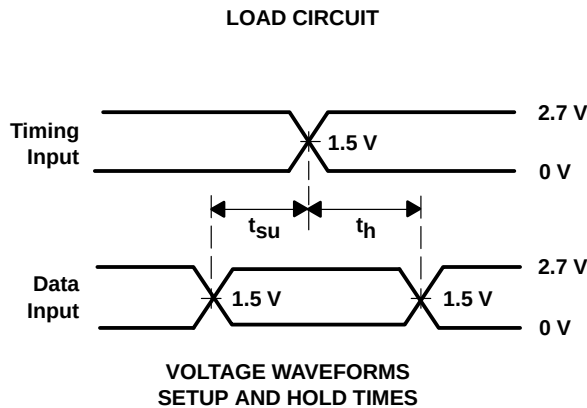
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

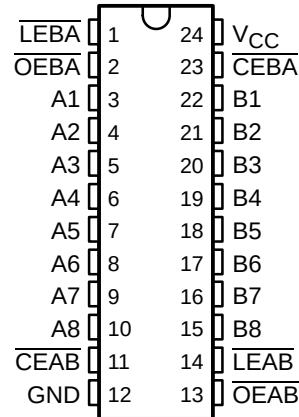
Figure 3. Load Circuit and Voltage Waveforms

SN74LVC544A OCTAL REGISTERED TRANSCIEVER WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal registered transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC544A contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ places the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the inverted data present at the output of the A latches. Data flow from B to A is similar to A to B, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC544A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS				OUTPUT B
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	
H	X	X	X	Z
L	X	H	X	Z
L	H	L	X	$B_0^\ddagger$
L	L	L	L	H
L	L	L	H	L

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

‡ Output level before the indicated steady-state input conditions were established

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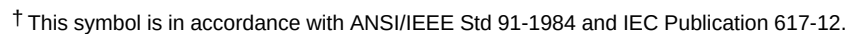
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logic symbol[†]



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I : (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	0.7		
	$V_{CC} = 2.7$ V to 3.6 V	0.8		
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT	
V _{OH}	I _{OH} = –100 μA		1.65 V to 3.6 V	V _{CC} –0.2			V	
	I _{OH} = –4 mA		1.65 V	1.2				
	I _{OH} = –8 mA		2.3 V	1.7				
	I _{OH} = –12 mA		2.7 V	2.2				
			3 V	2.4				
	I _{OH} = –24 mA		3 V	2.2				
V _{OL}	I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	V	
	I _{OL} = 4 mA		1.65 V			0.45		
	I _{OL} = 8 mA		2.3 V			0.7		
	I _{OL} = 12 mA		2.7 V			0.4		
	I _{OL} = 24 mA		3 V			0.55		
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V			±5	μA	
I _{off}		V _I or V _O = 5.5 V	0			±10	μA	
I _{OZ} [‡]		V _O = 0 to 5.5 V		3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND		3.6 V			10	μA	
	3.6 V ≤ V _I ≤ 5.5 V [§]					10		
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V			500	μA
C _i	Control inputs	V _I = V _{CC} or GND		3.3 V				pF
C _{i0}	A or B ports	V _O = V _{CC} or GND		3.3 V				pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration,	LEAB or LEBA low									ns
t _{su}	Setup time	Data before LEAB or LEBA↑	High								ns
			Low								
		Data before CEAB or CEBA↑	High								ns
			Low								
t _h	Hold time	Data after LEAB or LEBA↑									ns
		Data after CEAB or CEBA↑									

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A									ns
	$\overline{LEBA}$ or $\overline{LEAB}$	A or B									
t_{en}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B									ns
t_{dis}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B									ns
t_{en}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B									ns
t_{dis}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B									ns

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$f = 10\text{ MHz}$				pF
		Outputs disabled					

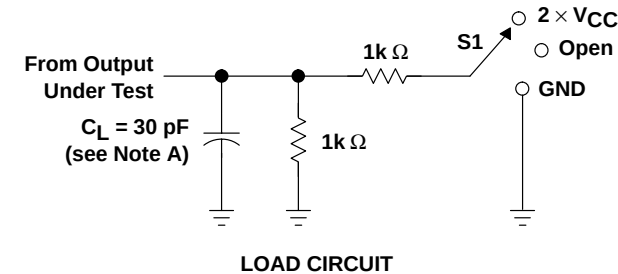
PRODUCT PREVIEW



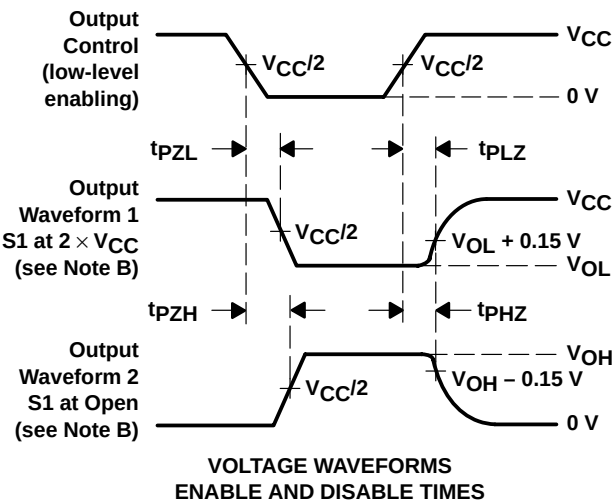
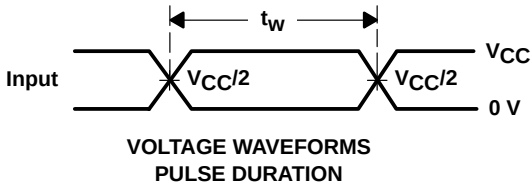
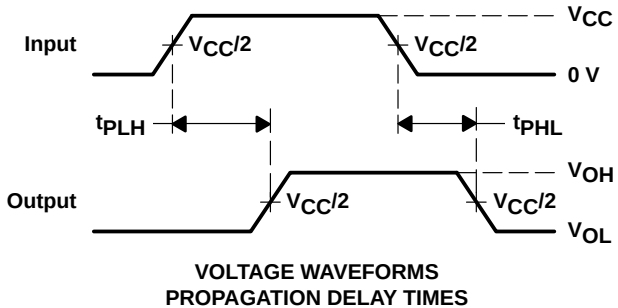
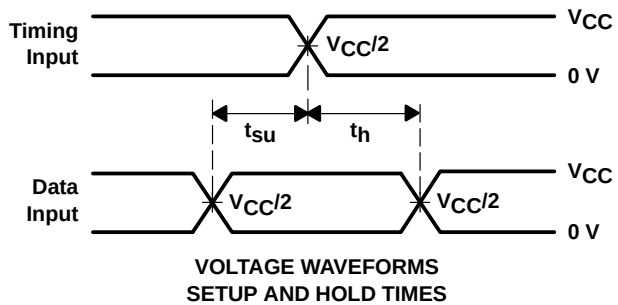
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PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PHZ}	Open

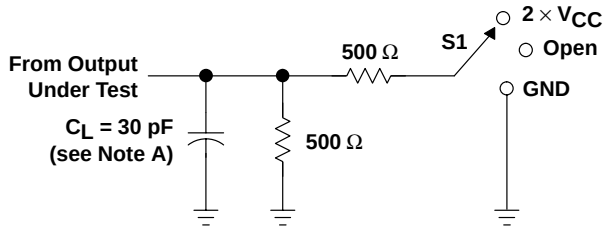


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

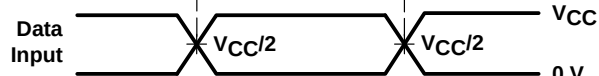
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

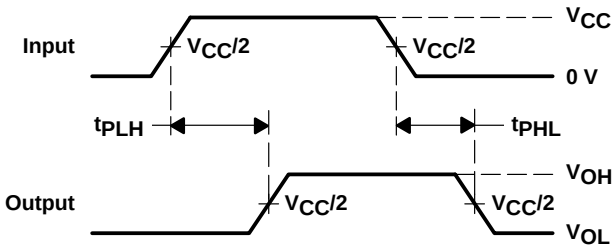


LOAD CIRCUIT

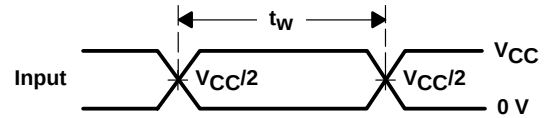
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



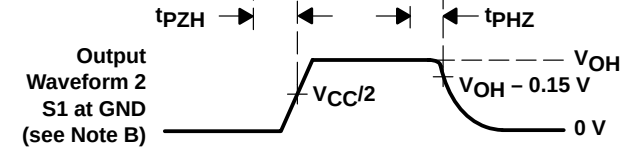
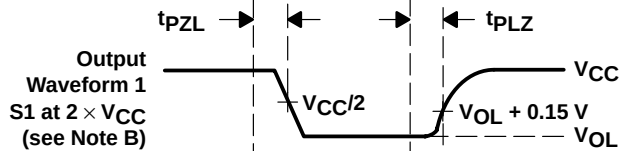
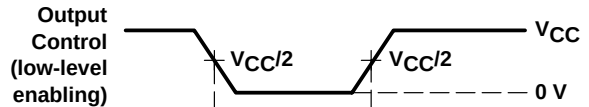
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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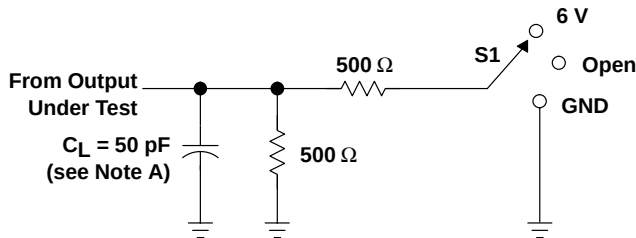
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WITH 3-STATE OUTPUTS

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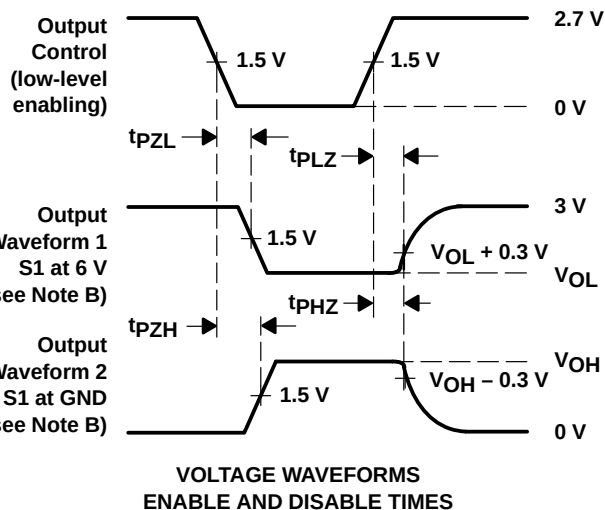
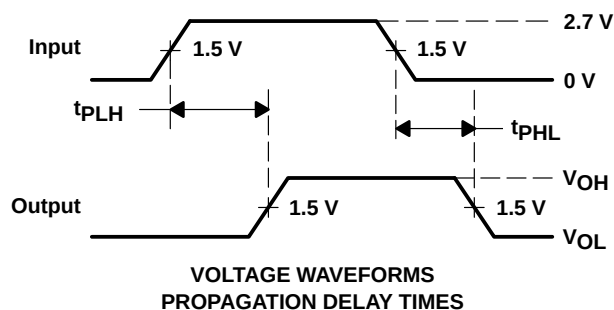
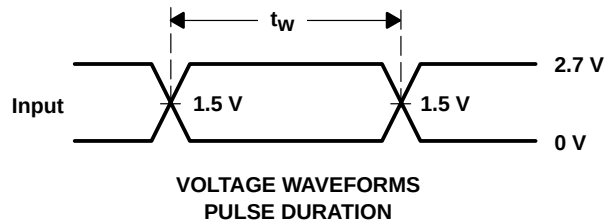
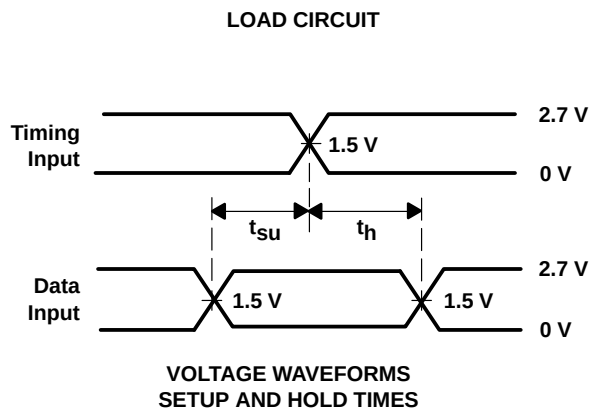
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC573A, SN74LVC573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCAS300I – JANUARY 1993 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Power Off Disables Outputs, Permitting Live Insertion
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and DIPs (J)

description

The SN54LVC573A octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC573A octal transparent D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels at the D inputs.

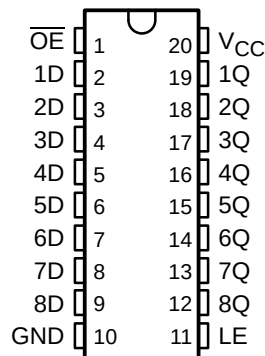
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

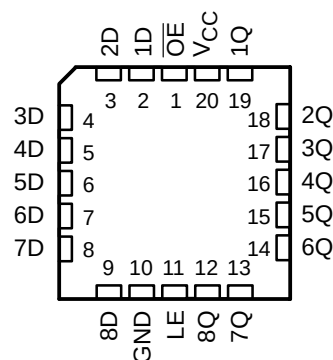
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

SN54LVC573A . . . J OR W PACKAGE
SN74LVC573A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVC573A . . . FK PACKAGE
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVC573A, SN74LVC573A

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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description (continued)

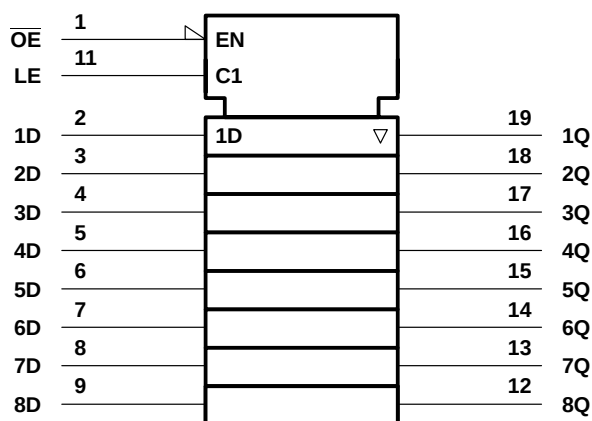
The SN54LVC573A is characterized for operation over the full military temperature range of -55°C to 125°C .

The SN74LVC573A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each latch)

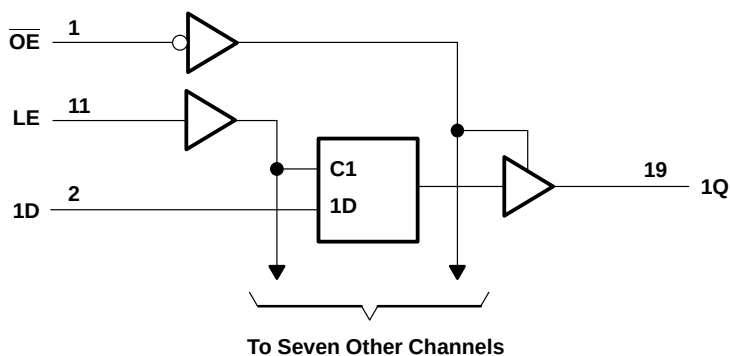
INPUTS			OUTPUT Q
OE	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVC573A, SN74LVC573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVC573A		SN74LVC573A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	Operating		2	3.6	1.65	3.6	V
	Data retention only		1.5		1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V				$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V				1.7		
	$V_{CC} = 2.7$ V to 3.6 V		2		2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V				$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V				0.7		
	$V_{CC} = 2.7$ V to 3.6 V			0.8	0.8		
V_I Input voltage			0	5.5	0	5.5	V
V_O Output voltage	High or low state		0	V_{CC}	0	V_{CC}	V
	3 state		0	5.5	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V				–4		mA
	$V_{CC} = 2.3$ V				–8		
	$V_{CC} = 2.7$ V			–12	–12		
	$V_{CC} = 3$ V			–24	–24		
I_{OL} Low-level output current	$V_{CC} = 1.65$ V				4		mA
	$V_{CC} = 2.3$ V				8		
	$V_{CC} = 2.7$ V			12	12		
	$V_{CC} = 3$ V			24	24		
$\Delta t/\Delta v$ Input transition rise or fall rate			0	6	0	6	ns/V
T_A Operating free-air temperature			–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVC573A, SN74LVC573A

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	SN54LVC573A			SN74LVC573A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OH}	I _{OH} = –100 μA		1.65 V to 3.6 V				V _{CC} –0.2			V
			2.7 V to 3.6 V	V _{CC} –0.2						
	I _{OH} = –4 mA		1.65 V				1.2			
	I _{OH} = –8 mA		2.3 V				1.7			
	I _{OH} = –12 mA		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	I _{OH} = –24 mA		3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA		1.65 V to 3.6 V				0.2			V
			2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA		1.65 V				0.45			
	I _{OL} = 8 mA		2.3 V				0.7			
	I _{OL} = 12 mA		2.7 V	0.4			0.4			
	I _{OL} = 24 mA		3 V	0.55			0.55			
I _I	V _I = 0 to 5.5 V		3.6 V	±5			±5			μA
I _{off}	V _I or V _O = 5.5 V		0				±10			μA
I _{OZ}	V _O = 0 to 5.5 V		3.6 V	±15			±10			μA
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	10			10			μA
	3.6 V ≤ V _I ≤ 5.5 V‡			10			10			
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND		3.3 V	4			4			pF
C _o	V _O = V _{CC} or GND		3.3 V	5.5			5.5			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

		SN54LVC573A				UNIT
		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high	3.3		3.3		ns
t _{SU}	Setup time, data before LE↓	2		2		ns
t _H	Hold time, data after LE↓	2.5		2.5		ns



SN54LVC573A, SN74LVC573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		SN74LVC573A								UNIT
		$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	†		†		3.3		3.3		ns
t _{su}	Setup time, data before LE↓	†		†		2		2		ns
t _h	Hold time, data after LE↓	†		†		1.5		1.5		ns

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC573A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	D	Q	7.7		1	6.9	ns
	LE		8.4		1	7.7	
t _{en}	$\overline{OE}$	Q	8.5		1	7.5	ns
t _{dis}	$\overline{OE}$	Q	7		0.5	6.7	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC573A								UNIT
			$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	†	†	†	†	7.7	1.5	6.9	ns	
	LE		†	†	†	†	8.4	2	7.7		
t_{en}	$\overline{OE}$	Q	†	†	†	†	8.5	1.5	7.5	ns	
t_{dis}	$\overline{OE}$	Q	†	†	†	†	7	1.6	6.5	ns	
$t_{sk(o)}^{\dagger}$								1		ns	

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	$f = 10\text{ MHz}$	†	†	37	pF
		Outputs disabled		†	†	4	

† This information was not available at the time of publication.

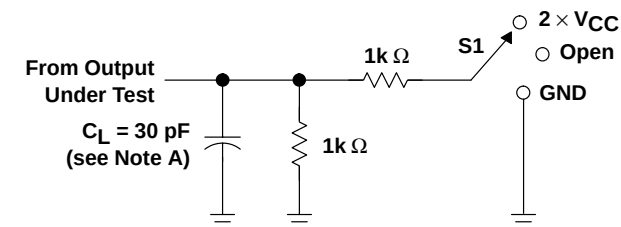


SN54LVC573A, SN74LVC573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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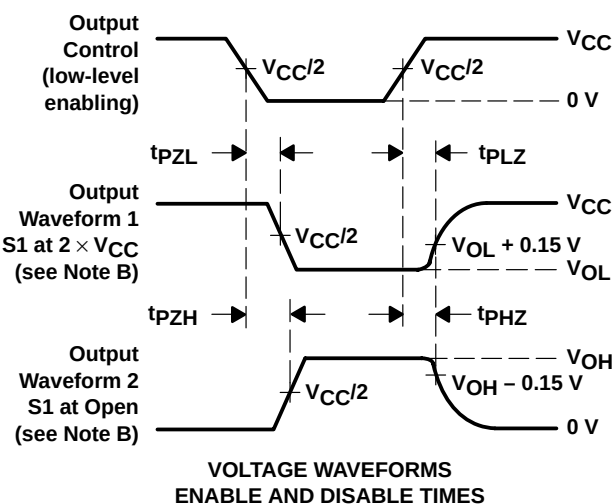
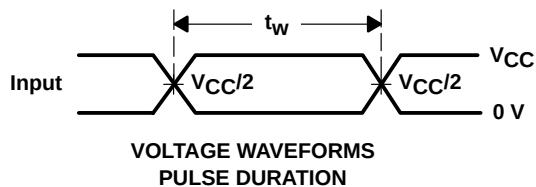
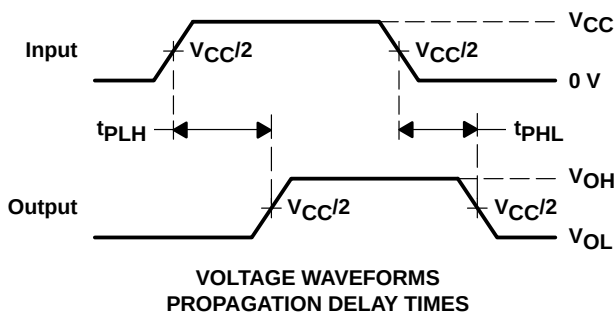
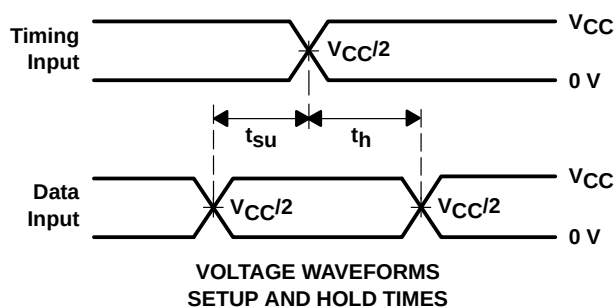
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

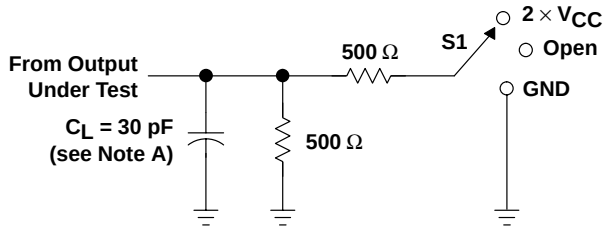
Figure 1. Load Circuit and Voltage Waveforms

SN54LVC573A, SN74LVC573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCAS300I – JANUARY 1993 – REVISED JUNE 1998

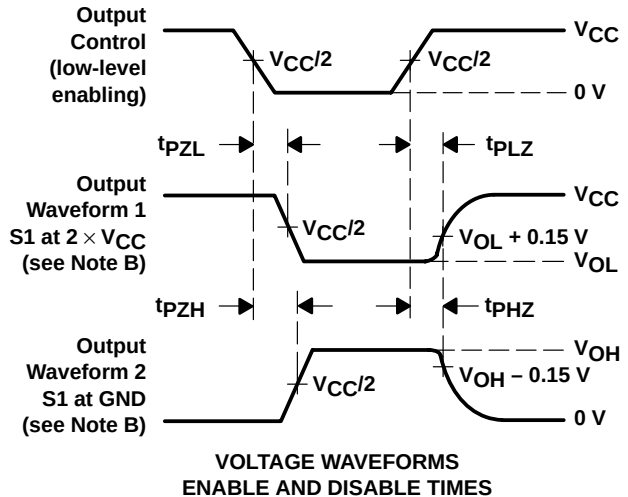
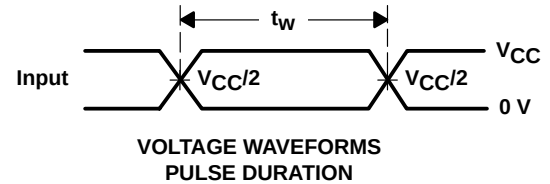
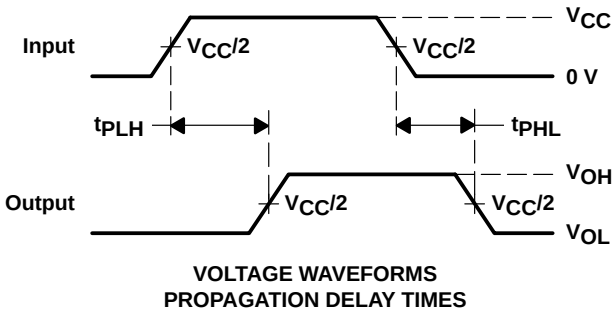
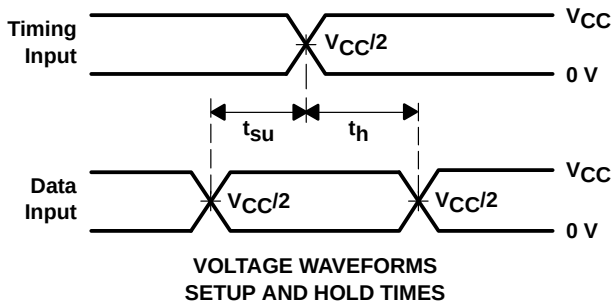
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHZ}	GND



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN54LVC573A, SN74LVC573A

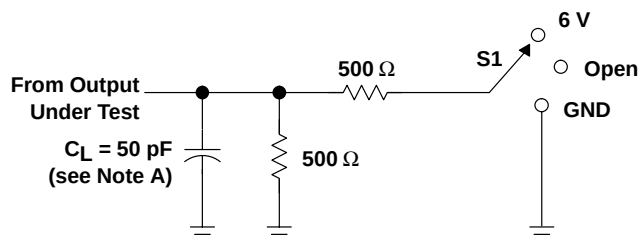
OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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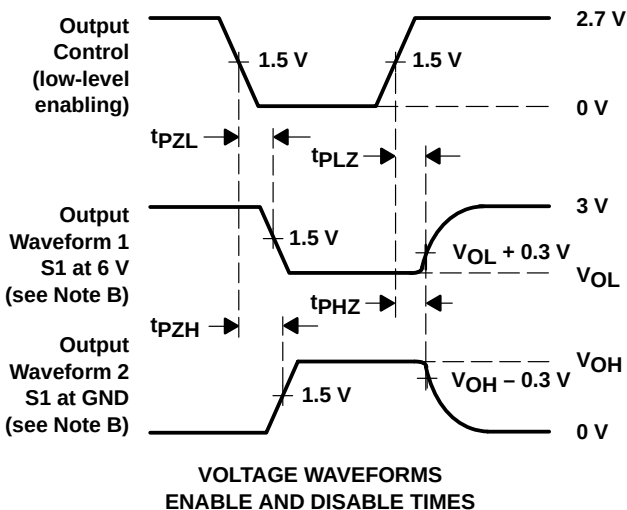
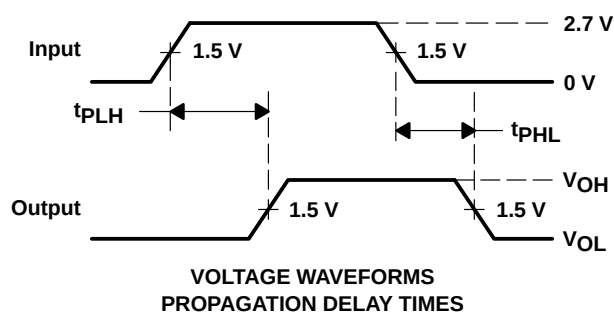
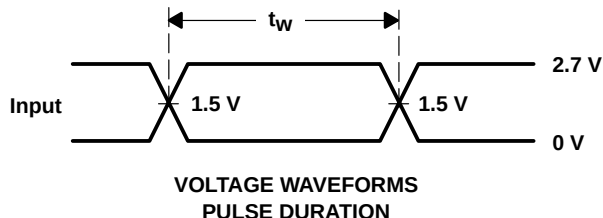
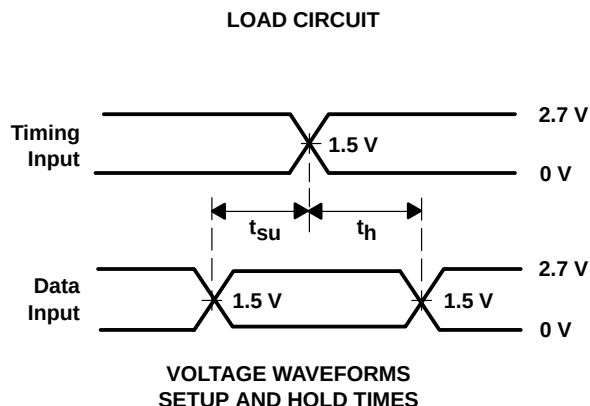
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC574A, SN74LVC574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS301I – JANUARY 1993 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and DIPs (J)**

description

The SN54LVC574A octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC574A octal edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels at the data (D) inputs.

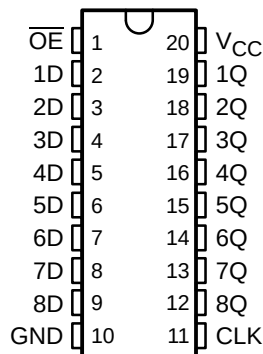
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

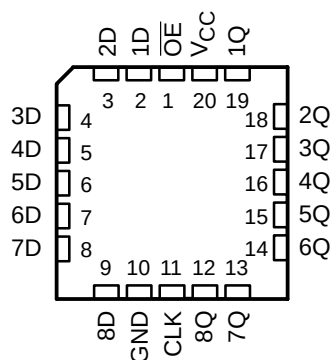
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

SN54LVC574A . . . J OR W PACKAGE
SN74LVC574A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVC574A . . . FK PACKAGE
(TOP VIEW)



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SN54LVC574A, SN74LVC574A

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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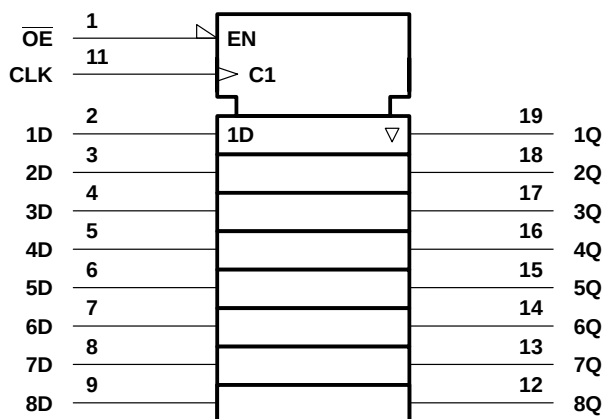
description (continued)

The SN54LVC574A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC574A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each flip-flop)

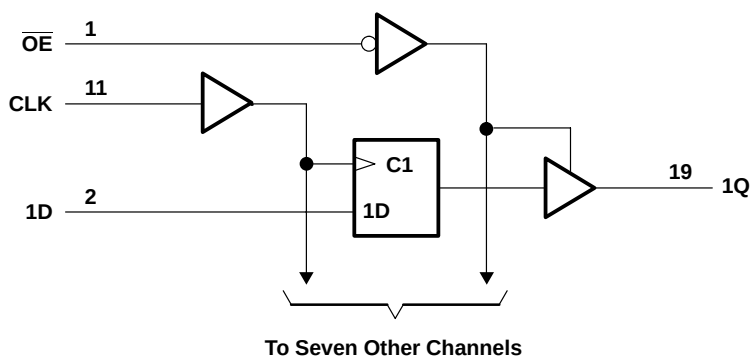
INPUTS			OUTPUT Q
OE	CLK	D	
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVC574A, SN74LVC574A

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVC574A		SN74LVC574A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3$ V to 2.7 V			1.7		
		$V_{CC} = 2.7$ V to 3.6 V	2		2		
V_{IL}	Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.35 \times V_{CC}$		V
		$V_{CC} = 2.3$ V to 2.7 V			0.7		
		$V_{CC} = 2.7$ V to 3.6 V		0.8	0.8		
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3 state	0	5.5	0	5.5	
I_{OH}	High-level output current	$V_{CC} = 1.65$ V				–4	mA
		$V_{CC} = 2.3$ V				–8	
		$V_{CC} = 2.7$ V		–12		–12	
		$V_{CC} = 3$ V		–24		–24	
I_{OL}	Low-level output current	$V_{CC} = 1.65$ V				4	mA
		$V_{CC} = 2.3$ V				8	
		$V_{CC} = 2.7$ V		12		12	
		$V_{CC} = 3$ V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	6	0	6	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVC574A, SN74LVC574A

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	SN54LVC574A			SN74LVC574A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OH}	I _{OH} = –100 μA		1.65 V to 3.6 V				V _{CC} –0.2			V
			2.7 V to 3.6 V	V _{CC} –0.2						
	I _{OH} = –4 mA		1.65 V				1.2			
	I _{OH} = –8 mA		2.3 V				1.7			
	I _{OH} = –12 mA		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	I _{OH} = –24 mA		3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA		1.65 V to 3.6 V				0.2			V
			2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA		1.65 V				0.45			
	I _{OL} = 8 mA		2.3 V				0.7			
	I _{OL} = 12 mA		2.7 V	0.4			0.4			
	I _{OL} = 24 mA		3 V	0.55			0.55			
I _I	V _I = 0 to 5.5 V		3.6 V	±5			±5			μA
I _{off}	V _I or V _O = 5.5 V		0				±10			μA
I _{OZ}	V _O = 0 to 5.5 V		3.6 V	±15			±10			μA
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	10			10			μA
	3.6 V ≤ V _I ≤ 5.5 V‡			10			10			
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND		3.3 V	4			4			pF
C _O	V _O = V _{CC} or GND		3.3 V	5.5			5.5			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

		SN54LVC574A				UNIT
		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	150		150		MHz
t _w	Pulse duration, CLK high or low	3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	2		2		ns
t _h	Hold time, data after CLK↑	2		2		ns



SN54LVC574A, SN74LVC574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		SN74LVC574A								UNIT
		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	†		†		150		150		MHz
t _w	Pulse duration, CLK high or low	†		†		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	†		†		2		2		ns
t _h	Hold time, data after CLK↑	†		†		1.5		1.5		ns

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC574A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
f _{max}			150		150		MHz
t _{pd}	D	Q	8		1	7	ns
t _{en}	OE	Q	9		1	7.5	ns
t _{dis}	OE	Q	7		0.5	6.4	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC574A								UNIT
			$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			†		†		150		150		MHz
t_{pd}	D	Q	†	†	†	†	8		2.2	7	ns
t_{en}	$\overline{\text{OE}}$	Q	†	†	†	†	8.5		1.5	7.5	ns
t_{dis}	$\overline{\text{OE}}$	Q	†	†	†	†	7		1.7	6.4	ns
$t_{\text{sk}(0)}^{\ddagger}$									1		ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	$f = 10\text{ MHz}$	†	†	43	pF
		Outputs disabled		†	†	15	

† This information was not available at the time of publication.



SN54LVC574A, SN74LVC574A

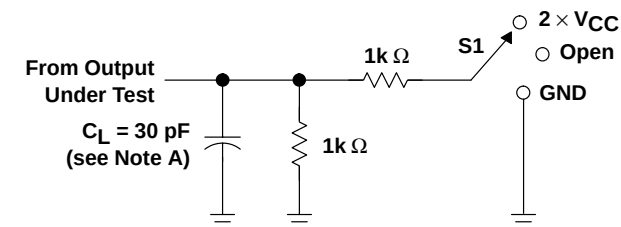
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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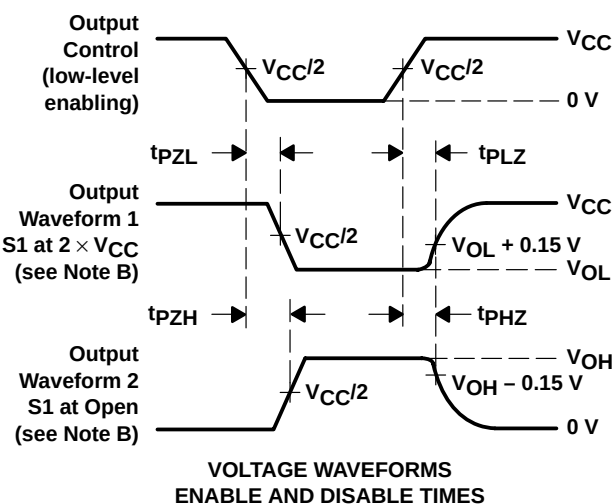
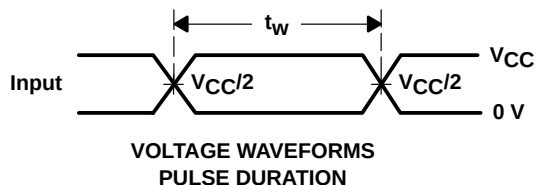
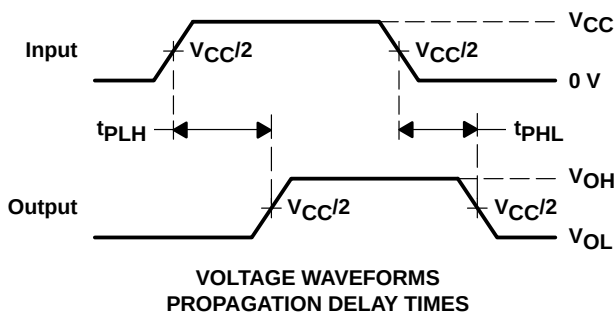
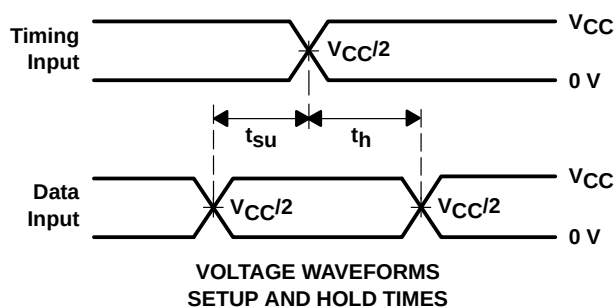
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

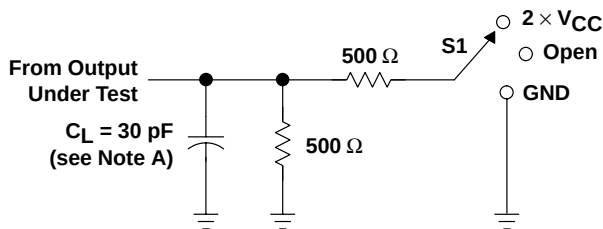
Figure 1. Load Circuit and Voltage Waveforms

SN54LVC574A, SN74LVC574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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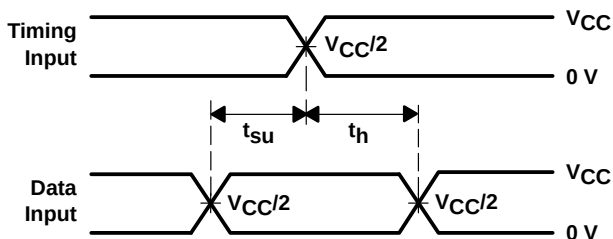
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

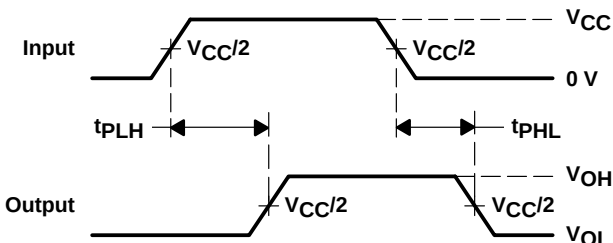


LOAD CIRCUIT

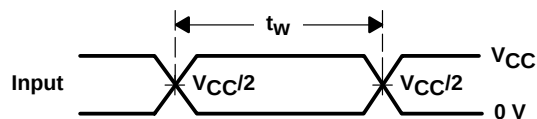
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



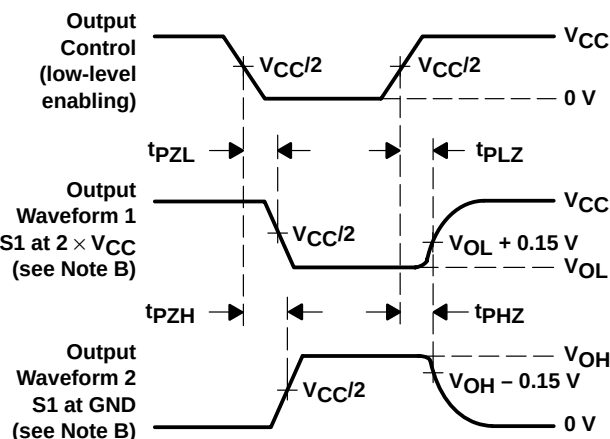
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN54LVC574A, SN74LVC574A

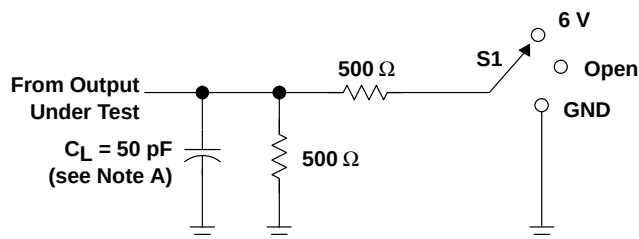
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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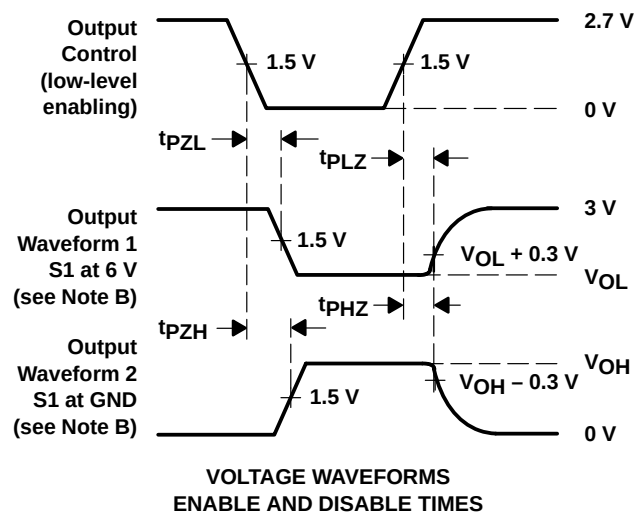
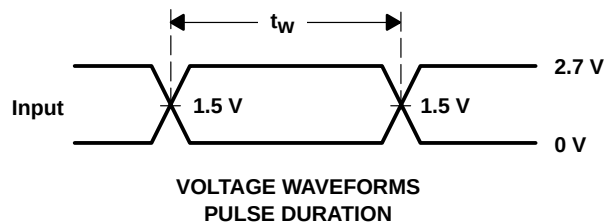
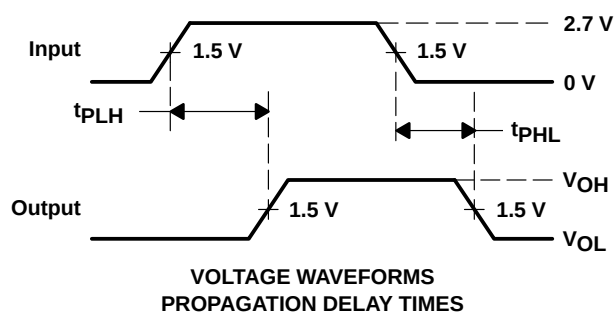
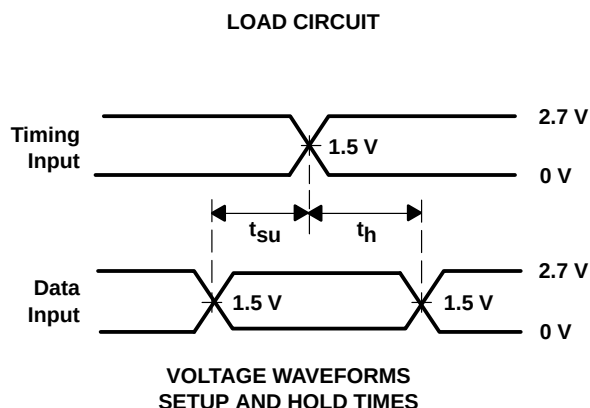
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC646A, SN74LVC646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCAS302G – JANUARY 1993 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Ceramic Chip Carriers (FK)**

description

The SN54LVC646A octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC646A octal bus transceiver and register is designed for 1.65-V to 3.6-V V_{CC} operation.

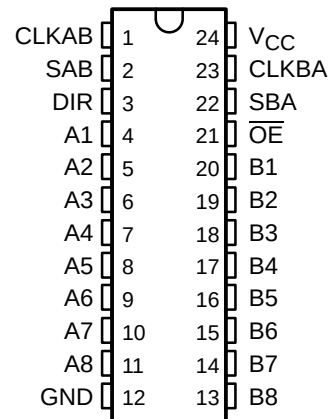
These devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that are performed with the 'LVC646A.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port is stored in either register or in both.

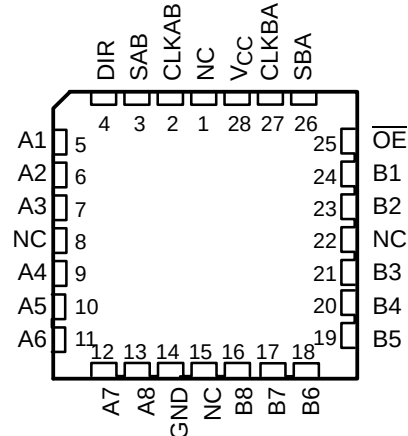
The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data is stored in one register and B data can be stored in the other register.

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

SN74LVC646A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVC646A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN54LVC646A, SN74LVC646A

OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

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description (continued)

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVC646A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC646A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	$\uparrow$	X	X	X	Input	Unspecified [†]	Store A, B unspecified [†]
X	X	X	$\uparrow$	X	X	Unspecified [†]	Input	Store B, A unspecified [†]
H	X	$\uparrow$	$\uparrow$	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

[†] The data-output functions can be enabled or disabled by various signals at $\overline{OE}$ and DIR. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

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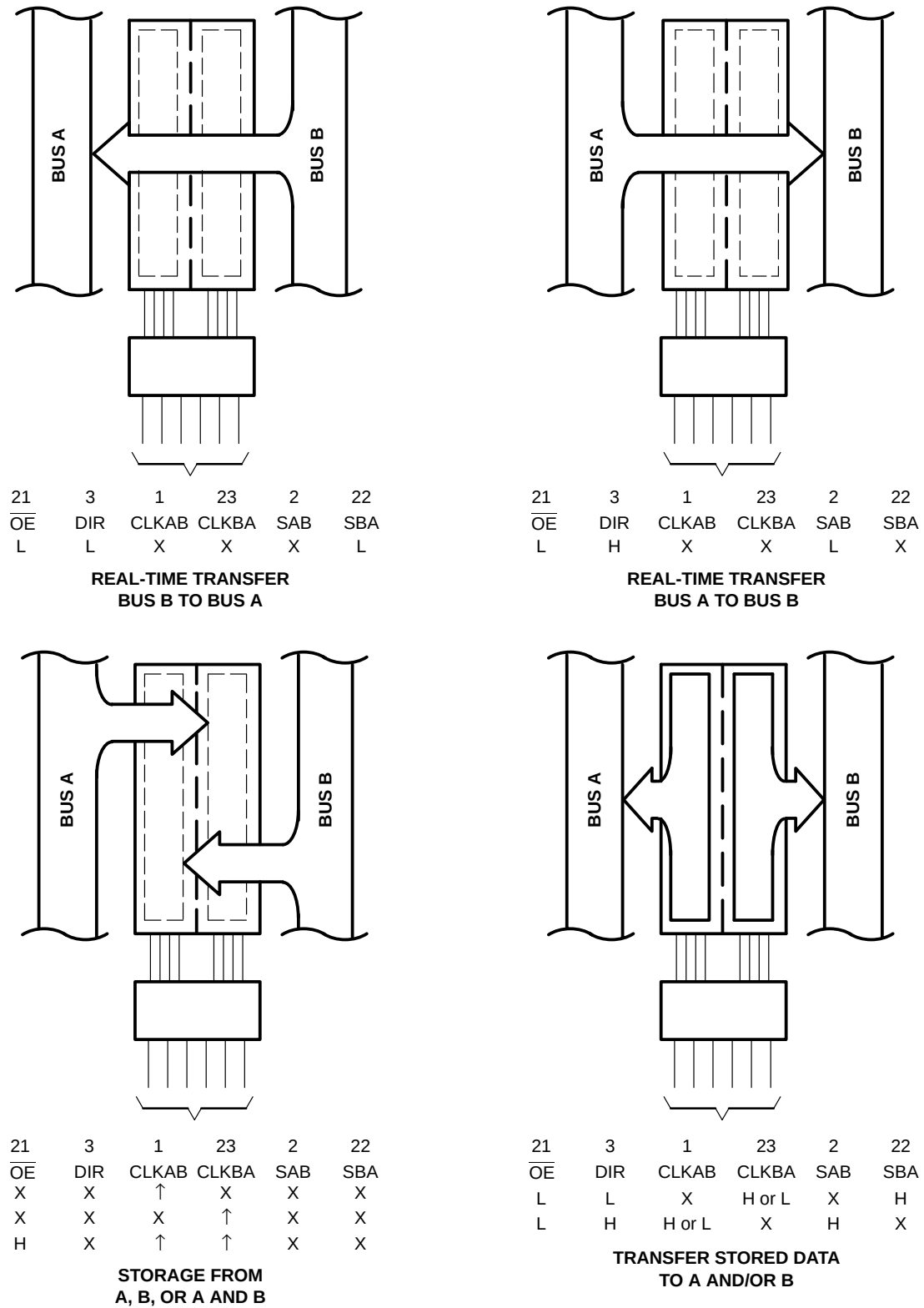


Figure 1. Bus-Management Functions

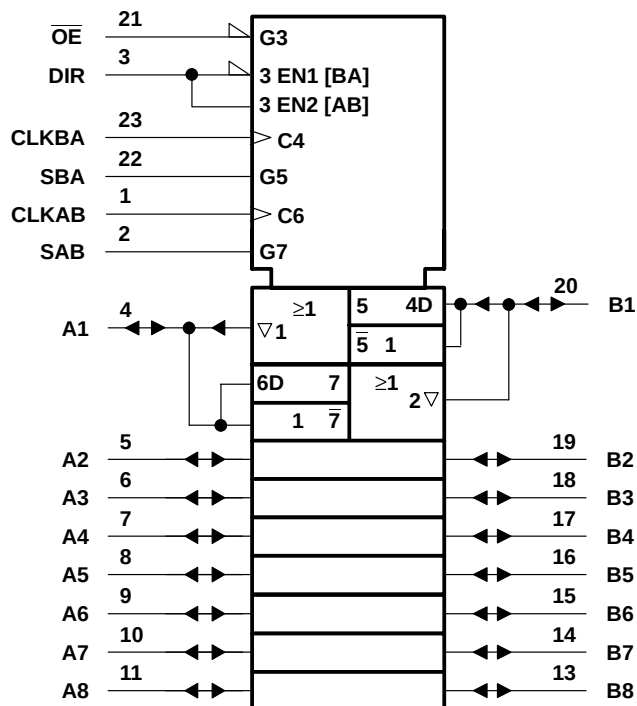
SN54LVC646A, SN74LVC646A

OCTAL BUS TRANSCEIVERS AND REGISTERS

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logic symbol†

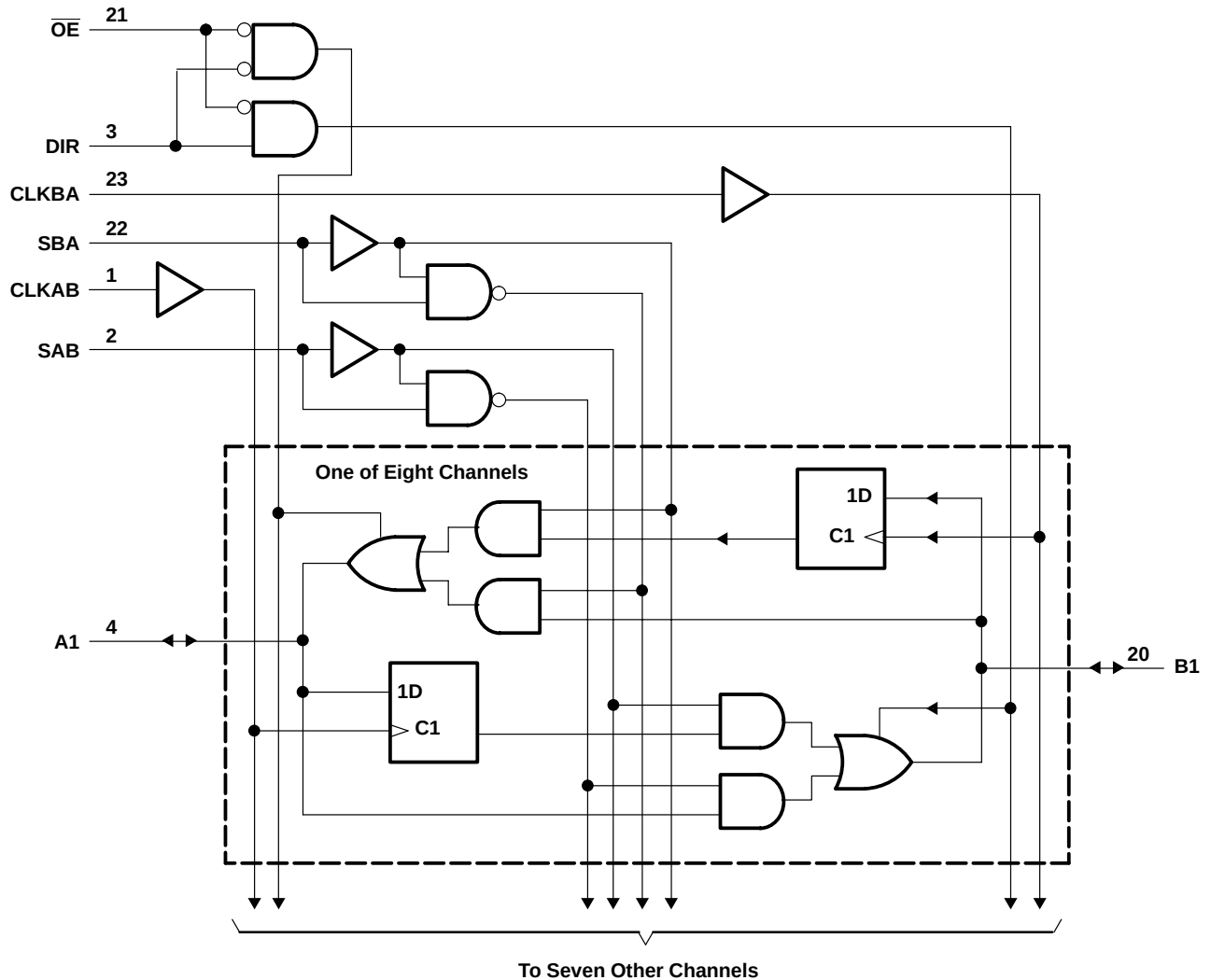


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, and PW packages.

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OCTAL BUS TRANSCEIVERS AND REGISTERS
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logic diagram (positive logic)



Pin numbers shown are for the DB, DW, and PW packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I : (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVC646A		SN74LVC646A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	Operating	2	3.6	1.65	3.6	V
	Data retention only	1.5		1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V			1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V			0.7		
	$V_{CC} = 2.7$ V to 3.6 V		0.8	0.8		
V_I Input voltage		0	5.5	0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
	3 state	0	5.5	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V				–4	mA
	$V_{CC} = 2.3$ V				–8	
	$V_{CC} = 2.7$ V		–12		–12	
	$V_{CC} = 3$ V		–24		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V				4	mA
	$V_{CC} = 2.3$ V				8	
	$V_{CC} = 2.7$ V		12		12	
	$V_{CC} = 3$ V		24		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	0	10	ns/V
T_A Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	SN54LVC646A			SN74LVC646A			UNIT	
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX		
V _{OH}		I _{OH} = –100 μA	1.65 V to 3.6 V				V _{CC} –0.2			V	
			2.7 V to 3.6 V	V _{CC} –0.2							
		I _{OH} = –4 mA	1.65 V				1.2				
		I _{OH} = –8 mA	2.3 V				1.7				
		I _{OH} = –12 mA	2.7 V	2.2			2.2				
			3 V	2.4			2.4				
		I _{OH} = –24 mA	3 V	2.2			2.2				
V _{OL}		I _{OL} = 100 μA	1.65 V to 3.6 V				0.2			V	
			2.7 V to 3.6 V	0.2							
		I _{OL} = 4 mA	1.65 V				0.45				
		I _{OL} = 8 mA	2.3 V				0.7				
		I _{OL} = 12 mA	2.7 V	0.4			0.4				
		I _{OL} = 24 mA	3 V	0.55			0.55				
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V	±5			±5			μA	
I _{off}		V _I or V _O = 5.5 V	0				±10			μA	
I _{OZ} [‡]		V _O = 0 to 5.5 V	3.6 V	±15			±10			μA	
I _{CC}	V _I = V _{CC} or GND		I _O = 0	3.6 V	10			10			μA
	3.6 V ≤ V _I ≤ 5.5 V§				10			10			
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500			μA	
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	4.5			4.5			pF	
C _{i0}	A or B ports	V _O = V _{CC} or GND	3.3 V	7.5			7.5			pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

		SN54LVC646A				UNIT
		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	150		150		MHz
t _w	Pulse duration	3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	1.6		1.5		ns
t _h	Hold time, data after CLK↑	1.7		1.7		ns



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 4)

		SN74LVC646A								UNIT
		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	†		†		150		150		MHz
t _w	Pulse duration	†		†		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	†		†		1.6		1.5		ns
t _h	Hold time, data after CLK↑	†		†		1.7		1.7		ns

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC646A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
f _{max}			150		150		MHz
t _{pd}	A or B	B or A	7.9		1	7.4	ns
	CLK	A or B	8.8		1	8.4	
	SBA or SAB		9.9		1	8.6	
t _{en}	$\overline{\text{OE}}$	A	10.2		1	8.2	ns
t _{dis}	$\overline{\text{OE}}$	A	8.9		1	7.5	ns
t _{en}	DIR	B	10.4		1	8.3	ns
t _{dis}	DIR	B	8.7		1	7.9	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC646A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		†		150		150		MHz
t _{pd}	A or B	B or A	†	†	†	†	7.9	1.4	7.4	ns	
	CLK	A or B	†	†	†	†	8.8	1.3	8.4		
	SBA or SAB		†	†	†	†	9.9	1.4	8.6		
t _{en}	$\overline{\text{OE}}$	A	†	†	†	†	10.2	1	8.2	ns	
t _{dis}	$\overline{\text{OE}}$	A	†	†	†	†	8.9	1	7.5	ns	
t _{en}	DIR	B	†	†	†	†	10.4	1.2	8.3	ns	
t _{dis}	DIR	B	†	†	†	†	8.7	1.1	7.9	ns	

† This information was not available at the time of publication.



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operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	f = 10 MHz	†	†	75	pF
		Outputs disabled		†	†	9	

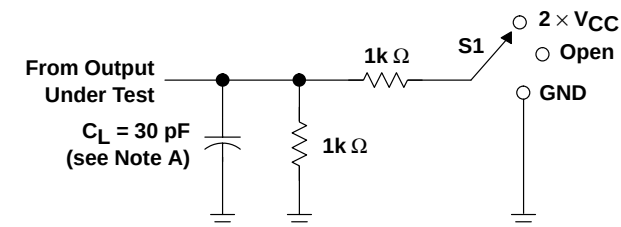
† This information was not available at the time of publication.

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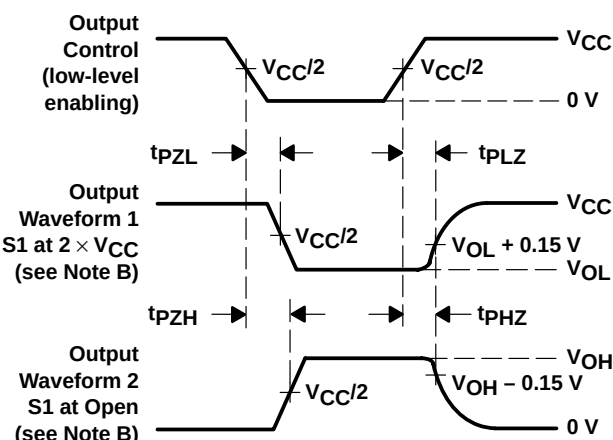
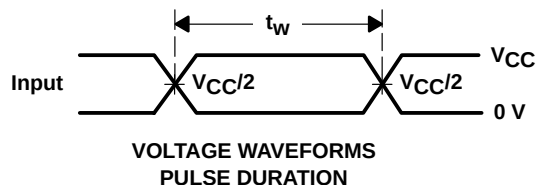
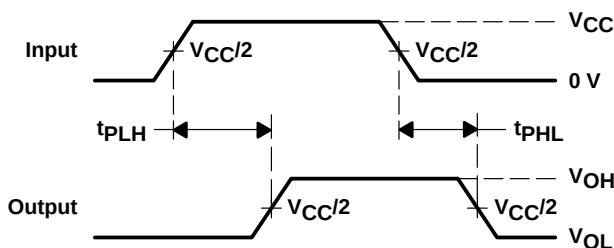
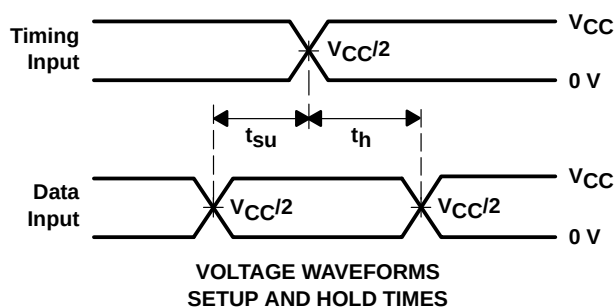
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

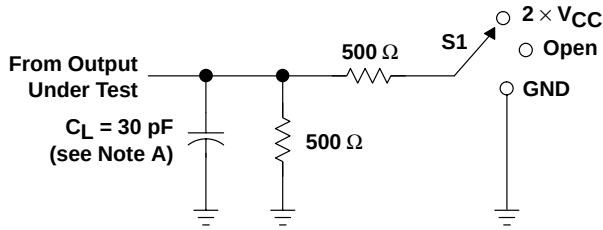
Figure 2. Load Circuit and Voltage Waveforms

SN54LVC646A, SN74LVC646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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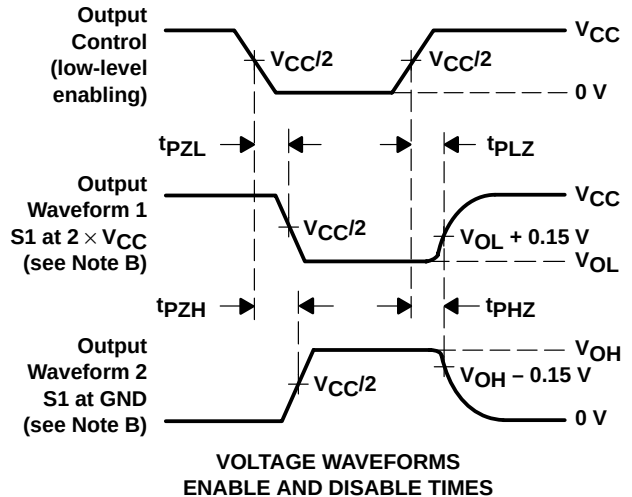
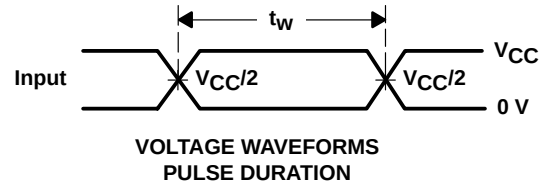
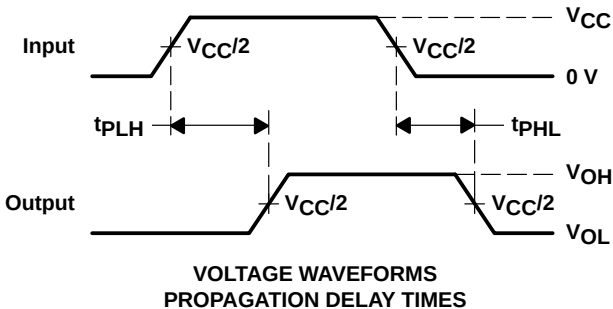
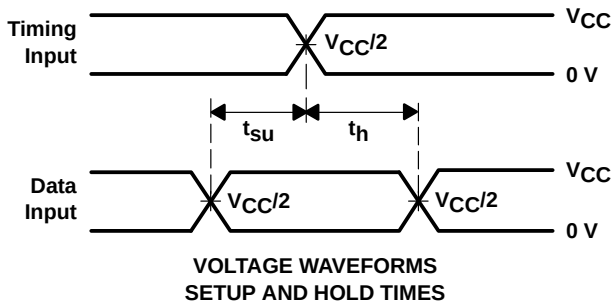
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



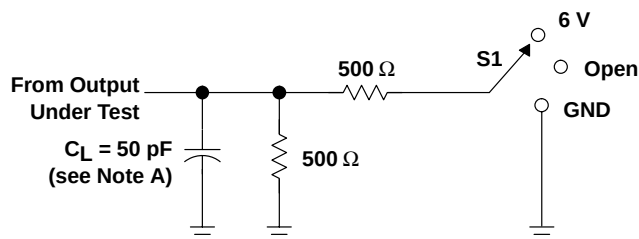
- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC646A, SN74LVC646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

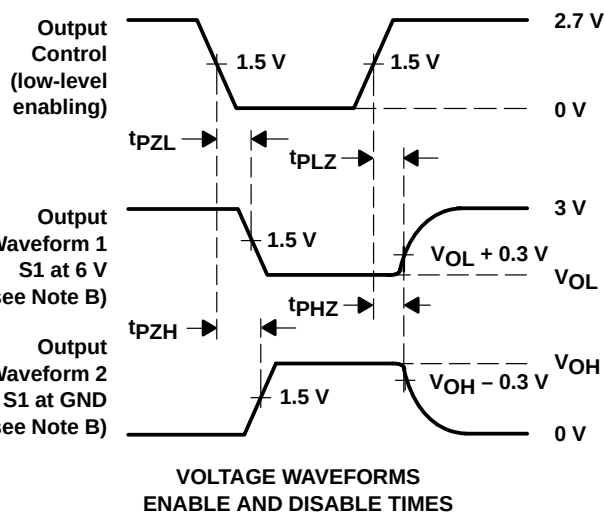
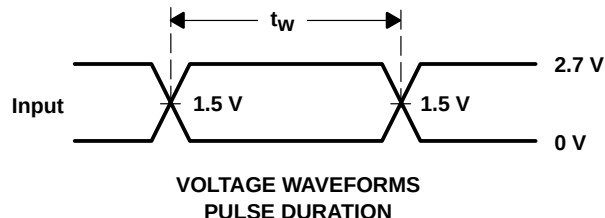
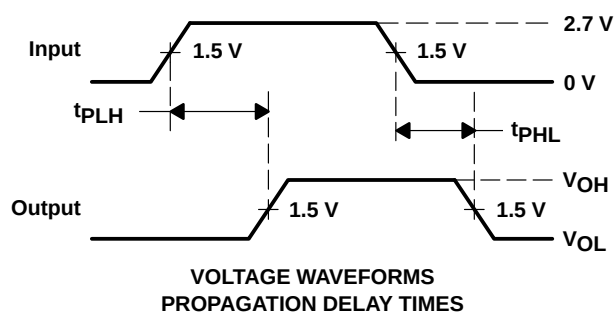
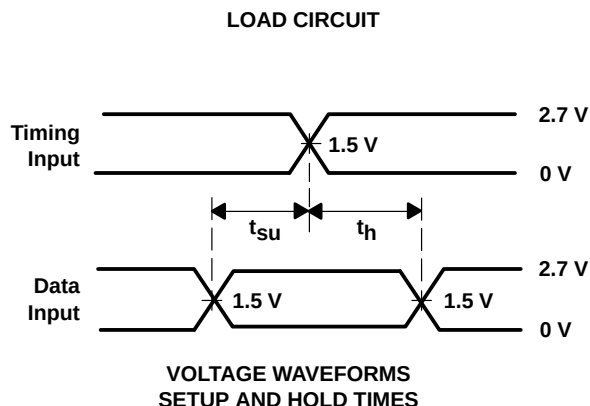
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PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 4. Load Circuit and Voltage Waveforms

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Ceramic Chip Carriers (FK)

description

The SN54LVC652A octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC652A octal bus transceiver and register is designed for 1.65-V to 3.6-V V_{CC} operation.

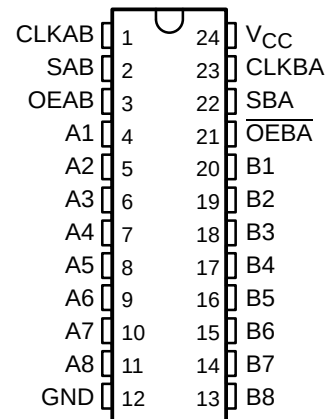
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that are performed with the 'LVC652A.

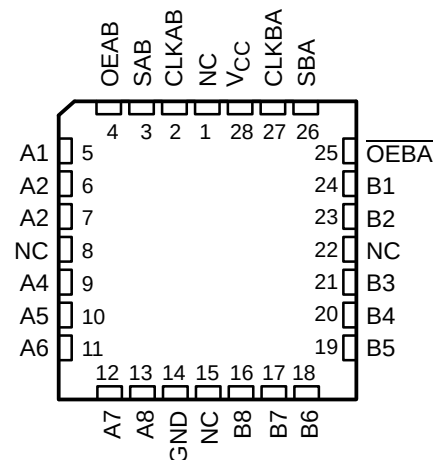
Data on the A or B data bus, or both, is stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

SN74LVC652A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVC652A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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description (continued)

To ensure the high-impedance state during power up or power down, $\overline{OEBA}$ should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54LVC652A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC652A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS						DATA I/O [†]		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified [‡]	Store A, hold B
H	H	↑	↑	X [‡]	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified [‡]	Input	Hold A, store B
L	L	↑	↑	X	X [‡]	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

[†] The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or $\overline{OEBA}$. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

[‡] Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered to load both registers.

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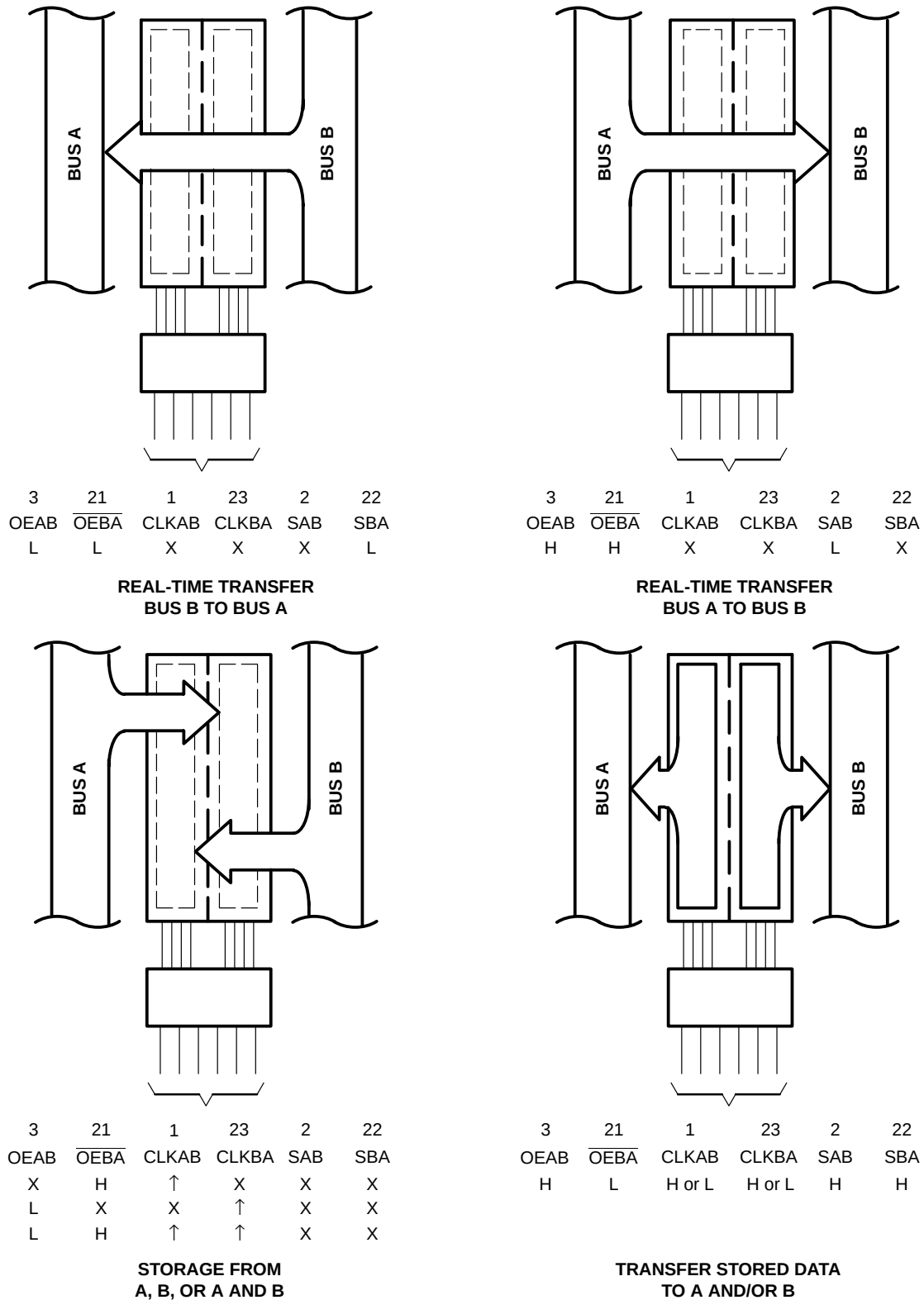


Figure 1. Bus-Management Functions

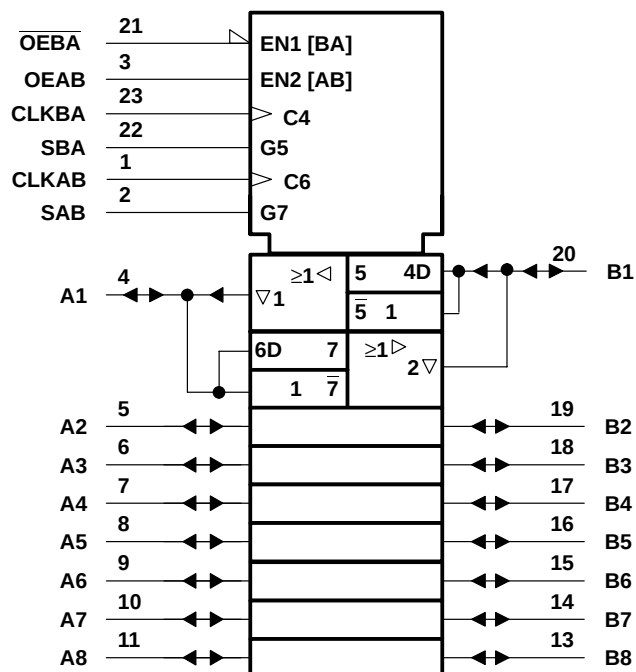
SN54LVC652A, SN74LVC652A

OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

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logic symbol†

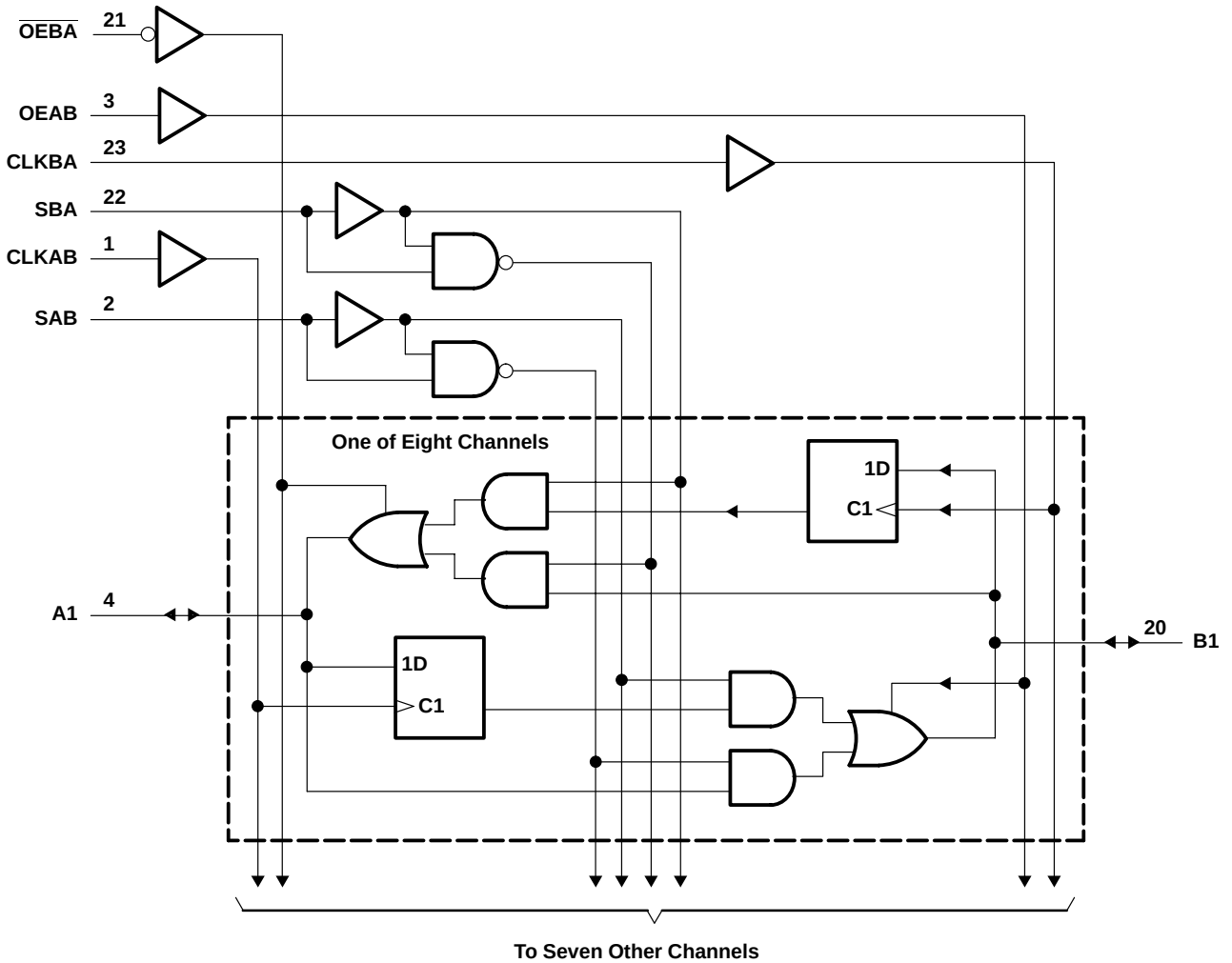


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, and PW packages.

SN54LVC652A, SN74LVC652A
OCTAL BUS TRANSCEIVERS AND REGISTERS
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logic diagram (positive logic)



Pin numbers shown are for the DB, DW, and PW packages.

SN54LVC652A, SN74LVC652A

OCTAL BUS TRANSCEIVERS AND REGISTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVC652A		SN74LVC652A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	Operating	2	3.6	1.65	3.6	V
	Data retention only	1.5		1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V			1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V			0.7		
	$V_{CC} = 2.7$ V to 3.6 V		0.8	0.8		
V_I Input voltage		0	5.5	0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
	3 state	0	5.5	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V				–4	mA
	$V_{CC} = 2.3$ V				–8	
	$V_{CC} = 2.7$ V		–12		–12	
	$V_{CC} = 3$ V		–24		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V				4	mA
	$V_{CC} = 2.3$ V				8	
	$V_{CC} = 2.7$ V		12		12	
	$V_{CC} = 3$ V		24		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	5	0	5	ns/V
T_A Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	SN54LVC652A			SN74LVC652A			UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V				V _{CC} –0.2			V	
		2.7 V to 3.6 V	V _{CC} –0.2							
	I _{OH} = –4 mA	1.65 V				1.2				
	I _{OH} = –8 mA	2.3 V				1.7				
	I _{OH} = –12 mA	2.7 V	2.2			2.2				
		3 V	2.4			2.4				
	I _{OH} = –24 mA	3 V	2.2			2.2				
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.2			V	
		2.7 V to 3.6 V	0.2							
	I _{OL} = 4 mA	1.65 V				0.45				
	I _{OL} = 8 mA	2.3 V				0.7				
	I _{OL} = 12 mA	2.7 V	0.4			0.4				
	I _{OL} = 24 mA	3 V	0.55			0.55				
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V	±5			±5			μA
I _{off}		V _I or V _O = 5.5 V	0				±10			μA
I _{OZ} [‡]		V _O = 0 to 5.5 V	3.6 V	±15			±10			μA
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	10			10			μA
	3.6 V ≤ V _I ≤ 5.5 V [§]			10			10			
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500			μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	4.5			4.5			pF
C _{iO}	A or B ports	V _O = V _{CC} or GND	3.3 V	7.5			7.5			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

		SN54LVC652A				UNIT
		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	80		100		MHz
t _w	Pulse duration	3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	1.6		1.5		ns
t _h	Hold time, data after CLK↑	0.5		1.5		ns

SN54LVC652A, SN74LVC652A

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 4)

		SN74LVC652A								UNIT
		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	†		†		80		100		MHz
t _w	Pulse duration	†		†		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	†		†		1.6		1.5		ns
t _h	Hold time, data after CLK↑	†		†		0.5		1.5		ns

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC652A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
f _{max}			80		100		MHz
t _{pd}	A or B	B or A	7.8		1	7.4	ns
	CLK	A or B	8.4		1	8	
	SAB or SBA	B or A	9.6		1	8.7	
t _{en}	$\overline{\text{OEBA}}$	A	8.9		1	7.4	ns
t _{dis}	$\overline{\text{OEBA}}$	A	8.1		1	7.5	ns
t _{en}	OEAB	B	8.6		1	7.1	ns
t _{dis}	OEAB	B	7.7		1	7.4	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC652A								UNIT
			$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		†		80		100		MHz
t _{pd}	A or B	B or A	†	†	†	†	7.8	1.5	7.4	ns	
	CLK	A or B	†	†	†	†	8.4	1.5	8		
	SAB or SBA	B or A	†	†	†	†	9.6	1.5	8.7		
t _{en}	$\overline{\text{OEBA}}$	A	†	†	†	†	8.9	1.5	7.4	ns	
t _{dis}	$\overline{\text{OEBA}}$	A	†	†	†	†	8.1	1.5	7.5	ns	
t _{en}	OEAB	B	†	†	†	†	8.6	1.5	7.1	ns	
t _{dis}	OEAB	B	†	†	†	†	7.7	1.5	7.4	ns	

† This information was not available at the time of publication.



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operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	f = 10 MHz	†	†	84	pF
		Outputs disabled		†	†	9.5	

† This information was not available at the time of publication.

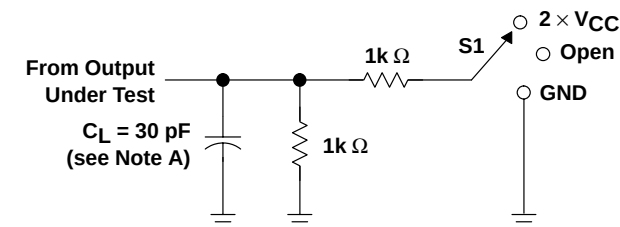


SN54LVC652A, SN74LVC652A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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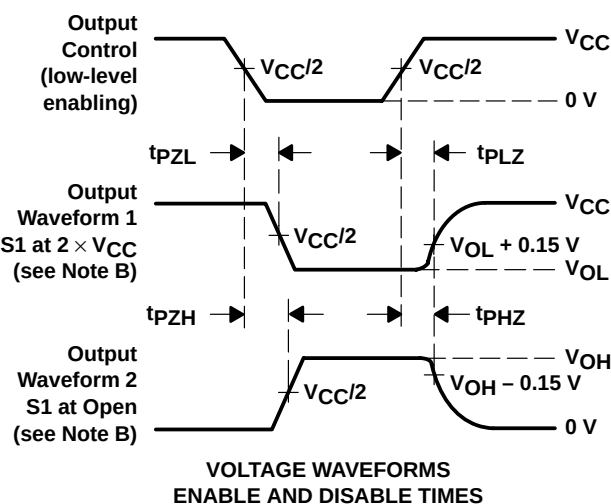
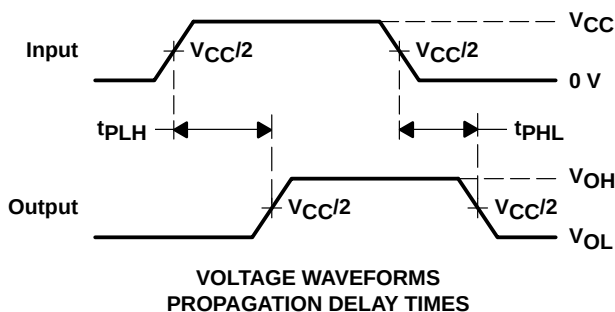
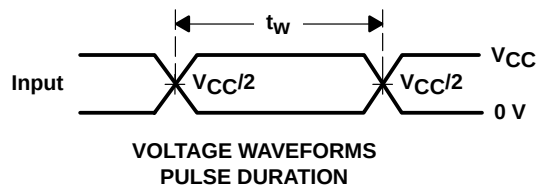
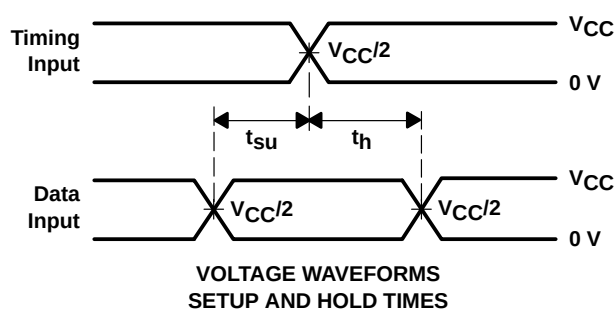
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	Open



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

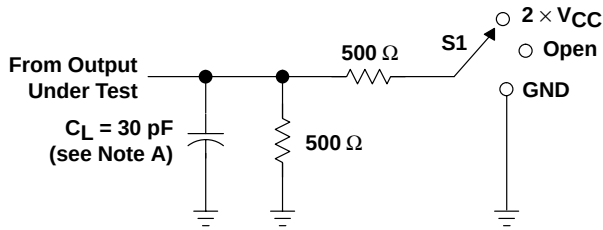
Figure 2. Load Circuit and Voltage Waveforms

SN54LVC652A, SN74LVC652A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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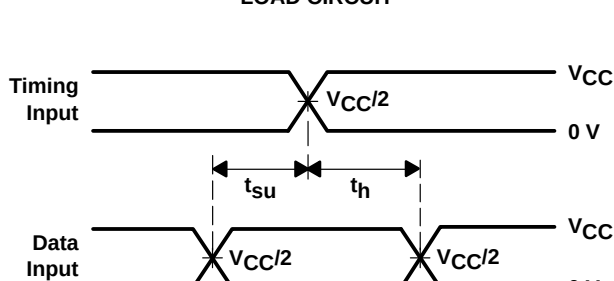
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

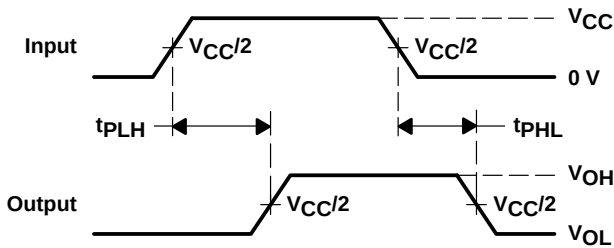


LOAD CIRCUIT

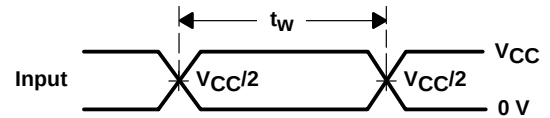
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



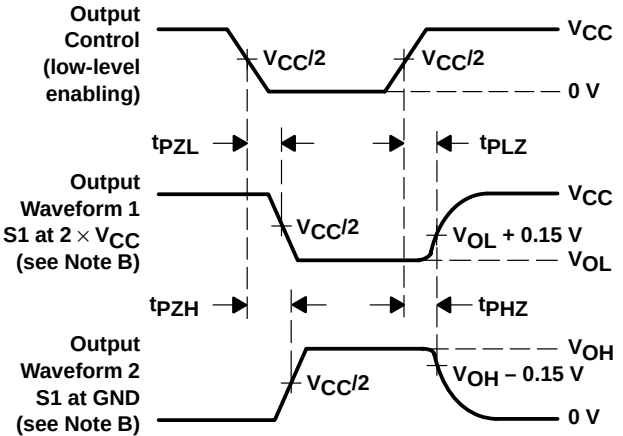
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

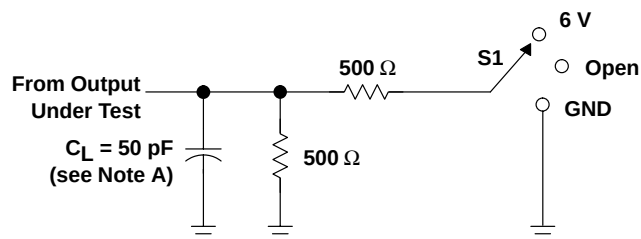
- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN54LVC652A, SN74LVC652A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

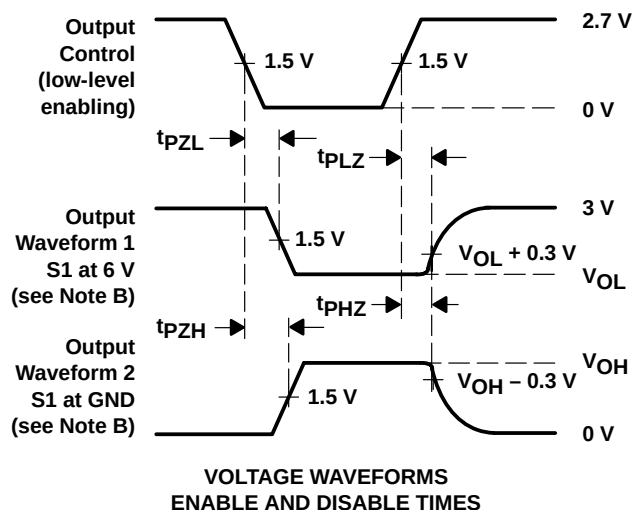
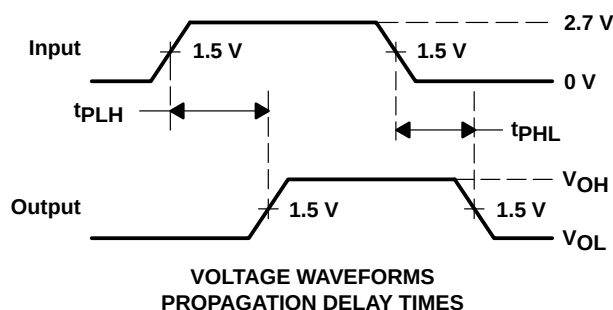
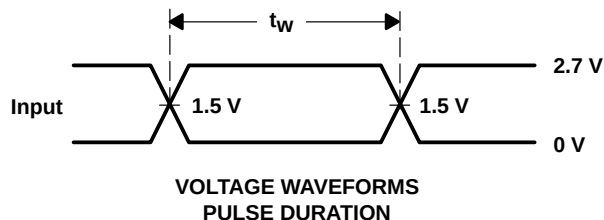
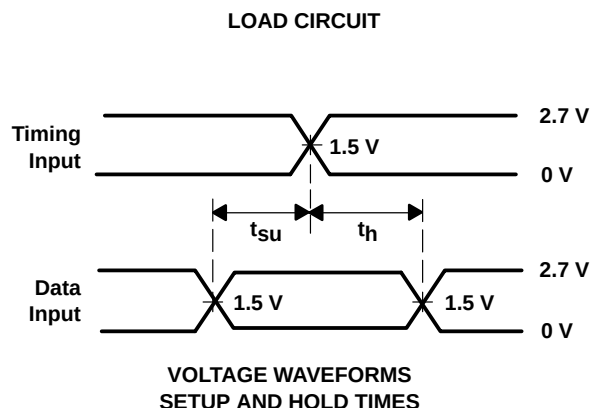
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PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 4. Load Circuit and Voltage Waveforms

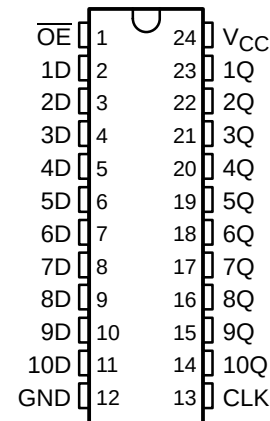
SN74LVC821A

10-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS304F – MARCH 1993 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Power Off Disables Outputs, Permitting Live Insertion
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 10-bit bus-interface flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC821A features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC821A is characterized for operation from -40°C to 85°C .

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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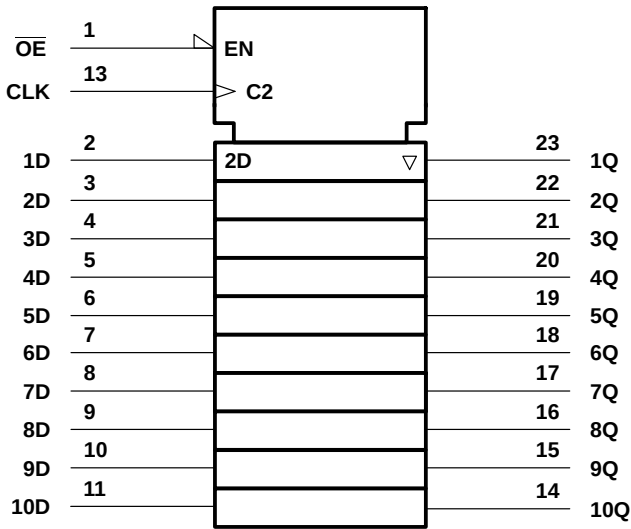
SN74LVC821A
10-BIT BUS-INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each flip-flop)

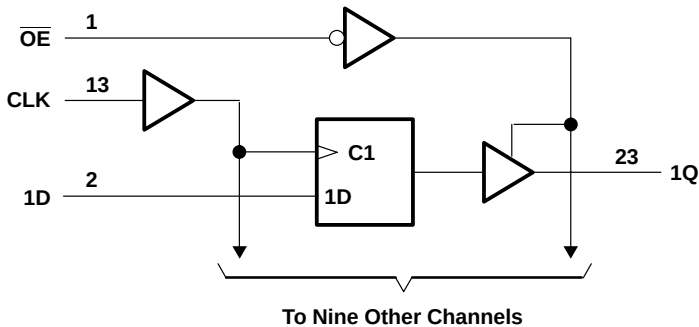
INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC821A

10-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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10-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 μA			1.65 V to 3.6 V	V _{CC} –0.2			V
	I _{OH} = –4 mA			1.65 V	1.2			
	I _{OH} = –8 mA			2.3 V	1.7			
	I _{OH} = –12 mA			2.7 V	2.2			
				3 V	2.4			
I _{OH} = –24 mA			3 V	2.2				
V _{OL}	I _{OL} = 100 μA			1.65 V to 3.6 V			0.2	V
	I _{OL} = 4 mA			1.65 V			0.45	
	I _{OL} = 8 mA			2.3 V			0.7	
	I _{OL} = 12 mA			2.7 V			0.4	
	I _{OL} = 24 mA			3 V			0.55	
I _I	V _I = 0 to 5.5 V			3.6 V			±5	μA
I _{off}	V _I or V _O = 5.5 V			0			±10	μA
I _{OZ}	V _O = 0 to 5.5 V			3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND		I _O = 0	3.6 V			10	μA
	3.6 V ≤ V _I ≤ 5.5 V [‡]						10	
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V		500		μA
C _i	Control inputs	V _I = V _{CC} or GND		3.3 V			5	pF
	Data inputs						4	
C _O		V _O = V _{CC} or GND		3.3 V		7		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	§		§		150		150		MHz
t _w	Pulse duration, CLK high or low	§		§		3.3		3.3		ns
t _{su}	Setup time, data before CLK	§		§		1.9		1.9		ns
t _h	Hold time, data after CLK	§		§		1.5		1.5		ns

§ This information was not available at the time of publication.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			†		†		150		150		MHz
t_{pd}	CLK	Q	†	†	†	†	8.5		2.2	7.3	ns
t_{en}	$\overline{OE}$	Q	†	†	†	†	8.8		1.3	7.6	ns
t_{dis}	$\overline{OE}$	Q	†	†	†	†	6.8		1.6	6.2	ns
$t_{sk(o)}^{\ddagger}$									1		ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	f = 10 MHz	†	†	65	pF
		Outputs disabled		†	†	48	

† This information was not available at the time of publication.

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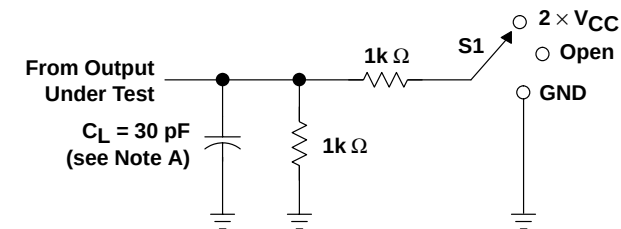
10-BIT BUS-INTERFACE FLIP-FLOP

WITH 3-STATE OUTPUTS

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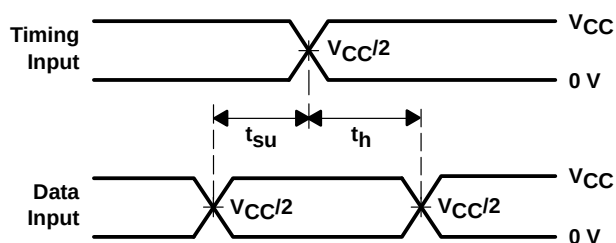
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

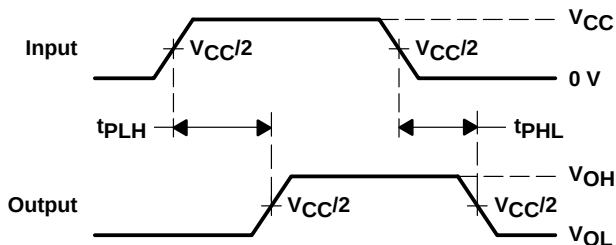


LOAD CIRCUIT

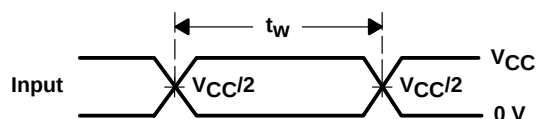
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



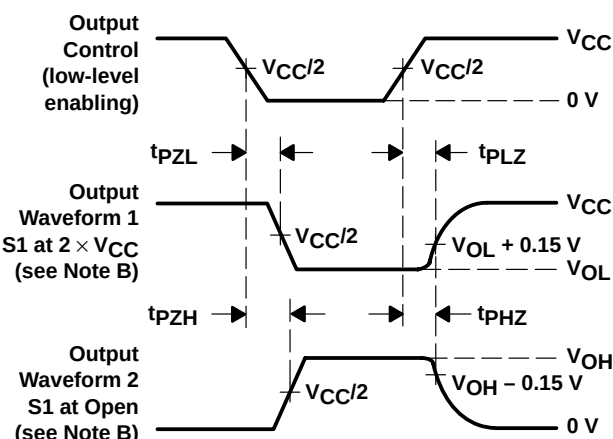
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



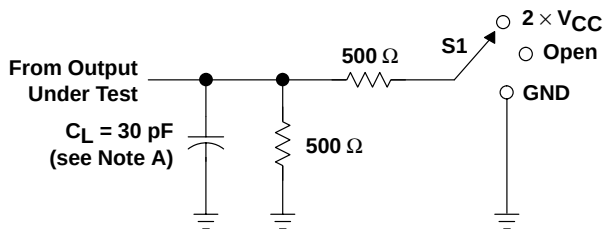
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

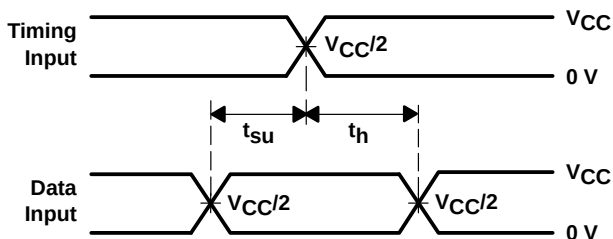
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

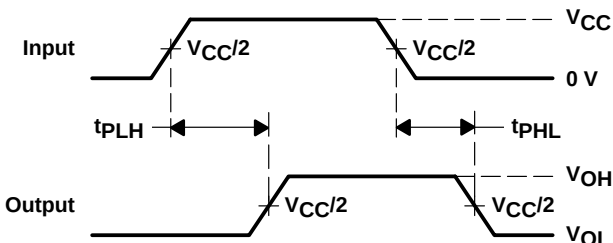


LOAD CIRCUIT

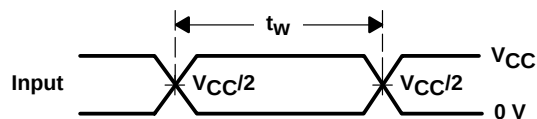
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



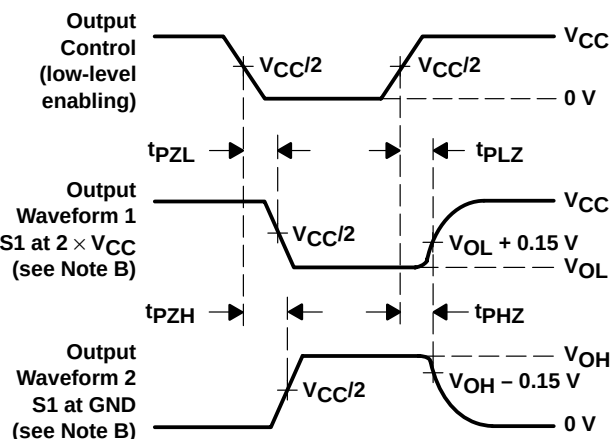
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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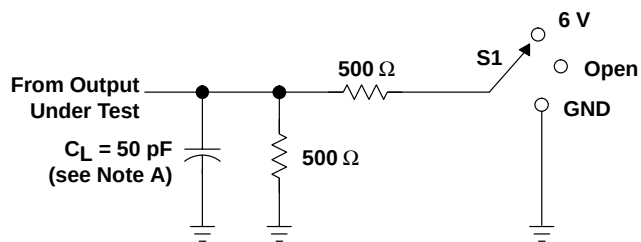
10-BIT BUS-INTERFACE FLIP-FLOP

WITH 3-STATE OUTPUTS

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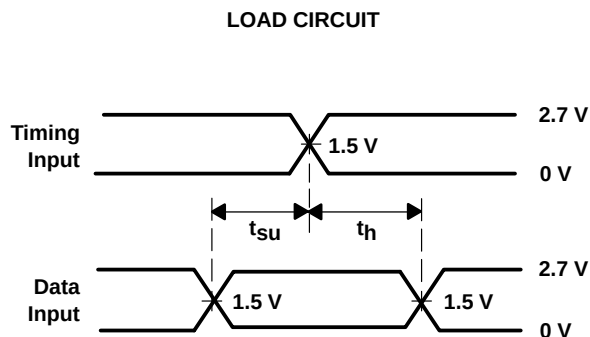
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$

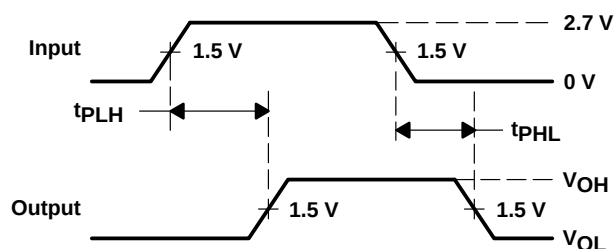


LOAD CIRCUIT

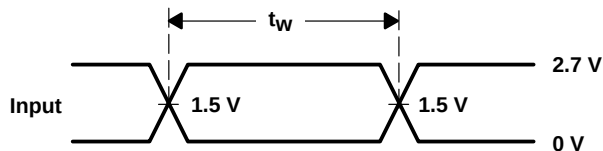
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



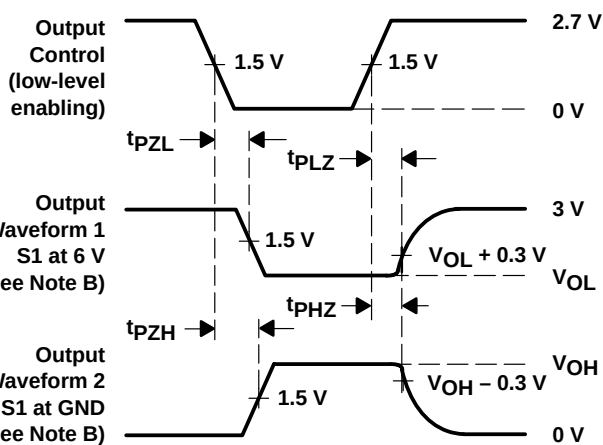
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

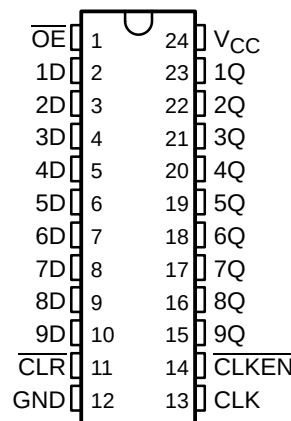
SN74LVC823A

9-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Power Off Disables Inputs/Outputs, Permitting Live Insertion
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 9-bit bus-interface flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC823A is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

With the clock-enable ($\overline{\text{CLKEN}}$) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high disables the clock buffer, latching the outputs. This device has noninverting data (D) inputs. Taking the clear ($\overline{\text{CLR}}$) input low causes the nine Q outputs to go low, independently of the clock.

A buffered output-enable ($\overline{\text{OE}}$) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. $\overline{\text{OE}}$ does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC823A is characterized for operation from -40°C to 85°C .

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN74LVC823A 9-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

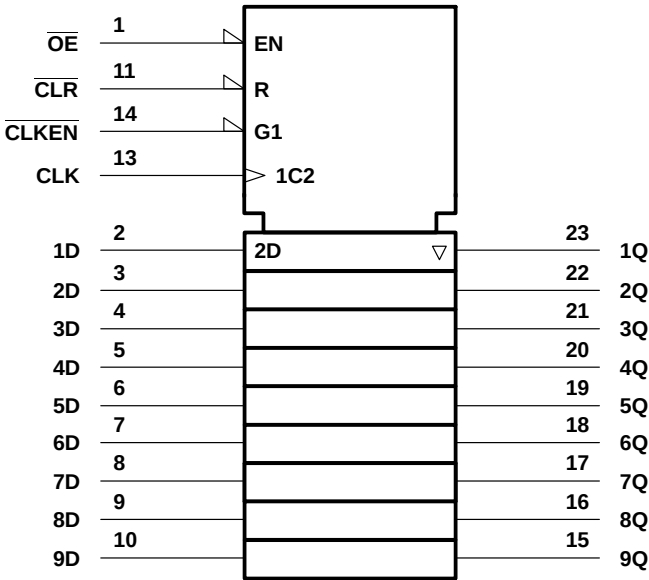
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FUNCTION TABLE

(each flip-flop)

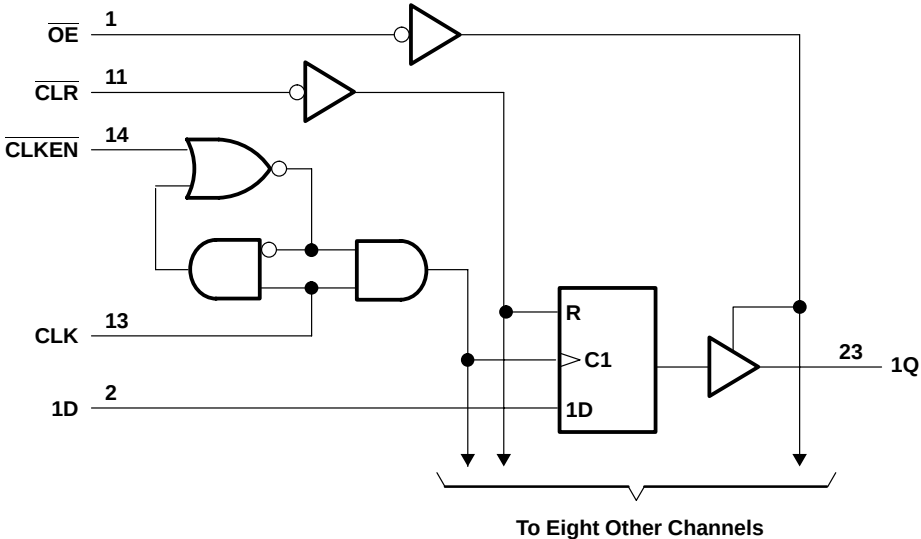
INPUTS					OUTPUT Q
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q ₀
H	X	X	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}		I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
		I _{OH} = –4 mA	1.65 V	1.2			
		I _{OH} = –8 mA	2.3 V	1.7			
		I _{OH} = –12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = –24 mA	3 V	2.2			
V _{OL}		I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
		I _{OL} = 4 mA	1.65 V	0.45			
		I _{OL} = 8 mA	2.3 V	0.7			
		I _{OL} = 12 mA	2.7 V	0.4			
		I _{OL} = 24 mA	3 V	0.55			
I _I		V _I = 0 to 5.5 V	3.6 V	±5			µA
I _{off}		V _I or V _O = 5.5 V	0	±10			µA
I _{OZ}		V _O = 0 to 5.5 V	3.6 V	±10			µA
I _{CC}		V _I = V _{CC} or GND	3.6 V	10			µA
		3.6 V ≤ V _I ≤ 5.5 V [‡]		10			
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	5			pF
	Data inputs			4			
C _O		V _O = V _{CC} or GND	3.3 V	7			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		§		§		150		150		MHz
t _w	Pulse duration	CL _R low	§		§		3.3		3.3		ns
		CLK high or low	§		§		3.3		3.3		
t _{su}	Setup time	CL _R inactive before CLK↑	§		§		1		1		ns
		Data before CLK↑	§		§		1.3		1.3		
		CL _{KEN} low before CLK↑	§		§		1.8		1.8		
t _h	Hold time	Data after CLK↑	§		§		2		2		ns
		CL _{KEN} low after CLK↑	§		§		1.3		1.3		

§ This information was not available at the time of publication.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			†		†		150		150		MHz
t_{pd}	CLK	Q	†	†	†	†	8.9		1.4	8	ns
	$\overline{\text{CLR}}$		†	†	†	†	8.8		2.5	7.9	
t_{en}	$\overline{\text{OE}}$	Q	†	†	†	†	8.3		1.6	7.2	ns
t_{dis}	$\overline{\text{OE}}$	Q	†	†	†	†	7.1		1.1	6	ns
$t_{sk(o)}^{\ddagger}$									1		ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	$f = 10\text{ MHz}$	†	†	59	pF
		Outputs disabled		†	†	46	

† This information was not available at the time of publication.

SN74LVC823A

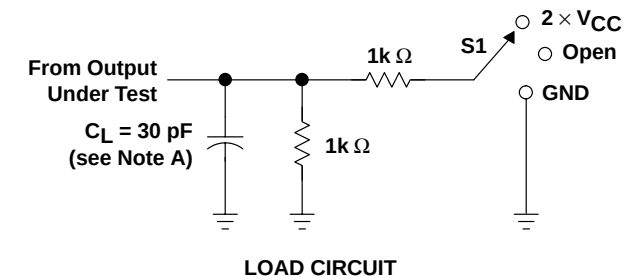
9-BIT BUS-INTERFACE FLIP-FLOP

WITH 3-STATE OUTPUTS

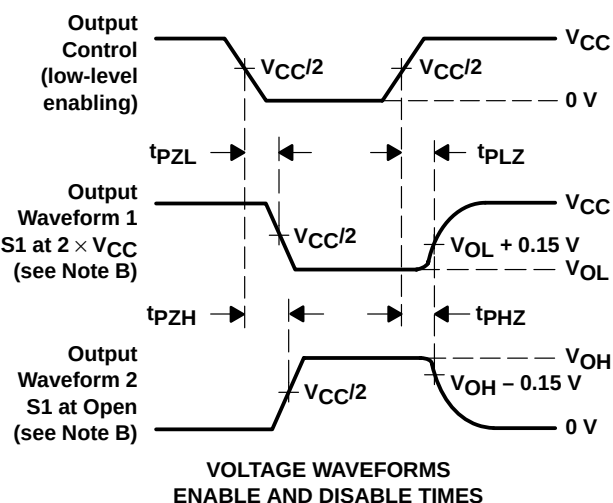
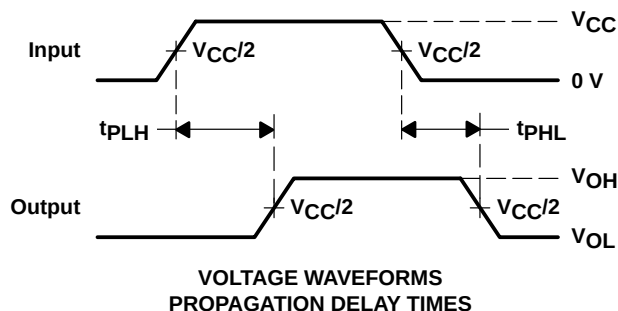
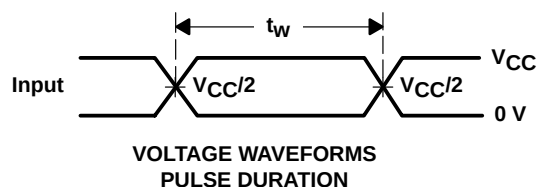
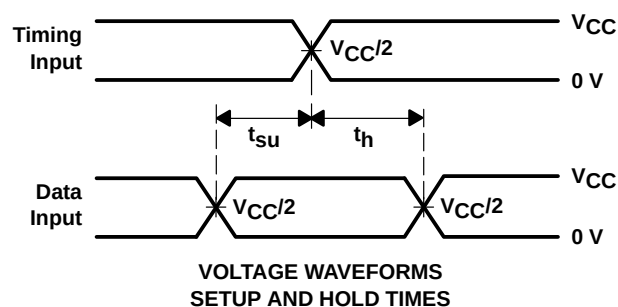
SCAS305F – MARCH 1993 – REVISED JUNE 1998

PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open

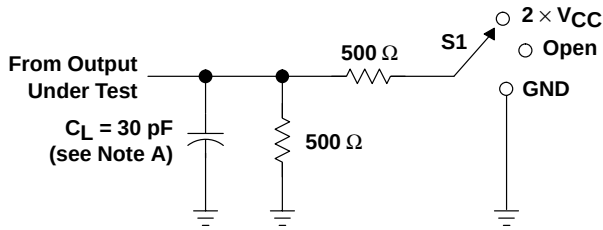


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

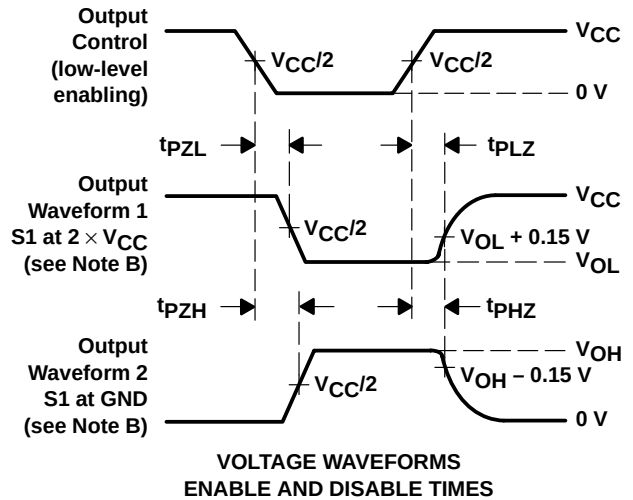
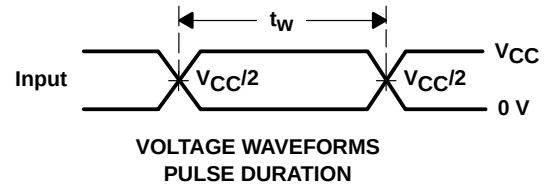
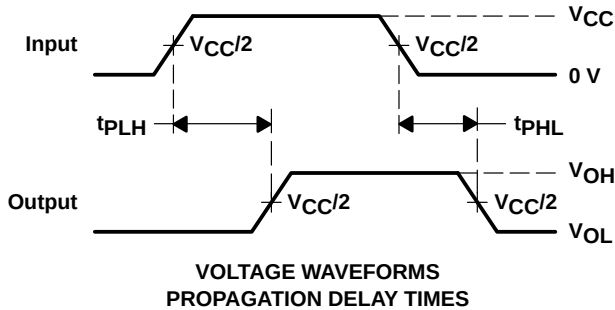
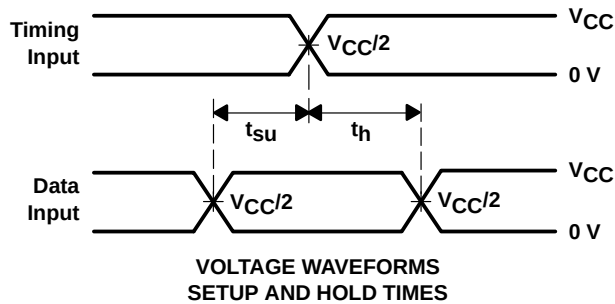
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PHL}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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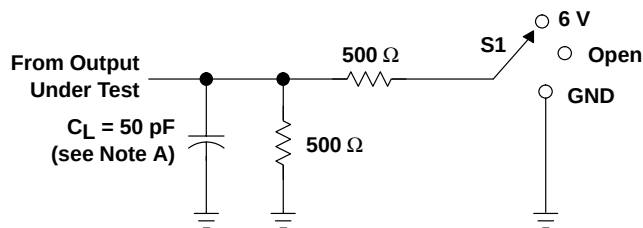
9-BIT BUS-INTERFACE FLIP-FLOP

WITH 3-STATE OUTPUTS

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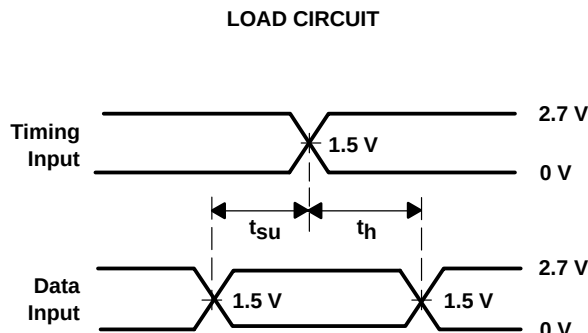
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

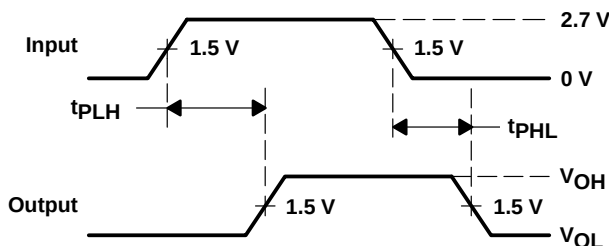


LOAD CIRCUIT

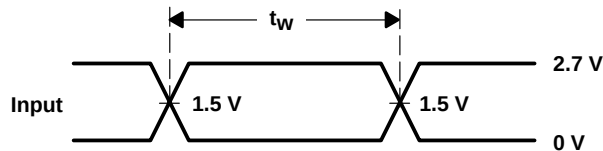
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



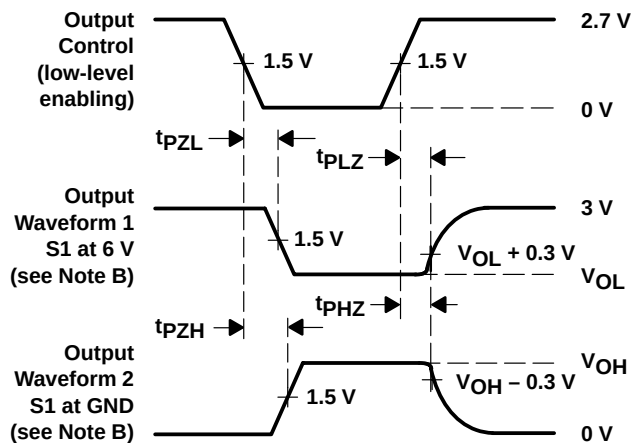
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

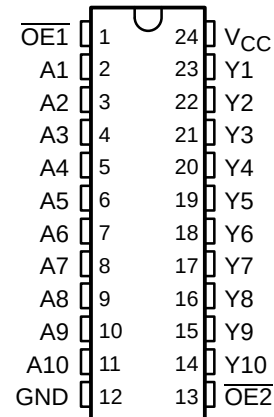
SN74LVC827A

10-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 10-bit buffer/bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC827A provides a high-performance bus interface for wide datapaths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all ten outputs are in the high-impedance state. The SN74LVC827A provides true data at its outputs.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC827A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

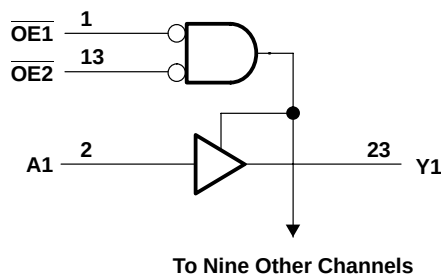
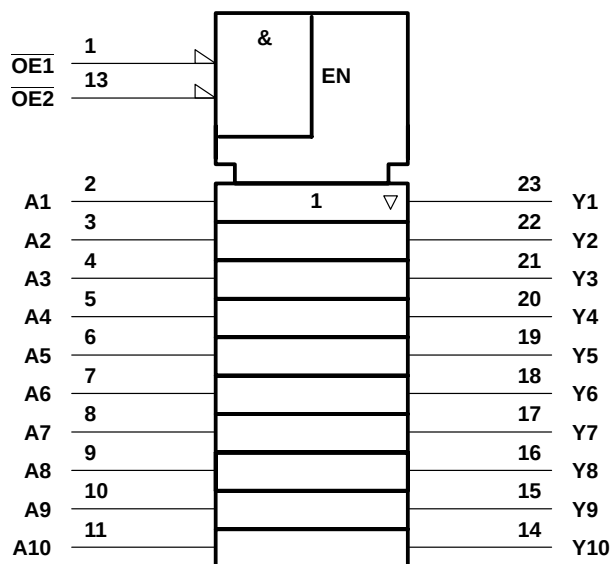


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logic diagram (positive logic)



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	−0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	−0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:

1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JEDEC 51.

SN74LVC827A
10-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	High or low state	0	V _{CC}	V
		3 state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V	−4		mA
		V _{CC} = 2.3 V	−8		
		V _{CC} = 2.7 V	−12		
		V _{CC} = 3 V	−24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		mA
		V _{CC} = 2.3 V	8		
		V _{CC} = 2.7 V	12		
		V _{CC} = 3 V	24		
Δt/Δv	Input transition rise or fall rate	0	10	ns/V	
T _A	Operating free-air temperature	−40	85	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74LVC827A
10-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}		I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
		I _{OH} = –4 mA	1.65 V	1.2			
		I _{OH} = –8 mA	2.3 V	1.7			
		I _{OH} = –12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = –24 mA	3 V	2.2			
V _{OL}		I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
		I _{OL} = 4 mA	1.65 V	0.45			
		I _{OL} = 8 mA	2.3 V	0.7			
		I _{OL} = 12 mA	2.7 V	0.4			
		I _{OL} = 24 mA	3 V	0.55			
I _I		V _I = 0 to 5.5 V	3.6 V	±5			µA
I _{off}		V _I or V _O = 5.5 V	0	±10			µA
I _{OZ}		V _O = 0 to 5.5 V	3.6 V	±10			µA
I _{CC}		V _I = V _{CC} or GND	3.6 V	10			µA
		3.6 V ≤ V _I ≤ 5.5 V [‡]		10			
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	5			pF
	Data inputs			4			
C _O		V _O = V _{CC} or GND	3.3 V	7			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	§	§	§	§	7.1		1	6.7	ns
t _{en}	$\overline{OE}$	Y	§	§	§	§	8.5		1	7.3	ns
t _{dis}	$\overline{OE}$	Y	§	§	§	§	7.3		1.8	6.7	ns
t _{sk(o)} [¶]										1	ns

§ This information was not available at the time of publication.

¶ Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

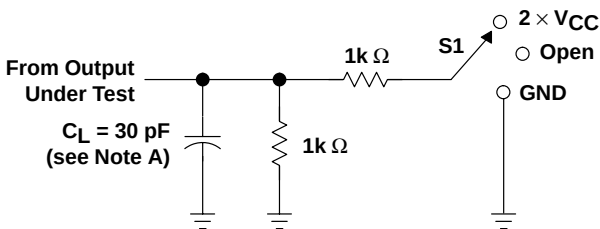
PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	§	§	24	pF
		Outputs disabled		§	§	5	

§ This information was not available at the time of publication.



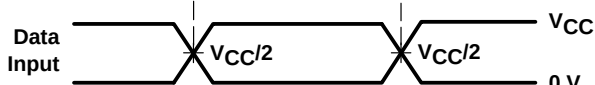
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

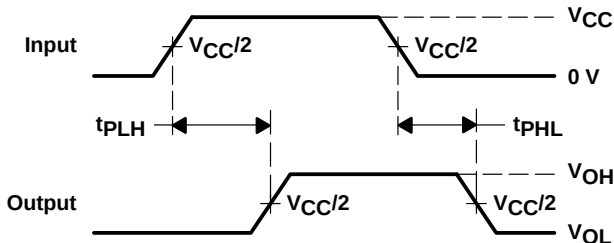


LOAD CIRCUIT

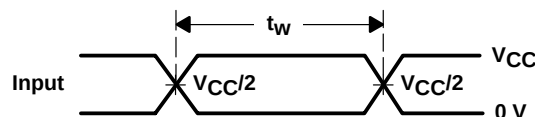
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



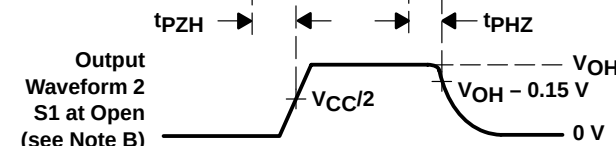
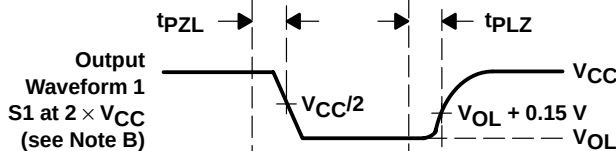
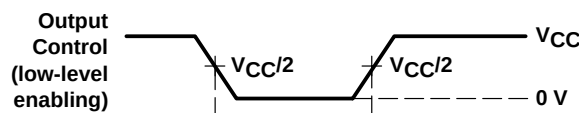
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC827A

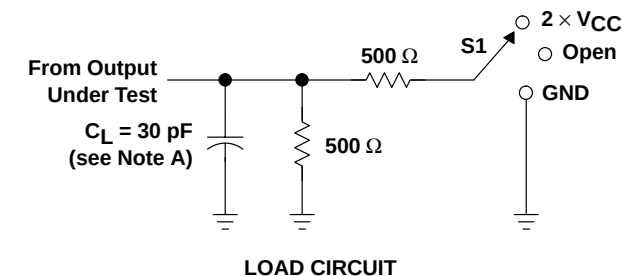
10-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

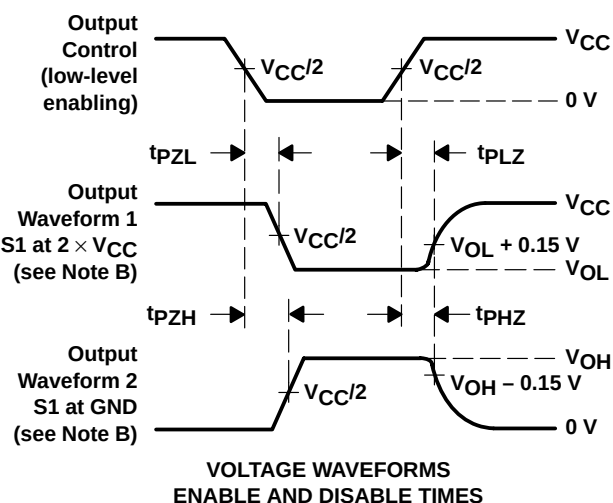
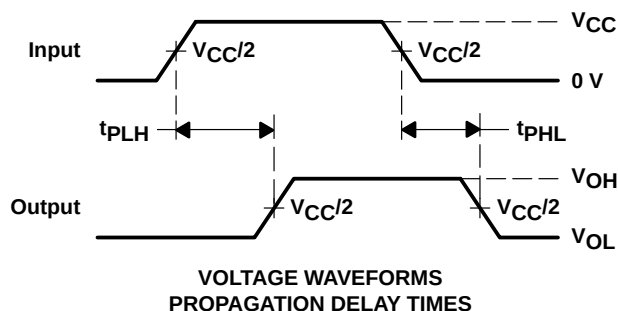
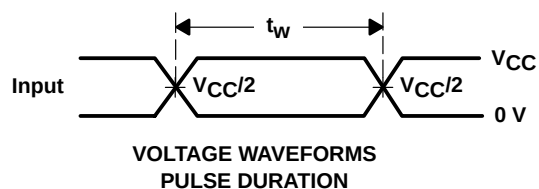
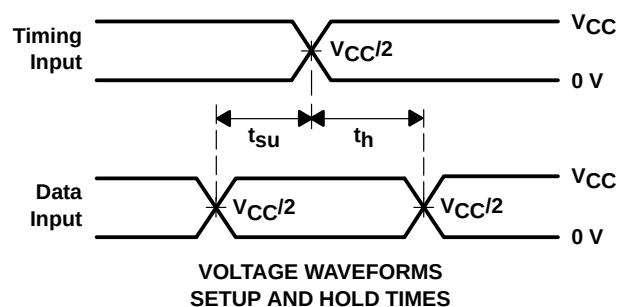
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PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND

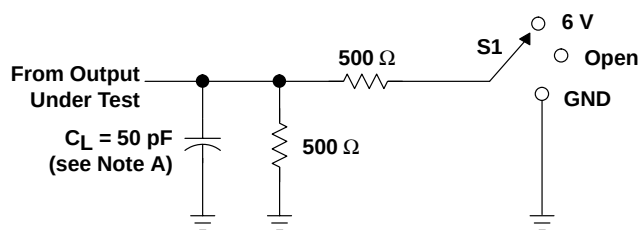


- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

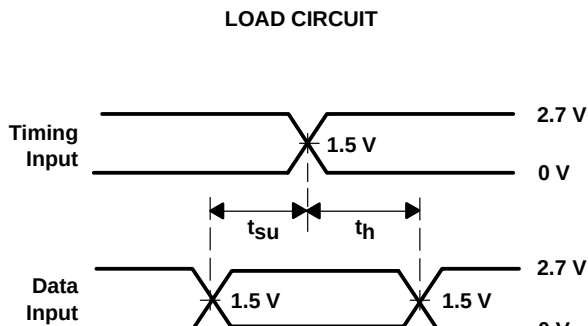
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

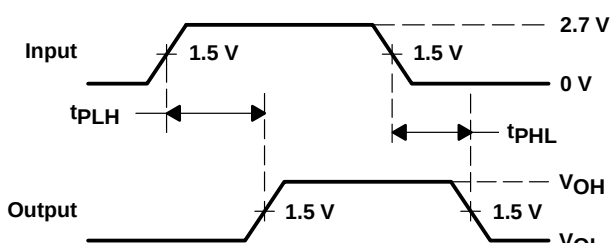


LOAD CIRCUIT

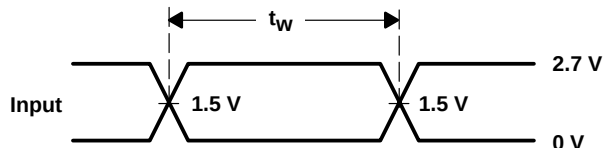
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



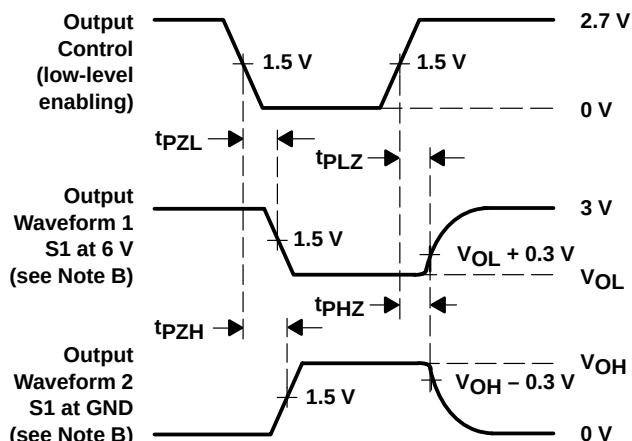
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

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 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

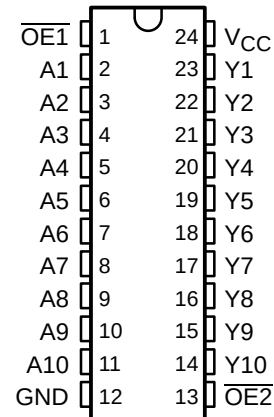
SN74LVC828A

10-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS347E – MARCH 1994 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 10-bit buffer/bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC828A provides a high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all ten outputs are in the high-impedance state. The SN74LVC828A provides inverting data at its outputs.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC828A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

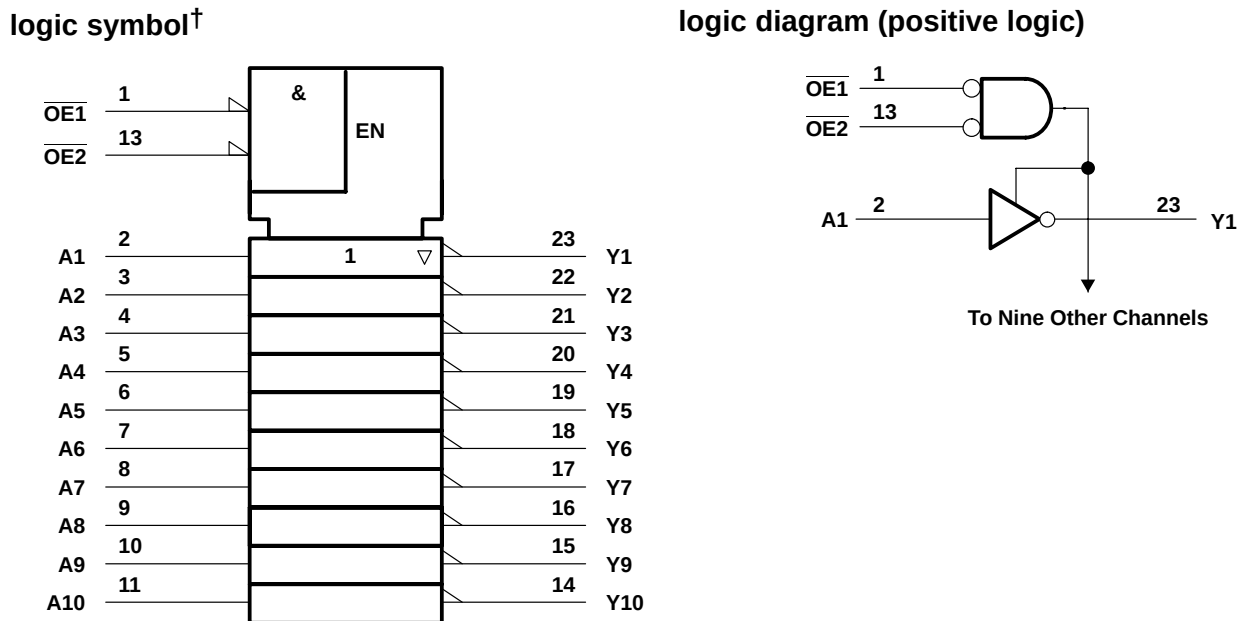
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† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN74LVC828A
10-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCAS347E – MARCH 1994 – REVISED JUNE 1998

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65 3.6	V
		Data retention only	1.5	
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 2.7 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 2.7 V to 3.6 V	0.8	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	High or low state	0 V _{CC}	V
		3 state	0 5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V	–4	mA
		V _{CC} = 2.3 V	–8	
		V _{CC} = 2.7 V	–12	
		V _{CC} = 3 V	–24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4	mA
		V _{CC} = 2.3 V	8	
		V _{CC} = 2.7 V	12	
		V _{CC} = 3 V	24	
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC828A
10-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 4 mA	1.65 V	0.45			
	I _{OL} = 8 mA	2.3 V	0.7			
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 0 to 5.5 V	3.6 V	±5			µA
I _{off}	V _I or V _O = 5.5 V	0	±10			µA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V	±10			µA
I _{CC}	V _I = V _{CC} or GND	3.6 V	10			µA
	3.6 V ≤ V _I ≤ 5.5 V [‡]		10			
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			µA
C _i	V _I = V _{CC} or GND	3.3 V	5			pF
C _o	V _O = V _{CC} or GND	3.3 V	7			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	§	§	§	§	7.1		1	6.7	ns
t _{en}	$\overline{\text{OE}}$	Y	§	§	§	§	8.5		1	7.3	ns
t _{dis}	$\overline{\text{OE}}$	Y	§	§	§	§	7.3		1.8	6.7	ns
t _{sk(o)} [¶]									1		ns

§ This information was not available at the time of publication.

¶ Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

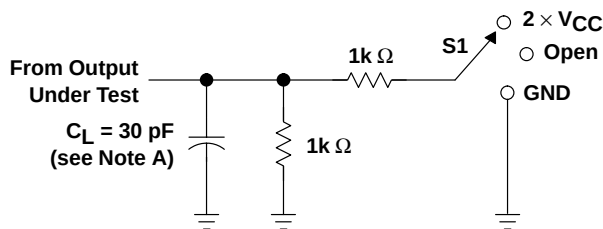
PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	§	§	24	pF
		Outputs disabled		§	§	7	

§ This information was not available at the time of publication.



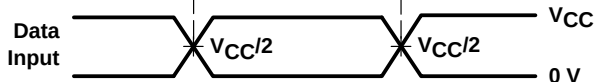
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

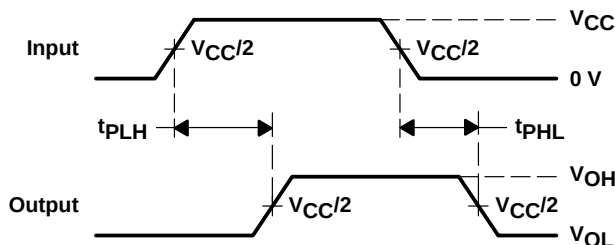


LOAD CIRCUIT

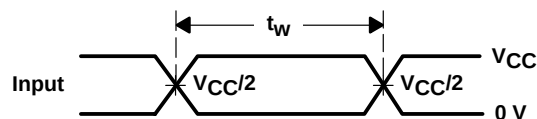
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



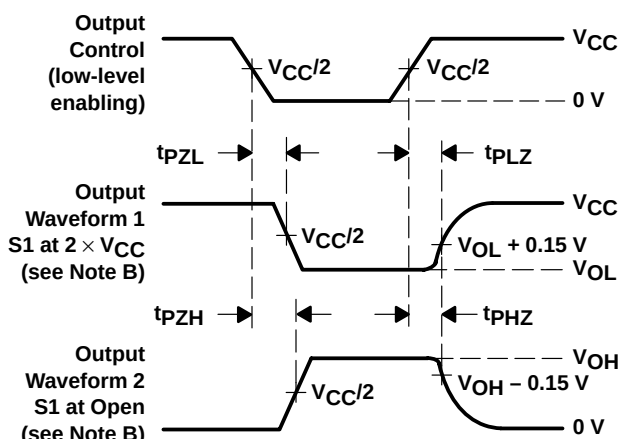
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC828A

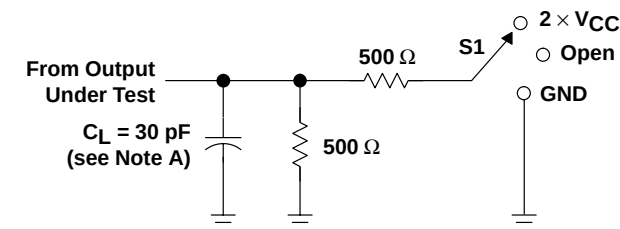
10-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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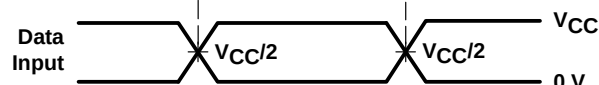
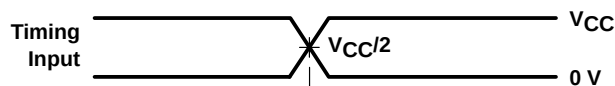
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

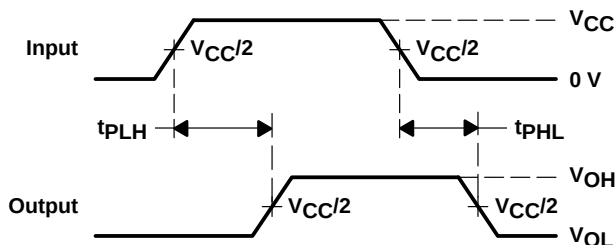


LOAD CIRCUIT

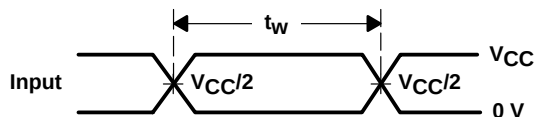
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



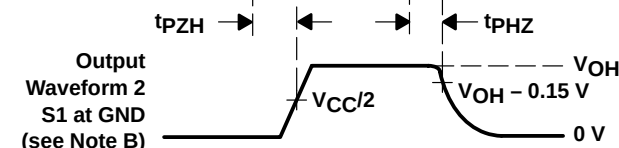
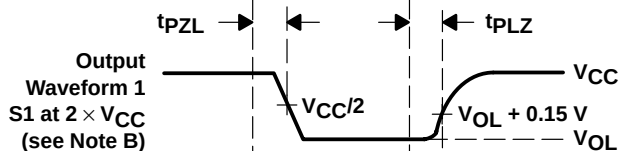
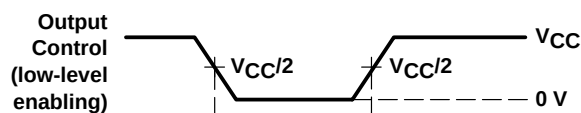
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



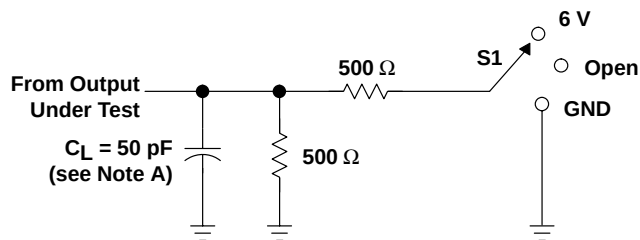
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

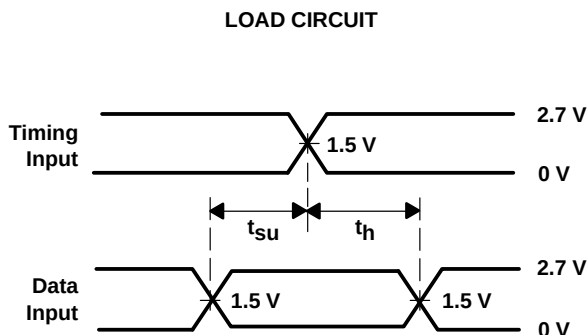
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

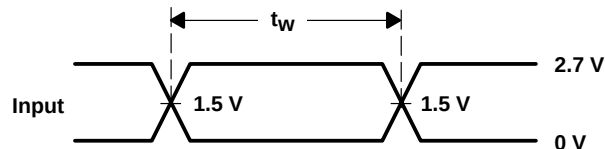


LOAD CIRCUIT

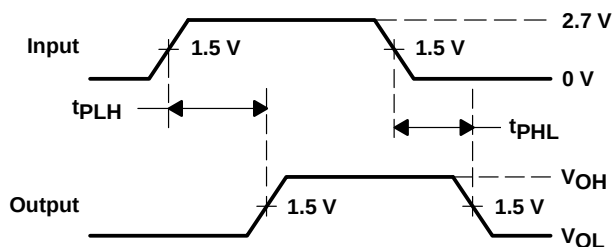
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



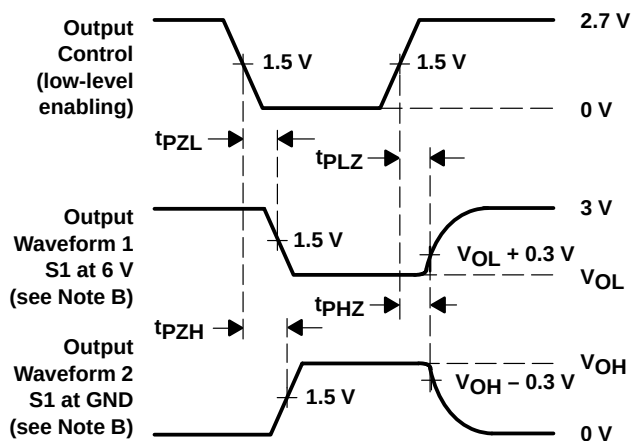
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

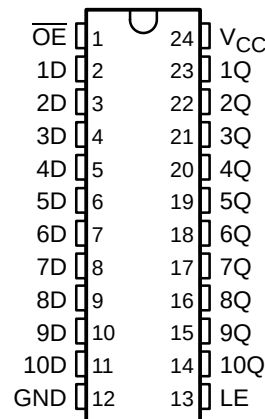
Figure 3. Load Circuit and Voltage Waveforms

SN74LVC841A 10-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS307G – MARCH 1993 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 10-bit bus-interface D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC841A is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC841A is characterized for operation from -40°C to 85°C .

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN74LVC841A

10-BIT BUS-INTERFACE D-TYPE LATCH

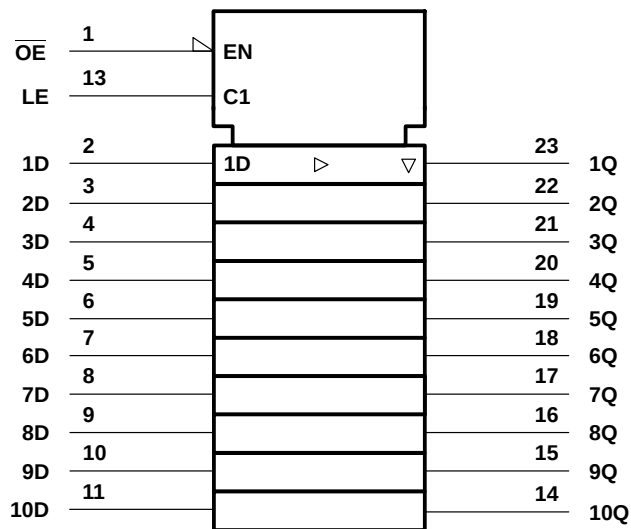
WITH 3-STATE OUTPUTS

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FUNCTION TABLE

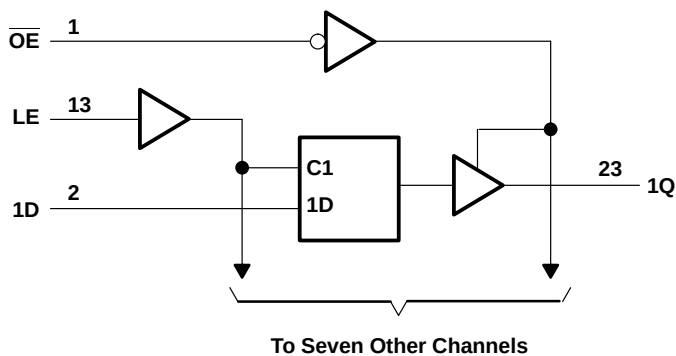
INPUTS			OUTPUT Q
OE	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC841A

10-BIT BUS-INTERFACE D-TYPE LATCH

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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10-BIT BUS-INTERFACE D-TYPE LATCH

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2			
	I _{OH} = –24 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V			0.2	V
	I _{OL} = 4 mA	1.65 V			0.45	
	I _{OL} = 8 mA	2.3 V			0.7	
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _{off}	V _I or V _O = 5.5 V	0			±10	µA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V			±10	µA
I _{CC}	V _I = V _{CC} or GND	3.6 V	I _O = 0		10	µA
	3.6 V ≤ V _I ≤ 5.5 V [‡]				10	
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	V _I = V _{CC} or GND	3.3 V		5		pF
C _o	V _O = V _{CC} or GND	3.3 V		7		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	§		§		3.3		3.3		ns
t _{su}	Setup time, data before LE↓	§		§		2.1		2.1		ns
t _h	Hold time, data after LE↓	§		§		1		1		ns

§ This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.2 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	D	Q	§	§	§	§	7.5		2.4	6.7	ns
	LE		§	§	§	§	8.6		2.7	7.6	
t _{en}	OE	Q	§	§	§	§	8.5		1.3	7.2	ns
t _{dis}	OE	Q	§	§	§	§	6.6		1.9	5.9	ns
t _{sk(o)} [¶]									1		ns

§ This information was not available at the time of publication.

¶ Skew between any two outputs of the same package switching in the same direction



SN74LVC841A
10-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS

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operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per latch	Outputs enabled	$f = 10\text{ MHz}$	†	†	25	pF
	Outputs disabled		†	†	6	

† This information was not available at the time of publication.

SN74LVC841A

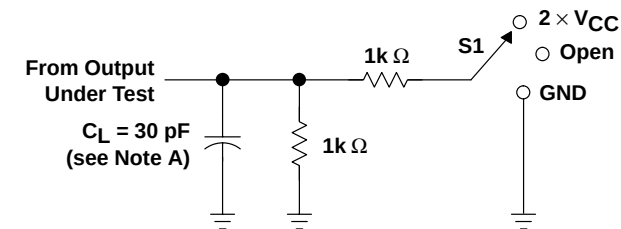
10-BIT BUS-INTERFACE D-TYPE LATCH

WITH 3-STATE OUTPUTS

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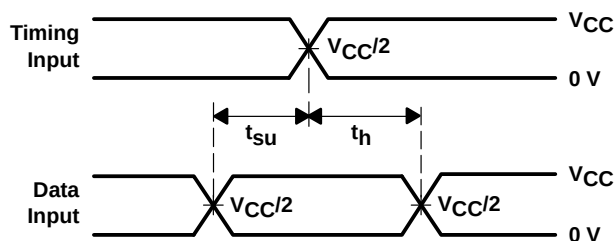
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

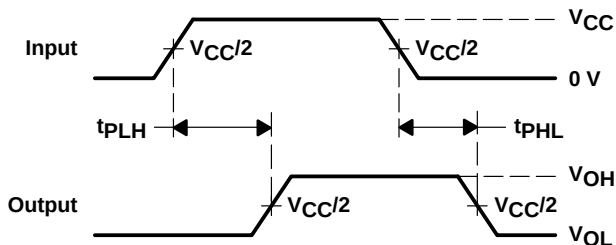


LOAD CIRCUIT

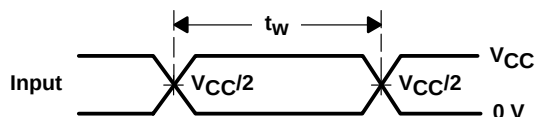
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



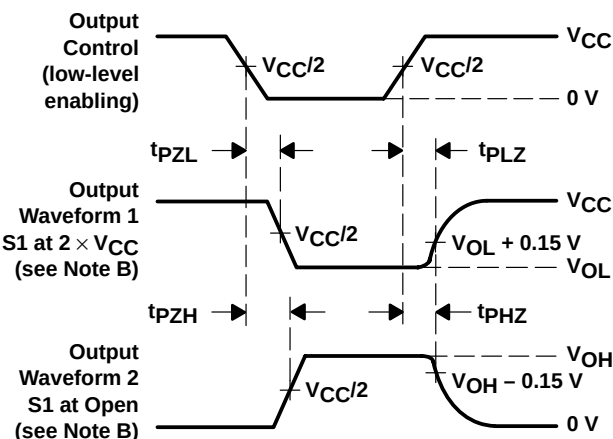
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC841A

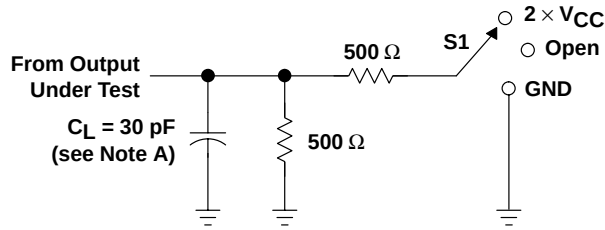
10-BIT BUS-INTERFACE D-TYPE LATCH

WITH 3-STATE OUTPUTS

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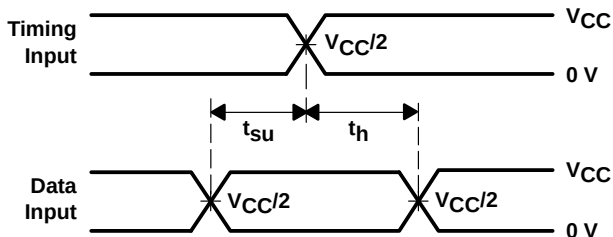
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

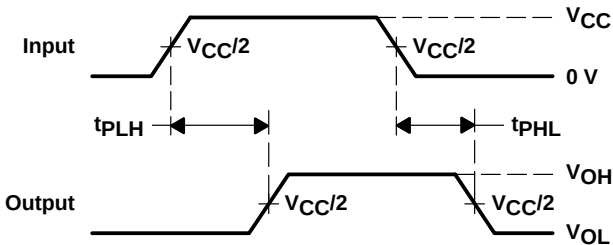


LOAD CIRCUIT

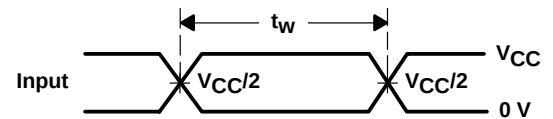
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PHZ}	GND



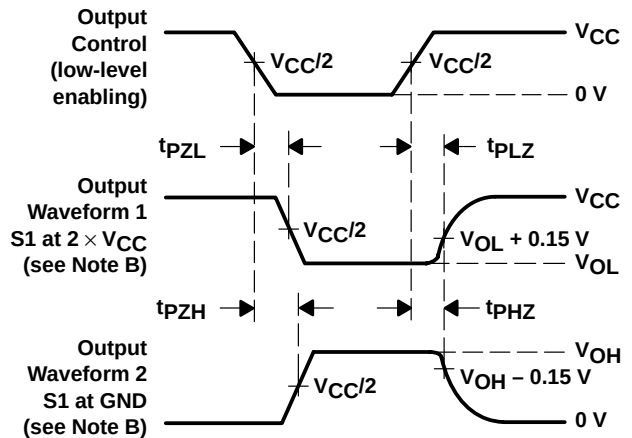
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

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 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN74LVC841A

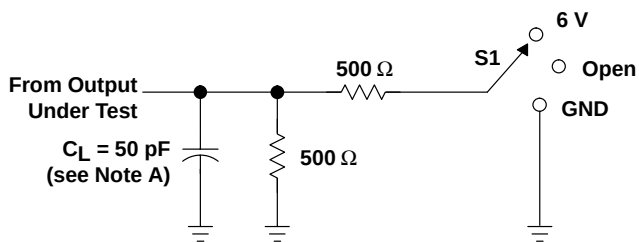
10-BIT BUS-INTERFACE D-TYPE LATCH

WITH 3-STATE OUTPUTS

SCAS307G – MARCH 1993 – REVISED JUNE 1998

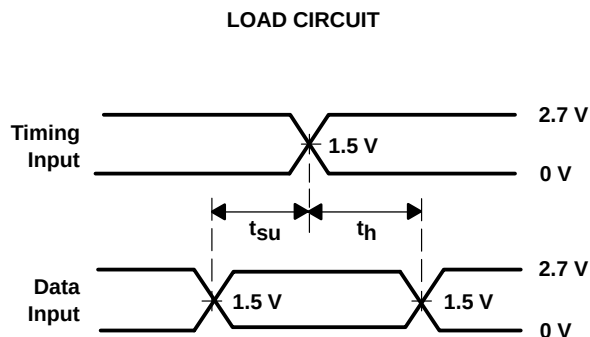
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

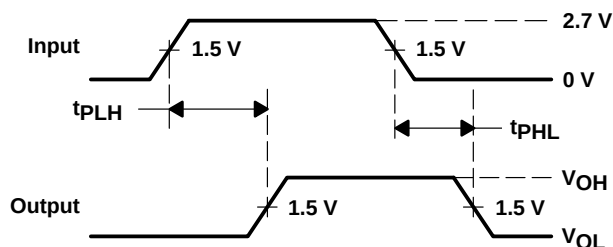


LOAD CIRCUIT

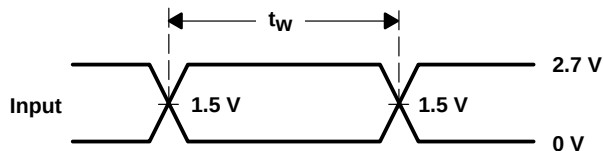
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



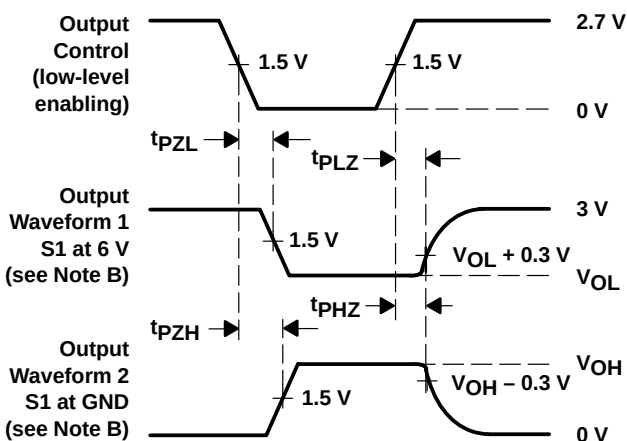
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

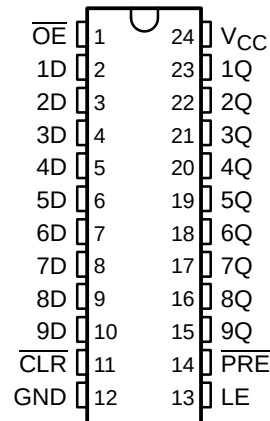
Figure 3. Load Circuit and Voltage Waveforms

SN74LVC843A 9-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 9-bit bus-interface D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC843A is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The nine latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC843A is characterized for operation from -40°C to 85°C .

PRODUCT PREVIEW

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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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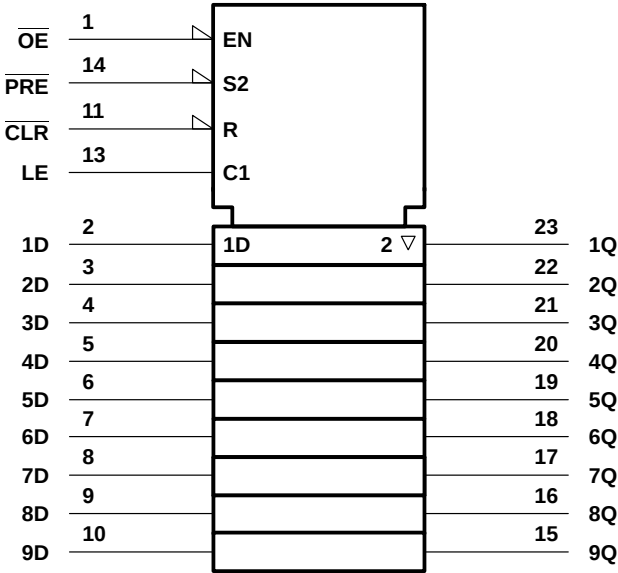
SN74LVC843A
9-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS

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FUNCTION TABLE

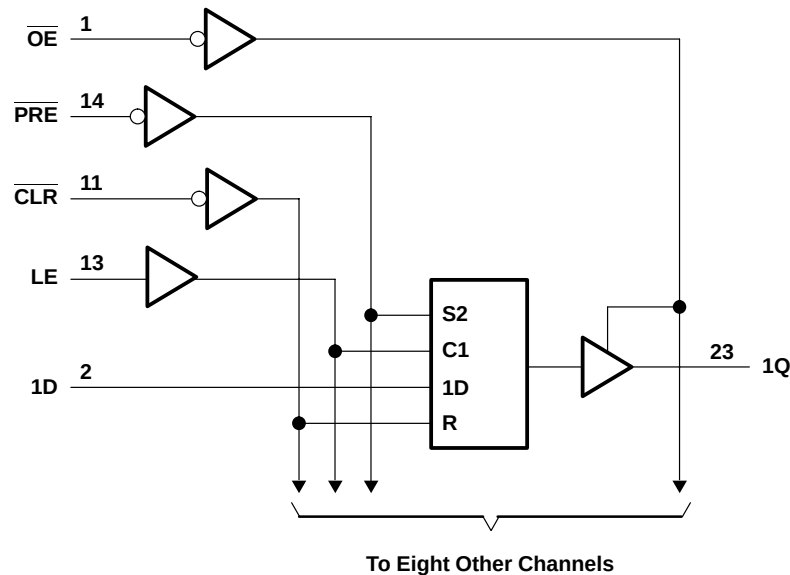
INPUTS					OUTPUT Q
PRE	CLR	OE	LE	D	
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q ₀
X	X	H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

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9-BIT BUS-INTERFACE D-TYPE LATCH

WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65 3.6	V
		Data retention only	1.5	
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 2.7 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 2.7 V to 3.6 V	0.8	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	High or low state	0 V _{CC}	V
		3 state	0 5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V	−4	mA
		V _{CC} = 2.3 V	−8	
		V _{CC} = 2.7 V	−12	
		V _{CC} = 3 V	−24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4	mA
		V _{CC} = 2.3 V	8	
		V _{CC} = 2.7 V	12	
		V _{CC} = 3 V	24	
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 μA		1.65 V to 3.6 V	V _{CC} –0.2			V
	I _{OH} = –4 mA		1.65 V	1.2			
	I _{OH} = –8 mA		2.3 V	1.7			
	I _{OH} = –12 mA		2.7 V	2.2			
			3 V	2.4			
	I _{OH} = –24 mA		3 V	2.2			
V _{OL}	I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	V
	I _{OL} = 4 mA		1.65 V			0.45	
	I _{OL} = 8 mA		2.3 V			0.7	
	I _{OL} = 12 mA		2.7 V			0.4	
	I _{OL} = 24 mA		3 V			0.55	
	I _I	V _I = 0 to 5.5 V		3.6 V			
I _{off}	V _I or V _O = 5.5 V		0			±10	μA
I _{OZ}	V _O = 0 to 5.5 V		3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V			10	μA
	3.6 V ≤ V _I ≤ 5.5 V [‡]					10	
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V			500	μA
C _i	V _I = V _{CC} or GND		3.3 V				pF
C _O	V _O = V _{CC} or GND		3.3 V				pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLR low									ns
		PRE low									
		LE low									
t _{su}	Setup time	Data before LE↓	Low								ns
		PRE inactive									
		CLR inactive									
t _h	Hold time	Data before LE↓	Low								ns
			High								

PRODUCT PREVIEW



SN74LVC843A 9-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

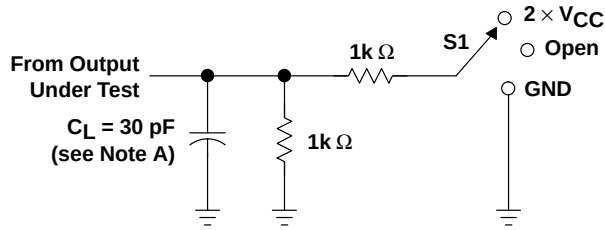
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	D	Q									ns
	LE										
	$\overline{\text{PRE}}$										
	$\overline{\text{CLR}}$										
t _{en}	$\overline{\text{OE}}$	Q									ns
t _{dis}	$\overline{\text{OE}}$	Q									ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per latch	Outputs enabled	f = 10 MHz				pF
		Outputs disabled					

PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

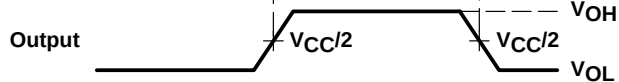


LOAD CIRCUIT

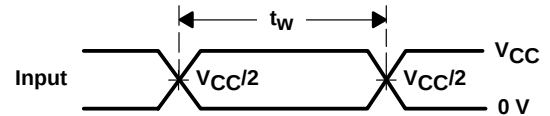
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PHL}	Open



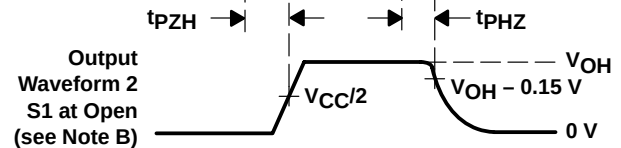
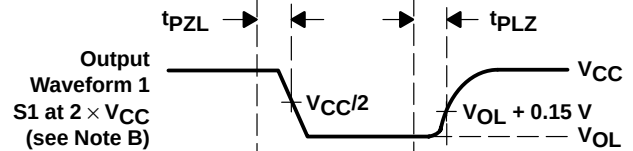
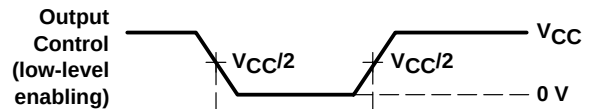
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC843A

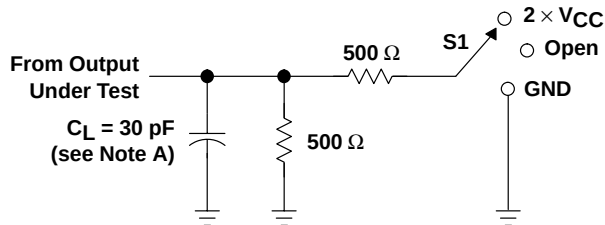
9-BIT BUS-INTERFACE D-TYPE LATCH

WITH 3-STATE OUTPUTS

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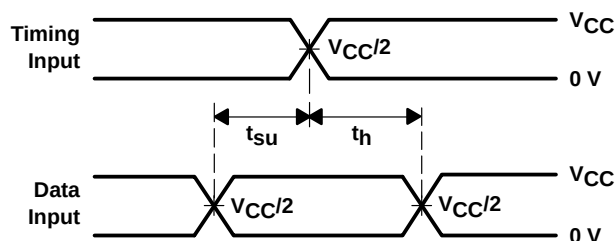
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

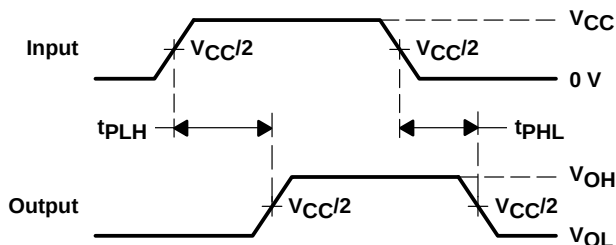


LOAD CIRCUIT

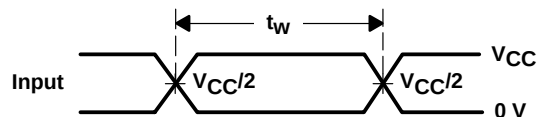
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



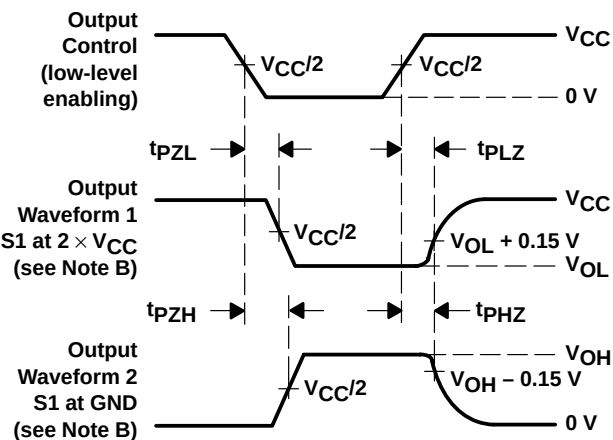
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



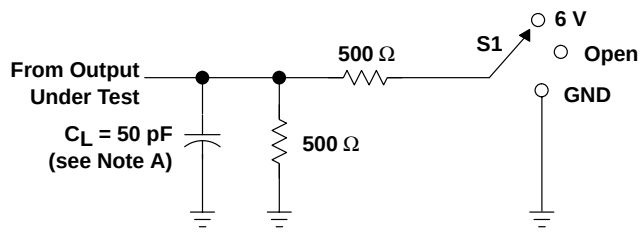
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
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 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

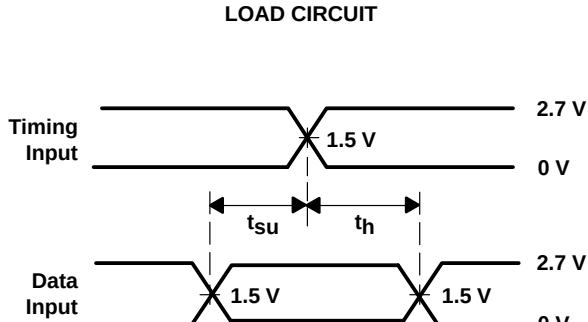
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

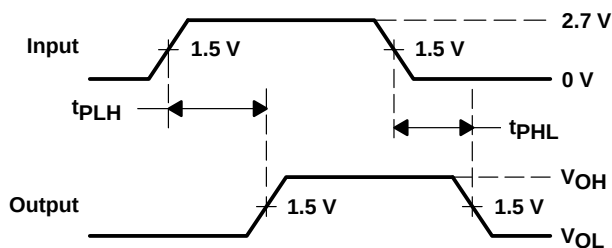


LOAD CIRCUIT

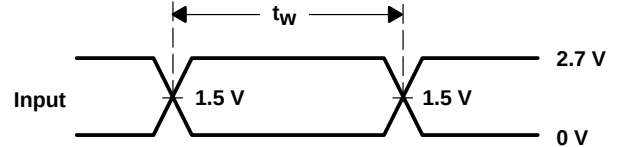
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



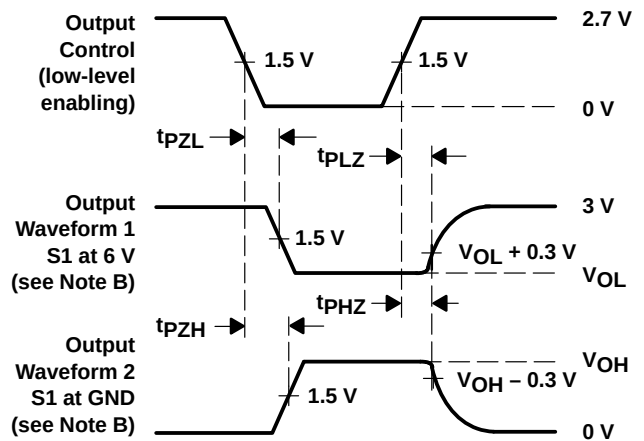
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



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PROPAGATION DELAY TIMES



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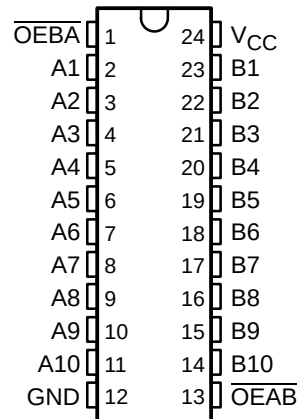
Figure 3. Load Circuit and Voltage Waveforms

SN74LVC861A 10-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS309F – MARCH 1993 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 10-bit bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC861A is designed for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing.

This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic levels at the output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) inputs.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC861A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OEAB}$	$\overline{OEBA}$	
L	H	A data to B bus
H	L	B data to A bus
H	H	Isolation
L	L	Latch A and B (A = B)

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

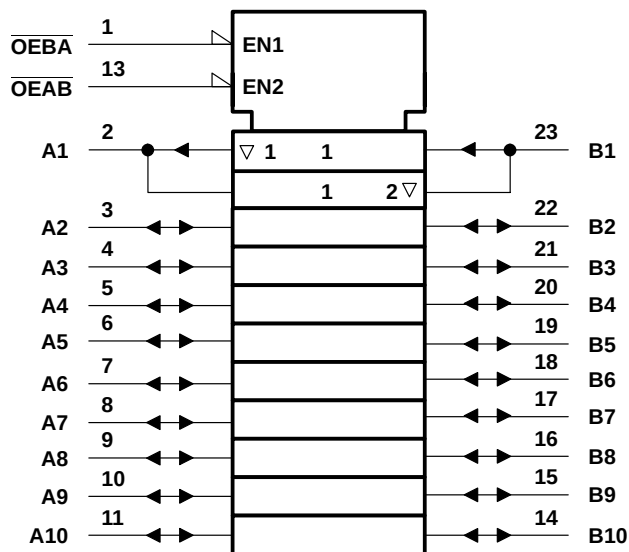


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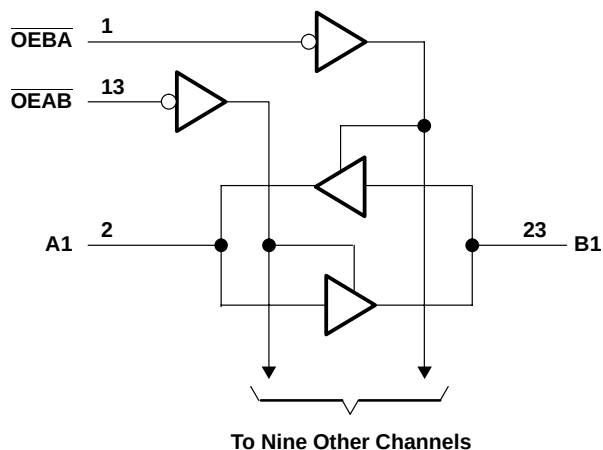
SN74LVC861A
10-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
 SCAS309F – MARCH 1993 – REVISED JUNE 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC861A
10-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I : (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74LVC861A
10-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT	
V _{OH}		I _{OH} = –100 μA	1.65 V to 3.6 V	V _{CC} –0.2			V	
		I _{OH} = –4 mA	1.65 V	1.2				
		I _{OH} = –8 mA	2.3 V	1.7				
		I _{OH} = –12 mA	2.7 V	2.2				
			3 V	2.4				
		I _{OH} = –24 mA	3 V	2.2				
V _{OL}		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V	
		I _{OL} = 4 mA	1.65 V			0.45		
		I _{OL} = 8 mA	2.3 V			0.7		
		I _{OL} = 12 mA	2.7 V			0.4		
		I _{OL} = 24 mA	3 V			0.55		
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V			±5	μA	
I _{off}		V _I or V _O = 5.5 V	0			±10	μA	
I _{OZ} [‡]		V _O = 0 to 5.5 V		3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND		3.6 V			10	μA	
	3.6 V ≤ V _I ≤ 5.5 V [§]					10		
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V		500	μA	
C _i	Control inputs	V _I = V _{CC} or GND		3.3 V		5	pF	
C _{io}	A or B ports	V _O = V _{CC} or GND		3.3 V		7	pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	¶	¶	¶	¶	6.8		1.3	6.4	ns
t _{en}	OEAB or OEBA	A or B	¶	¶	¶	¶	8.2		1	7	ns
t _{dis}	OEAB or OEBA	A or B	¶	¶	¶	¶	6.6		1.7	5.9	ns
t _{sk(o)} [#]									1		ns

¶ This information was not available at the time of publication.

[#] Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

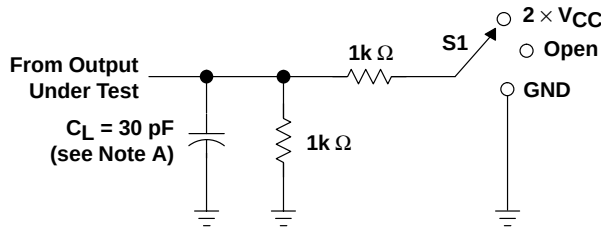
PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	f = 10 MHz	¶	¶	29	pF
		Outputs disabled		¶	¶	5	

¶ This information was not available at the time of publication.



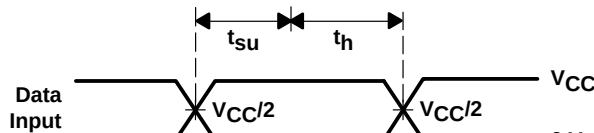
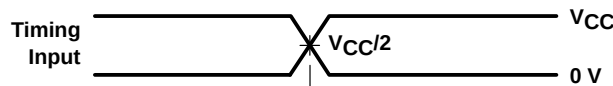
PARAMETER MEASUREMENT INFORMATION

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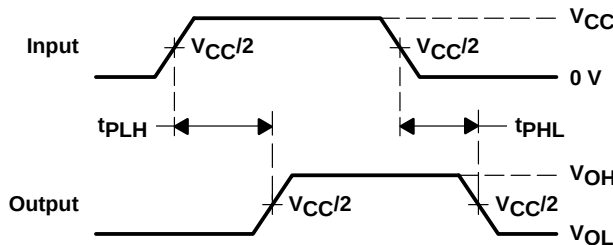


LOAD CIRCUIT

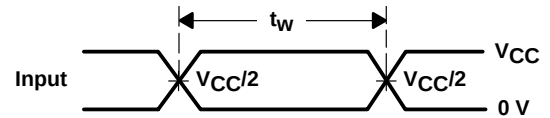
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



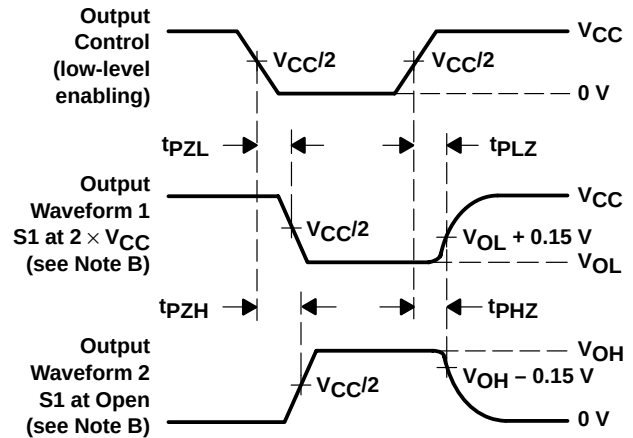
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
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 - The outputs are measured one at a time with one transition per measurement.
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Figure 1. Load Circuit and Voltage Waveforms

SN74LVC861A

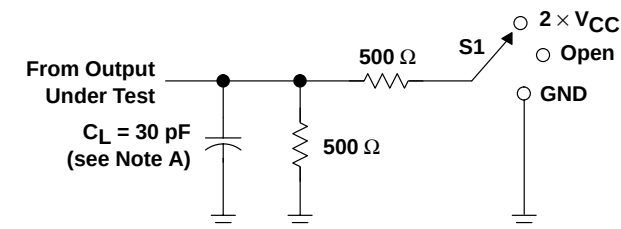
10-BIT BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

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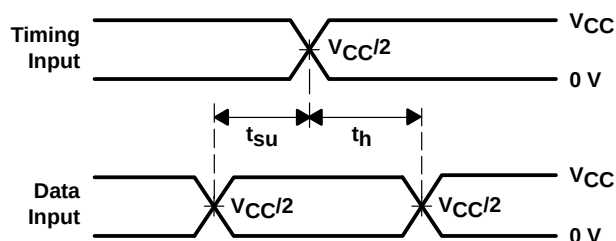
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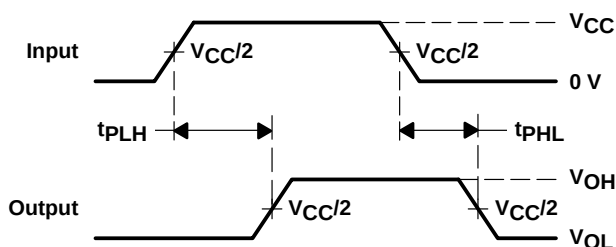


LOAD CIRCUIT

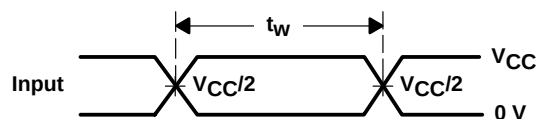
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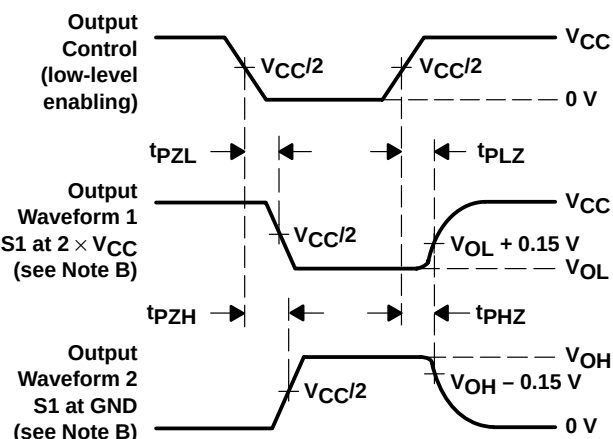
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



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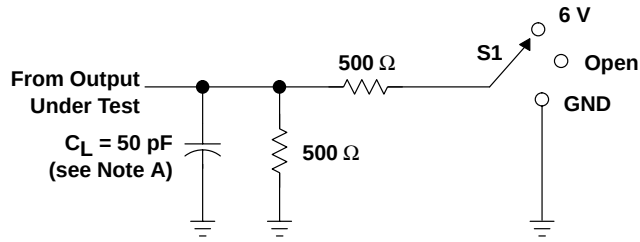
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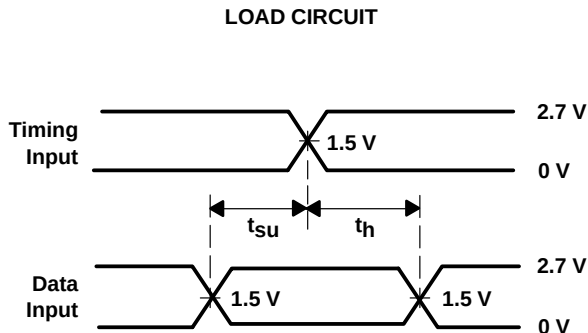
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$

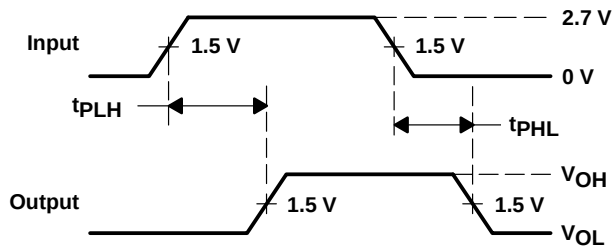


LOAD CIRCUIT

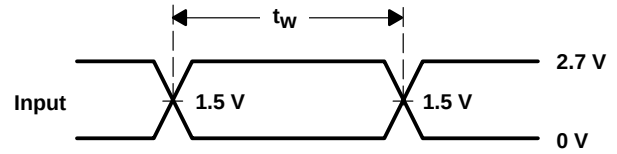
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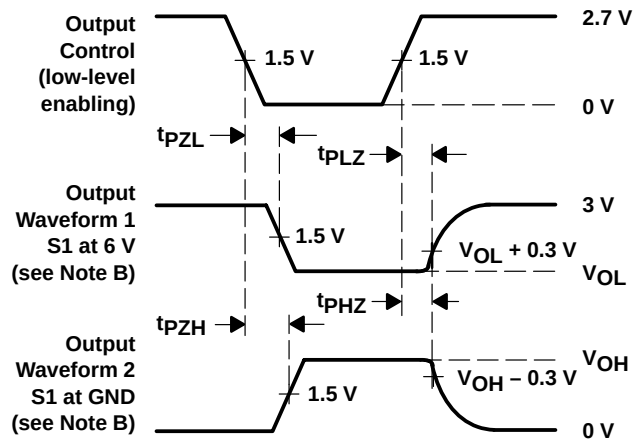
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SETUP AND HOLD TIMES



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PROPAGATION DELAY TIMES



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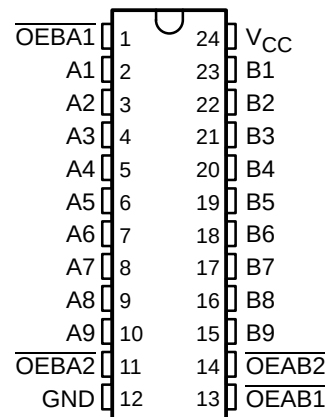
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SCAS310G – MARCH 1993 – REVISED JUNE 1998

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(TOP VIEW)



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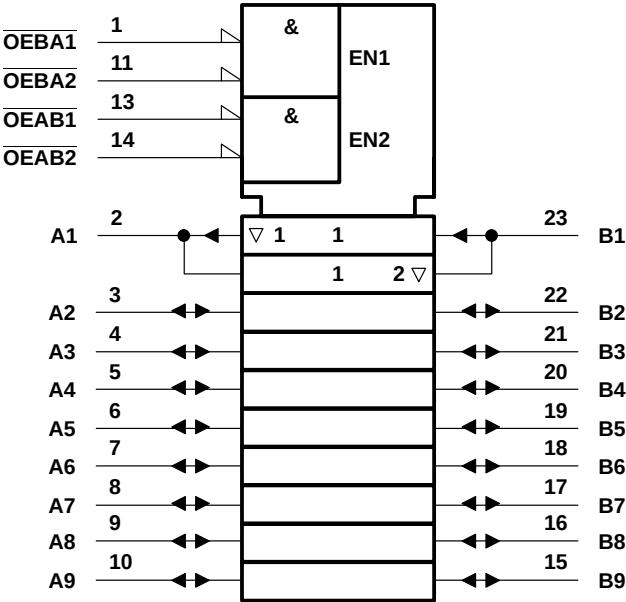
SN74LVC863A
9-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

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FUNCTION TABLE

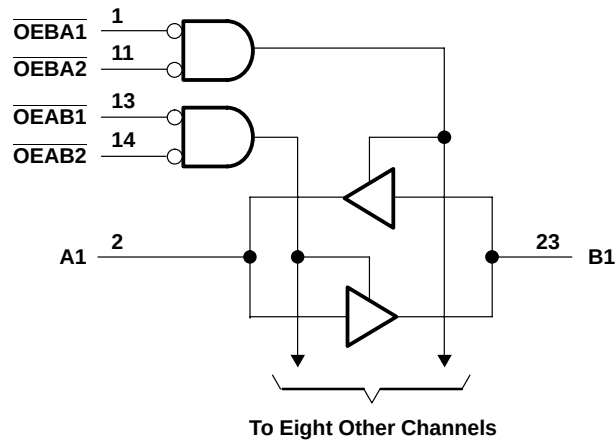
INPUTS				OPERATION
OEAB1	OEAB2	OEBA1	OEBA2	
L	L	L	L	Latch A and B
L	L	H	X	A to B
L	L	X	H	
H	X	L	L	B to A
X	H	L	L	
H	X	H	X	Isolation
H	X	X	H	
X	H	X	H	
X	H	H	X	

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I : (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	High or low state	0	V _{CC}	V
		3 state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V	−4		mA
		V _{CC} = 2.3 V	−8		
		V _{CC} = 2.7 V	−12		
		V _{CC} = 3 V	−24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		mA
		V _{CC} = 2.3 V	8		
		V _{CC} = 2.7 V	12		
		V _{CC} = 3 V	24		
Δt/Δv	Input transition rise or fall rate	0	10	ns/V	
T _A	Operating free-air temperature	−40	85	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}		I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
		I _{OH} = –4 mA	1.65 V	1.2			
		I _{OH} = –8 mA	2.3 V	1.7			
		I _{OH} = –12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = –24 mA	3 V	2.2			
V _{OL}		I _{OL} = 100 µA	1.65 V to 3.6 V			0.2	V
		I _{OL} = 4 mA	1.65 V			0.45	
		I _{OL} = 8 mA	2.3 V			0.7	
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _{off}		V _I or V _O = 5.5 V	0			±10	µA
I _{OZ} [‡]		V _O = 0 to 5.5 V	3.6 V			±10	µA
I _{CC}		V _I = V _{CC} or GND	3.6 V			10	µA
		3.6 V ≤ V _I ≤ 5.5 V [§]				10	
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V			5	pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V			7	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	¶	¶	¶	¶	6.8		1.7	6.1	ns
t _{en}	OEAB or OEBA	A or B	¶	¶	¶	¶	8.3		1.2	7.2	ns
t _{dis}	OEAB or OEBA	A or B	¶	¶	¶	¶	7		2	6.3	ns

¶ This information was not available at the time of publication.

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	f = 10 MHz	¶	¶	27	pF
		Outputs disabled		¶	¶	5	

¶ This information was not available at the time of publication.



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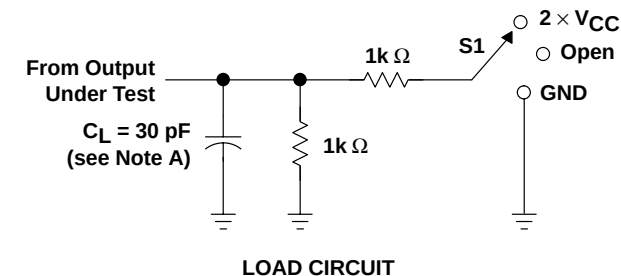
9-BIT BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

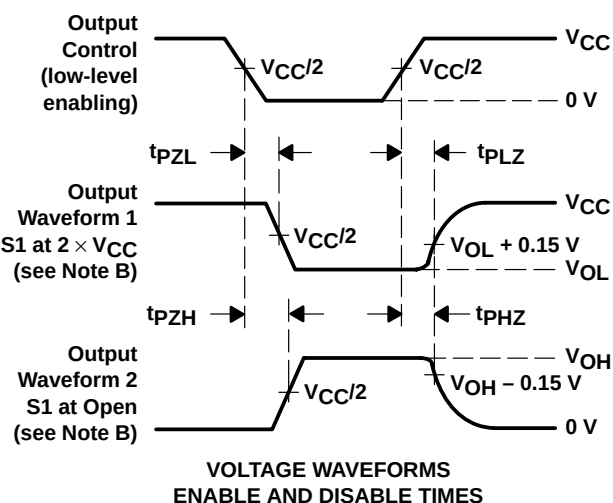
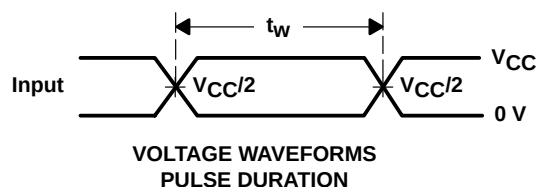
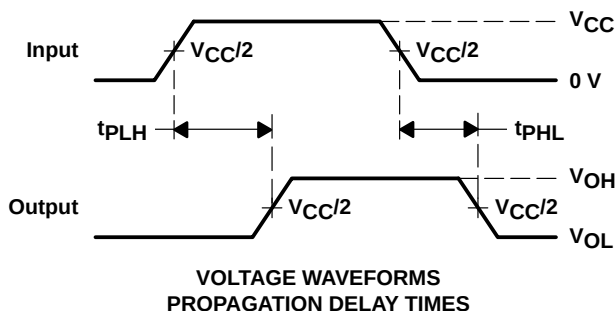
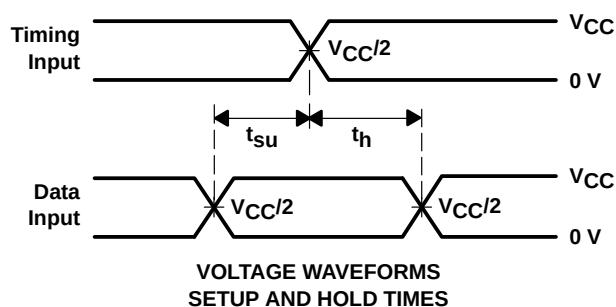
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PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open

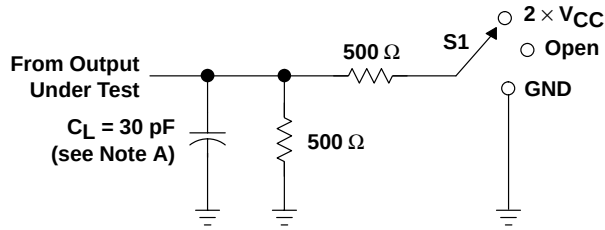


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

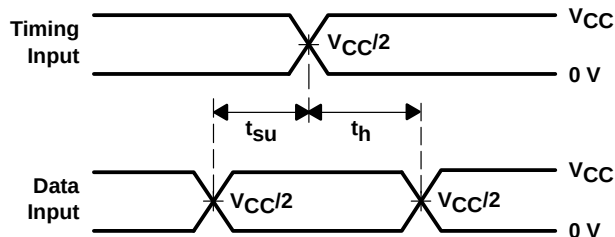
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

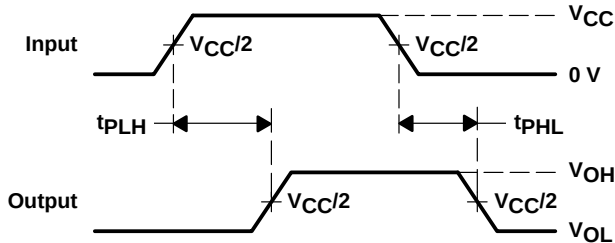


LOAD CIRCUIT

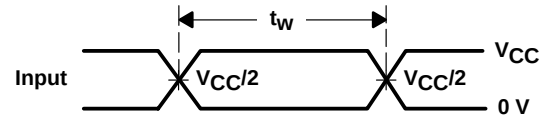
TEST	S1
t_{pd}	Open
t_{pLZ}/t_{pZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PHZ}	GND



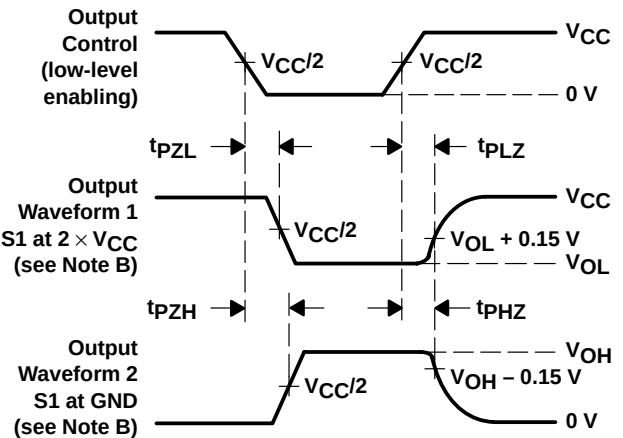
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{pLZ} and t_{pHZ} are the same as t_{dis} .
 - t_{pZL} and t_{pZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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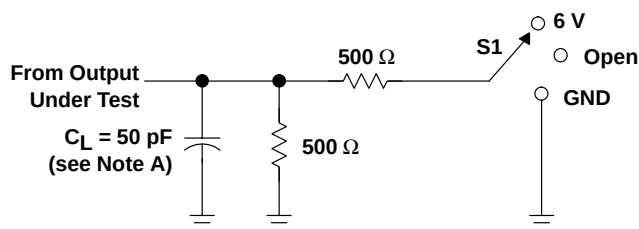
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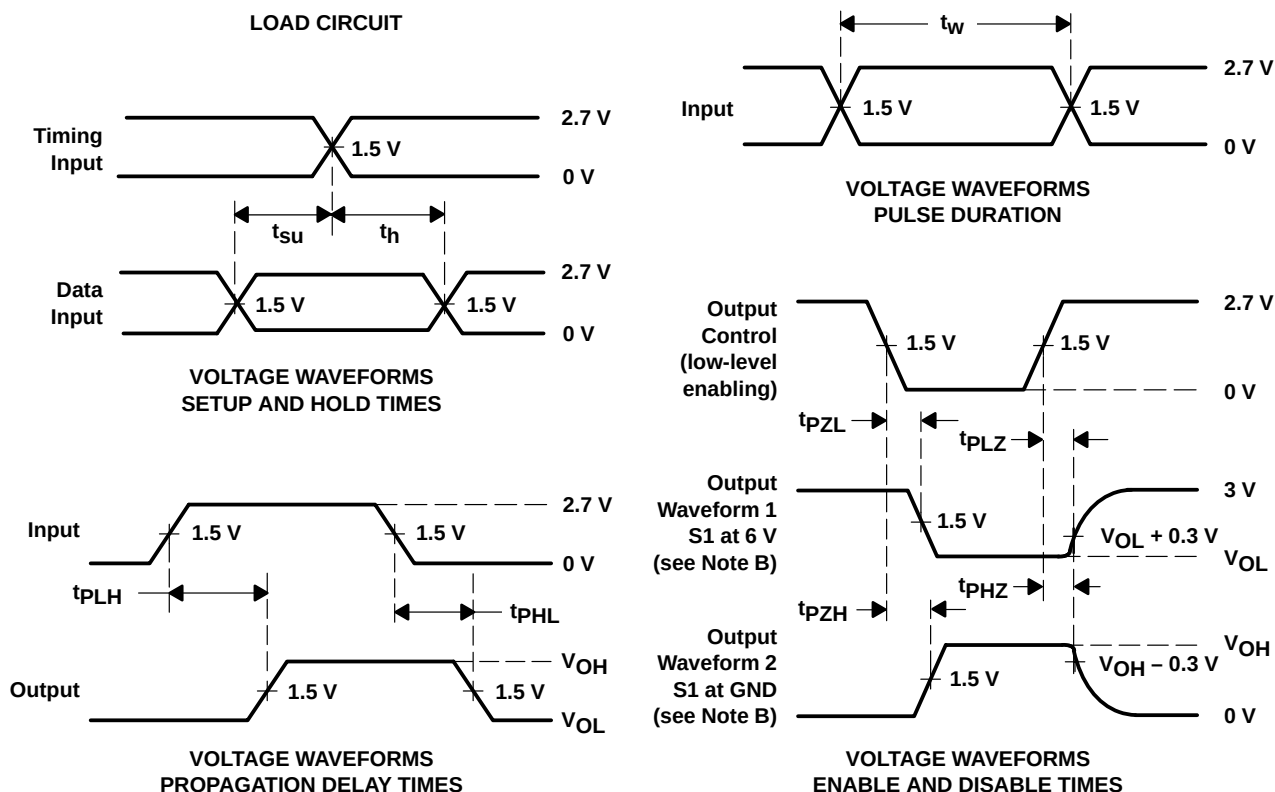
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

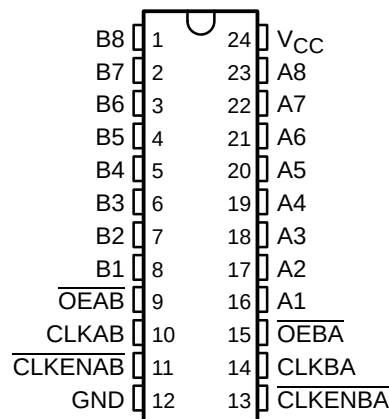
Figure 3. Load Circuit and Voltage Waveforms

SN74LVC2952A OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver and register is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC2952A consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input, provided that the clock-enable ($\overline{CLKENAB}$ or $\overline{CLKENBA}$) input is low. Taking the output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) input low accesses the data on either port.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC2952A is characterized for operation from -40°C to 85°C .

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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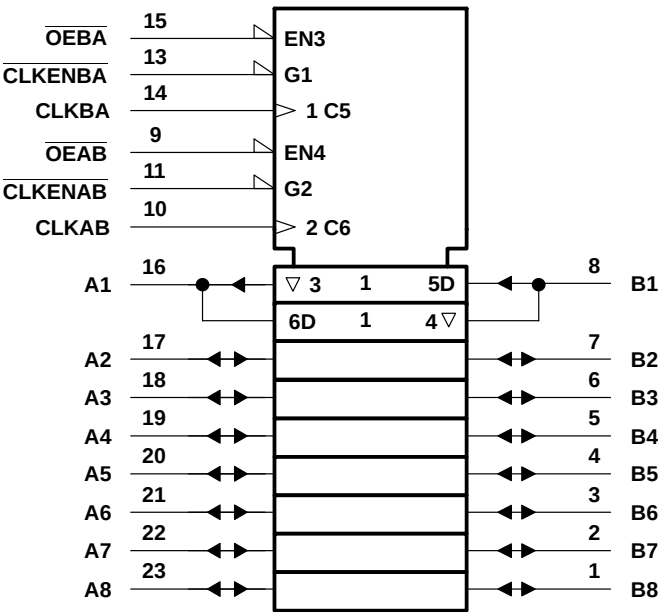
FUNCTION TABLE†

INPUTS				OUTPUT B
CLKENAB	CLKAB	OEAB	A	
H	X	L	X	B ₀ ‡
X	H or L	L	X	B ₀ ‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar, but uses CLKENBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established

logic symbol§

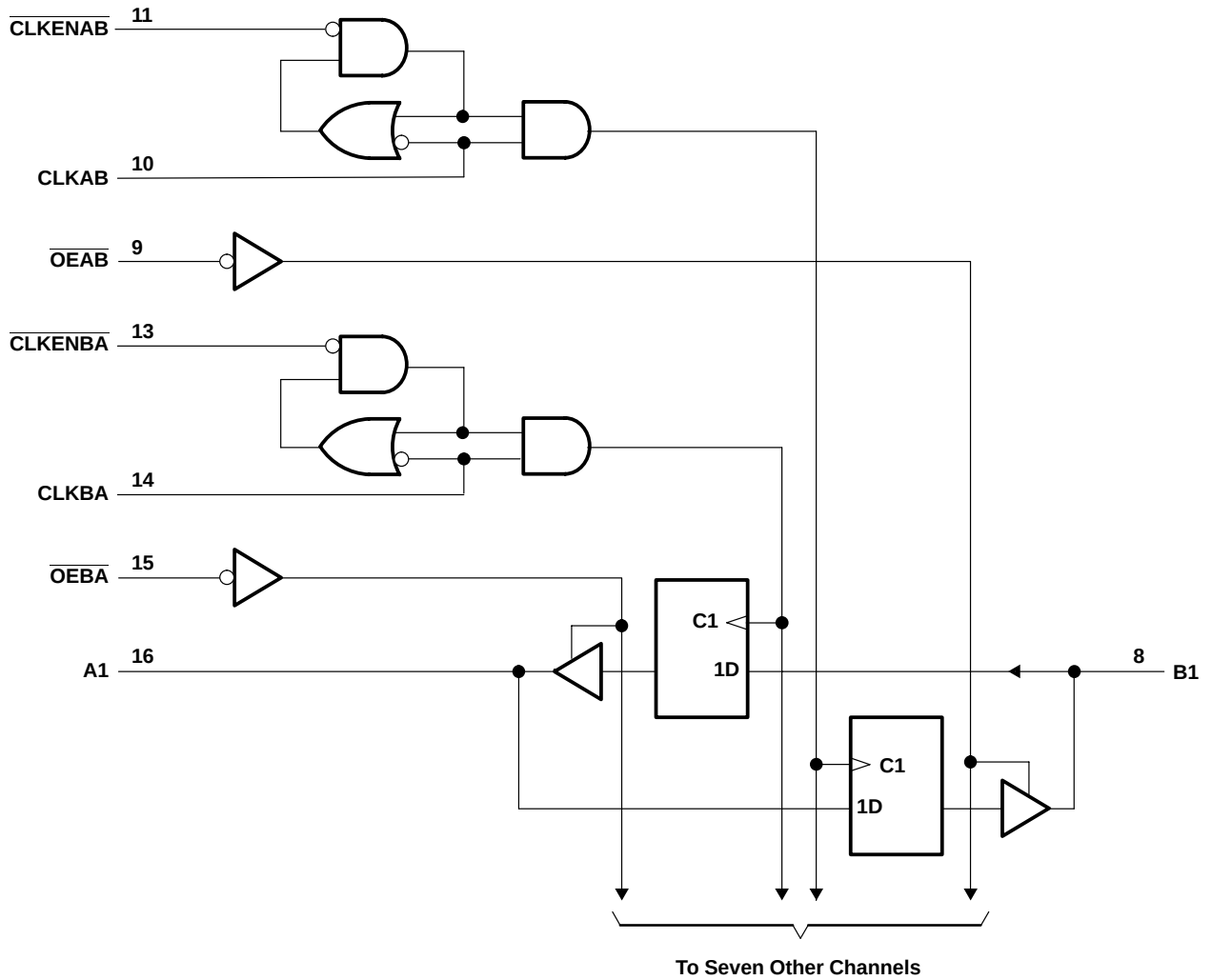


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I : (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}		I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
		I _{OH} = –4 mA	1.65 V	1.2			
		I _{OH} = –8 mA	2.3 V	1.7			
		I _{OH} = –12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = –24 mA	3 V	2.2			
V _{OL}		I _{OL} = 100 µA	1.65 V to 3.6 V			0.2	V
		I _{OL} = 4 mA	1.65 V			0.45	
		I _{OL} = 8 mA	2.3 V			0.7	
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _{off}		V _I or V _O = 5.5 V	0			±10	µA
I _{OZ} [‡]		V _O = 0 to 5.5 V	3.6 V			±10	µA
I _{CC}		V _I = V _{CC} or GND	3.6 V			10	µA
		3.6 V ≤ V _I ≤ 5.5 V [§]				10	
I _{CC}		I _O = 0					
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V			5	pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V			8.5	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		¶		¶		150		150		MHz
t _w	Pulse duration, CLK high or low		¶		¶		3.3		3.3		ns
t _{su}	Setup time	Data before CLK high	¶		¶		1.7		1.3		ns
		CLKEN before CLK high	¶		¶		1.3		1.1		
t _h	Hold time	Data after CLK high	¶		¶		1.8		1.1		ns
		CLKEN after CLK high	¶		¶		1.4		1.1		

¶ This information was not available at the time of publication.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			†		†		150		150		MHz
t_{pd}	CLKAB or CLKBA	B or A	†	†	†	†	8.8		1	8.2	ns
t_{en}	$\overline{OE}$	A or B	†	†	†	†	9		1	7.8	ns
t_{dis}	$\overline{OE}$	A or B	†	†	†	†	8.8		1	7.8	ns
$t_{sk(o)}^{\ddagger}$									1		ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$f = 10\text{ MHz}$	†	†	79	pF
		Outputs disabled		†	†	41	

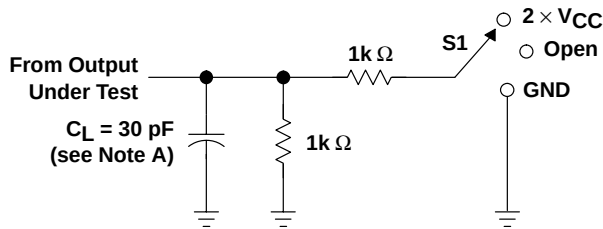
† This information was not available at the time of publication.



SN74LVC2952A OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

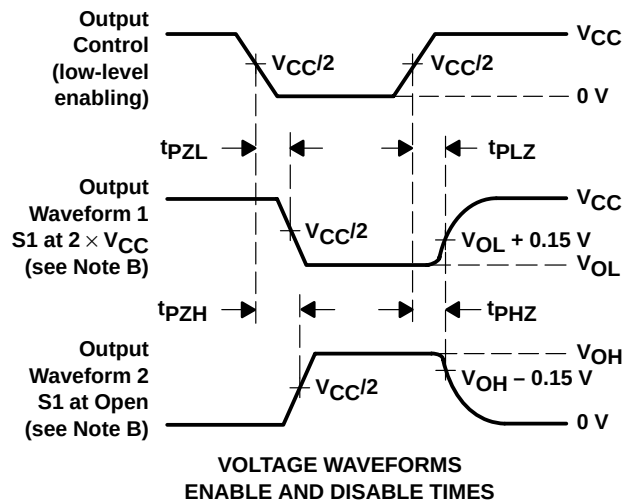
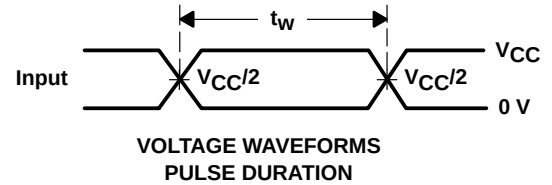
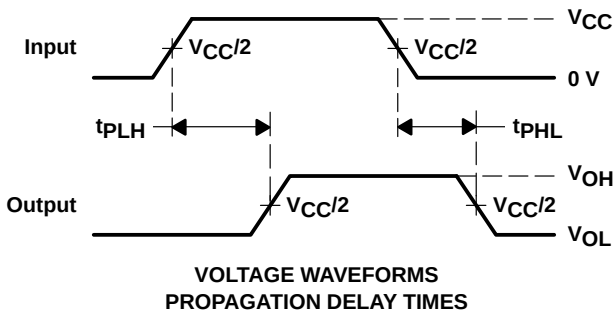
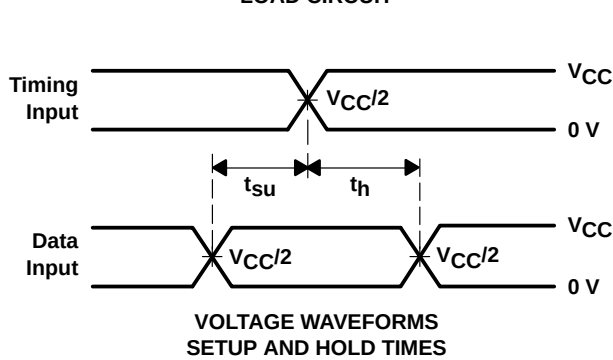
SCAS311F – JANUARY 1993 – REVISED JUNE 1998

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC2952A

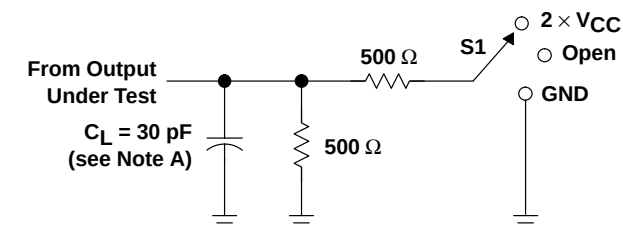
OCTAL BUS TRANSCEIVER AND REGISTER

WITH 3-STATE OUTPUTS

SCAS311F – JANUARY 1993 – REVISED JUNE 1998

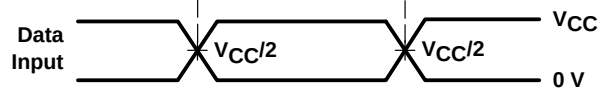
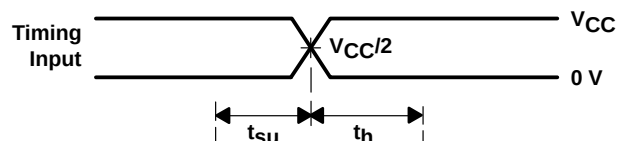
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

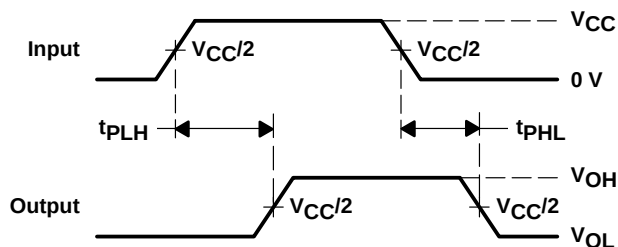


LOAD CIRCUIT

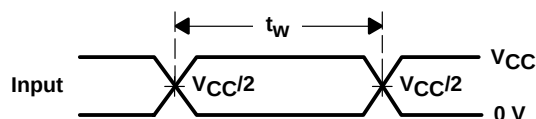
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



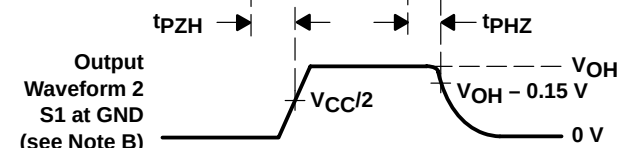
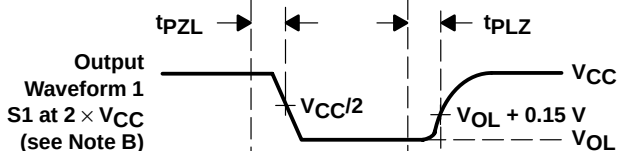
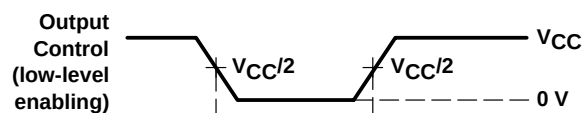
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

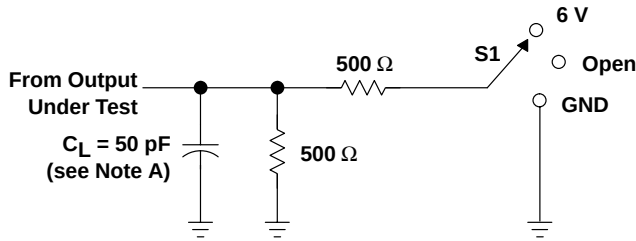


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

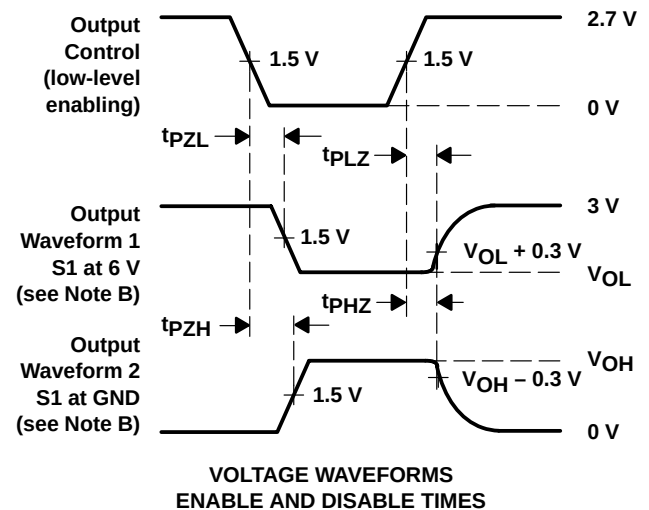
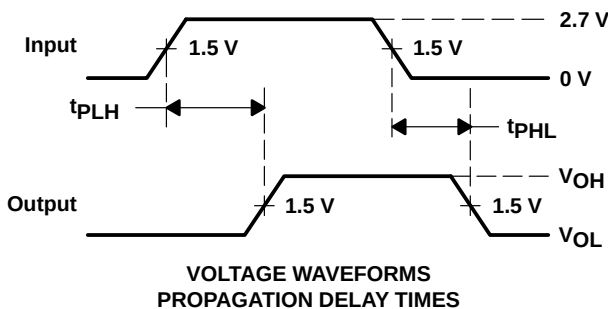
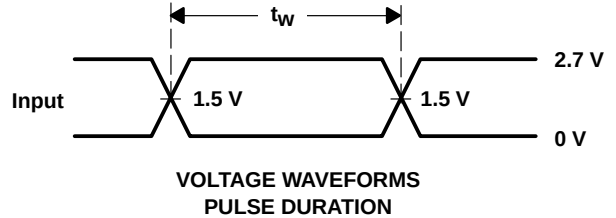
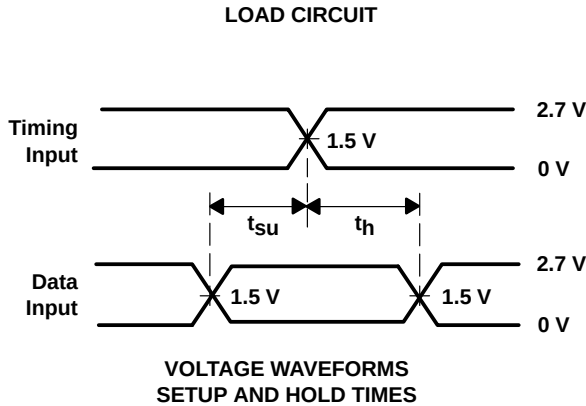
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

General Information	1
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LVC Octals	3
LVC Widebus™	4
LVC 3.3-V to 5-V Translators and Cable Drivers	5
LV Gates and MSI	6
LV Octals	7
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Mechanical Data	9

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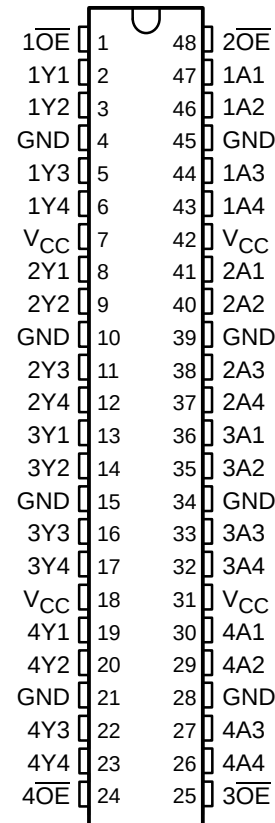
SN74LVCH16240A

16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

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- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH16240A is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH16240A is characterized for operation from -40°C to 85°C .

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



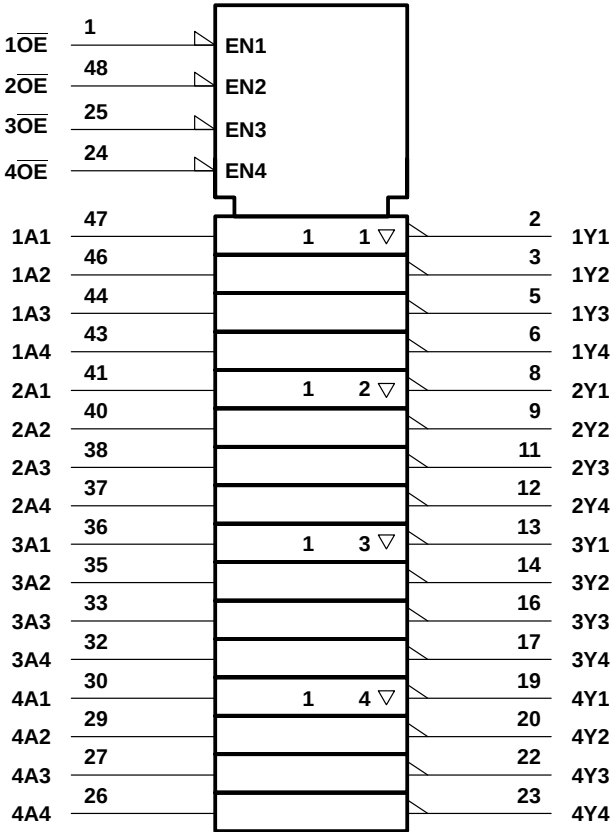
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FUNCTION TABLE
(each 4-bit buffer)

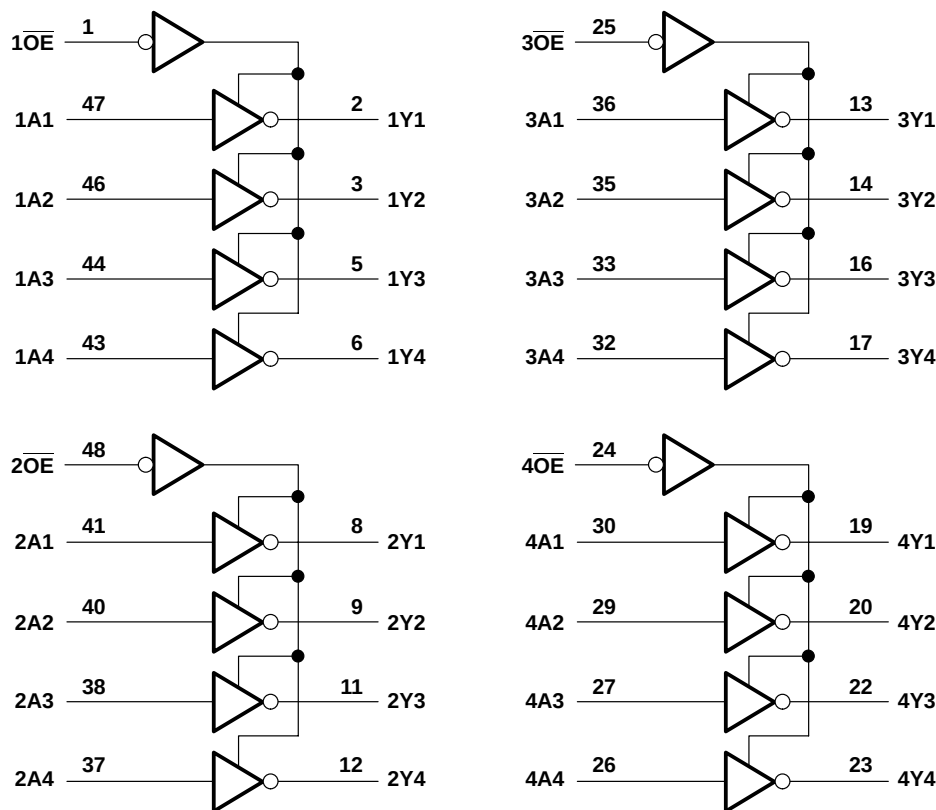
INPUTS		OUTPUT Y
OE	A	
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN74LVCH16240A
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65 3.6	V
		Data retention only	1.5	
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 2.7 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 2.7 V to 3.6 V	0.8	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	High or low state	0 V _{CC}	V
		3 state	0 5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V	−4	mA
		V _{CC} = 2.3 V	−8	
		V _{CC} = 2.7 V	−12	
		V _{CC} = 3 V	−24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4	mA
		V _{CC} = 2.3 V	8	
		V _{CC} = 2.7 V	12	
		V _{CC} = 3 V	24	
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVCH16240A
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} – 0.2			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 4 mA	1.65 V	0.45			
	I _{OL} = 8 mA	2.3 V	0.7			
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _I (hold)	V _I = 0.58 V	1.65 V	‡			µA
	V _I = 1.07 V		‡			
	V _I = 0.7 V	2.3 V	45			
	V _I = 1.7 V		–45			
	V _I = 0.8 V	3 V	75			
	V _I = 2 V		–75			
	V _I = 0 to 3.6 V [§]	3.6 V			±500	
I _{off}	V _I or V _O = 5.5 V	0			±10	µA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V			±10	µA
I _{CC}	V _I = V _{CC} or GND	3.6 V			20	µA
	3.6 V ≤ V _I ≤ 5.5 V [¶]				20	
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	V _I = V _{CC} or GND	3.3 V			5	pF
C _O	V _O = V _{CC} or GND	3.3 V			6	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This information was not available at the time of publication.

[§] This is the bus-hold maximum dynamic current required to switch the input from one state to another.

[¶] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	‡	‡	‡	‡	5		1	4.2	ns
t _{en}	$\overline{\text{OE}}$	Y	‡	‡	‡	‡	5.8		1.5	4.7	ns
t _{dis}	$\overline{\text{OE}}$	Y	‡	‡	‡	‡	6.6		1.5	5.9	ns

[‡] This information was not available at the time of publication.



SN74LVCH16240A
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

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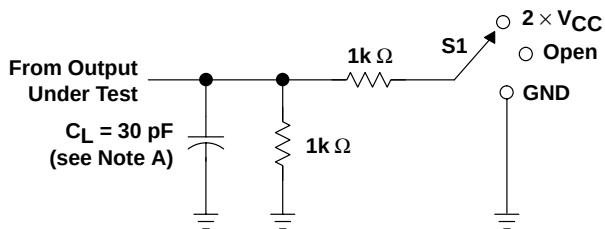
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	$f = 10\text{ MHz}$	†	†	34	pF
	Outputs disabled		†	†	3	

† This information was not available at the time of publication.

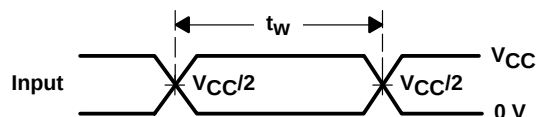
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

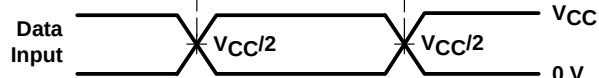


LOAD CIRCUIT

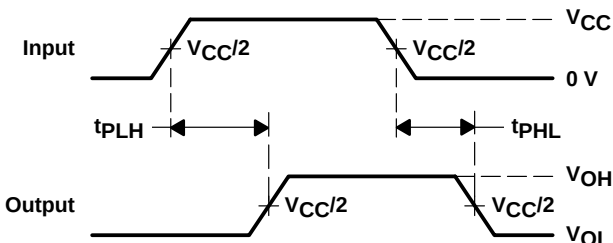
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



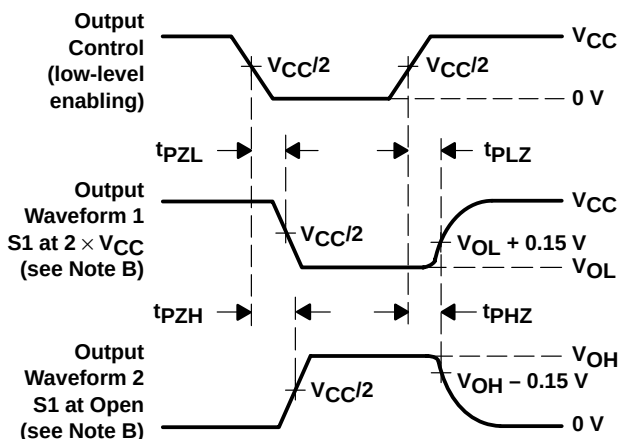
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVCH16240A

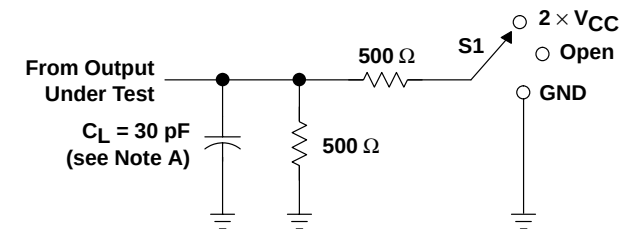
16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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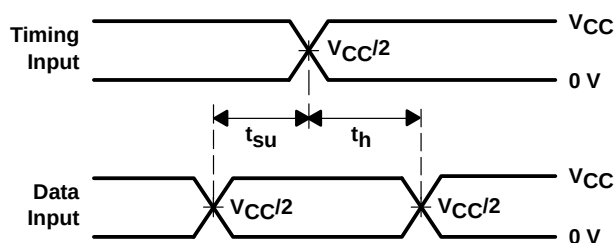
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

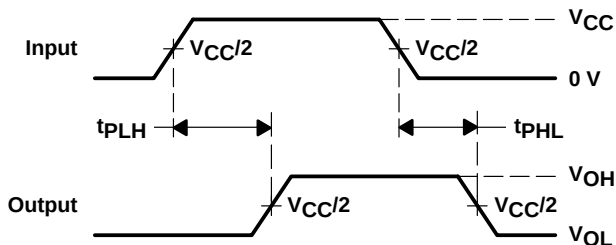


LOAD CIRCUIT

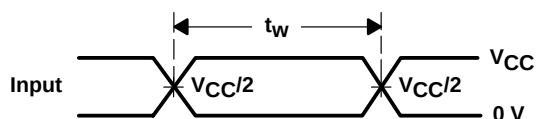
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



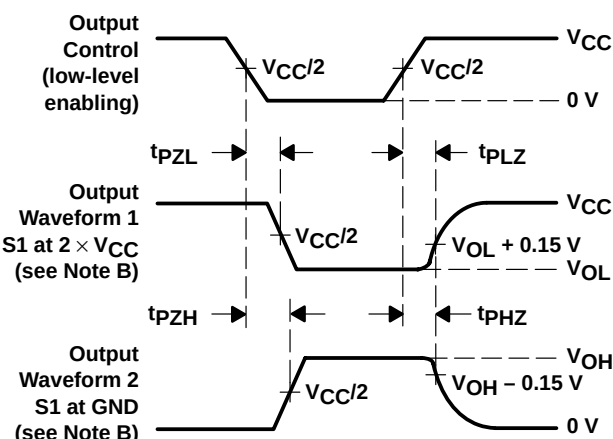
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



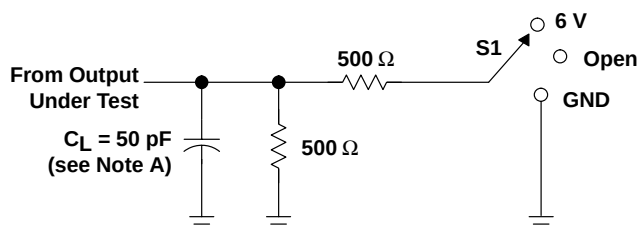
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

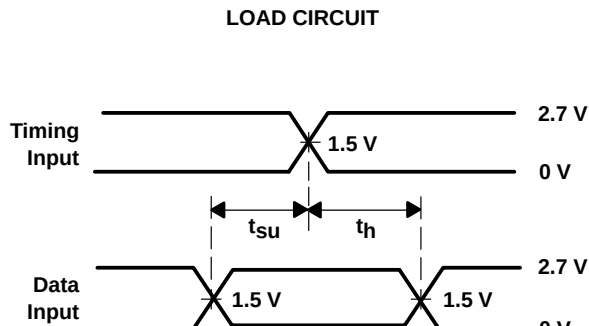
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$

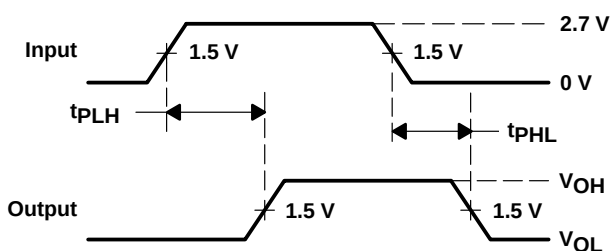


LOAD CIRCUIT

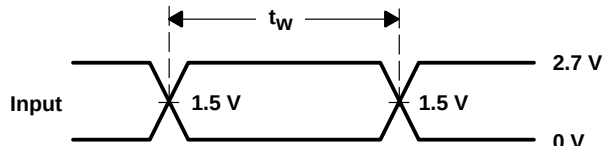
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



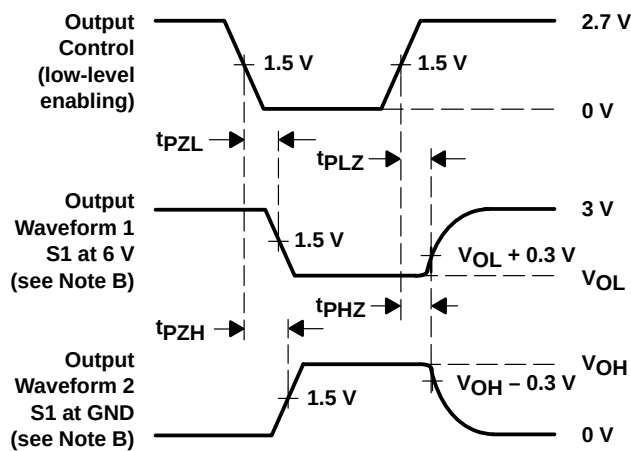
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN74LVCH16241A

16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS348E – MARCH 1994 – REVISED JUNE 1998

- Member of the Texas Instruments *Widebus*™ Family
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH16241A is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

This device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer, and provides true outputs and complementary output-enable (OE and $\overline{OE}$) inputs.

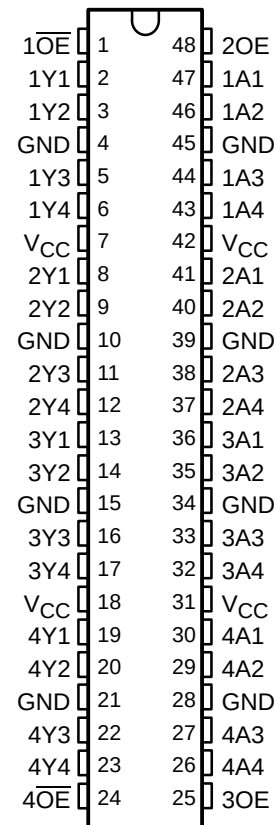
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH16241A is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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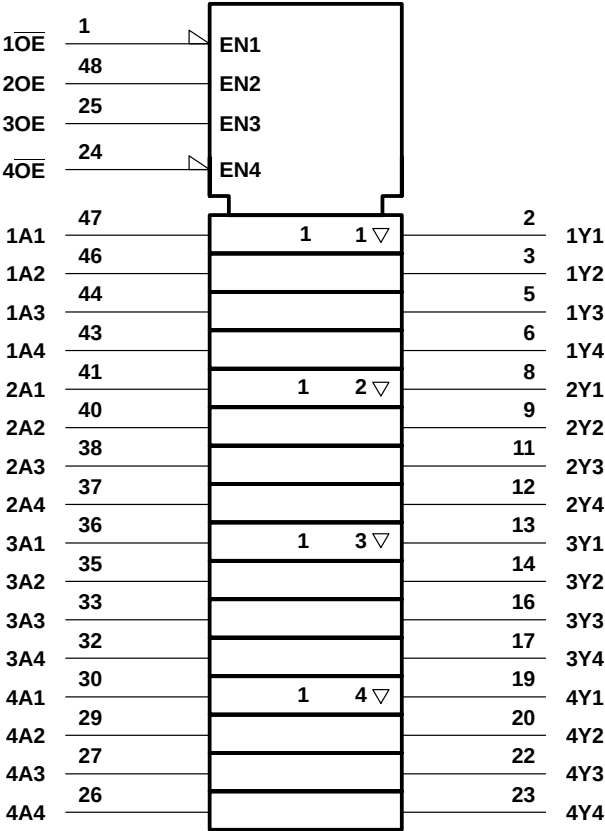
SN74LVCH16241A
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
SCAS348E – MARCH 1994 – REVISED JUNE 1998

FUNCTION TABLES

INPUTS		OUTPUTS 1Y, 4Y
1OE, 4OE	1A, 4A	
L	H	H
L	L	L
H	X	Z

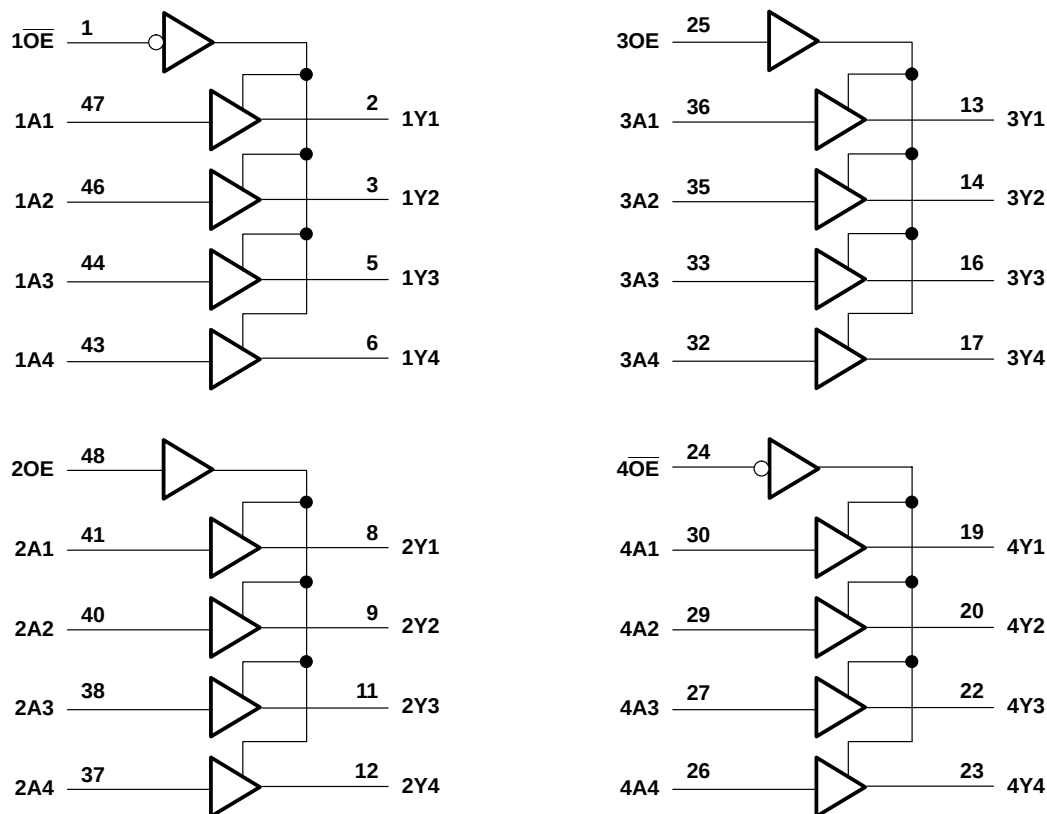
INPUTS		OUTPUTS 2Y, 3Y
2OE, 3OE	2A, 3A	
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

SN74LVCH16241A 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS348E – MARCH 1994 – REVISED JUNE 1998

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65 3.6	V
		Data retention only	1.5	
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 2.7 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 2.7 V to 3.6 V	0.8	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	High or low state	0 V _{CC}	V
		3 state	0 5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V	−4	mA
		V _{CC} = 2.3 V	−8	
		V _{CC} = 2.7 V	−12	
		V _{CC} = 3 V	−24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4	mA
		V _{CC} = 2.3 V	8	
		V _{CC} = 2.7 V	12	
		V _{CC} = 3 V	24	
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVCH16241A
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCAS348E – MARCH 1994 – REVISED JUNE 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} – 0.2			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 4 mA	1.65 V	0.45			
	I _{OL} = 8 mA	2.3 V	0.7			
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _I (hold)	V _I = 0.58 V	1.65 V				µA
	V _I = 1.07 V					
	V _I = 0.7 V		45			
	V _I = 1.7 V	2.3 V	–45			
	V _I = 0.8 V		75			
	V _I = 2 V	3 V	–75			
	V _I = 0 to 3.6 V [‡]	3.6 V			±500	
I _{off}	V _I or V _O = 5.5 V	0			±10	µA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V			±10	µA
I _{CC}	V _I = V _{CC} or GND	3.6 V			20	µA
	3.6 V ≤ V _I ≤ 5.5 V [§]				20	
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	V _I = V _{CC} or GND	3.3 V				pF
C _O	V _O = V _{CC} or GND	3.3 V				pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This is the bus-hold maximum dynamic current required to switch the input from one state to another.

[§] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y									ns
t _{en}	OE or $\overline{\text{OE}}$	Y									ns
t _{dis}	OE or $\overline{\text{OE}}$	Y									ns

PRODUCT PREVIEW



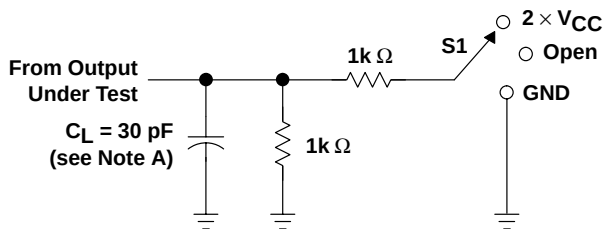
SN74LVCH16241A
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
SCAS348E – MARCH 1994 – REVISED JUNE 1998

operating characteristics, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	$f = 10\text{ MHz}$				pF
	Outputs disabled					

PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

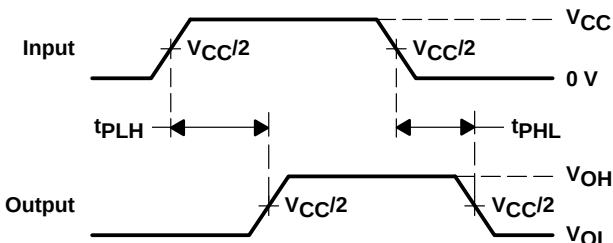


LOAD CIRCUIT

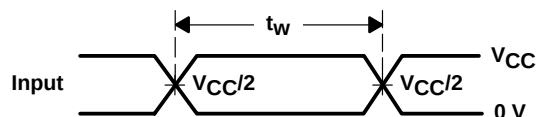
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



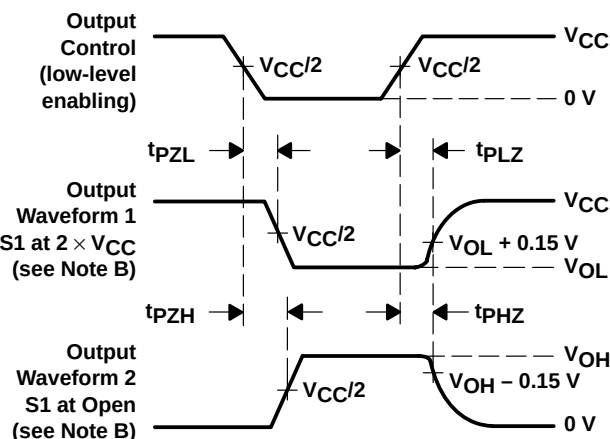
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVCH16241A

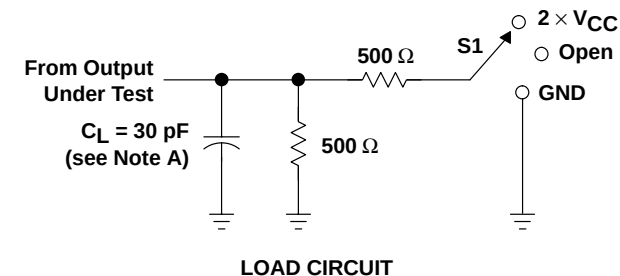
16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

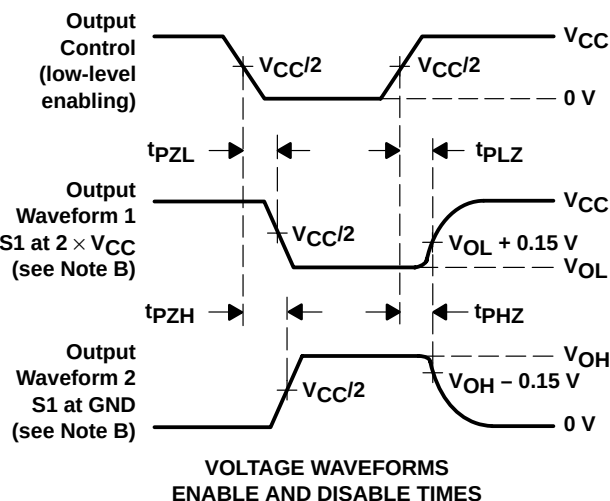
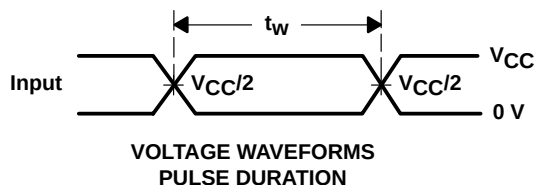
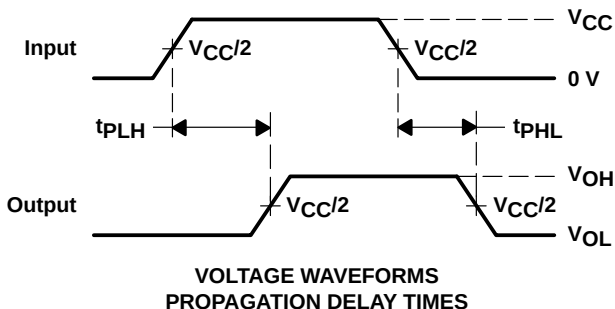
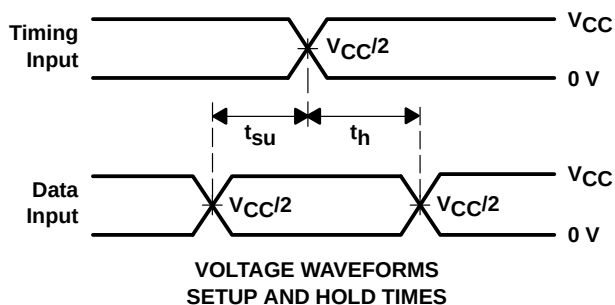
SCAS348E – MARCH 1994 – REVISED JUNE 1998

PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND

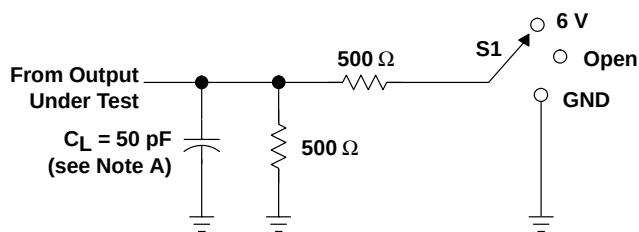


- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

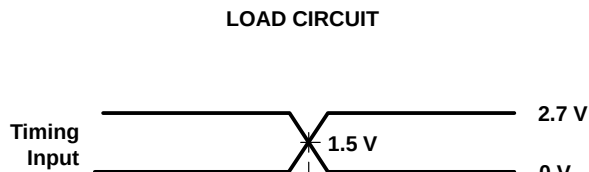
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

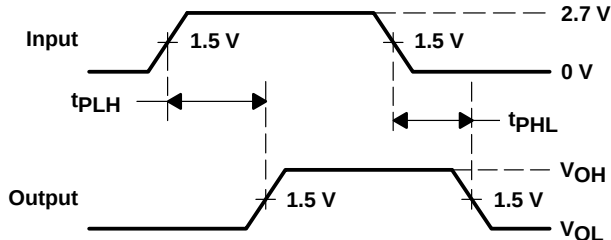


LOAD CIRCUIT

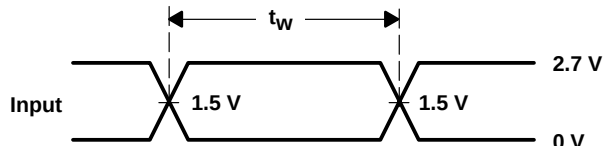
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



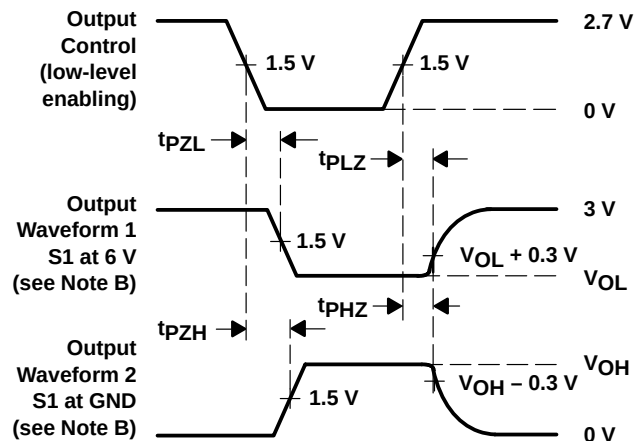
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN74LVC16244A

16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCES061G – DECEMBER 1995 – REVISED JUNE 1998

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation On All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC16244A is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

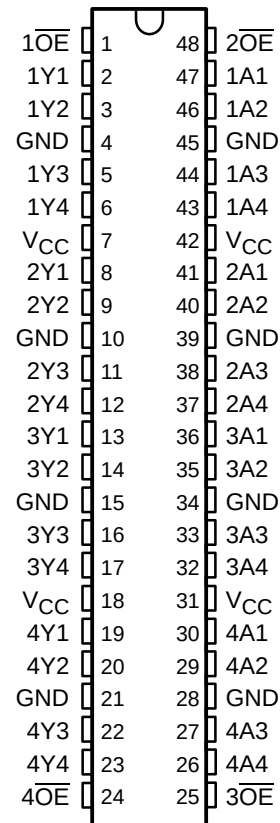
The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC16244A is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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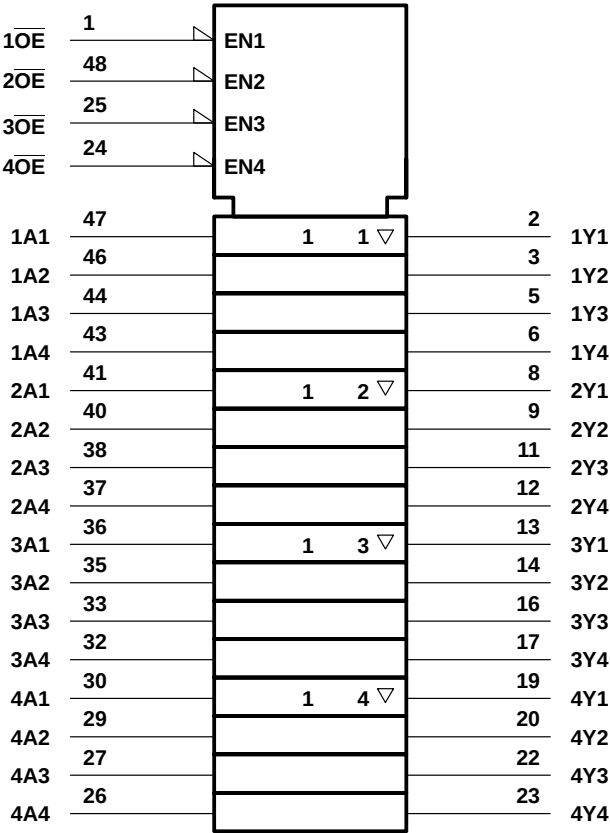
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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logic symbol†

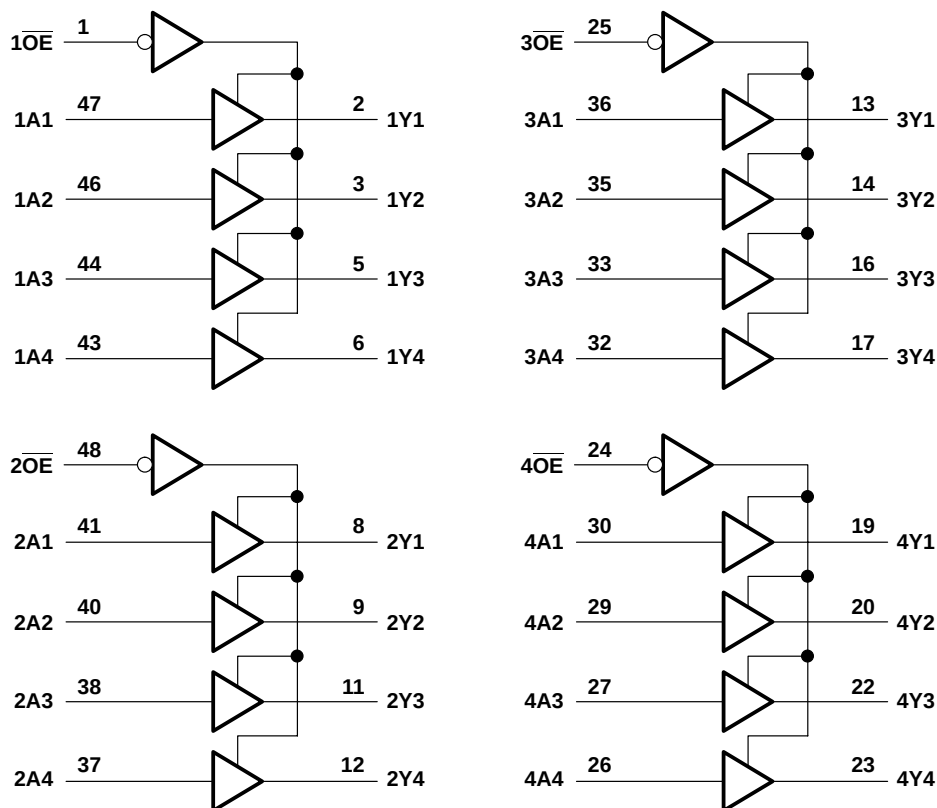


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LVC16244A
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCES061G – DECEMBER 1995 – REVISED JUNE 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

SN74LVC16244A
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCES061G – DECEMBER 1995 – REVISED JUNE 1998

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage	0	5.5		V
V _O	Output voltage	High or low state	0	V _{CC}	V
		3 state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V		−4	mA
		V _{CC} = 2.3 V		−8	
		V _{CC} = 2.7 V		−12	
		V _{CC} = 3 V		−24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		8	
		V _{CC} = 2.7 V		12	
		V _{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate	0	10		ns/V
T _A	Operating free-air temperature	−40	85		°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC16244A
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 4 mA	1.65 V	0.45			
	I _{OL} = 8 mA	2.3 V	0.7			
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _{off}	V _I or V _O = 5.5 V	0			±10	µA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V			±10	µA
I _{CC}	V _I = V _{CC} or GND	3.6 V			20	µA
	3.6 V ≤ V _I ≤ 5.5 V [‡]				20	
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	V _I = V _{CC} or GND	3.3 V			5.5	pF
C ₀	V _O = V _{CC} or GND	3.3 V			6	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	§	§	§	§	4.7		1.1	4.1	ns
t _{en}	$\overline{\text{OE}}$	Y	§	§	§	§	5.8		1	4.6	ns
t _{dis}	$\overline{\text{OE}}$	Y	§	§	§	§	6.2		1.8	5.8	ns
t _{sk(o)} [¶]									1		ns

§ This information was not available at the time of publication.

¶ Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	§	§	34	pF
		Outputs disabled	§	§	4	

§ This information was not available at the time of publication.



SN74LVC16244A

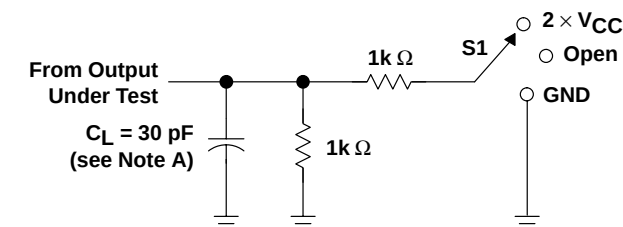
16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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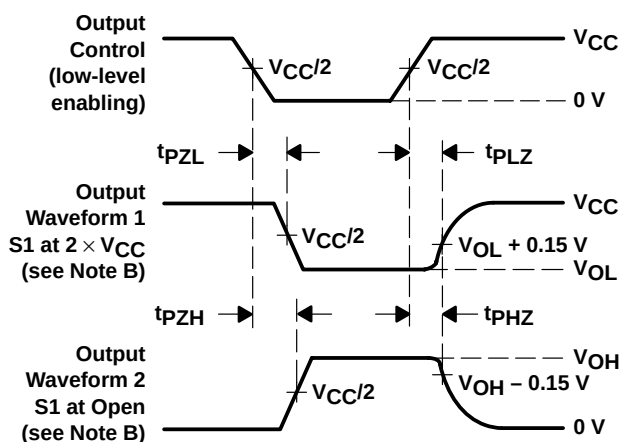
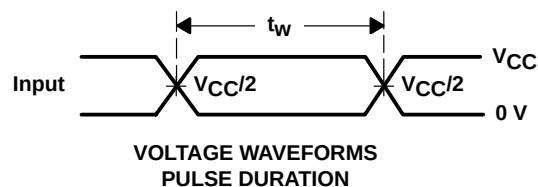
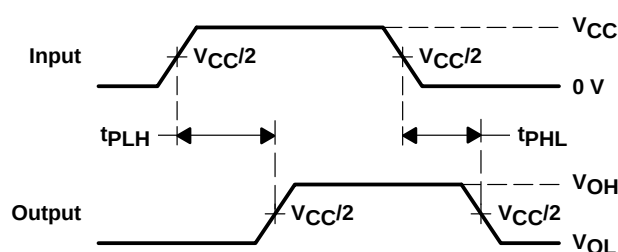
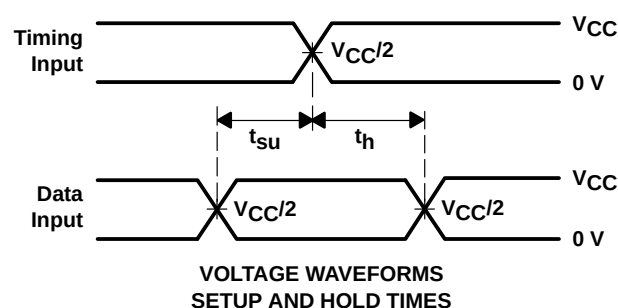
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PHZ}	Open

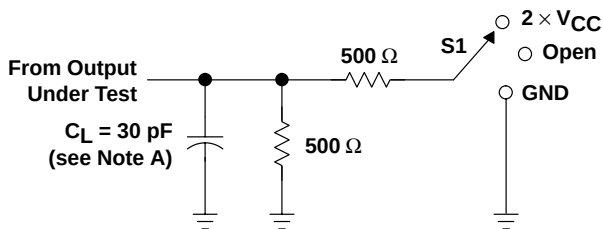


- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

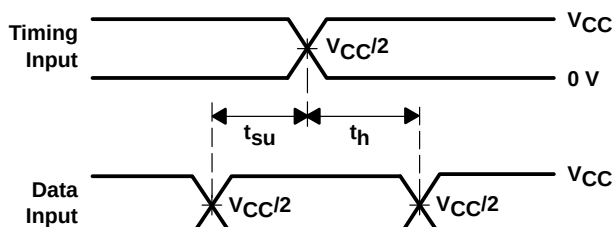
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

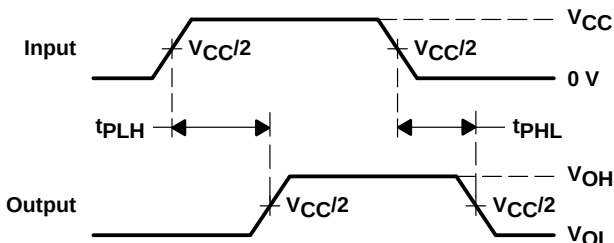


LOAD CIRCUIT

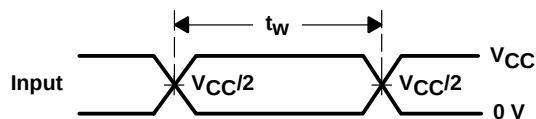
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



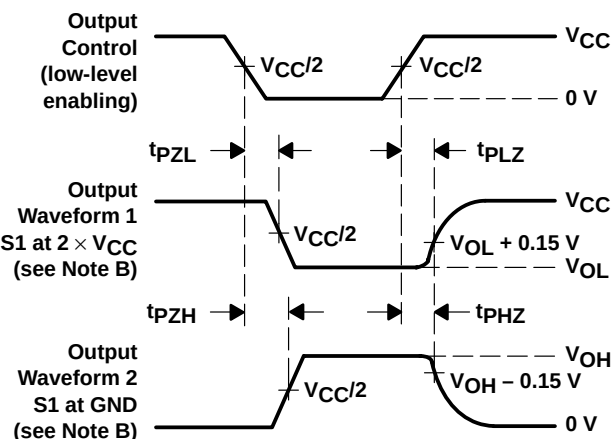
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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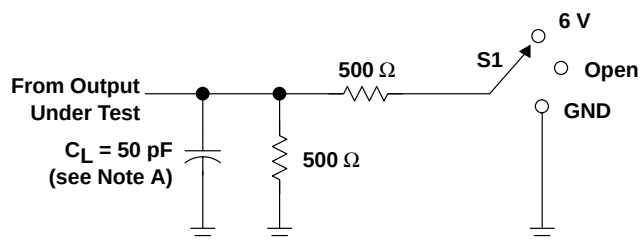
16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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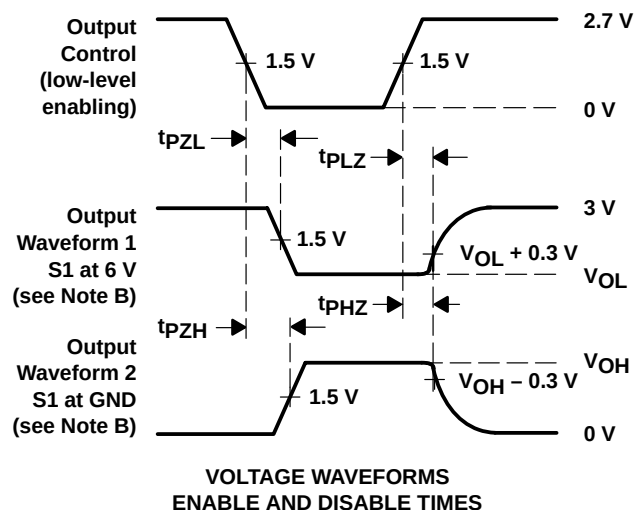
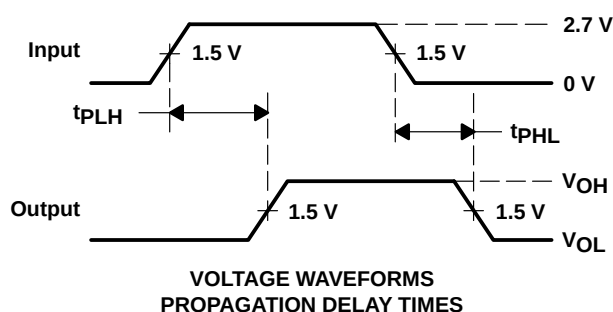
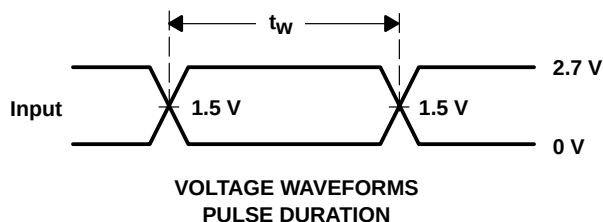
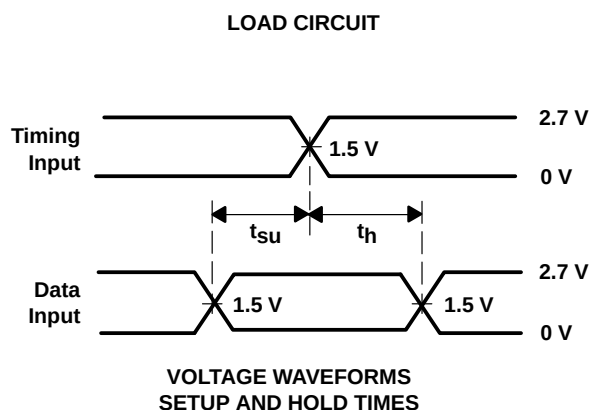
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

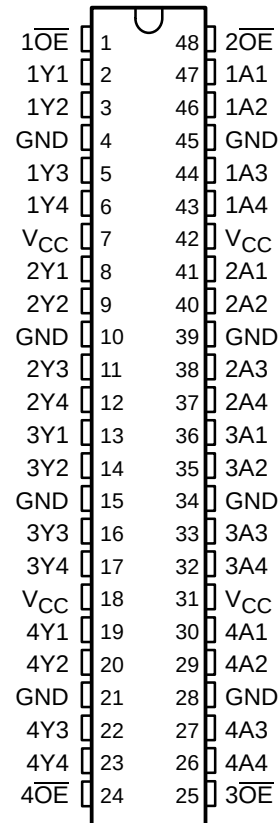
SN74LVCH16244A

16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

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- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH16244A is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH16244A is characterized for operation from -40°C to 85°C .

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



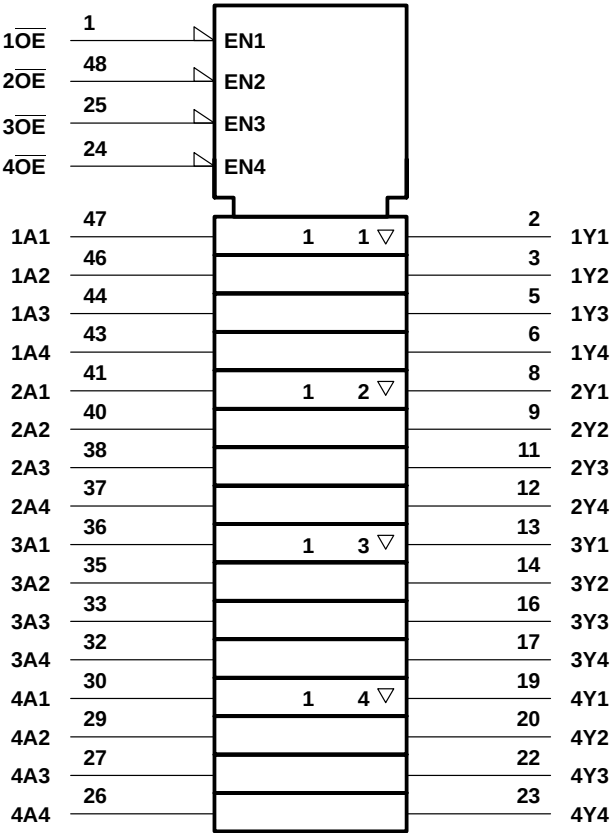
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FUNCTION TABLE
(each 4-bit buffer)

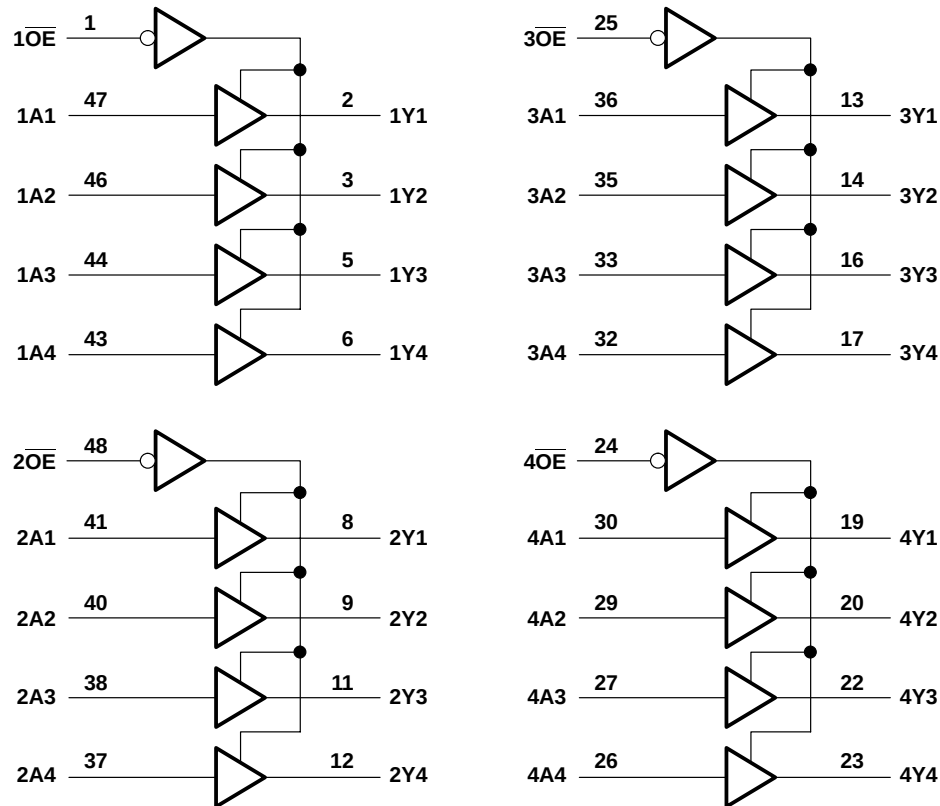
INPUTS		OUTPUT Y
OE	A	
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

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16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	High or low state	0	V _{CC}	V
		3 state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V	−4		mA
		V _{CC} = 2.3 V	−8		
		V _{CC} = 2.7 V	−12		
		V _{CC} = 3 V	−24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		mA
		V _{CC} = 2.3 V	8		
		V _{CC} = 2.7 V	12		
		V _{CC} = 3 V	24		
Δt/Δv	Input transition rise or fall rate	0	10	ns/V	
T _A	Operating free-air temperature	−40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 μA		1.65 V to 3.6 V	V _{CC} –0.2		V	
	I _{OH} = –4 mA		1.65 V	1.2			
	I _{OH} = –8 mA		2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2				
		3 V	2.4				
	I _{OH} = –24 mA	3 V	2.2				
V _{OL}	I _{OL} = 100 μA		1.65 V to 3.6 V	0.2		V	
	I _{OL} = 4 mA		1.65 V	0.45			
	I _{OL} = 8 mA		2.3 V	0.7			
	I _{OL} = 12 mA		2.7 V	0.4			
	I _{OL} = 24 mA		3 V	0.55			
I _I	V _I = 0 to 5.5 V		3.6 V	±5		μA	
I _I (hold)	V _I = 0.58 V		1.65 V	‡		μA	
	V _I = 1.07 V			‡			
	V _I = 0.7 V		2.3 V	45			
	V _I = 1.7 V			–45			
	V _I = 0.8 V		3 V	75			
	V _I = 2 V			–75			
	V _I = 0 to 3.6 V [§]		3.6 V	±500			
I _{off}	V _I or V _O = 5.5 V		0	±10		μA	
I _{OZ}	V _O = 0 to 5.5 V		3.6 V	±10		μA	
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	20		μA	
	3.6 V ≤ V _I ≤ 5.5 V [¶]			20			
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V	500		μA	
C _i	V _I = V _{CC} or GND		3.3 V	5.5		pF	
C _O	V _O = V _{CC} or GND		3.3 V	6		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This information was not available at the time of publication.

[§] This is the bus-hold maximum dynamic current required to switch the input from one state to another.

[¶] This applies in the disabled state only.



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16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	†	†	†	†	4.7		1.1	4.1	ns
t_{en}	$\overline{OE}$	Y	†	†	†	†	5.8		1	4.6	ns
t_{dis}	$\overline{OE}$	Y	†	†	†	†	6.2		1.8	5.8	ns
$t_{sk(o)}^{\ddagger}$									1		ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction.

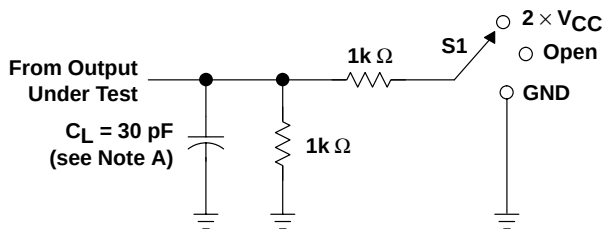
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	†	†	34	pF
		Outputs disabled		†	†	4	

† This information was not available at the time of publication.

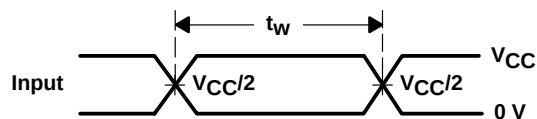
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$$

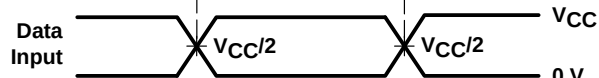


LOAD CIRCUIT

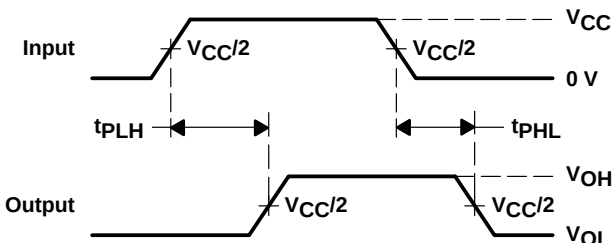
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



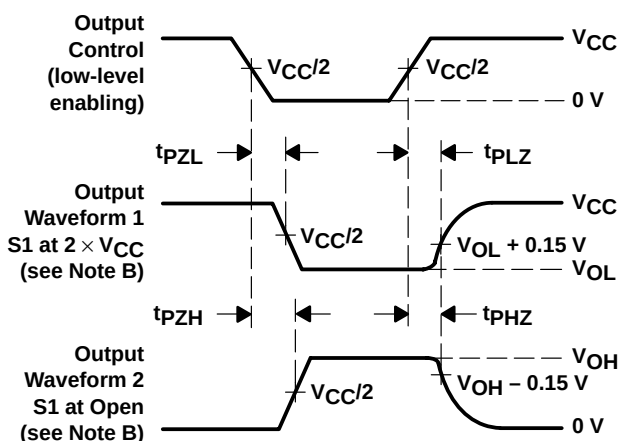
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVCH16244A

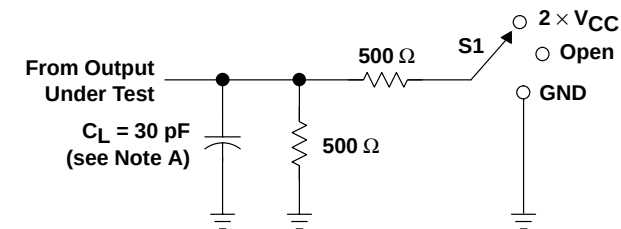
16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

SCAS313G – NOVEMBER 1993 – REVISED JUNE 1998

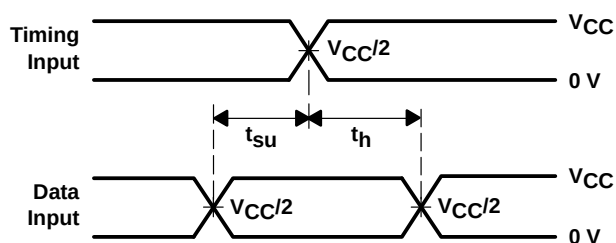
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

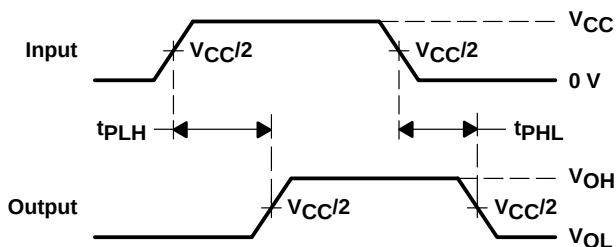


LOAD CIRCUIT

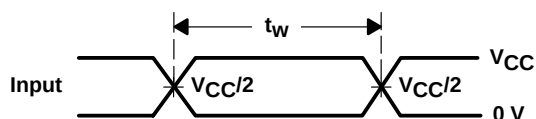
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



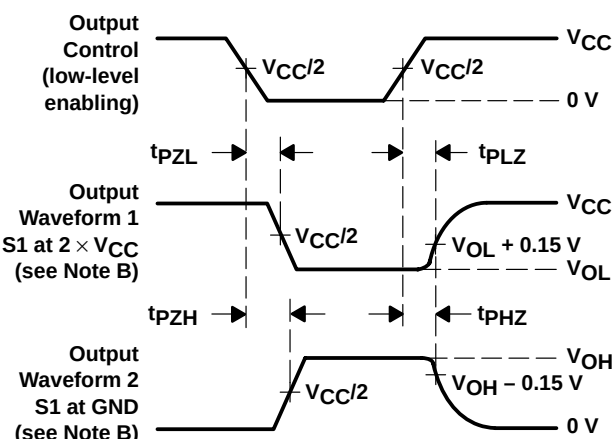
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



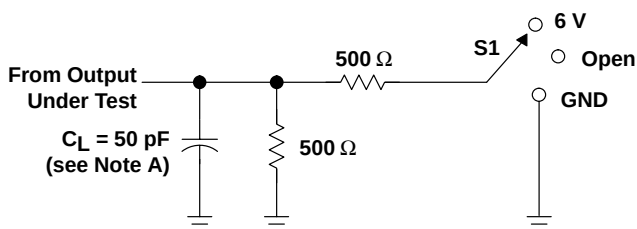
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

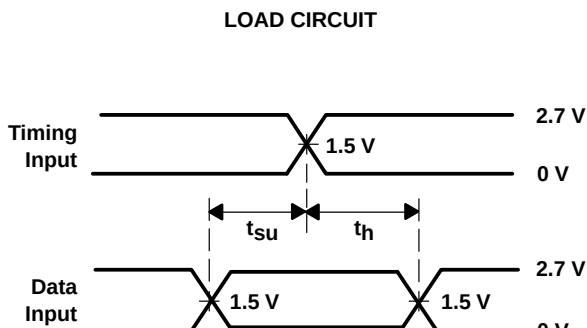
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

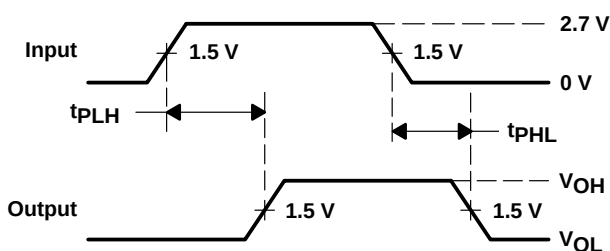


LOAD CIRCUIT

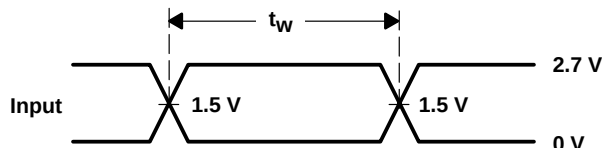
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



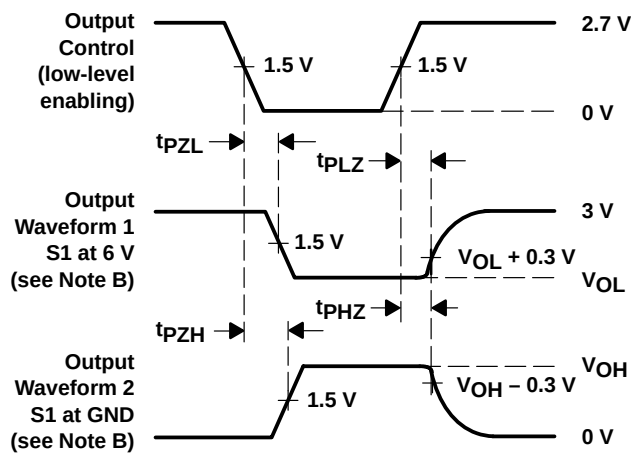
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

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 - The outputs are measured one at a time with one transition per measurement.
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 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN74LVC16245A 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES062G – DECEMBER 1995 – REVISED JUNE 1998

- Member of the Texas Instruments *Widebus*™ Family
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Power Off Disables Outputs, Permitting Live Insertion
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit (dual-octal) noninverting bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC16245A is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

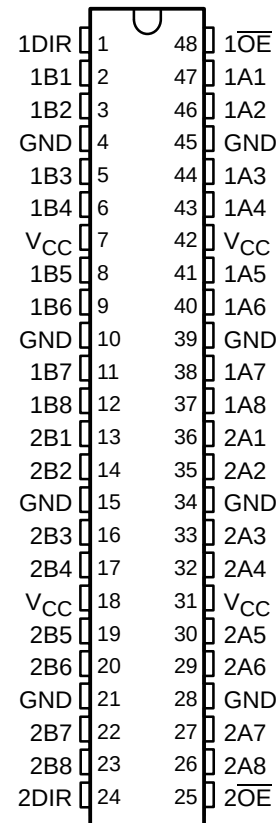
This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC16245A is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



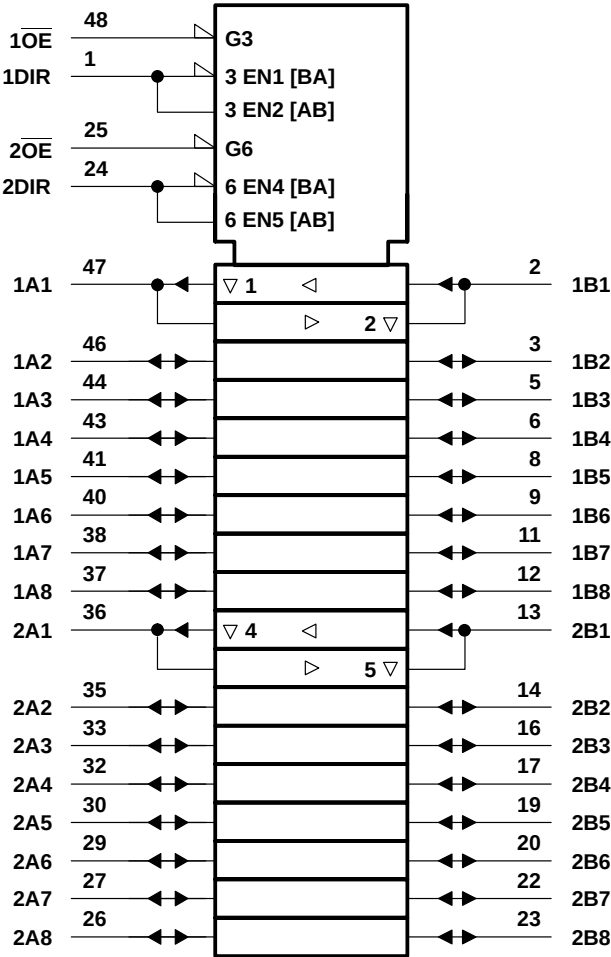
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FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



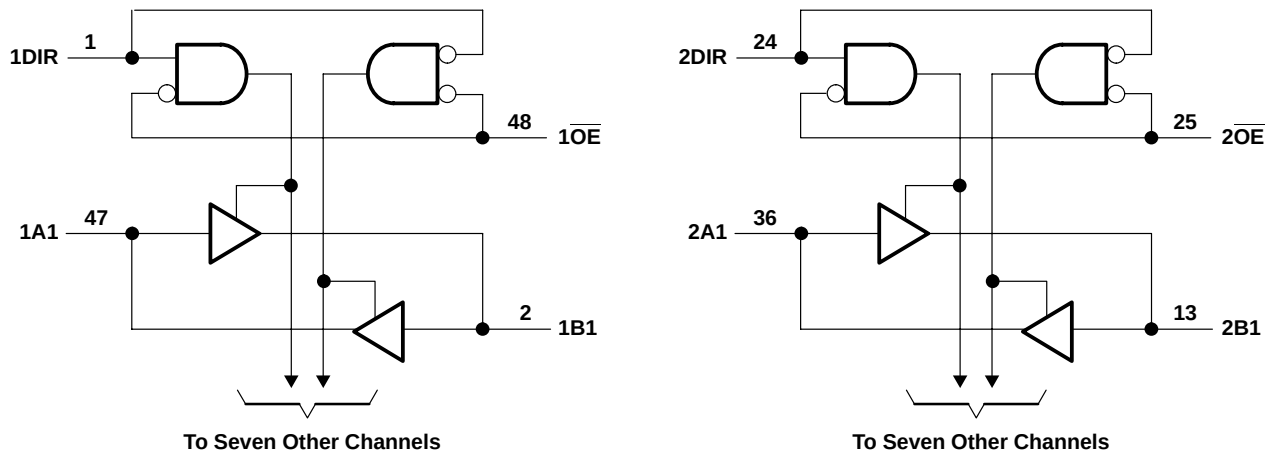
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LVC16245A

16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I : (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

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16-BIT BUS TRANSCEIVER

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65 \text{ V}$		–4	mA
	$V_{CC} = 2.3 \text{ V}$		–8	
	$V_{CC} = 2.7 \text{ V}$		–12	
	$V_{CC} = 3 \text{ V}$		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65 \text{ V}$		4	mA
	$V_{CC} = 2.3 \text{ V}$		8	
	$V_{CC} = 2.7 \text{ V}$		12	
	$V_{CC} = 3 \text{ V}$		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	5	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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16-BIT BUS TRANSCEIVER
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}		I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
		I _{OH} = –4 mA	1.65 V	1.2			
		I _{OH} = –8 mA	2.3 V	1.7			
		I _{OH} = –12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = –24 mA	3 V	2.2			
V _{OL}		I _{OL} = 100 µA	1.65 V to 3.6 V			0.2	V
		I _{OL} = 4 mA	1.65 V			0.45	
		I _{OL} = 8 mA	2.3 V			0.7	
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _{off}		V _I or V _O = 5.5 V	0			±10	µA
I _{OZ} [‡]		V _O = 0 to 5.5 V	3.6 V			±10	µA
I _{CC}		V _I = V _{CC} or GND	3.6 V			20	µA
		3.6 V ≤ V _I ≤ 5.5 V [§]				20	
I _{CC}		I _O = 0					
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V			5	pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V			7.5	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	¶	¶	¶	¶	4.7		1	4	ns
t _{en}	$\overline{\text{OE}}$	A or B	¶	¶	¶	¶	6.7		1.5	5.5	ns
t _{dis}	$\overline{\text{OE}}$	A or B	¶	¶	¶	¶	7.1		1.5	6.6	ns
t _{sk(o)} [#]									1		ns

¶ This information was not available at the time of publication.

Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	f = 10 MHz	¶	¶	38	pF
		Outputs disabled		¶	¶	4	

¶ This information was not available at the time of publication.



SN74LVC16245A

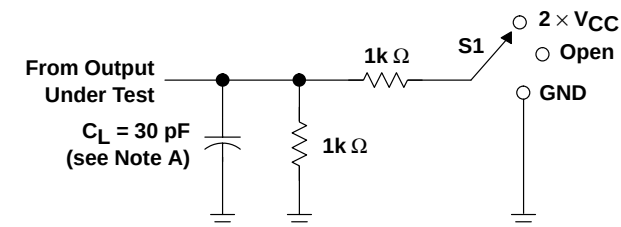
16-BIT BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCES062G – DECEMBER 1995 – REVISED JUNE 1998

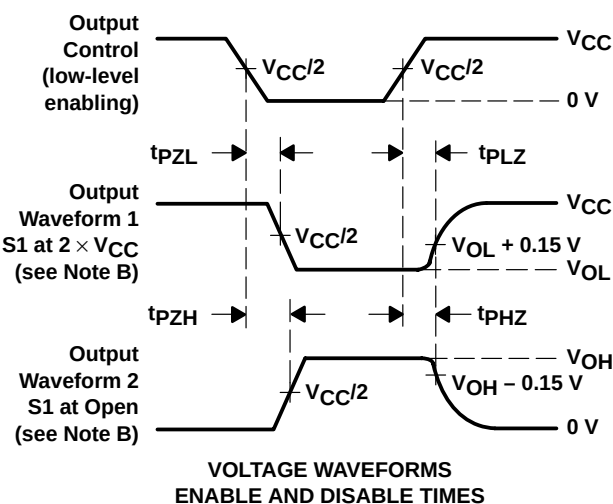
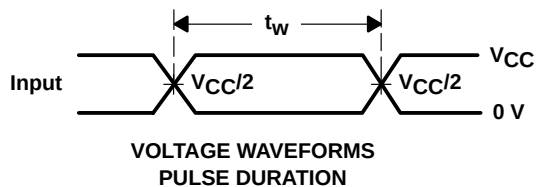
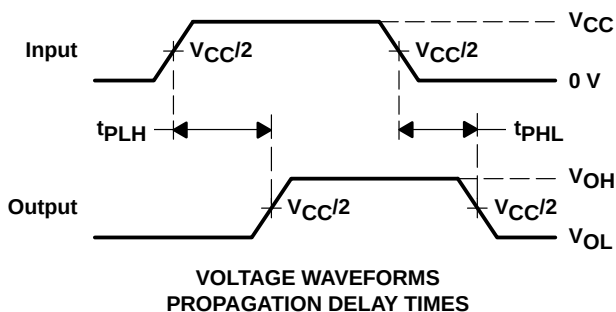
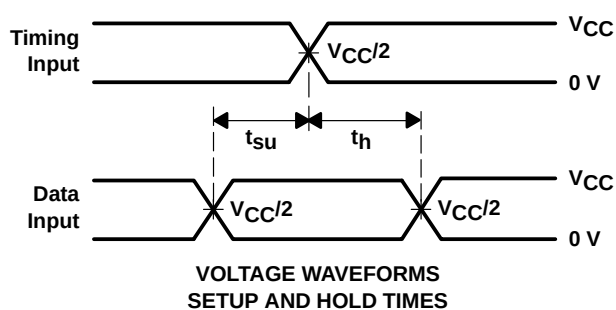
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	Open

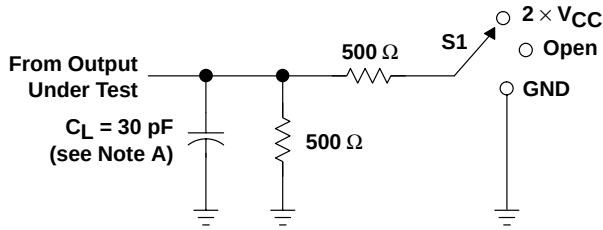


- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

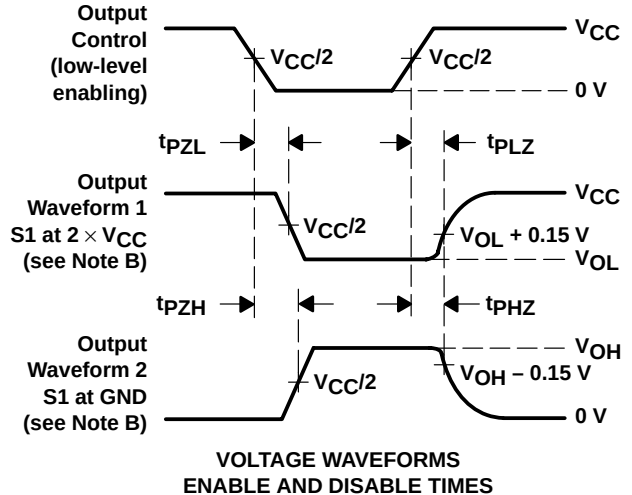
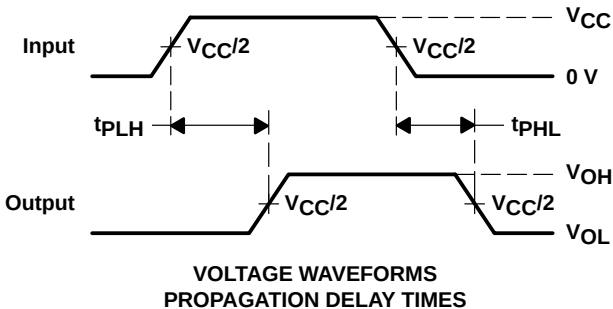
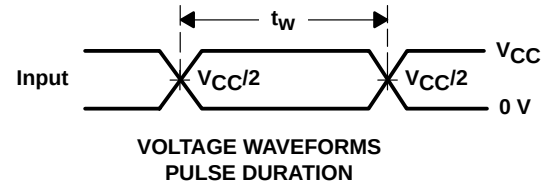
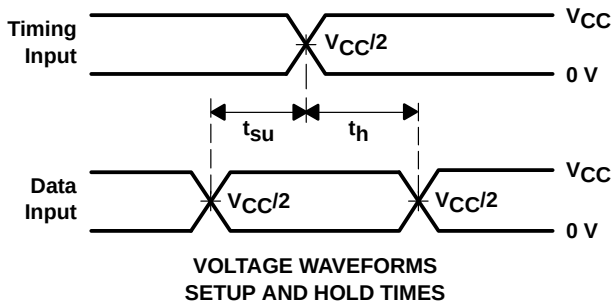
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
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- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN74LVC16245A

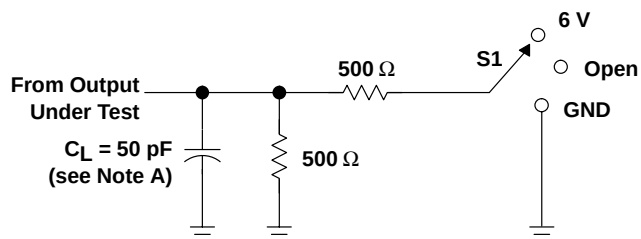
16-BIT BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

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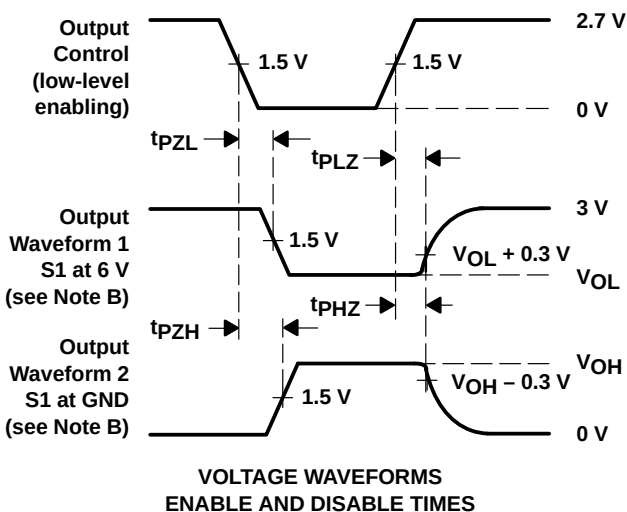
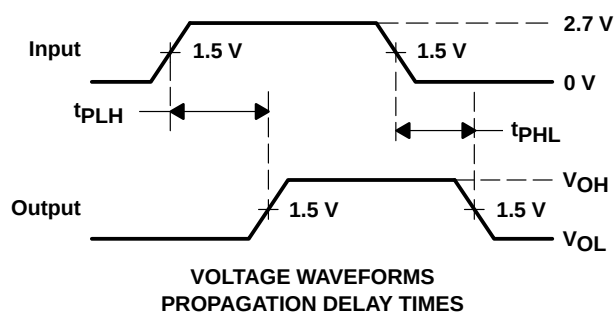
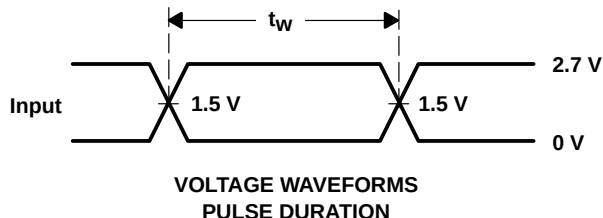
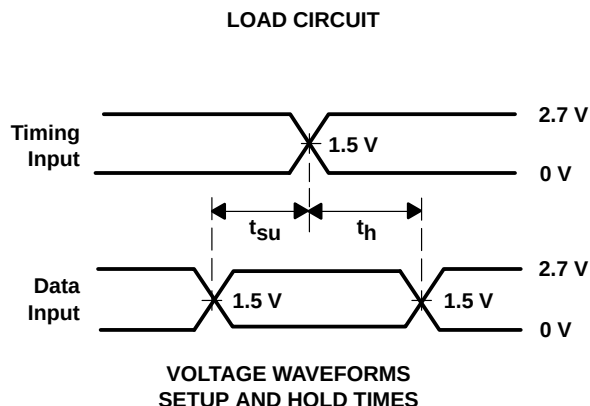
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

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Figure 3. Load Circuit and Voltage Waveforms

SN74LVCH16245A

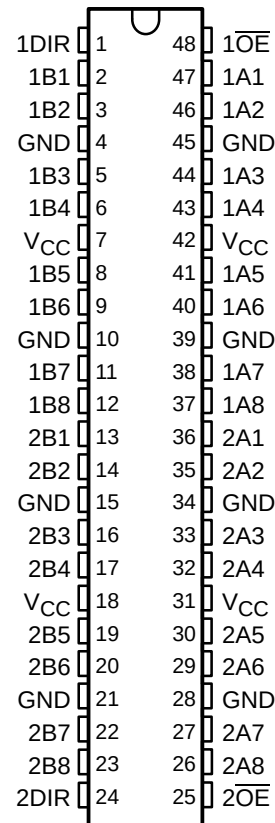
16-BIT BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

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- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DGG OR DL PACKAGE
(TOP VIEW)



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To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH16245A is characterized for operation from -40°C to 85°C .

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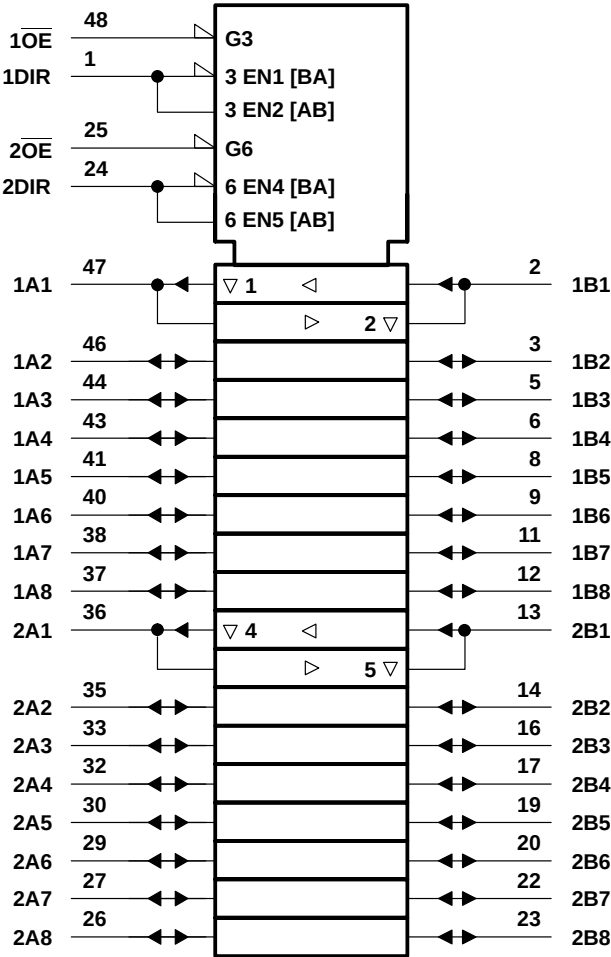
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FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

[illegible]

4-51

SN74LVCH16245A

16-BIT BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCES063G – DECEMBER 1995 – REVISED JUNE 1998

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65 \text{ V}$		–4	mA
	$V_{CC} = 2.3 \text{ V}$		–8	
	$V_{CC} = 2.7 \text{ V}$		–12	
	$V_{CC} = 3 \text{ V}$		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65 \text{ V}$		4	mA
	$V_{CC} = 2.3 \text{ V}$		8	
	$V_{CC} = 2.7 \text{ V}$		12	
	$V_{CC} = 3 \text{ V}$		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	5	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVCH16245A
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCES063G – DECEMBER 1995 – REVISED JUNE 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}		I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
		I _{OH} = –4 mA	1.65 V	1.2			
		I _{OH} = –8 mA	2.3 V	1.7			
		I _{OH} = –12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = –24 mA	3 V	2.2			
V _{OL}		I _{OL} = 100 µA	1.65 V to 3.6 V			0.2	V
		I _{OL} = 4 mA	1.65 V			0.45	
		I _{OL} = 8 mA	2.3 V			0.7	
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _I (hold)	A or B ports	V _I = 0.58 V	1.65 V	‡			µA
		V _I = 1.07 V		‡			
		V _I = 0.7 V	2.3 V	45			
		V _I = 1.7 V		–45			
		V _I = 0.8 V	3 V	75			
		V _I = 2 V		–75			
		V _I = 0 to 3.6 V [§]	3.6 V			±500	
I _{off}		V _I or V _O = 5.5 V	0			±10	µA
I _{OZ} [¶]		V _O = 0 to 5.5 V	3.6 V			±10	µA
I _{CC}		V _I = V _{CC} or GND	3.6 V			20	µA
		3.6 V ≤ V _I ≤ 5.5 V [#]				20	
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V			5	pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V			7.5	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This information was not available at the time of publication.

[§] This is the bus-hold maximum dynamic current required to switch the input from one state to another.

[¶] For I/O ports, the parameter I_{OZ} includes the input leakage current, but not I_I(hold).

[#] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	‡	‡	‡	‡	4.7		1	4	ns
t _{en}	$\overline{\text{OE}}$	A or B	‡	‡	‡	‡	6.7		1.5	5.5	ns
t _{dis}	$\overline{\text{OE}}$	A or B	‡	‡	‡	‡	7.1		1.5	6.6	ns
t _{sk(o)}									1		ns

[‡] This information was not available at the time of publication.

^{||} Skew between any two outputs of the same package switching in the same direction



SN74LVCH16245A
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

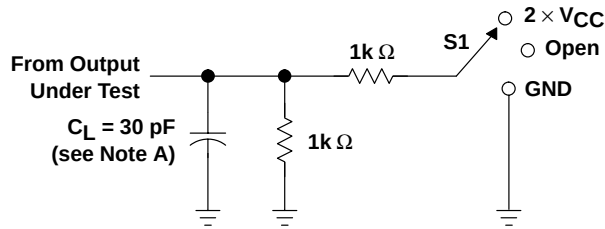
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operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	$f = 10\text{ MHz}$		†	†	40	pF
	Outputs disabled			†	†	4	

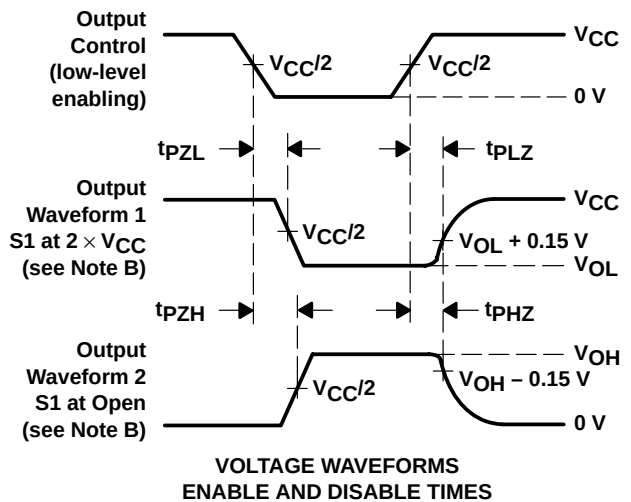
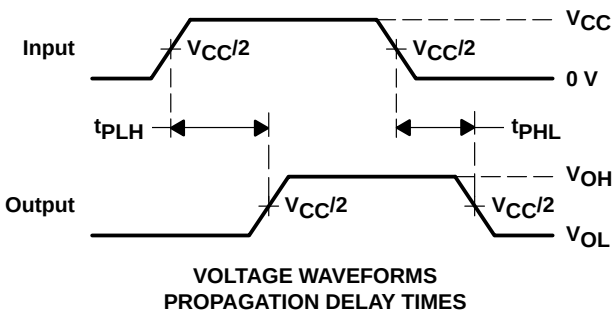
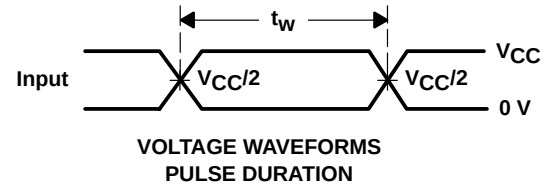
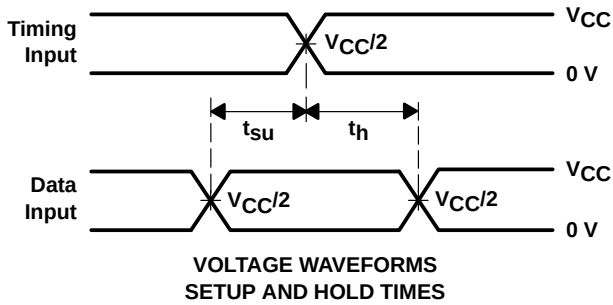
† This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVCH16245A

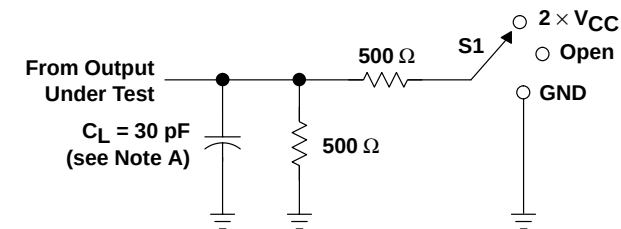
16-BIT BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCES063G – DECEMBER 1995 – REVISED JUNE 1998

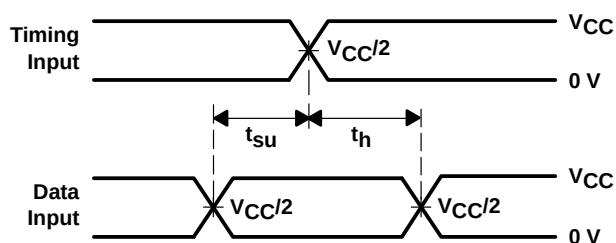
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

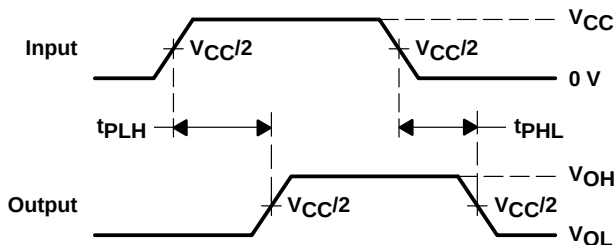


LOAD CIRCUIT

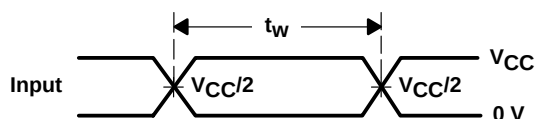
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



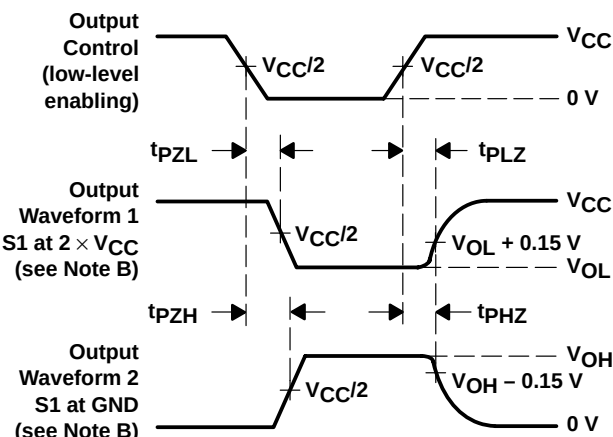
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

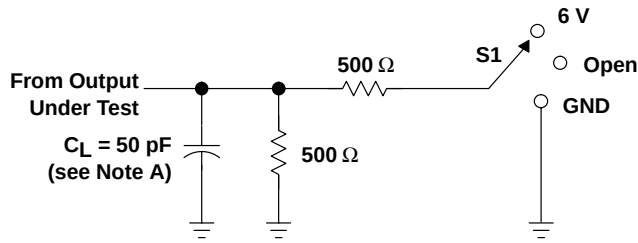


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

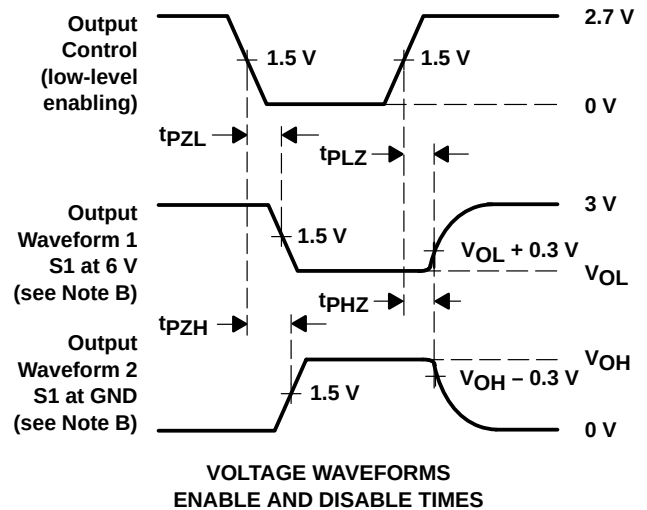
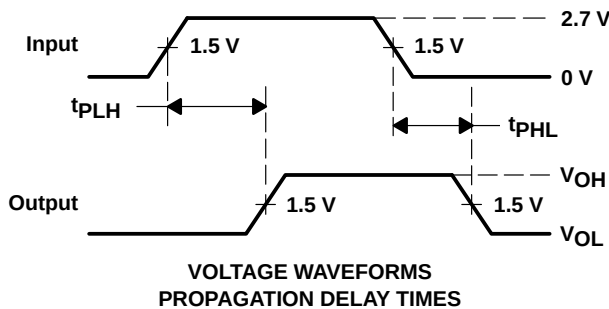
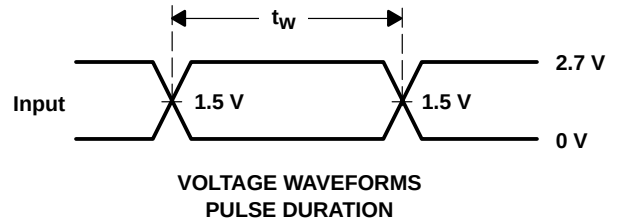
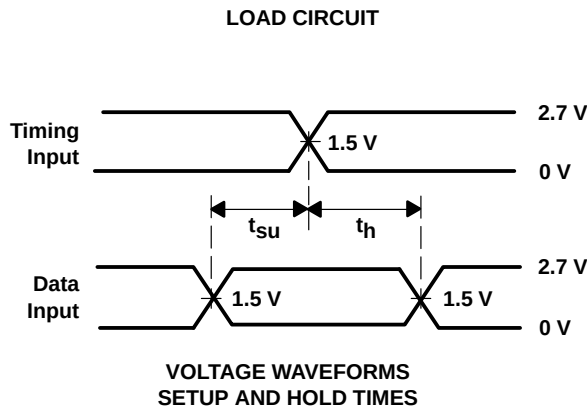
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN74LVCH16373A 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS568G – MARCH 1996 – REVISED JUNE 1998

- Member of the Texas Instruments *Widebus*™ Family
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DGG OR DL PACKAGE
(TOP VIEW)

$\overline{1OE}$	1	48	1LE
1Q1	2	47	1D1
1Q2	3	46	1D2
GND	4	45	GND
1Q3	5	44	1D3
1Q4	6	43	1D4
V_{CC}	7	42	V_{CC}
1Q5	8	41	1D5
1Q6	9	40	1D6
GND	10	39	GND
1Q7	11	38	1D7
1Q8	12	37	1D8
2Q1	13	36	2D1
2Q2	14	35	2D2
GND	15	34	GND
2Q3	16	33	2D3
2Q4	17	32	2D4
V_{CC}	18	31	V_{CC}
2Q5	19	30	2D5
2Q6	20	29	2D6
GND	21	28	GND
2Q7	22	27	2D7
2Q8	23	26	2D8
$\overline{2OE}$	24	25	2LE

description

This 16-bit transparent D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH16373A is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH16373A is characterized for operation from -40°C to 85°C .

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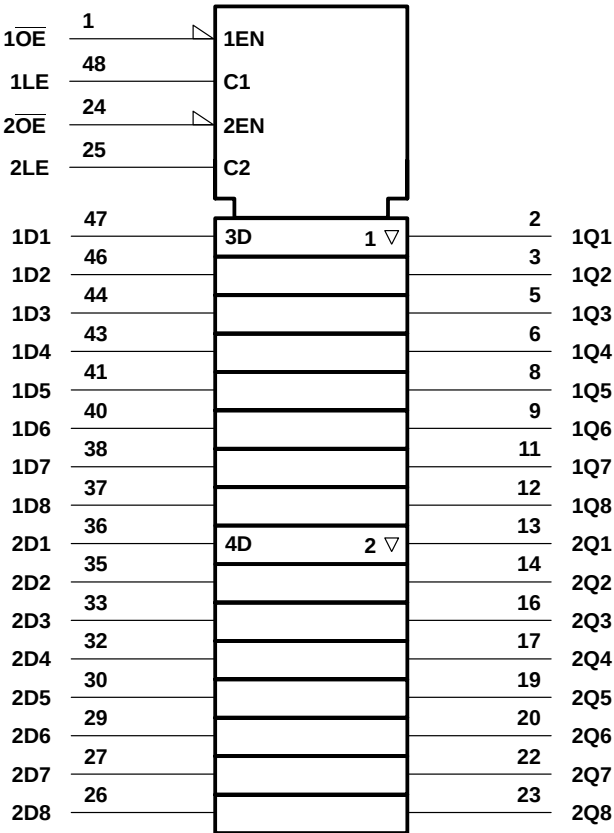
SN74LVCH16373A 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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FUNCTION TABLE

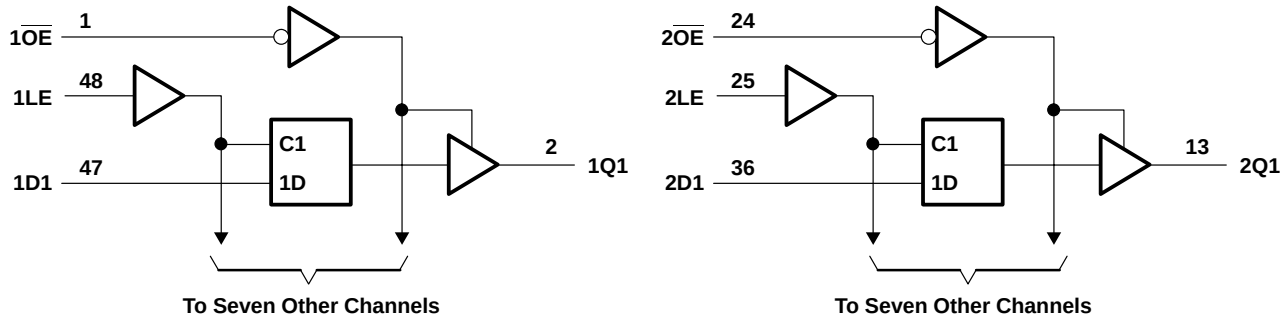
INPUTS			OUTPUT Q
OE	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVCH16373A
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

SCAS568G – MARCH 1996 – REVISED JUNE 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74LVCH16373A
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} – 0.2			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 4 mA	1.65 V	0.45			
	I _{OL} = 8 mA	2.3 V	0.7			
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 0 to 5.5 V	3.6 V	±5			µA
I _I (hold)	V _I = 0.58 V	1.65 V	‡			µA
	V _I = 1.07 V		‡			
	V _I = 0.7 V	2.3 V	45			
	V _I = 1.7 V		–45			
	V _I = 0.8 V	3 V	75			
	V _I = 2 V		–75			
	V _I = 0 to 3.6 V [§]	3.6 V	±500			
I _{off}	V _I or V _O = 5.5 V	0	±10			µA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V	±10			µA
I _{CC}	V _I = V _{CC} or GND	3.6 V	20			µA
	3.6 V ≤ V _I ≤ 5.5 V [¶]		20			
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			µA
C _i	V _I = V _{CC} or GND	3.3 V	5			pF
C _o	V _O = V _{CC} or GND	3.3 V	6.5			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This information was not available at the time of publication.

[§] This is the bus-hold maximum dynamic current required to switch the input from one state to another.

[¶] This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	‡		‡		3.3		3.3		ns
t _{su}	Setup time, data before LE↓	‡		‡		1.7		1.7		ns
t _h	Hold time, data after LE↓	‡		‡		1.2		1.2		ns

[‡] This information was not available at the time of publication.



SN74LVCH16373A
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	†	†	†	†	4.9		1.6	4.2	ns
	LE		†	†	†	†	5.3		2.1	4.6	
t_{en}	$\overline{OE}$	Q	†	†	†	†	5.7		1.3	4.7	ns
t_{dis}	$\overline{OE}$	Q	†	†	†	†	6.3		2.5	5.9	ns

† This information was not available at the time of publication.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per latch	Outputs enabled	f = 10 MHz	†	†	39	pF
		Outputs disabled		†	†	6	

† This information was not available at the time of publication.

SN74LVCH16373A

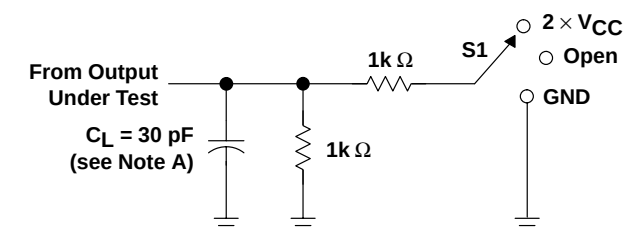
16-BIT TRANSPARENT D-TYPE LATCH

WITH 3-STATE OUTPUTS

SCAS568G – MARCH 1996 – REVISED JUNE 1998

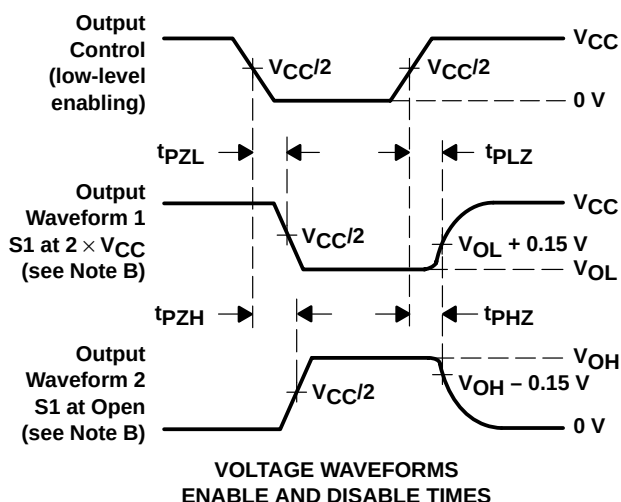
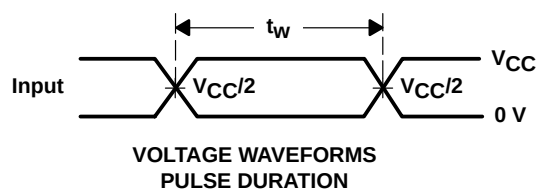
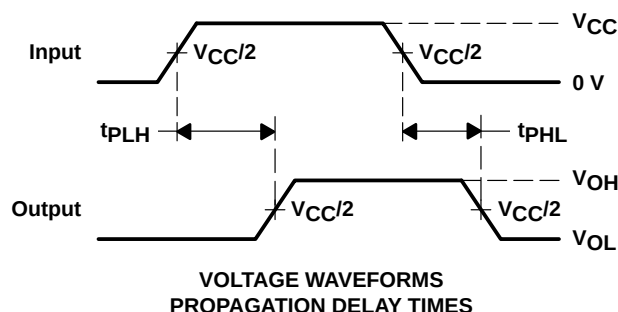
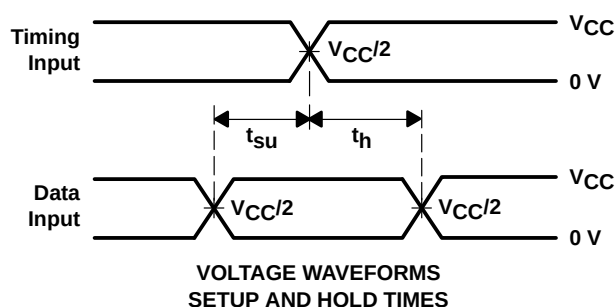
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVCH16373A

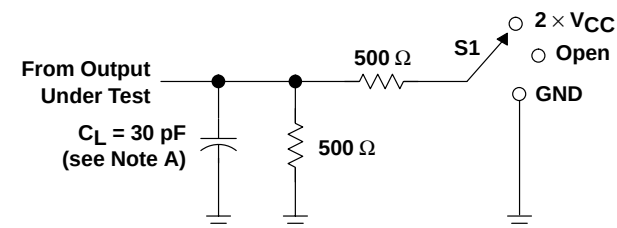
16-BIT TRANSPARENT D-TYPE LATCH

WITH 3-STATE OUTPUTS

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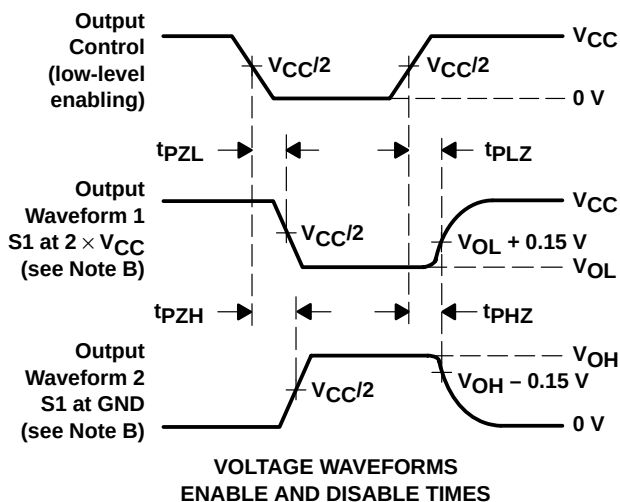
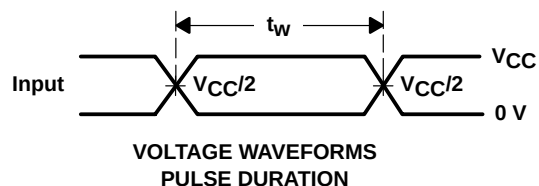
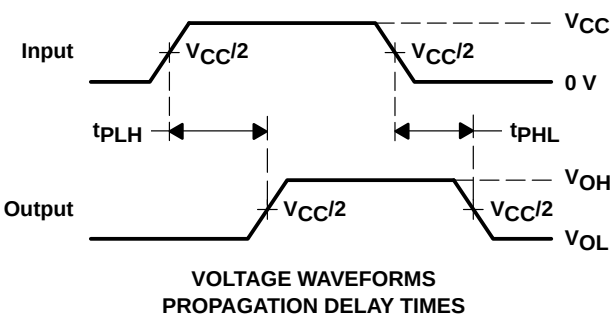
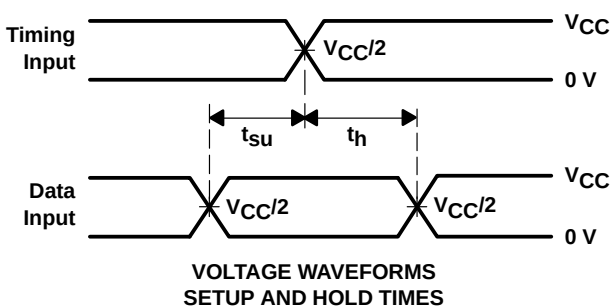
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN74LVCH16373A

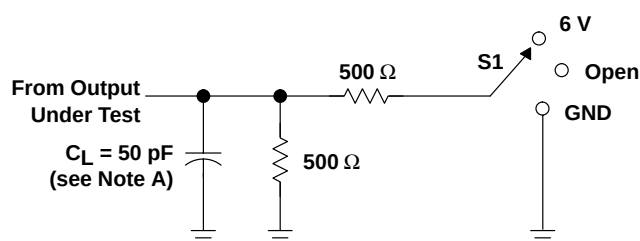
16-BIT TRANSPARENT D-TYPE LATCH

WITH 3-STATE OUTPUTS

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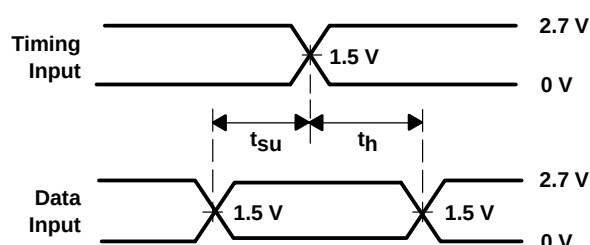
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

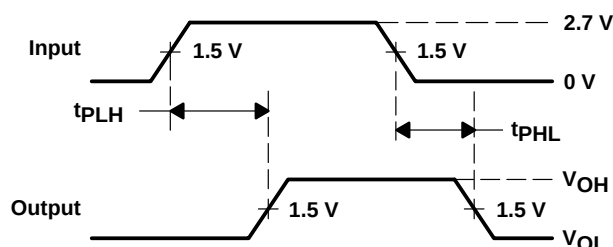


LOAD CIRCUIT

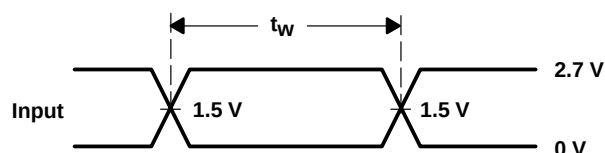
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



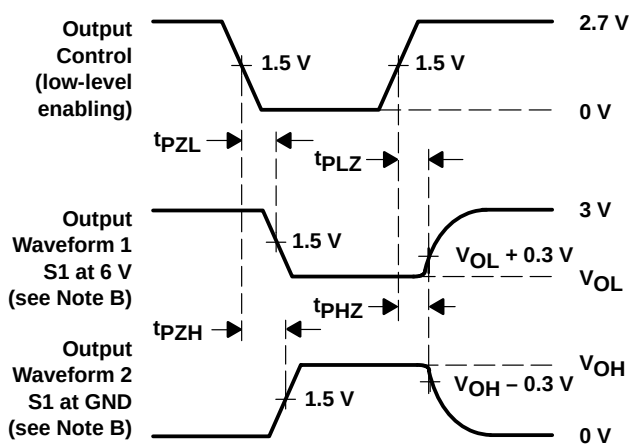
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

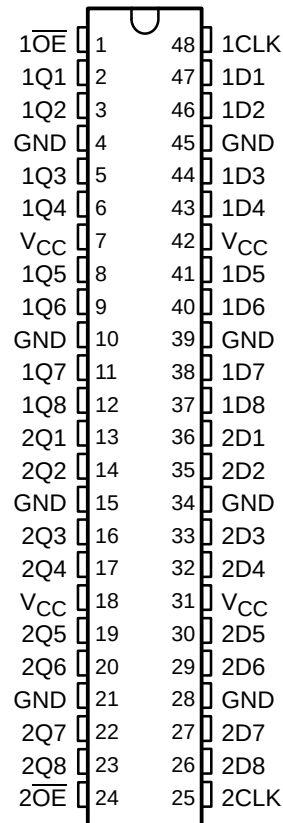
SN74LVCH16374A

16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input and Output Voltages With 3.3-V V_{CC})
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH16374A is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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description (continued)

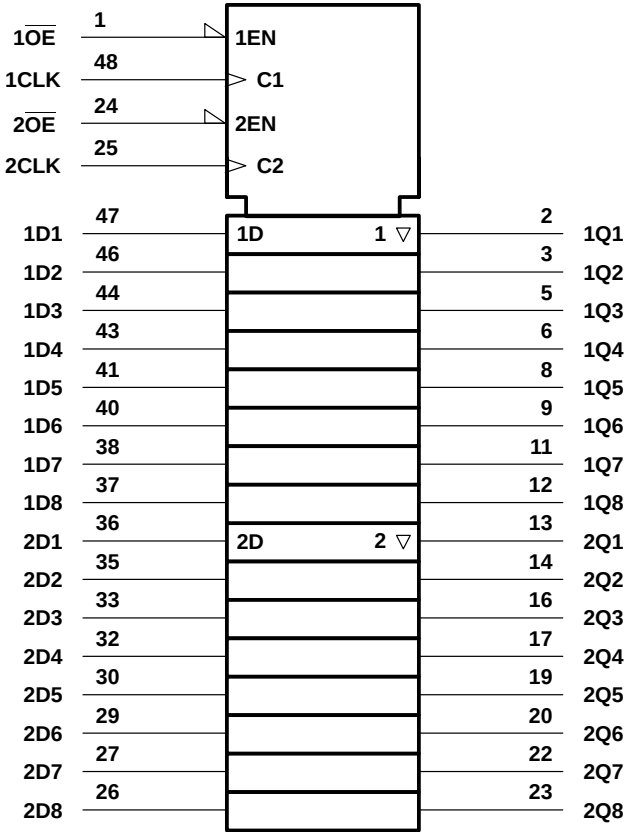
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH16374A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT Q
OE	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	Q ₀
H	X	X	Z

logic symbol†

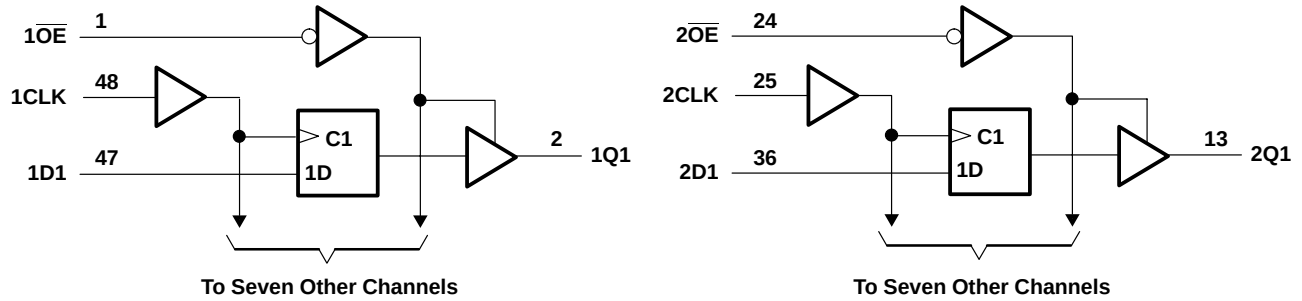


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{Stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.



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16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	High or low state	0	V _{CC}	V
		3 state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V	−4		mA
		V _{CC} = 2.3 V	−8		
		V _{CC} = 2.7 V	−12		
		V _{CC} = 3 V	−24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		mA
		V _{CC} = 2.3 V	8		
		V _{CC} = 2.7 V	12		
		V _{CC} = 3 V	24		
Δt/Δv	Input transition rise or fall rate	0	10	ns/V	
T _A	Operating free-air temperature	−40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 4 mA	1.65 V	0.45			
	I _{OL} = 8 mA	2.3 V	0.7			
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _I (hold)	V _I = 0.58 V	1.65 V	‡			µA
	V _I = 1.07 V		‡			
	V _I = 0.7 V	2.3 V	45			
	V _I = 1.7 V		–45			
	V _I = 0.8 V	3 V	75			
	V _I = 2 V		–75			
	V _I = 0 to 3.6 V [§]	3.6 V			±500	
I _{off}	V _I or V _O = 5.5 V	0			±10	µA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V			±10	µA
I _{CC}	V _I = V _{CC} or GND	3.6 V			20	µA
	3.6 V ≤ V _I ≤ 5.5 V [¶]				20	
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	V _I = V _{CC} or GND	3.3 V			5	pF
C _O	V _O = V _{CC} or GND	3.3 V			6.5	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This information was not available at the time of publication.

[§] This is the bus-hold maximum dynamic current required to switch the input from one state to another.

[¶] This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		‡		‡		150		150	MHz
t _w	Pulse duration, CLK high or low		‡		‡		3.3		3.3	ns
t _{su}	Setup time, data before CLK↑		‡		‡		1.9		1.9	ns
t _h	Hold time, data after CLK↑		‡		‡		1.1		1.1	ns

[‡] This information was not available at the time of publication.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		†		150		150		MHz
t _{pd}	CLK	Q	†	†	†	†	4.9		1.5	4.5	ns
t _{en}	$\overline{OE}$	Q	†	†	†	†	5.3		1.5	4.6	ns
t _{dis}	$\overline{OE}$	Q	†	†	†	†	6.1		1.5	5.5	ns
t _{sk(o)} [‡]									1		ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	f = 10 MHz	†	†	58	pF
		Outputs disabled		†	†	24	

† This information was not available at the time of publication.



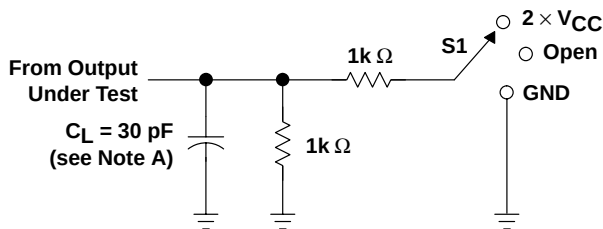
SN74LVCH16374A

16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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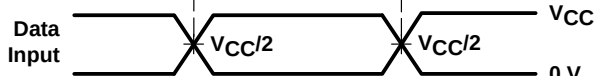
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

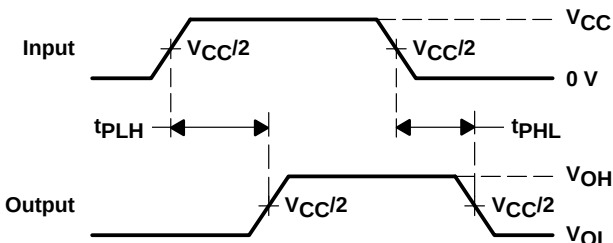


LOAD CIRCUIT

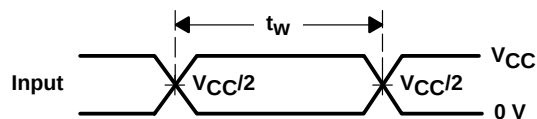
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



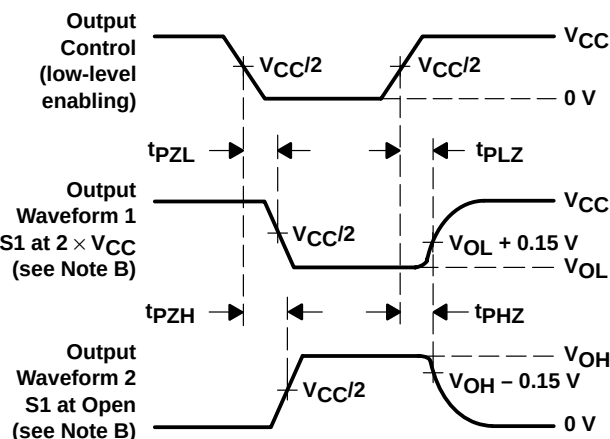
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVCH16374A

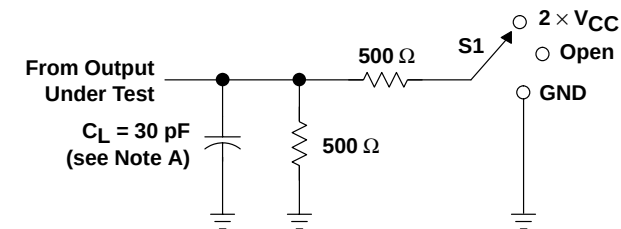
16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP

WITH 3-STATE OUTPUTS

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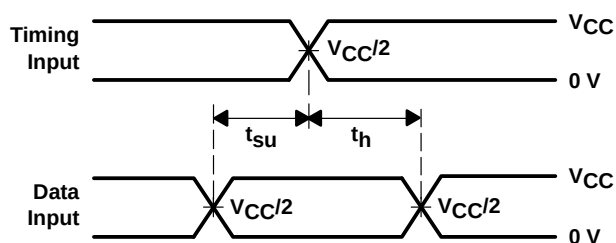
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

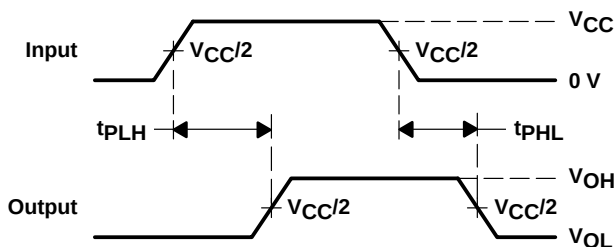


LOAD CIRCUIT

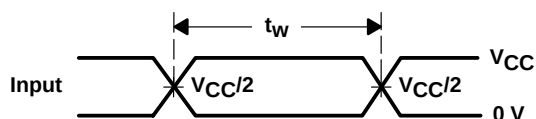
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



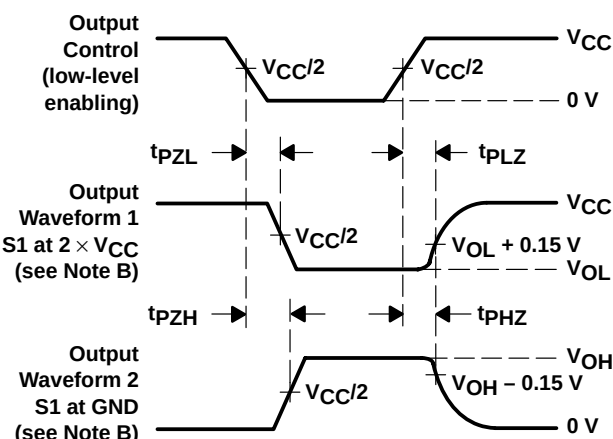
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

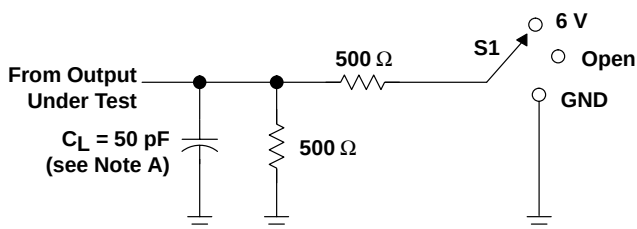
SN74LVCH16374A

16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS565F – MARCH 1996 – REVISED JUNE 1998

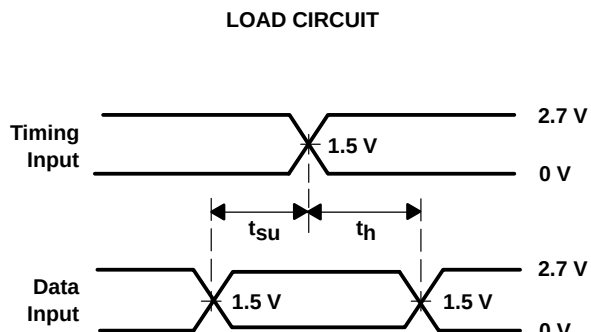
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$

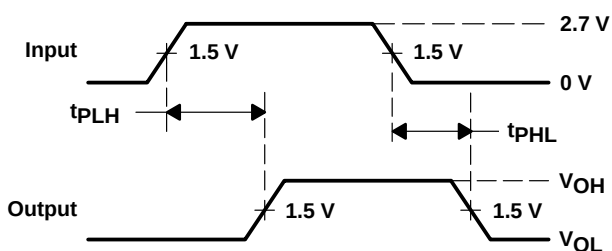


LOAD CIRCUIT

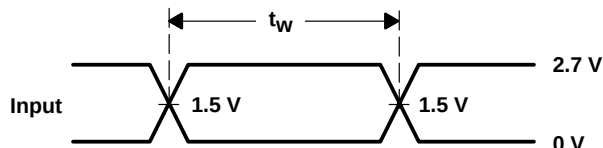
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



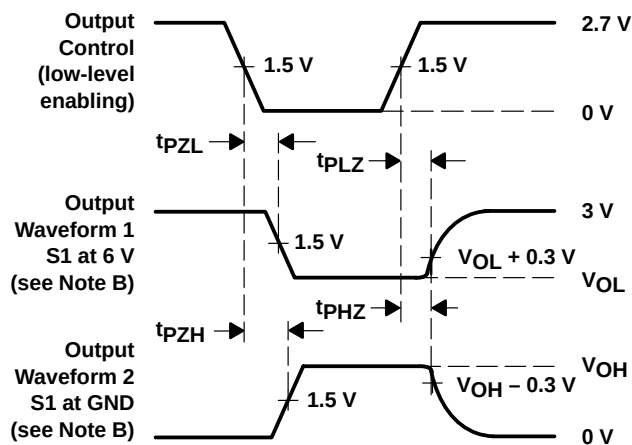
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN74LVCH16540A

16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS569G – MARCH 1996 – REVISED JUNE 1998

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Power Off Disables Outputs, Permitting Live Insertion
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin-Shrink Small-Outline (DGG) Packages

description

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation, and provides a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

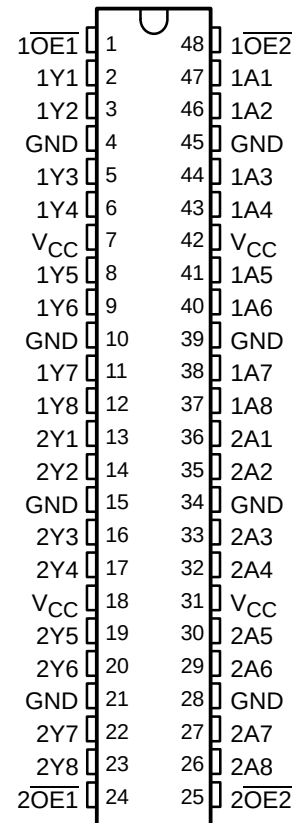
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH16540A is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



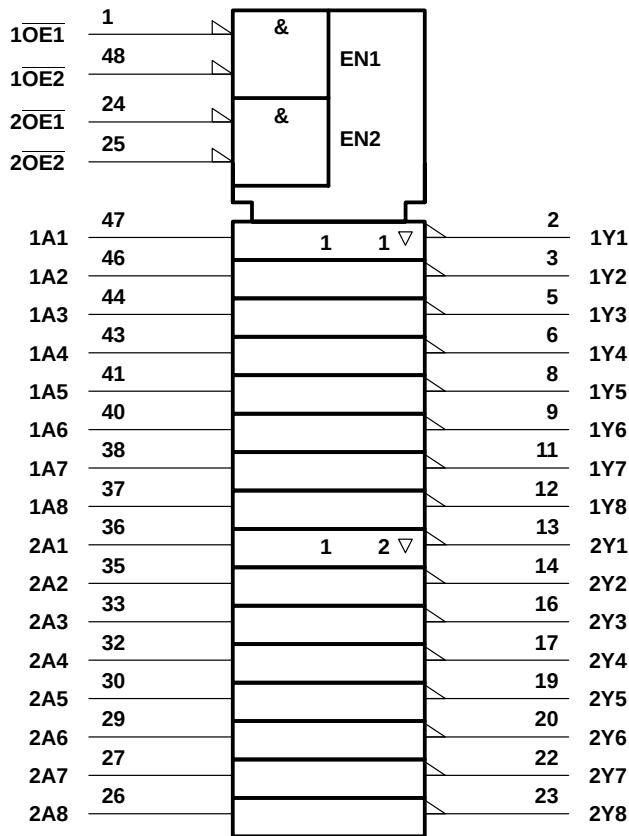
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FUNCTION TABLE
(each 8-bit section)

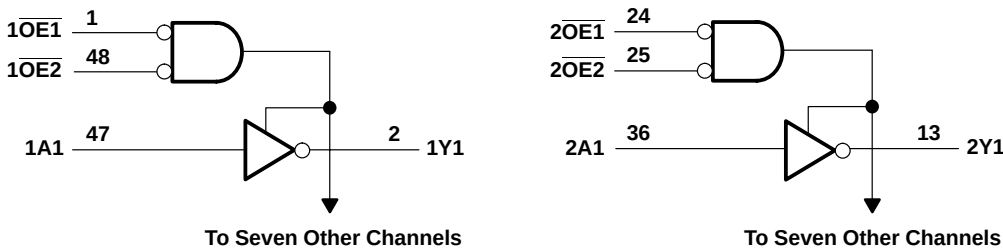
INPUTS			OUTPUT Y
OE1	OE2	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65 3.6	V
		Data retention only	1.5	
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 2.7 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 2.7 V to 3.6 V	0.8	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	High or low state	0 V _{CC}	V
		3 state	0 5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V	–4	mA
		V _{CC} = 2.3 V	–8	
		V _{CC} = 2.7 V	–12	
		V _{CC} = 3 V	–24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4	mA
		V _{CC} = 2.3 V	8	
		V _{CC} = 2.7 V	12	
		V _{CC} = 3 V	24	
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2			
	I _{OH} = –12 mA	3 V	2.4			
	I _{OH} = –24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 4 mA	1.65 V	0.45			
	I _{OL} = 8 mA	2.3 V	0.7			
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 0 to 5.5 V	3.6 V	±5			µA
I _I (hold)	V _I = 0.58 V	1.65 V	‡			µA
	V _I = 1.07 V		‡			
	V _I = 0.7 V	2.3 V	45			
	V _I = 1.7 V		–45			
	V _I = 0.8 V	3 V	75			
	V _I = 2 V		–75			
	V _I = 0 to 3.6 V [§]	3.6 V	±500			
I _{off}	V _I or V _O = 5.5 V	0	±10			µA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V	±10			µA
I _{CC}	V _I = V _{CC} or GND	3.6 V	20			µA
	3.6 V ≤ V _I ≤ 5.5 V [¶]		20			
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			µA
C _i	V _I = V _{CC} or GND	3.3 V	5			pF
C _O	V _O = V _{CC} or GND	3.3 V	6.5			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This information was not available at the time of publication.

[§] This is the bus-hold maximum dynamic current required to switch the input from one state to another.

[¶] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	‡	‡	‡	‡	4.5		1	3.7	ns
t _{en}	$\overline{\text{OE}}$	Y	‡	‡	‡	‡	5.9		1.5	4.8	ns
t _{dis}	$\overline{\text{OE}}$	Y	‡	‡	‡	‡	6.3		1.6	5.9	ns

[‡] This information was not available at the time of publication.



SN74LVCH16540A
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

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operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	†	†	34	pF
		Outputs disabled		†	†	2	

† This information was not available at the time of publication.



SN74LVCH16540A

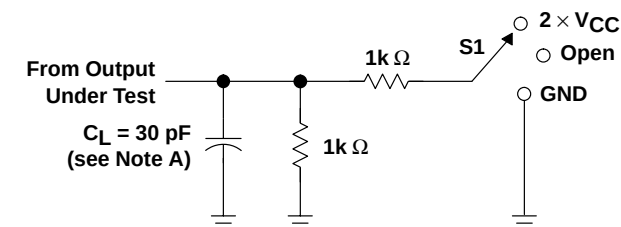
16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

SCAS569G – MARCH 1996 – REVISED JUNE 1998

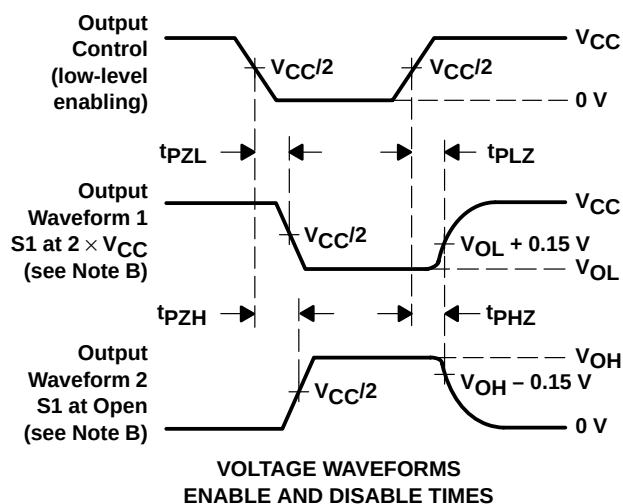
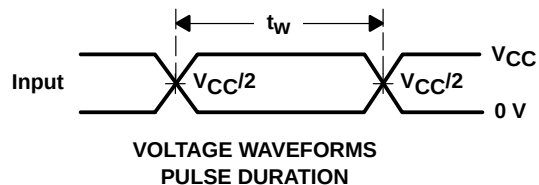
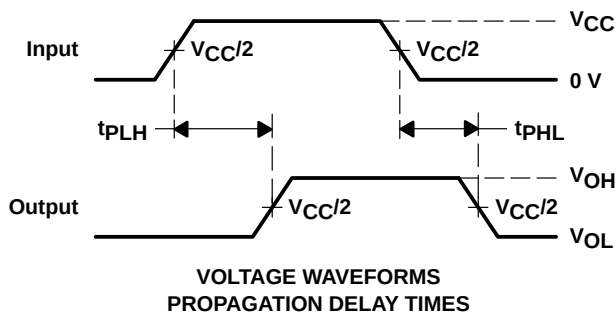
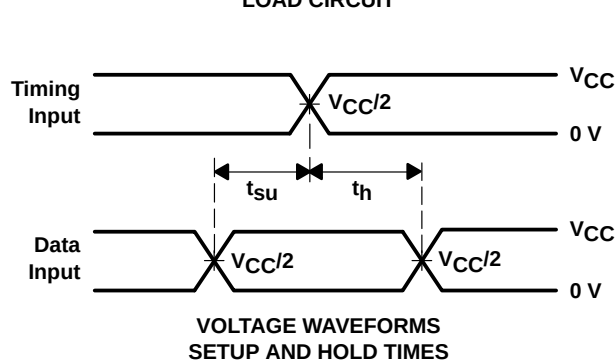
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	Open

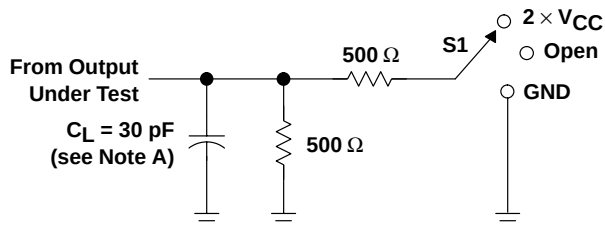


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

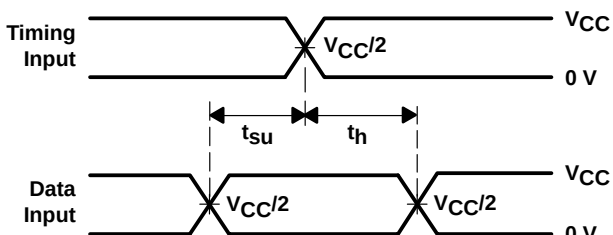
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

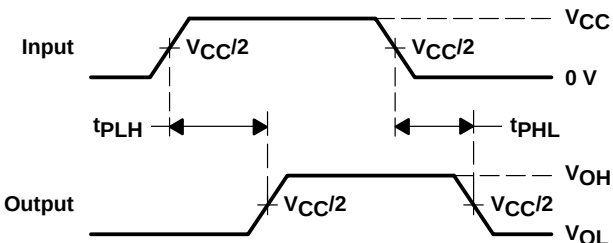


LOAD CIRCUIT

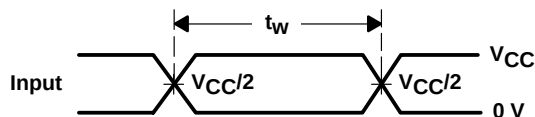
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



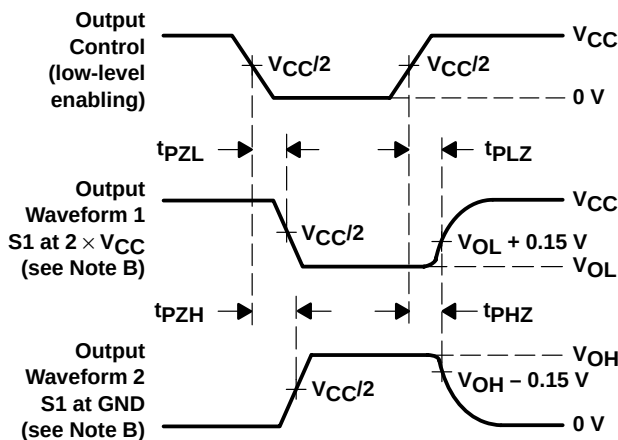
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN74LVCH16540A

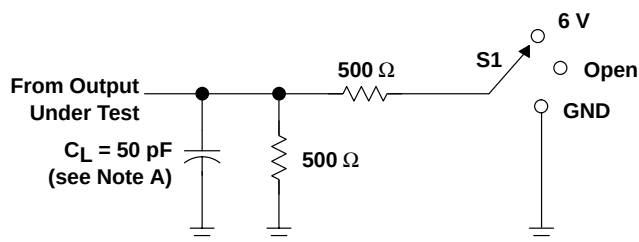
16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

SCAS569G – MARCH 1996 – REVISED JUNE 1998

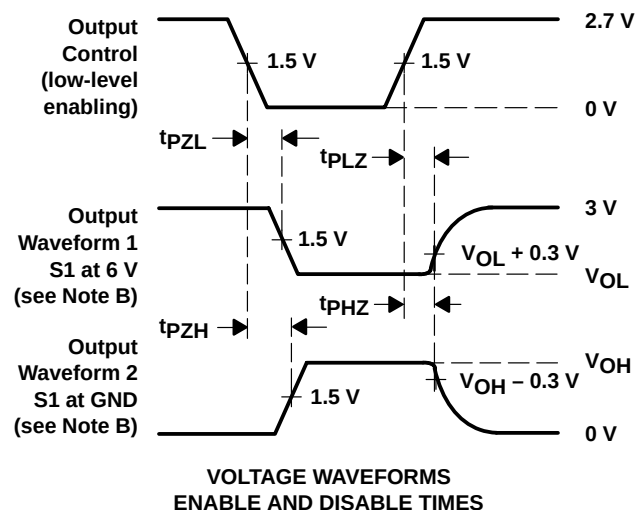
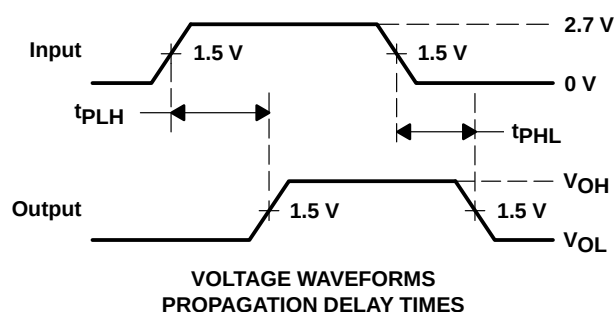
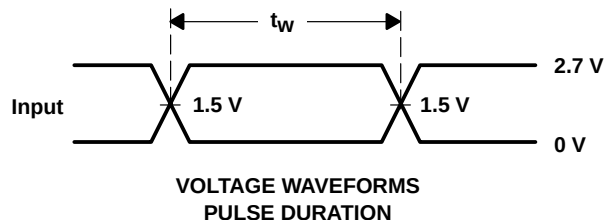
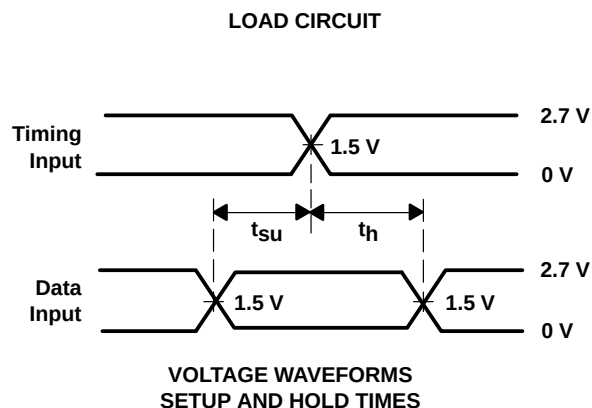
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

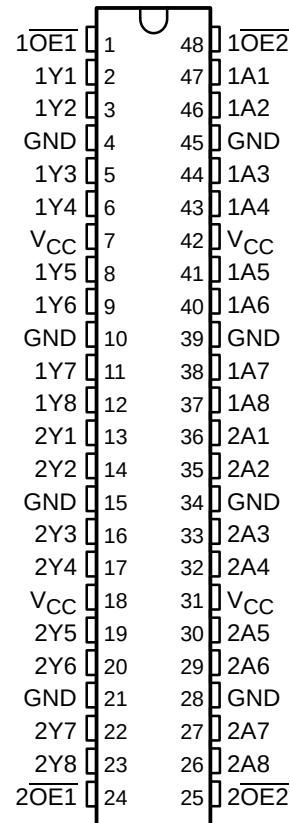
SN74LVCH16541A

16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS567G – MARCH 1996 – REVISED JUNE 1998

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Thin-Shrink Small-Outline (DGG) and Plastic 300-mil Shrink Small-Outline (DL) Packages

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH16541A is a noninverting 16-bit buffer composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable ($1\overline{OE}1$ and $1\overline{OE}2$ or $2\overline{OE}1$ and $2\overline{OE}2$) inputs must be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH16541A is characterized for operation from -40°C to 85°C .

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



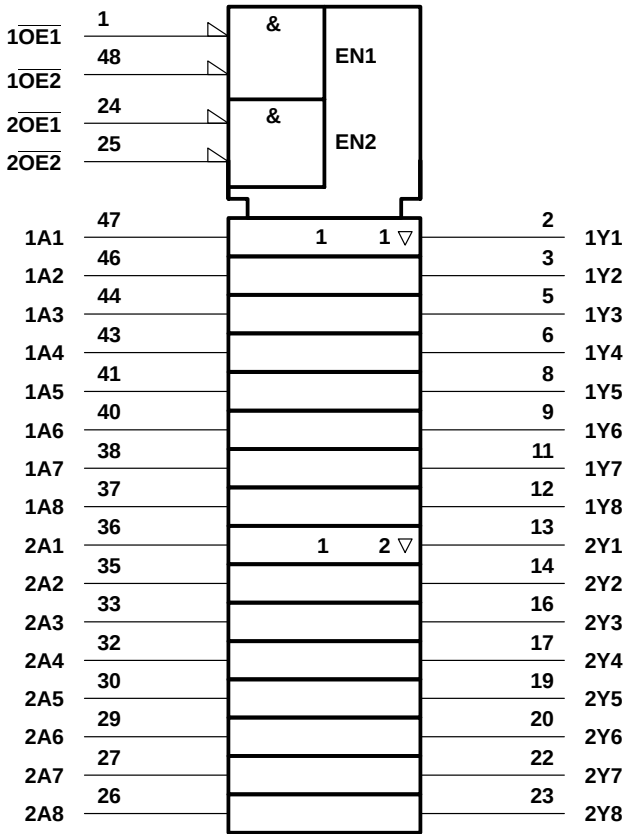
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FUNCTION TABLE
(each 8-bit section)

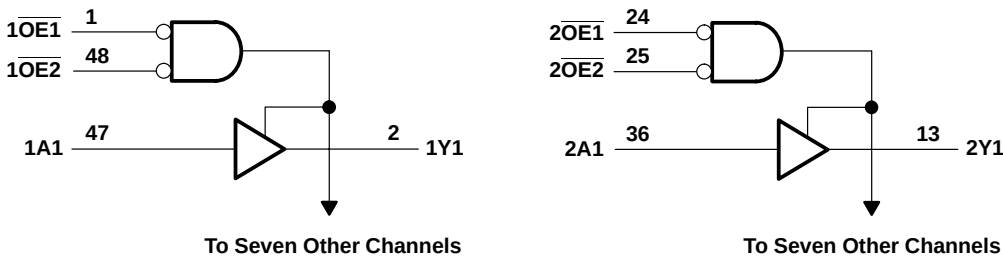
INPUTS			OUTPUT Y
OE1	OE2	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.7			
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V			0.2	V
	I _{OL} = 4 mA	1.65 V			0.45	
	I _{OL} = 8 mA	2.3 V			0.7	
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _I (hold)	V _I = 0.58 V	1.65 V		‡		µA
	V _I = 1.07 V			‡		
	V _I = 0.7 V	2.3 V		45		
	V _I = 1.7 V			–45		
	V _I = 0.8 V	3 V		75		
	V _I = 2 V			–75		
	V _I = 0 to 3.6 V [§]	3.6 V			±500	
I _{off}	V _I or V _O = 5.5 V	0			±10	µA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V			±10	µA
I _{CC}	V _I = V _{CC} or GND	3.6 V	I _O = 0		20	µA
	3.6 V ≤ V _I ≤ 5.5 V [¶]				20	
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	V _I = V _{CC} or GND	3.3 V		5		pF
C _O	V _O = V _{CC} or GND	3.3 V		6.5		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This information was not available at the time of publication.

[§] This is the bus-hold maximum dynamic current required to switch the input from one state to another.

[¶] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	‡	‡	‡	‡	5		1.1	4.2	ns
t _{en}	$\overline{\text{OE}}$	Y	‡	‡	‡	‡	6.9		1.5	5.6	ns
t _{dis}	$\overline{\text{OE}}$	Y	‡	‡	‡	‡	7.4		1.9	6.8	ns

[‡] This information was not available at the time of publication.



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operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	†	†	35	pF
		Outputs disabled		†	†	4	

† This information was not available at the time of publication.



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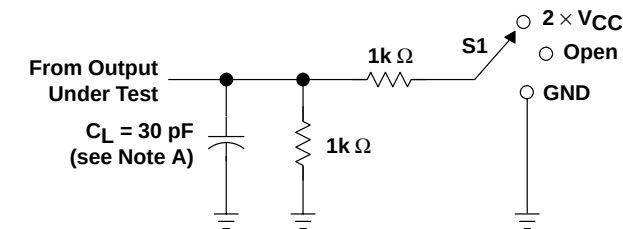
16-BIT BUFFER/DRIVER

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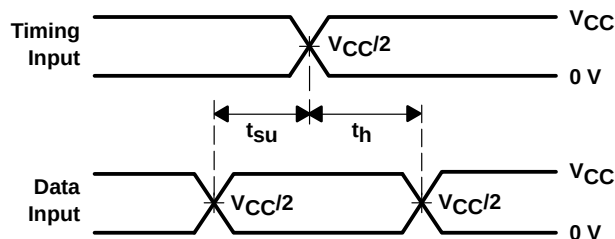
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

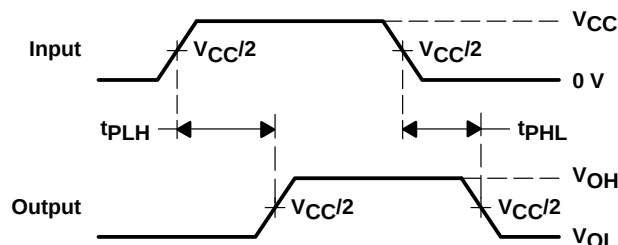


LOAD CIRCUIT

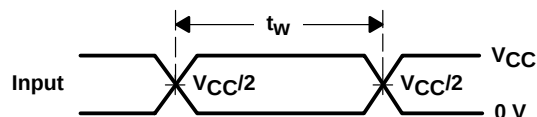
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



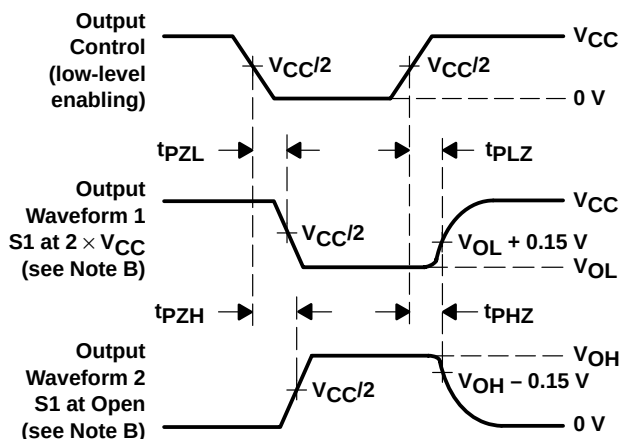
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



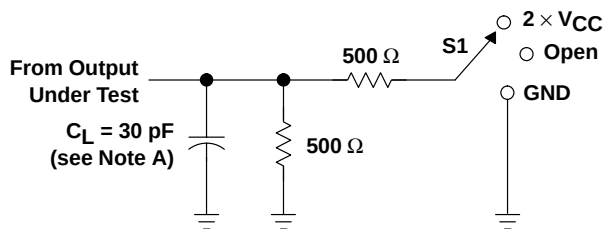
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

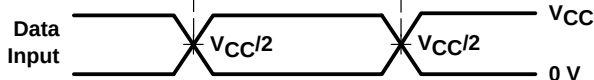
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

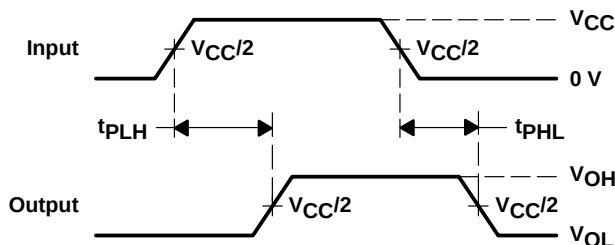


LOAD CIRCUIT

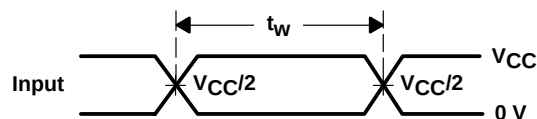
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



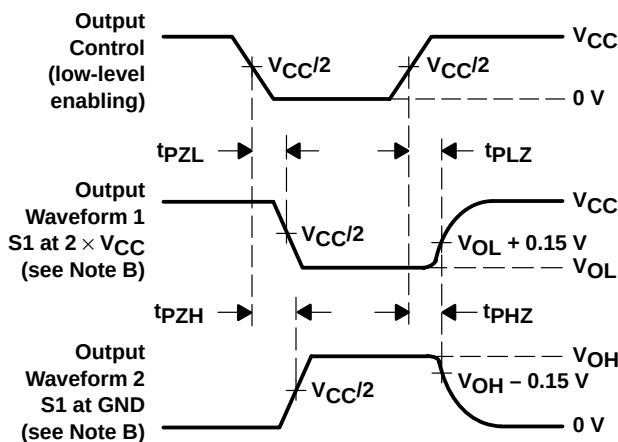
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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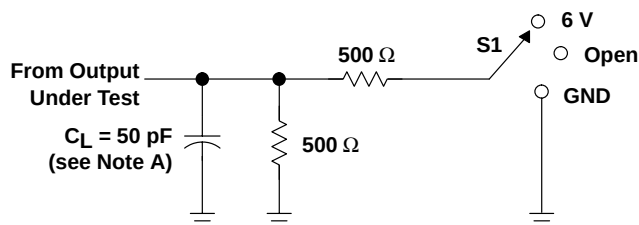
16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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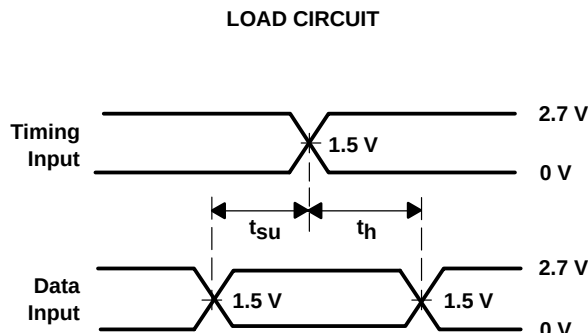
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

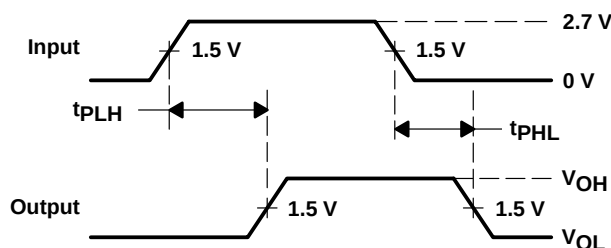


LOAD CIRCUIT

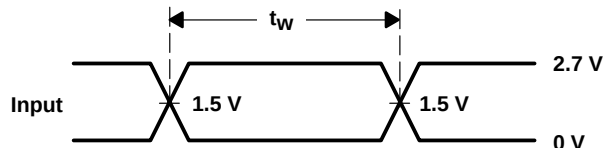
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



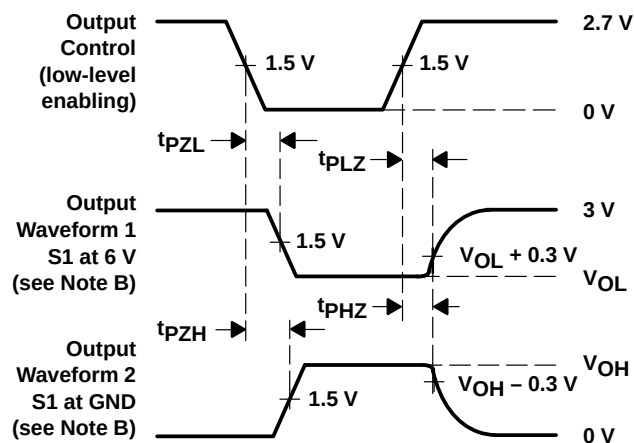
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- OTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

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16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

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- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit registered transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH16543A can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

DGG OR DL PACKAGE
(TOP VIEW)

$\overline{1OEAB}$	1	56	$\overline{1OEBA}$
$\overline{1LEAB}$	2	55	$\overline{1LEBA}$
$\overline{1CEAB}$	3	54	$\overline{1CEBA}$
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
$\overline{2CEAB}$	26	31	$\overline{2CEBA}$
$\overline{2LEAB}$	27	30	$\overline{2LEBA}$
$\overline{2OEAB}$	28	29	$\overline{2OEBA}$

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description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH16543A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE[†]
(each 8-bit section)

INPUTS				OUTPUT B
CEAB	LEAB	OEAB	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B ₀ [‡]
L	L	L	L	L
L	L	L	H	H

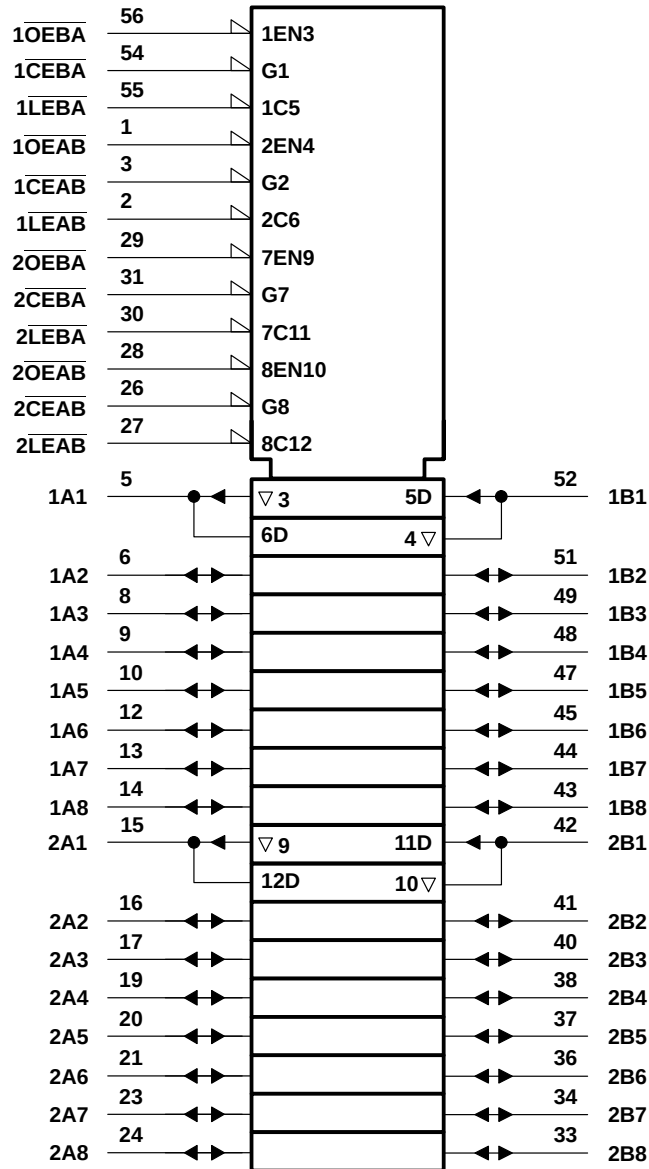
[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.

[‡] Output level before the indicated steady-state input conditions were established

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logic symbol[†]



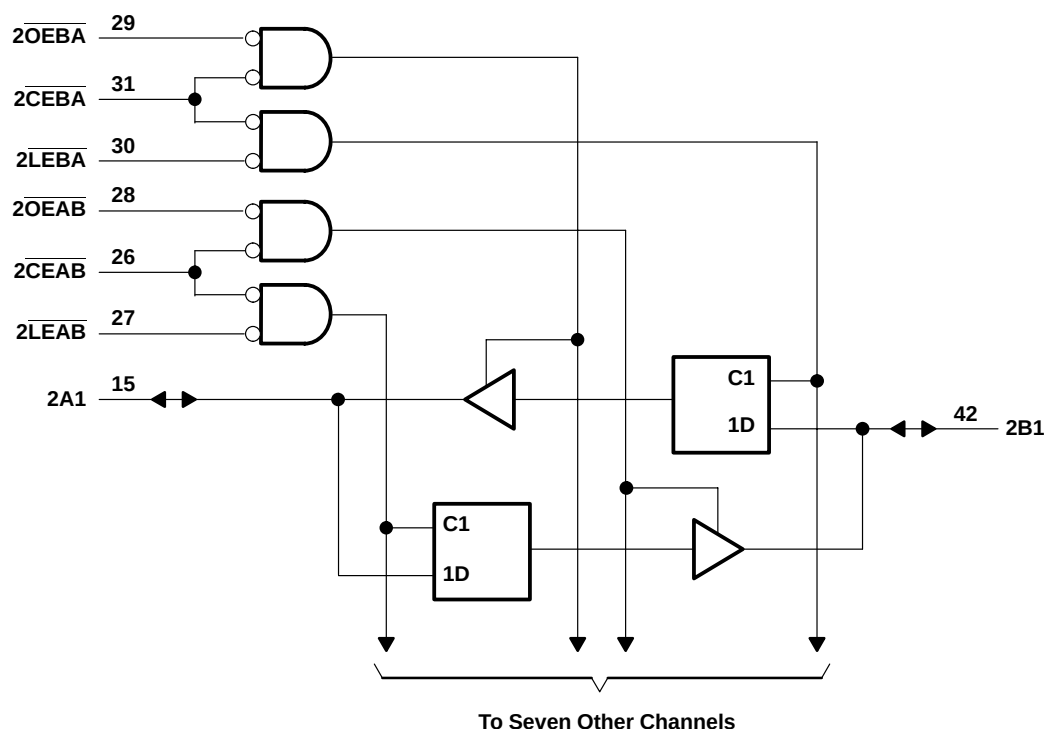
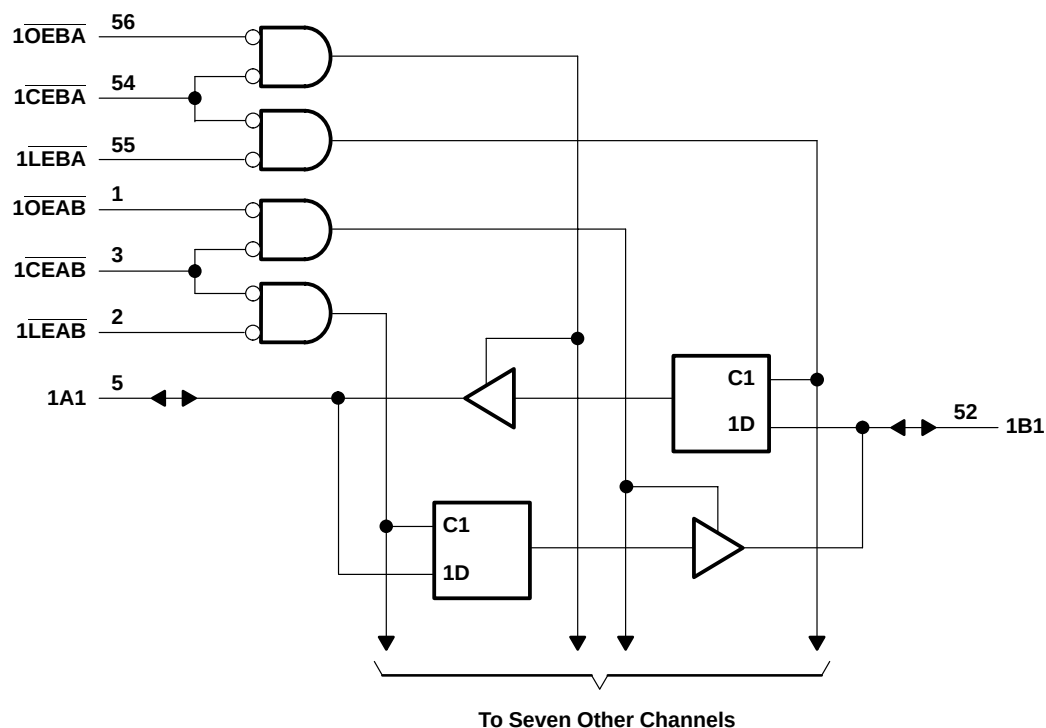
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I : (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}			I _{OH} = −100 μA	1.65 V to 3.6 V	V _{CC} −0.2			V
			I _{OH} = −4 mA	1.65 V	1.2			
			I _{OH} = −8 mA	2.3 V	1.7			
			I _{OH} = −12 mA	2.7 V	2.2			
				3 V	2.4			
			I _{OH} = −24 mA	3 V	2.2			
V _{OL}			I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
			I _{OL} = 4 mA	1.65 V			0.45	
			I _{OL} = 8 mA	2.3 V			0.7	
			I _{OL} = 12 mA	2.7 V			0.4	
			I _{OL} = 24 mA	3 V			0.55	
I _I	Control inputs	V _I = 0 to 5.5 V		3.6 V			±5	μA
I _{off}		V _I or V _O = 5.5 V		0			±10	μA
I _{I(hold)}	A or B ports	V _I = 0.58 V		1.65 V	‡			μA
		V _I = 1.07 V			‡			
		V _I = 0.7 V		2.3 V	45			
		V _I = 1.7 V			−45			
		V _I = 0.8 V		3 V	75			
		V _I = 2 V			−75			
		V _I = 0 to 3.6 V [§]		3.6 V	±500			
I _{OZ} [¶]		V _O = 0 to 5.5 V		3.6 V			±10	μA
I _{CC}		V _I = V _{CC} or GND		3.6 V			20	μA
		3.6 V ≤ V _I ≤ 5.5 V [#]					20	
ΔI _{CC}		One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V			500	μA
C _i	Control inputs	V _I = V _{CC} or GND		3.3 V			5	pF
C _{io}	A or B ports	V _O = V _{CC} or GND		3.3 V			8	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This information was not available at the time of publication.

[§] This is the bus-hold maximum dynamic current required to switch the input from one state to another.

[¶] For I/O ports, the parameter I_{OZ} includes the input leakage current, but not I_{I(hold)}.

[#] This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, $\overline{\text{LE}}$ or $\overline{\text{CE}}$ low	‡		‡		3.3		3.3		ns
t _{su}	Setup time, data before $\overline{\text{LE}}$ or $\overline{\text{CE}}$ ↓	‡		‡		1.1		1.1		ns
t _h	Hold time, data after $\overline{\text{LE}}$ or $\overline{\text{CE}}$ ↓	‡		‡		1.9		1.9		ns

[‡] This information was not available at the time of publication.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	†	†	†	†	6.1		1.2	5.4	ns
	$\overline{LE}$	A or B	†	†	†	†	7.4		1.5	6.1	
t_{en}	$\overline{CE}$	A or B	†	†	†	†	7.9		1.2	6.6	ns
t_{dis}			†	†	†	†	7.1		1.5	6.6	
t_{en}	$\overline{OE}$	A or B	†	†	†	†	7.6		1	6.3	ns
t_{dis}			†	†	†	†	6.9		1.5	6.3	

† This information was not available at the time of publication.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$f = 10\text{ MHz}$	†	†	44	pF
		Outputs disabled		†	†	4	

† This information was not available at the time of publication.

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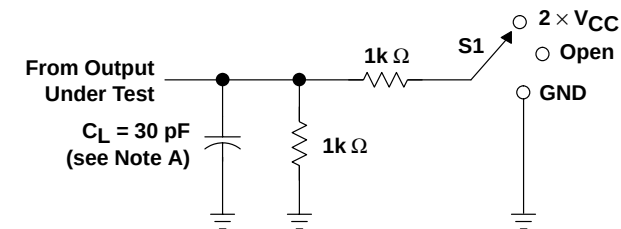
16-BIT REGISTERED TRANSCEIVER

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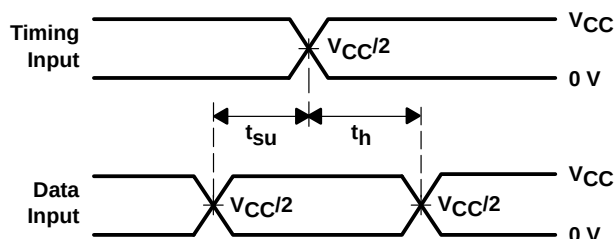
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

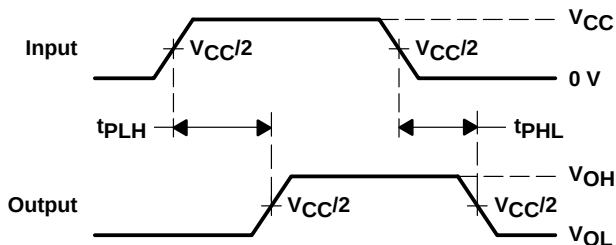


LOAD CIRCUIT

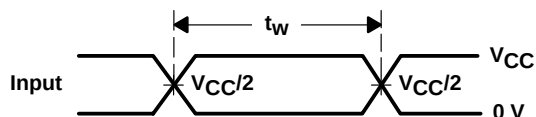
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



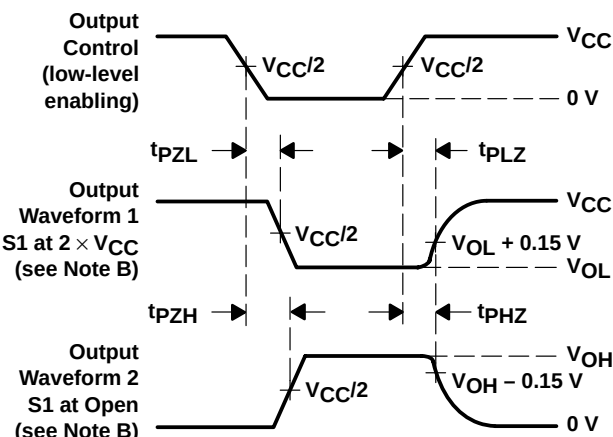
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



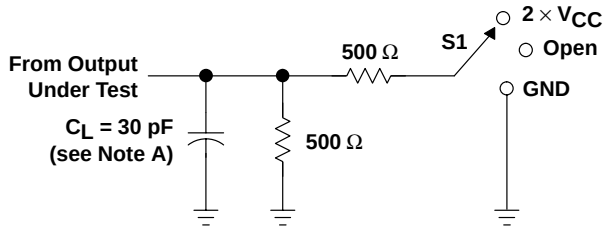
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

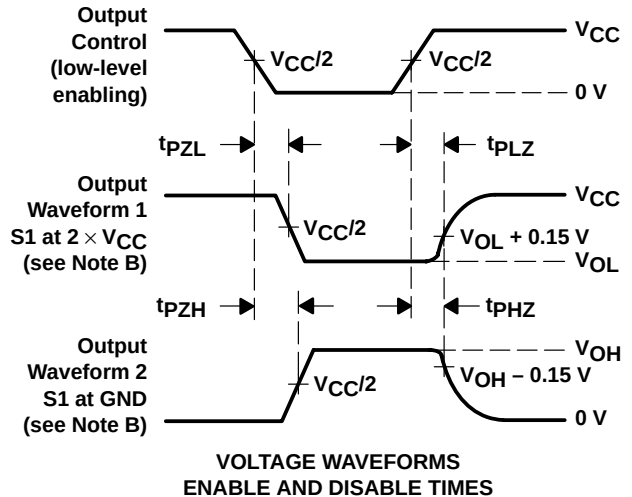
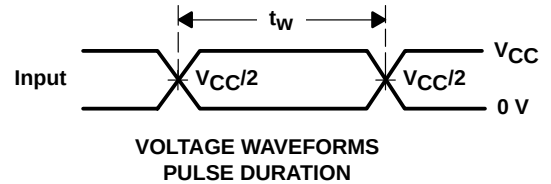
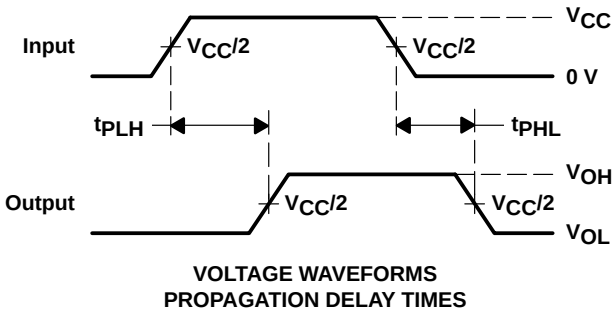
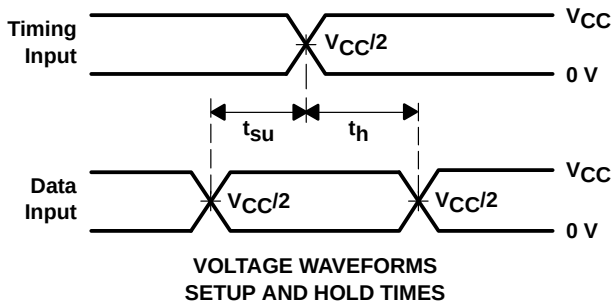
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PHZ}	GND



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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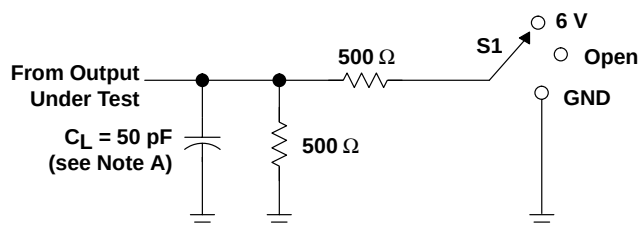
16-BIT REGISTERED TRANSCEIVER

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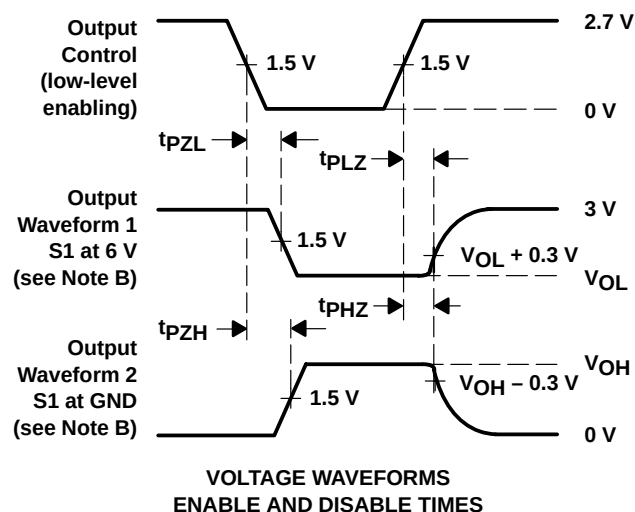
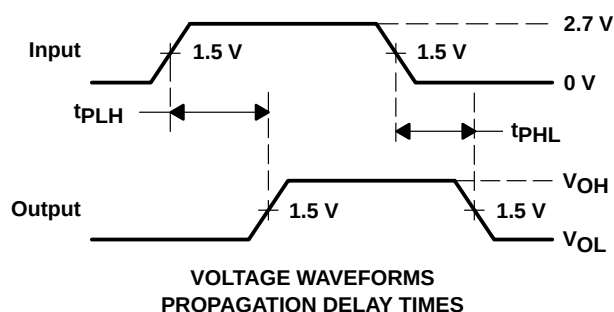
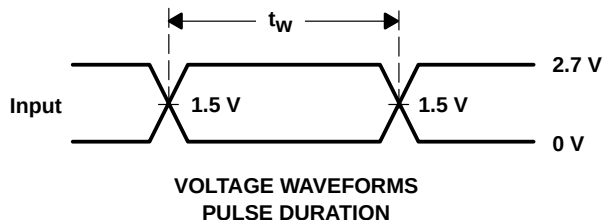
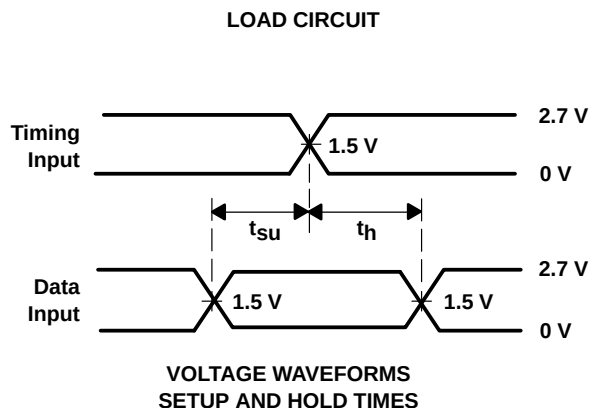
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

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- Member of the Texas Instruments *Widebus*™ Family
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Power Off Disables Outputs, Permitting Live Insertion
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit bus transceiver and register is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH16646A can be used as two 8-bit transceivers or one 16-bit transceiver. The device consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers.

Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVCH16646A.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data can be stored in one register and/or B data can be stored in the other register.

DGG OR DL PACKAGE
(TOP VIEW)

1DIR	1	56	$1\overline{OE}$
1CLKAB	2	55	1CLKBA
1SAB	3	54	1SBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2SAB	26	31	2SBA
2CLKAB	27	30	2CLKBA
2DIR	28	29	$2\overline{OE}$

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description (continued)

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.

The SN74LVCH16646A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS						DATA I/O [†]		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified	Store A, B unspecified [†]
X	X	X	↑	X	X	Unspecified	Input	Store B, A unspecified [†]
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A data to bus

[†] The data-output functions may be enabled or disabled by various signals at $\overline{OE}$ or DIR. Data-input functions always are enabled, i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

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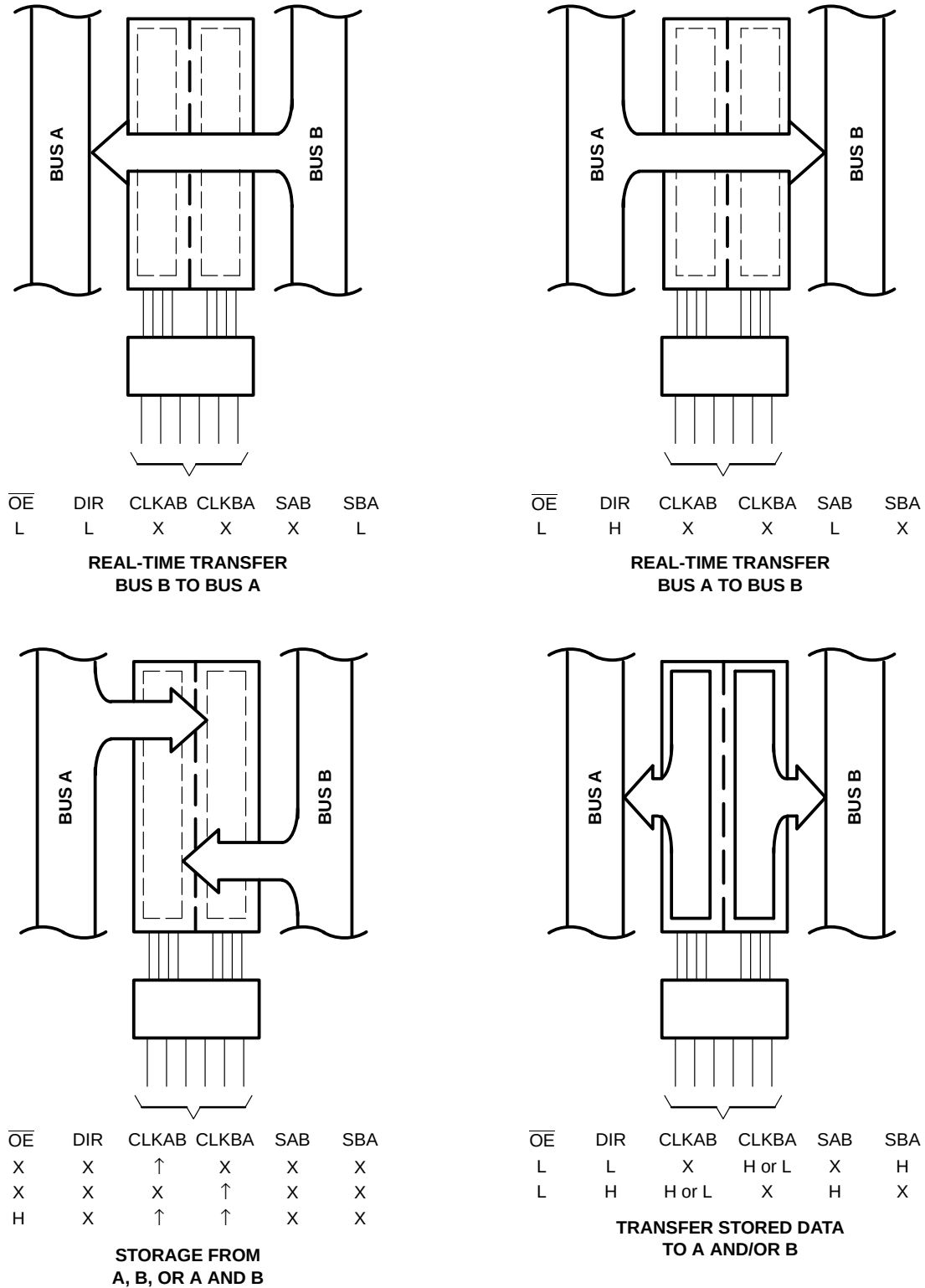


Figure 1. Bus-Management Functions

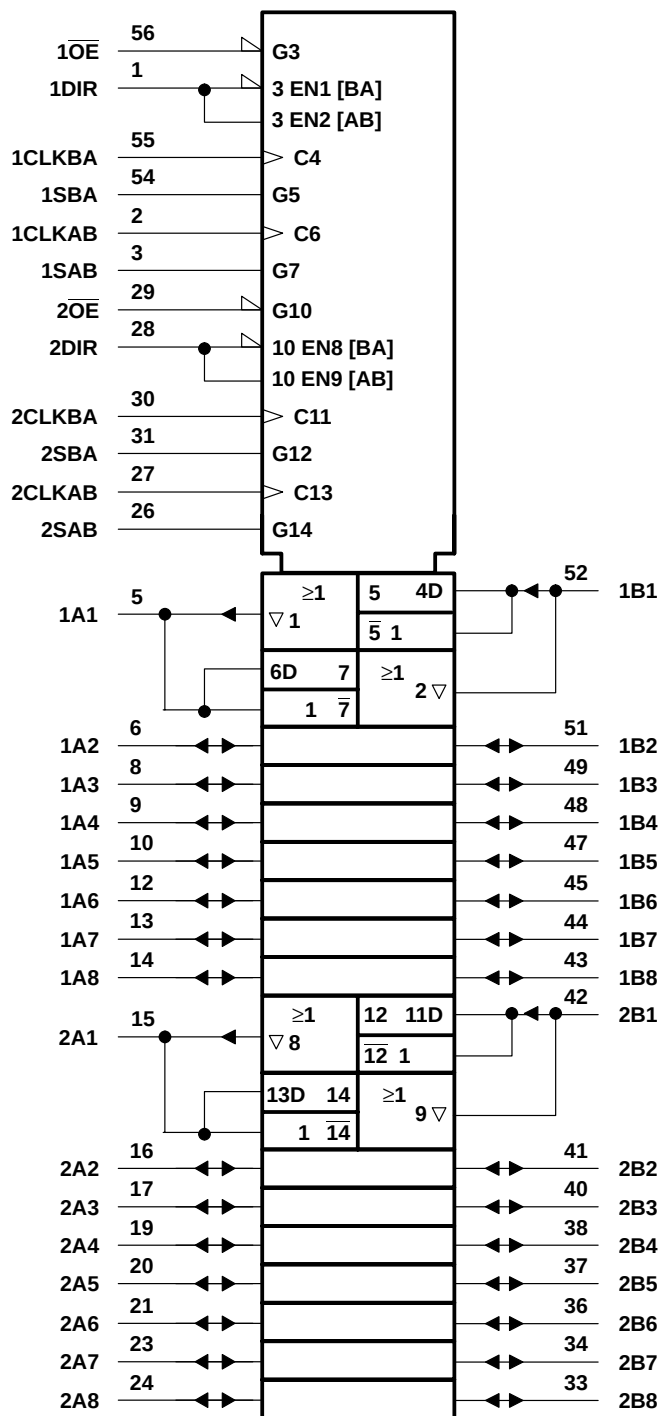
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logic symbol†

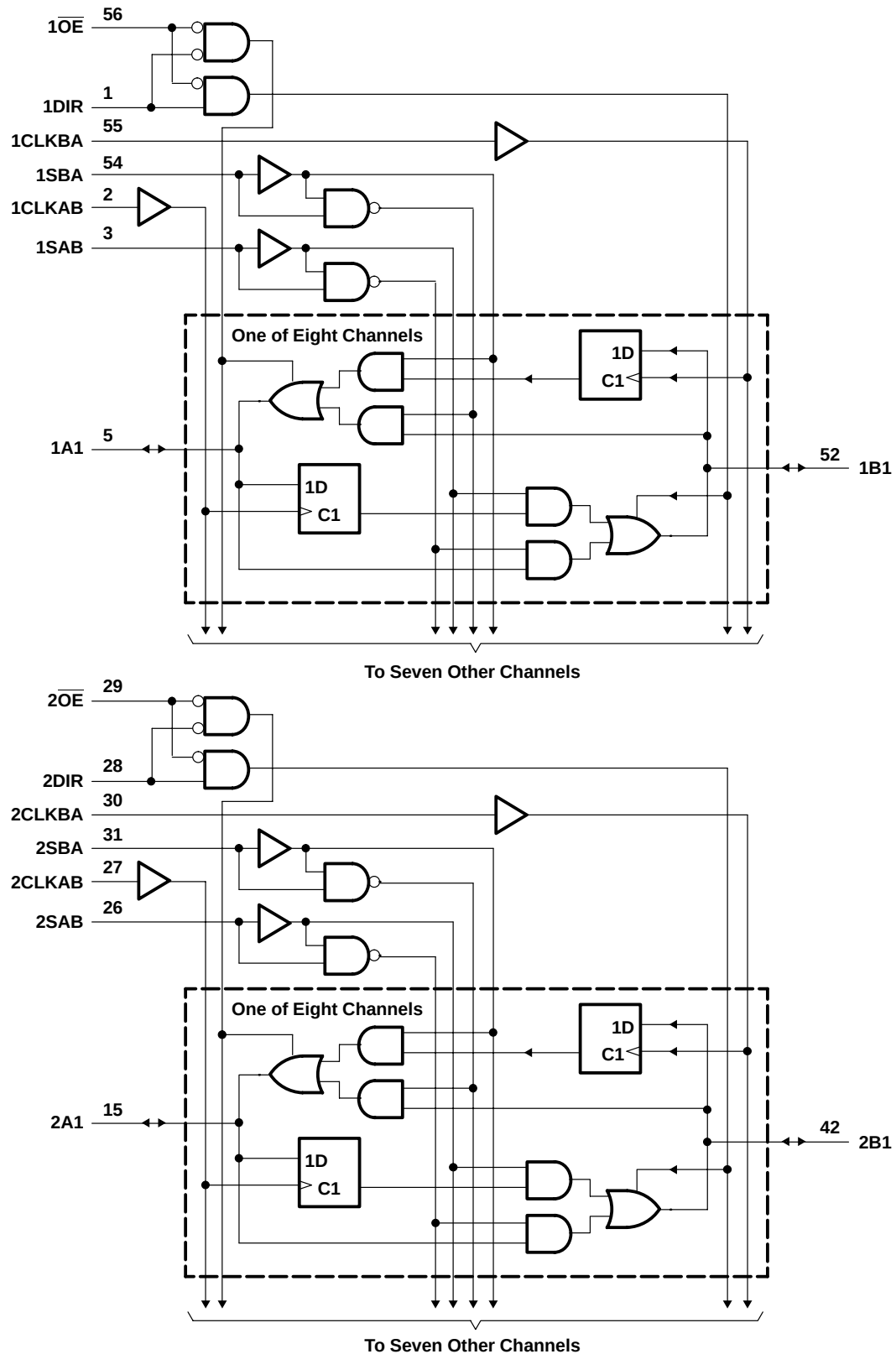


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I : (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}		I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
		I _{OH} = –4 mA	1.65 V	1.2			
		I _{OH} = –8 mA	2.3 V	1.7			
		I _{OH} = –12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = –24 mA	3 V	2.2			
V _{OL}		I _{OL} = 100 µA	1.65 V to 3.6 V			0.2	V
		I _{OL} = 4 mA	1.65 V			0.45	
		I _{OL} = 8 mA	2.3 V			0.7	
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _I (hold)	A or B ports	V _I = 0.58 V	1.65 V	‡			µA
		V _I = 1.07 V		‡			
		V _I = 0.7 V	2.3 V	45			
		V _I = 1.7 V		–45			
		V _I = 0.8 V	3 V	75			
		V _I = 2 V		–75			
		V _I = 0 to 3.6 V [§]	3.6 V			±500	
I _{off}		V _I or V _O = 5.5 V	0			±10	µA
I _{OZ} [¶]		V _O = 0 to 5.5 V	3.6 V			±10	µA
I _{CC}		V _I = V _{CC} or GND	3.6 V			20	µA
		3.6 V ≤ V _I ≤ 5.5 V [#]				20	
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V			5	pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V			8.5	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This information was not available at the time of publication.

[§] This is the bus-hold maximum dynamic current required to switch the input from one state to another.

[¶] For I/O ports, the parameter I_{OZ} includes the input leakage current, but not I_I(hold).

[#] This applies in the disabled state only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 2 through 4)

		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	‡		‡		150		150		MHz
t _w	Pulse duration, CLK high or low	‡		‡		3.3		3.3		ns
t _{su}	Setup time, A or B before CLKAB [↑] or CLKBA [↑]	‡		‡		3.2		2.9		ns
t _h	Hold time, A or B after CLKAB [↑] or CLKBA [↑]	‡		‡		0		0.3		ns

[‡] This information was not available at the time of publication.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			†		†		150		150		MHz
t_{pd}	A or B	B or A	†	†	†	†	6.8		1.3	5.7	ns
	CLKAB or CLKBA	A or B	†	†	†	†	7.9		1.8	6.7	
	SAB or SBA		†	†	†	†	9.2		1.7	7.7	
t_{en}	$\overline{OE}$	A or B	†	†	†	†	8.5		1.3	6.9	ns
t_{dis}			†	†	†	†	7.7		2.1	6.9	
t_{en}	DIR	A or B	†	†	†	†	8.5		1.4	7.2	ns
t_{dis}			†	†	†	†	7.8		2	7	

† This information was not available at the time of publication.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$f = 10\text{ MHz}$	†	†	60	pF
		Outputs disabled		†	†	12	

† This information was not available at the time of publication.

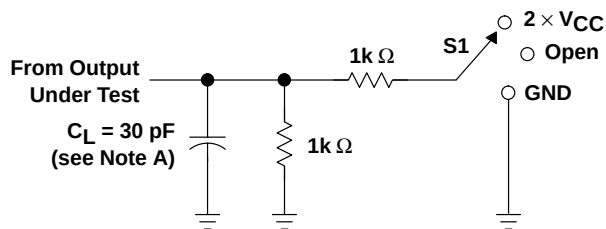
SN74LVCH16646A

16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS318H – NOVEMBER 1993 – REVISED JUNE 1998

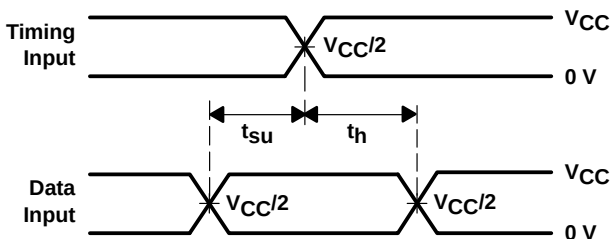
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

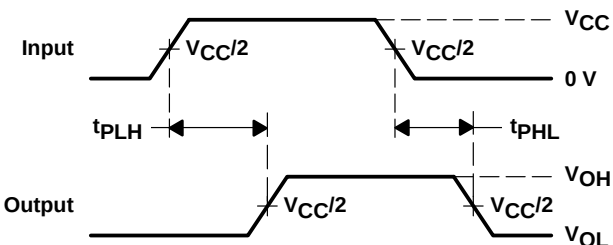


LOAD CIRCUIT

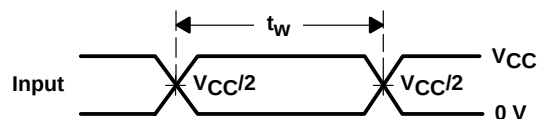
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



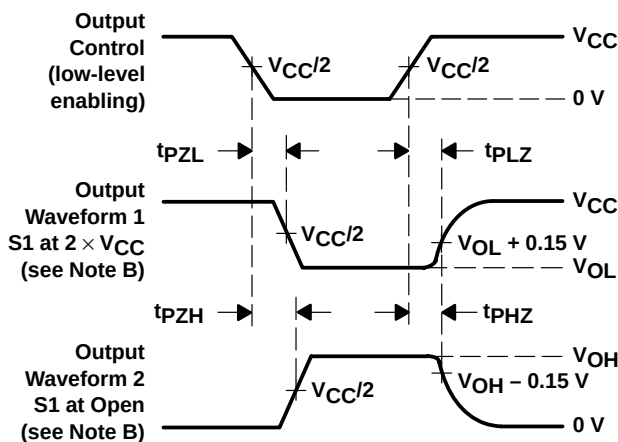
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN74LVCH16646A

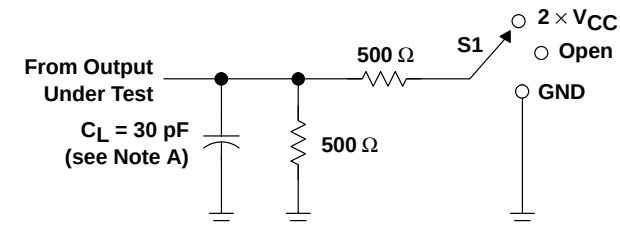
16-BIT BUS TRANSCEIVER AND REGISTER

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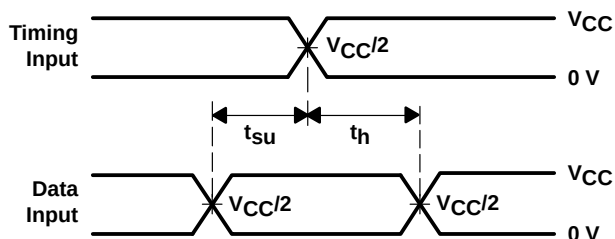
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

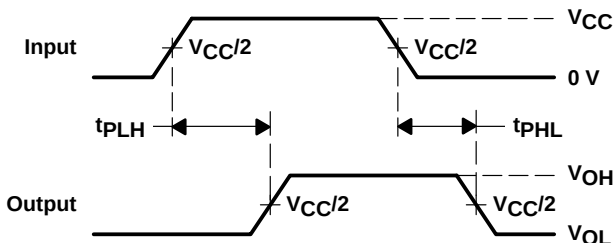


LOAD CIRCUIT

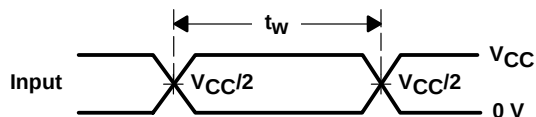
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHZ}	GND



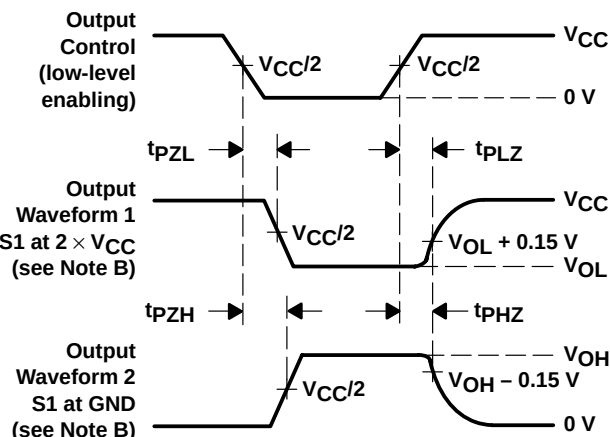
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



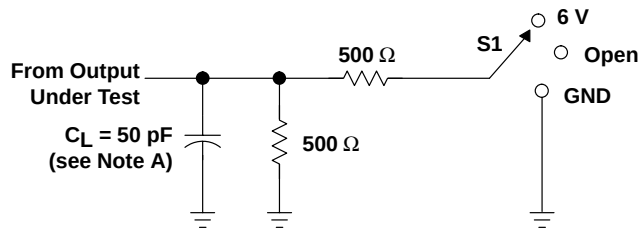
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

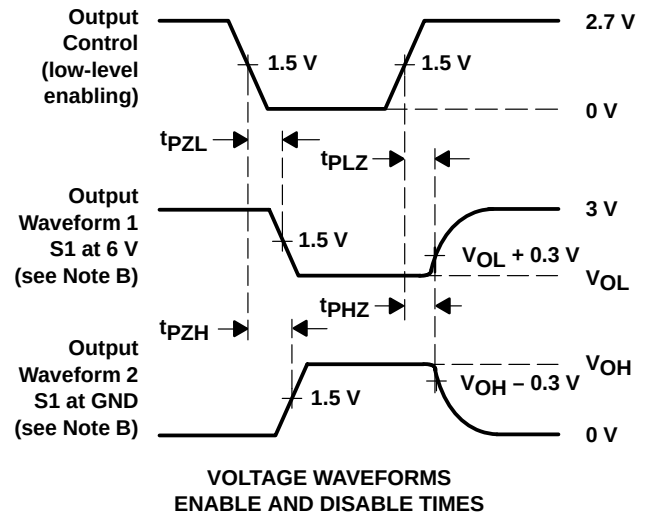
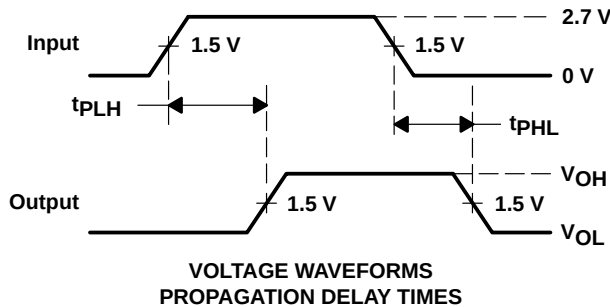
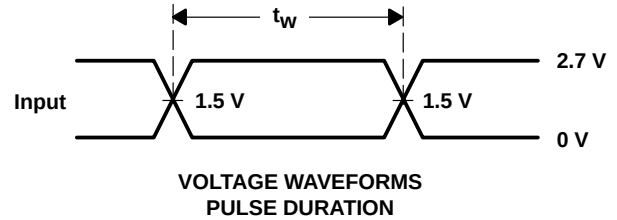
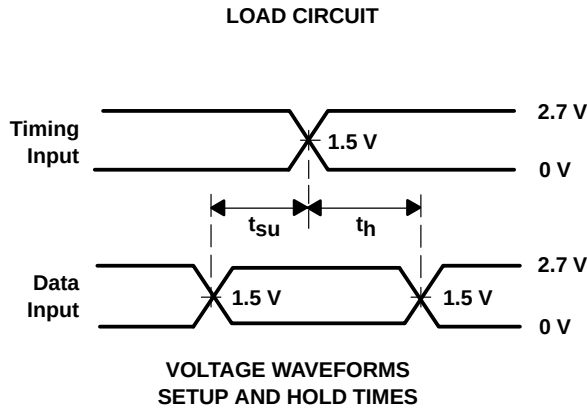
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 4. Load Circuit and Voltage Waveforms

SN74LVCH16652A 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

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- Member of the Texas Instruments *Widebus*™ Family
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit bus transceiver and register is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH16652A consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and $\overline{\text{OEBA}}$) inputs control the transceiver functions. Select-control (SAB and SBA) inputs select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVCH16652A.

DGG OR DL PACKAGE
(TOP VIEW)

1OEAB	1	56	$\overline{1\text{OEBA}}$
1CLKAB	2	55	1CLKBA
1SAB	3	54	1SBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2SAB	26	31	2SBA
2CLKAB	27	30	2CLKBA
2OEAB	28	29	$\overline{2\text{OEBA}}$

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description (continued)

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last level configuration.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.

The SN74LVCH16652A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS						DATA I/O [†]		OPERATION OR FUNCTION
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified [‡]	Store A, hold B
H	H	↑	↑	X [‡]	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified [‡]	Input	Hold A, store B
L	L	↑	↑	X	X [‡]	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

[†] The data-output functions may be enabled or disabled by a variety of level combinations at OEAB or $\overline{\text{OEBA}}$. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

[‡] Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered to load both registers.

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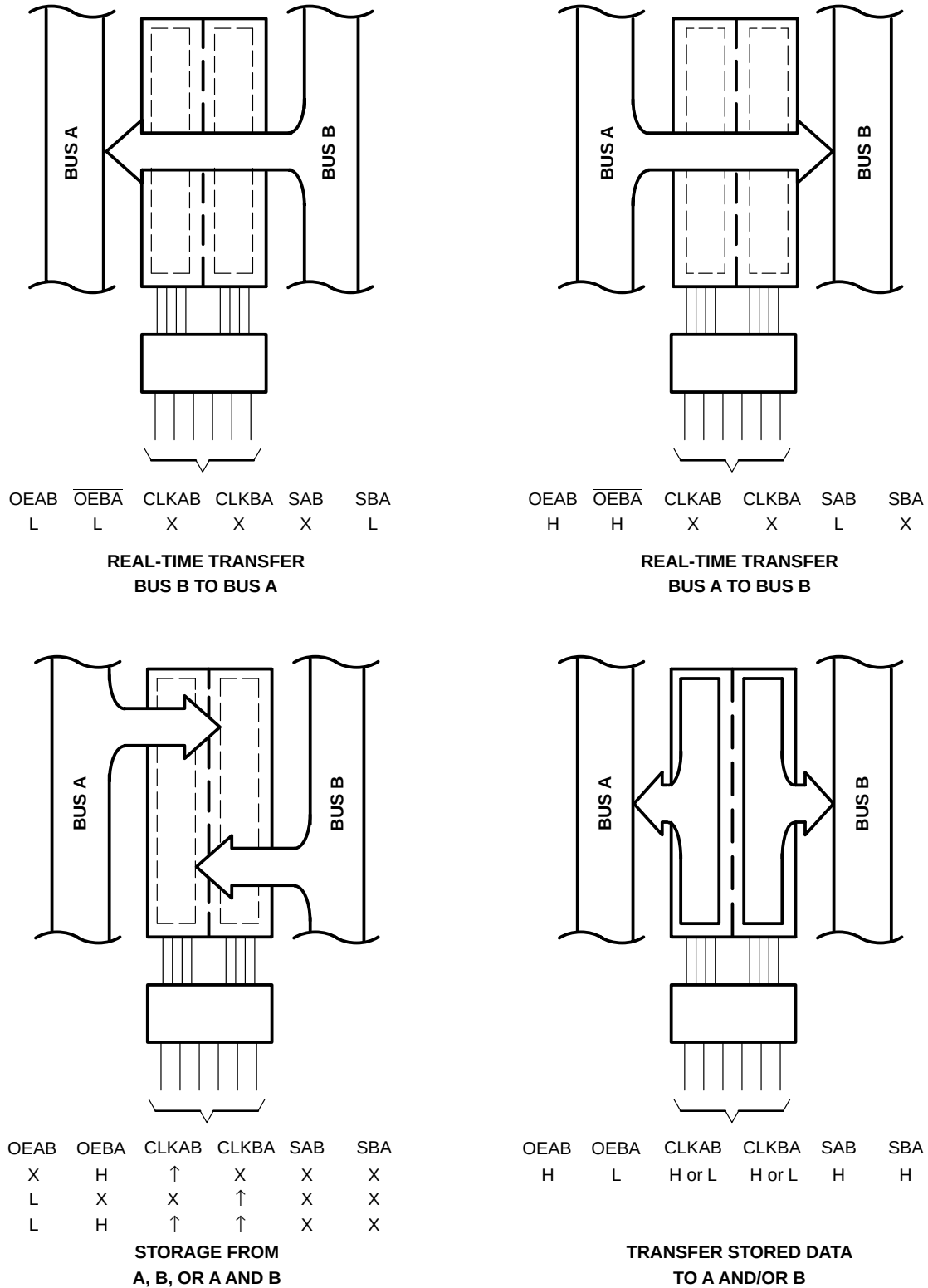


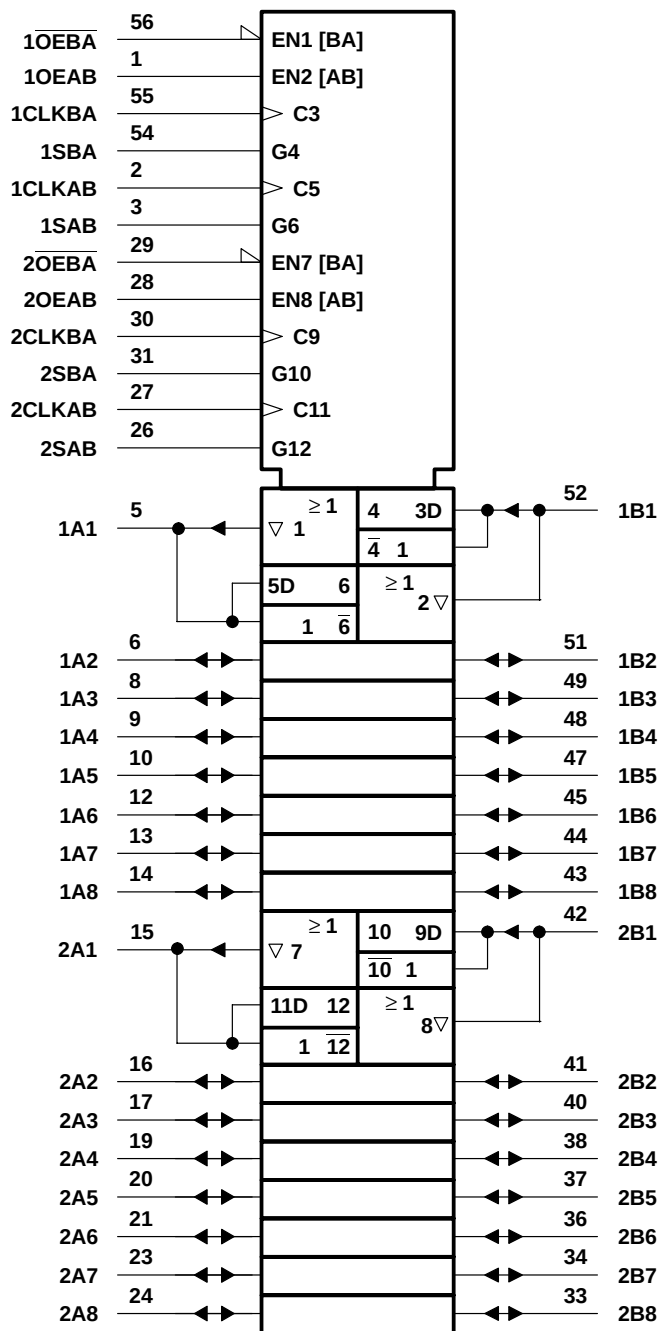
Figure 1. Bus-Management Functions

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logic symbol†

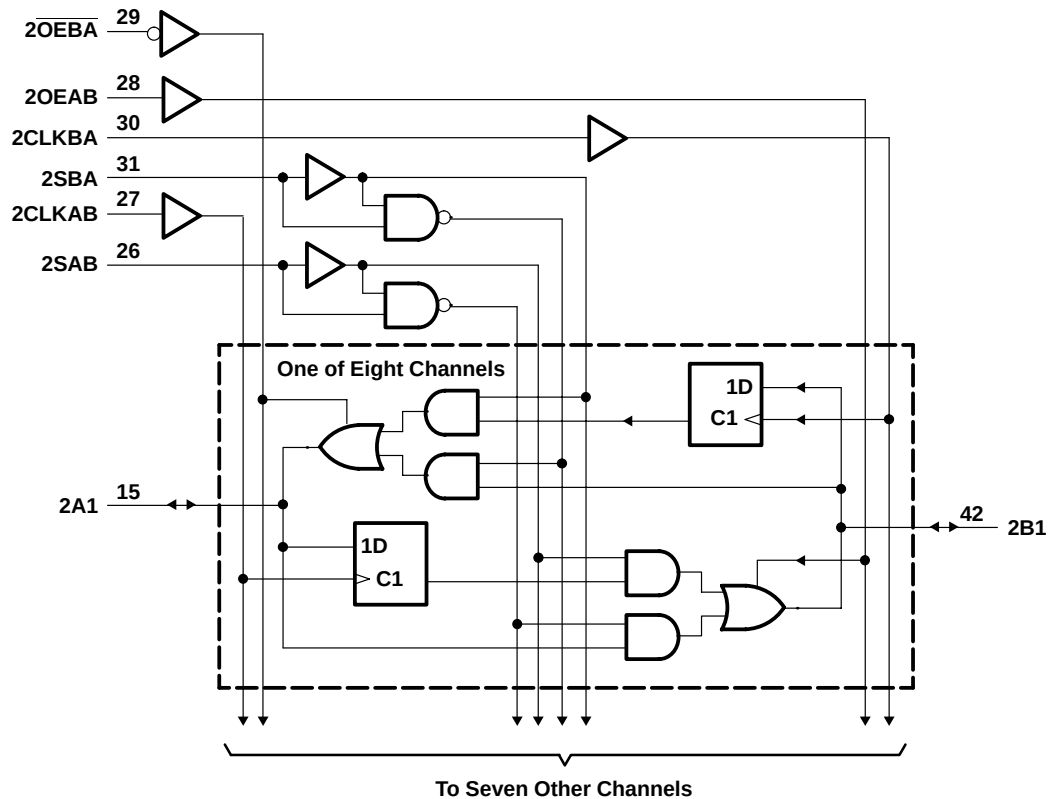
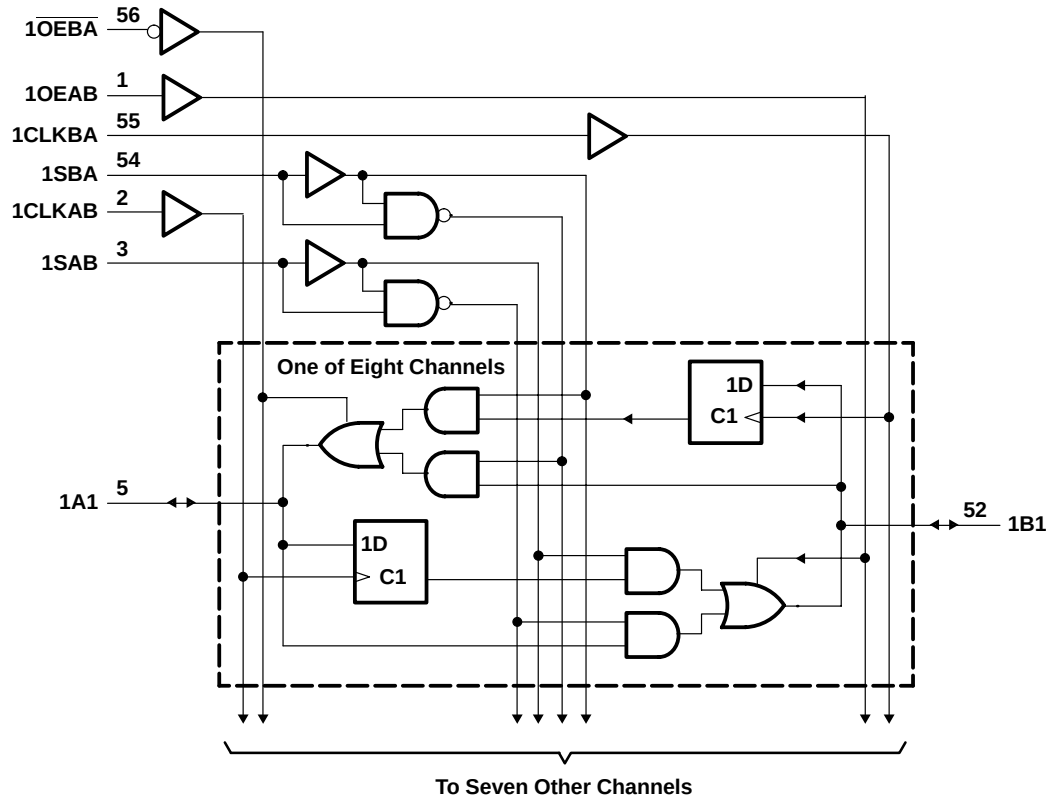


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I : (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}		I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
		I _{OH} = –4 mA	1.65 V	1.2			
		I _{OH} = –8 mA	2.3 V	1.7			
		I _{OH} = –12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = –24 mA	3 V	2.2			
V _{OL}		I _{OL} = 100 µA	1.65 V to 3.6 V			0.2	V
		I _{OL} = 4 mA	1.65 V			0.45	
		I _{OL} = 8 mA	2.3 V			0.7	
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _I (hold)	A or B ports	V _I = 0.58 V	1.65 V	‡			µA
		V _I = 1.07 V		‡			
		V _I = 0.7 V	2.3 V	45			
		V _I = 1.7 V		–45			
		V _I = 0.8 V	3 V	75			
		V _I = 2 V		–75			
		V _I = 0 to 3.6 V [§]	3.6 V			±500	
I _{off}		V _I or V _O = 5.5 V	0			±10	µA
I _{OZ} [¶]		V _O = 0 to 5.5 V	3.6 V			±10	µA
I _{CC}		V _I = V _{CC} or GND	3.6 V			20	µA
		3.6 V ≤ V _I ≤ 5.5 V [#]				20	
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V			5	pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V			8	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This information was not available at the time of publication.

[§] This is the bus-hold maximum dynamic current required to switch the input from one state to another.

[¶] For I/O ports, the parameter I_{OZ} includes the input leakage current, but not I_I(hold).

[#] This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 4)

		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	‡		‡		150		150		MHz
t _w	Pulse duration, CLK high or low	‡		‡		3.3		3.3		ns
t _{su}	Setup time, A or B before CLKAB [↑] or CLKBA [↑]	‡		‡		3.4		3		ns
t _h	Hold time, A or B after CLKAB [↑] or CLKBA [↑]	‡		‡		0		0.2		ns

[‡] This information was not available at the time of publication.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			†		†		150		150		MHz
t_{pd}	A or B	B or A	†	†	†	†	6.4		1.4	6.3	ns
	CLKAB or CLKBA	A or B	†	†	†	†	7.3		2.4	6.4	
	SAB or SBA	B or A	†	†	†	†	8.8		1.9	7.4	
t_{en}	$\overline{OE}$ or OE	A or B	†	†	†	†	6.6		1.6	6.3	ns
t_{dis}	$\overline{OE}$ or OE	A or B	†	†	†	†	6.6		1.2	6.2	ns

† This information was not available at the time of publication.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$f = 10\text{ MHz}$	†	†	55	pF
		Outputs disabled		†	†	12	

† This information was not available at the time of publication.

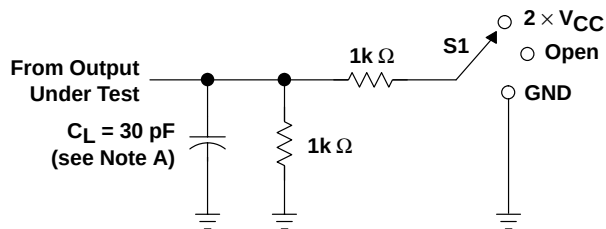
SN74LVCH16652A

16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS319G – NOVEMBER 1993 – REVISED JUNE 1998

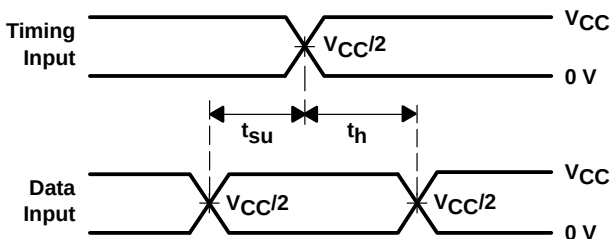
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

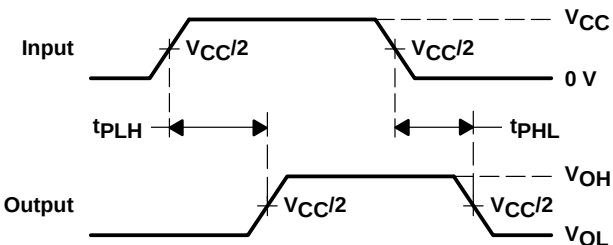


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PHZ}	Open



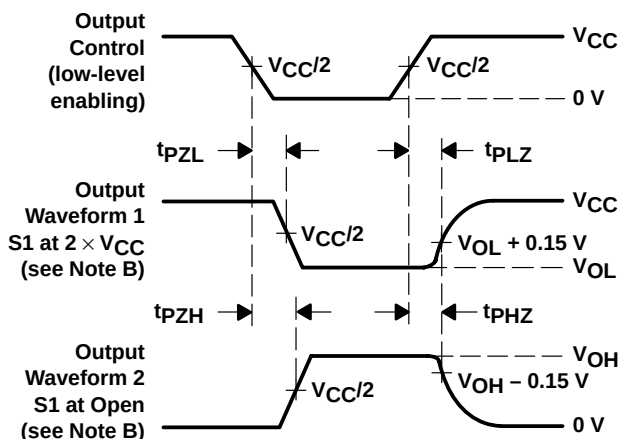
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN74LVCH16652A

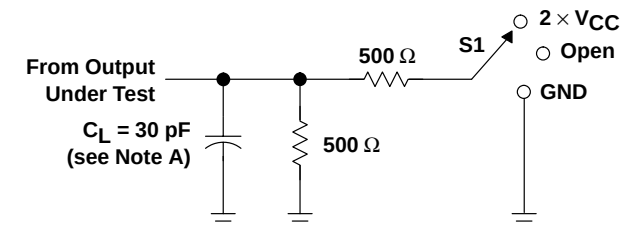
16-BIT BUS TRANSCEIVER AND REGISTER

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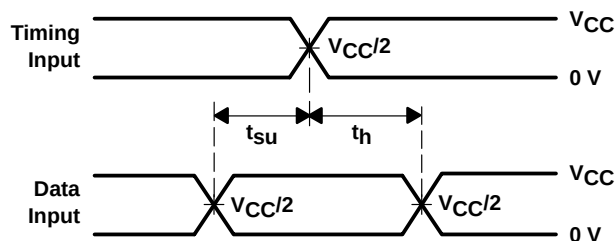
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

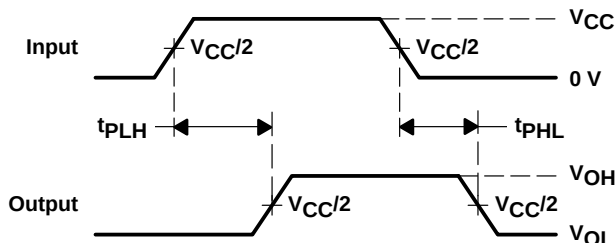


LOAD CIRCUIT

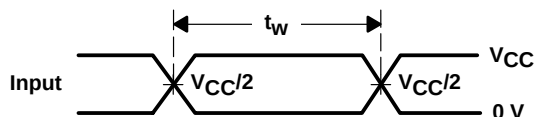
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



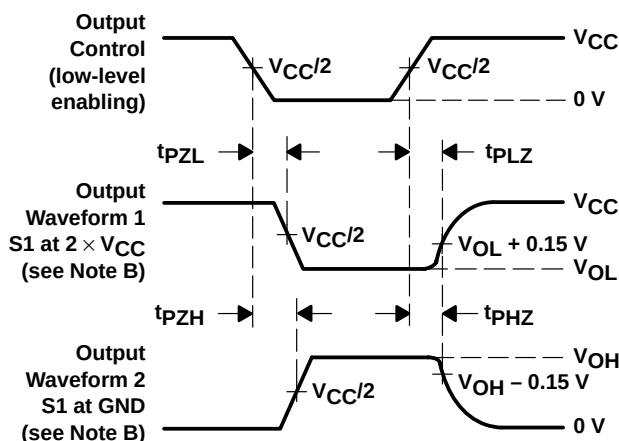
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



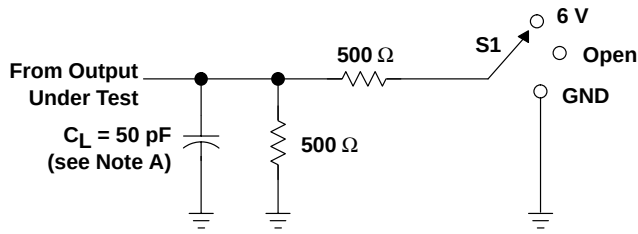
VOLTAGE WAVEFORMS
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Figure 3. Load Circuit and Voltage Waveforms

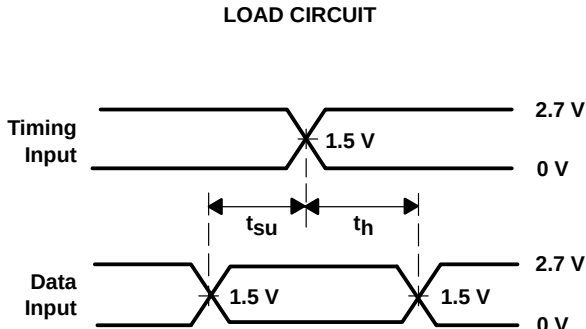
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

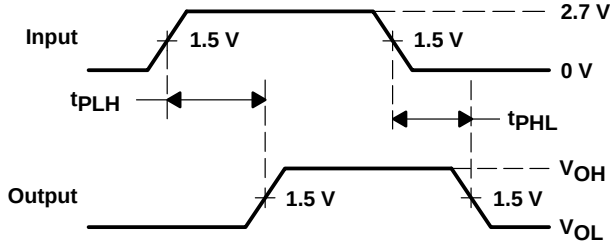


LOAD CIRCUIT

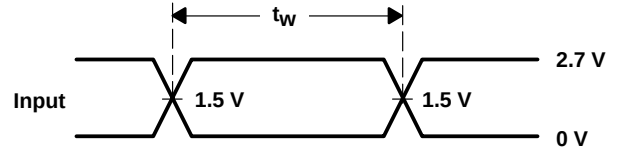
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



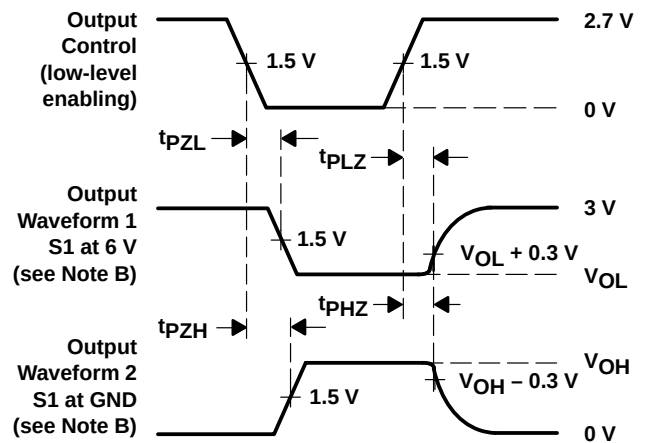
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

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 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 4. Load Circuit and Voltage Waveforms

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16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

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- Member of the Texas Instruments *Widebus*™ Family
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Power Off Disables Outputs, Permitting Live Insertion
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit registered transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH16952A contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. It can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input, provided that the clock-enable (CEAB or CEBA) input is low. Taking the output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH16952A is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)

$\overline{1OEAB}$	1	56	$\overline{1OEBA}$
$\overline{1CLKAB}$	2	55	$\overline{1CLKBA}$
$\overline{1CEAB}$	3	54	$\overline{1CEBA}$
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
$\overline{2CEAB}$	26	31	$\overline{2CEBA}$
$\overline{2CLKAB}$	27	30	$\overline{2CLKBA}$
$\overline{2OEAB}$	28	29	$\overline{2OEBA}$

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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WITH 3-STATE OUTPUTS

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FUNCTION TABLE†

INPUTS				OUTPUT B
CEAB	CLKAB	OEAB	A	
H	X	L	X	B0‡
X	L	L	X	B0‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

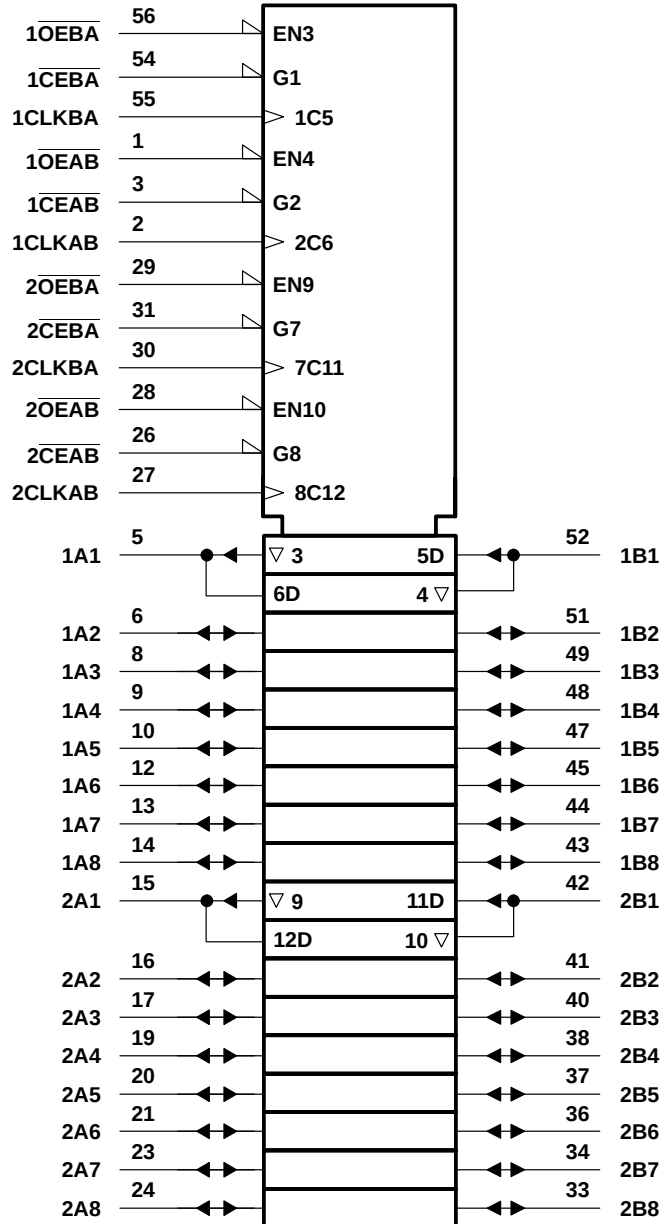
† A-to-B data flow is shown; B-to-A data flow is similar, but uses CEBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established

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logic symbol[†]

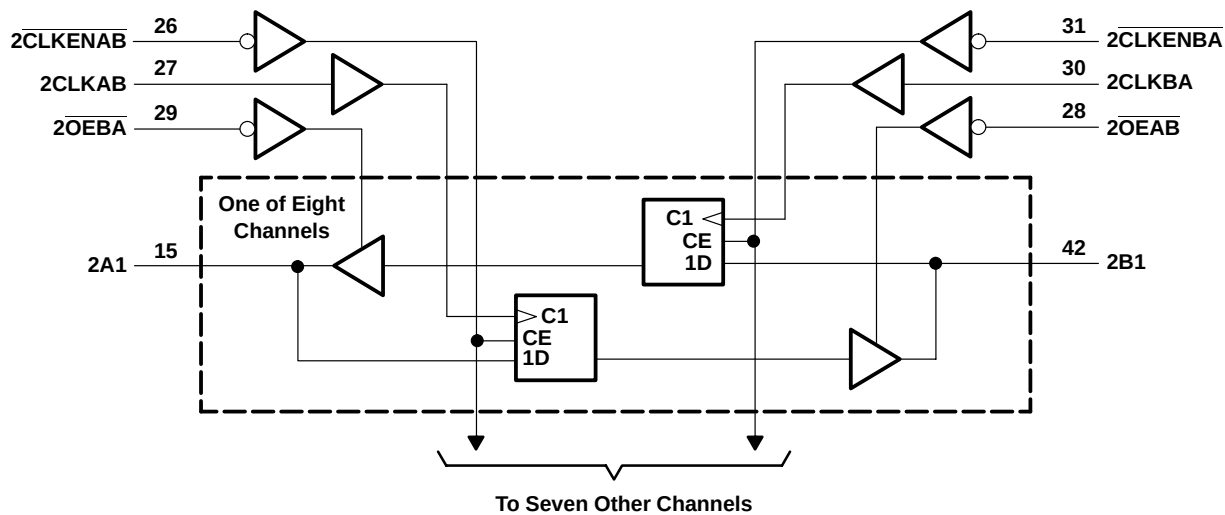
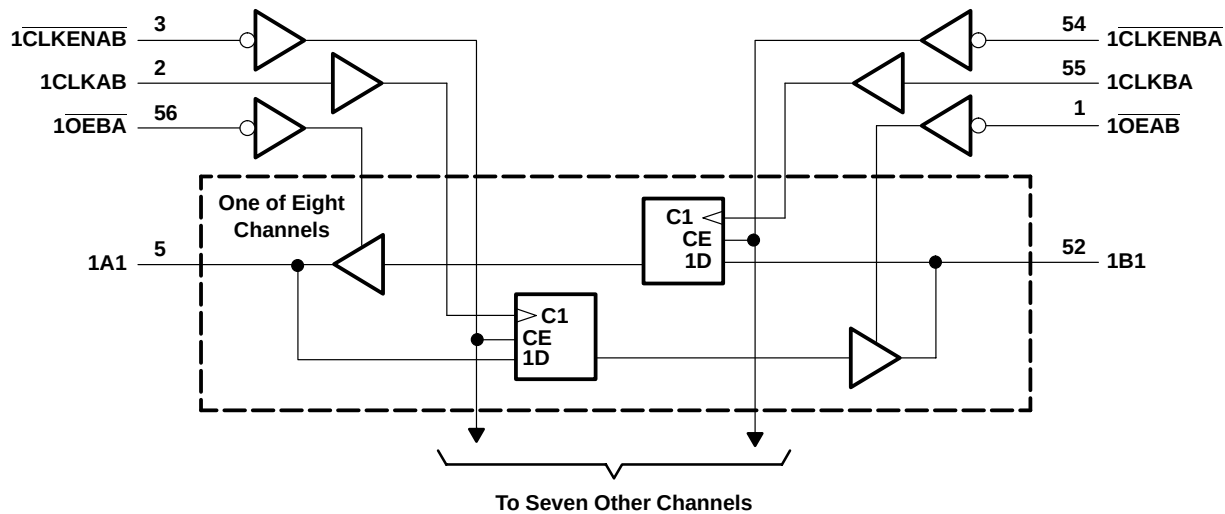


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



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WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I : (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	0.7		
	$V_{CC} = 2.7$ V to 3.6 V	0.8		
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}		I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
		I _{OH} = –4 mA	1.65 V	1.2			
		I _{OH} = –8 mA	2.3 V	1.7			
		I _{OH} = –12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = –24 mA	3 V	2.2			
V _{OL}		I _{OL} = 100 µA	1.65 V to 3.6 V			0.2	V
		I _{OL} = 4 mA	1.65 V			0.45	
		I _{OL} = 8 mA	2.3 V			0.7	
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _{I(hold)}	A or B ports	V _I = 0.58 V	1.65 V			‡	µA
		V _I = 1.07 V				‡	
		V _I = 0.7 V	2.3 V			45	
		V _I = 1.7 V				–45	
		V _I = 0.8 V	3 V			75	
		V _I = 2 V				–75	
		V _I = 0 to 3.6 V [§]	3.6 V			±500	
I _{off}		V _I or V _O = 5.5 V	0			±10	µA
I _{OZ} [¶]		V _O = 0 to 5.5 V	3.6 V			±10	µA
I _{CC}		V _I = V _{CC} or GND	3.6 V	I _O = 0		20	µA
		3.6 V ≤ V _I ≤ 5.5 V [#]				20	
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V		5		pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V		8.5		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This information was not available at the time of publication.

[§] This is the bus-hold maximum dynamic current required to switch the input from one state to another.

[¶] For I/O ports, the parameter I_{OZ} includes the input leakage current, but not I_{I(hold)}.

[#] This applies in the disabled state only.



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		†		†		150		150		MHz
t _w	Pulse duration, CLK high or low		†		†		3.3		3.3		ns
t _{su}	Setup time	Data before CLK↑	†		†		3.4		2.8		ns
		$\overline{\text{CE}}$ before CLK↑	†		†		1.8		1.4		
t _h	Hold time	Data after CLK↑	†		†		0.5		0.5		ns
		$\overline{\text{CE}}$ after CLK↑	†		†		1.1		1.9		

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			†		†		150		150		MHz
t_{pd}	CLKAB or CLKBA	B or A	†	†	†	†	7.6		1.6	6.6	ns
t_{en}	$\overline{\text{OE}}$	A or B	†	†	†	†	8		1.1	6.6	ns
t_{dis}	$\overline{\text{OE}}$	A or B	†	†	†	†	7.1		1.9	6.7	ns
$t_{\text{sk(o)}}^\ddagger$									1		ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	†	†	87	pF
		Outputs disabled	†	†	43	

† This information was not available at the time of publication.

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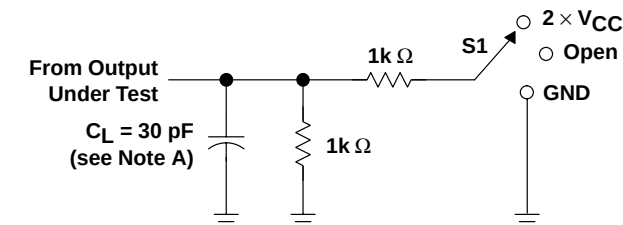
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WITH 3-STATE OUTPUTS

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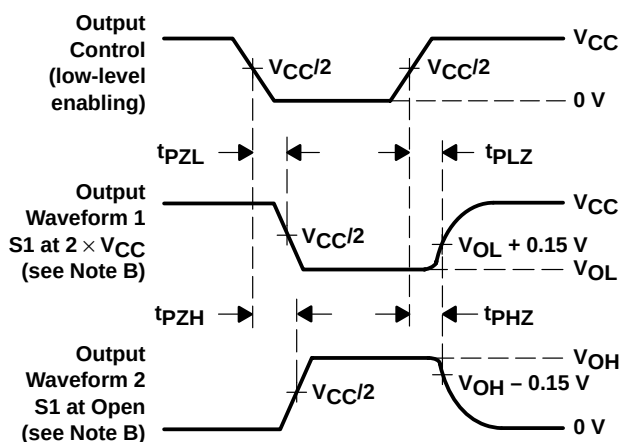
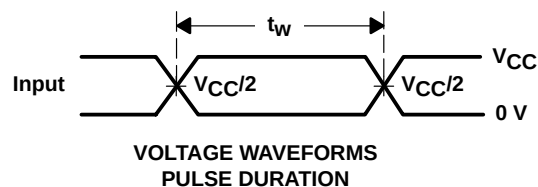
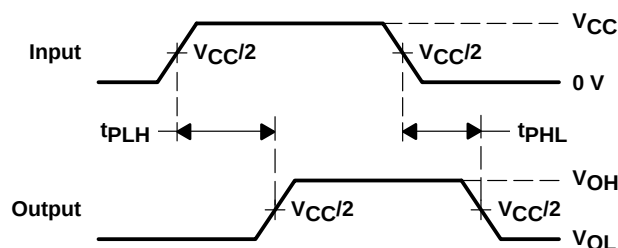
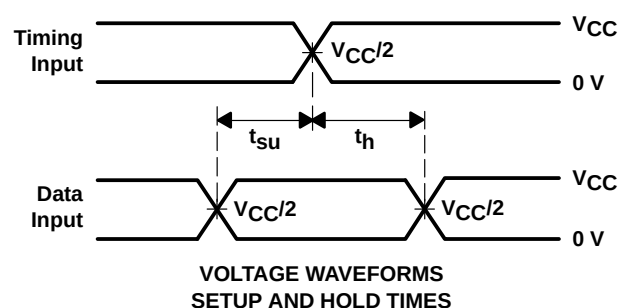
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$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times$ V_{CC}
t_{PHZ}/t_{PHL}	Open

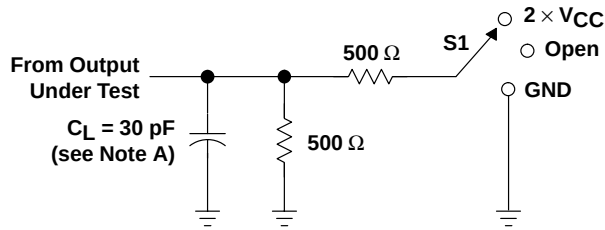


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 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

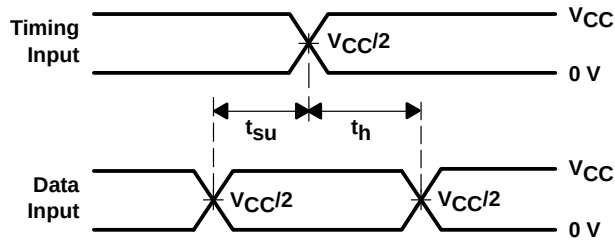
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

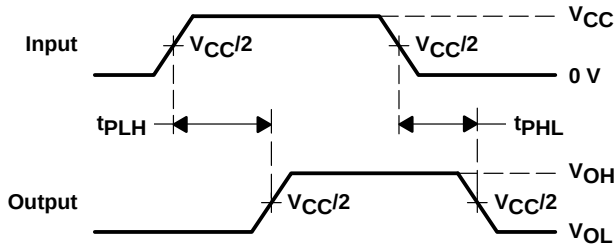


LOAD CIRCUIT

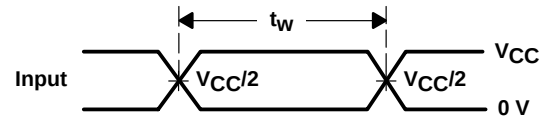
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PHL}	GND



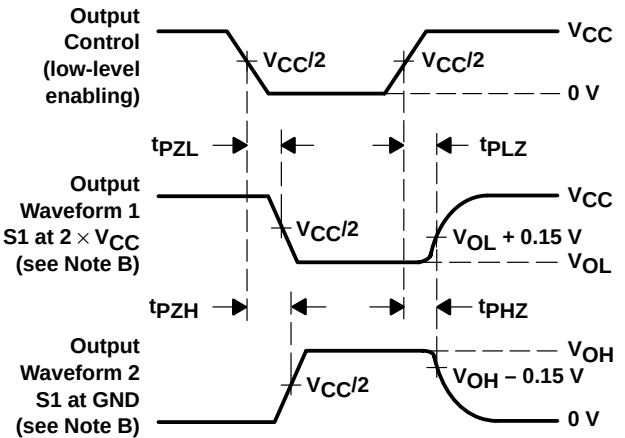
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN74LVCH16952A

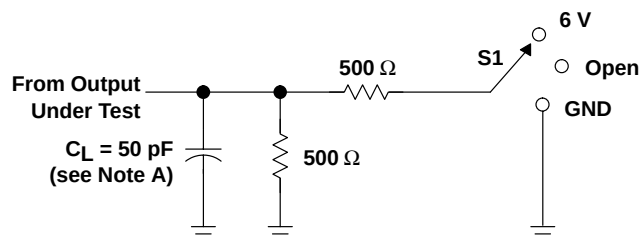
16-BIT REGISTERED TRANSCEIVER

WITH 3-STATE OUTPUTS

SCAS320F – NOVEMBER 1993 – REVISED JUNE 1998

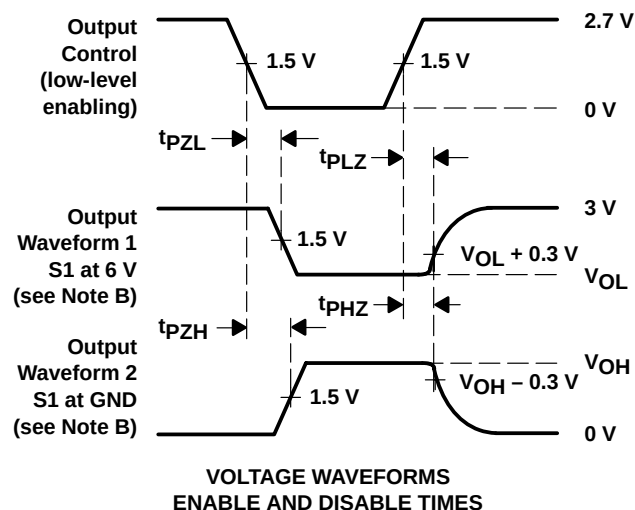
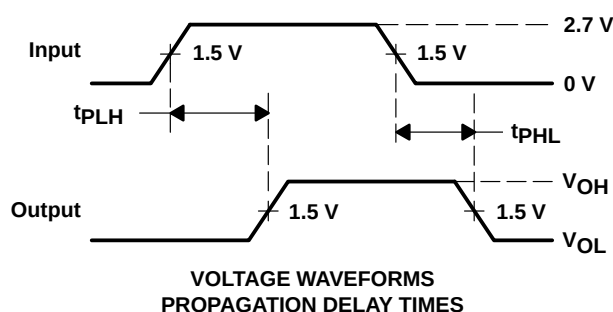
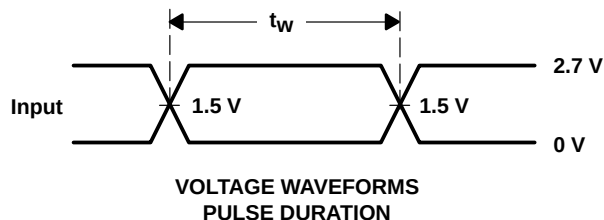
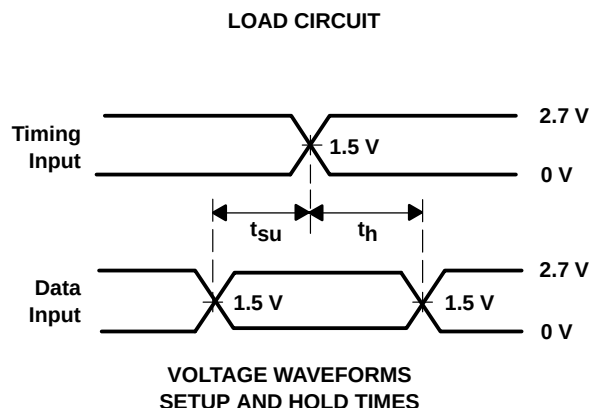
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN74LVC161284

19-BIT BUS INTERFACE WITH 3-STATE OUTPUTS

SCAS583G – NOVEMBER 1996 – REVISED APRIL 1998

- **3-State Outputs Drive Bus Lines Directly**
- **1.4-k Ω Pullup Resistors Integrated on All Open-Drain Outputs Eliminate the Need for Discrete Resistors**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Designed for the IEEE Std 1284-I (Level 1 Type) and IEEE Std 1284-II (Level 2 Type) Electrical Specifications**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin-Shrink Small-Outline (DGG) Packages**

description

The SN74LVC161284 is designed for 3-V to 3.6-V V_{CC} operation. This device provides asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

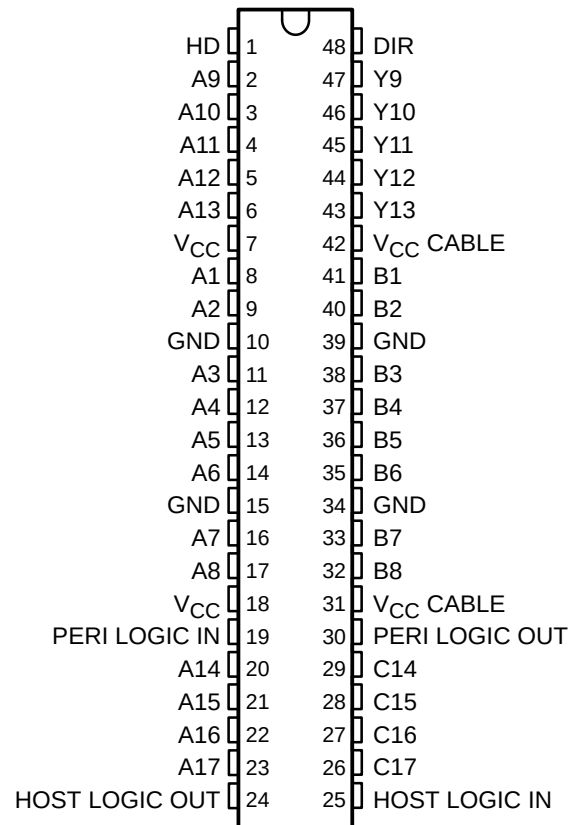
This device has eight bidirectional bits; data can flow in the A-to-B direction when DIR is high, and in the B-to-A direction when DIR is low. This device also has five drivers, which drive the cable side, and four receivers. The SN74LVC161284 has one receiver dedicated to the HOST LOGIC line and a driver to drive the PERI LOGIC line.

The output drive mode is determined by the high-drive (HD) control pin. When HD is high, the outputs are in a totem-pole configuration, and in an open-drain configuration when HD is low. This meets the drive requirements as specified in the IEEE Std 1284-I (level 1 type) and IEEE Std 1284-II (level 2 type) parallel peripheral-interface specifications. Except for HOST LOGIC IN and PERI LOGIC OUT, all cable-side pins have a 1.4-k Ω integrated pullup resistor. The pullup resistor is switched off if the associated output driver is in the low state or if the output voltage is above V_{CC} CABLE. If V_{CC} CABLE is off, PERI LOGIC OUT is set to low.

The device has two supply voltages. V_{CC} is designed for 3-V to 3.6-V operation. V_{CC} CABLE supplies the inputs and output buffers of the cable side only and is designed for 3-V to 3.6-V and for 4.7-V to 5.5-V operation. Even when V_{CC} CABLE is 3 V to 3.6 V, the cable-side I/O pins are 5-V tolerant.

The SN74LVC161284 is characterized for operation from 0°C to 70°C.

DGG OR DL PACKAGE
(TOP VIEW)



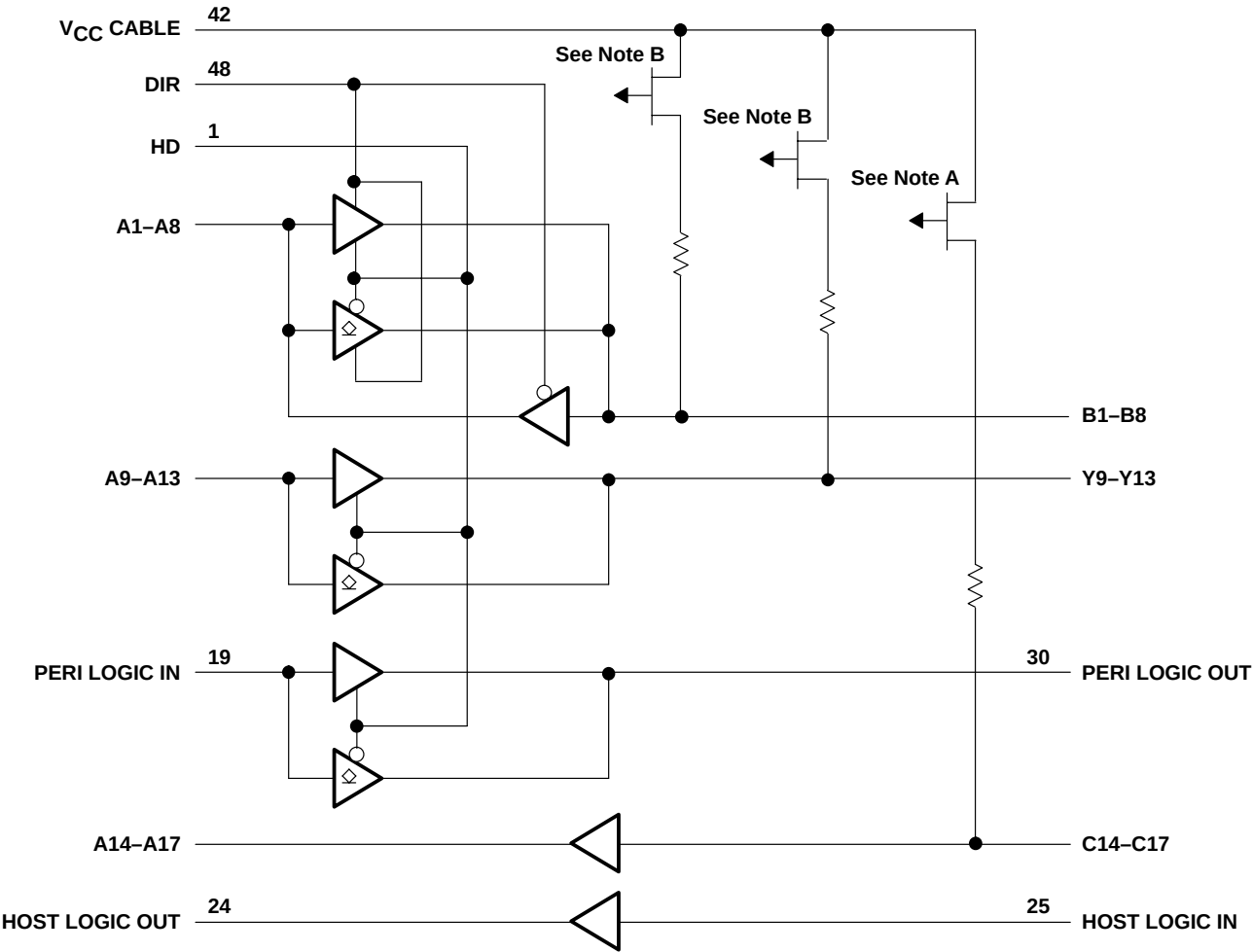
SN74LVC161284
19-BIT BUS INTERFACE
WITH 3-STATE OUTPUTS

SCAS583G – NOVEMBER 1996 – REVISED APRIL 1998

FUNCTION TABLE

INPUTS		OUTPUT	MODE
DIR	HD		
L	L	Open drain	A9–A13 to Y9–Y13 and PERI LOGIC IN to PERI LOGIC OUT
		Totem pole	B1–B8 to A1–A8 and C14–C17 to A14–A17
L	H	Totem pole	B1–B8 to A1–A8, A9–A13 to Y9–Y13, PERI LOGIC IN to PERI LOGIC OUT, and C14–C17 to A14–A17
H	L	Open drain	A1–A8 to B1–B8, A9–A13 to Y9–Y13, and PERI LOGIC IN to PERI LOGIC OUT
		Totem pole	C14–C17 to A14–A17
H	H	Totem pole	A1–A8 to B1–B8, A9–A13 to Y9–Y13, C14–C17 to A14–A17, and PERI LOGIC IN to PERI LOGIC OUT

logic diagram



NOTES: A. The PMOS transistor prevents backdriving current from the signal pins to V_{CC} CABLE when V_{CC} CABLE is open or at GND.
B. The PMOS transistors prevent backdriving current from the signal pins to V_{CC} CABLE when V_{CC} CABLE is open or at GND. The PMOS transistor is turned off when the associated driver is in the low state.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range: V_{CC} CABLE	–0.5 V to 7 V
V_{CC}	–0.5 V to 4.6 V
Input and output voltage range, V_I and V_O : Cable side (see Notes 1 and 2)	–2 V to 7 V
Peripheral side (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O : Except PERI LOGIC OUT	±50 mA
PERI LOGIC OUT	±100 mA
Continuous current through each V_{CC} or GND	±200 mA
Output high sink current, I_{SK} ($V_O = 5.5$ V and V_{CC} CABLE = 3 V)	65 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The ac input voltage pulsewidth is limited to 40 ns if the amplitude is greater than –0.5 V.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC} CABLE	Supply voltage for the cable side, V_{CC} CABLE $\geq V_{CC}$		3	5.5	V
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level input voltage	A, B, DIR, and HD	2	V	
		C14–C17	2.3		
		HOST LOGIC IN	2.6		
		PERI LOGIC IN	2		
V_{IL}	Low-level input voltage	A, B, DIR, and HD	0.8	V	
		C14–C17	0.8		
		HOST LOGIC IN	1.6		
		PERI LOGIC IN	0.8		
V_I	Input voltage	Peripheral side	0	V_{CC}	V
		Cable side	0	5.5	
V_O	Open-drain output voltage	HD low	0	5.5	V
I_{OH}	High-level output current	HD high, B and Y outputs	–14	mA	
		A outputs and HOST LOGIC OUT	–4		
		PERI LOGIC OUT	–0.5		
I_{OL}	Low-level output current	B and Y outputs	14	mA	
		A outputs and HOST LOGIC OUT	4		
		PERI LOGIC OUT	84		
T_A	Operating free-air temperature		0	70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC161284

19-BIT BUS INTERFACE

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range,
V_{CC} CABLE = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
ΔV _t	Input hysteresis	V _{thH} – V _{thL} for all inputs except the C inputs and HOST LOGIC IN	3.3 V	0.4		V	
		V _{thH} – V _{thL} for the HOST LOGIC IN	3.3 V	0.2			
		V _{thH} – V _{thL} for the C inputs	3.3 V	0.8			
V _{IH}	A, B, DIR, HD, and PERI LOGIC IN		3 V to 3.6 V	2		V	
	C inputs		3.45 V	2.3	2		
	HOST LOGIC IN		3.45 V	2.6	2.4		
V _{IL}	A, B, DIR, HD, and PERI LOGIC IN		3 V to 3.6 V	0.8		V	
	C inputs		3.6 V	1.2			
	HOST LOGIC IN		3.6 V	1.9			
V _{OH}	HD high, B and Y outputs	I _{OH} = –14 mA	3 V	2.23		V	
			4.7 V [‡]	2.4			
	HD high, A outputs, and HOST LOGIC OUT	I _{OH} = –4 mA	3 V	2.4			
			I _{OH} = –50 μA	3 V	2.8		
	PERI LOGIC OUT	I _{OH} = –0.5 mA	3.15 V	3.1			
			4.7 V [‡]	4.5			
V _{OL}	B and Y outputs	I _{OL} = 14 mA	3 V	0.77		V	
	A outputs and HOST LOGIC OUT	I _{OL} = 50 μA	3 V	0.2			
		I _{OL} = 4 mA	3 V	0.4			
	PERI LOGIC OUT	I _{OL} = 84 mA	3 V	0.8			
I _I	C inputs	V _I = V _{CC}	3.6 V [§]	50		μA	
		V _I = GND (pullup resistors)	3.6 V [§]	–3.5		mA	
	All inputs except the B or C inputs	V _I = V _{CC} or GND	3.6 V	±1		μA	
I _{OZ}	B outputs	V _O = V _{CC}	3.6 V	20		μA	
		V _O = GND (pullup resistors)	3.6 V [§]	–3.5		mA	
	A1–A8	V _O = V _{CC} or GND	3.6 V	±20		μA	
	Open-drain Y outputs	V _O = GND (pullup resistors)	3.6 V [§]	–3.5		mA	
I _{off}	Leakage to GND, B and Y outputs	V _I or V _O = 0 to 7 V	0 V	100		μA	
	Leakage to V _{CC} , B and Y outputs			10			
I _{CC} [¶]		V _I = V _{CC} , I _O = 0	3.6 V	0.8		mA	
		V _I = GND (12 × pullup)	3.6 V	45			
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	3		4	pF
C _{io}	All inputs	V _O = V _{CC} or GND	3.3 V	7		15	pF
Z _O	Cable side	I _{OH} = –35 mA	3.3 V	45			Ω
R pullup	Cable side	V _O = 0 V (in Hi Z)	3.3 V	1.15		1.65	kΩ

[†] Typical values are measured at V_{CC} = 3.3 V, V_{CC} CABLE = 5 V, and T_A = 25°C.

[‡] V_{CC} CABLE = 3.3 V

[§] V_{CC} CABLE = 3.6 V

[¶] A maximum current of 170 μ A per pin is added to I_{CC} if the pullup resistor pin is above V_{CC}.



SN74LVC161284
19-BIT BUS INTERFACE
WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP [†]	MAX	UNIT
t _{PLH}	Totem pole	A or B	B or A	1		40	ns
t _{PHL}				1		40	
t _{slew}	Totem pole	Cable-side outputs		0.05		0.4	V/ns
t _{en}	Totem pole	HD	B, Y, and PERI LOGIC OUT	1		25	ns
t _{dis}	Totem pole	HD	B, Y, and PERI LOGIC OUT	1		25	ns
t _{en} –t _{dis}				1		10	ns
t _{en}		DIR	A	1		50	ns
t _{dis}		DIR	A	1		15	ns
t _{dis}		DIR	B	1		50	ns
t _r , t _f	Open drain	A	B or Y			120	ns
t _{sk(o)} [‡]		A or B	B or A		2.5	10	ns

[†] Typical values are measured at V_{CC} = 3.3 V, V_{CC CABLE} = 5 V, and T_A = 25°C.

[‡] Skew is measured at 1/2 (V_{OH} + V_{OL}) for signals switching in the same direction.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	Outputs enabled	C _L = 0, f = 10 MHz	45	pF



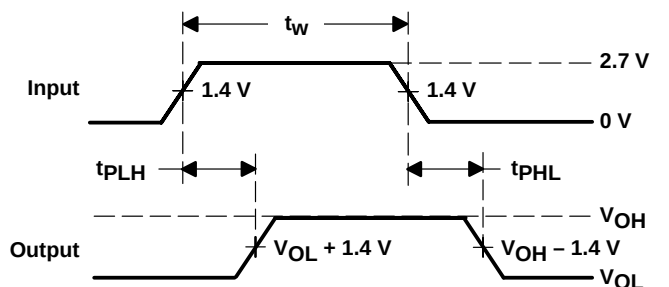
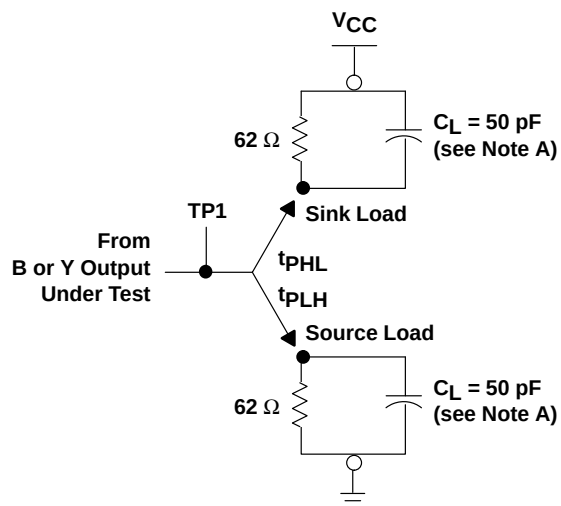
SN74LVC161284

19-BIT BUS INTERFACE

WITH 3-STATE OUTPUTS

SCAS583G – NOVEMBER 1996 – REVISED APRIL 1998

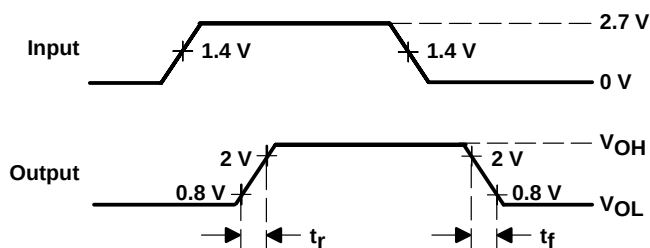
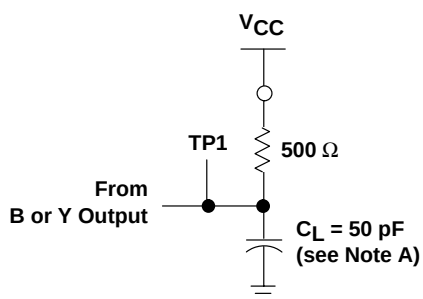
PARAMETER MEASUREMENT INFORMATION



Input rise and fall times are 3 ns, $150 \text{ ns} < \text{pulse width} < 10 \mu\text{s}$ for both low-to-high and high-to-low transitions. Slew rate is measured between 0.4 V and 0.9 V for the rising edge and between 2.4 V and 1.9 V for the falling edge.

VOLTAGE WAVEFORMS MEASURED AT TP1
PROPAGATION DELAY TIMES (A to B)

SLEW RATE A-TO-B OR Y LOAD (Totem Pole)



Rise and fall times (open drain) $< 120 \text{ ns}$.
Input rise and fall times are 3 ns.

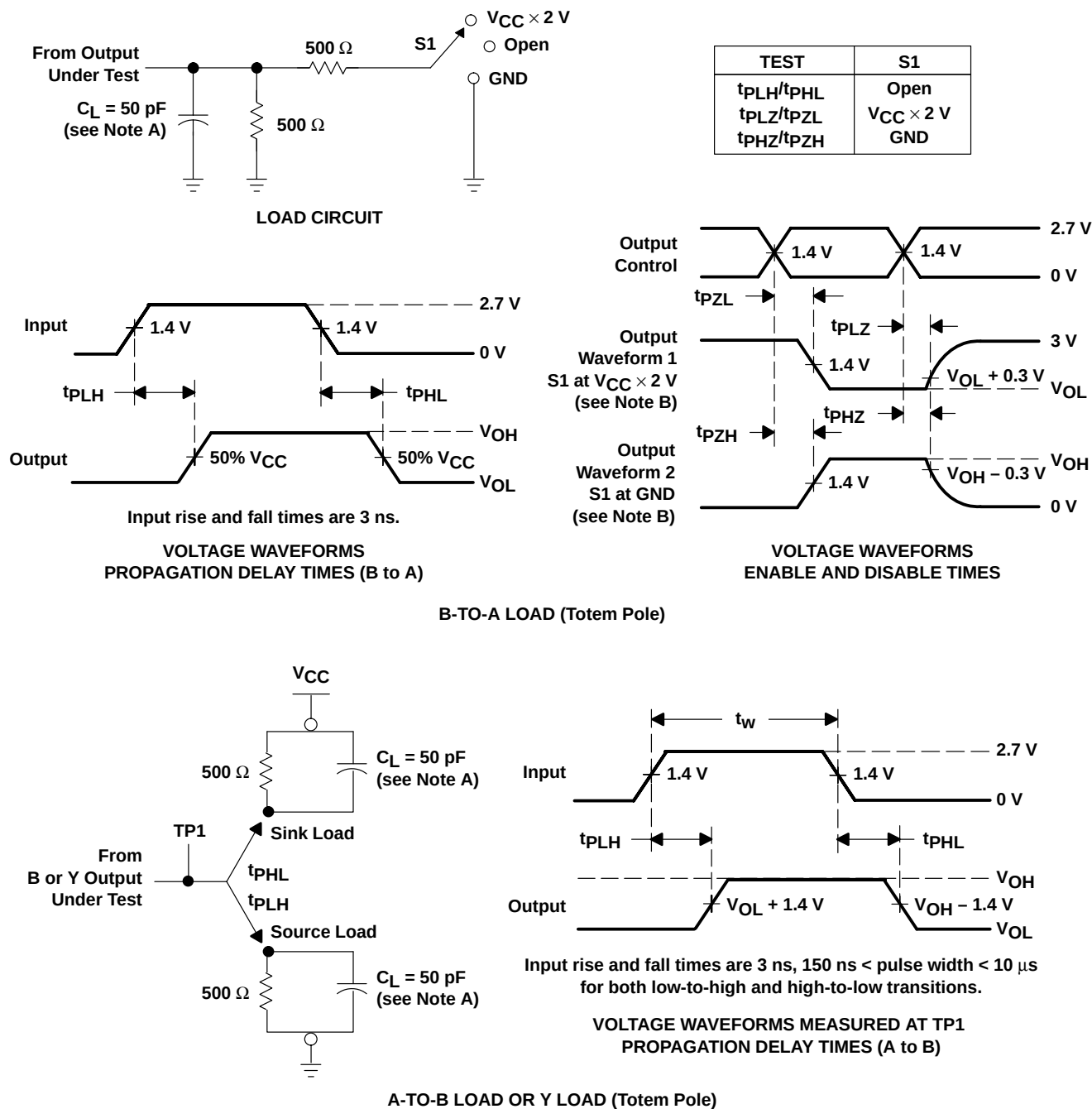
VOLTAGE WAVEFORMS MEASURED AT TP1, B SIDE

A-TO-B LOAD OR Y LOAD (Open Drain)

- NOTES: A. C_L includes probe and jig capacitance.
B. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

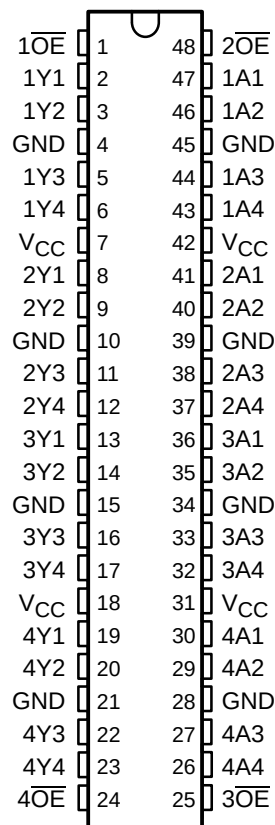
SN74LVCH162244A

16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS545F – OCTOBER 1995 – REVISED JUNE 1998

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (G) Packages

DL OR G PACKAGE
(TOP VIEW)



NOTE: G is the abbreviated alias for the DGG package.

description

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH162244A is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

The outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVCH162244A is characterized for operation from -40°C to 85°C .

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



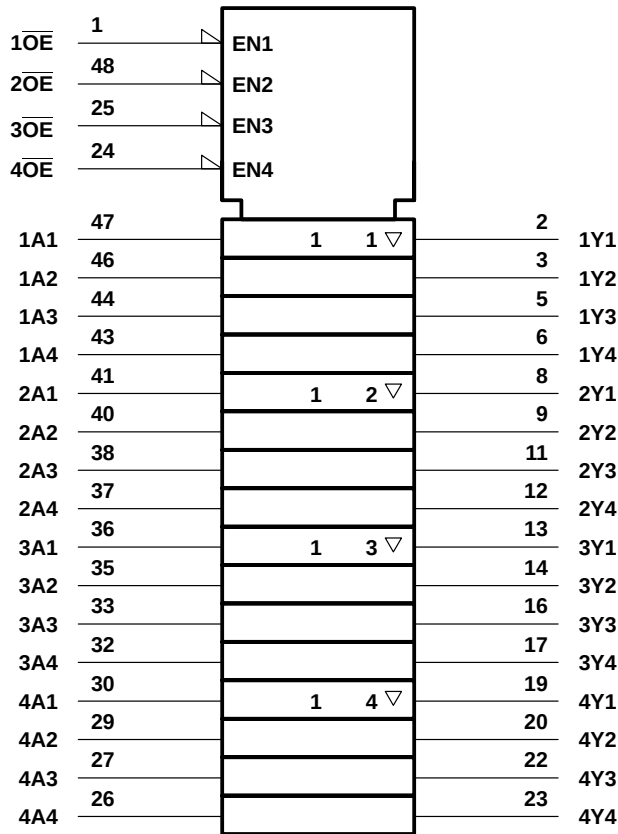
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FUNCTION TABLE
(each 4-bit buffer)

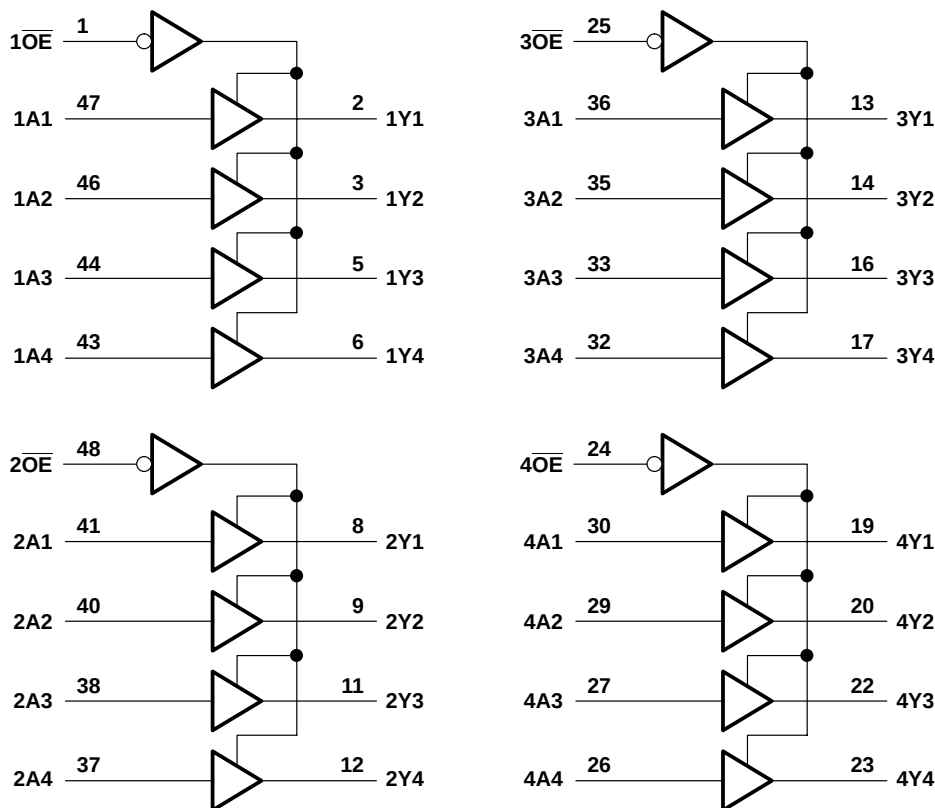
INPUTS		OUTPUT Y
OE	A	
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DL package	94°C/W
G package	89°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN74LVCH162244A
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage	0	5.5		V
V _O	Output voltage	High or low state	0	V _{CC}	V
		3 state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V		−2	mA
		V _{CC} = 2.3 V		−4	
		V _{CC} = 2.7 V		−8	
		V _{CC} = 3 V		−12	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		2	mA
		V _{CC} = 2.3 V		4	
		V _{CC} = 2.7 V		8	
		V _{CC} = 3 V		12	
Δt/Δv	Input transition rise or fall rate	0	10		ns/V
T _A	Operating free-air temperature	−40	85		°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74LVCH162244A
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCAS545F – OCTOBER 1995 – REVISED JUNE 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
	I _{OH} = –2 mA	1.65 V	1.2			
	I _{OH} = –4 mA	2.3 V	1.7			
		2.7 V	2.2			
	I _{OH} = –6 mA	3 V	2.4			
	I _{OH} = –8 mA	2.7 V	2			
	I _{OH} = –12 mA	3 V	2			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 2 mA	1.65 V	0.45			
	I _{OL} = 4 mA	2.3 V	0.7			
		2.7 V	0.4			
	I _{OL} = 6 mA	3 V	0.55			
	I _{OL} = 8 mA	2.7 V	0.6			
	I _{OL} = 12 mA	3 V	0.8			
I _I	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _I (hold)	V _I = 0.58 V	1.65 V	‡			µA
	V _I = 1.07 V		‡			
	V _I = 0.7 V	2.3 V	45			
	V _I = 1.7 V		–45			
	V _I = 0.8 V	3 V	75			
	V _I = 2 V		–75			
	V _I = 0 to 3.6 V [§]	3.6 V			±500	
I _{off}	V _I or V _O = 5.5 V	0			±10	µA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V			±10	µA
I _{CC}	V _I = V _{CC} or GND	3.6 V			20	µA
	3.6 V ≤ V _I ≤ 5.5 V [¶]				20	
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	V _I = V _{CC} or GND	3.3 V			5.5	pF
C _o	V _O = V _{CC} or GND	3.3 V			6	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This information was not available at the time of publication.

[§] This is the bus-hold maximum dynamic current required to switch the input from one state to another.

[¶] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	‡	‡	‡	‡	5.6		1.1	4.4	ns
t _{en}	$\overline{\text{OE}}$	Y	‡	‡	‡	‡	6.9		1	5.5	ns
t _{dis}	$\overline{\text{OE}}$	Y	‡	‡	‡	‡	6.8		1.8	6.3	ns

[‡] This information was not available at the time of publication.



SN74LVCH162244A
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCAS545F – OCTOBER 1995 – REVISED JUNE 1998

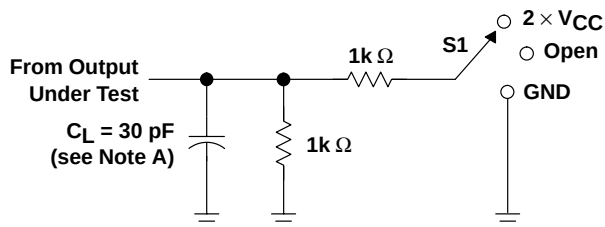
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	$f = 10\text{ MHz}$		†	†	35	pF
	Outputs disabled			†	†	4	

† This information was not available at the time of publication.

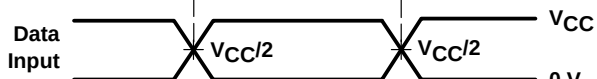
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

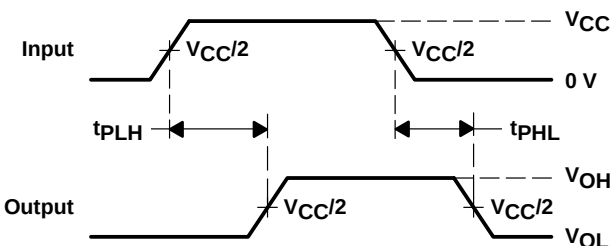


LOAD CIRCUIT

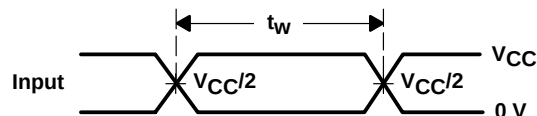
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



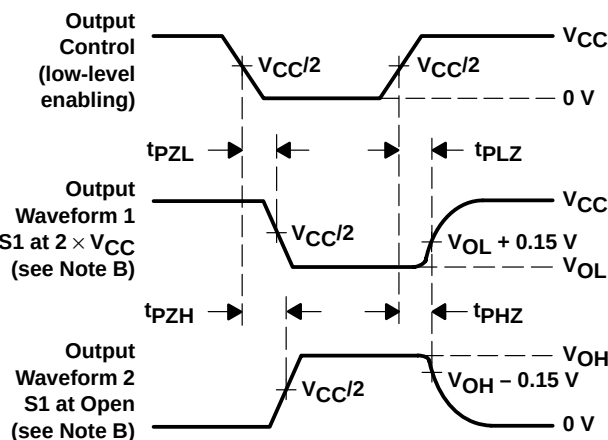
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVCH162244A

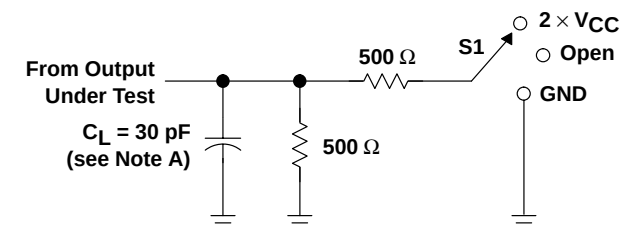
16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

SCAS545F – OCTOBER 1995 – REVISED JUNE 1998

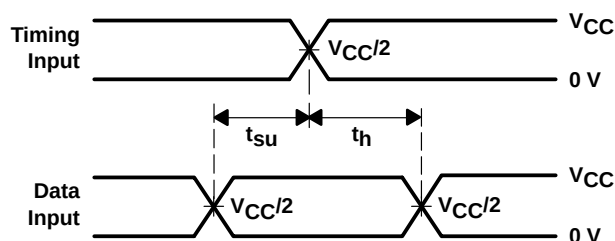
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

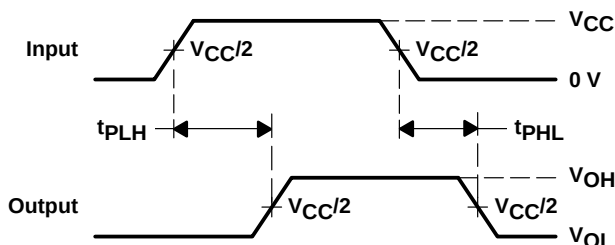


LOAD CIRCUIT

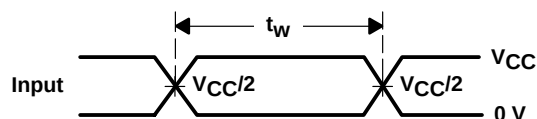
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



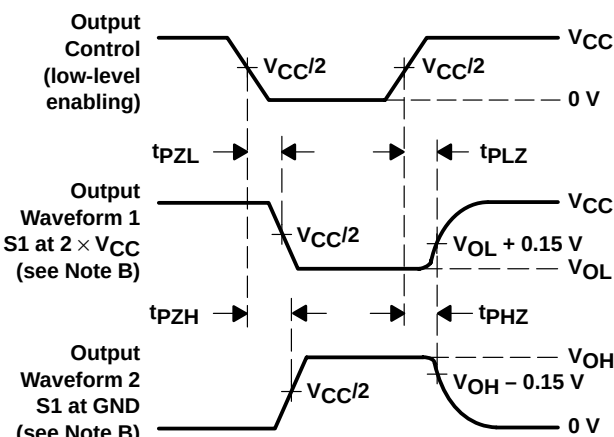
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



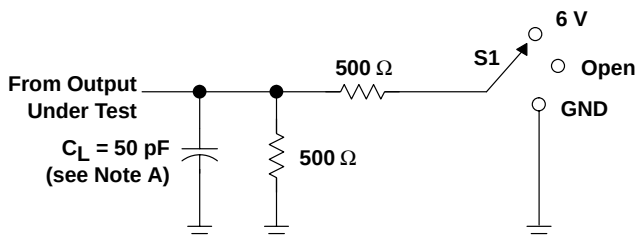
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

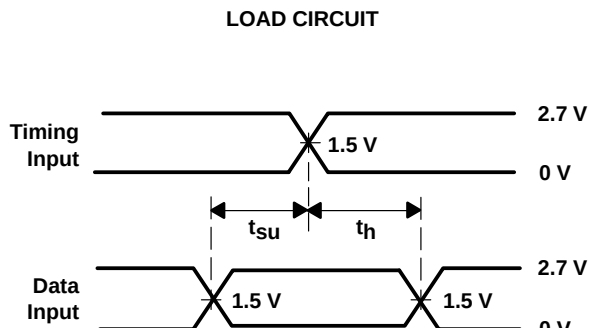
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$

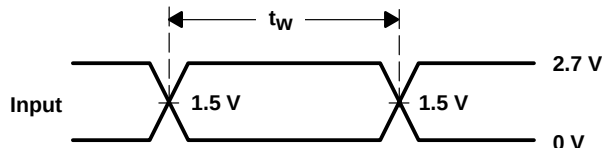


LOAD CIRCUIT

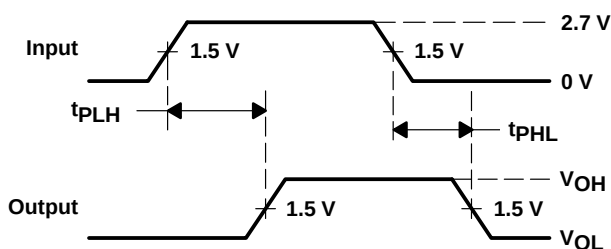
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



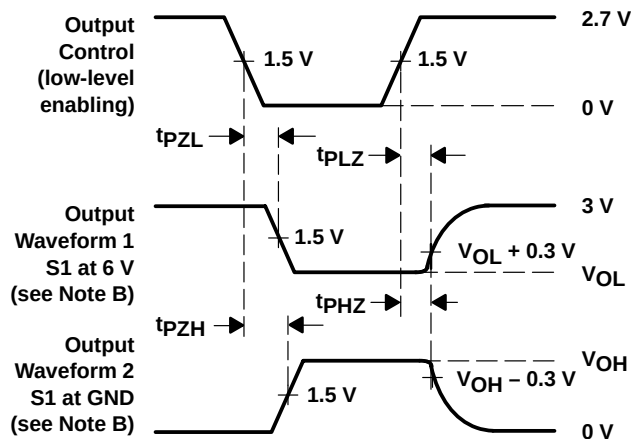
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

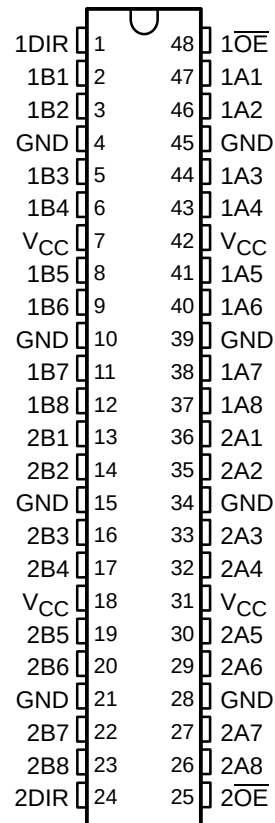
Figure 3. Load Circuit and Voltage Waveforms

SN74LVCHR162245A 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS582E – NOVEMBER 1996 – REVISED JUNE 1998

- Member of the Texas Instruments *Widebus*™ Family
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Power Off Disables Inputs/Outputs, Permitting Live Insertion
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- All Outputs Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- Package Options Include Plastic 300-mil Shrink Small-Outline (L) and Thin Shrink Small-Outline (G) Packages

G OR L PACKAGE
(TOP VIEW)



NOTE: G is the abbreviated alias for the DGG package, and L is the abbreviated alias for the DL package.

description

This 16-bit (dual-octal) noninverting bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCHR162245A is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

All outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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description (continued)

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

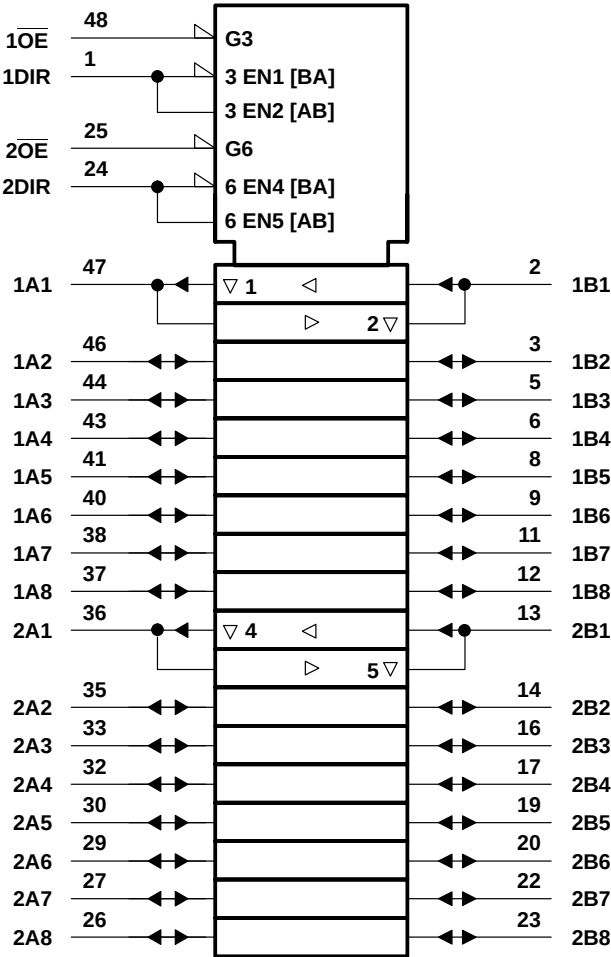
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCHR162245A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†

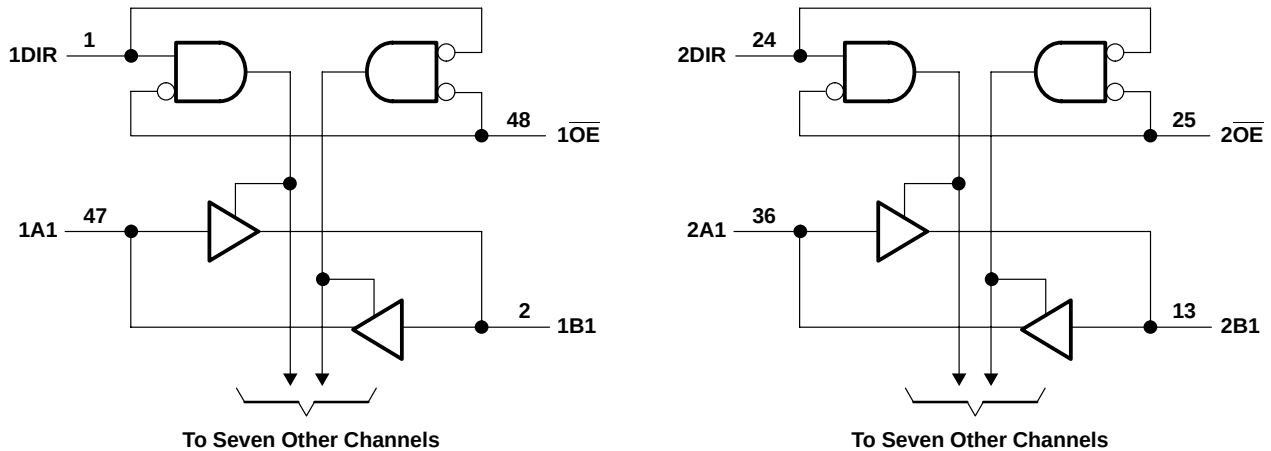


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LVCHR162245A
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I : (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): G package	89°C/W
L package	97°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65 \text{ V}$		–2	mA
	$V_{CC} = 2.3 \text{ V}$		–4	
	$V_{CC} = 2.7 \text{ V}$		–8	
	$V_{CC} = 3 \text{ V}$		–12	
I_{OL} Low-level output current	$V_{CC} = 1.65 \text{ V}$		2	mA
	$V_{CC} = 2.3 \text{ V}$		4	
	$V_{CC} = 2.7 \text{ V}$		8	
	$V_{CC} = 3 \text{ V}$		12	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}			I _{OH} = –100 μA	1.65 V to 3.6 V	V _{CC} –0.2		V
			I _{OH} = –2 mA	1.65 V	1.2		
			I _{OH} = –4 mA	2.3 V	1.7		
				2.7 V	2.2		
			I _{OH} = –6 mA	3 V	2.4		
			I _{OH} = –8 mA	2.7 V	2		
			I _{OH} = –12 mA	3 V	2		
V _{OL}			I _{OL} = 100 μA	1.65 V to 3.6 V	0.2		V
			I _{OL} = 2 mA	1.65 V	0.45		
			I _{OL} = 4 mA	2.3 V	0.7		
				2.7 V	0.4		
			I _{OL} = 6 mA	3 V	0.55		
			I _{OL} = 8 mA	2.7 V	0.6		
			I _{OL} = 12 mA	3 V	0.8		
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V	±5		μA	
I _I (hold)	A or B ports	V _I = 0.58 V	1.65 V	‡		μA	
		V _I = 1.07 V		‡			
		V _I = 0.7 V	2.3 V	45			
		V _I = 1.7 V		–45			
		V _I = 0.8 V	3 V	75			
		V _I = 2 V		–75			
		V _I = 0 to 3.6 V [§]		3.6 V	±500		
		I _{off}		V _I or V _O = 5.5 V	0		±10
I _{OZ} [¶]		V _O = 0 to 5.5 V	3.6 V	±10		μA	
I _{CC}		V _I = V _{CC} or GND,	3.6 V	20		μA	
		3.6 V ≤ V _I ≤ 5.5 V [#]		20			
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V	500		μA
C _i	Control inputs	V _I = V _{CC} or GND		3.3 V	3		pF
C _{io}	A or B ports	V _O = V _{CC} or GND		3.3 V	12		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This information was not available at the time of publication.

[§] This is the bus-hold maximum dynamic current required to switch the input from one state to another.

[¶] For I/O ports, the parameter I_{OZ} includes the input leakage current, but not I_I(hold).

[#] This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	‡	‡	‡	‡	5.7		1.5	4.8	ns
t _{en}	$\overline{\text{OE}}$	A or B	‡	‡	‡	‡	7.9		1.5	6.3	ns
t _{dis}	$\overline{\text{OE}}$	A or B	‡	‡	‡	‡	8.3		2.2	7.4	ns

[‡] This information was not available at the time of publication.



SN74LVCHR162245A
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

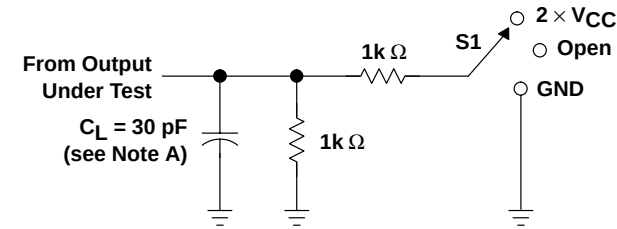
SCAS582E – NOVEMBER 1996 – REVISED JUNE 1998

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	f = 10 MHz	†	†	39	pF
		Outputs disabled		†	†	4	

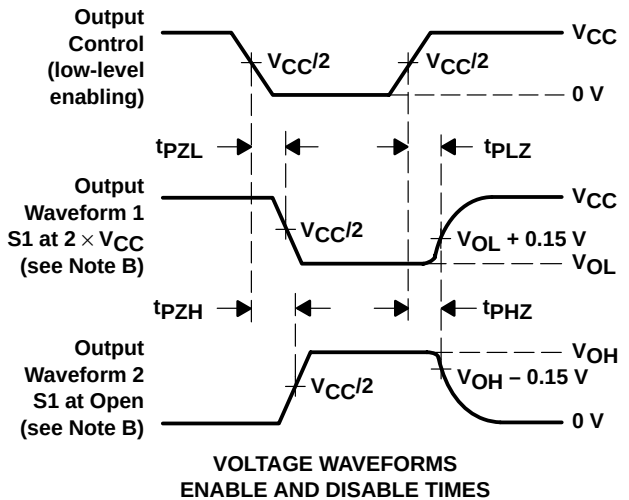
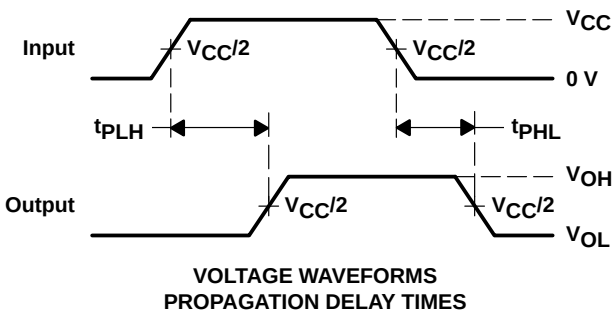
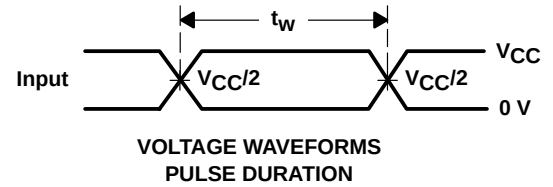
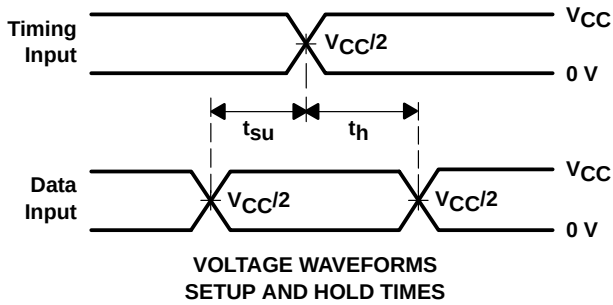
† This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVCHR162245A

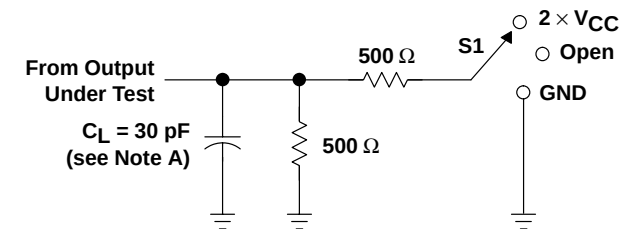
16-BIT BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCAS582E – NOVEMBER 1996 – REVISED JUNE 1998

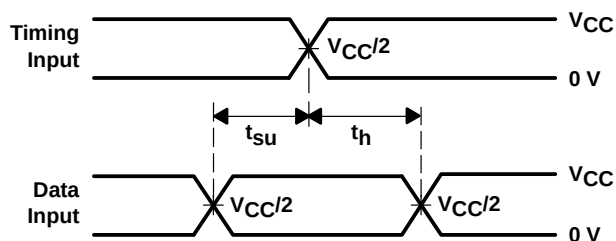
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

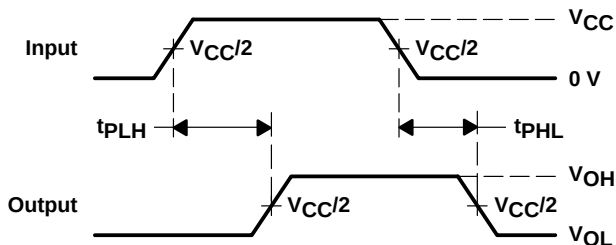


LOAD CIRCUIT

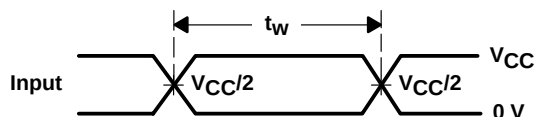
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



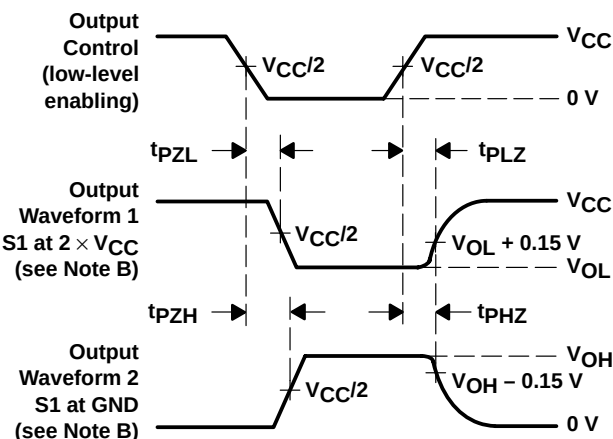
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

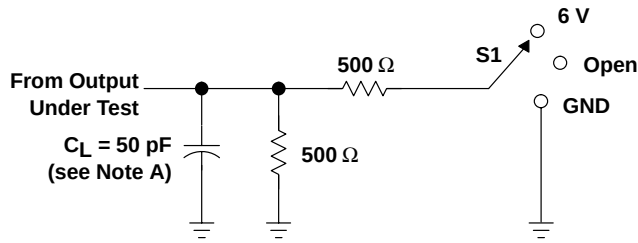


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

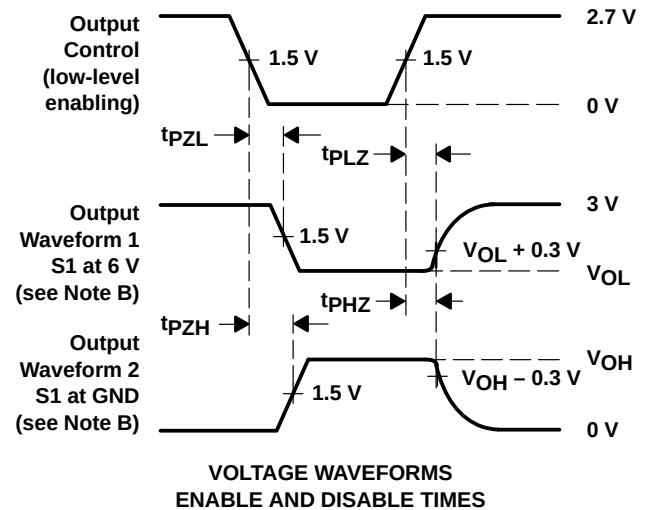
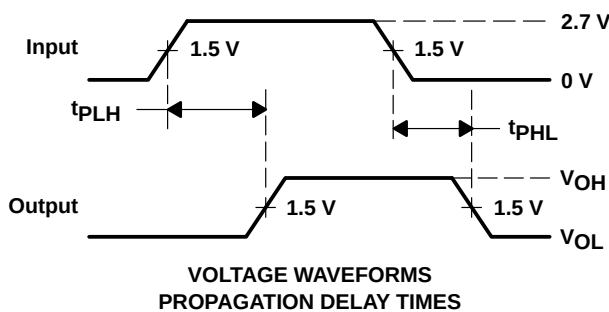
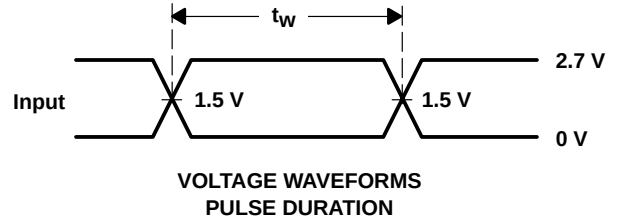
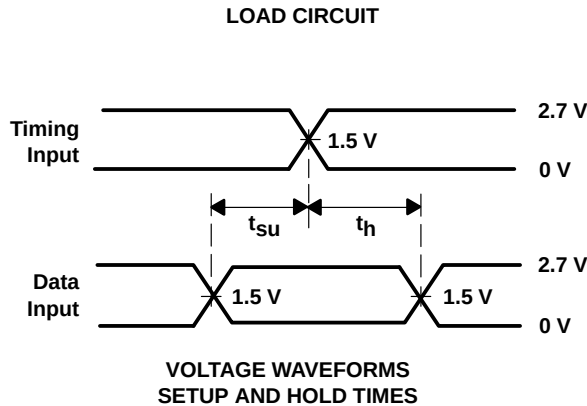
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

General Information	1
LVC Gates and MSI	2
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LVC Widebus™	4
LVC 3.3-V to 5-V Translators and Cable Drivers	5
LV Gates and MSI	6
LV Octals	7
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Mechanical Data	9

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SN74LVCC3245A

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

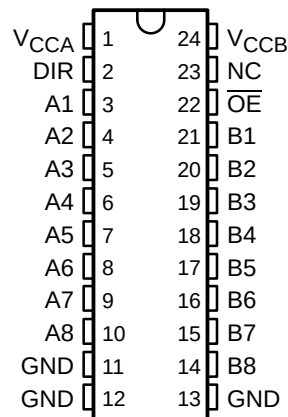
description

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails. The B port is designed to track V_{CCB} , which accepts voltages from 3 V to 5.5 V, and the A port is designed to track V_{CCA} , which operates at 2.3 V to 3.6 V. This allows for translation from a 3.3-V to a 5-V system environment and vice versa, or from a 2.5-V to a 3.3-V system environment and vice versa.

The SN74LVCC3245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The SN74LVCC3245A is characterized for operation from -40°C to 85°C .

DB, DW, OR PW PACKAGE (TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



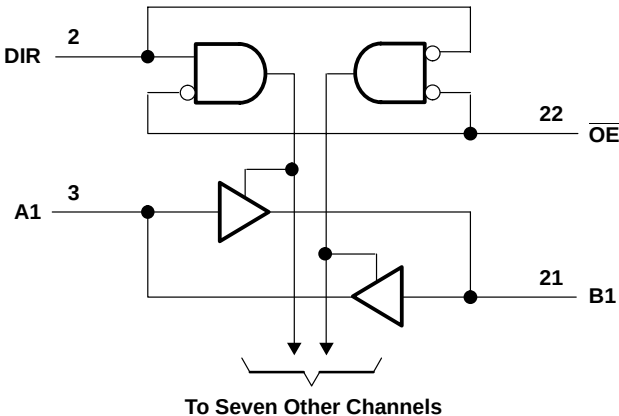
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SN74LVCC3245A
OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE
AND 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CCA} and V _{CCB}	−0.5 V to 6 V
Input voltage range, V _I : All A port (see Note 2)	−0.5 to V _{CCA} + 0.5 V
All B port (see Note 1)	−0.5 to V _{CCB} + 0.5 V
Except I/O ports (see Note 2)	−0.5 to V _{CCA} + 0.5 V
Output voltage range, V _O (see Note 1): All A port	−0.5 to V _{CCA} + 0.5 V
All B port	−0.5 to V _{CCB} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	−50 mA
Output clamp current, I _{OK} (V _O < 0)	−50 mA
Continuous output current, I _O	±50 mA
Continuous current through V _{CCA} , V _{CCB} , or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T _{stg}	−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. This value is limited to 6 V maximum.
 2. This value is limited to 4.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN74LVCC3245A

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		V _{CCA}	V _{CCB}	MIN	NOM	MAX	UNIT
V _{CCA}	Supply voltage			2.3	3.3	3.6	V
V _{CCB}	Supply voltage			3	5	5.5	V
V _{IHA}	High-level input voltage	V _{OB} ≤ 0.1 V, V _{OB} ≥ V _{CCB} – 0.1 V	2.3 V	3 V	1.7		V
			2.7 V	3 V	2		
			3 V	3.6 V	2		
			3.6 V	5.5 V	2		
V _{IHB}	High-level input voltage	V _{OA} ≤ 0.1 V, V _{OA} ≥ V _{CCA} – 0.1 V	2.3 V	3 V	2		V
			2.7 V	3 V	2		
			3 V	3.6 V	2		
			3.6 V	5.5 V	3.85		
V _{ILA}	Low-level input voltage	V _{OB} ≤ 0.1 V, V _{OB} ≥ V _{CCB} – 0.1 V	2.3 V	3 V		0.7	V
			2.7 V	3 V		0.8	
			3 V	3.6 V		0.8	
			3.6 V	5.5 V		0.8	
V _{ILB}	Low-level input voltage	V _{OA} ≤ 0.1 V, V _{OA} ≥ V _{CCA} – 0.1 V	2.3 V	3 V		0.8	V
			2.7 V	3 V		0.8	
			3 V	3.6 V		0.8	
			3.6 V	5.5 V		1.65	
V _{IA}	Input voltage			0		V _{CCA}	V
V _{IB}	Input voltage			0		V _{CCB}	V
V _{OA}	Output voltage			0		V _{CCA}	V
V _{OB}	Output voltage			0		V _{CCB}	V
I _{OHA}	High-level output current		2.3 V	3 V		–8	mA
			2.7 V	3 V		–12	
			3.3 V	3 V		–24	
I _{OHB}	High-level output current		2.3 V	3.3 V		–12	mA
			2.7 V	3.3 V		–12	
			3.3 V	3 V		–24	
I _{OLA}	Low-level output current		2.3 V	3 V		8	mA
			2.7 V	3 V		12	
			3.3 V	3 V		24	
I _{OLB}	Low-level output current		2.3 V	3.3 V		12	mA
			2.7 V	3.3 V		12	
			3.3 V	3 V		24	
Δt/Δv	Input transition rise or fall rate			0		10	ns/V
T _A	Operating free-air temperature			–40		85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74LVCC3245A

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	MIN	TYP	MAX	UNIT
V _{OHA}		I _{OH} = –100 µA	3 V	3 V	2.9	3		V
		I _{OH} = –8 mA	2.3 V	3 V	2			
		I _{OH} = –12 mA	2.7 V	3 V	2.2	2.5		
			3 V	3 V	2.4	2.8		
		I _{OH} = –24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	2	2.3		
V _{OHB}		I _{OH} = –100 µA	3 V	3 V	2.9	3		V
		I _{OH} = –12 mA	2.3 V	3 V	2.4			
			2.7 V	3 V	2.4	2.8		
		I _{OH} = –24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	3.2	4.2		
V _{OLA}		I _{OL} = 100 µA	3 V	3 V			0.1	V
		I _{OL} = 8 mA	2.3 V	3 V			0.6	
		I _{OL} = 12 mA	2.7 V	3 V		0.1	0.5	
		I _{OL} = 24 mA	3 V	3 V		0.2	0.5	
			2.7 V	4.5 V		0.2	0.5	
V _{OLB}		I _{OL} = 100 µA	3 V	3 V			0.1	V
		I _{OL} = 12 mA	2.3 V	3 V			0.4	
		I _{OL} = 24 mA	3 V	3 V		0.2	0.5	
				4.5 V		0.2	0.5	
I _I	Control inputs	V _I = V _{CCA} or GND	3.6 V	3.6 V	±0.1	±1		µA
I _{OZ} [†]	A or B ports	V _O = V _{CCA/B} or GND, V _I = V _{IL} or V _{IH}	3.6 V	3.6 V	±0.5	±5		µA
I _{CCA}	B to A	A port = V _{CCA} or GND, I _O = 0	3.6 V	Open		5	50	µA
		B port = V _{CCB} or GND, I _O = 0	3.6 V	3.6 V		5	50	
				5.5 V		5	50	
I _{CCB}	A to B	A port = V _{CCA} or GND, I _O = 0	3.6 V	3.6 V		5	50	µA
				5.5 V		8	80	
ΔI _{CCA} [‡]	A port	V _I = V _{CCA} – 0.6 V, Other inputs at V _{CCA} or GND, OE at GND and DIR at V _{CCA}	3.6 V	3.6 V		0.35	0.5	mA
	OE	V _I = V _{CCA} – 0.6 V, Other inputs at V _{CCA} or GND, DIR at V _{CCA}	3.6 V	3.6 V		0.35	0.5	
	DIR	V _I = V _{CCA} – 0.6 V, Other inputs at V _{CCA} or GND, OE at GND	3.6 V	3.6 V		0.35	0.5	
ΔI _{CCB} [‡]	B port	V _I = V _{CCB} – 2.1 V, Other inputs at V _{CCB} or GND, OE at GND and DIR at GND	3.6 V	5.5 V		1	1.5	mA
C _i	Control inputs	V _I = V _{CCA} or GND	Open	Open		4		pF
C _{io}	A or B ports	V _O = V _{CCA/B} or GND	3.3 V	5 V		18.5		pF
C _{pd}	A to B	Outputs enabled	3.3 V	5 V		38		pF
	B to A	Outputs enabled	3.3 V	5 V		36.5		

[†] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[‡] This is the increase in supply current for each input that is at one of the specified voltage levels rather than 0 V or the associated V_{CC}.



SN74LVCC3245A

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

SCAS585E – NOVEMBER 1996 – REVISED MAY 1998

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}$, $V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}$, $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	A	B	1	9.4	1	6	1	7.1	ns
t_{PLH}			1	9.1	1	5.3	1	7.2	
t_{PHL}	B	A	1	11.2	1	5.8	1	6.4	ns
t_{PLH}			1	9.9	1	7	1	7.6	
t_{PZL}	$\overline{OE}$	A	1	14.5	1	9.2	1	9.7	ns
t_{PZH}			1	12.9	1	9.5	1	9.5	
t_{PZL}	$\overline{OE}$	B	1	13	1	8.1	1	9.2	ns
t_{PZH}			1	12.8	1	8.4	1	9.9	
t_{PLZ}	$\overline{OE}$	A	1	7.1	1	5.5	1	6.6	ns
t_{PHZ}			1	6.9	1	7.8	1	6.9	
t_{PLZ}	$\overline{OE}$	B	1	8.8	1	7.3	1	7.5	ns
t_{PHZ}			1	8.9	1	7	1	7.9	



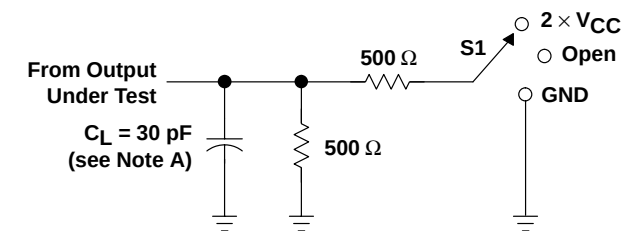
SN74LVCC3245A

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

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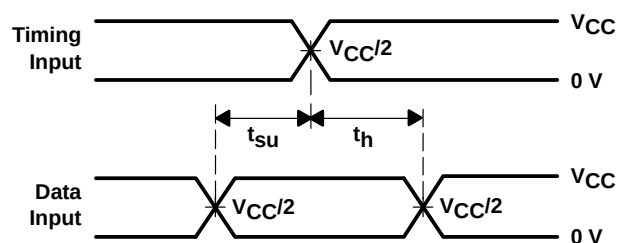
PARAMETER MEASUREMENT INFORMATION FOR A PORT

$$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V AND } V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$$

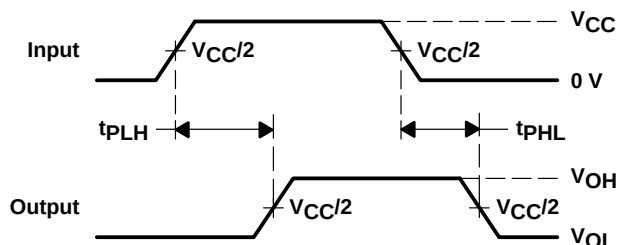


LOAD CIRCUIT

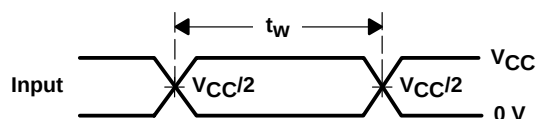
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



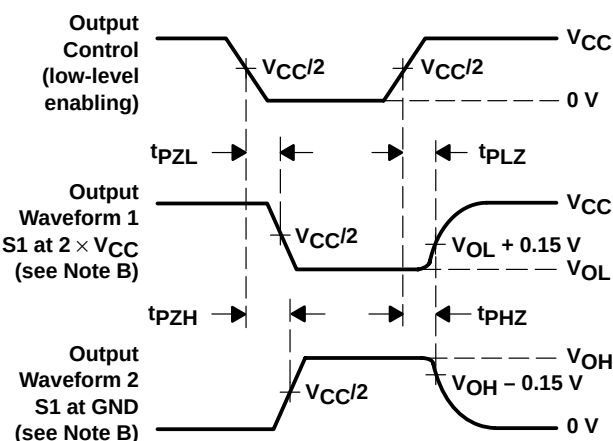
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

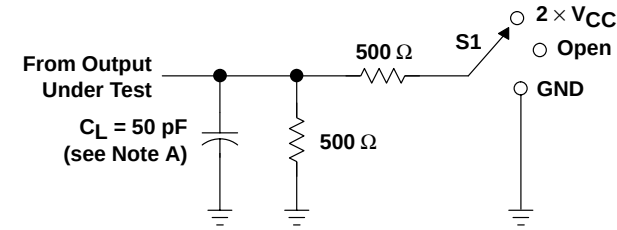
SN74LVCC3245A

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

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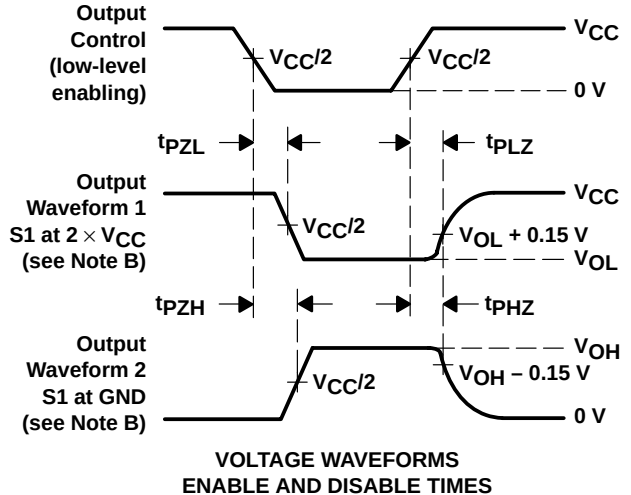
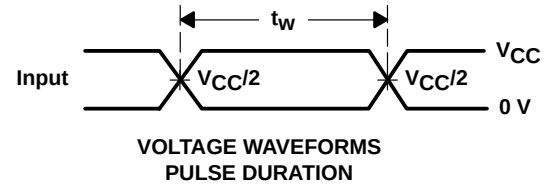
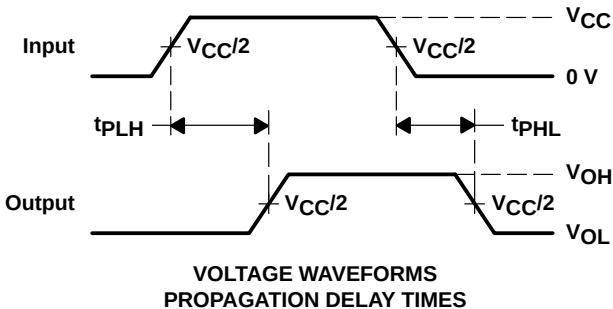
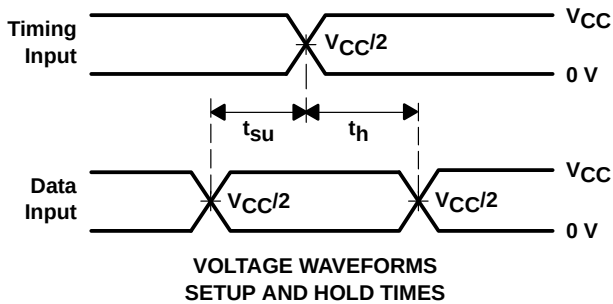
PARAMETER MEASUREMENT INFORMATION FOR B PORT

$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ AND $V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHZ}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

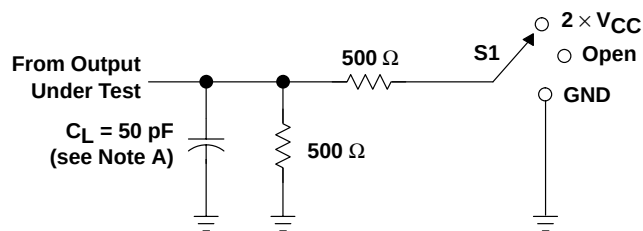
SN74LVCC3245A

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

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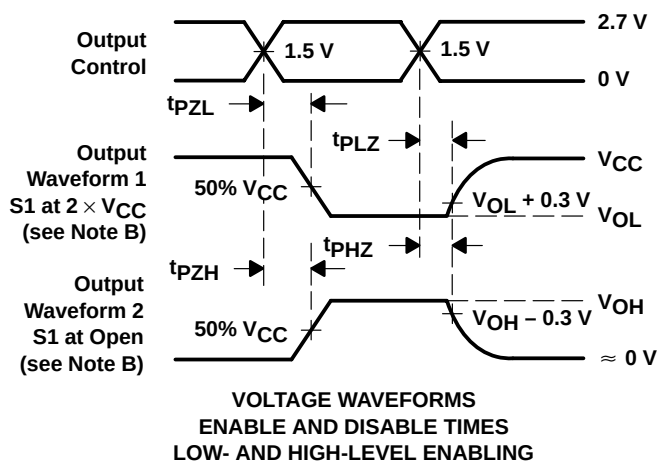
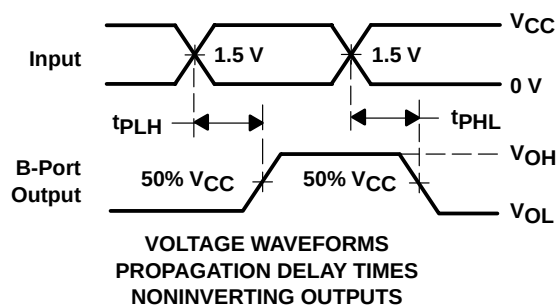
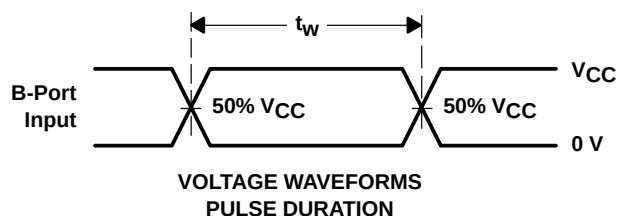
PARAMETER MEASUREMENT INFORMATION FOR B PORT

$V_{CCA} = 3.6 \text{ V}$ AND $V_{CCB} = 5.5 \text{ V}$



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.

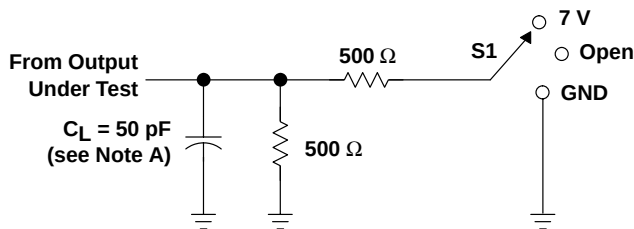
Figure 3. Load Circuit and Voltage Waveforms

SN74LVCC3245A

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

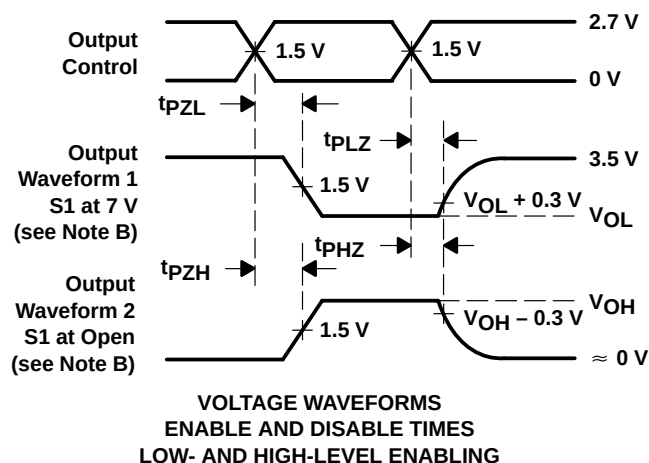
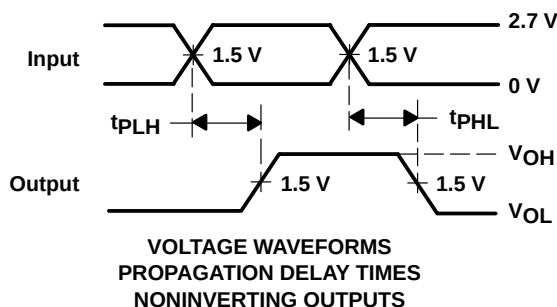
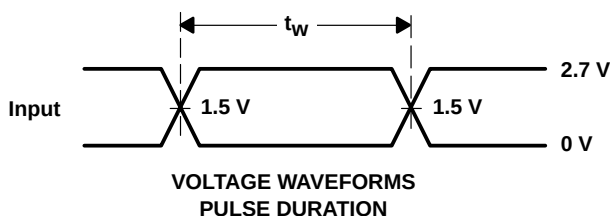
SCAS585E – NOVEMBER 1996 – REVISED MAY 1998

PARAMETER MEASUREMENT INFORMATION FOR A AND B PORT V_{CCA} AND $V_{CCB} = 3.6\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 4. Load Circuit and Voltage Waveforms

SN74LVC4245A

OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

SCAS375D – MARCH 1994 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **3.3-V to 5-V Bidirectional Level Shifter**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

description

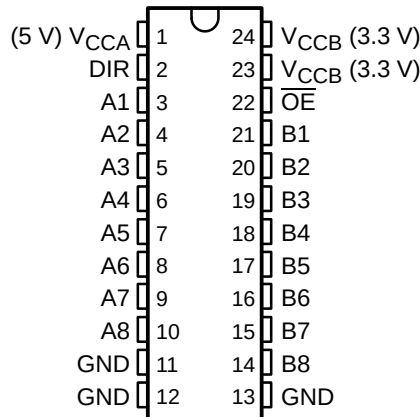
This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB} , which is set at 3.3 V, and A port has V_{CCA} , which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa.

The SN74LVC4245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The SN74LVC4245A pinout allows the designer to switch to a normal all-3.3-V or all-5-V 20-pin '245 device without board re-layout. The designer uses the data paths for pins 2–11 and 14–23 of the SN74LVC4245A to align with the conventional '245 pinout.

The SN74LVC4245A is characterized for operation from -40°C to 85°C .

DB, DW, OR PW PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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Logic diagram of the 74VHC147 decoder. The inputs are DIR (2), A1 (3), and A0 (1). The outputs are 22, OE, 21, and B1. The diagram shows two 3-input AND gates and two 2-input AND gates. A bracket indicates that there are seven other channels.

Supply voltage range, V_{CCA}		-0.5 V to 6.5 V
Input voltage range, V_I : A port (see Note 1)		-0.5 V to $V_{CCA} + 0.5$ V
Control inputs		-0.5 V to 6 V
Output voltage range, V_O : A port (see Note 1)		-0.5 V to $V_{CCA} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)		-50 mA
Output clamp current, I_{OK} ($V_O < 0$)		-50 mA
Continuous output current, I_O		± 50 mA
Continuous current through each V_{CCA} or GND		± 100 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package		104°C/W
DW package		81°C/W
PW package		120°C/W
Storage temperature range, T_{stg}		-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This value is limited to 6 V maximum.
2. The package thermal impedance is calculated in accordance with JESD 51.

SN74LVC4245A

OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range for $V_{CCB} = 3.3\text{ V}$ (unless otherwise noted)[†]

Supply voltage range, V_{CCB}	–0.5 V to 4.6 V
Input voltage range, V_I : B port (see Note 3)	–0.5 V to $V_{CCB} + 0.5\text{ V}$
Output voltage range, V_O : B port (see Note 3)	–0.5 V to $V_{CCB} + 0.5\text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CCB} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. The package thermal impedance is calculated in accordance with JESD 51.

3. This value is limited to 4.6 V maximum.

recommended operating conditions for $V_{CCA} = 5\text{ V}$ (see Note 4)

	MIN	MAX	UNIT
V_{CCA} Supply voltage	4.5	5.5	V
V_{IH} High-level input voltage	2		V
V_{IL} Low-level input voltage		0.8	V
V_I Input voltage	0	V_{CCA}	V
V_O Output voltage	0	V_{CCA}	V
I_{OH} High-level output current		–24	mA
I_{OL} Low-level output current		24	mA
T_A Operating free-air temperature	–40	85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions for $V_{CCB} = 3.3\text{ V}$ (see Note 4)

			MIN	MAX	UNIT
V _{CCB}	Supply voltage		2.7	3.6	V
V _{IH}	High-level input voltage	V _{CCB} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CCB} = 2.7 V to 3.6 V		0.8	V
V _I	Input voltage		0	V _{CCB}	V
V _O	Output voltage		0	V _{CCB}	V
I _{OH}	High-level output current	V _{CCB} = 2.7 V		–12	mA
		V _{CCB} = 3 V		–24	
I _{OL}	Low-level output current	V _{CCB} = 2.7 V		12	mA
		V _{CCB} = 3 V		24	
T _A	Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74LVC4245A

OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range for $V_{CCA} = 5\text{ V}$ (unless otherwise noted) (see Note 5)

PARAMETER		TEST CONDITIONS	V_{CCA}	MIN	TYP [†]	MAX	UNIT
V_{OH}		$I_{OH} = -100\text{ }\mu\text{A}$	4.5 V	4.3			V
			5.5 V	5.3			
		$I_{OH} = -24\text{ mA}$	4.5 V	3.7			
			5.5 V	4.7			
V_{OL}		$I_{OL} = 100\text{ }\mu\text{A}$	4.5 V			0.2	V
			5.5 V			0.2	
		$I_{OL} = 24\text{ mA}$	4.5 V			0.55	
			5.5 V			0.55	
I_I	Control inputs	$V_I = V_{CCA}$ or GND	5.5 V			± 1	μA
$I_{OZ}^{\ddagger}$	A port	$V_O = V_{CCA}$ or GND	5.5 V			± 5	μA
I_{CCA}		$V_I = V_{CCA}$ or GND, $I_O = 0$	5.5 V			80	μA
$\Delta I_{CCA}^{\S}$		One input at 3.4 V, Other inputs at V_{CCA} or GND	5.5 V			1.5	mA
C_i	Control inputs	$V_I = V_{CCA}$ or GND	Open		5		pF
C_{io}	A port	$V_O = V_{CCA}$ or GND	5 V		11		pF

[†] All typical values are measured at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or the associated V_{CC} .

NOTE 5: $V_{CCB} = 2.7\text{ V}$ to 3.6 V

electrical characteristics over recommended operating free-air temperature range for $V_{CCB} = 3.3\text{ V}$ (unless otherwise noted) (see Note 6)

PARAMETER		TEST CONDITIONS	V_{CCB}	MIN	TYP ^{†¶}	MAX	UNIT
V_{OH}		$I_{OH} = -100\text{ }\mu\text{A}$	2.7 V to 3.6 V	$V_{CC}-0.2$			V
			2.7 V	2.2			
		$I_{OH} = -12\text{ mA}$	3 V	2.4			
			3 V	2			
V_{OL}		$I_{OL} = 100\text{ }\mu\text{A}$	2.7 V to 3.6 V			0.2	V
		$I_{OL} = 12\text{ mA}$	2.7 V			0.4	
		$I_{OL} = 24\text{ mA}$	3 V			0.55	
$I_{OZ}^{\ddagger}$	B port	$V_O = V_{CCB}$ or GND	3.6 V			± 5	μA
I_{CCB}		$V_I = V_{CCB}$ or GND, $I_O = 0$	3.6 V			50	μA
$\Delta I_{CCB}^{\S}$		One input at $V_{CCB} - 0.6\text{ V}$, Other inputs at V_{CCB} or GND	2.7 V to 3.6 V			0.5	mA
C_{io}	B port	$V_O = V_{CCB}$ or GND	3.3 V		11		pF

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or the associated V_{CC} .

[¶] All typical values are measured at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

NOTE 6: $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$



SN74LVC4245A
OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER
WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCA} = 5 \text{ V} \pm 0.5 \text{ V}$, $V_{CCB} = 2.7 \text{ V TO } 3.6 \text{ V}$		UNIT
			MIN	MAX	
t_{PHL}	A	B	1	6.3	ns
t_{PLH}			1	6.7	
t_{PHL}	B	A	1	6.1	ns
t_{PLH}			1	5	
t_{PZL}	$\overline{OE}$	A	1	9	ns
t_{PZH}			1	8.1	
t_{PZL}	$\overline{OE}$	B	1	8.8	ns
t_{PZH}			1	9.8	
t_{PLZ}	$\overline{OE}$	A	1	7	ns
t_{PHZ}			1	5.8	
t_{PLZ}	$\overline{OE}$	B	1	7.7	ns
t_{PHZ}			1	7.8	

operating characteristics, $V_{CCA} = 5 \text{ V}$, $V_{CCB} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 0$, $f = 10 \text{ MHz}$	39.5	pF
		Outputs disabled		5	



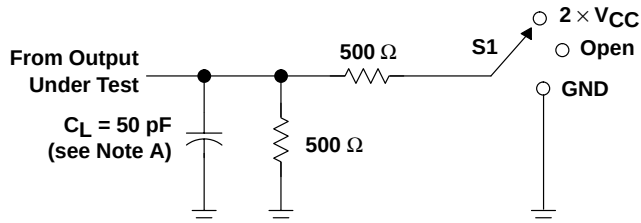
SN74LVC4245A

OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER

WITH 3-STATE OUTPUTS

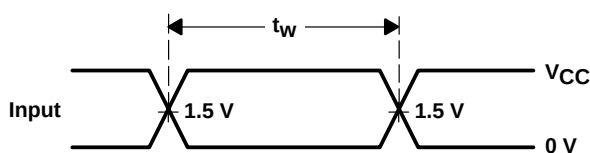
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PARAMETER MEASUREMENT INFORMATION (A PORT)

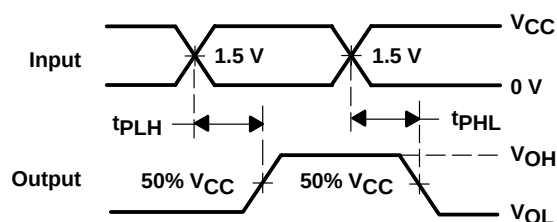


LOAD CIRCUIT

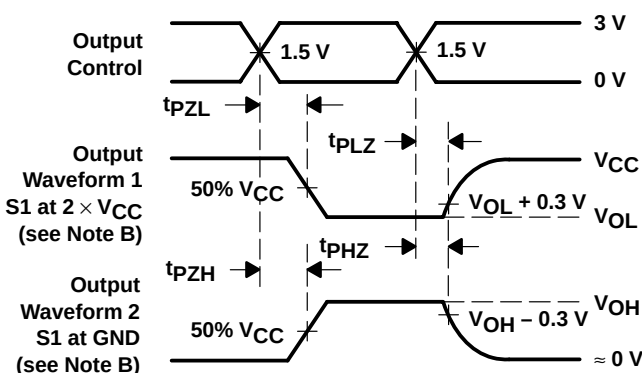
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.

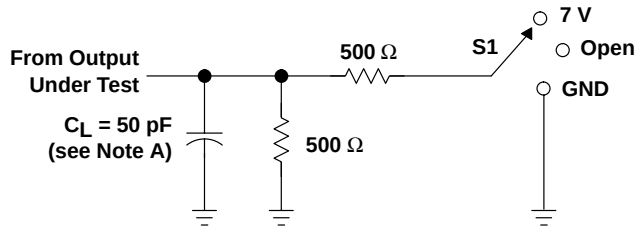
Figure 1. Load Circuit and Voltage Waveforms

SN74LVC4245A

OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

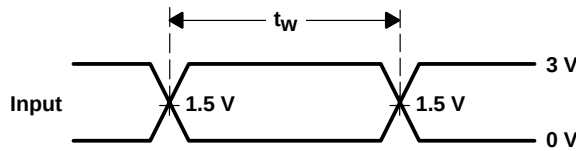
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PARAMETER MEASUREMENT INFORMATION (B PORT)

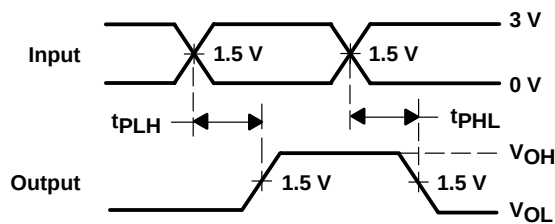


LOAD CIRCUIT

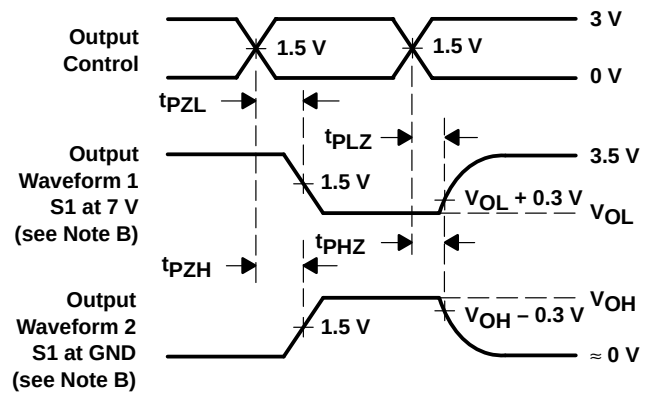
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

SN74LVCC4245A

OCTAL DUAL-SUPPLY BUS TRANSCEIVER

WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

SCAS584E – NOVEMBER 1996 – REVISED APRIL 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

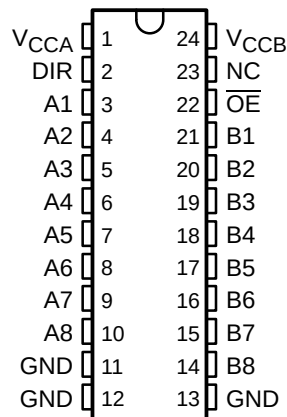
description

This 8-bit (octal) noninverting bus transceiver uses two separate power-supply rails. The A port, V_{CCA} , is dedicated to accept a 5-V supply level, and the configurable B port, which is designed to track V_{CCB} , accepts voltages from 3 V to 5 V. This allows for translation from a 3.3-V to a 5-V environment and vice versa.

The SN74LVCC4245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The SN74LVCC4245A is characterized for operation from -40°C to 85°C .

**DB, DW, OR PW PACKAGE
(TOP VIEW)**



NC – No internal connection

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

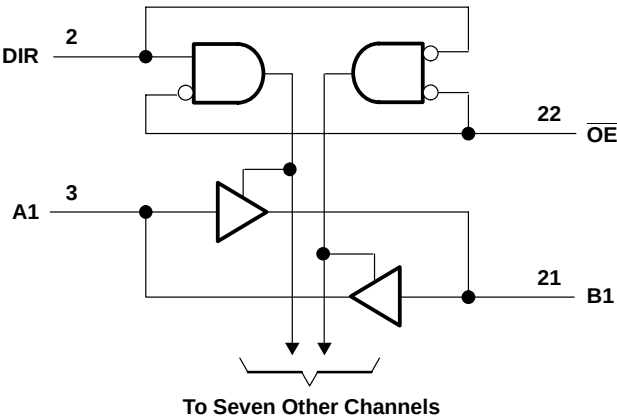


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SN74LVCC4245A
OCTAL DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS
SCAS584E – NOVEMBER 1996 – REVISED APRIL 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CCA} and V _{CCB}	−0.5 V to 6 V
Input voltage range, V _I (see Note 1): I/O ports (A port)	−0.5 to V _{CCA} + 0.5 V
I/O ports (B port)	−0.5 to V _{CCB} + 0.5 V
Except I/O ports	−0.5 to V _{CCA} + 0.5 V
Output voltage range, V _O (see Note 1): (A port)	−0.5 to V _{CCA} + 0.5 V
(B port)	−0.5 to V _{CCB} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	−50 mA
Output clamp current, I _{OK} (V _O < 0)	−50 mA
Continuous output current, I _O	±50 mA
Continuous current through V _{CCA} , V _{CCB} , or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 2): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T _{stg}	−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. This value is limited to 6 V maximum.
 2. The package thermal impedance is calculated in accordance with JESD 51.

SN74LVCC4245A
OCTAL DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

SCAS584E – NOVEMBER 1996 – REVISED APRIL 1998

recommended operating conditions (see Note 3)

		V _{CCA}	V _{CCB}	MIN	NOM	MAX	UNIT
V _{CCA}	Supply voltage			4.5	5	5.5	V
V _{CCB}	Supply voltage			2.7	3.3	5.5	V
V _{IHA}	High-level input voltage	4.5 V	2.7 V	2			V
			3.6 V	2			
			5.5 V	2			
V _{IHB}	High-level input voltage	4.5 V	2.7 V	2			V
			3.6 V	2			
			5.5 V	3.85			
V _{ILA}	Low-level input voltage	4.5 V	2.7 V			0.8	V
			3.6 V			0.8	
			5.5 V			0.8	
V _{ILB}	Low-level input voltage	4.5 V	2.7 V			0.8	V
			3.6 V			0.8	
			5.5 V			1.65	
V _{IA}	Input voltage			0		V _{CCA}	V
V _{IB}	Input voltage			0		V _{CCB}	V
V _{OA}	Output voltage			0		V _{CCA}	V
V _{OB}	Output voltage			0		V _{CCB}	V
I _{OHA}	High-level output current	4.5 V	3 V			–24	mA
I _{OHB}	High-level output current	4.5 V	2.7 V to 4.5 V			–24	mA
I _{OLA}	Low-level output current	4.5 V	3 V			24	mA
I _{OLB}	Low-level output current	4.5 V	2.7 V to 4.5 V			24	mA
T _A	Operating free-air temperature			–40		85	°C

NOTE 3: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVCC4245A
OCTAL DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

SCAS584E – NOVEMBER 1996 – REVISED APRIL 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	MIN	TYP	MAX	UNIT
V _{OHA}		I _{OH} = –100 µA	4.5 V	3 V	4.4	4.49		V
		I _{OH} = –24 mA	4.5 V	3 V	3.76	4.25		
V _{OHB}		I _{OH} = –100 µA	4.5 V	3 V	2.9	2.99		V
		I _{OH} = –12 mA	4.5 V	2.7 V	2.2	2.5		
				3 V	2.46	2.85		
		I _{OH} = –24 mA	4.5 V	2.7 V	2.1	2.3		
				3 V	2.25	2.65		
				4.5 V	3.76	4.25		
V _{OLA}		I _{OL} = 100 µA	4.5 V	3 V			0.1	V
		I _{OL} = 24 mA	4.5 V	3 V		0.21	0.44	
V _{OLB}		I _{OL} = 100 µA	4.5 V	3 V			0.1	V
		I _{OL} = 12 mA	4.5 V	2.7 V		0.11	0.44	
		I _{OL} = 24 mA	4.5 V	2.7 V		0.22	0.5	
				3 V		0.21	0.44	
				4.5 V		0.18	0.44	
I _I	Control inputs	V _I = V _{CCA} or GND	5.5 V	3.6 V		±0.1	±1	µA
				5.5 V		±0.1	±1	
I _{OZ} [†]	A or B ports	V _O = V _{CCA/B} or GND, V _I = V _{IL} or V _{IH}	5.5 V	3.6 V		±0.5	±5	µA
I _{CCA}	B to A	A _n = V _{CC} or GND	5.5 V	Open		8	80	µA
		I _O (A port) = 0, B _n = V _{CCB} or GND	5.5 V	3.6 V		8	80	
				5.5 V		8	80	
I _{CCB}	A to B	A _n = V _{CCA} or GND, I _O (B port) = 0	5.5 V	3.6 V		5	50	µA
				5.5 V		8	80	
ΔI _{CCA} [‡]	A port	V _I = V _{CCA} – 2.1 V, Other inputs at V _{CCA} or GND, $\overline{\text{OE}}$ at GND and DIR at V _{CCA}	5.5 V	5.5 V		1.35	1.5	mA
	$\overline{\text{OE}}$	V _I = V _{CCA} – 2.1 V, Other inputs at V _{CCA} or GND, DIR at V _{CCA} or GND	5.5 V	5.5 V		1	1.5	
	DIR	V _I = V _{CCA} – 2.1 V, Other inputs at V _{CCA} or GND, $\overline{\text{OE}}$ at V _{CCA} or GND	5.5 V	3.6 V		1	1.5	
ΔI _{CCB} [‡]	B port	V _I = V _{CCB} – 0.6 V, Other inputs at V _{CCB} or GND, $\overline{\text{OE}}$ at GND and DIR at GND	5.5 V	3.6 V		0.35	0.5	mA
C _i	Control inputs	V _I = V _{CCA} or GND	Open	Open		5		pF
C _{io}	A or B ports	V _O = V _{CCA/B} or GND	5 V	3.3 V		11		pF

[†] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or the associated V_{CC}.



SN74LVCC4245A
OCTAL DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figures 1 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCA} = 5 \text{ V} \pm 0.5 \text{ V}$, $V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		$V_{CCA} = 5 \text{ V} \pm 0.5 \text{ V}$, $V_{CCB} = 2.7 \text{ V TO } 3.6 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{PHL}	A	B	1	7.1	1	7	ns
t_{PLH}			1	6	1	7	
t_{PHL}	B	A	1	6.8	1	6.2	ns
t_{PLH}			1	6.1	1	5.3	
t_{PZL}	$\overline{OE}$	A	1	9	1	9	ns
t_{PZH}			1	8.3	1	8	
t_{PZL}	$\overline{OE}$	B	1	8.2	1	10	ns
t_{PZH}			1	8.1	1	10.2	
t_{PLZ}	$\overline{OE}$	A	1	4.7	1	5.2	ns
t_{PHZ}			1	4.9	1	5.2	
t_{PLZ}	$\overline{OE}$	B	1	5.4	1	5.4	ns
t_{PHZ}			1	6.3	1	7.4	

operating characteristics, $V_{CCA} = 5 \text{ V}$, $V_{CCB} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 0$, $f = 10 \text{ MHz}$	20	pF
		Outputs disabled		6.5	

SN74LVCC4245A

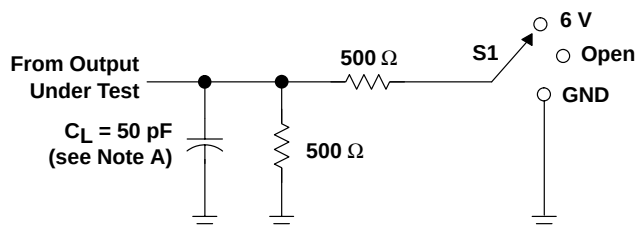
OCTAL DUAL-SUPPLY BUS TRANSCEIVER

WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

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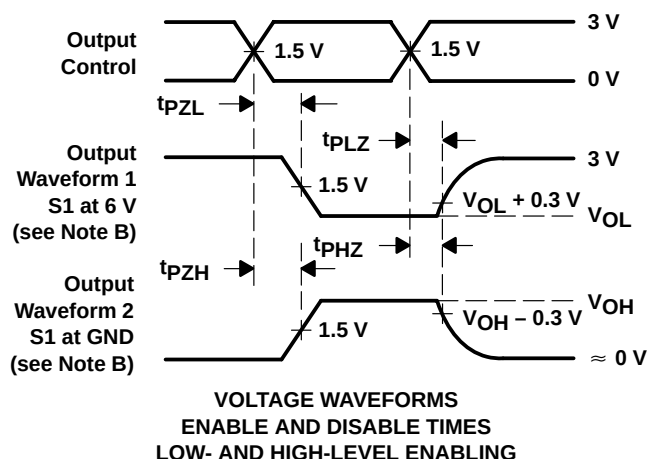
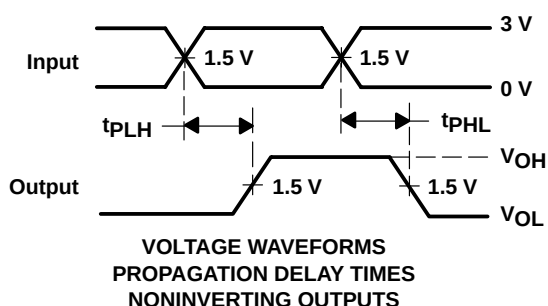
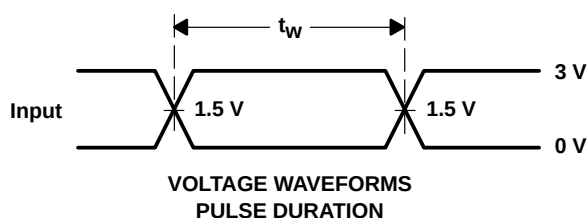
PARAMETER MEASUREMENT INFORMATION FOR A TO B

$V_{CCA} = 4.5 \text{ V TO } 5.5 \text{ V}$ AND $V_{CCB} = 2.7 \text{ V TO } 3.6 \text{ V}$



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.

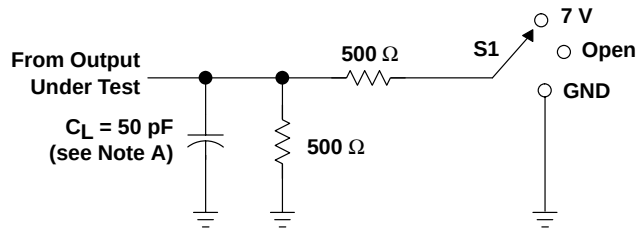
Figure 1. Load Circuit and Voltage Waveforms

SN74LVCC4245A
OCTAL DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

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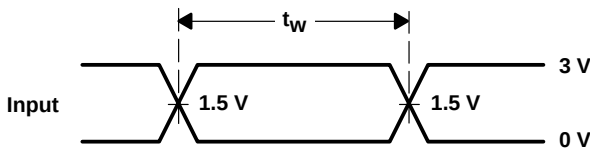
PARAMETER MEASUREMENT INFORMATION FOR A TO B

$V_{CCA} = 4.5\text{ V TO }5.5\text{ V AND }V_{CCB} = 3.6\text{ V TO }5.5\text{ V}$

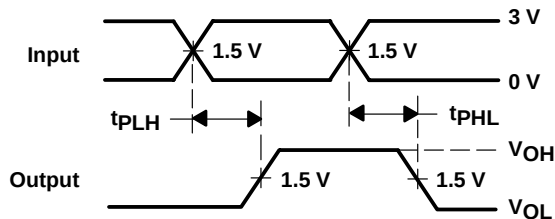


LOAD CIRCUIT

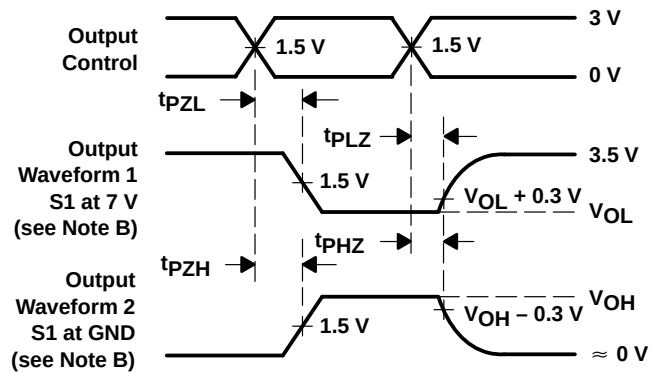
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

SN74LVCC4245A

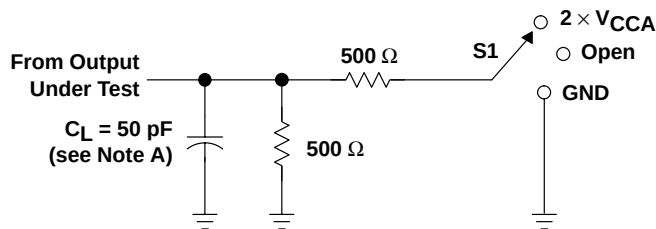
OCTAL DUAL-SUPPLY BUS TRANSCEIVER

WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

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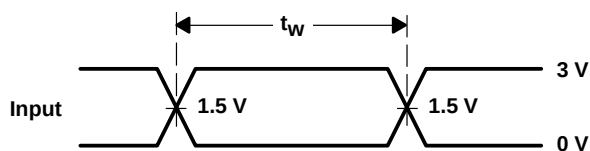
PARAMETER MEASUREMENT INFORMATION FOR B TO A

$V_{CCA} = 4.5 \text{ V TO } 5.5 \text{ V}$ AND $V_{CCB} = 2.7 \text{ V TO } 3.6 \text{ V}$

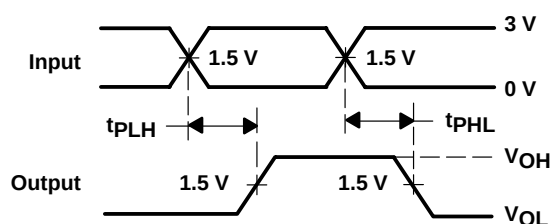


LOAD CIRCUIT

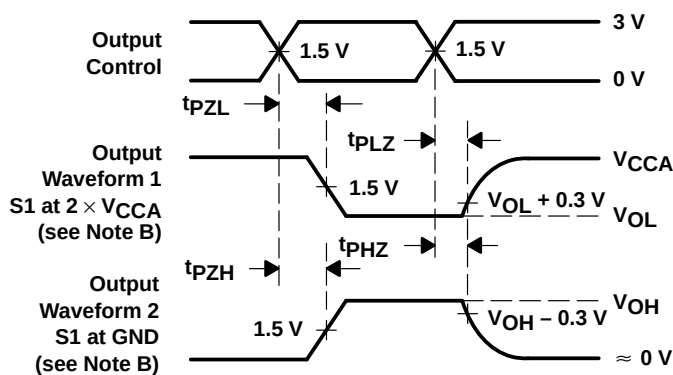
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CCA}$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

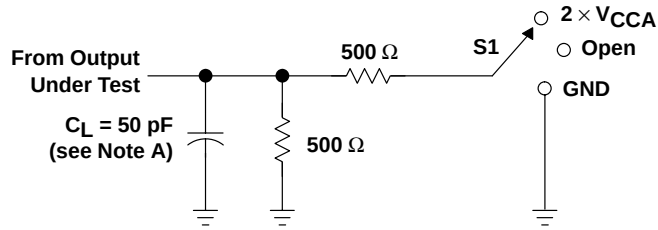
- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuit and Voltage Waveforms

SN74LVCC4245A
OCTAL DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

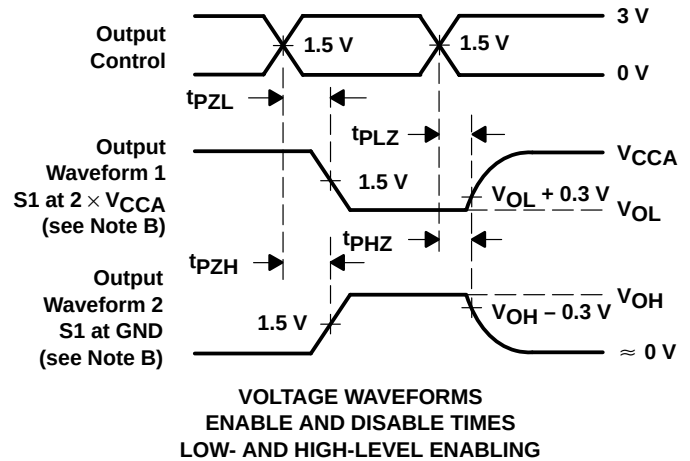
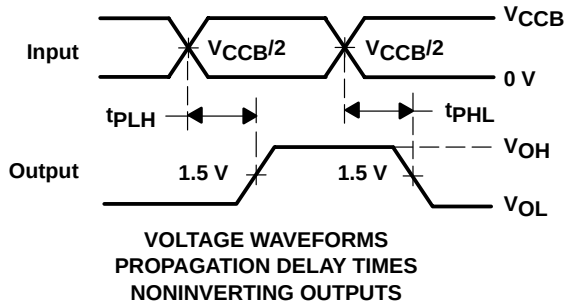
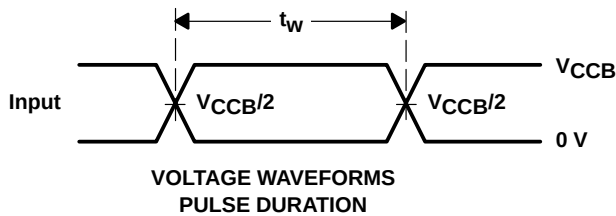
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PARAMETER MEASUREMENT INFORMATION FOR B TO A
 $V_{CCA} = 4.5 \text{ V TO } 5.5 \text{ V}$ AND $V_{CCB} = 3.6 \text{ V TO } 5.5 \text{ V}$



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCA}$
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 4. Load Circuit and Voltage Waveforms

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SN54LV00A, SN74LV00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and 300-mil DIPs (J)

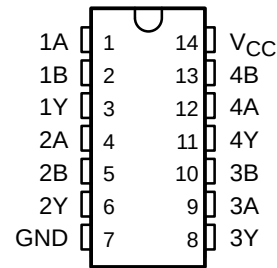
description

These quadruple 2-input positive-NAND gates are designed for 2-V to 5.5-V V_{CC} operation.

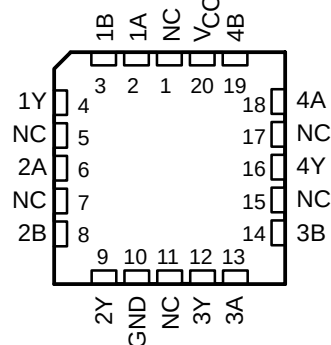
The 'LV00A devices perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54LV00A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV00A is characterized for operation from -40°C to 85°C .

SN54LV00A . . . J OR W PACKAGE
SN74LV00A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV00A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

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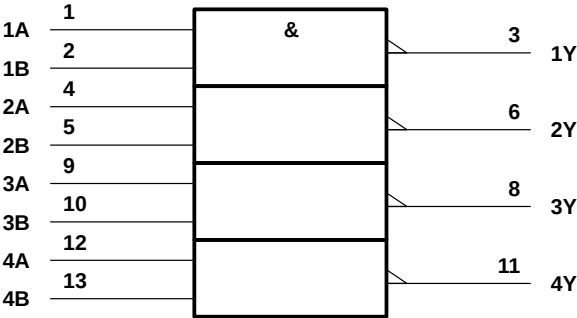
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SN54LV00A, SN74LV00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

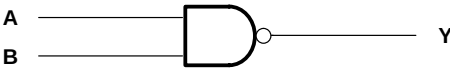
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
DGV package	182°C/W
NS package	127°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV00A, SN74LV00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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recommended operating conditions (see Note 4)

		SN54LV00A		SN74LV00A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	–50	–50		μA
		V _{CC} = 2.3 V to 2.7 V	–2	–2		
		V _{CC} = 3 V to 3.6 V	–6	–6		
		V _{CC} = 4.5 V to 5.5 V	–12	–12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50		μA
		V _{CC} = 2.3 V to 2.7 V	2	2		
		V _{CC} = 3 V to 3.6 V	6	6		
		V _{CC} = 4.5 V to 5.5 V	12	12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV00A			SN74LV00A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –6 mA	3 V	2.48			2.48			
	I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	3.4			3.4			pF
		5 V	3.4			3.4			

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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SN54LV00A, SN74LV00A

QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV00A		SN74LV00A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF		7.1	12.9	1	16	1	15	ns
t _{pd}	A	Y	C _L = 50 pF		9.6	16.6	1	21	1	20	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV00A		SN74LV00A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF		5	7.9	1	10.5	1	9.5	ns
t _{pd}	A	Y	C _L = 50 pF		6.9	11.4	1	14	1	13	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV00A		SN74LV00A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF		3.6	5.5	1	7.5	1	6.5	ns
t _{pd}	A	Y	C _L = 50 pF		4.9	7.5	1	9.5	1	8.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER						SN74LV00A			UNIT
						MIN	TYP	MAX	
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}						0.2	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}						−0.1	−0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}						3.1		V
V _{IH(D)}	High-level dynamic input voltage						2.31		V
V _{IL(D)}	Low-level dynamic input voltage							0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

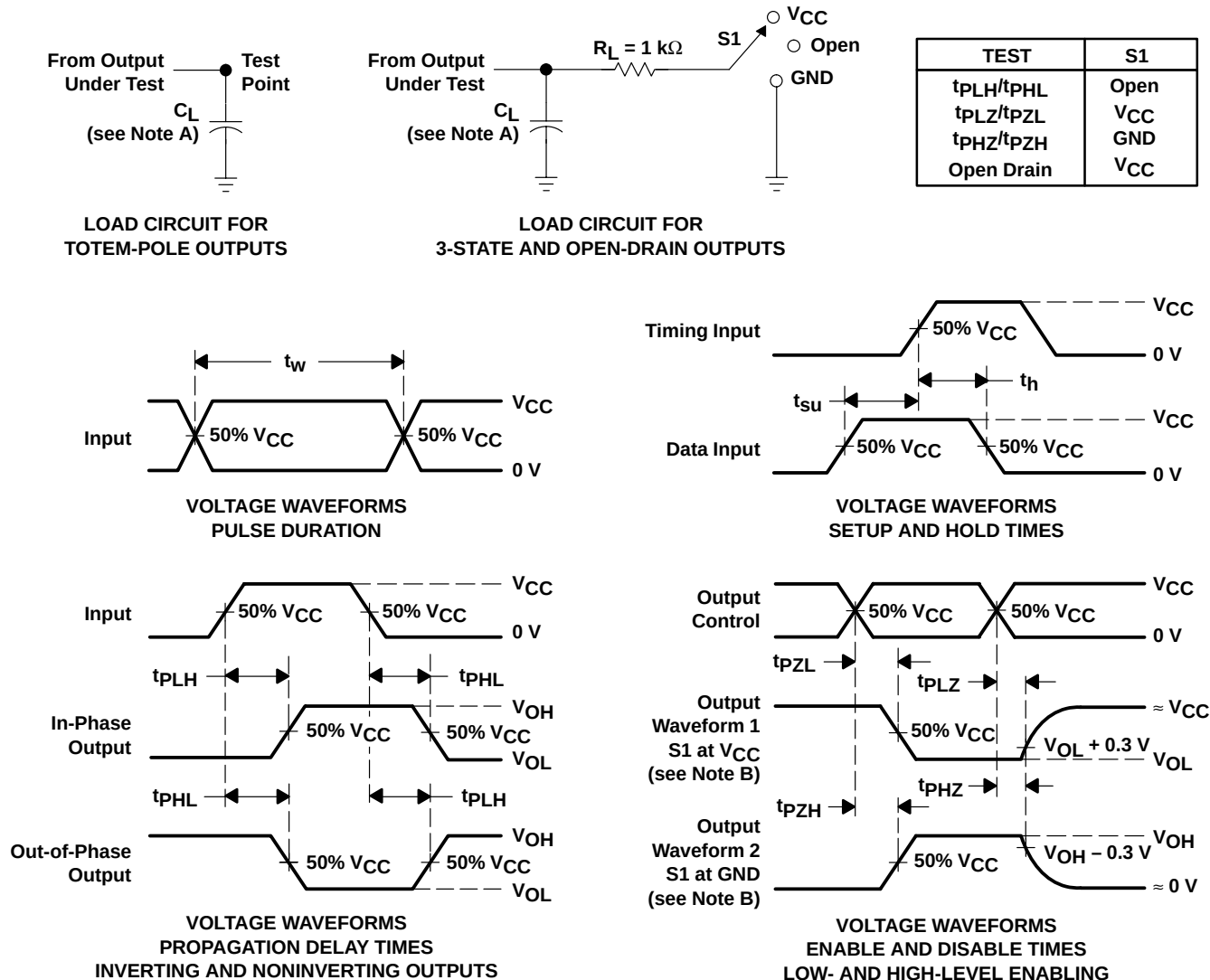
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance	C _L = 50 pF, f = 10 MHz		3.3 V	9.5	pF
				5 V	11	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV02A, SN74LV02A QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCLS390B – APRIL 1998 – REVISED JULY 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 $< 0.8\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 $> 2\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

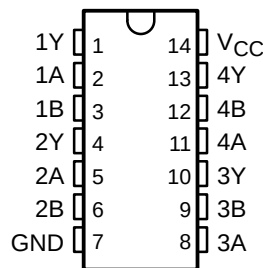
description

The 'LV02A devices are quadruple 2-input positive-NOR gates designed for 2-V to 5.5-V V_{CC} operation.

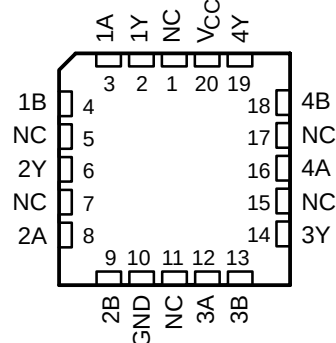
The 'LV02A devices perform the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54LV02A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV02A is characterized for operation from -40°C to 85°C .

SN54LV02A . . . J OR W PACKAGE
SN74LV02A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV02A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT Y
A	B	
H	X	L
X	H	L
L	L	H

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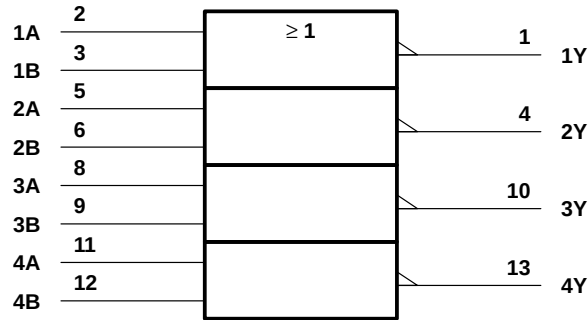
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SN54LV02A, SN74LV02A
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCLS390B – APRIL 1998 – REVISED JULY 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
DGV package	182°C/W
NS package	127°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV02A, SN74LV02A QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCLS390B – APRIL 1998 – REVISED JULY 1998

recommended operating conditions (see Note 4)

		SN54LV02A		SN74LV02A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	–50	–50		μA
		V _{CC} = 2.3 V to 2.7 V	–2	–2		
		V _{CC} = 3 V to 3.6 V	–6	–6		
		V _{CC} = 4.5 V to 5.5 V	–12	–12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50		μA
		V _{CC} = 2.3 V to 2.7 V	2	2		
		V _{CC} = 3 V to 3.6 V	6	6		
		V _{CC} = 4.5 V to 5.5 V	12	12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200		ns/V
		V _{CC} = 3 V to 3.6 V	0	100		
		V _{CC} = 4.5 V to 5.5 V	0	20		
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV02A			SN74LV02A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –6 mA	3 V	2.48			2.48			
	I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	1.6			1.6			pF

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SN54LV02A, SN74LV02A

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCLS390B – APRIL 1998 – REVISED JULY 1998

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV02A		SN74LV02A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A or B	Y	$C_L = 15\text{ pF}$		8.3	12.4	1	15	1	15	ns
t_{pd}	A or B	Y	$C_L = 50\text{ pF}$		11	16.1	1	19	1	19	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV02A		SN74LV02A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A or B	Y	$C_L = 15\text{ pF}$		5.6	7.9	1	9.5	1	9.5	ns
t_{pd}	A or B	Y	$C_L = 50\text{ pF}$		7.6	11.4	1	13	1	13	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV02A		SN74LV02A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A or B	Y	$C_L = 15\text{ pF}$		3.9	5.5	1	6.5	1	6.5	ns
t_{pd}	A or B	Y	$C_L = 50\text{ pF}$		5.3	7.5	1	8.5	1	8.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV02A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.2	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.1	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.2		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

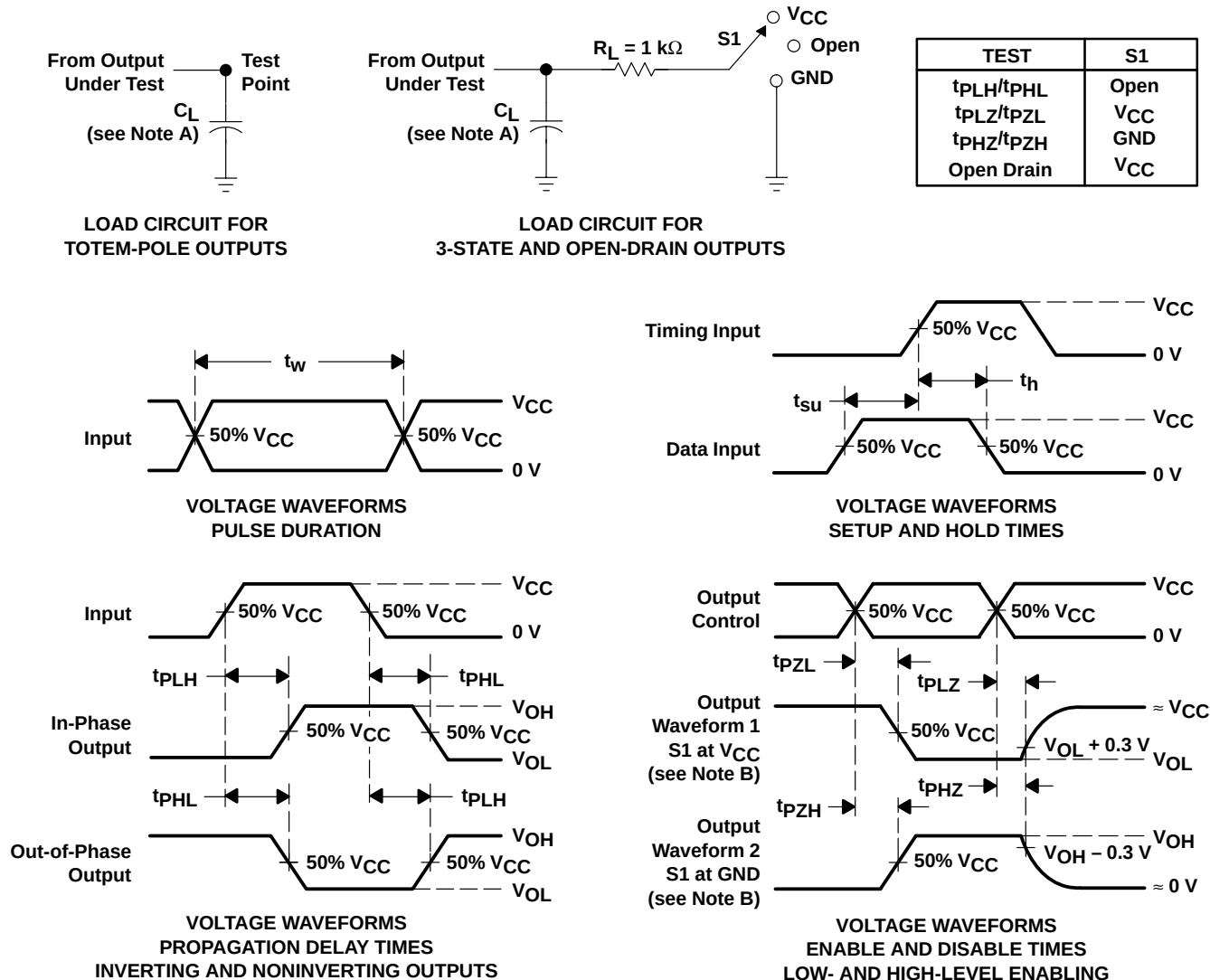
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	8.9	pF
			5 V	10.3	

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

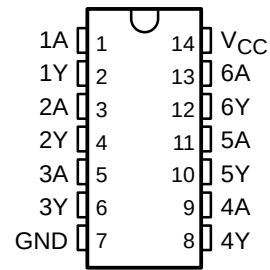
description

These hex inverters are designed for 2-V to 5.5-V V_{CC} operation.

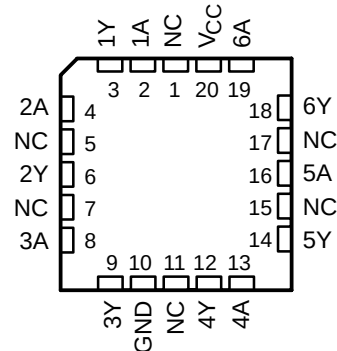
The 'LV04A devices contain six independent inverters. These devices perform the Boolean function $Y = \bar{A}$.

The SN54LV04A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV04A is characterized for operation from -40°C to 85°C .

SN54LV04A . . . J OR W PACKAGE
SN74LV04A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV04A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

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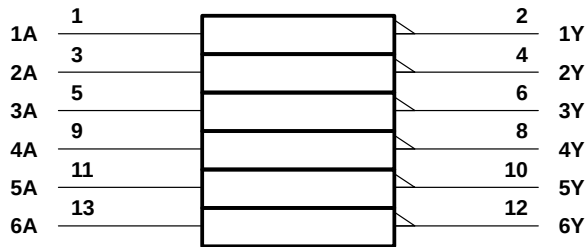
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SN54LV04A, SN74LV04A
HEX INVERTERS

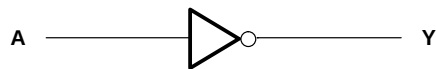
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
DGV package	182°C/W
NS package	127°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV04A, SN74LV04A HEX INVERTERS

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recommended operating conditions (see Note 4)

			SN54LV04A		SN74LV04A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		–50		–50	μA
		V _{CC} = 2.3 V to 2.7 V		–2		–2	
		V _{CC} = 3 V to 3.6 V		–6		–6	
		V _{CC} = 4.5 V to 5.5 V		–12		–12	
I _{OL}	Low-level output current	V _{CC} = 2 V		50		50	μA
		V _{CC} = 2.3 V to 2.7 V		2		2	
		V _{CC} = 3 V to 3.6 V		6		6	
		V _{CC} = 4.5 V to 5.5 V		12		12	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV04A			SN74LV04A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –6 mA	3 V	2.48			2.48			
	I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I _{OL} = 2 mA	2.3 V			0.4			0.4	
	I _{OL} = 6 mA	3 V			0.44			0.44	
	I _{OL} = 12 mA	4.5 V			0.55			0.55	
I _I	V _I = V _{CC} or GND	5.5 V			±1			±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			20			20	μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V			5			5	μA
C _i	V _I = V _{CC} or GND	3.3 V		2.3			2.3		pF
		5 V		2.3			2.3		

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SN54LV04A, SN74LV04A HEX INVERTERS

SCLS388B – SEPTEMBER 1997 – REVISED JUNE 1998

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV04A		SN74LV04A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$		7.1	11.7	1	14	1	14	ns
t_{pd}	A	Y	$C_L = 50\text{ pF}$		10	15.5	1	18	1	18	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV04A		SN74LV04A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$		5.1	7.1	1	8.5	1	8.5	ns
t_{pd}	A	Y	$C_L = 50\text{ pF}$		7.3	10.6	1	12	1	12	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV04A		SN74LV04A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$		3.6	5.5	1	6.5	1	6.5	ns
t_{pd}	A	Y	$C_L = 50\text{ pF}$		5.1	7.5	1	8.5	1	8.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER			SN74LV04A			UNIT
			MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.26	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			-0.01	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}			3.1		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage				0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

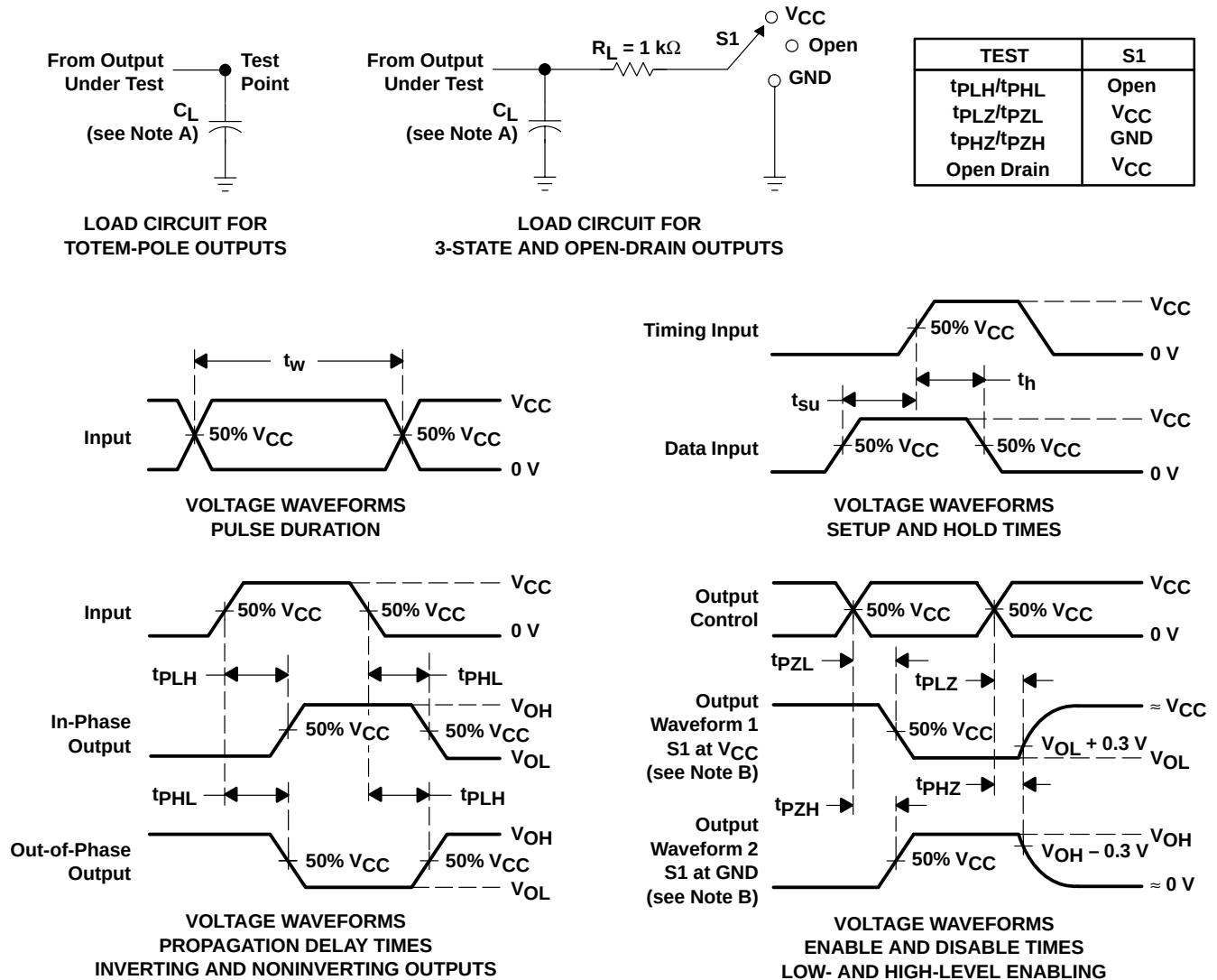
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	9.6	pF
			5 V	11.4	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LVU04A, SN74LVU04A HEX INVERTERS

SCES130C – MARCH 1998 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Unbuffered Outputs**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

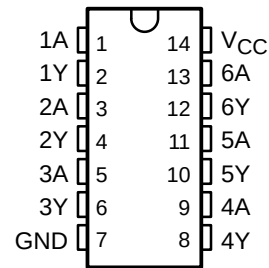
description

These hex inverters are designed for 2-V to 5.5-V V_{CC} operation.

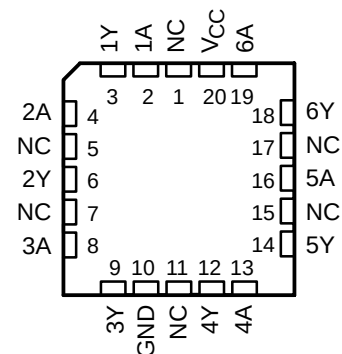
The 'LVU04A devices contain six independent inverters with unbuffered outputs. These devices perform the Boolean function $Y = \bar{A}$.

The SN54LVU04A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVU04A is characterized for operation from -40°C to 85°C .

SN54LVU04A ... J OR W PACKAGE
SN74LVU04A ... D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LVU04A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

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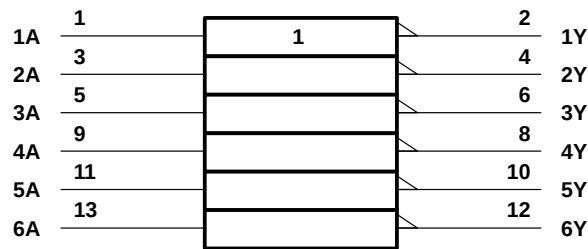
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SN54LVU04A, SN74LVU04A
HEX INVERTERS

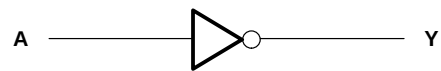
SCES130C – MARCH 1998 – REVISED JUNE 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
DGV package	182°C/W
NS package	127°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LVU04A, SN74LVU04A HEX INVERTERS

SCES130C – MARCH 1998 – REVISED JUNE 1998

recommended operating conditions (see Note 4)

			SN54LVU04A		SN74LVU04A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.7		1.7		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.8		V _{CC} × 0.8		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.8		V _{CC} × 0.8		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.8		V _{CC} × 0.8		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.3		0.3	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.2		V _{CC} × 0.2	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.2		V _{CC} × 0.2	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.2		V _{CC} × 0.2	
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		–50		–50	μA
		V _{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V _{CC} = 3 V to 3.6 V		–6		–6	
		V _{CC} = 4.5 V to 5.5 V		–12		–12	
I _{OL}	Low-level output current	V _{CC} = 2 V		50		50	μA
		V _{CC} = 2.3 V to 2.7 V		2		2	mA
		V _{CC} = 3 V to 3.6 V		6		6	
		V _{CC} = 4.5 V to 5.5 V		12		12	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVU04A			SN74LVU04A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –6 mA	3 V	2.48			2.48			
	I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
C _i	V _I = V _{CC} or GND	3.3 V	4			4			pF

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SN54LVU04A, SN74LVU04A HEX INVERTERS

SCES130C – MARCH 1998 – REVISED JUNE 1998

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LVU04A		SN74LVU04A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$		3.2	10.9	1	14	1	14	ns
t_{pd}	A	Y	$C_L = 50\text{ pF}$		6.6	13.4	1	16	1	16	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LVU04A		SN74LVU04A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$		2.5	8.9	1	10.5	1	10.5	ns
t_{pd}	A	Y	$C_L = 50\text{ pF}$		4.7	11.4	1	13	1	13	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LVU04A		SN74LVU04A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$		2.2	5.5	1	6.5	1	6.5	ns
t_{pd}	A	Y	$C_L = 50\text{ pF}$		3.9	7	1	8	1	8	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER				SN74LVU04A			UNIT
				MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}				0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}				-0.1	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				3		V
$V_{IH(D)}$	High-level dynamic input voltage				2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage					0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

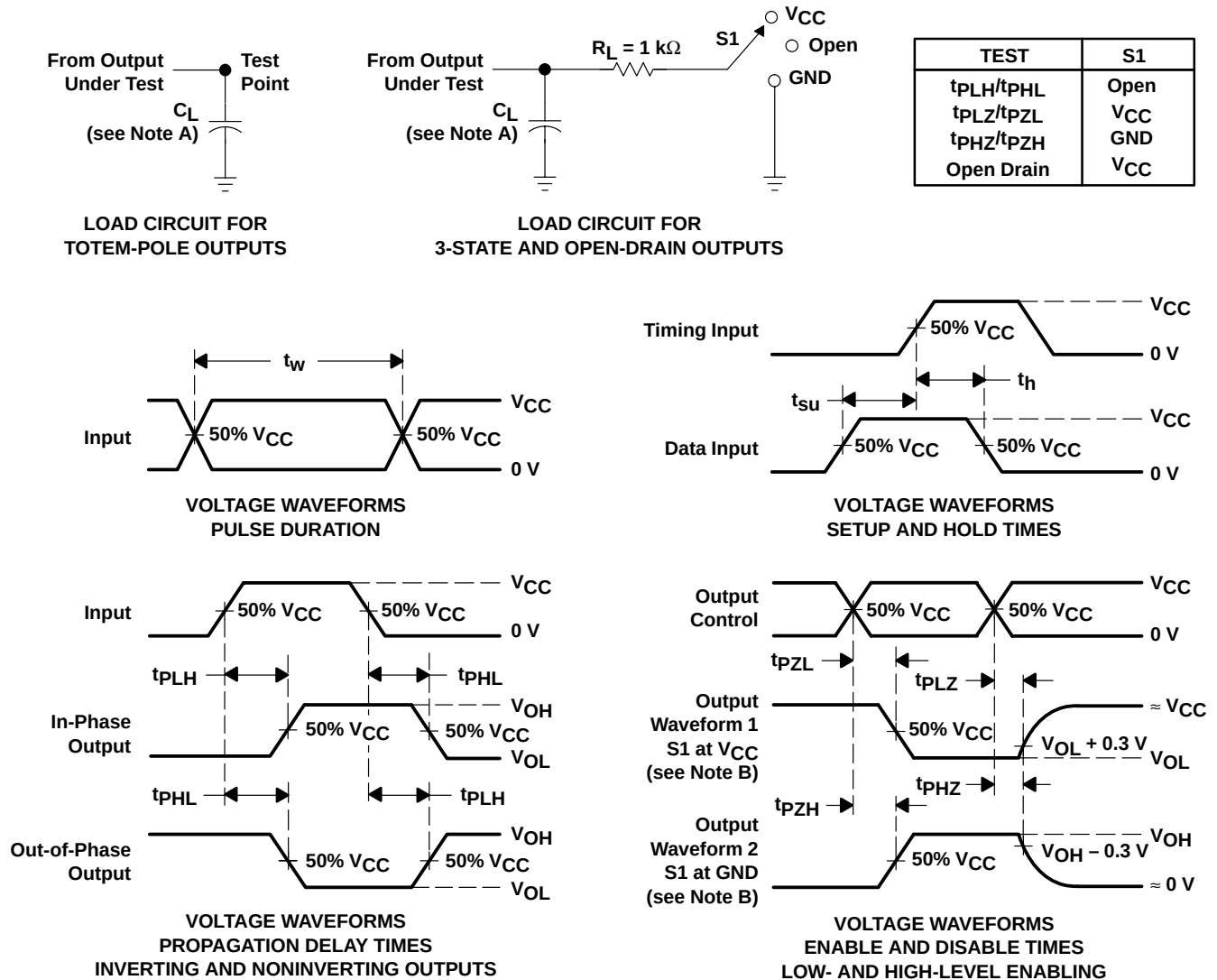
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$	$f = 10\text{ MHz}$	3.3 V	5.6	pF
				5 V	6.7	

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV05A, SN74LV05A HEX INVERTERS WITH OPEN-DRAIN OUTPUTS

SCLS391B – APRIL 1998 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

description

The 'LV05A devices contain six independent inverters designed for 2-V to 5.5-V V_{CC} operation.

These devices perform the Boolean function $Y = \bar{A}$.

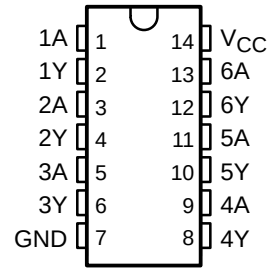
The open-drain outputs require pullup resistors to perform correctly and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

The SN54LV05A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV05A is characterized for operation from -40°C to 85°C .

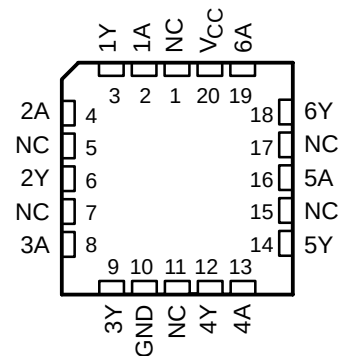
FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

SN54LV05A . . . J OR W PACKAGE
SN74LV05A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV05A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

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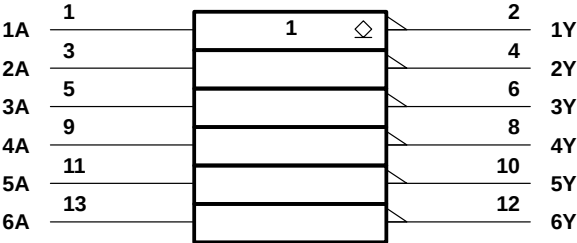
SN54LV05A, SN74LV05A

HEX INVERTERS

WITH OPEN-DRAIN OUTPUTS

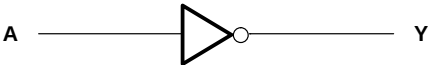
SCLS391B – APRIL 1998 – REVISED JUNE 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
DGV package	182°C/W
NS package	127°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

PRODUCT PREVIEW

recommended operating conditions (see Note 4)

			SN54LV05A		SN74LV05A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OL}	Low-level output current	V _{CC} = 2 V		50		50	μA
		V _{CC} = 2.3 V to 2.7 V		2		2	
		V _{CC} = 3 V to 3.6 V		6		6	
		V _{CC} = 4.5 V to 5.5 V		12		12	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54LV05A		SN74LV05A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V			0.1		0.1		0.1	V
	I _{OL} = 2 mA	2.3 V			0.4		0.4		0.4	
	I _{OL} = 6 mA	3 V			0.44		0.44		0.44	
	I _{OL} = 12 mA	4.5 V			0.55		0.55		0.55	
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		20		20	μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V			5		5		5	μA

PRODUCT PREVIEW

SN54LV05A, SN74LV05A HEX INVERTERS WITH OPEN-DRAIN OUTPUTS

SCLS391B – APRIL 1998 – REVISED JUNE 1998

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV05A		SN74LV05A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$								ns
t_{pd}	A	Y	$C_L = 50\text{ pF}$								ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV05A		SN74LV05A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$								ns
t_{pd}	A	Y	$C_L = 50\text{ pF}$								ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV05A		SN74LV05A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$								ns
t_{pd}	A	Y	$C_L = 50\text{ pF}$								ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

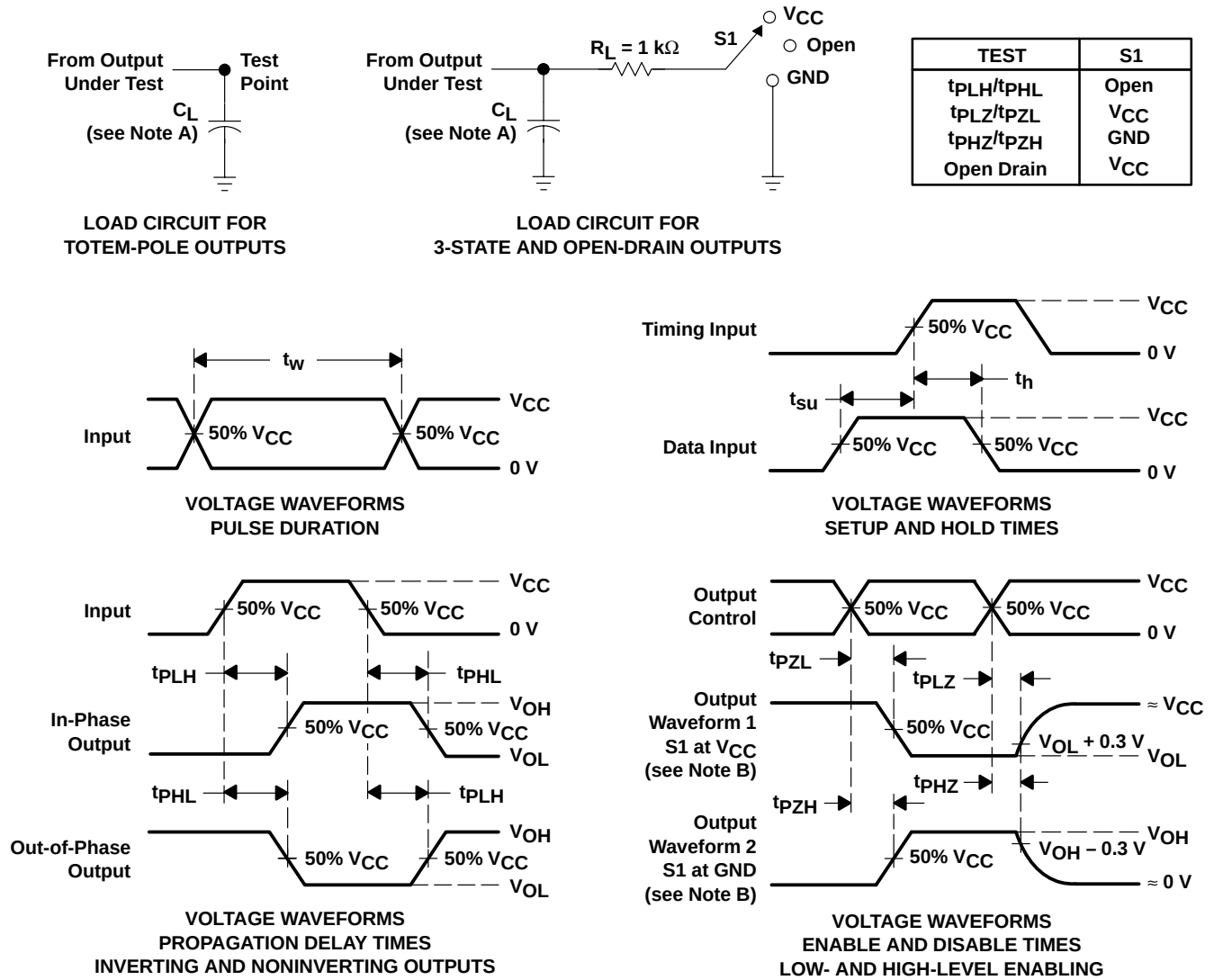
PARAMETER				SN74LV05A			UNIT
				MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}						V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}						V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}						V
$V_{IH(D)}$	High-level dynamic input voltage						V
$V_{IL(D)}$	Low-level dynamic input voltage						V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V		pF
			5 V		

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV08A, SN74LV08A QUADRUPLE 2-INPUT POSITIVE-AND GATES

SCLS387B – SEPTEMBER 1997 – REVISED MAY 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

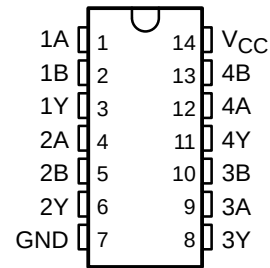
description

These quadruple 2-input positive-AND gates are designed for 2-V to 5.5-V V_{CC} operation.

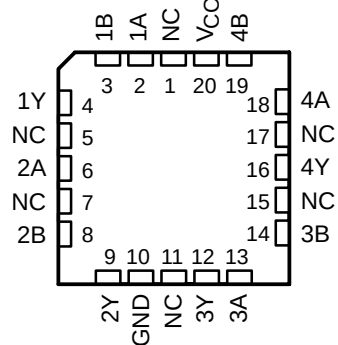
The 'LV08A devices perform the Boolean function $Y = A \bullet B$ or $Y = \overline{A + B}$ in positive logic.

The SN54LV08A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV08A is characterized for operation from -40°C to 85°C .

SN54LV08A . . . J OR W PACKAGE
SN74LV08A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV08A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

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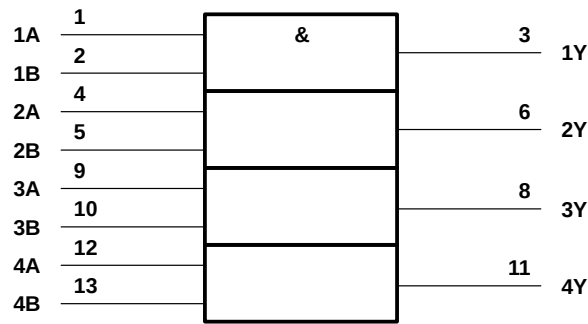
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SN54LV08A, SN74LV08A
QUADRUPLE 2-INPUT POSITIVE-AND GATES

SCLS387B – SEPTEMBER 1997 – REVISED MAY 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
DGV package	182°C/W
NS package	127°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV08A, SN74LV08A QUADRUPLE 2-INPUT POSITIVE-AND GATES

SCLS387B – SEPTEMBER 1997 – REVISED MAY 1998

recommended operating conditions (see Note 4)

		SN54LV08A		SN74LV08A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	–50	–50		μA
		V _{CC} = 2.3 V to 2.7 V	–2	–2		
		V _{CC} = 3 V to 3.6 V	–6	–6		
		V _{CC} = 4.5 V to 5.5 V	–12	–12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50		μA
		V _{CC} = 2.3 V to 2.7 V	2	2		
		V _{CC} = 3 V to 3.6 V	6	6		
		V _{CC} = 4.5 V to 5.5 V	12	12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200		ns/V
		V _{CC} = 3 V to 3.6 V	0	100		
		V _{CC} = 4.5 V to 5.5 V	0	20		
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV08A			SN74LV08A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –6 mA	3 V	2.48			2.48			
	I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I _{OL} = 2 mA	2.3 V			0.4			0.4	
	I _{OL} = 6 mA	3 V			0.44			0.44	
	I _{OL} = 12 mA	4.5 V			0.55			0.55	
I _I	V _I = V _{CC} or GND	5.5 V			±1			±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			20			20	μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V			5			5	μA
C _i	V _I = V _{CC} or GND	3.3 V		3.4			3.4		pF
		5 V		3.4			3.4		

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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SN54LV08A, SN74LV08A

QUADRUPLE 2-INPUT POSITIVE-AND GATES

SCLS387B – SEPTEMBER 1997 – REVISED MAY 1998

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV08A		SN74LV08A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	Y	C _L = 15 pF		7.9	13.8	1	17	1	16	ns
t _{pd}	A or B	Y	C _L = 50 pF		10.5	17.3	1	21	1	20	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV08A		SN74LV08A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	Y	C _L = 15 pF		5.6	8.8	1	11.5	1	10.5	ns
t _{pd}	A or B	Y	C _L = 50 pF		7.5	12.3	1	15	1	14	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV08A		SN74LV08A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	Y	C _L = 15 pF		4.1	5.9	1	8	1	7	ns
t _{pd}	A or B	Y	C _L = 50 pF		5.5	7.9	1	10	1	9	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74LV08A			UNIT
		MIN	TYP	MAX	
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.2	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		−0.1	−0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		3.1		V
V _{IH(D)}	High-level dynamic input voltage		2.31		V
V _{IL(D)}	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

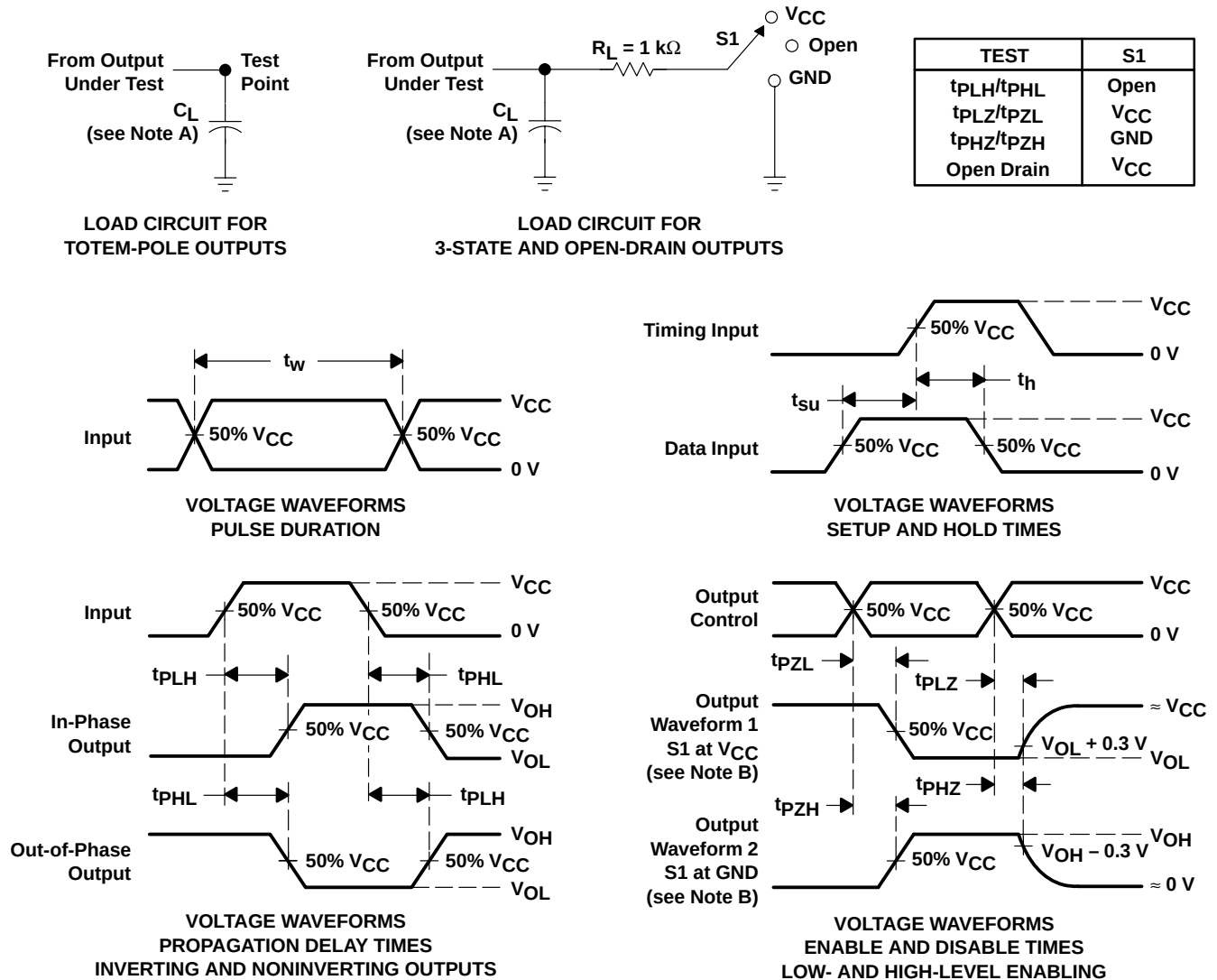
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance	C _L = 50 pF, f = 10 MHz	3.3 V	9.5	pF
			5 V	11	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV14A, SN74LV14A HEX SCHMITT-TRIGGER INVERTERS

SCLS386B – SEPTEMBER 1997 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

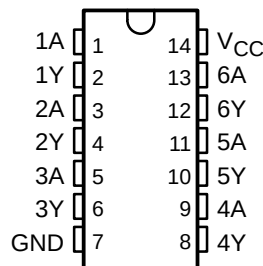
description

These hex Schmitt-trigger inverters are designed for 2-V to 5.5-V V_{CC} operation.

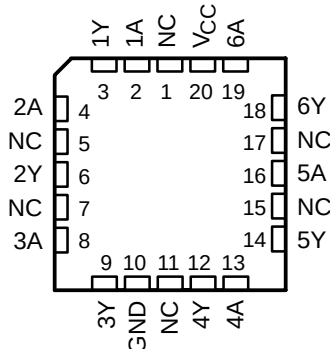
The 'LV14A devices contain six independent inverters. These devices perform the Boolean function $Y = \bar{A}$.

The SN54LV14A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV14A is characterized for operation from -40°C to 85°C .

SN54LV14A . . . J OR W PACKAGE
SN74LV14A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV14A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

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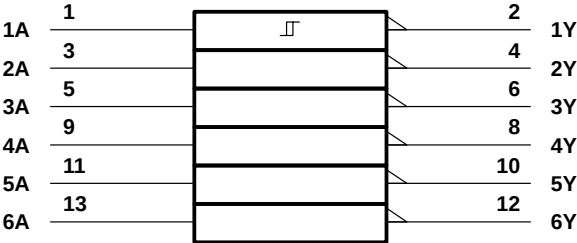
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SN54LV14A, SN74LV14A HEX SCHMITT-TRIGGER INVERTERS

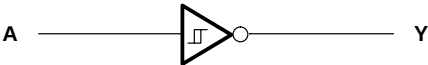
SCLS386B – SEPTEMBER 1997 – REVISED JUNE 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
DGV package	182°C/W
NS package	127°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stressratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV14A, SN74LV14A HEX SCHMITT-TRIGGER INVERTERS

SCLS386B – SEPTEMBER 1997 – REVISED JUNE 1998

recommended operating conditions (see Note 4)

			SN54LV14A		SN74LV14A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		–50		–50	μA
		V _{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V _{CC} = 3 V to 3.6 V		–6		–6	
		V _{CC} = 4.5 V to 5.5 V		–12		–12	
I _{OL}	Low-level output current	V _{CC} = 2 V		50		50	μA
		V _{CC} = 2.3 V to 2.7 V		2		2	mA
		V _{CC} = 3 V to 3.6 V		6		6	
		V _{CC} = 4.5 V to 5.5 V		12		12	
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LV14A, SN74LV14A HEX SCHMITT-TRIGGER INVERTERS

SCLS386B – SEPTEMBER 1997 – REVISED JUNE 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV14A			SN74LV14A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{T+} Positive-going threshold		2.5 V	1.75			1.75			V
		3.3 V	2.31			2.31			
		5 V	3.5			3.5			
V _{T–} Negative-going threshold		2.5 V	0.75			0.75			V
		3.3 V	0.99			0.99			
		5 V	1.5			1.5			
ΔV_T Hysteresis (V _{T+} – V _{T–})		2.5 V	0.25			0.25			V
		3.3 V	0.33			0.33			
		5 V	0.5			0.5			
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –6 mA	3 V	2.48			2.48			
	I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	2.3			2.3			pF
		5 V	2.3			2.3			

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV14A		SN74LV14A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF	10.2	19.7		1	22	1	22	ns
t _{pd}	A	Y	C _L = 50 pF	13.3	24		1	27	1	27	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV14A		SN74LV14A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF	7.3	12.8		1	15.9	1	15	ns
t _{pd}	A	Y	C _L = 50 pF	9.6	16.3		1	19.4	1	18.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LV14A, SN74LV14A HEX SCHMITT-TRIGGER INVERTERS

SCLS386B – SEPTEMBER 1997 – REVISED JUNE 1998

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV14A		SN74LV14A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$		5.1	8.6	1	10	1	10	ns
t_{pd}	A	Y	$C_L = 50\text{ pF}$		6.7	10.6	1	12	1	12	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV14A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.22	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.1	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	8.8	pF
			5 V	9.6	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

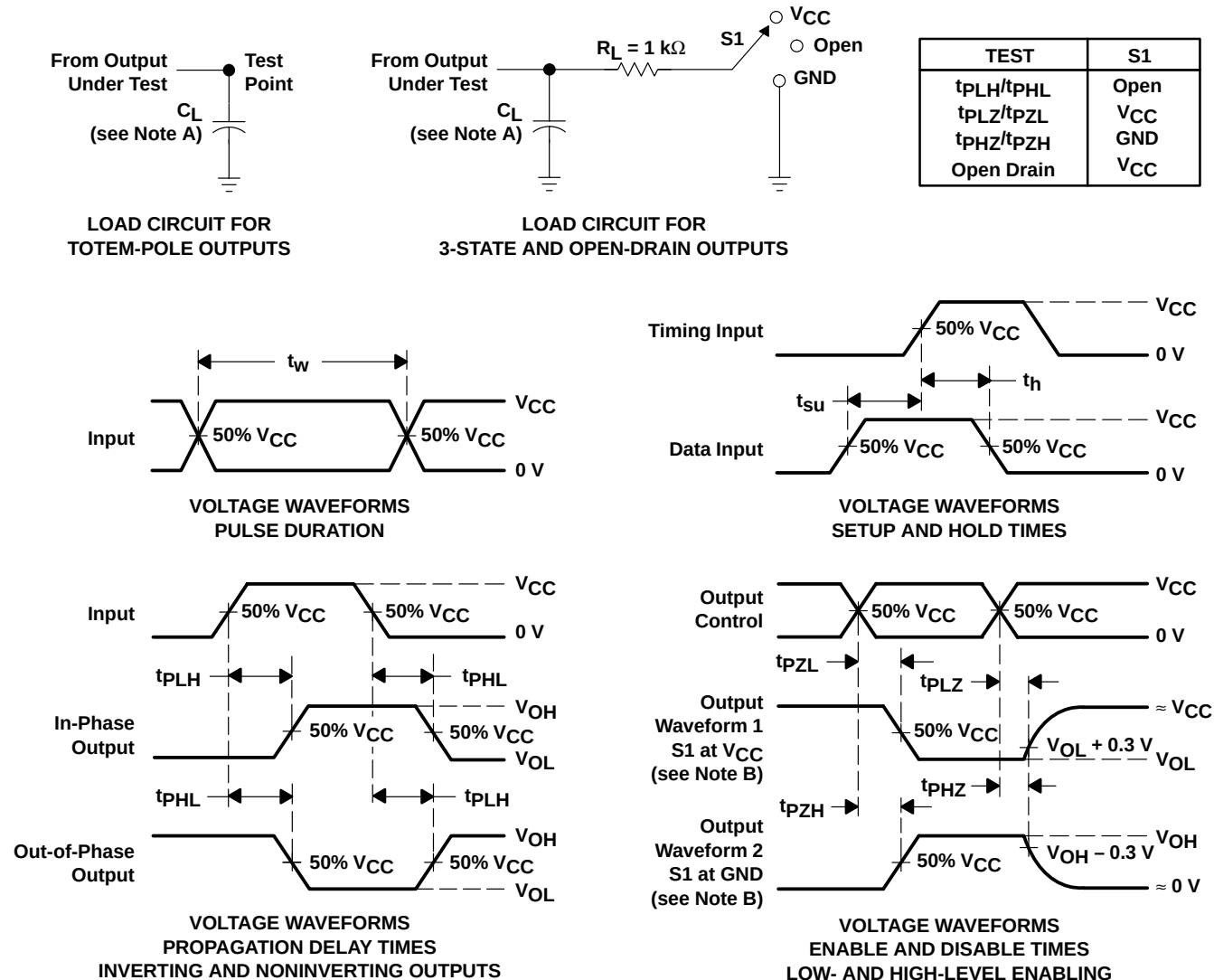


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SN54LV14A, SN74LV14A HEX SCHMITT-TRIGGER INVERTERS

SCLS386B – SEPTEMBER 1997 – REVISED JUNE 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV32A, SN74LV32A QUADRUPLE 2-INPUT POSITIVE-OR GATES

SCLS385A – SEPTEMBER 1997 – REVISED APRIL 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

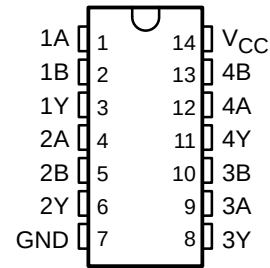
description

These quadruple 2-input positive-OR gates are designed for 2-V to 5.5-V V_{CC} operation.

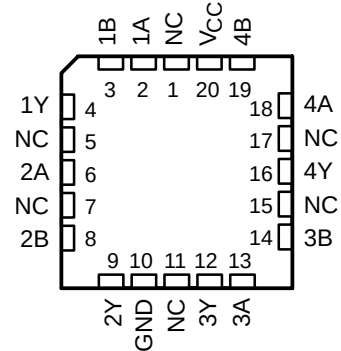
The 'LV32A devices perform the Boolean function $Y = A + B$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54LV32A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV32A is characterized for operation from -40°C to 85°C .

SN54LV32A ... J OR W PACKAGE
SN74LV32A ... D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV32A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT Y
A	B	
H	X	H
X	H	H
L	L	L

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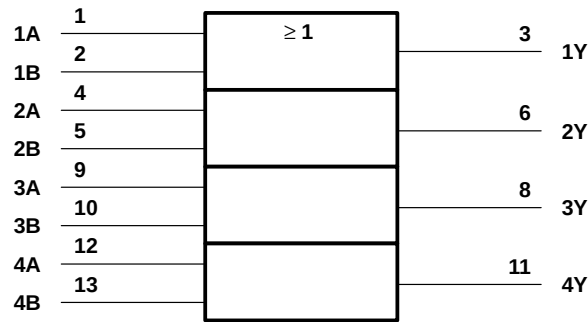
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SN54LV32A, SN74LV32A
QUADRUPLE 2-INPUT POSITIVE-OR GATES

SCLS385A – SEPTEMBER 1997 – REVISED APRIL 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	127°C/W
DB package	158°C/W
DGV package	182°C/W
N package	127°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV32A, SN74LV32A QUADRUPLE 2-INPUT POSITIVE-OR GATES

SCLS385A – SEPTEMBER 1997 – REVISED APRIL 1998

recommended operating conditions (see Note 4)

		SN54LV32A		SN74LV32A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	–50	–50		μA
		V _{CC} = 2.3 V to 2.7 V	–2	–2		
		V _{CC} = 3 V to 3.6 V	–6	–6		
		V _{CC} = 4.5 V to 5.5 V	–12	–12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50		μA
		V _{CC} = 2.3 V to 2.7 V	2	2		
		V _{CC} = 3 V to 3.6 V	6	6		
		V _{CC} = 4.5 V to 5.5 V	12	12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200		ns/V
		V _{CC} = 3 V to 3.6 V	0	100		
		V _{CC} = 4.5 V to 5.5 V	0	20		
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV32A			SN74LV32A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –6 mA	3 V	2.48			2.48			
	I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	3.4			3.4			pF
		5 V	3.4			3.4			

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SN54LV32A, SN74LV32A

QUADRUPLE 2-INPUT POSITIVE-OR GATES

SCLS385A – SEPTEMBER 1997 – REVISED APRIL 1998

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV32A		SN74LV32A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	Y	C _L = 15 pF		7.1	12.8	1	16	1	15	ns
t _{pd}	A or B	Y	C _L = 50 pF		9.6	16.2	1	20	1	19	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV32A		SN74LV32A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	Y	C _L = 15 pF		5	7.9	1	9.5	1	9.5	ns
t _{pd}	A or B	Y	C _L = 50 pF		6.9	11.4	1	13	1	13	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV32A		SN74LV32A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	Y	C _L = 15 pF		3.6	5.5	1	6.5	1	6.5	ns
t _{pd}	A or B	Y	C _L = 50 pF		4.9	7.5	1	8.5	1	8.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER				SN74LV32A			UNIT
				MIN	TYP	MAX	
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}				0.2	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}				–0.1	–0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}				3.1		V
V _{IH(D)}	High-level dynamic input voltage				2.31		V
V _{IL(D)}	Low-level dynamic input voltage					0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

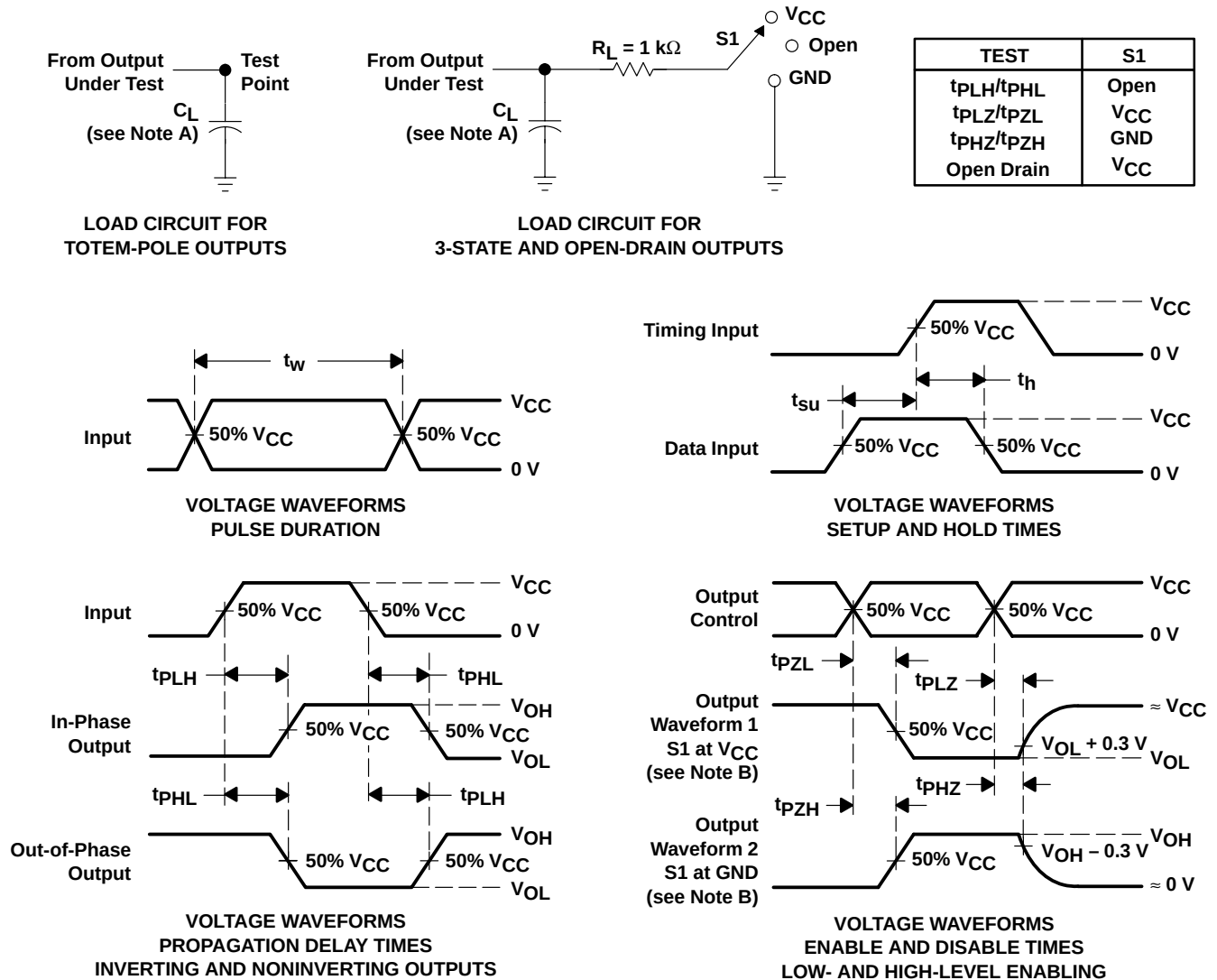
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance	C _L = 50 pF, f = 10 MHz		3.3 V	9.5	pF
				5 V	11	

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV74A, SN74LV74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

SCLS381D – AUGUST 1997 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

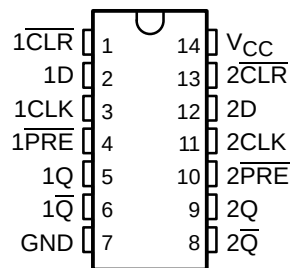
description

These dual positive-edge-triggered D-type flip-flops are designed for 2-V to 5.5-V V_{CC} operation.

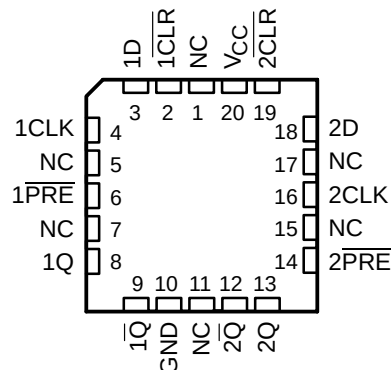
A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN54LV74A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV74A is characterized for operation from -40°C to 85°C .

SN54LV74A . . . J OR W PACKAGE
SN74LV74A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV74A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

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SN54LV74A, SN74LV74A

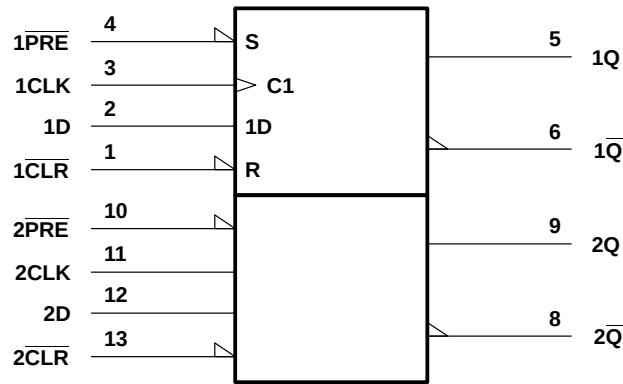
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

SCLS381D – AUGUST 1997 – REVISED JUNE 1998

FUNCTION TABLE					
INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	Q̄ ₀

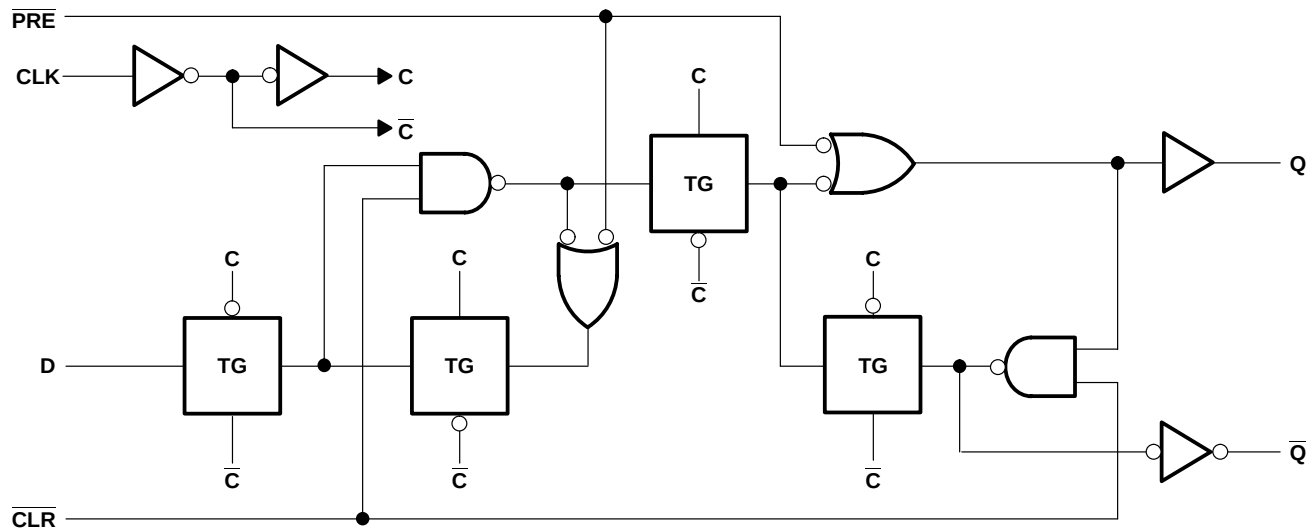
† This configuration is unstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram, each flip-flop (positive logic)



SN54LV74A, SN74LV74A

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

SCLS381D – AUGUST 1997 – REVISED JUNE 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	127°C/W
DB package	158°C/W
DGV package	182°C/W
NS package	127°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV74A		SN74LV74A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5		0.5	V
		$V_{CC} = 2.3$ V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		$V_{CC} = 3$ V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		–50		–50	μA
		$V_{CC} = 2.3$ V to 2.7 V		–2		–2	mA
		$V_{CC} = 3$ V to 3.6 V		–6		–6	
		$V_{CC} = 4.5$ V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50		50	μA
		$V_{CC} = 2.3$ V to 2.7 V		2		2	mA
		$V_{CC} = 3$ V to 3.6 V		6		6	
		$V_{CC} = 4.5$ V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V	0	200	0	200	ns/V
		$V_{CC} = 3$ V to 3.6 V	0	100	0	100	
		$V_{CC} = 4.5$ V to 5.5 V	0	20	0	20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LV74A, SN74LV74A

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

SCLS381D – AUGUST 1997 – REVISED JUNE 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV74A			SN74LV74A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –6 mA	3 V	2.48			2.48			
	I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	2.1			2.1			pF
		5 V	2.1			2.1			

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER			T _A = 25°C		SN54LV74A		SN74LV74A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	PRE or CLR low	8		9		9		ns
		CLK	8		9		9		
t _{su}	Setup time before CLK↑	Data	8		9		9		ns
		PRE or CLR inactive	7		7		7		
t _h	Hold time, data after CLK↑		0.5		0.5		0.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER			T _A = 25°C		SN54LV74A		SN74LV74A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	PRE or CLR low	6		7		7		ns
		CLK	6		7		7		
t _{su}	Setup time before CLK↑	Data	6		7		7		ns
		PRE or CLR inactive	5		5		5		
t _h	Hold time, data after CLK↑		0.5		0.5		0.5		ns

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SN54LV74A, SN74LV74A

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

SCLS381D – AUGUST 1997 – REVISED JUNE 1998

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER			$T_A = 25^\circ\text{C}$		SN54LV74A		SN74LV74A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	5		5		5		ns
		CLK	5		5		5		
t_{su}	Setup time before CLK $\uparrow$	Data	5		5		5		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	3		3		3		
t_h	Hold time, data after CLK $\uparrow$		0.5		0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV74A		SN74LV74A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$	50	100		40		40		MHz
			$C_L = 50\text{ pF}$	30	70		25		25		
t_{pd}^*	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	$C_L = 15\text{ pF}$	9.8	14.8		1	17	1	17	ns
	CLK			11.1	16.4		1	19	1	19	
t_{pd}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	$C_L = 50\text{ pF}$	13	17.4		1	20	1	20	ns
	CLK			14.2	20		1	23	1	23	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV74A		SN74LV74A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$	80	140		70		70		MHz
			$C_L = 50\text{ pF}$	50	90		45		45		
t_{pd}^*	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	$C_L = 15\text{ pF}$	6.9	12.3		1	14.5	1	14.5	ns
	CLK			7.9	11.9		1	14	1	14	
t_{pd}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	$C_L = 50\text{ pF}$	9.2	15.8		1	18	1	18	ns
	CLK			10.2	15.4		1	17.5	1	17.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV74A		SN74LV74A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$	130	180		110		110		MHz
			$C_L = 50\text{ pF}$	90	140		75		75		
t_{pd}^*	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	$C_L = 15\text{ pF}$	5	7.7		1	9	1	9	ns
	CLK			5.6	7.3		1	8.5	1	8.5	
t_{pd}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	$C_L = 50\text{ pF}$	6.6	9.7		1	11	1	11	ns
	CLK			7.2	9.3		1	10.5	1	10.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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SN54LV74A, SN74LV74A

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

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noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER	SN74LV74A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		0.1	0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		-0.04	-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		3.2		V
$V_{IH(D)}$ High-level dynamic input voltage	2.31			V
$V_{IL(D)}$ Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

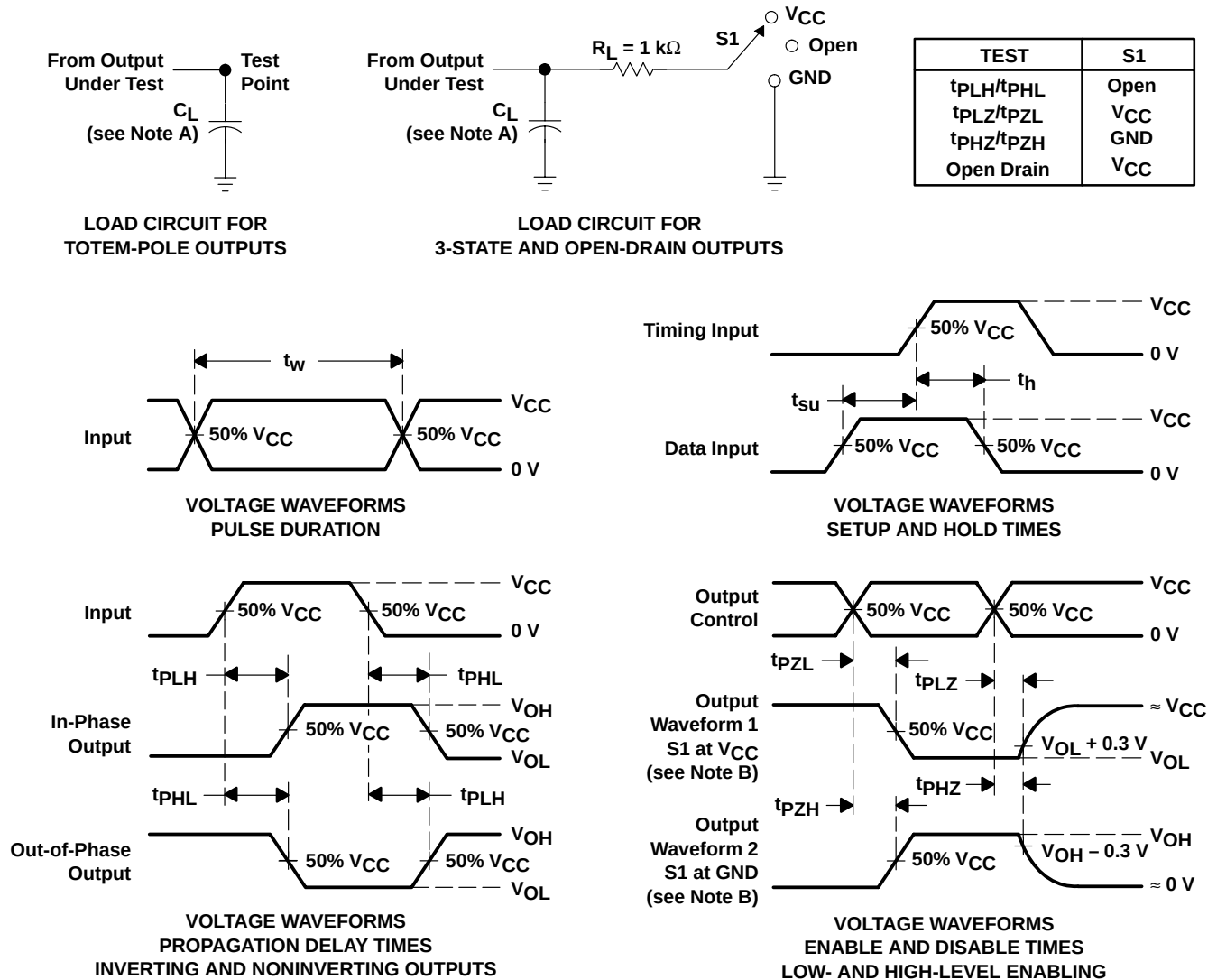
PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	21	pF
		5 V	23	

SN54LV74A, SN74LV74A

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV86A, SN74LV86A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SCLS392 – APRIL 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

description

The 'LV86A devices are quadruple 2-input exclusive-OR gates designed for 2-V to 5.5-V V_{CC} operation.

These devices contain four independent 2-input exclusive-OR gates. They perform the Boolean function $Y = A \oplus B$ or $Y = \bar{A}B + A\bar{B}$ in positive logic.

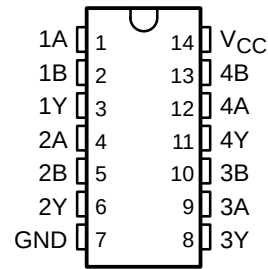
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

The SN54LV86A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV86A is characterized for operation from -40°C to 85°C .

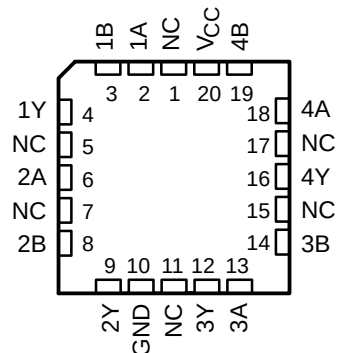
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

SN54LV86A . . . J OR W PACKAGE
SN74LV86A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV86A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

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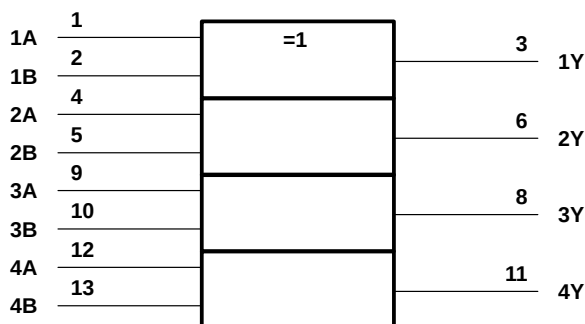
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SN54LV86A, SN74LV86A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

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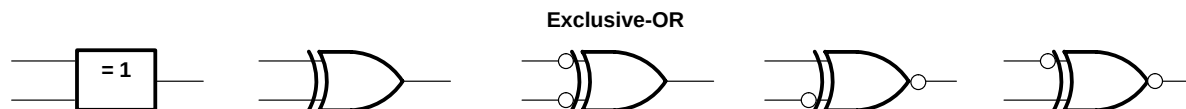
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

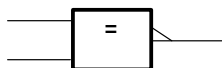
exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an 'LV86A gate in positive logic; negation may be shown at any two ports.

Logic Identity Element



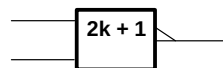
The output is active (low) if all inputs stand at the same logic level (i.e., $A = B$).

Even-Parity Element



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

Odd-Parity Element



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

SN54LV86A, SN74LV86A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	127°C/W
DB package	158°C/W
DGV package	182°C/W
NS package	127°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV86A		SN74LV86A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5		0.5	V
		$V_{CC} = 2.3$ V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		$V_{CC} = 3$ V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		–50		–50	μA
		$V_{CC} = 2.3$ V to 2.7 V		–2		–2	mA
		$V_{CC} = 3$ V to 3.6 V		–6		–6	
		$V_{CC} = 4.5$ V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50		50	μA
		$V_{CC} = 2.3$ V to 2.7 V		2		2	mA
		$V_{CC} = 3$ V to 3.6 V		6		6	
		$V_{CC} = 4.5$ V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V	0	200	0	200	ns/V
		$V_{CC} = 3$ V to 3.6 V	0	100	0	100	
		$V_{CC} = 4.5$ V to 5.5 V	0	20	0	20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LV86A, SN74LV86A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SCLS392 – APRIL 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV86A			SN74LV86A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = −50 μA	2 V to 5.5 V	V _{CC} −0.1			V _{CC} −0.1			V
	I _{OH} = −2 mA	2.3 V	2			2			
	I _{OH} = −6 mA	3 V	2.48			2.48			
	I _{OH} = −12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V							pF
		5 V							

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV86A		SN74LV86A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	Y	C _L = 15 pF								ns
t _{pd}	A or B	Y	C _L = 50 pF								ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV86A		SN74LV86A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	Y	C _L = 15 pF								ns
t _{pd}	A or B	Y	C _L = 50 pF								ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV86A		SN74LV86A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	Y	C _L = 15 pF								ns
t _{pd}	A or B	Y	C _L = 50 pF								ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW



SN54LV86A, SN74LV86A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SCLS392 – APRIL 1998

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER	SN74LV86A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$ High-level dynamic input voltage				V
$V_{IL(D)}$ Low-level dynamic input voltage				V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V		pF
		5 V		

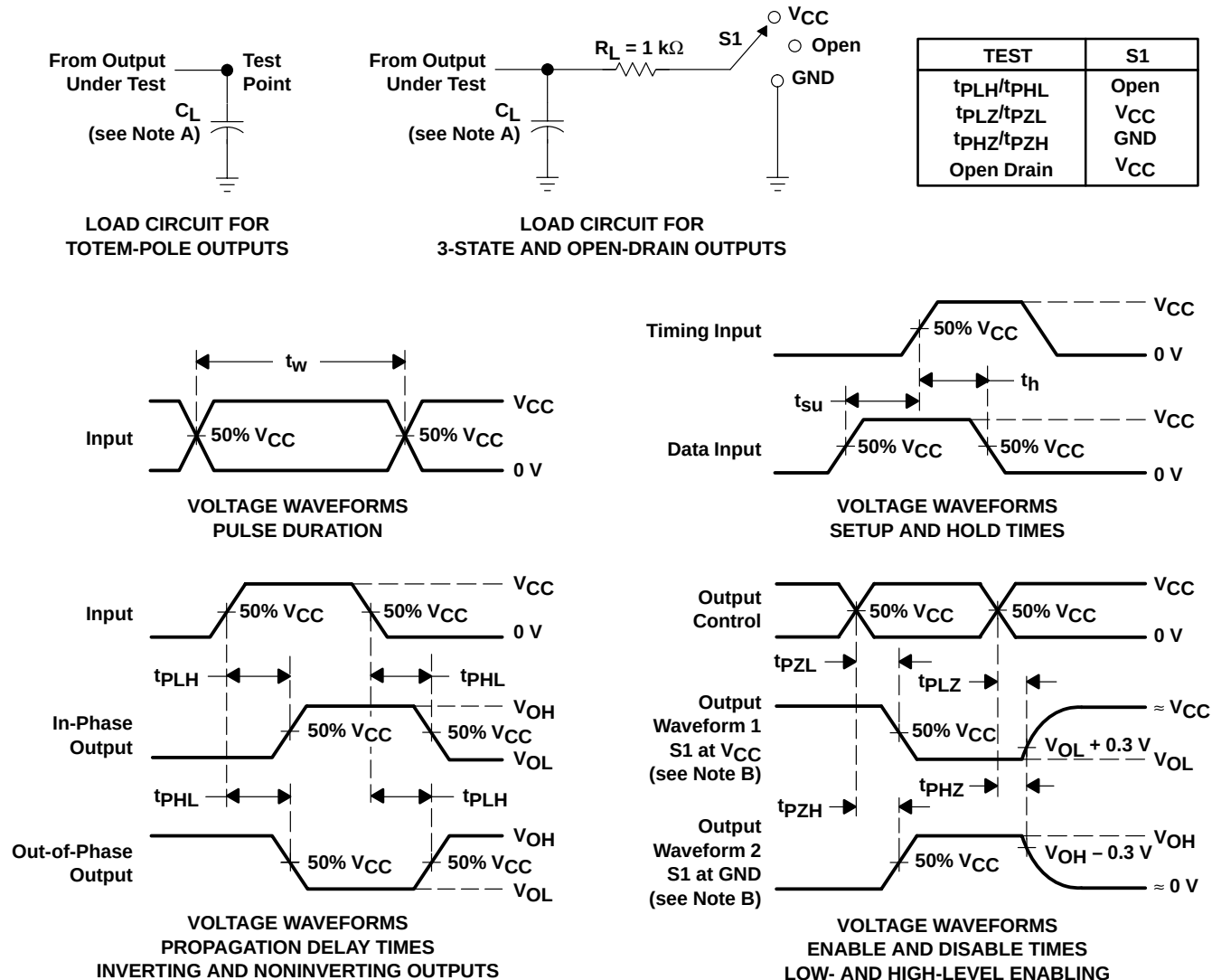
PRODUCT PREVIEW



SN54LV86A, SN74LV86A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SCLS392 – APRIL 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV123A, SN74LV123A DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

SCLS393 – APRIL 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- Edge Triggered From Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

description

The 'LV123A devices are dual retriggerable monostable multivibrators designed for 2-V to 5.5-V V_{CC} operation.

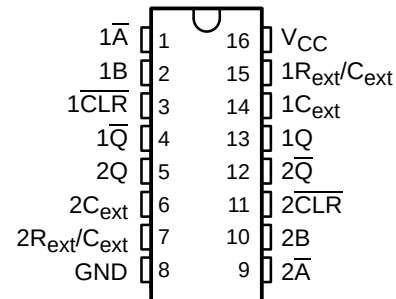
These edge-triggered multivibrators feature output pulse-duration control by three methods. In the first method, the $\bar{A}$ input is low and the B input goes high. In the second method, the B input is high and the $\bar{A}$ input goes low. In the third method, the $\bar{A}$ input is low, the B input is high, and the clear (CLR) input goes high.

The basic pulse duration is programmed by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC} . To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC} .

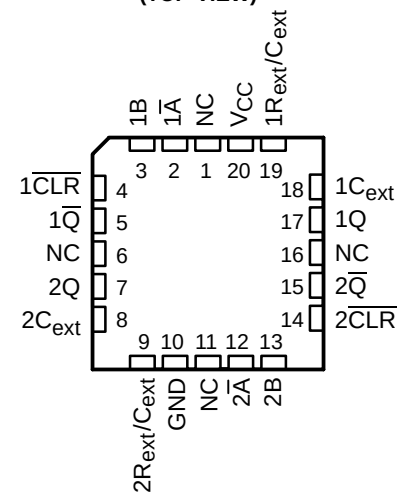
Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active ($\bar{A}$) or high-level-active (B) input. Pulse duration can be reduced by taking CLR low. Figure 1 illustrates pulse control by retriggering the inputs and early clearing.

The SN54LV123A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV123A is characterized for operation from -40°C to 85°C .

SN54LV123A . . . J OR W PACKAGE
SN74LV123A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV123A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

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SN54LV123A, SN74LV123A DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

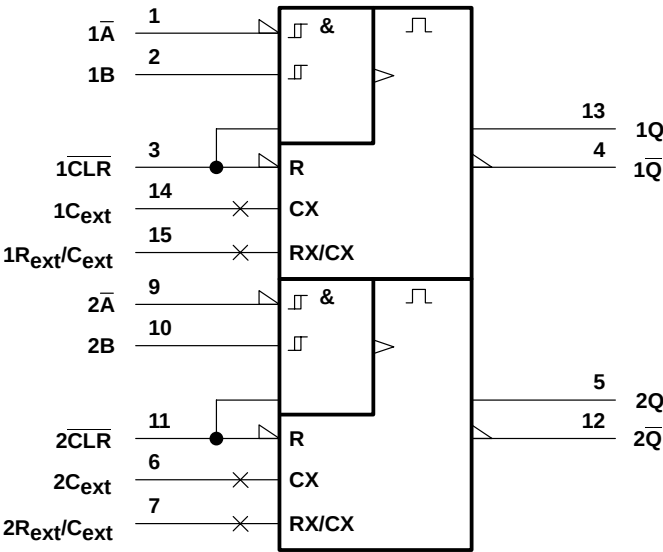
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FUNCTION TABLE

INPUTS			OUTPUTS	
CLR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L [†]	H [†]
X	X	L	L [†]	H [†]
H	L	↑	⌋	⌋
H	↓	H	⌋	⌋
↑	L	H	⌋	⌋

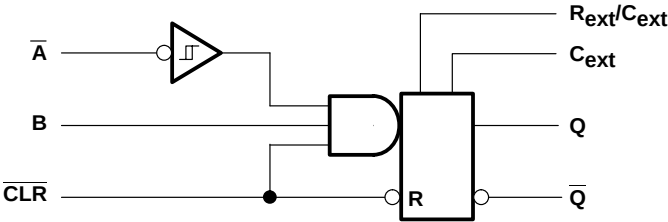
[†] These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

logic symbol[‡]



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram, each multivibrator (positive logic)



SN54LV123A, SN74LV123A DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

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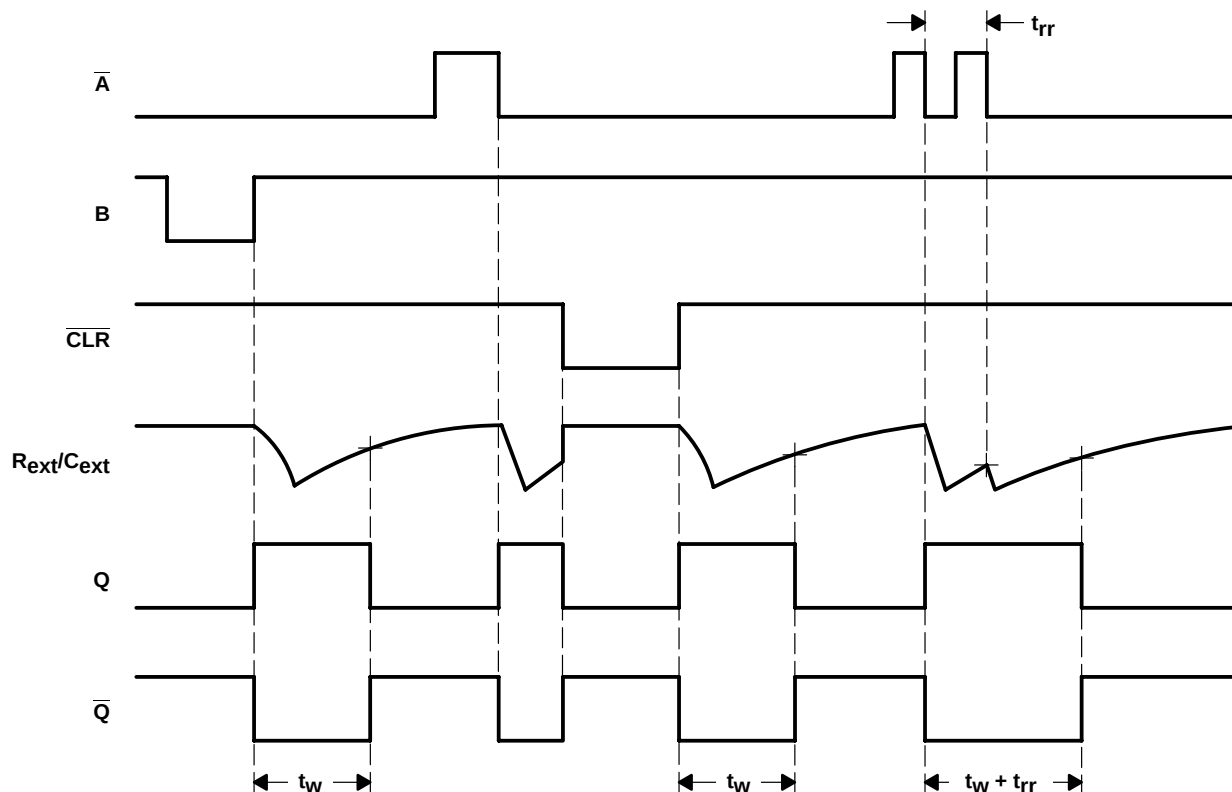


Figure 1. Input and Output Timing

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
NS package	111°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV123A, SN74LV123A

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

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recommended operating conditions (see Note 4)

			SN54LV123A		SN74LV123A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5		1.5		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5		0.5	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2\text{ V}$		–50		–50	mA
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		–2		–2	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		–6		–6	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		–12		–12	
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$		50		50	mA
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		2		2	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		6		6	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0	200	0	200	ns/V
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	0	100	0	100	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	0	20	0	20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LV123A, SN74LV123A DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	SN54LV123A			SN74LV123A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}		I _{OH} = −50 μA	2 V to 5.5 V	V _{CC} −0.1			V _{CC} −0.1			V
		I _{OH} = −2 mA	2.3 V	2			2			
		I _{OH} = −6 mA	3 V	2.48			2.48			
		I _{OH} = −12 mA	4.5 V	3.8			3.8			
V _{OL}		I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
		I _{OL} = 2 mA	2.3 V	0.4			0.4			
		I _{OL} = 6 mA	3 V	0.44			0.44			
		I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	R _{ext} /C _{ext} [†]	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
	$\overline{A}$, B, and $\overline{CLR}$	V _I = V _{CC} or GND	0 V	±1			±1			
			5.5 V	±1			±1			
I _{CC}	Quiescent	V _I = V _{CC} or GND, I _O = 0	5.5 V	40			40			μA
I _{CC}	Active state (per circuit)	V _I = V _{CC} or GND, R _{ext} /C _{ext} = 0.5 V _{CC}	2.7 V							μA
			3.6 V							
			5.5 V							
I _{off}		V _I or V _O = 0 to 5.5 V	0 V				5			μA
C _i		V _I = V _{CC} or GND	3.3 V							pF
			5 V							

[†] This test is performed with the terminal in the off-state condition.

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figures 1 and 2)

			TEST CONDITIONS		T _A = 25°C			SN54LV123A		SN74LV123A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CL $\overline{R}$										ns
		A $\overline{A}$ or B trigger										
t _{rr}	Pulse retrigger time	R _{ext} = 1 kΩ	C _{ext} = 100 pF									ns
			C _{ext} = 0.01 μF									μs

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figures 1 and 2)

			TEST CONDITIONS		T _A = 25°C			SN54LV123A		SN74LV123A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CL $\overline{R}$										ns
		$\overline{A}$ or B trigger										
t _{rr}	Pulse retrigger time	R _{ext} = 1 kΩ	C _{ext} = 100 pF								ns	
			C _{ext} = 0.01 μF								μs	

PRODUCT PREVIEW



SN54LV123A, SN74LV123A DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figures 1 and 2)

			TEST CONDITIONS		T _A = 25°C			SN54LV123A		SN74LV123A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CL $\overline{\text{R}}$										ns
		A $\overline{\text{A}}$ or B trigger										
t _{rr}	Pulse retrigger time	R _{ext} = 1 kΩ		C _{ext} = 100 pF								ns
				C _{ext} = 0.01 μF								μs

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			SN54LV123A		SN74LV123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} [*]	$\overline{\text{A}}$ or B	Q or $\overline{\text{Q}}$	C _L = 15 pF								ns
t _{PHL} [*]											
t _{PLH} [*]	$\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$									
t _{PHL} [*]											
t _{PLH} [*]	$\overline{\text{CLR}}$ trigger	Q or $\overline{\text{Q}}$									
t _{PHL} [*]											
t _{PLH}	$\overline{\text{A}}$ or B	Q or $\overline{\text{Q}}$	C _L = 50 pF								ns
t _{PHL}											
t _{PLH}	$\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$									
t _{PHL}											
t _{PLH}	$\overline{\text{CLR}}$ trigger	Q or $\overline{\text{Q}}$									
t _{PHL}											
t _w [†]		Q or $\overline{\text{Q}}$	C _L = 50 pF, C _{ext} = 28 pF, R _{ext} = 2 kΩ								ns
			C _L = 50 pF, C _{ext} = 0.01 μF, R _{ext} = 10 kΩ								μs
			C _L = 50 pF, C _{ext} = 0.1 μF, R _{ext} = 10 kΩ								ms
Δt _w [‡]											%

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

$^\dagger t_w$ = Duration of pulse at Q and $\overline{\text{Q}}$ outputs

$^\ddagger \Delta t_w$ = Output pulse duration variation (Q and $\overline{\text{Q}}$) between circuits in same package

PRODUCT PREVIEW



SN54LV123A, SN74LV123A

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			SN54LV123A		SN74LV123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} [*]	$\overline{A}$ or B	Q or $\overline{Q}$	C _L = 15 pF							ns	
t _{PHL} [*]											
t _{PLH} [*]	$\overline{\text{CLR}}$	Q or $\overline{Q}$									
t _{PHL} [*]											
t _{PLH} [*]	$\overline{\text{CLR}}$ trigger	Q or $\overline{Q}$									
t _{PHL} [*]											
t _{PLH}	$\overline{A}$ or B	Q or $\overline{Q}$	C _L = 50 pF						ns		
t _{PHL}											
t _{PLH}	$\overline{\text{CLR}}$	Q or $\overline{Q}$									
t _{PHL}											
t _{PLH}	$\overline{\text{CLR}}$ trigger	Q or $\overline{Q}$									
t _{PHL}											
t _w [†]		Q or $\overline{Q}$	C _L = 50 pF, C _{ext} = 28 pF, R _{ext} = 2 kΩ						ns		
			C _L = 50 pF, C _{ext} = 0.01 μF, R _{ext} = 10 kΩ						μs		
			C _L = 50 pF, C _{ext} = 0.1 μF, R _{ext} = 10 kΩ						ms		
Δt _w [‡]									%		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

$^\dagger t_w$ = Duration of pulse at Q and $\bar{Q}$ outputs

$^\ddagger \Delta t_w$ = Output pulse duration variation (Q and $\bar{Q}$) between circuits in same package

PRODUCT PREVIEW



SN54LV123A, SN74LV123A DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			SN54LV123A		SN74LV123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} [*]	$\overline{A}$ or B	Q or $\overline{Q}$	C _L = 15 pF								ns
t _{PHL} [*]											
t _{PLH} [*]	$\overline{CLR}$	Q or $\overline{Q}$									
t _{PHL} [*]											
t _{PLH} [*]	$\overline{CLR}$ trigger	Q or $\overline{Q}$									
t _{PHL} [*]											
t _{PLH}	$\overline{A}$ or B	Q or $\overline{Q}$	C _L = 50 pF								ns
t _{PHL}											
t _{PLH}	$\overline{CLR}$	Q or $\overline{Q}$									
t _{PHL}											
t _{PLH}	$\overline{CLR}$ trigger	Q or $\overline{Q}$									
t _{PHL}											
t _W [†]		Q or $\overline{Q}$	C _L = 50 pF, C _{ext} = 28 pF, R _{ext} = 2 kΩ								ns
			C _L = 50 pF, C _{ext} = 0.01 μF, R _{ext} = 10 kΩ								μs
			C _L = 50 pF, C _{ext} = 0.1 μF, R _{ext} = 10 kΩ								ms
Δt _W [‡]											%

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

$^\dagger t_w$ = Duration of pulse at Q and $\bar{Q}$ outputs

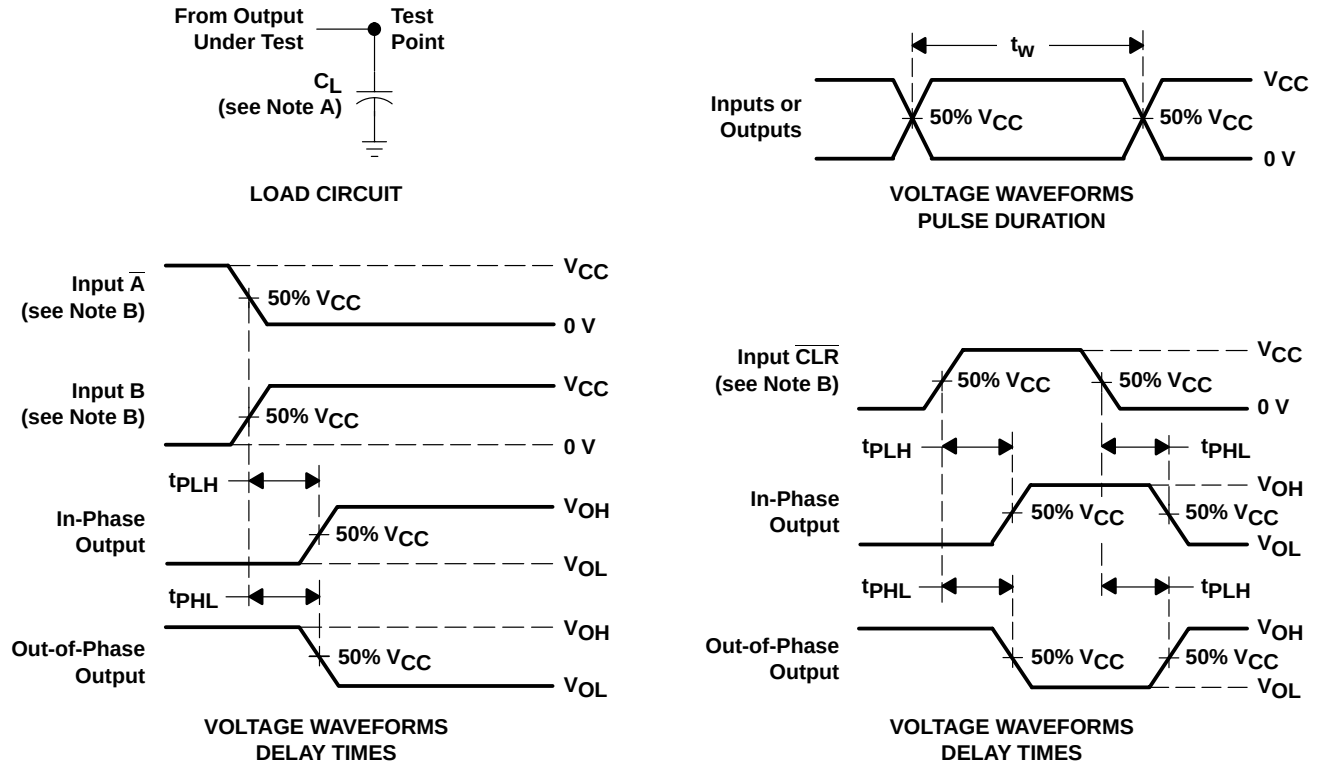
$^\ddagger \Delta t_w$ = Output pulse duration variation (Q and $\bar{Q}$) between circuits in same package

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V		pF
			5 V		



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

SN54LV125A, SN74LV125A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCES124D – DECEMBER 1997 – REVISED JULY 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

description

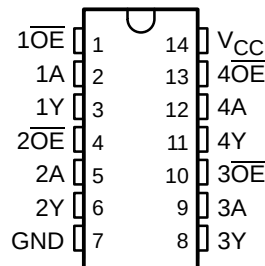
The 'LV125A quadruple bus buffer gates are designed for 2-V to 5.5-V V_{CC} operation.

These devices feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

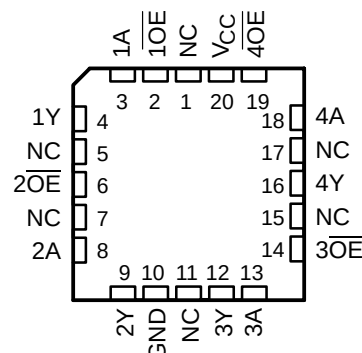
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV125A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV125A is characterized for operation from -40°C to 85°C .

SN54LV125A . . . J OR W PACKAGE
SN74LV125A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV125A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Z

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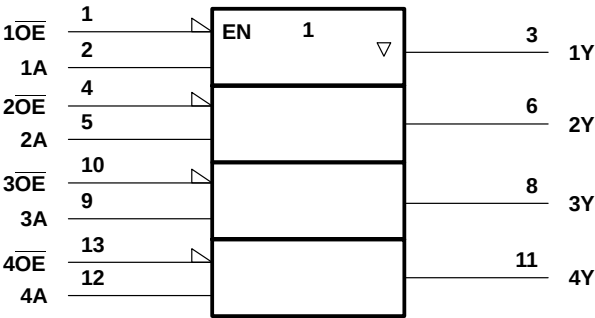
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SN54LV125A, SN74LV125A
QUADRUPLE BUS BUFFER GATES
WITH 3-STATE OUTPUTS

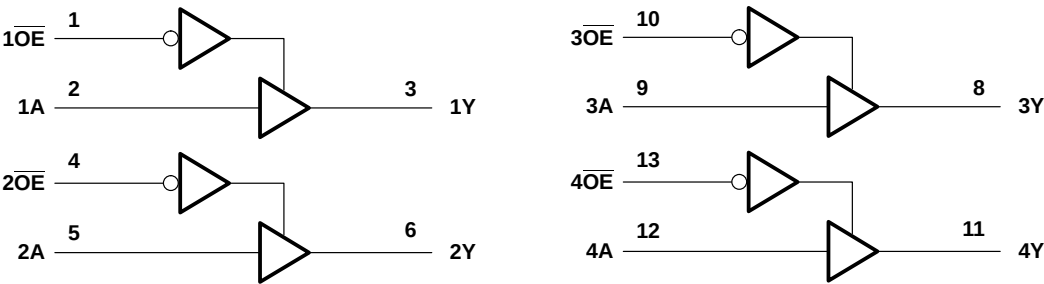
SCES124D – DECEMBER 1997 – REVISED JULY 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
DGV package	182°C/W
NS package	127°C/W
PW package	170°C/W
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV125A, SN74LV125A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCES124D – DECEMBER 1997 – REVISED JULY 1998

recommended operating conditions (see Note 4)

		SN54LV125A		SN74LV125A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	High or low state	0 V _{CC}	0 V _{CC}		V
		3-state	0 5.5	0 5.5		
I _{OH}	High-level output current	V _{CC} = 2 V	–50	–50		μA
		V _{CC} = 2.3 V to 2.7 V	–2	–2		
		V _{CC} = 3 V to 3.6 V	–8	–8		mA
		V _{CC} = 4.5 V to 5.5 V	–16	–16		
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50		μA
		V _{CC} = 2.3 V to 2.7 V	2	2		
		V _{CC} = 3 V to 3.6 V	8	8		mA
		V _{CC} = 4.5 V to 5.5 V	16	16		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0 200	0 200		ns/V
		V _{CC} = 3 V to 3.6 V	0 100	0 100		
		V _{CC} = 4.5 V to 5.5 V	0 20	0 20		
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV125A			SN74LV125A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –8 mA	3 V	2.48			2.48			
	I _{OH} = –16 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 8 mA	3 V	0.44			0.44			
	I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	2			2			pF

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SN54LV125A, SN74LV125A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCES124D – DECEMBER 1997 – REVISED JULY 1998

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV125A		SN74LV125A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$	6.8	13		1	15.5	1	15.5	ns
t_{en}^*	$\overline{OE}$	Y		7	13		1	15.5	1	15.5	
t_{dis}^*	$\overline{OE}$	Y		5.1	14.7		1	17	1	17	
t_{pd}	A	Y	$C_L = 50\text{ pF}$	8.7	16.5		1	18.5	1	18.5	ns
t_{en}	$\overline{OE}$	Y		8.8	16.5		1	18.5	1	18.5	
t_{dis}	$\overline{OE}$	Y		7.3	18.2		1	20.5	1	20.5	
$t_{sk(o)}^\dagger$				2						2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV125A		SN74LV125A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$	4.8	8		1	9.5	1	9.5	ns
t_{en}^*	$\overline{OE}$	Y		4.8	8		1	9.5	1	9.5	
t_{dis}^*	$\overline{OE}$	Y		4.1	9.7		1	11.5	1	11.5	
t_{pd}	A	Y	$C_L = 50\text{ pF}$	6.1	11.5		1	13	1	13	ns
t_{en}	$\overline{OE}$	Y		6.2	11.5		1	13	1	13	
t_{dis}	$\overline{OE}$	Y		5.5	13.2		1	15	1	15	
$t_{sk(o)}^\dagger$				1.5						1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV125A		SN74LV125A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$	3.4	5.5		1	6.5	1	6.5	ns
t_{en}^*	$\overline{OE}$	Y		3.4	5.1		1	6	1	6	
t_{dis}^*	$\overline{OE}$	Y		3.2	6.8		1	8	1	8	
t_{pd}	A	Y	$C_L = 50\text{ pF}$	4.3	7.5		1	8.5	1	8.5	ns
t_{en}	$\overline{OE}$	Y		4.4	7.1		1	8	1	8	
t_{dis}	$\overline{OE}$	Y		4	8.8		1	10	1	10	
$t_{sk(o)}^\dagger$				1						1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

SN54LV125A, SN74LV125A
QUADRUPLER BUS BUFFER GATES
WITH 3-STATE OUTPUTS

SCES124D – DECEMBER 1997 – REVISED JULY 1998

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV125A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.36	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.27	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.04		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

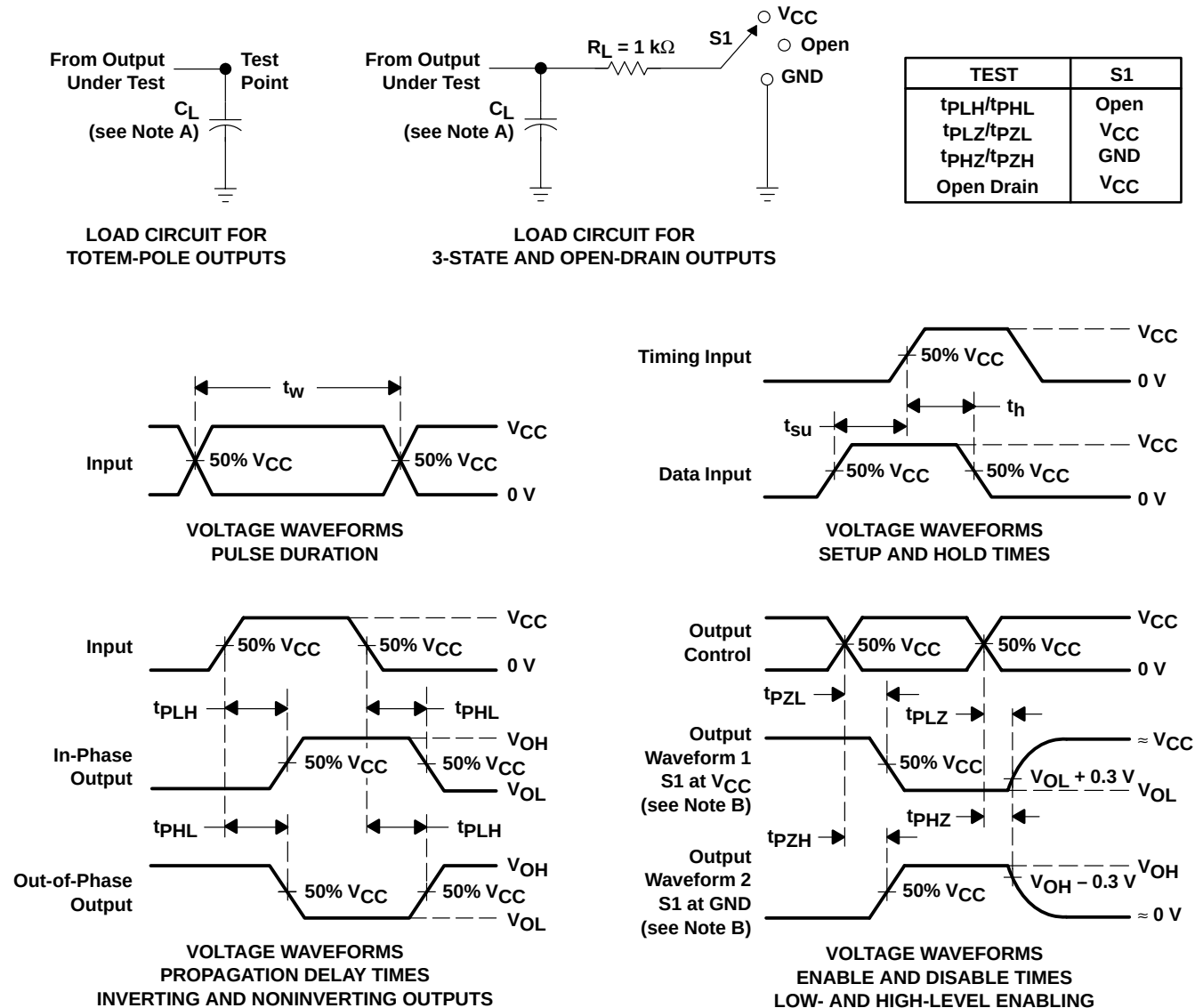
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance	Outputs enabled	C _L = 50 pF, f = 10 MHz	3.3 V	15.5	pF
				5 V	17.6	

SN54LV125A, SN74LV125A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCES124D – DECEMBER 1997 – REVISED JULY 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV126A, SN74LV126A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCES131C – MARCH 1998 – REVISED JULY 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

description

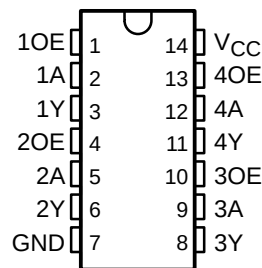
These quadruple bus buffer gates are designed for 2-V to 5.5-V V_{CC} operation.

The 'LV126A devices feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

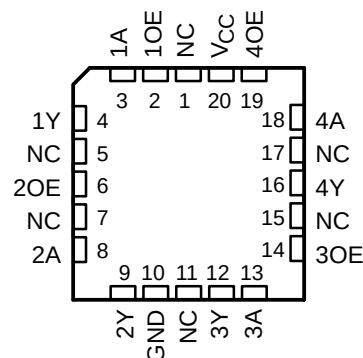
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN54LV126A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV126A is characterized for operation from -40°C to 85°C .

SN54LV126A . . . J OR W PACKAGE
SN74LV126A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV126A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	X	Z

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 **TEXAS
INSTRUMENTS**

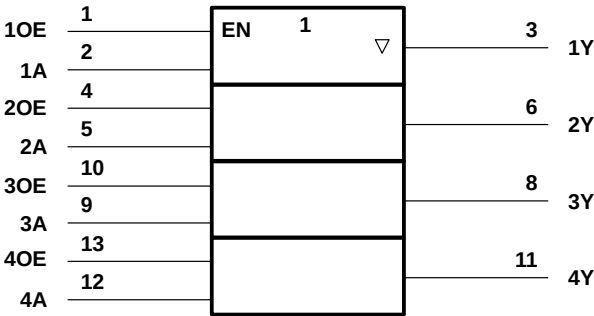
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SN54LV126A, SN74LV126A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

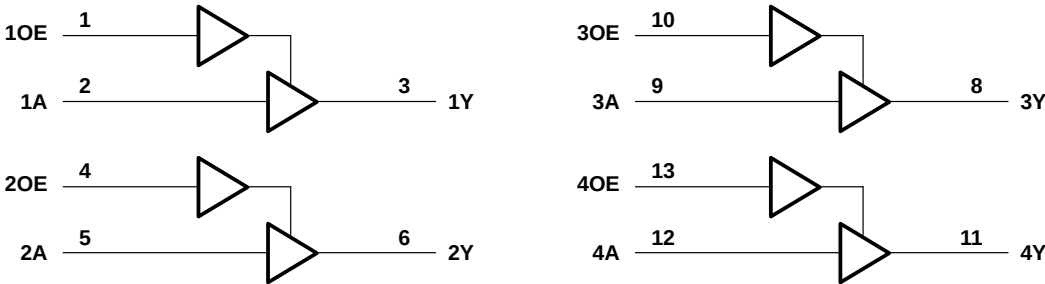
SCES131C – MARCH 1998 – REVISED JULY 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
DGV package	182°C/W
NS package	127°C/W
PW package	170°C/W
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV126A, SN74LV126A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		SN54LV126A		SN74LV126A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	High or low state	0 V _{CC}	0 V _{CC}		V
		3-state	0 5.5	0 5.5		
I _{OH}	High-level output current	V _{CC} = 2 V	–50	–50		μA
		V _{CC} = 2.3 V to 2.7 V	–2	–2		
		V _{CC} = 3 V to 3.6 V	–8	–8		mA
		V _{CC} = 4.5 V to 5.5 V	–16	–16		
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50		μA
		V _{CC} = 2.3 V to 2.7 V	2	2		
		V _{CC} = 3 V to 3.6 V	8	8		mA
		V _{CC} = 4.5 V to 5.5 V	16	16		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0 200	0 200		ns/V
		V _{CC} = 3 V to 3.6 V	0 100	0 100		
		V _{CC} = 4.5 V to 5.5 V	0 20	0 20		
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV126A			SN74LV126A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –8 mA	3 V	2.48			2.48			
	I _{OH} = –16 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 8 mA	3 V	0.44			0.44			
	I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	1.6			1.6			pF

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SN54LV126A, SN74LV126A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCES131C – MARCH 1998 – REVISED JULY 1998

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV126A		SN74LV126A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$	7.1	13		1	15.5	1	15.5	ns
t_{en}^*	OE	Y		7.4	13		1	15.5	1	15.5	
t_{dis}^*	OE	Y		5.7	14.7		1	17	1	17	
t_{pd}	A	Y	$C_L = 50\text{ pF}$	9.2	16.5		1	18.5	1	18.5	ns
t_{en}	OE	Y		9.5	16.5		1	18.5	1	18.5	
t_{dis}	OE	Y		8.1	18.2		15	20.5	1	20.5	
$t_{sk(o)}^\dagger$					2					2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV126A		SN74LV126A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$	5	8		1	9.5	1	9.5	ns
t_{en}^*	OE	Y		5.1	8		1	9.5	1	9.5	
t_{dis}^*	OE	Y		4.4	9.7		1	11.5	1	11.5	
t_{pd}	A	Y	$C_L = 50\text{ pF}$	6.4	11.5		1	13	1	13	ns
t_{en}	OE	Y		6.6	11.5		1	13	1	13	
t_{dis}	OE	Y		6.1	13.2		1	15	1	15	
$t_{sk(o)}^\dagger$					1.5					1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV126A		SN74LV126A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$	3.5	5.5		1	6.5	1	6.5	ns
t_{en}^*	OE	Y		3.6	5.1		1	6	1	6	
t_{dis}^*	OE	Y		3.3	6.8		1	8	1	8	
t_{pd}	A	Y	$C_L = 50\text{ pF}$	4.6	7.5		1	8.5	1	8.5	ns
t_{en}	OE	Y		4.6	7.1		1	8	1	8	
t_{dis}	OE	Y		4.3	8.8		1	10	1	10	
$t_{sk(o)}^\dagger$					1					1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LV126A, SN74LV126A
QUADRUPLER BUS BUFFER GATES
WITH 3-STATE OUTPUTS

SCES131C – MARCH 1998 – REVISED JULY 1998

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV126A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.32	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.23	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.06		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.97	V

NOTE 5: Characteristics are for surface-mount packages only.

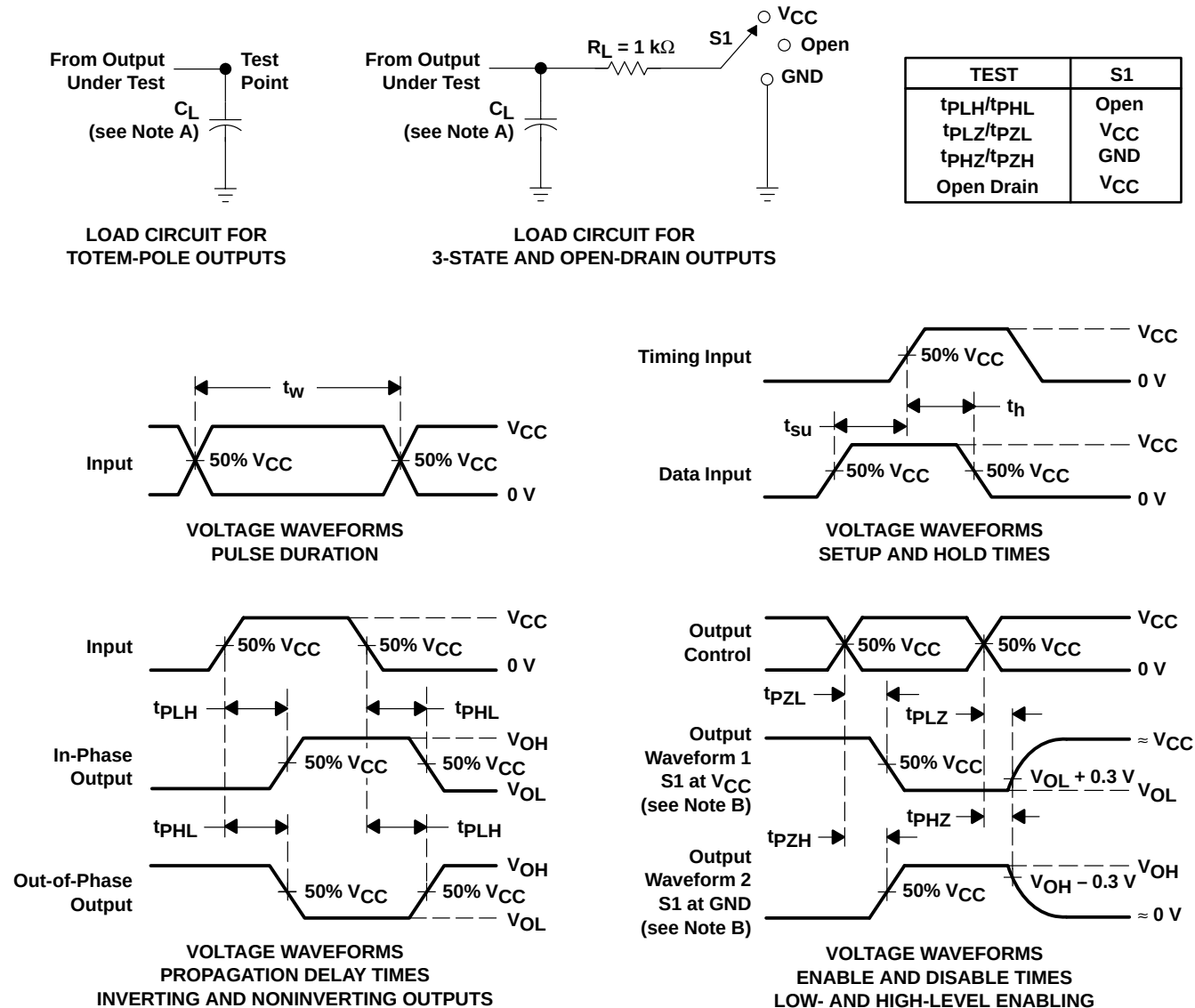
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance		3.3 V	14.4	pF
	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	5 V	15.9	

SN54LV126A, SN74LV126A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCES131C – MARCH 1998 – REVISED JULY 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV132A, SN74LV132A QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT-TRIGGER INPUTS

SCLS394A – APRIL 1998 – REVISED MAY 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

description

The 'LV132A devices are quadruple positive-NAND gates designed for 2-V to 5.5-V V_{CC} operation.

The 'LV132A devices perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals.

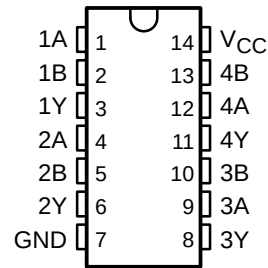
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The SN54LV132A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV132A is characterized for operation from -40°C to 85°C .

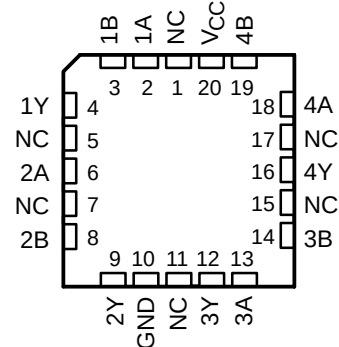
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

SN54LV132A . . . J OR W PACKAGE
SN74LV132A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV132A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

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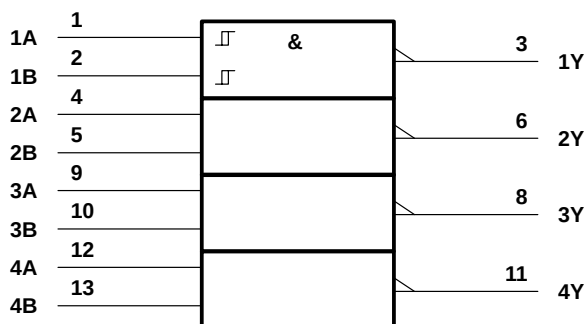
SN54LV132A, SN74LV132A

QUADRUPLE POSITIVE-NAND GATES

WITH SCHMITT-TRIGGER INPUTS

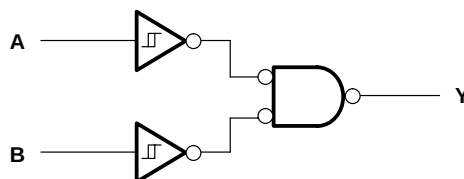
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
DGV package	182°C/W
NS package	127°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV132A, SN74LV132A
QUADRUPLE POSITIVE-NAND GATES
WITH SCHMITT-TRIGGER INPUTS

SCLS394A – APRIL 1998 – REVISED MAY 1998

recommended operating conditions (see Note 4)

			SN54LV132A		SN74LV132A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		–50		–50	μA
		V _{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V _{CC} = 3 V to 3.6 V		–6		–6	
		V _{CC} = 4.5 V to 5.5 V		–12		–12	
I _{OL}	Low-level output current	V _{CC} = 2 V		50		50	μA
		V _{CC} = 2.3 V to 2.7 V		2		2	mA
		V _{CC} = 3 V to 3.6 V		6		6	
		V _{CC} = 4.5 V to 5.5 V		12		12	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW



SN54LV132A, SN74LV132A

QUADRUPLE POSITIVE-NAND GATES

WITH SCHMITT-TRIGGER INPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV132A			SN74LV132A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{T+} Positive-going input threshold voltage		3 V	2.2			2.2			V
		4.5 V	3.15			3.15			
		5.5 V	3.85			3.85			
V _{T–} Negative-going input threshold voltage		3 V	0.9			0.9			V
		4.5 V	1.35			1.35			
		5.5 V	1.65			1.65			
ΔV _T Hysteresis (V _{T+} – V _{T–})		3 V	0.3			1.2			V
		4.5 V	0.4			1.4			
		5.5 V	0.5			1.6			
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –6 mA	3 V	2.48			2.48			
	I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V							pF
		5 V							

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV132A		SN74LV132A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	Y	C _L = 15 pF								ns
t _{pd}	A or B	Y	C _L = 50 pF								ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV132A		SN74LV132A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	Y	C _L = 15 pF								ns
t _{pd}	A or B	Y	C _L = 50 pF								ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.



SN54LV132A, SN74LV132A
QUADRUPLE POSITIVE-NAND GATES
WITH SCHMITT-TRIGGER INPUTS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV132A		SN74LV132A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A or B	Y	$C_L = 15\text{ pF}$								ns
t_{pd}	A or B	Y	$C_L = 50\text{ pF}$								ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV132A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage				V
$V_{IL(D)}$	Low-level dynamic input voltage				V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V		pF
			5 V		

PRODUCT PREVIEW



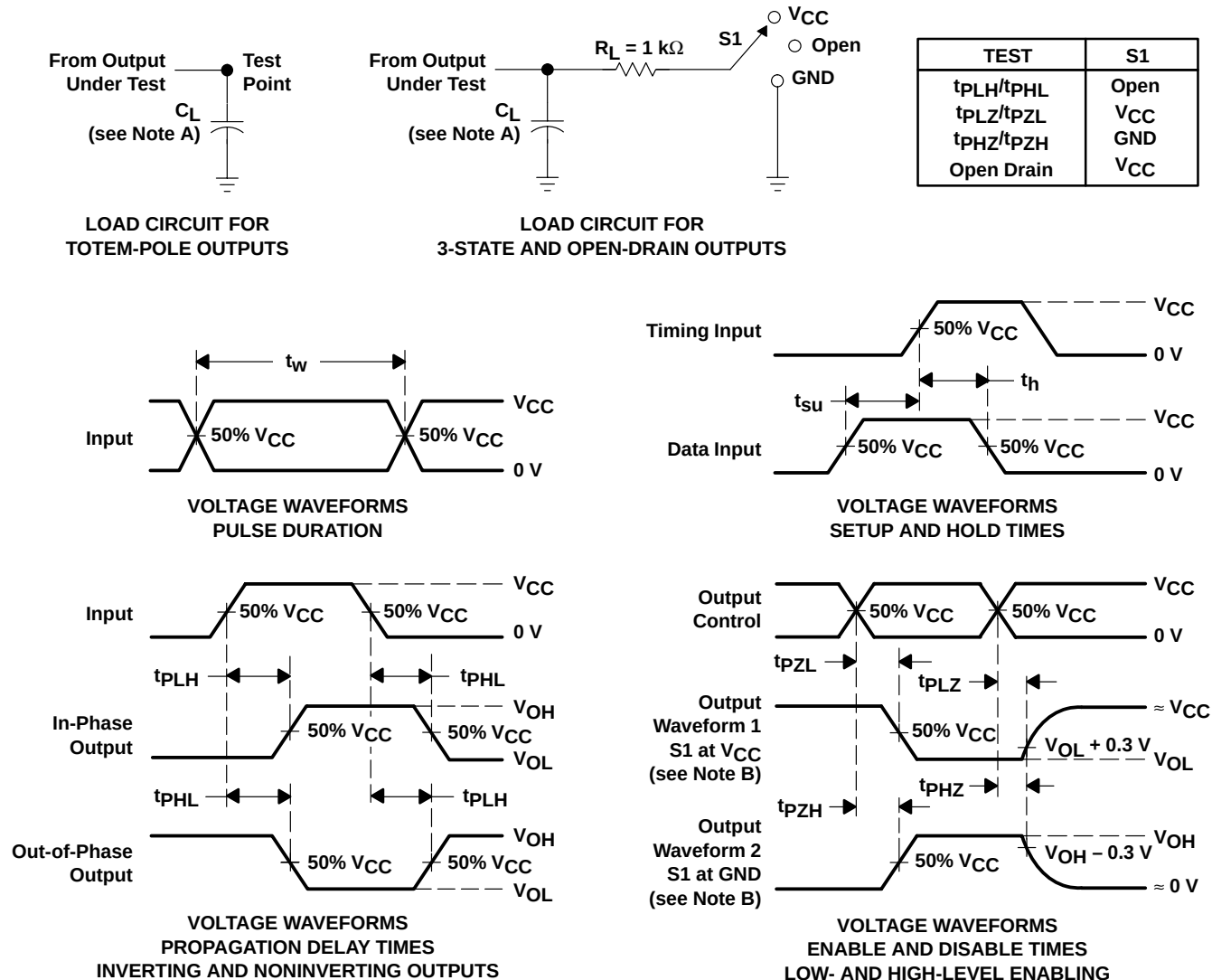
SN54LV132A, SN74LV132A

QUADRUPLE POSITIVE-NAND GATES

WITH SCHMITT-TRIGGER INPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV138A, SN74LV138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

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- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

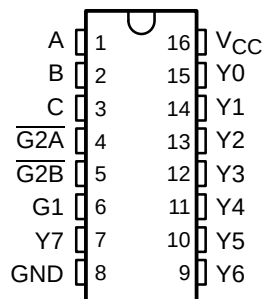
The 'LV138A devices are 3-line to 8-line decoders/demultiplexers designed for 2-V to 5.5-V V_{CC} operation.

These devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

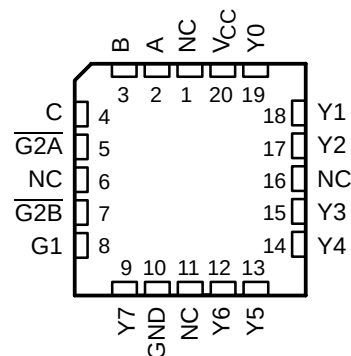
The conditions at the binary-select inputs (A, B, C) and the three enable inputs ($G1$, $\overline{G2A}$, $\overline{G2B}$) select one of eight output lines. The two active-low ($\overline{G2A}$, $\overline{G2B}$) and one active-high ($G1$) enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54LV138A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV138A is characterized for operation from -40°C to 85°C .

SN54LV138A . . . J OR W PACKAGE
SN74LV138A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV138A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

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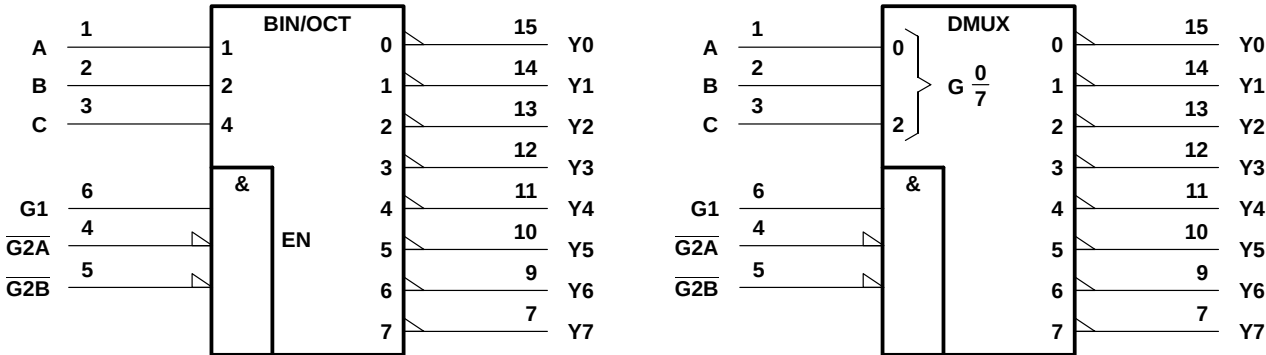
SN54LV138A, SN74LV138A
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

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FUNCTION TABLE

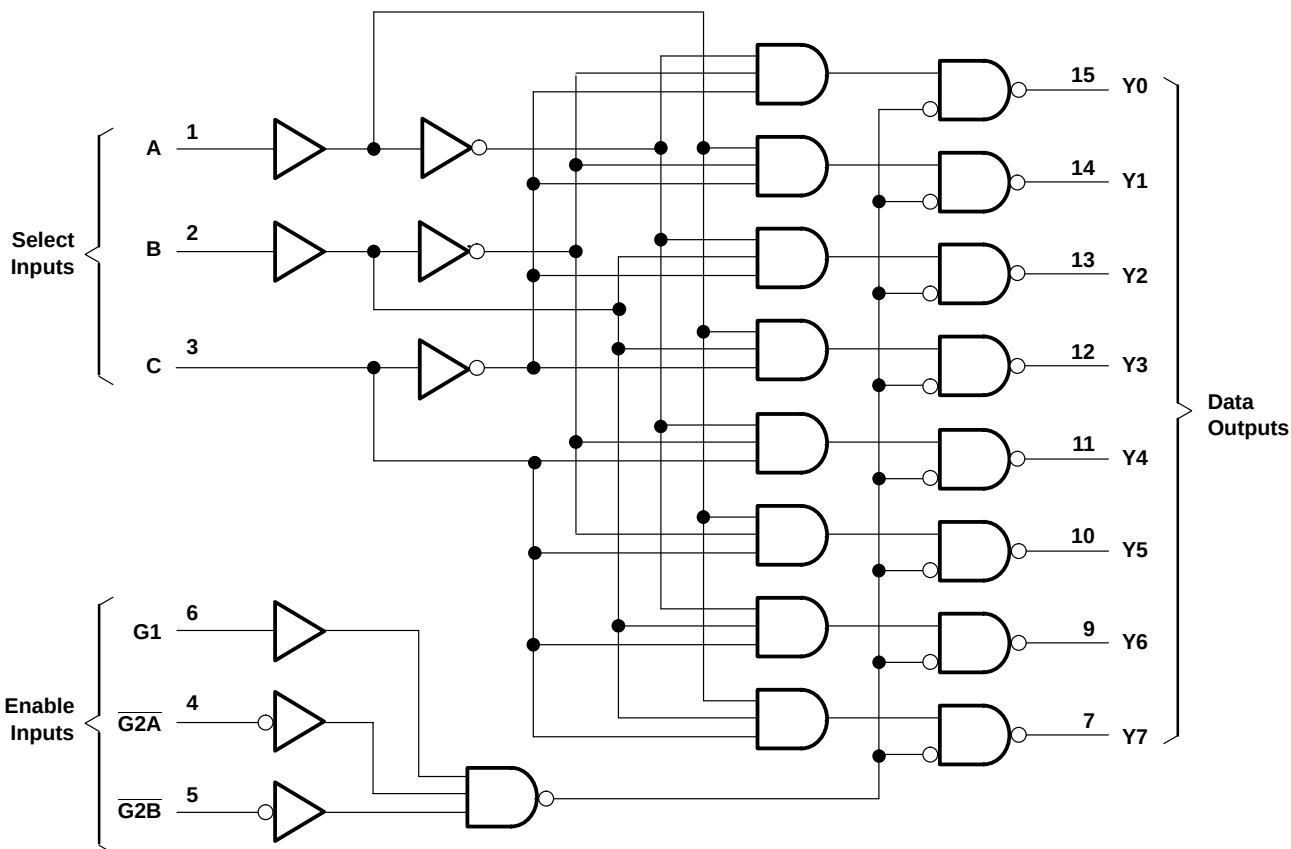
ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

logic symbols (alternatives)[†]



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
NS package	111°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV138A, SN74LV138A

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

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recommended operating conditions (see Note 4)

			SN54LV138A		SN74LV138A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−6		−6		
		V _{CC} = 4.5 V to 5.5 V	−12		−12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	6		6		
		V _{CC} = 4.5 V to 5.5 V	12		12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV138A			SN74LV138A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = −50 μA	2 V to 5.5 V	V _{CC} −0.1			V _{CC} −0.1			V
	I _{OH} = −2 mA	2.3 V	2			2			
	I _{OH} = −6 mA	3 V	2.48			2.48			
	I _{OH} = −12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	2.1			2.1			pF

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SN54LV138A, SN74LV138A

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

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**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV138A		SN74LV138A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A, B, or C	Y	C _L = 15 pF	11.7	17.6		1	21	1	21	ns
	G1			12.3	19.2		1	22	1	22	
	G2A or G2B			11.4	18.2		1	21	1	21	
t _{pd}	A, B, or C	Y	C _L = 50 pF	14.9	21.4		1	25	1	25	ns
	G1			15.7	22.6		1	26	1	26	
	G2A or G2B			14.8	22		1	25	1	25	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV138A		SN74LV138A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A, B, or C	Y	C _L = 15 pF	8.1	11.4		1	13	1	13	ns
	G1			8.4	12.8		1	15	1	15	
	G2A or G2B			7.8	11.4		1	13.5	1	13.5	
t _{pd}	A, B, or C	Y	C _L = 50 pF	10.3	15.8		1	18	1	18	ns
	G1			10.6	16.3		1	18.5	1	18.5	
	G2A or G2B			10	14.9		1	17	1	17	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV138A		SN74LV138A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A, B, or C	Y	C _L = 15 pF	5.6	8.1		1	9.5	1	9.5	ns
	G1			5.7	8.1		1	9.5	1	9.5	
	G2A or G2B			5.4	8.1		1	9.5	1	9.5	
t _{pd}	A, B, or C	Y	C _L = 50 pF	7	10.1		1	11.5	1	11.5	ns
	G1			7.1	10.1		1	11.5	1	11.5	
	G2A or G2B			6.8	10.1		1	11.5	1	11.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance	C _L = 50 pF, f = 10 MHz		3.3 V	16.8	pF
				5 V	19.1	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



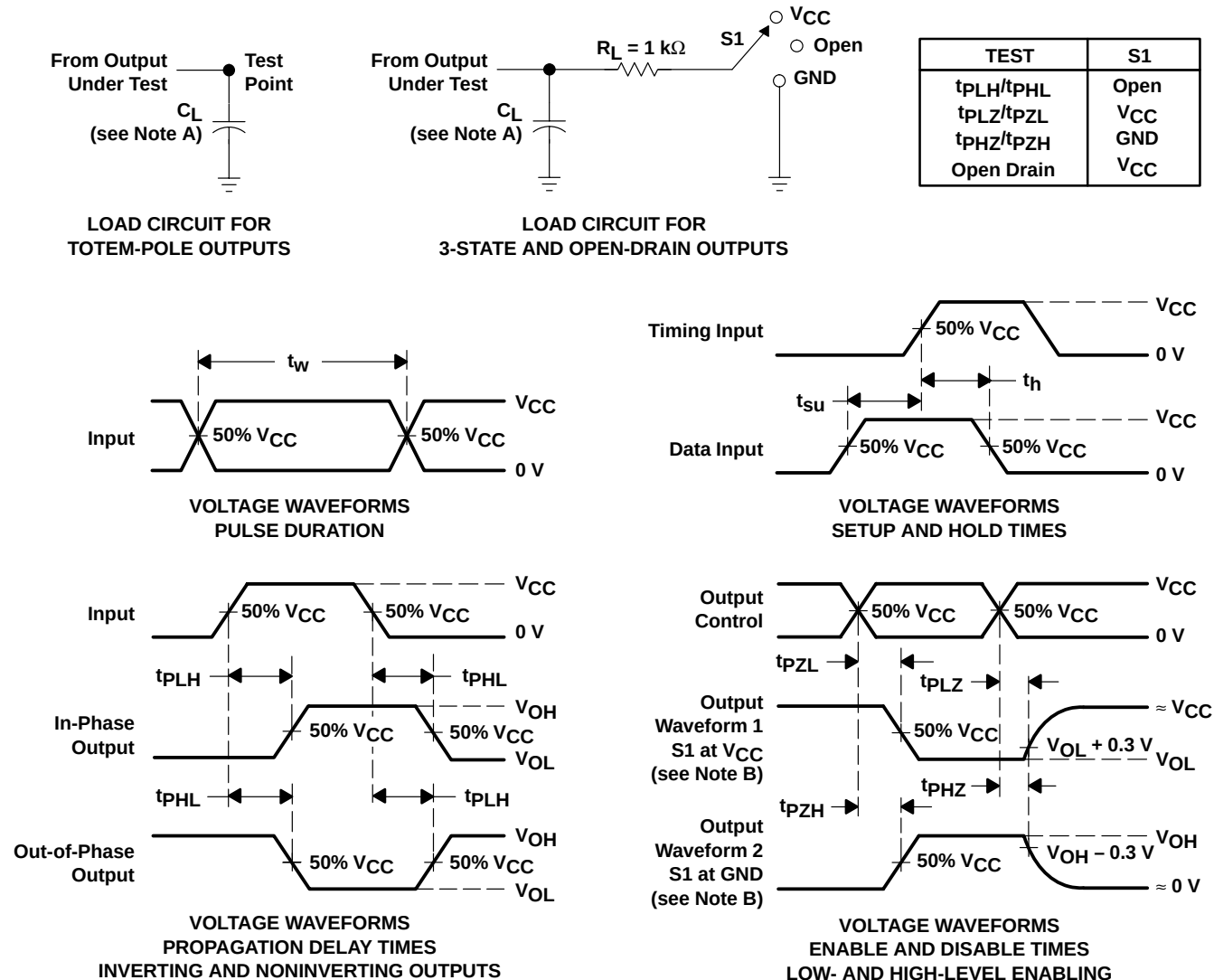
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SN54LV138A, SN74LV138A

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

SCLS395B – APRIL 1998 – REVISED JULY 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV139A, SN74LV139A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

SCLS396 – APRIL 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

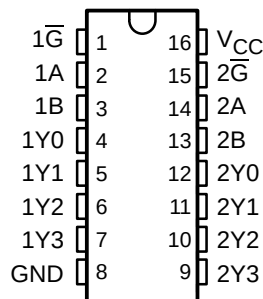
The 'LV139A devices are dual 2-line to 4-line decoders/demultiplexers designed for 2-V to 5.5-V V_{CC} operation.

These devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay time of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

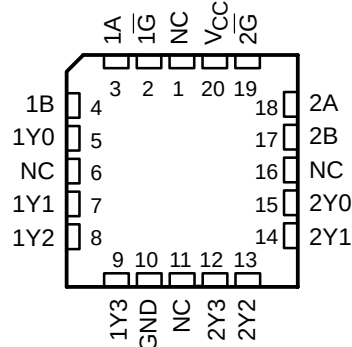
The 'LV139A devices comprise two individual 2-line to 4-line decoders in a single package. The active-low enable ($\overline{G}$) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The SN54LV139A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV139A is characterized for operation from -40°C to 85°C .

SN54LV139A ... J OR W PACKAGE
SN74LV139A ... D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV139A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

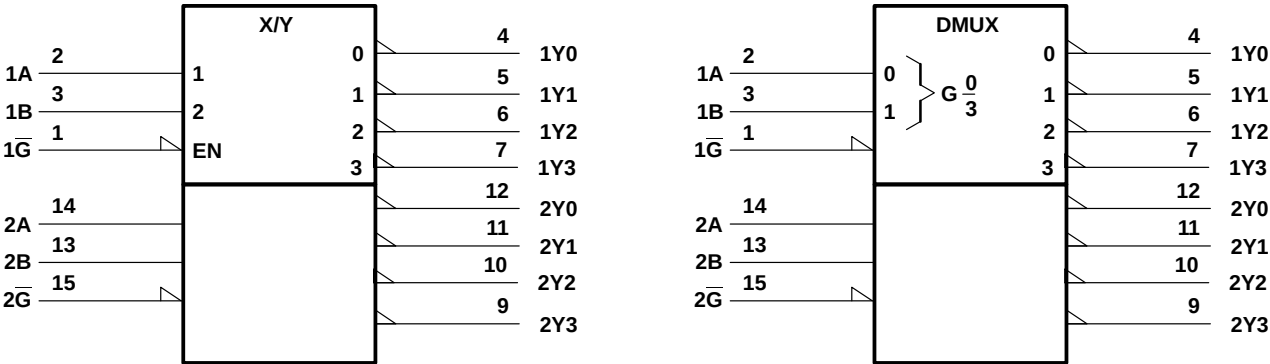
SN54LV139A, SN74LV139A
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

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FUNCTION TABLE

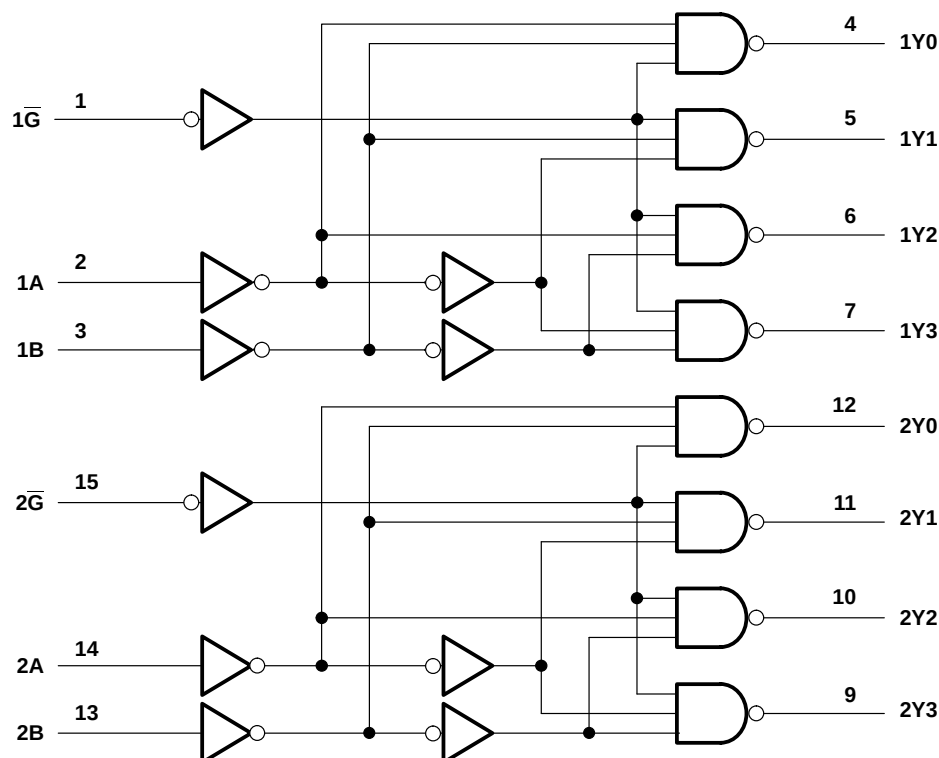
INPUTS			OUTPUTS			
$\overline{G}$	SELECT					
	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

logic symbols (alternatives)[†]



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
NS package	111°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

PRODUCT PREVIEW

SN54LV139A, SN74LV139A

DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

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recommended operating conditions (see Note 4)

			SN54LV139A		SN74LV139A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−6		−6		
		V _{CC} = 4.5 V to 5.5 V	−12		−12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	6		6		
		V _{CC} = 4.5 V to 5.5 V	12		12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV139A			SN74LV139A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = −50 μA	2 V to 5.5 V	V _{CC} −0.1			V _{CC} −0.1			V
	I _{OH} = −2 mA	2.3 V	2			2			
	I _{OH} = −6 mA	3 V	2.48			2.48			
	I _{OH} = −12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V							pF
		5 V							



SN54LV139A, SN74LV139A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

SCLS396 – APRIL 1998

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV139A		SN74LV139A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A or B	Y	$C_L = 15\text{ pF}$								ns
	$\overline{G}$	Y									
t_{pd}	A or B	Y	$C_L = 50\text{ pF}$								ns
	$\overline{G}$	Y									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV139A		SN74LV139A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A or B	Y	$C_L = 15\text{ pF}$								ns
	$\overline{G}$	Y									
t_{pd}	A or B	Y	$C_L = 50\text{ pF}$								ns
	$\overline{G}$	Y									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV139A		SN74LV139A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A or B	Y	$C_L = 15\text{ pF}$								ns
	$\overline{G}$	Y									
t_{pd}	A or B	Y	$C_L = 50\text{ pF}$								ns
	$\overline{G}$	Y									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER				SN74LV139A			UNIT
				MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}						V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}						V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}						V
$V_{IH(D)}$	High-level dynamic input voltage						V
$V_{IL(D)}$	Low-level dynamic input voltage						V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$		3.3 V		pF
				5 V		

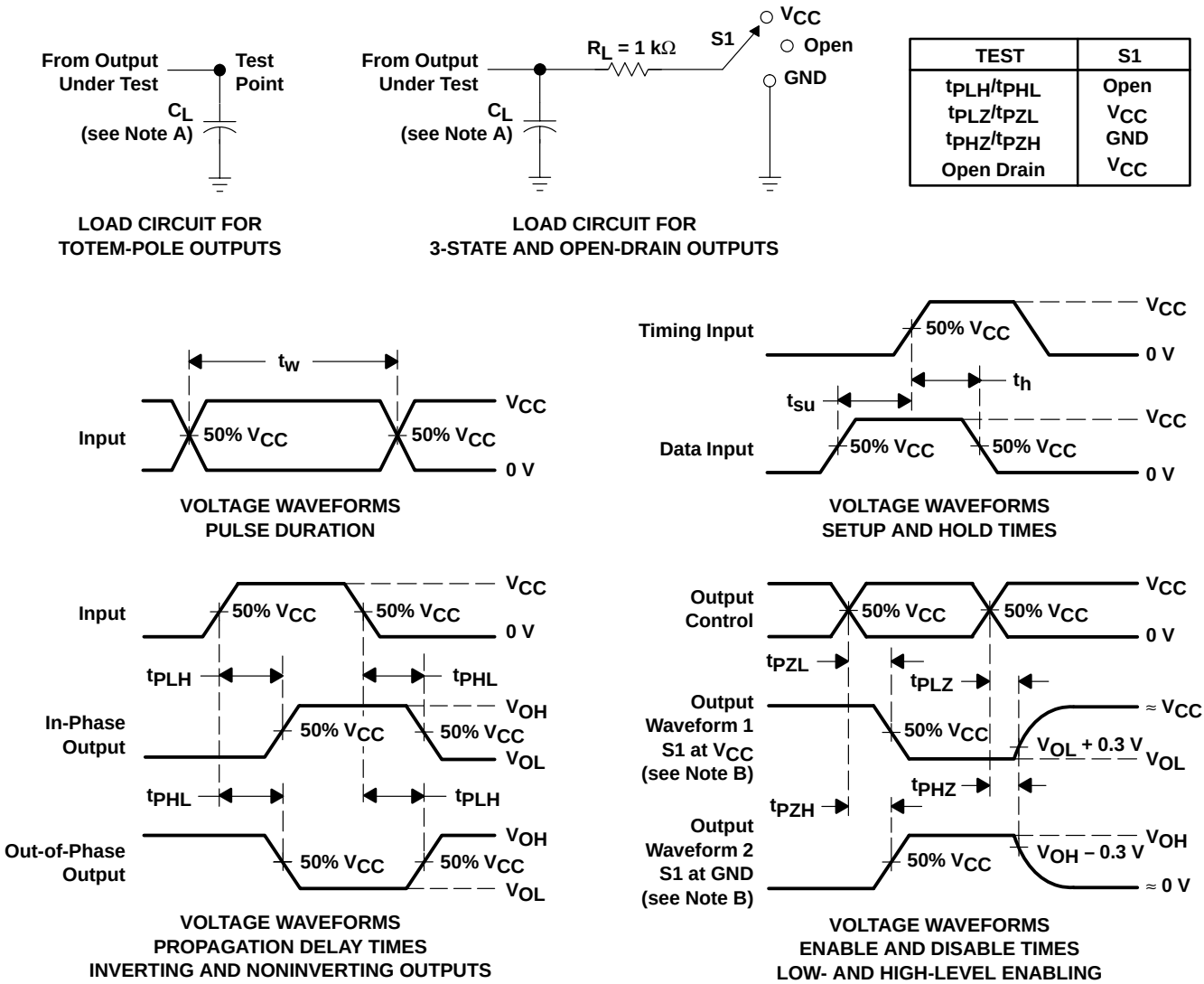
PRODUCT PREVIEW



SN54LV139A, SN74LV139A
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

SCLS396 – APRIL 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV157A, SN74LV157A QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCLS397 – APRIL 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

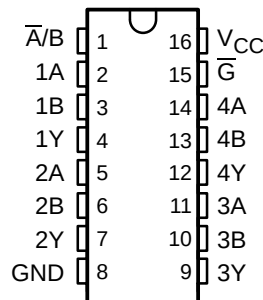
description

The 'LV157A devices are quadruple 2-line to 1-line data selectors/multiplexers designed for 2-V to 5.5-V V_{CC} operation.

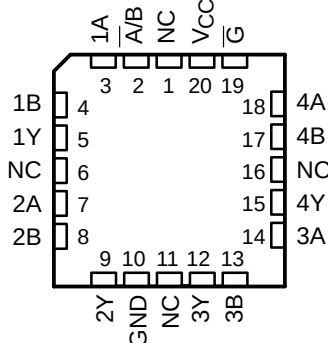
These devices contain inverters and drivers to supply full data selection to the four output gates. A separate strobe ($\bar{G}$) input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 'LV157A devices present true data.

The SN54LV157A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV157A is characterized for operation from -40°C to 85°C .

SN54LV157A ... J OR W PACKAGE
SN74LV157A ... D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV157A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

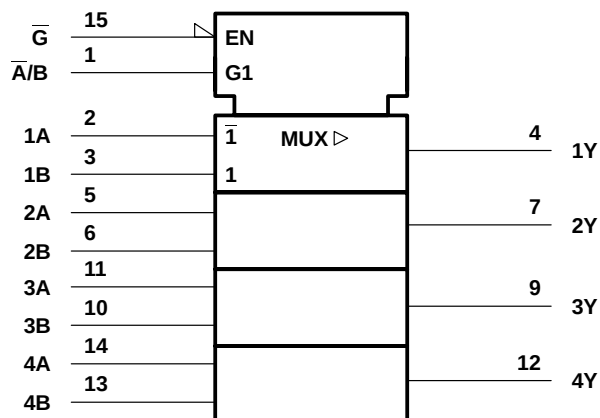
FUNCTION TABLE

$\bar{G}$	SELECT $\bar{A/B}$	DATA		OUTPUT Y
		A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

SN54LV157A, SN74LV157A QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

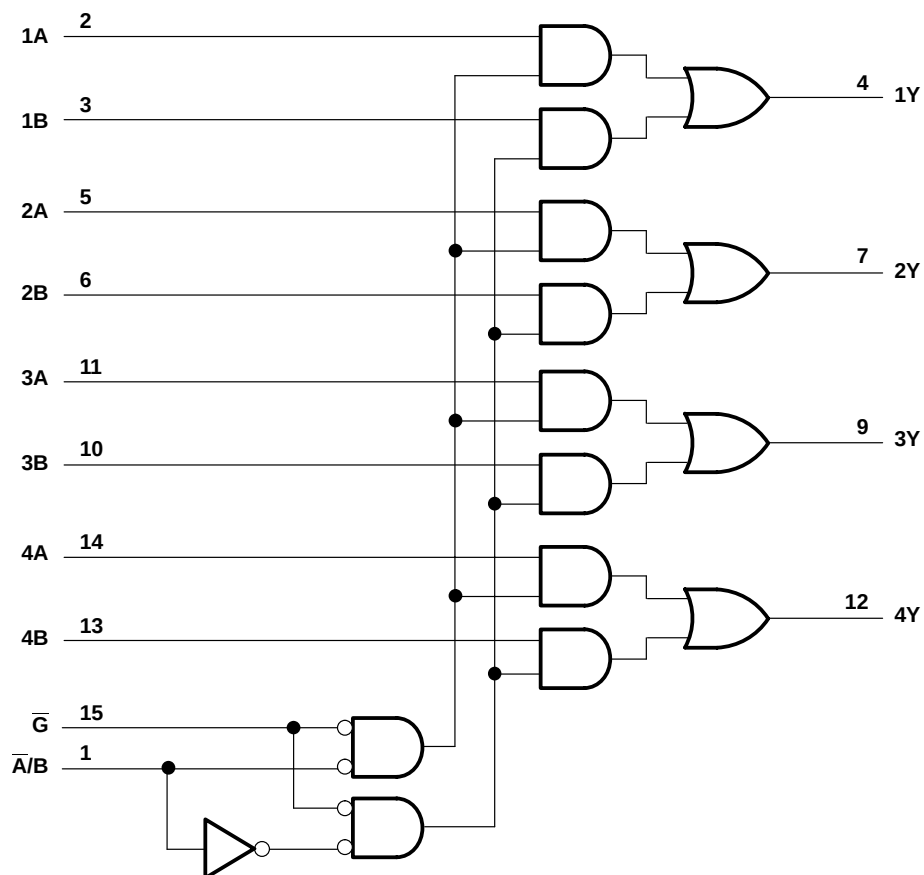
SCLS397 – APRIL 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

SN54LV157A, SN74LV157A QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCLS397 – APRIL 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
NS package	111°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV157A		SN74LV157A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−6		−6		
		V _{CC} = 4.5 V to 5.5 V	−12		−12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	6		6		
		V _{CC} = 4.5 V to 5.5 V	12		12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LV157A, SN74LV157A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV157A			SN74LV157A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -6 mA	3 V	2.48			2.48			
	I _{OH} = -12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V							pF
		5 V							

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV157A		SN74LV157A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	Y	C _L = 15 pF								ns
	$\bar{A}/B$	Y									
	$\bar{G}$	Y									
t _{pd}	A or B	Y	C _L = 50 pF								ns
	$\bar{A}/B$	Y									
	$\bar{G}$	Y									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV157A		SN74LV157A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	Y	C _L = 15 pF								ns
	$\bar{A}/B$	Y									
	$\bar{G}$	Y									
t _{pd}	A or B	Y	C _L = 50 pF								ns
	$\bar{A}/B$	Y									
	$\bar{G}$	Y									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.



SN54LV157A, SN74LV157A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV157A		SN74LV157A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A or B	Y	$C_L = 15\text{ pF}$								ns
	$\overline{A}/B$	Y									
	$\overline{G}$	Y									
t_{pd}	A or B	Y	$C_L = 50\text{ pF}$								ns
	$\overline{A}/B$	Y									
	$\overline{G}$	Y									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV157A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage				V
$V_{IL(D)}$	Low-level dynamic input voltage				V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$		3.3 V		pF
				5 V		

PRODUCT PREVIEW

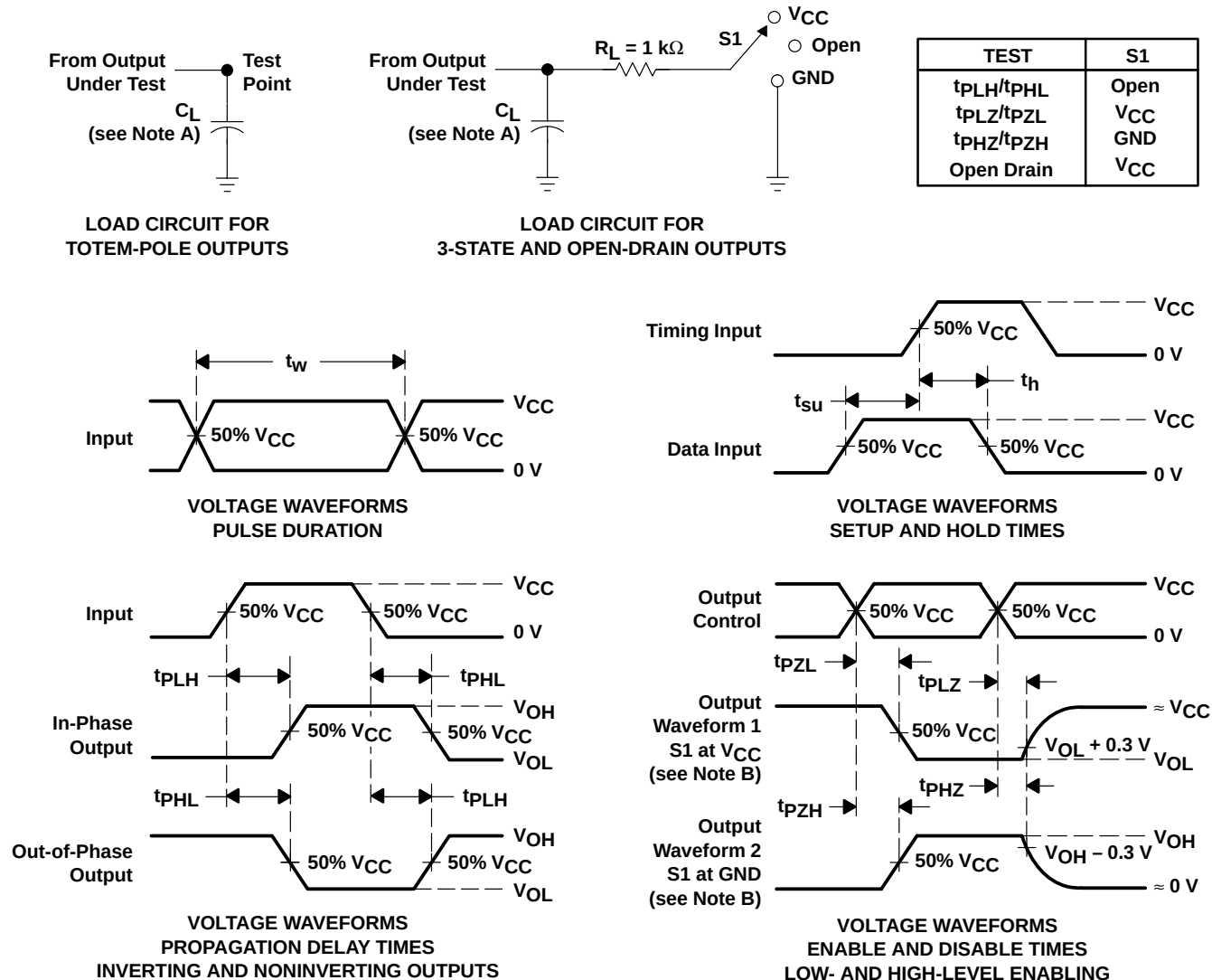


SN54LV157A, SN74LV157A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 $< 0.8\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 $> 2\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

The 'LV161A devices are 4-bit synchronous binary counters designed for 2-V to 5.5-V V_{CC} operation.

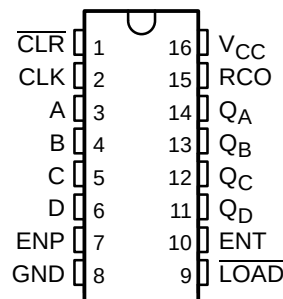
These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that normally are associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

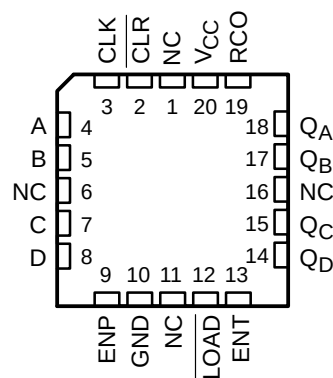
The clear function for the 'LV161A devices is asynchronous. A low level at the clear ($\overline{\text{CLR}}$) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, load ($\overline{\text{LOAD}}$), or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are ENP, ENT, and a ripple-carry output (RCO). Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

SN54LV161A . . . J OR W PACKAGE
SN74LV161A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV161A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LV161A, SN74LV161A

4-BIT SYNCHRONOUS BINARY COUNTERS

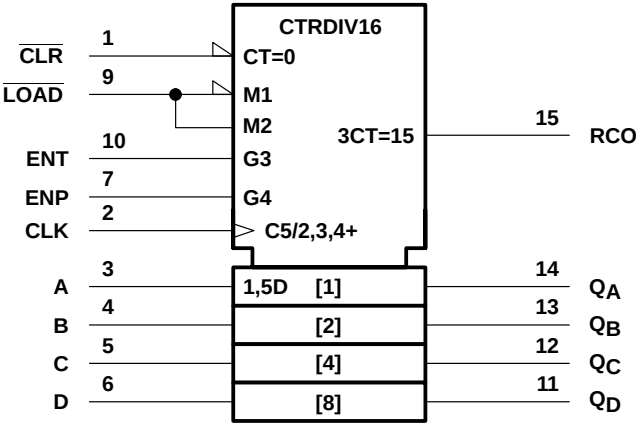
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description (continued)

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

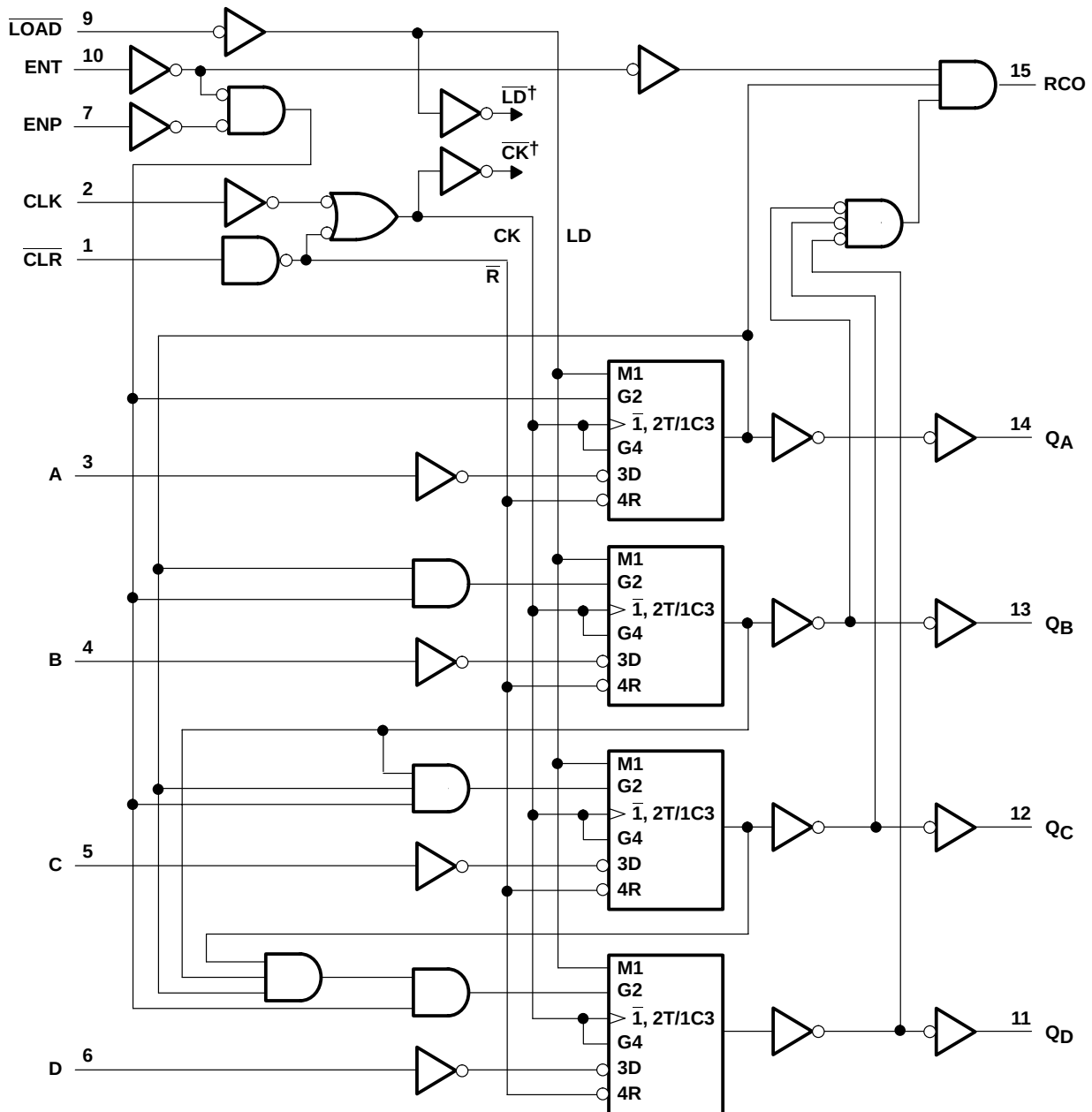
The SN54LV161A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV161A is characterized for operation from -40°C to 85°C .

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

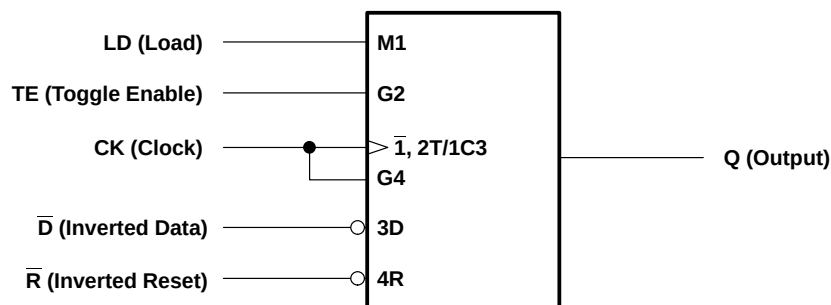
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

PRODUCT PREVIEW

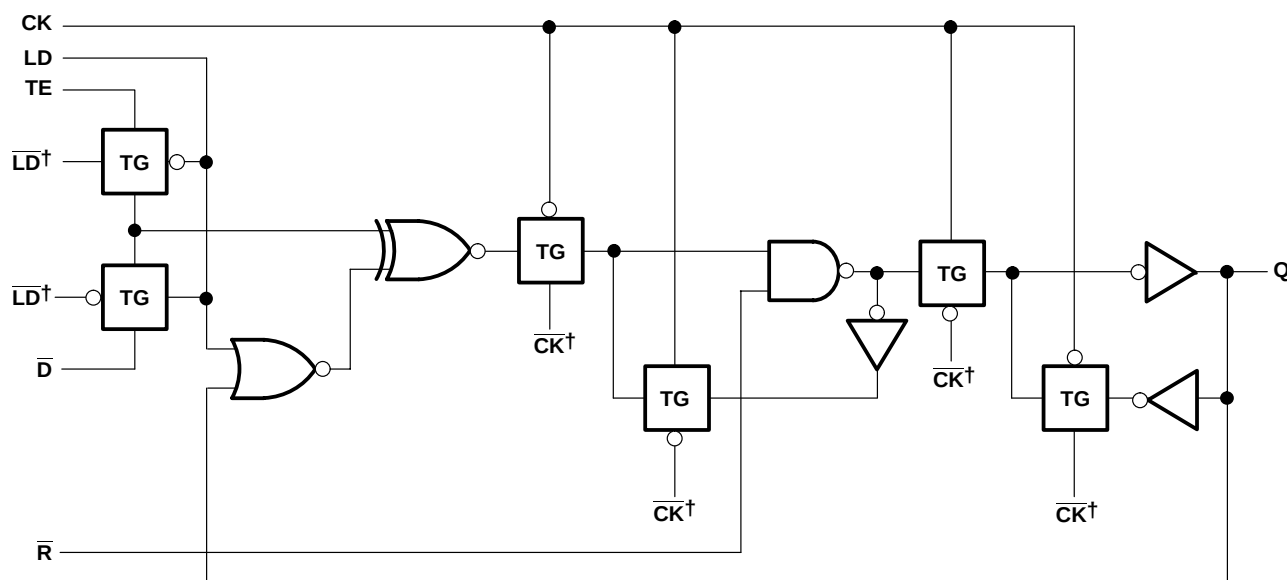
SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

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logic symbol, each D/T flip-flop



logic diagram, each D/T flip-flop (positive logic)



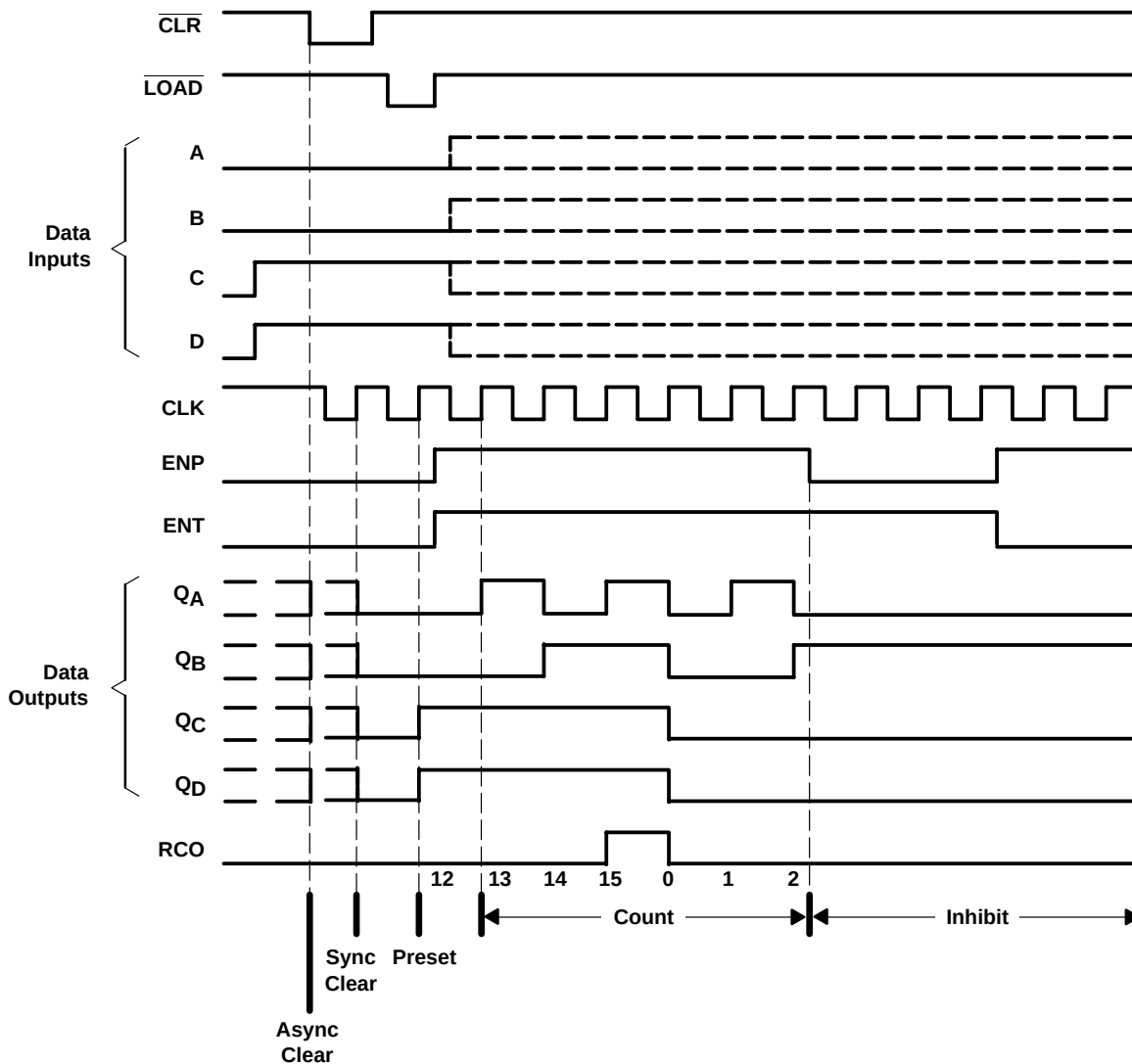
† The origins of $\overline{LD}$ and $\overline{CK}$ are shown in the logic diagram of the overall device.

PRODUCT PREVIEW

typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (asynchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



PRODUCT PREVIEW

SN54LV161A, SN74LV161A

4-BIT SYNCHRONOUS BINARY COUNTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
NS package	111°C/W
PW package	149°C/W

Storage temperature range, T_{stg} –65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV161A		SN74LV161A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−6		−6		
		V _{CC} = 4.5 V to 5.5 V	−12		−12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	6		6		
		V _{CC} = 4.5 V to 5.5 V	12		12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV161A			SN74LV161A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –6 mA	3 V	2.48			2.48			
	I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V							pF
		5 V							

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		SN54LV161A		SN74LV161A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration	CLK high or low							ns
		CLR low							
t _{su}	Setup time before CLK↑	CLR							ns
		Data (A, B, C, and D)							
		ENP, ENT							
		LOAD low							
t _h	Hold time, all synchronous inputs after CLK↑								ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		SN54LV161A		SN74LV161A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration	CLK high or low							ns
		CLR low							
t _{su}	Setup time before CLK↑	CLR							ns
		Data (A, B, C, and D)							
		ENP, ENT							
		LOAD low							
t _h	Hold time, all synchronous inputs after CLK↑								ns

PRODUCT PREVIEW



SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV161A		SN74LV161A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low						ns
		$\overline{\text{CLR}}$ low						
t_{su}	Setup time before $\text{CLK}\uparrow$	$\overline{\text{CLR}}$						ns
		Data (A, B, C, and D)						
		ENP, ENT						
		$\overline{\text{LOAD}}$ low						
t_h	Hold time, all synchronous inputs after $\text{CLK}\uparrow$							ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV161A		SN74LV161A		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f _{max}			C _L = 15 pF*								MHz	
			C _L = 50 pF									
t _{PLH} *	CLK	Q	C _L = 15 pF								ns	
t _{PHL} *												
t _{PLH} *	CLK	RCO (count mode)										
t _{PHL} *												
t _{PLH} *	CLK	RCO (preset mode)										
t _{PHL} *												
t _{PLH} *	ENT	RCO										
t _{PHL} *												
t _{PHL} *	$\overline{\text{CLR}}$	Q										
		RCO										
t _{PLH}	CLK	Q	C _L = 50 pF								ns	
t _{PHL}												
t _{PLH}	CLK	RCO (count mode)										
t _{PHL}												
t _{PLH}	CLK	RCO (preset mode)										
t _{PHL}												
t _{PLH}	ENT	RCO										
t _{PHL}												
t _{PHL}	$\overline{\text{CLR}}$	Q										
		RCO										

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW



SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV161A		SN74LV161A		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f _{max}			C _L = 15 pF*								MHz	
			C _L = 50 pF									
t _{PLH} *	CLK	Q	C _L = 15 pF								ns	
t _{PHL} *												
t _{PLH} *	CLK	RCO (count mode)										
t _{PHL} *												
t _{PLH} *	CLK	RCO (preset mode)										
t _{PHL} *												
t _{PLH} *	ENT	RCO										
t _{PHL} *												
t _{PHL} *	CLR	Q										
		RCO										
t _{PLH}	CLK	Q	C _L = 50 pF								ns	
t _{PHL}												
t _{PLH}	CLK	RCO (count mode)										
t _{PHL}												
t _{PLH}	CLK	RCO (preset mode)										
t _{PHL}												
t _{PLH}	ENT	RCO										
t _{PHL}												
t _{PHL}	CLR	Q										
		RCO										

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW



SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV161A		SN74LV161A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF*								MHz
			C _L = 50 pF								
t _{PLH} *	CLK	Q	C _L = 15 pF							ns	
t _{PHL} *											
t _{PLH} *	CLK	RCO (count mode)									
t _{PHL} *											
t _{PLH} *	CLK	RCO (preset mode)									
t _{PHL} *											
t _{PLH} *	ENT	RCO									
t _{PHL} *											
t _{PHL} *	$\overline{\text{CLR}}$	Q								ns	
		RCO									
t _{PLH}	CLK	Q	C _L = 50 pF								
t _{PHL}											
t _{PLH}	CLK	RCO (count mode)									
t _{PHL}											
t _{PLH}	CLK	RCO (preset mode)									
t _{PHL}											
t _{PLH}	ENT	RCO									
t _{PHL}											
t _{PHL}	$\overline{\text{CLR}}$	Q									
		RCO									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

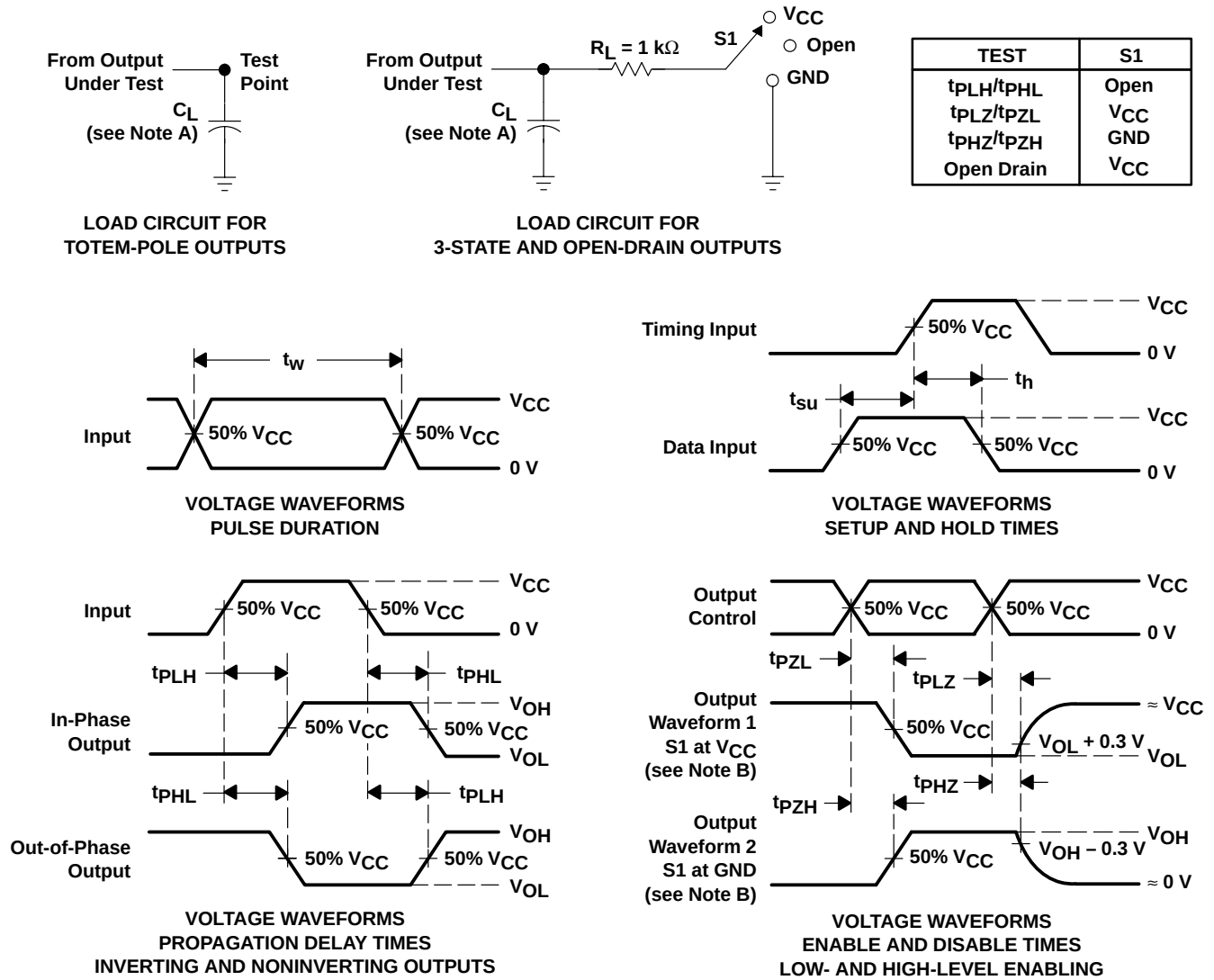
PARAMETER	SN74LV161A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$ High-level dynamic input voltage				V
$V_{IL(D)}$ Low-level dynamic input voltage				V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V		pF
		5 V		

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV163A, SN74LV163A 4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS405 – APRIL 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

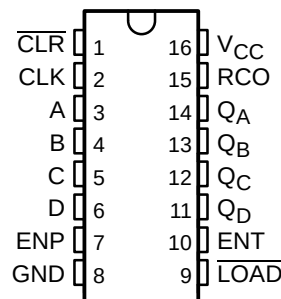
The 'LV163A devices are 4-bit synchronous binary counters designed for 2-V to 5.5-V V_{CC} operation.

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'LV163A devices are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

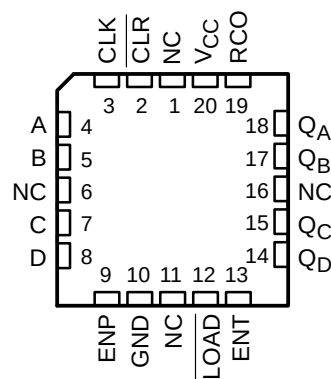
These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the 'LV163A devices is synchronous. A low level at the clear ($\overline{\text{CLR}}$) input sets all four of the flip-flop outputs low after the next low-to-high transition of CLK, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to $\overline{\text{CLR}}$ to synchronously clear the counter to 0000 (LLLL).

SN54LV163A . . . J OR W PACKAGE
SN74LV163A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV163A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

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SN54LV163A, SN74LV163A
4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS405 – APRIL 1998

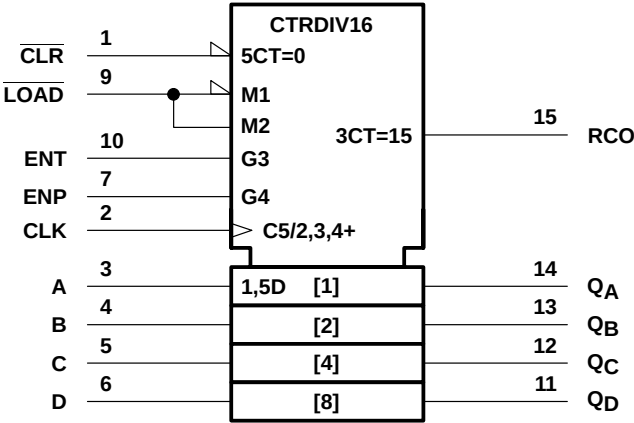
description (continued)

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP, ENT, and a ripple-carry output (RCO) are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

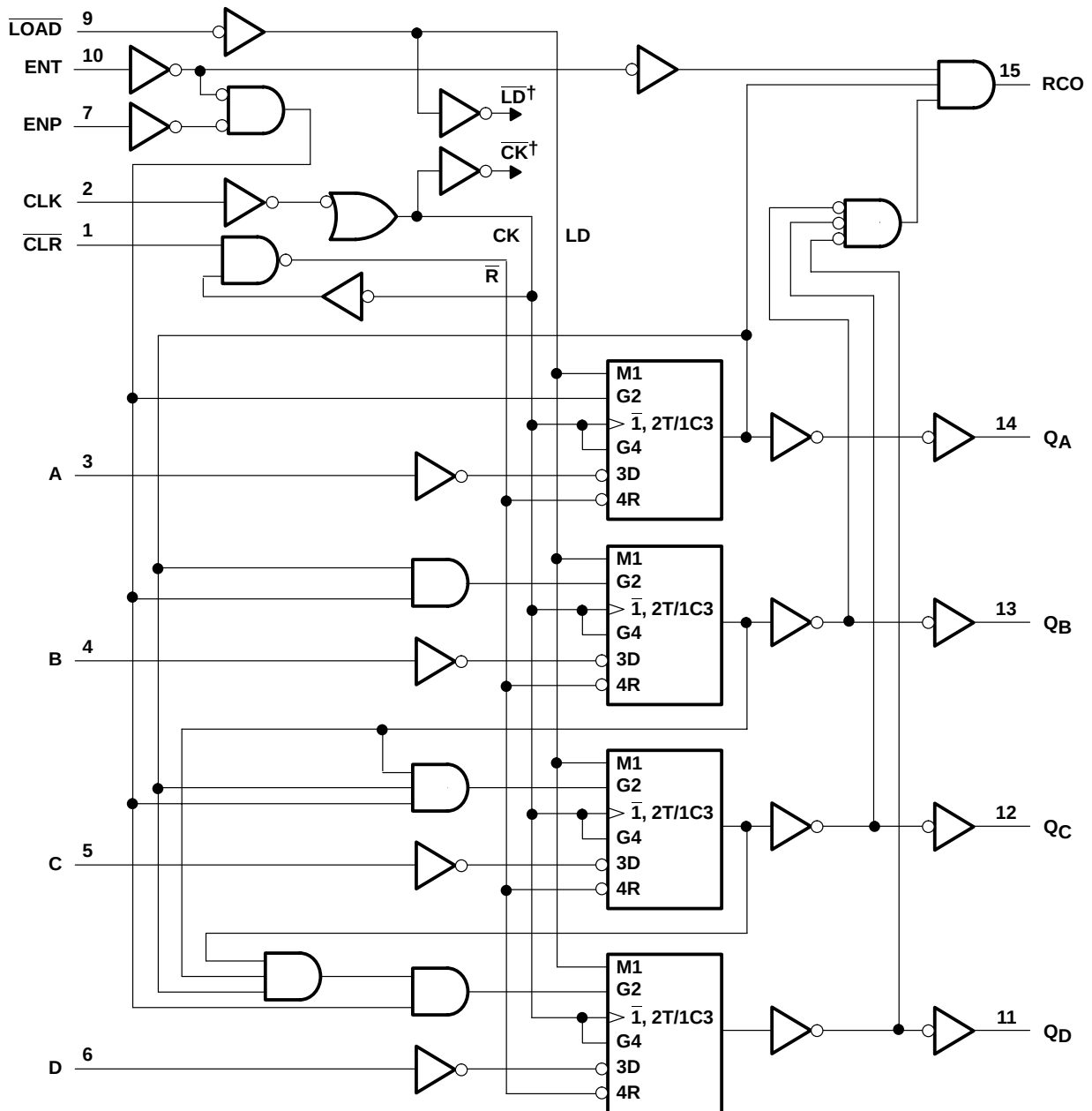
The SN54LV163A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV163A is characterized for operation from –40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

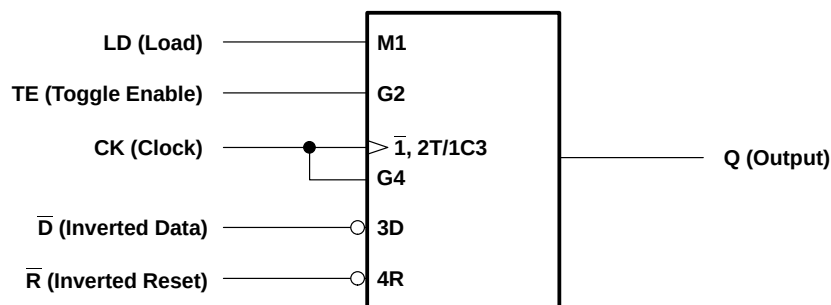
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

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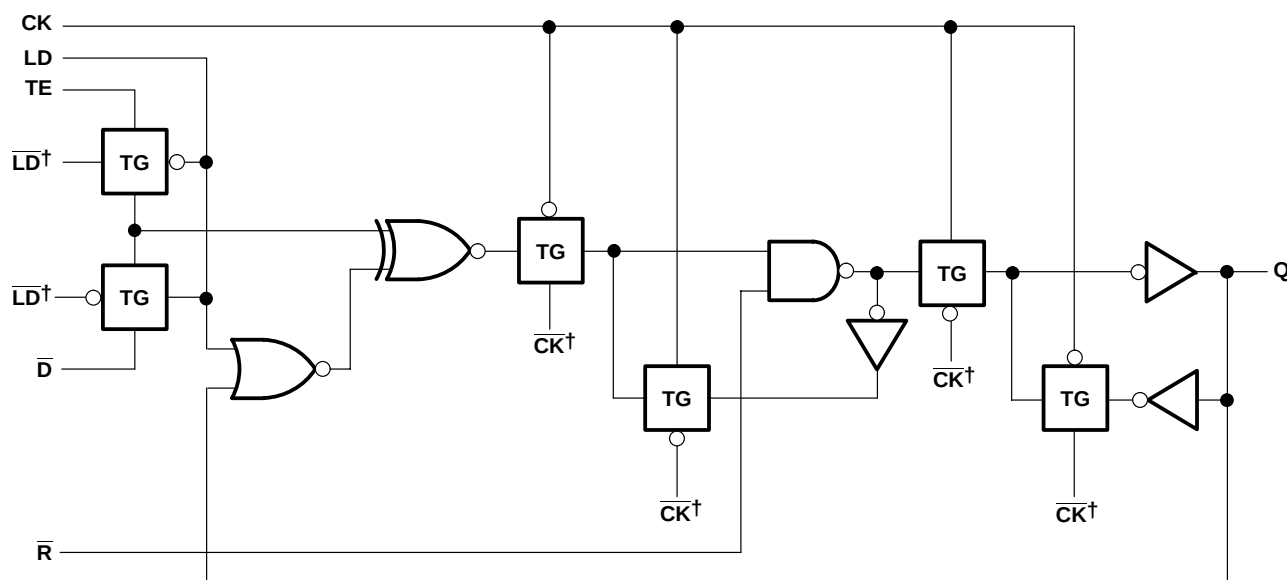
SN54LV163A, SN74LV163A 4-BIT SYNCHRONOUS BINARY COUNTERS

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logic symbol, each D/T flip-flop



logic diagram, each D/T flip-flop (positive logic)



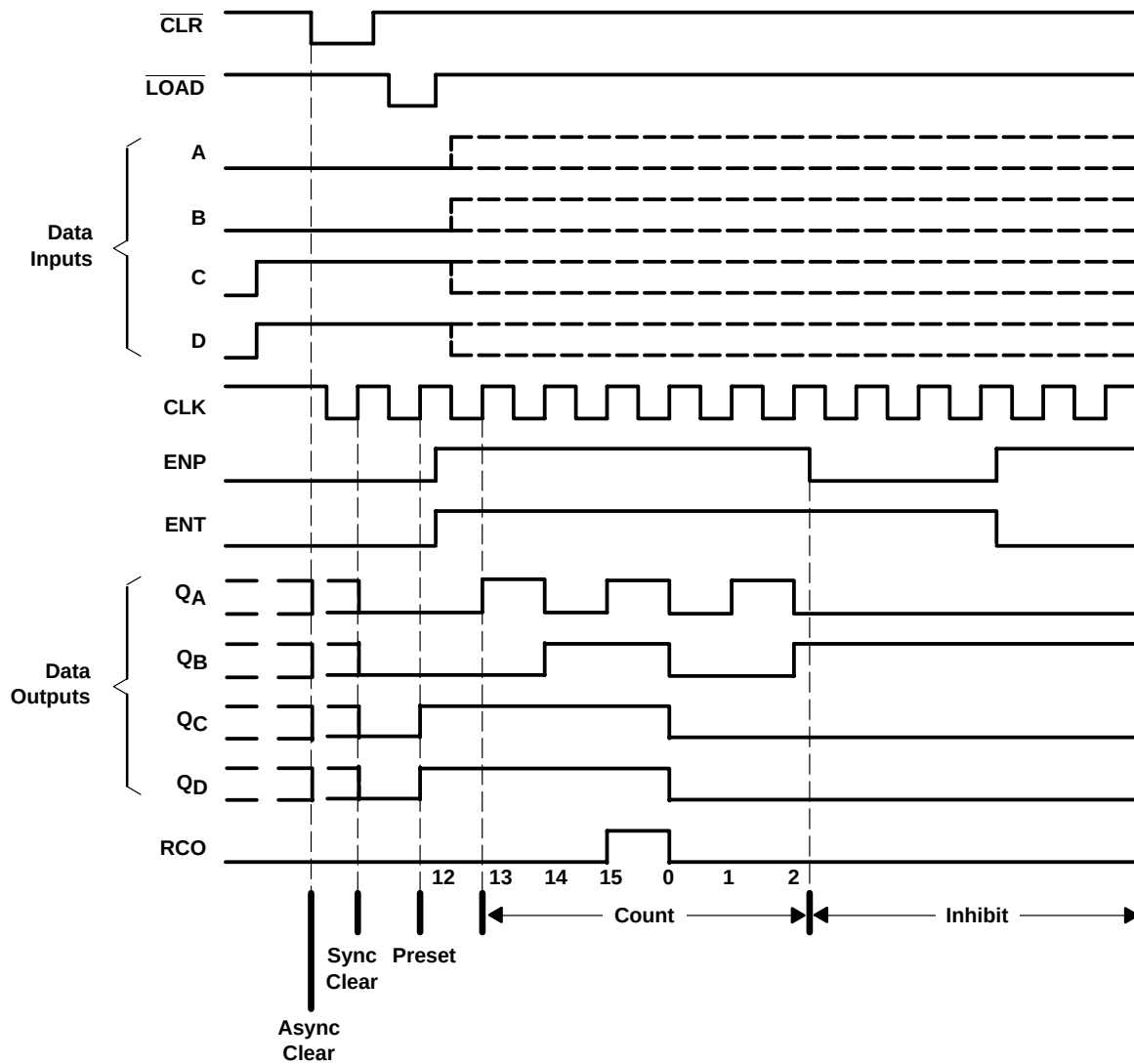
† The origins of $\overline{LD}$ and $\overline{CK}$ are shown in the logic diagram of the overall device.

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typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (synchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



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SN54LV163A, SN74LV163A

4-BIT SYNCHRONOUS BINARY COUNTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
NS package	111°C/W
PW package	149°C/W

Storage temperature range, T_{stg} –65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV163A		SN74LV163A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−6		−6		
		V _{CC} = 4.5 V to 5.5 V	−12		−12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	6		6		
		V _{CC} = 4.5 V to 5.5 V	12		12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LV163A, SN74LV163A 4-BIT SYNCHRONOUS BINARY COUNTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV163A			SN74LV163A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -6 mA	3 V	2.48			2.48			
	I _{OH} = -12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V							pF
		5 V							

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54LV163A		SN74LV163A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, CLK high or low							ns
t _{su}	Setup time before CLK↑	CLR						ns
		Data (A, B, C, and D)						
		ENP, ENT						
		LOAD low						
t _h	Hold time, all synchronous inputs after CLK↑							ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54LV163A		SN74LV163A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, CLK high or low							ns
t _{su}	Setup time before CLK↑	CLR						ns
		Data (A, B, C, and D)						
		ENP, ENT						
		LOAD low						
t _h	Hold time, all synchronous inputs after CLK↑							ns

PRODUCT PREVIEW



SN54LV163A, SN74LV163A

4-BIT SYNCHRONOUS BINARY COUNTERS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV163A		SN74LV163A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, CLK high or low							ns
t_{su}	Setup time before CLK $\uparrow$	$\overline{\text{CLR}}$						ns
		Data (A, B, C, and D)						
		ENP, ENT						
		$\overline{\text{LOAD}}$ low						
t_h	Hold time, all synchronous inputs after CLK $\uparrow$							ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV163A		SN74LV163A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF*								MHz
			C _L = 50 pF								
t _{PLH} *	CLK	Q	C _L = 15 pF								ns
t _{PHL} *											
t _{PLH} *	CLK	RCO (count mode)									
t _{PHL} *											
t _{PLH} *	CLK	RCO (preset mode)									
t _{PHL} *											
t _{PLH} *	ENT	RCO									
t _{PHL} *											
t _{PLH}	CLK	Q	C _L = 50 pF								ns
t _{PHL}											
t _{PLH}	CLK	RCO (count mode)									
t _{PHL}											
t _{PLH}	CLK	RCO (preset mode)									
t _{PHL}											
t _{PLH}	ENT	RCO									
t _{PHL}											

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW



SN54LV163A, SN74LV163A 4-BIT SYNCHRONOUS BINARY COUNTERS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV163A		SN74LV163A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF*								MHz
			C _L = 50 pF								
t _{PLH} *	CLK	Q	C _L = 15 pF							ns	
t _{PHL} *											
t _{PLH} *	CLK	RCO (count mode)									
t _{PHL} *											
t _{PLH} *	CLK	RCO (preset mode)									
t _{PHL} *											
t _{PLH} *	ENT	RCO									
t _{PHL} *											
t _{PLH}	CLK	Q	C _L = 50 pF							ns	
t _{PHL}											
t _{PLH}	CLK	RCO (count mode)									
t _{PHL}											
t _{PLH}	CLK	RCO (preset mode)									
t _{PHL}											
t _{PLH}	ENT	RCO									
t _{PHL}											

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV163A		SN74LV163A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF*								MHz
			C _L = 50 pF								
t _{PLH} *	CLK	Q	C _L = 15 pF							ns	
t _{PHL} *											
t _{PLH} *	CLK	RCO (count mode)									
t _{PHL} *											
t _{PLH} *	CLK	RCO (preset mode)									
t _{PHL} *											
t _{PLH} *	ENT	RCO									
t _{PHL} *											
t _{PLH}	CLK	Q	C _L = 50 pF							ns	
t _{PHL}											
t _{PLH}	CLK	RCO (count mode)									
t _{PHL}											
t _{PLH}	CLK	RCO (preset mode)									
t _{PHL}											
t _{PLH}	ENT	RCO									
t _{PHL}											

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW



SN54LV163A, SN74LV163A
4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS405 – APRIL 1998

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

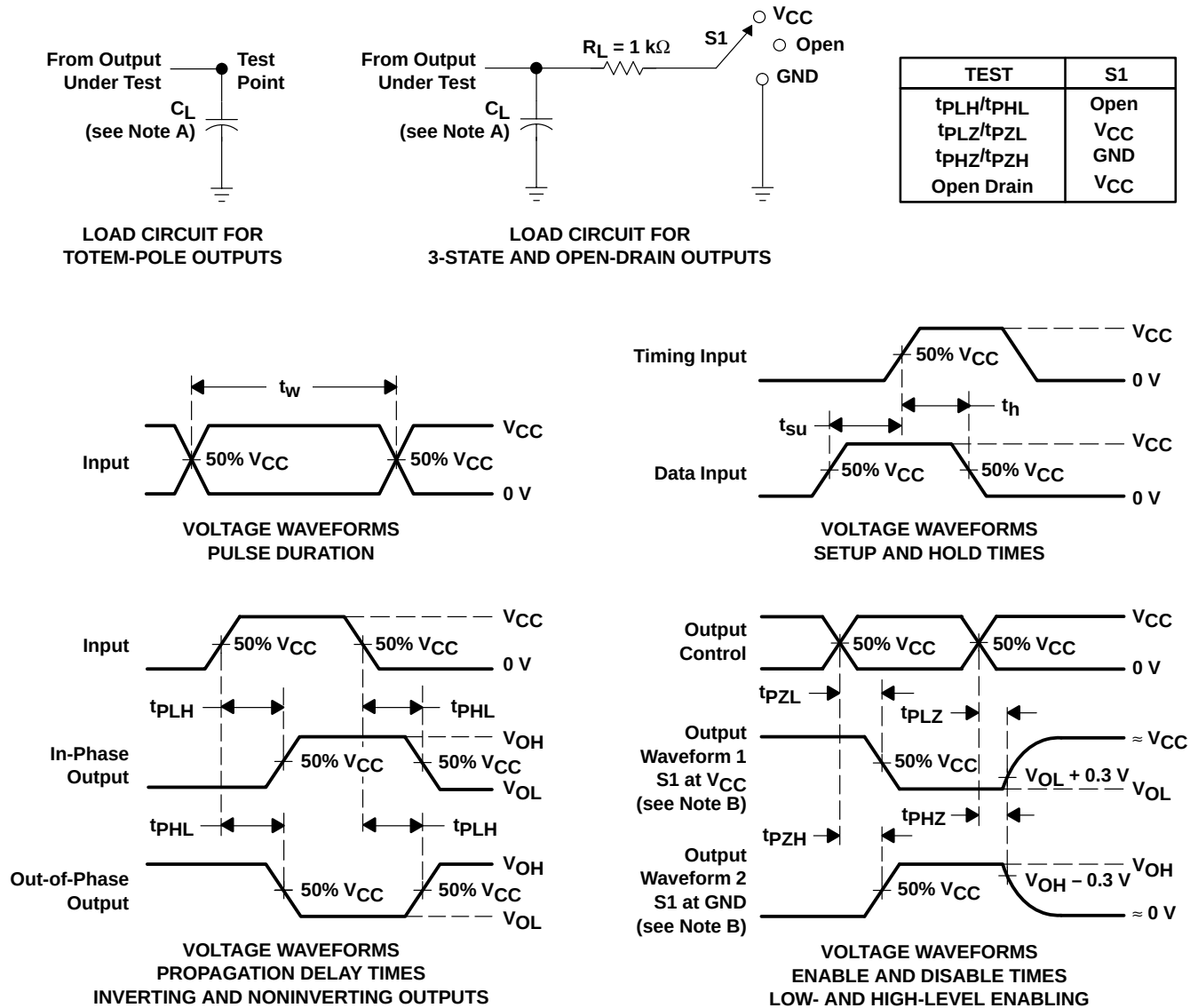
PARAMETER	SN74LV163A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$ High-level dynamic input voltage				V
$V_{IL(D)}$ Low-level dynamic input voltage				V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V		pF
		5 V		

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV164A, SN74LV164A 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

SCLS403B – APRIL 1998 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 $< 0.8\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 $> 2\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

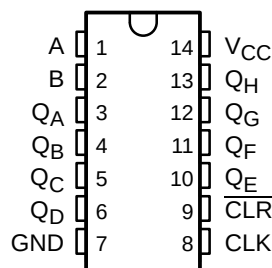
description

The 'LV164A devices are 8-bit parallel-out serial shift registers designed for 2-V to 5.5-V V_{CC} operation.

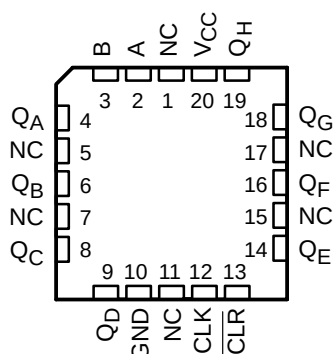
These devices feature AND-gated serial (A and B) inputs and an asynchronous clear ($\overline{\text{CLR}}$) input. The gated serial inputs permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock (CLK) input.

The SN54LV164A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV164A is characterized for operation from -40°C to 85°C .

SN54LV164A ... J OR W PACKAGE
SN74LV164A ... D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV164A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS		
$\overline{\text{CLR}}$	CLK	A	B	QA	QB ... QH	
L	X	X	X	L	L	L
H	L	X	X	QA0	QB0	QH0
H	↑	H	H	H	QAn	QGn
H	↑	L	X	L	QAn	QGn
H	↑	X	L	L	QAn	QGn

QA0, QB0, QH0 = the level of QA, QB, or QH, respectively, before the indicated steady-state inputs conditions were established

QAn, QGn = the level of QA or QG before the most recent ↑ transition of the clock; indicates a 1-bit shift

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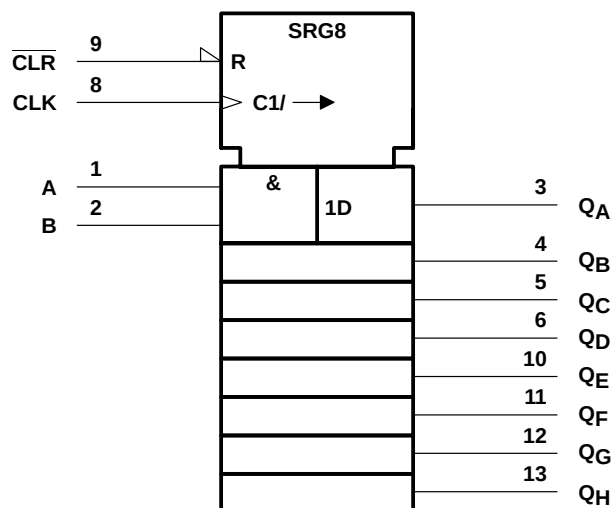
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SN54LV164A, SN74LV164A

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

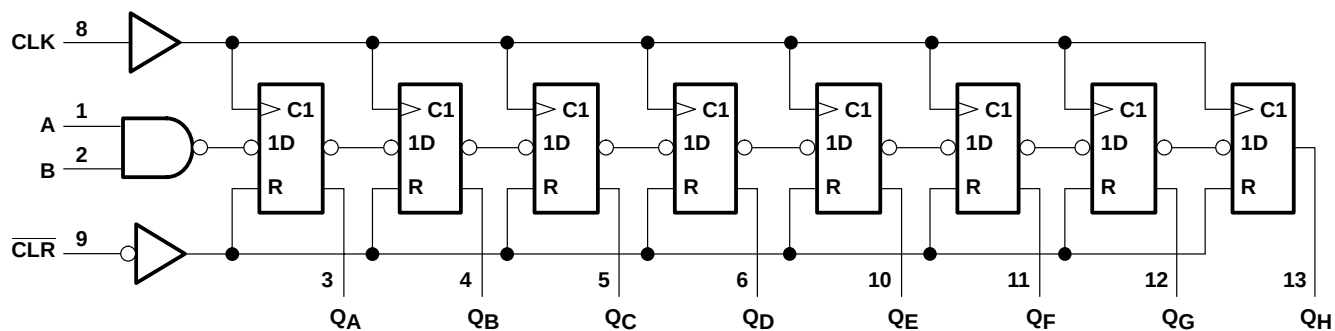
SCLS403B – APRIL 1998 – REVISED JUNE 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)

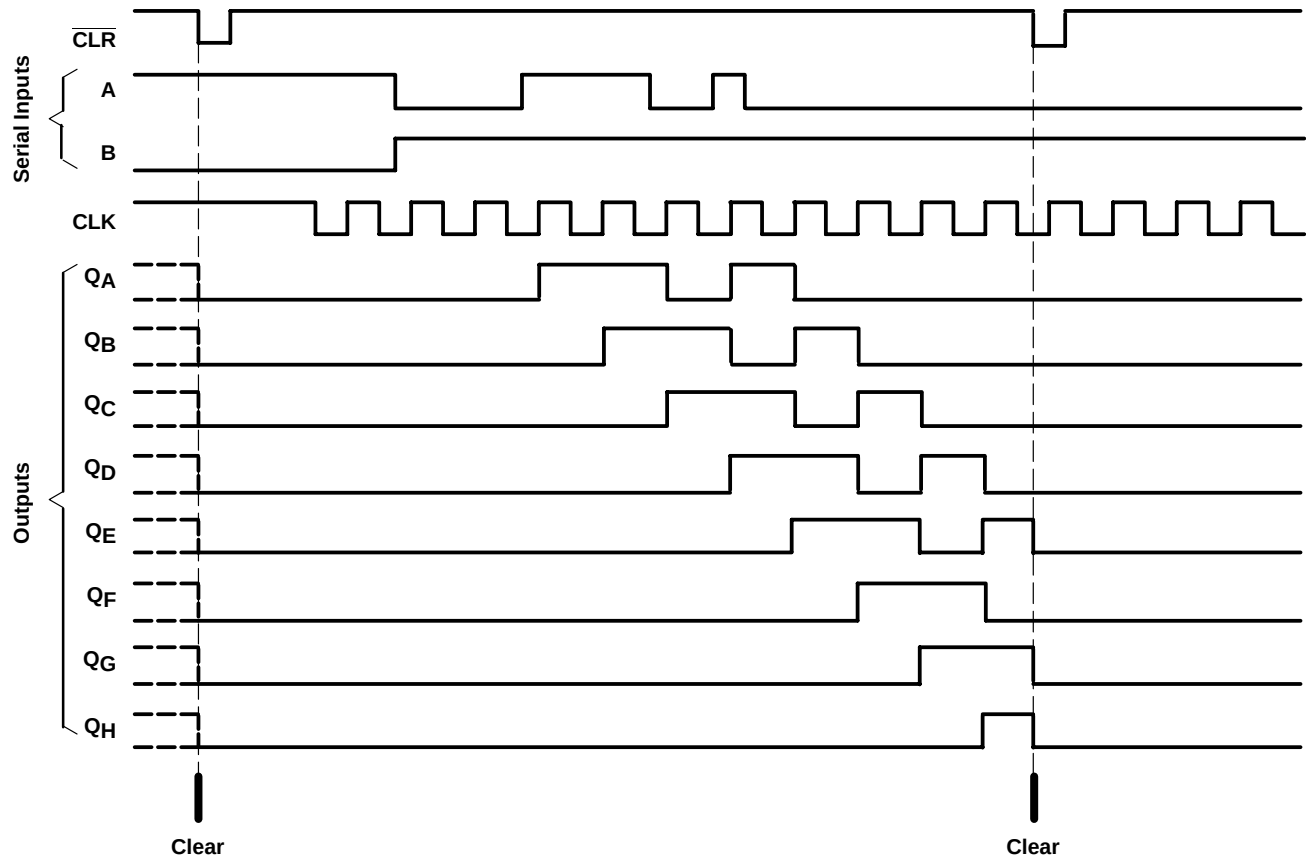


Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

SN54LV164A, SN74LV164A 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

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typical clear, shift, and clear sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	127°C/W
DB package	158°C/W
DGV package	182°C/W
NS package	127°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.



SN54LV164A, SN74LV164A

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

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recommended operating conditions (see Note 4)

			SN54LV164A		SN74LV164A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−6		−6		
		V _{CC} = 4.5 V to 5.5 V	−12		−12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	6		6		
		V _{CC} = 4.5 V to 5.5 V	12		12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV164A			SN74LV164A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = −50 μA	2 V to 5.5 V	V _{CC} −0.1			V _{CC} −0.1			V
	I _{OH} = −2 mA	2.3 V	2			2			
	I _{OH} = −6 mA	3 V	2.48			2.48			
	I _{OH} = −12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	2.2			2.2			pF

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SN54LV164A, SN74LV164A 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV164A		SN74LV164A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLR low	6		6.5		6.5		ns
		CLK high or low	6.5		7.5		7.5		
t_{su}	Setup time	Data before CLK $\uparrow$	6.5		8.5		8.5		ns
		CLR inactive	3		3		3		
t_h	Hold time	Data after CLK $\uparrow$	-0.5		0		0		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV164A		SN74LV164A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLR low	5		5		5		ns
		CLK high or low	5		5		5		
t_{su}	Setup time	Data before CLK $\uparrow$	5		6		6		ns
		CLR inactive	2.5		2.5		2.5		
t_h	Hold time	Data after CLK $\uparrow$	0		0		0		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV164A		SN74LV164A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLR low	5		5		5		ns
		CLK high or low	5		5		5		
t_{su}	Setup time	Data before CLK $\uparrow$	4.5		4.5		4.5		ns
		CLR inactive	2.5		2.5		2.5		
t_h	Hold time	Data after CLK $\uparrow$	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV164A		SN74LV164A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$	55	105		50		50		MHz
			$C_L = 50\text{ pF}$	45	85		40		40		
t_{pd}^*	CLK	Q	$C_L = 15\text{ pF}$	9.2	17.6		1	20	1	20	ns
t_{PHL}^*	CLR	Q		8.6	16		1	18	1	18	
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$	11.5	21.1		1	24	1	24	ns
t_{PHL}	CLR	Q		10.8	19.5		1	22	1	22	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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SN54LV164A, SN74LV164A

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV164A		SN74LV164A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			$C_L = 15\text{ pF}^*$	80	155		65		65		MHz
			$C_L = 50\text{ pF}$	50	120		45		45		
t_{pd}^*	CLK	Q	$C_L = 15\text{ pF}$		6.4	12.8	1	15	1	15	ns
t_{PHL}^*	$\overline{\text{CLR}}$				6	12.8	1	15	1	15	
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$		8.3	16.3	1	18.5	1	18.5	ns
t_{PHL}	$\overline{\text{CLR}}$				7.9	16.3	1	18.5	1	18.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV164A		SN74LV164A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			$C_L = 15\text{ pF}^*$	125	220		105		105		MHz
			$C_L = 50\text{ pF}$	85	165		75		75		
t_{pd}^*	CLK	Q	$C_L = 15\text{ pF}$		4.5	9	1	10.5	1	10.5	ns
t_{PHL}^*	$\overline{\text{CLR}}$				4.2	8.6	1	10	1	10	
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$		6	11	1	12.5	1	12.5	ns
t_{PHL}	$\overline{\text{CLR}}$				5.8	10.6	1	12.5	1	12.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV164A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.28	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.22	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.09		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

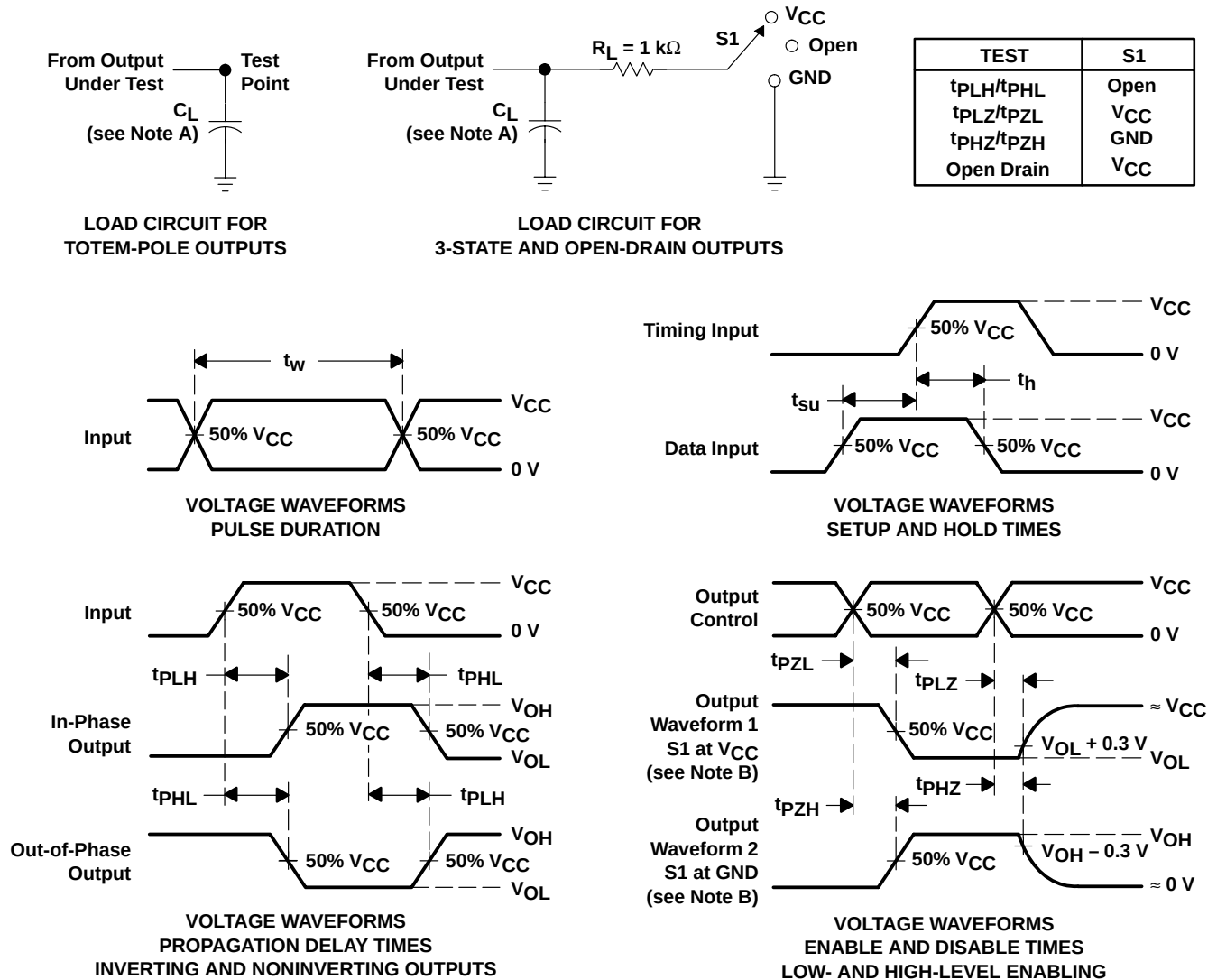
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	48.1	pF
			5 V	47.5	

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

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- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
< 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

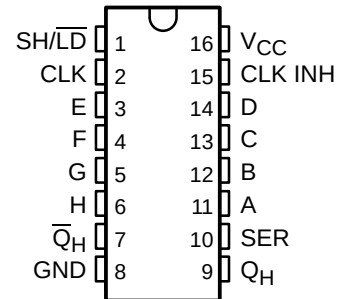
The 'LV165A devices are parallel-load, 8-bit shift registers designed for 2-V to 5.5-V V_{CC} operation.

When the device is clocked, data is shifted toward the serial output Q_H . Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the shift/load ($SH/\overline{LD}$) input. The 'LV165A devices feature a clock inhibit function and a complemented serial output $\overline{Q}_H$.

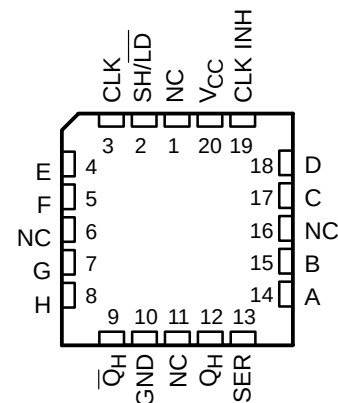
Clocking is accomplished by a low-to-high transition of the clock (CLK) input while $SH/\overline{LD}$ is held high and clock inhibit (CLK INH) is held low. The functions of the CLK and CLK INH inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLK INH accomplishes clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when $SH/\overline{LD}$ is held high. The parallel inputs to the register are enabled while $SH/\overline{LD}$ is held low, independently of the levels of CLK, CLK INH, or SER.

The SN54LV165A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV165A is characterized for operation from -40°C to 85°C .

SN54LV165A . . . J OR W PACKAGE
SN74LV165A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV165A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS			OPERATION
$SH/\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	Q_0
H	X	H	Q_0
H	L	↑	Shift
H	↑	L	Shift

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 **TEXAS
INSTRUMENTS**

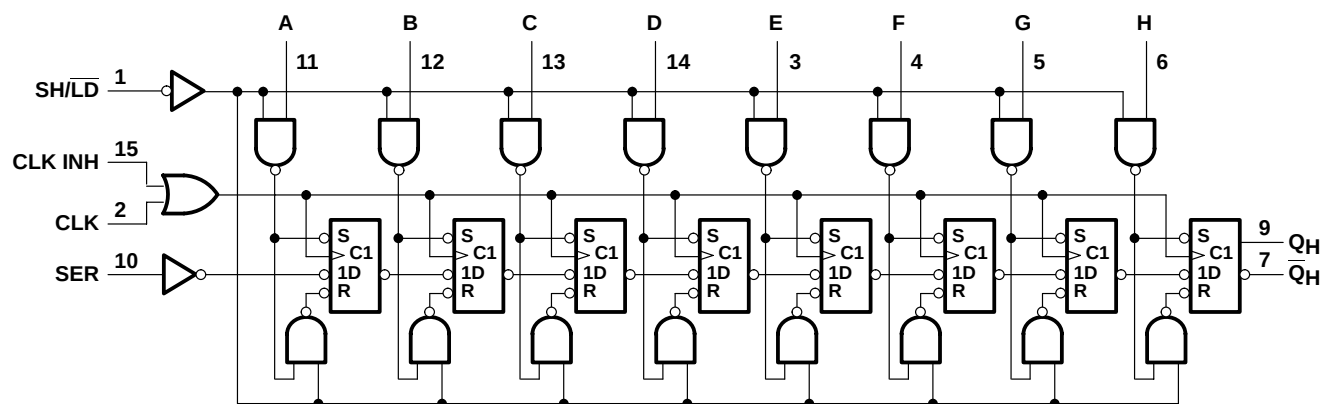
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SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

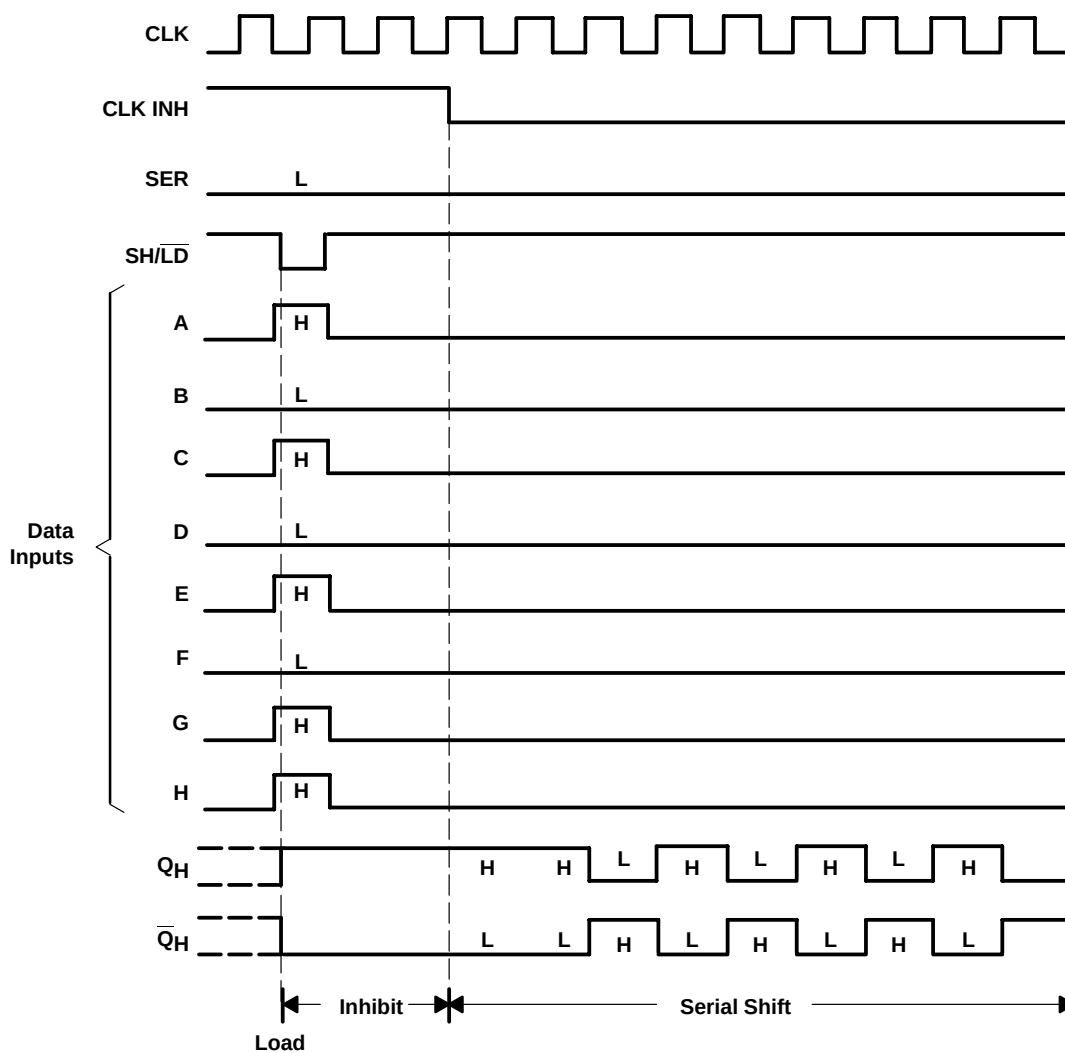
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logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

typical shift, load, and inhibit sequences



SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
NS package	111°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV165A		SN74LV165A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−6		−6		
		V _{CC} = 4.5 V to 5.5 V	−12		−12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	6		6		
		V _{CC} = 4.5 V to 5.5 V	12		12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV165A			SN74LV165A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –6 mA	3 V	2.48			2.48			
	I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	1.7			1.7			pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		SN54LV165A		SN74LV165A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLK high or low	8.5		9		9		ns
		SH/LD low	11		13		13		
t _{su}	Setup time	SH/LD high before CLK↑	7		8.5		8.5		ns
		SER before CLK↑	8.5		9.5		9.5		
		CLK INH before CLK↑	7		7		7		
		Data before SH/LD↑	11.5		12		12		
t _h	Hold time	SER data after CLK↑	−1		0		0		ns
		Parallel data after SH/LD↑	0		0.5		0.5		
		SH/LD high after CLK↑	0		0		0		

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		SN54LV165A		SN74LV165A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLK high or low	6		7		7		ns
		SH/LD low	7.5		9		9		
t _{su}	Setup time	SH/LD high before CLK↑	5		6		6		ns
		SER before CLK↑	5		6		6		
		CLK INH before CLK↑	5		5		5		
		Data before SH/LD↑	7.5		8.5		8.5		
t _h	Hold time	SER data after CLK↑	0		0		0		ns
		Parallel data after SH/LD↑	0.5		0.5		0.5		
		SH/LD high after CLK↑	0		0		0		

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SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV165A		SN74LV165A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLK high or low	4		4		4		ns
		SH/ $\overline{\text{LD}}$ low	5		6		6		
t_{su}	Setup time	SH/ $\overline{\text{LD}}$ high before CLK $\uparrow$	4		4		4		ns
		SER before CLK $\uparrow$	4		4		4		
		CLK INH before CLK $\uparrow$	3.5		3.5		3.5		
		Data before SH/ $\overline{\text{LD}}$ $\uparrow$	5		5		5		
t_h	Hold time	SER data after CLK $\uparrow$	0.5		0.5		0.5		ns
		Parallel data after SH/ $\overline{\text{LD}}$ $\uparrow$	1		1		1		
		SH/ $\overline{\text{LD}}$ high after CLK $\uparrow$	0.5		0.5		0.5		

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV165A		SN74LV165A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$	50	80		45		45		MHz
			$C_L = 50\text{ pF}$	40	65		35		35		
t_{pd}^*	CLK	Q_H or $\overline{Q}_H$	$C_L = 15\text{ pF}$	12.2	19.8		1	22	1	22	ns
	SH/ $\overline{\text{LD}}$			13.1	21.5		1	23.5	1	23.5	
	H			12.9	21.7		1	24	1	24	
t_{pd}	CLK	Q_H or $\overline{Q}_H$	$C_L = 50\text{ pF}$	15.3	23.3		1	26	1	26	ns
	SH/ $\overline{\text{LD}}$			16.1	25.1		1	28	1	28	
	H			15.9	25.3		1	28	1	28	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV165A		SN74LV165A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$	65	115		55		55		MHz
			$C_L = 50\text{ pF}$	60	90		50		50		
t_{pd}^*	CLK	Q_H or $\overline{Q}_H$	$C_L = 15\text{ pF}$	8.6	15.4		1	18	1	18	ns
	SH/ $\overline{\text{LD}}$			9.1	15.8		1	18.5	1	18.5	
	H			8.9	14.1		1	16.5	1	16.5	
t_{pd}	CLK	Q_H or $\overline{Q}_H$	$C_L = 50\text{ pF}$	10.9	18.9		1	21.5	1	21.5	ns
	SH/ $\overline{\text{LD}}$			11.3	19.3		1	22	1	22	
	H			11.1	17.6		1	20	1	20	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV165A		SN74LV165A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$	110	165		90		90		MHz
			$C_L = 50\text{ pF}$	95	125		85		85		
t_{pd}^*	CLK	Q_H or $\overline{Q}_H$	$C_L = 15\text{ pF}$		6	9.9	1	11.5	1	11.5	ns
	SH/ $\overline{\text{LD}}$				6	9.9	1	11.5	1	11.5	
	H				6	9	1	10.5	1	10.5	
t_{pd}	CLK	Q_H or $\overline{Q}_H$	$C_L = 50\text{ pF}$		7.7	11.9	1	13.5	1	13.5	ns
	SH/ $\overline{\text{LD}}$				7.7	11.9	1	13.5	1	13.5	
	H				7.6	11	1	12.5	1	12.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

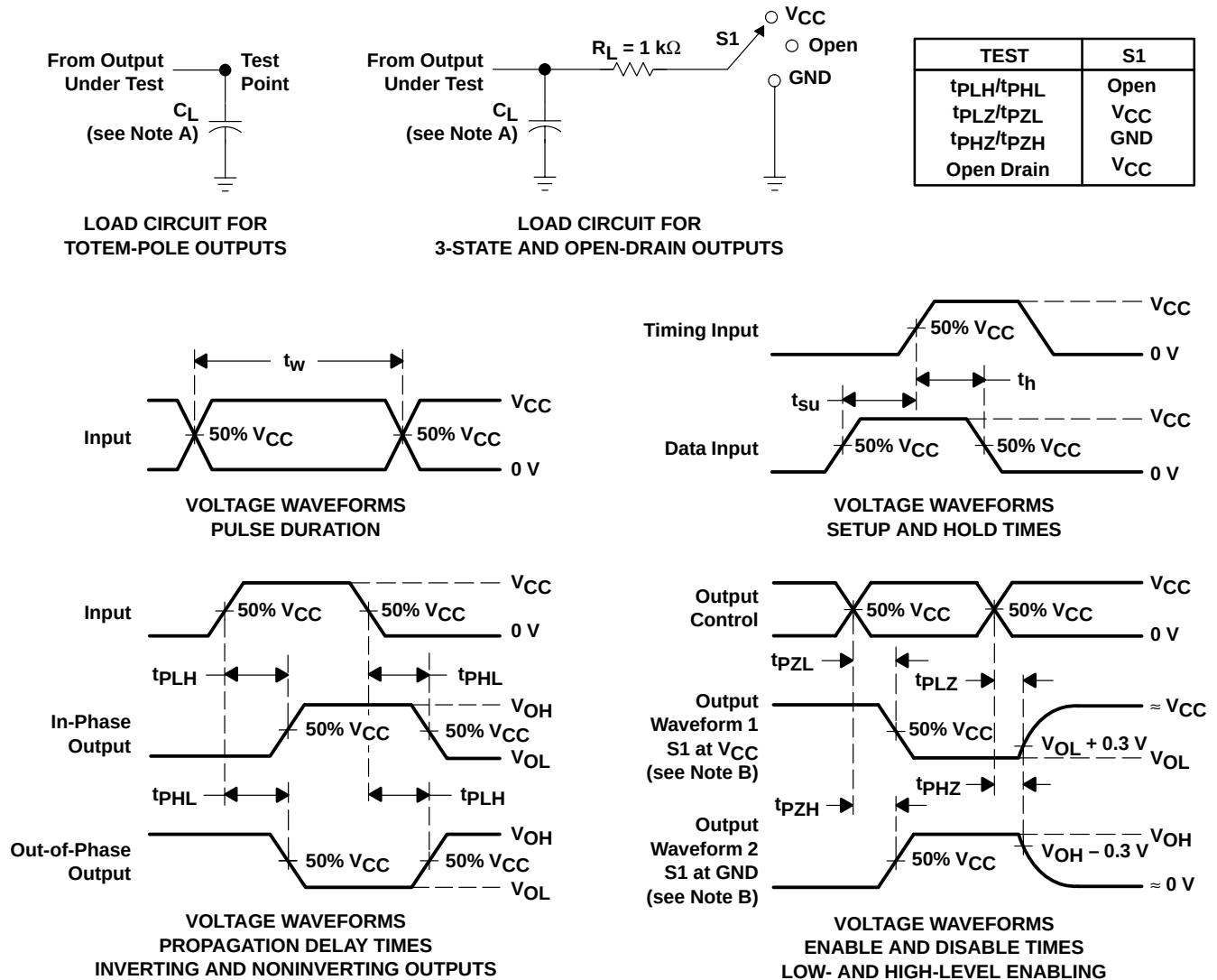
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}, f = 10\text{ MHz}$	3.3 V	36.1	pF
			5 V	37.5	

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV174A, SN74LV174A HEX D-TYPE FLIP-FLOPS WITH CLEAR

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- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

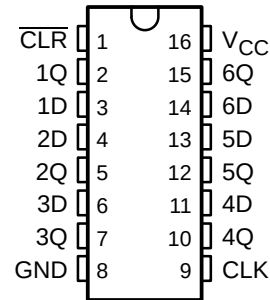
description

The 'LV174A devices are hex D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

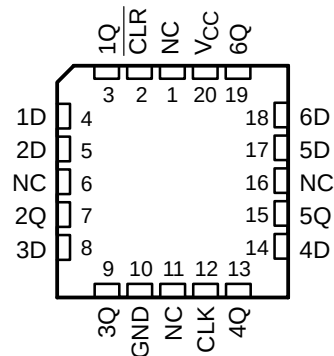
These devices are monolithic positive-edge-triggered flip-flops with a direct clear ($\overline{\text{CLR}}$) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of the clock pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN54LV174A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV174A is characterized for operation from -40°C to 85°C .

SN54LV174A . . . J OR W PACKAGE
SN74LV174A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV174A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS			OUTPUT Q
$\overline{\text{CLR}}$	CLK	D	
L	X	X	L
H	$\uparrow$	H	H
H	$\uparrow$	L	L
H	L	X	Q_0

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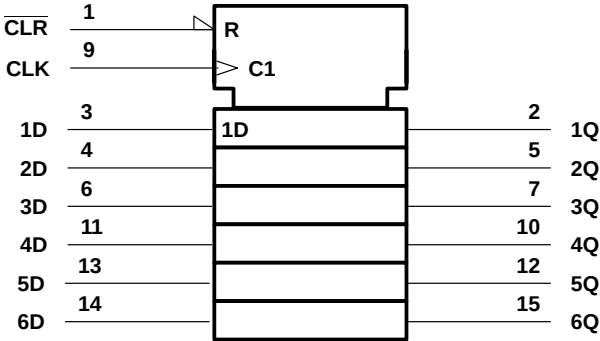
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SN54LV174A, SN74LV174A HEX D-TYPE FLIP-FLOPS WITH CLEAR

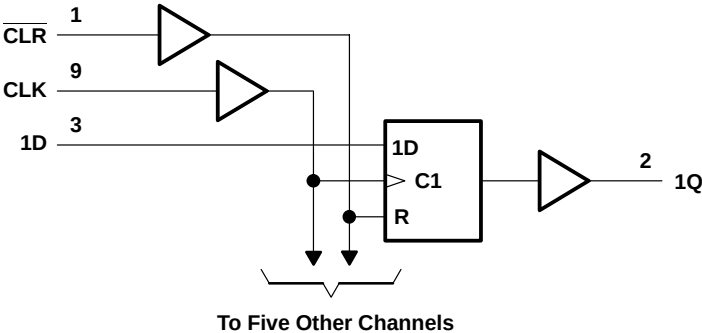
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
NS package	111°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV174A, SN74LV174A HEX D-TYPE FLIP-FLOPS WITH CLEAR

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recommended operating conditions (see Note 4)

			SN54LV174A		SN74LV174A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	–50		–50		μA
		V _{CC} = 2.3 V to 2.7 V	–2		–2		mA
		V _{CC} = 3 V to 3.6 V	–6		–6		
		V _{CC} = 4.5 V to 5.5 V	–12		–12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	6		6		
		V _{CC} = 4.5 V to 5.5 V	12		12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV174A			SN74LV174A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –6 mA	3 V	2.48			2.48			
	I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	1.7			1.7			pF

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SN54LV174A, SN74LV174A

HEX D-TYPE FLIP-FLOPS

WITH CLEAR

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLR low	6			6.5		6.5		ns
		CLK high or low	7			7		7		
t_{su}	Setup time before CLK $\uparrow$	Data	8.5			9.5		9.5		ns
		CLR inactive	4			4		4		
t_h	Hold time, data after CLK $\uparrow$		-0.5			0		0		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLR low	5			5		5		ns
		CLK high or low	5			5		5		
t_{su}	Setup time before CLK $\uparrow$	Data	5			6		6		ns
		CLR inactive	3			3		3		
t_h	Hold time, data after CLK $\uparrow$		0			0		0		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLR low	5			5		5		ns
		CLK high or low	5			5		5		
t_{su}	Setup time before CLK $\uparrow$	Data	4.5			4.5		4.5		ns
		CLR inactive	2.5			2.5		2.5		
t_h	Hold time, data after CLK $\uparrow$		0.5			0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$	55	115		50		50		MHz
			$C_L = 50\text{ pF}$	45	90		40		40		
t_{pd}^*	CLR	Q	$C_L = 15\text{ pF}$		6.3	17.3	1	19.5	1	19.5	ns
	CLK				8.4	17.1	1	19	1	19	
t_{pd}	CLR	Q	$C_L = 50\text{ pF}$		8.2	21.9	1	23.5	1	23.5	ns
	CLK				10.8	20.6	1	23	1	23	
$t_{sk(o)}^\dagger$						2				2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

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SN54LV174A, SN74LV174A HEX D-TYPE FLIP-FLOPS WITH CLEAR

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}^*$	95	170		80		80		MHz
			$C_L = 50 \text{ pF}$	55	130		50		50		
t_{pd}^*	$\overline{\text{CLR}}$	Q	$C_L = 15 \text{ pF}$	4.5	11.4		1	13.5	1	13.5	ns
	CLK			5.8	11		1	13	1	13	
t_{pd}	$\overline{\text{CLR}}$	Q	$C_L = 50 \text{ pF}$	6	14.9		1	17	1	17	ns
	CLK			7.5	14.5		1	16.5	1	16.5	
$t_{\text{sk(o)}}^\dagger$				1.5					1.5		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV174A		SN74LV174A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}^*$	130	240		110		110		MHz
			$C_L = 50 \text{ pF}$	90	180		80		80		
t_{pd}^*	$\overline{\text{CLR}}$	Q	$C_L = 15 \text{ pF}$	3	7.6		1	9	1	9	ns
	CLK			4.1	7.2		1	8.5	1	8.5	
t_{pd}	$\overline{\text{CLR}}$	Q	$C_L = 50 \text{ pF}$	4.2	9.6		1	11	1	11	ns
	CLK			5.5	9.2		1	10.5	1	10.5	
$t_{\text{sk(o)}}^\dagger$				1					1		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

noise characteristics, $V_{CC} = 3.3 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV174A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.34	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.3	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.02		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage		0.99		V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$		3.3 V	14	pF
				5 V	15.1	

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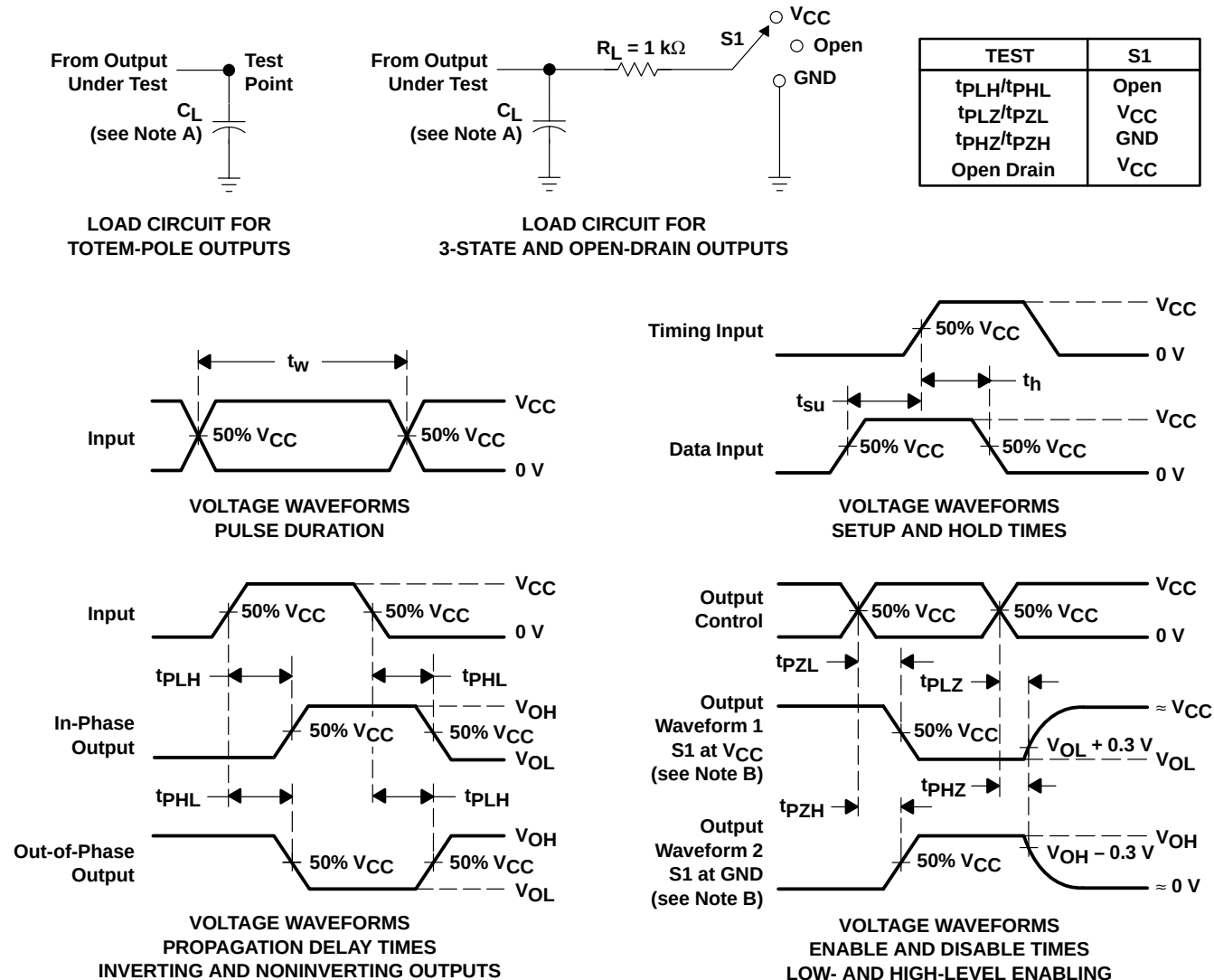


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SN54LV174A, SN74LV174A HEX D-TYPE FLIP-FLOPS WITH CLEAR

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SCLS400A – APRIL 1998 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 $< 0.8\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 $> 2\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Contain Four Flip-Flops With Double-Rail Outputs**
- **Applications Include:**
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

The 'LV175A devices are quadruple D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

These devices have a direct clear ($\overline{\text{CLR}}$) input and feature complementary outputs from each flip-flop.

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse.

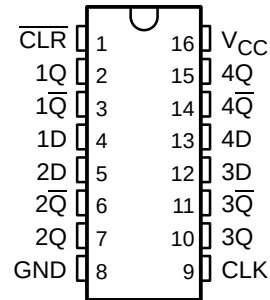
Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

The SN54LV175A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV175A is characterized for operation from -40°C to 85°C .

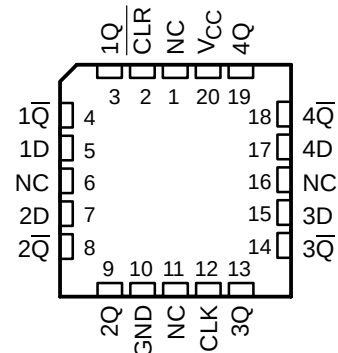
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUTS	
$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	X	X	L	H
H	$\uparrow$	H	H	L
H	$\uparrow$	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

SN54LV175A ... J OR W PACKAGE
SN74LV175A ... D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV175A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

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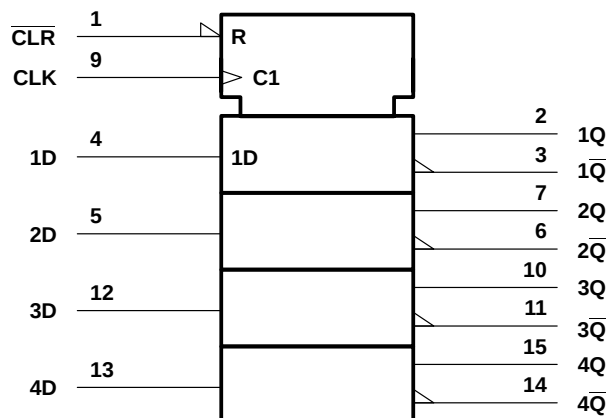
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SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

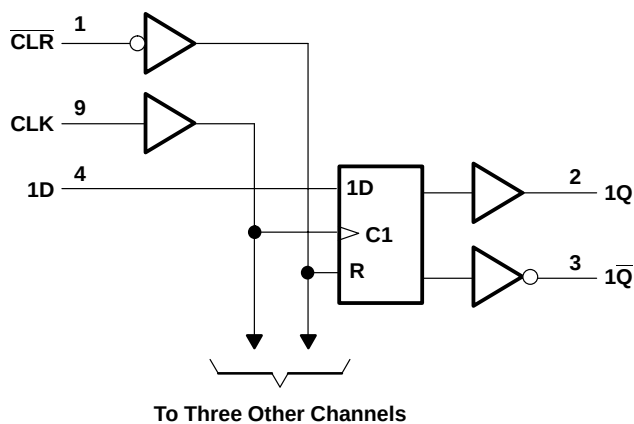
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SCLS400A – APRIL 1998 – REVISED JUNE 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
NS package	111°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV175A		SN74LV175A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−6		−6		
		V _{CC} = 4.5 V to 5.5 V	−12		−12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	6		6		
		V _{CC} = 4.5 V to 5.5 V	12		12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV175A			SN74LV175A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -6 mA	3 V	2.48			2.48			
	I _{OH} = -12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V							pF
		5 V							

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		SN54LV175A		SN74LV175A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLR low						ns	
		CLK high or low							
t _{su}	Setup time before CLK↑	Data						ns	
		CLR inactive							
t _h	Hold time, data after CLK↑							ns	

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54LV175A		SN74LV175A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CL _R low						ns
		CLK high or low						
t _{su}	Setup time before CLK↑	Data						ns
		CL _R inactive						
t _h	Hold time, data after CLK↑							ns



SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV175A		SN74LV175A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLR low							ns
		CLK high or low							
t_{su}	Setup time before CLK $\uparrow$	Data							ns
		CLR inactive							
t_h	Hold time, data after CLK $\uparrow$								ns

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV175A		SN74LV175A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$								MHz
			$C_L = 50\text{ pF}$								
t_{pd}^*	$\overline{\text{CLR}}$	Any	$C_L = 15\text{ pF}$								ns
	CLK	Any									
t_{pd}	$\overline{\text{CLR}}$	Any	$C_L = 50\text{ pF}$								ns
	CLK	Any									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV175A		SN74LV175A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$								MHz
			$C_L = 50\text{ pF}$								
t_{pd}^*	$\overline{\text{CLR}}$	Any	$C_L = 15\text{ pF}$								ns
	CLK	Any									
t_{pd}	$\overline{\text{CLR}}$	Any	$C_L = 50\text{ pF}$								ns
	CLK	Any									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV175A		SN74LV175A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$								MHz
			$C_L = 50\text{ pF}$								
t_{pd}^*	$\overline{\text{CLR}}$	Any	$C_L = 15\text{ pF}$								ns
	CLK	Any									
t_{pd}	$\overline{\text{CLR}}$	Any	$C_L = 50\text{ pF}$								ns
	CLK	Any									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW



SN54LV175A, SN74LV175A
QUADRUPLE D-TYPE FLIP-FLOPS
WITH CLEAR

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noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

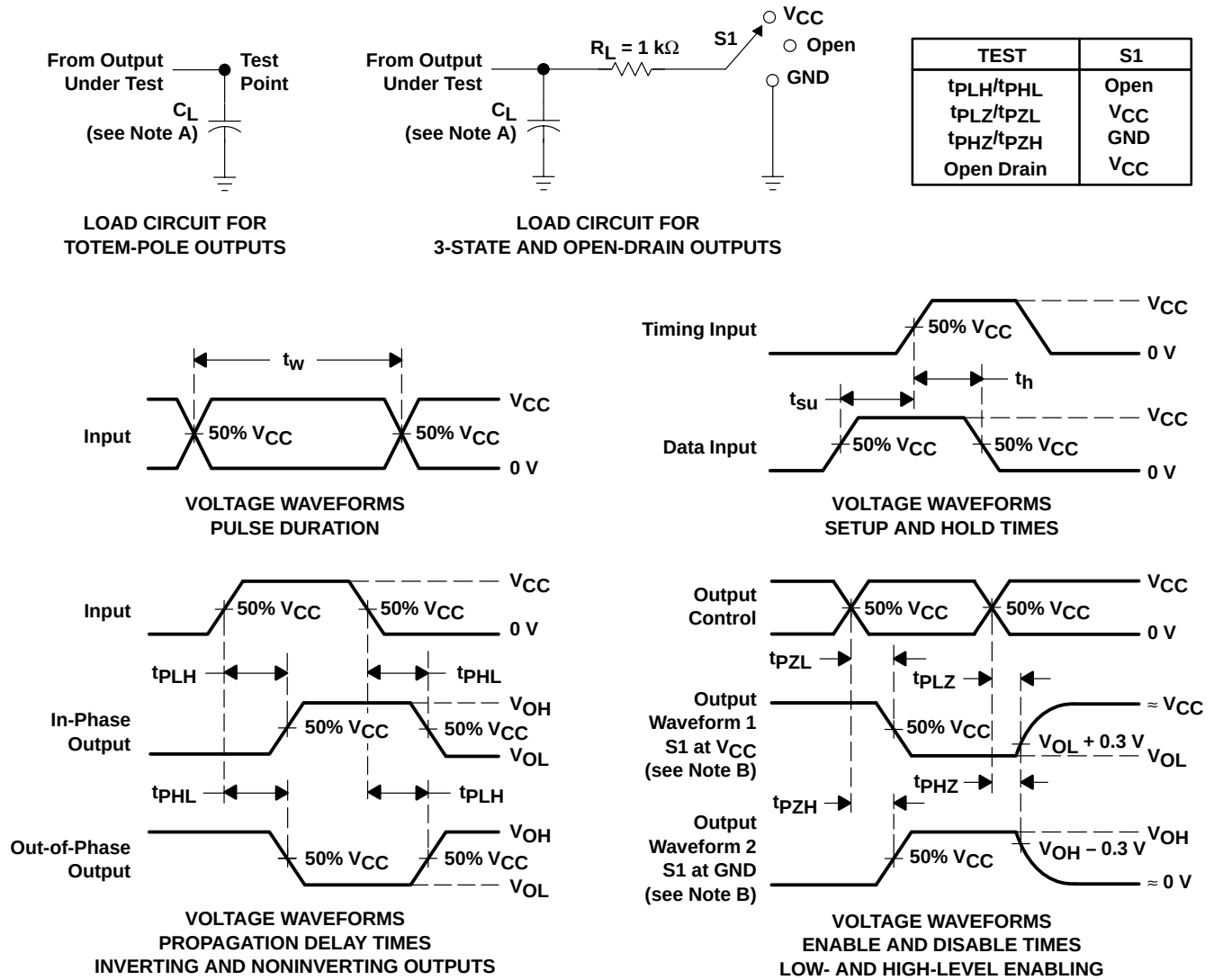
PARAMETER	SN74LV175A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$ High-level dynamic input voltage				V
$V_{IL(D)}$ Low-level dynamic input voltage				V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$		pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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SN54LV240A, SN74LV240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

description

These octal buffers/drivers are designed for 2-V to 5.5-V V_{CC} operation.

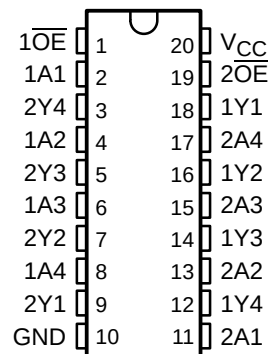
The 'LV240A devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

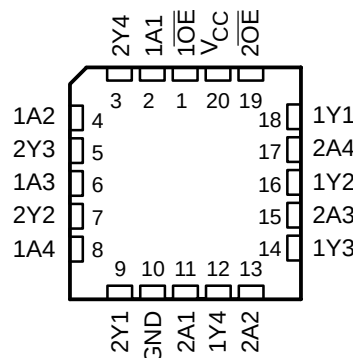
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV240A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV240A is characterized for operation from -40°C to 85°C .

SN54LV240A . . . J OR W PACKAGE
SN74LV240A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV240A . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	L
L	L	H
H	X	Z

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 **TEXAS
INSTRUMENTS**

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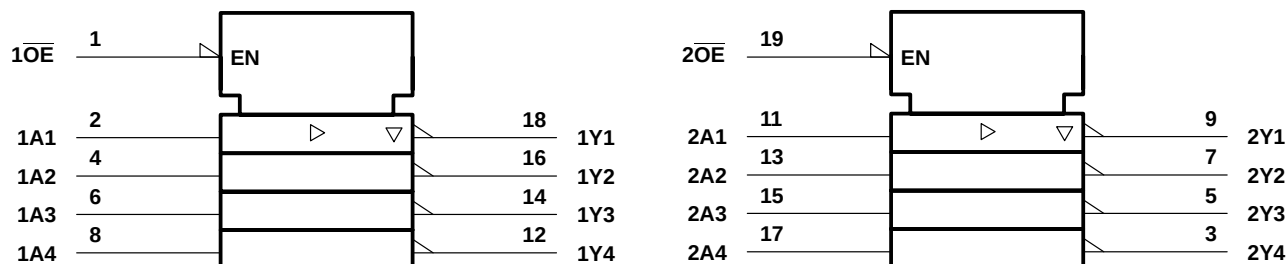
SN54LV240A, SN74LV240A

OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

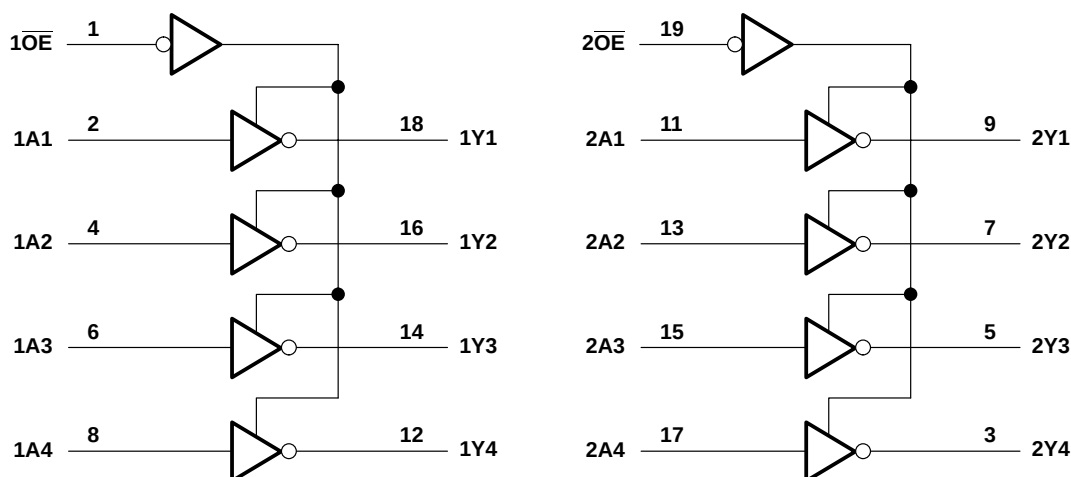
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range applied in high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DGV package	146°C/W
DW package	97°C/W
NS package	100°C/W
PW package	128°C/W

Storage temperature range, T_{stg} –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV240A, SN74LV240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

			SN54LV240A		SN74LV240A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	0	V _{CC}	V
		3-state	0	5.5	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−8		−8		
		V _{CC} = 4.5 V to 5.5 V	−16		−16		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	8		8		
		V _{CC} = 4.5 V to 5.5 V	16		16		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LV240A, SN74LV240A

OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV240A			SN74LV240A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -8 mA	3 V	2.48			2.48			
	I _{OH} = -16 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 8 mA	3 V	0.44			0.44			
	I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	20			20			μA
C _i	V _I = V _{CC} or GND	3.3 V	2.3			2.3			pF
		5 V	2.3			2.3			

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV240A		SN74LV240A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF	6.3	11.6		1	14	1	14	ns
t _{en} *	OE	Y		8.5	14.6		1	17	1	17	
t _{dis} *	OE	Y		9.7	14.1		1	16	1	16	
t _{pd}	A	Y	C _L = 50 pF	8.2	14.4		1	17	1	17	ns
t _{en}	OE	Y		10.3	17.8		1	21	1	21	
t _{dis}	OE	Y		14.2	19.2		1	21	1	21	
t _{sk(o)} †					2					2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV240A		SN74LV240A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF	4.6	7.5		1	9	1	9	ns
t _{en} *	OE	Y		6.2	10.6		1	12.5	1	12.5	
t _{dis} *	OE	Y		8.3	12.5		1	13.5	1	13.5	
t _{pd}	A	Y	C _L = 50 pF	5.9	11		1	12.5	1	12.5	ns
t _{en}	OE	Y		7.5	14.1		1	16	1	16	
t _{dis}	OE	Y		11.8	15		1	17	1	17	
t _{sk(o)} †					1.5					1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LV240A, SN74LV240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV240A		SN74LV240A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$	3.4	5.5		1	6.5	1	6.5	ns
t_{en}^*	$\overline{OE}$	Y		4.6	7.3		1	8.5	1	8.5	
t_{dis}^*	$\overline{OE}$	Y		7.4	12.2		1	13.5	1	13.5	
t_{pd}	A	Y	$C_L = 50\text{ pF}$	4.4	7.5		1	8.5	1	8.5	ns
t_{en}	$\overline{OE}$	Y		5.6	9.3		1	10.5	1	10.5	
t_{dis}	$\overline{OE}$	Y		9.7	14.2		1	15.5	1	15.5	
$t_{sk(o)}^\dagger$						1				1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV240A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.56		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.49		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.82		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

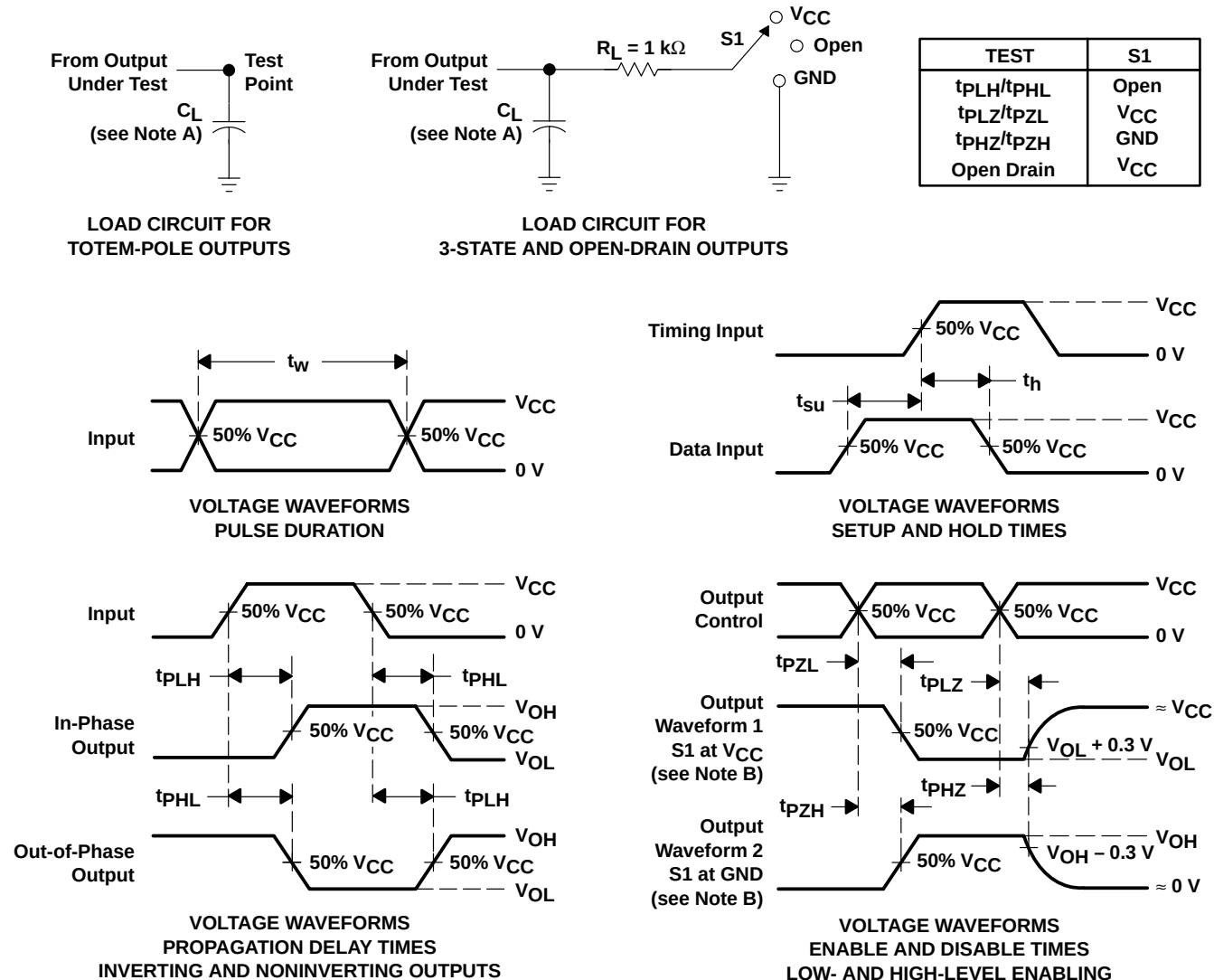
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$		3.3 V	14	pF
				5 V	16	

SN54LV240A, SN74LV240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV244A, SN74LV244A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS383B – SEPTEMBER 1997 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

These octal buffers/line drivers are designed for 2-V to 5.5-V V_{CC} operation.

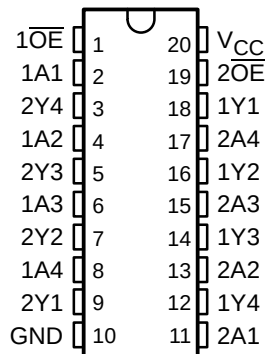
The 'LV244A devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

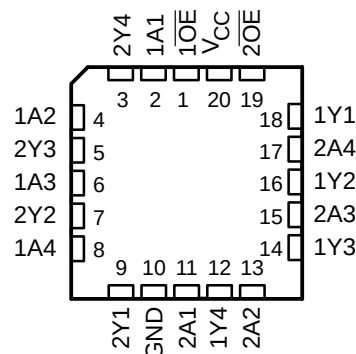
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV244A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV244A is characterized for operation from -40°C to 85°C .

SN54LV244A . . . J OR W PACKAGE
SN74LV244A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV244A . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Z

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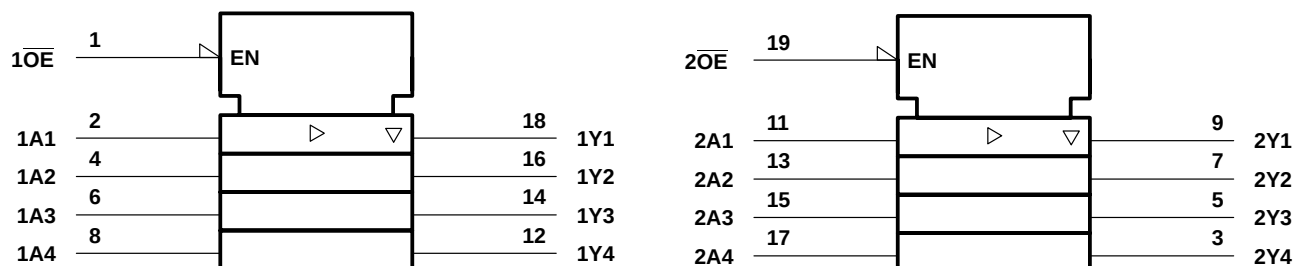
SN54LV244A, SN74LV244A

OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

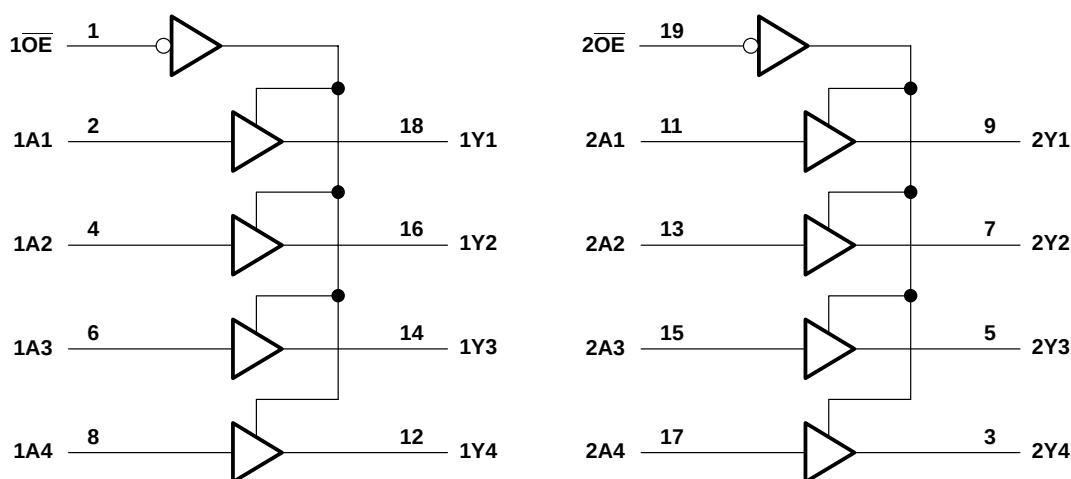
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range applied in high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3):	
DB package	115°C/W
DGV package	146°C/W
DW package	97°C/W
NS package	100°C/W
PW package	128°C/W

Storage temperature range, T_{stg} –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV244A, SN74LV244A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		SN54LV244A		SN74LV244A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	High or low state	0 V _{CC}	0 V _{CC}		V
		3-state	0 5.5	0 5.5		
I _{OH}	High-level output current	V _{CC} = 2 V	–50	–50		μA
		V _{CC} = 2.3 V to 2.7 V	–2	–2		mA
		V _{CC} = 3 V to 3.6 V	–8	–8		
		V _{CC} = 4.5 V to 5.5 V	–16	–16		
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50		μA
		V _{CC} = 2.3 V to 2.7 V	2	2		mA
		V _{CC} = 3 V to 3.6 V	8	8		
		V _{CC} = 4.5 V to 5.5 V	16	16		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0 200	0 200		ns/V
		V _{CC} = 3 V to 3.6 V	0 100	0 100		
		V _{CC} = 4.5 V to 5.5 V	0 20	0 20		
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LV244A, SN74LV244A

OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV244A			SN74LV244A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -8 mA	3 V	2.48			2.48			
	I _{OH} = -16 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 8 mA	3 V	0.44			0.44			
	I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	20			20			μA
C _i	V _I = V _{CC} or GND	3.3 V	2.3			2.3			pF
		5 V	2.3			2.3			

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV244A		SN74LV244A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF	7.5	12.5		1	15	1	15	ns
t _{en} *	OE	Y		8.9	14.6		1	17	1	17	
t _{dis} *	OE	Y		9.1	14.1		1	16	1	16	
t _{pd}	A	Y	C _L = 50 pF	9.5	15.3		1	18	1	18	ns
t _{en}	OE	Y		10.8	17.8		1	21	1	21	
t _{dis}	OE	Y		13.4	19.2		1	21	1	21	
t _{sk(o)} †					2					2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV244A		SN74LV244A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF	5.4	8.4		1	10	1	10	ns
t _{en} *	OE	Y		6.3	10.6		1	12.5	1	12.5	
t _{dis} *	OE	Y		7.6	11		1	13	1	13	
t _{pd}	A	Y	C _L = 50 pF	6.8	11.9		1	13.5	1	13.5	ns
t _{en}	OE	Y		7.8	14.1		1	16	1	16	
t _{dis}	OE	Y		11	16		1	18	1	18	
t _{sk(o)} †					1.5					1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

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SN54LV244A, SN74LV244A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV244A		SN74LV244A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$	3.9	5.5		1	6.5	1	6.5	ns
t_{en}^*	$\overline{OE}$	Y		4.5	7.3		1	8.5	1	8.5	
t_{dis}^*	$\overline{OE}$	Y		6.5	12.2		1	13.5	1	13.5	
t_{pd}	A	Y	$C_L = 50\text{ pF}$	4.9	7.5		1	8.5	1	8.5	ns
t_{en}	$\overline{OE}$	Y		5.6	9.3		1	10.5	1	10.5	
t_{dis}	$\overline{OE}$	Y		8.8	14.2		1	15.5	1	15.5	
$t_{sk(o)}^\dagger$					1					1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV244A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.55		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.5		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

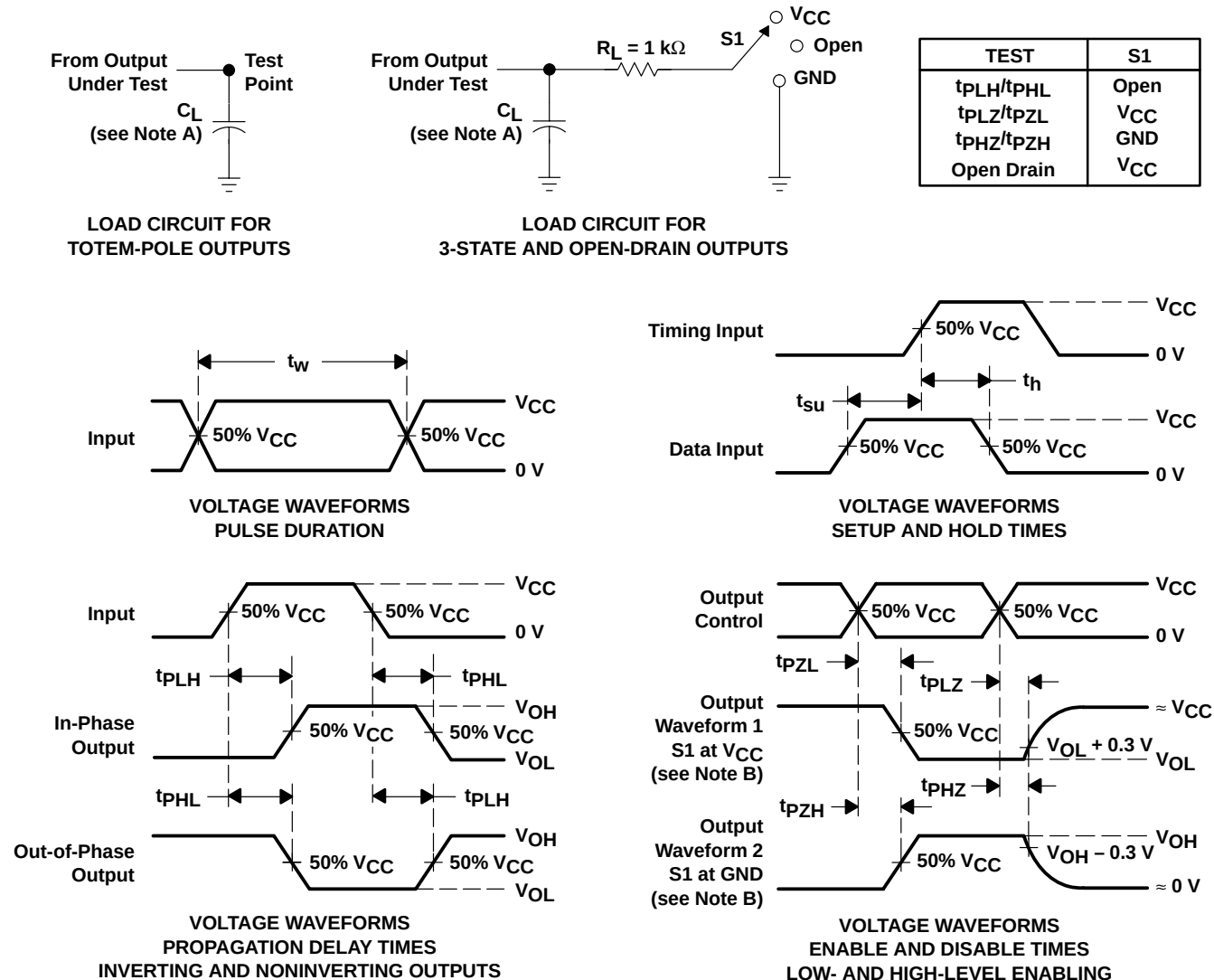
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	14	pF
			5 V	16	

SN54LV244A, SN74LV244A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV245A, SN74LV245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCLS382C – SEPTEMBER 1997 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

description

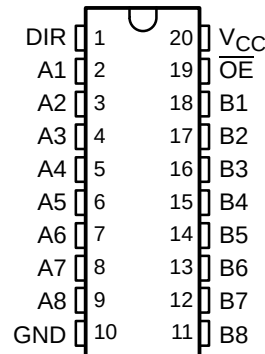
These octal bus transceivers are designed for 2-V to 5.5-V V_{CC} operation.

The 'LV245A devices are designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

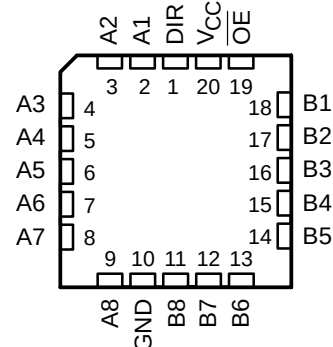
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV245A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV245A is characterized for operation from -40°C to 85°C .

SN54LV245A . . . J OR W PACKAGE
SN74LV245A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV245A . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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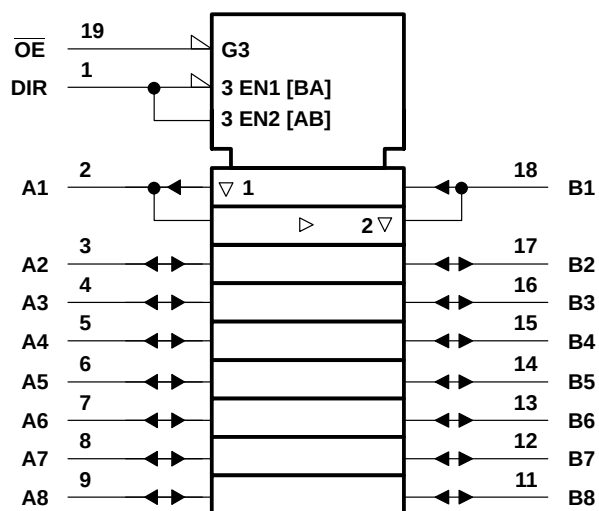
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SN54LV245A, SN74LV245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

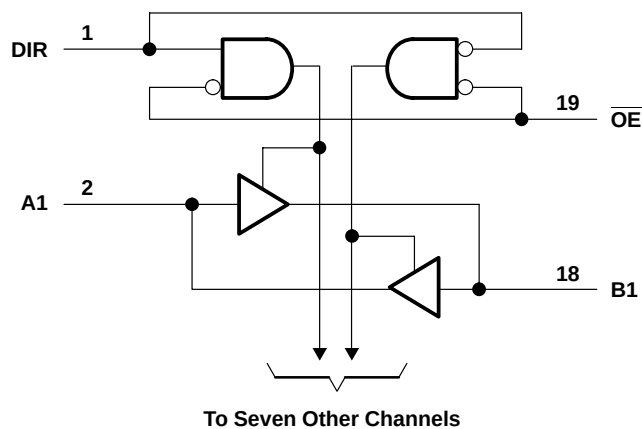
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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Supply voltage range, V_{CC}		-0.5 V to 7 V
Input voltage range, V_I : Except I/O ports (see Note 1)		-0.5 V to 7 V
I/O ports (see Notes 1 and 2)		-0.5 V to $V_{CC} + 0.5$ V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2)		-0.5 V to $V_{CC} + 0.5$ V
Output voltage range applied in high-impedance or power-off state, V_O (see Note 1)		-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)		-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)		± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		± 35 mA
Continuous current through V_{CC} or GND		± 70 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package		115°C/W
DGV package		146°C/W
DW package		97°C/W
NS package		100°C/W
PW package		128°C/W
Storage temperature range, T_{Stg}		-65°C to 150°C

NOTES:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JEDEC 51.

SN54LV245A, SN74LV245A

OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

			SN54LV245A		SN74LV245A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	0	V _{CC}	V
		3-state	0	5.5	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−8		−8		
		V _{CC} = 4.5 V to 5.5 V	−16		−16		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	8		8		
		V _{CC} = 4.5 V to 5.5 V	16		16		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LV245A, SN74LV245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	SN54LV245A		SN74LV245A		UNIT
				MIN	TYP	MAX	MIN	
V _{OH}		I _{OH} = −50 μA	2 V to 5.5 V	V _{CC} −0.1		V _{CC} −0.1		V
		I _{OH} = −2 mA	2.3 V	2		2		
		I _{OH} = −8 mA	3 V	2.48		2.48		
		I _{OH} = −16 mA	4.5 V	3.8		3.8		
V _{OL}		I _{OL} = 50 μA	2 V to 5.5 V	0.1		0.1		V
		I _{OL} = 2 mA	2.3 V	0.4		0.4		
		I _{OL} = 8 mA	3 V	0.44		0.44		
		I _{OL} = 16 mA	4.5 V	0.55		0.55		
I _I		V _I = V _{CC} or GND	5.5 V	±1		±1		μA
I _{OZ}		V _O = V _{CC} or GND	5.5 V	±5		±5		μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V	20		20		μA
I _{off}		V _I or V _O = 0 to 5.5 V	0 V	5		5		μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	2.4		2.4		pF
			5 V	2.4		2.4		
C _{io}	A or B port	V _O = V _{CC} or GND	3.3 V	5.4		5.4		pF
			5 V	5.4		5.4		

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV245A		SN74LV245A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	B or A	C _L = 15 pF	8.3	13		1	15	1	15	ns
t _{en} *	$\overline{\text{OE}}$	A or B		11.8	19.9		1	22	1	22	
t _{dis} *	$\overline{\text{OE}}$	A or B		11.8	18.1		1	20	1	20	
t _{pd}	A or B	B or A	C _L = 50 pF	11.2	15.9		1	18	1	18	ns
t _{en}	$\overline{\text{OE}}$	A or B		14.1	22.7		1	26	1	26	
t _{dis}	$\overline{\text{OE}}$	A or B		17.6	23.1		1	25	1	25	
t _{sk(o)} †				2						2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

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SN54LV245A, SN74LV245A

OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCLS382C – SEPTEMBER 1997 – REVISED JUNE 1998

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV245A		SN74LV245A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A or B	B or A	$C_L = 15\text{ pF}$	5.9	8.4		1	10	1	10	ns
t_{en}^*	$\overline{OE}$	A or B		8.2	13.2		1	15.5	1	15.5	
t_{dis}^*	$\overline{OE}$	A or B		9.6	16.5		1	19.5	1	19.5	
t_{pd}	A or B	B or A	$C_L = 50\text{ pF}$	7.9	11.9		1	13.5	1	13.5	ns
t_{en}	$\overline{OE}$	A or B		9.9	16.7		1	19	1	19	
t_{dis}	$\overline{OE}$	A or B		13.9	19.8		1	22	1	22	
$t_{sk(o)}^\dagger$					1.5					1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV245A		SN74LV245A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A or B	B or A	$C_L = 15\text{ pF}$	4.3	5.5		1	6.5	1	6.5	ns
t_{en}^*	$\overline{OE}$	A or B		5.7	8.5		1	10.6	1	10	
t_{dis}^*	$\overline{OE}$	A or B		7.8	12.8		1	14.7	1	14.2	
t_{pd}	A or B	B or A	$C_L = 50\text{ pF}$	5.6	7.5		1	8.5	1	8.5	ns
t_{en}	$\overline{OE}$	A or B		7	10.6		1	12	1	12	
t_{dis}	$\overline{OE}$	A or B		10.9	14.7		1	16	1	16	
$t_{sk(o)}^\dagger$					1					1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV245A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.45		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.45		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.94		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

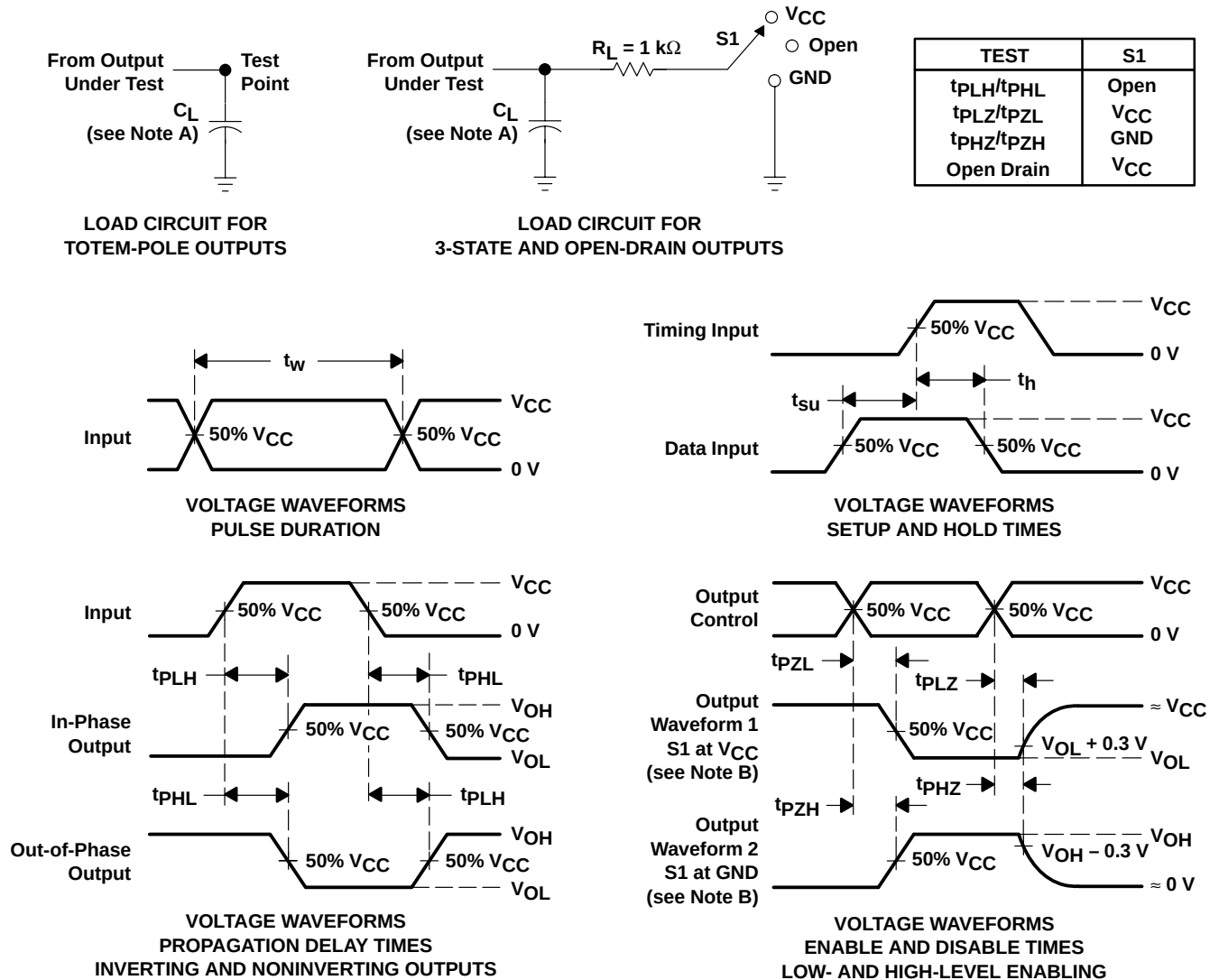
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	20	pF
				5 V	25	

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV273A, SN74LV273A OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCLS399 – APRIL 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 $< 0.8\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 $> 2\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

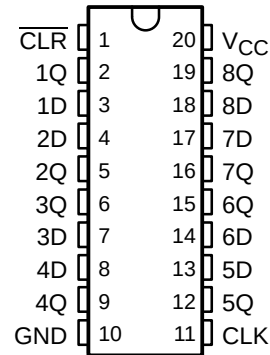
description

The 'LV273A devices are octal D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

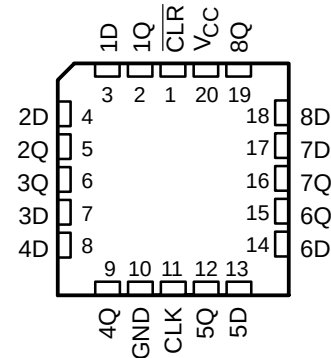
These devices are positive-edge-triggered flip-flops with direct clear (CLR) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN54LV273A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV273A is characterized for operation from -40°C to 85°C .

SN54LV273A . . . J OR W PACKAGE
SN74LV273A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV273A . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
CLR	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

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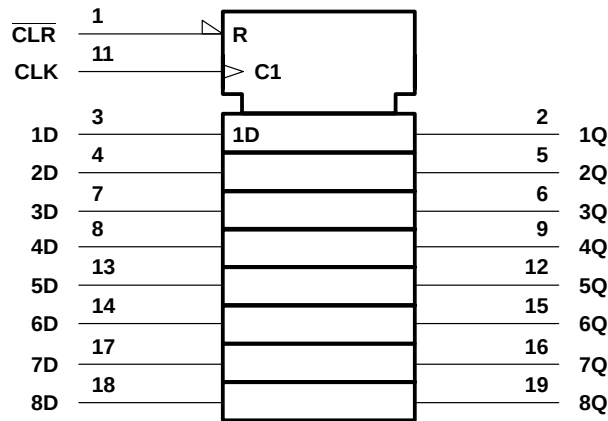
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PRODUCT PREVIEW

SN54LV273A, SN74LV273A
OCTAL D-TYPE FLIP-FLOPS
WITH CLEAR

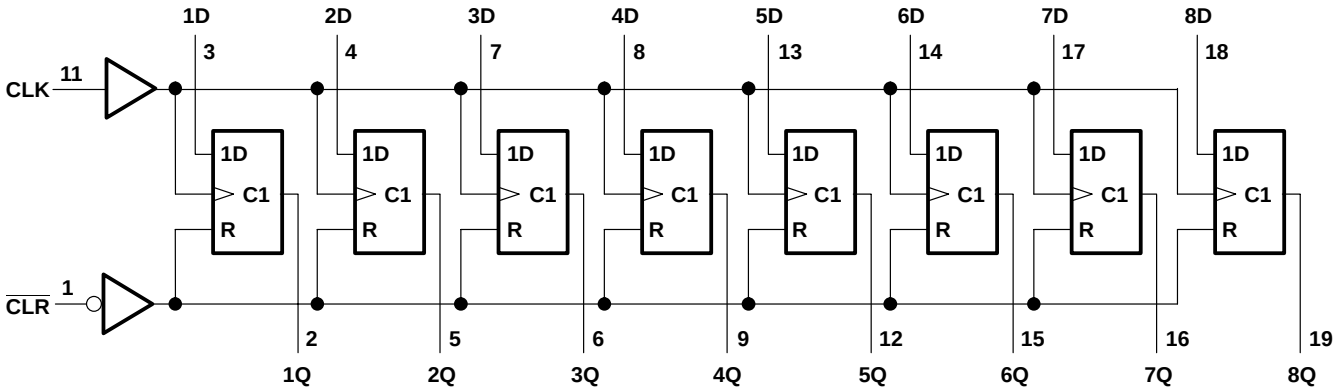
SCLS399 – APRIL 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

SN54LV273A, SN74LV273A

OCTAL D-TYPE FLIP-FLOPS

WITH CLEAR

SCLS399 – APRIL 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV273A			SN74LV273A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -6 mA	3 V	2.48			2.48			
	I _{OH} = -12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V							pF
		5 V							

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54LV273A		SN74LV273A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLR low						ns
		CLK high or low						
t _{su}	Setup time, data before CLK↑	Data						ns
		CLR inactive						
t _h	Hold time, data after CLK↑							ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		SN54LV273A		SN74LV273A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLR low						ns	
		CLK high or low							
t _{su}	Setup time, data before CLK↑	Data						ns	
		CLR inactive							
t _h	Hold time, data after CLK↑							ns	



SN54LV273A, SN74LV273A
OCTAL D-TYPE FLIP-FLOPS
WITH CLEAR

SCLS399 – APRIL 1998

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV273A		SN74LV273A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLR low						ns
		CLK high or low						
t_{su}	Setup time, data before CLK $\uparrow$	Data						ns
		CLR inactive						
t_h	Hold time, data after CLK $\uparrow$							ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV273A		SN74LV273A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$								MHz
			$C_L = 50\text{ pF}$								
t_{pd}^*	CLK	Q	$C_L = 15\text{ pF}$								ns
t_{PHL}^*	$\overline{\text{CLR}}$	Q									
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$								ns
t_{PHL}	$\overline{\text{CLR}}$	Q									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV273A		SN74LV273A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$								MHz
			$C_L = 50\text{ pF}$								
t_{pd}^*	CLK	Q	$C_L = 15\text{ pF}$								ns
t_{PHL}^*	$\overline{\text{CLR}}$	Q									
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$								ns
t_{PHL}	$\overline{\text{CLR}}$	Q									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV273A		SN74LV273A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$								MHz
			$C_L = 50\text{ pF}$								
t_{pd}^*	CLK	Q	$C_L = 15\text{ pF}$								ns
t_{PHL}^*	$\overline{\text{CLR}}$	Q									
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$								ns
t_{PHL}	$\overline{\text{CLR}}$	Q									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW



SN54LV273A, SN74LV273A
OCTAL D-TYPE FLIP-FLOPS
WITH CLEAR

SCLS399 – APRIL 1998

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

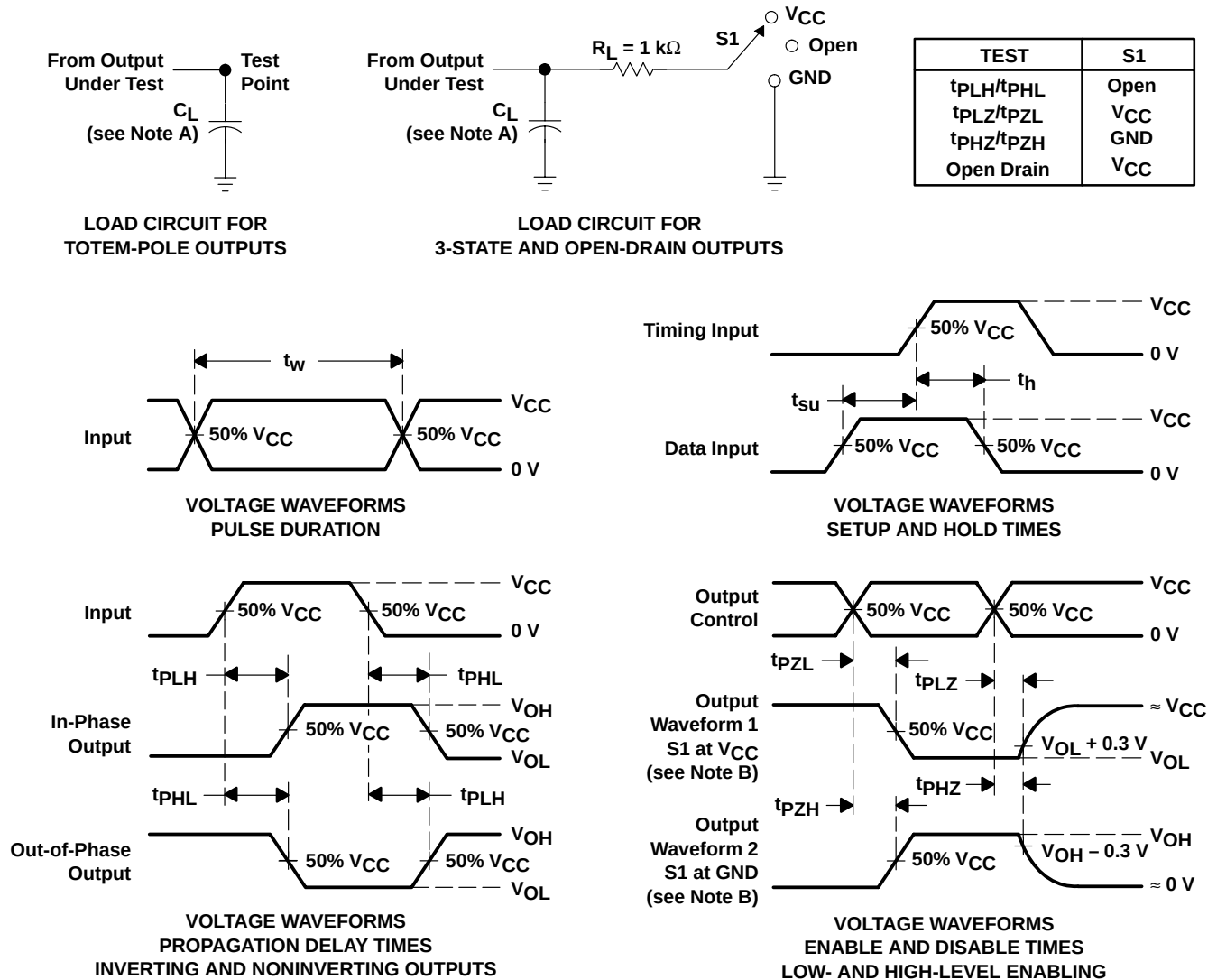
PARAMETER	SN74LV273A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$ High-level dynamic input voltage				V
$V_{IL(D)}$ Low-level dynamic input voltage				V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V		pF
		5 V		

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV367A, SN74LV367A HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS398A – APRIL 1998 – REVISED JULY 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **True Outputs**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

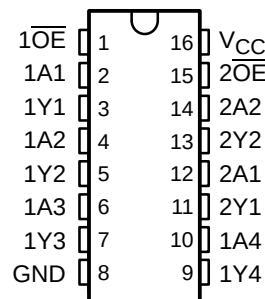
The 'LV367A devices are hex buffers and line drivers designed for 2-V to 5.5-V V_{CC} operation. These devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 'LV367A devices are organized as dual 4-line and 2-line buffers/drivers with active-low output-enable ($\overline{1OE}$ and $\overline{2OE}$) inputs. When $\overline{OE}$ is low, the device passes noninverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

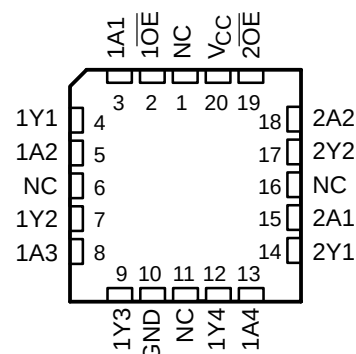
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV367A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV367A is characterized for operation from -40°C to 85°C .

SN54LV367A . . . J OR W PACKAGE
SN74LV367A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV367A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each buffer/driver)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
H	X	Z
L	H	H
L	L	L

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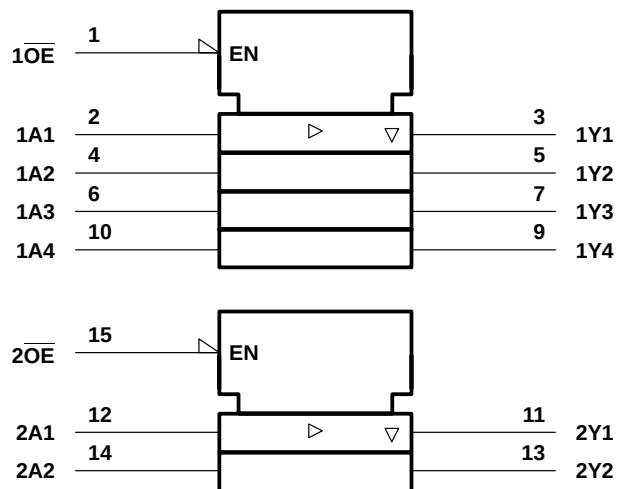
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SN54LV367A, SN74LV367A HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

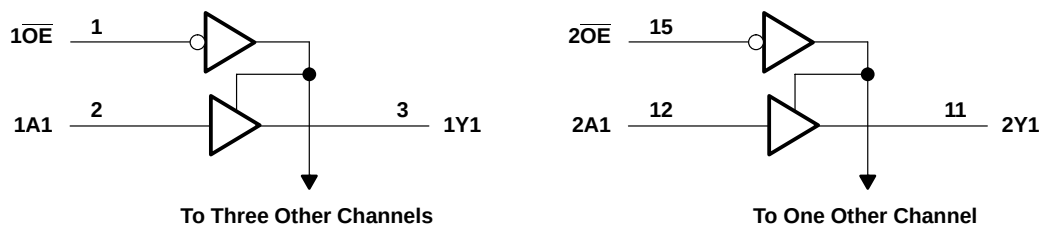
SCLS398A – APRIL 1998 – REVISED JULY 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

SN54LV367A, SN74LV367A
HEX BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS

SCLS398A – APRIL 1998 – REVISED JULY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range applied in high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
NS package	111°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

PRODUCT PREVIEW



SN54LV367A, SN74LV367A HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS398A – APRIL 1998 – REVISED JULY 1998

recommended operating conditions (see Note 4)

			SN54LV367A		SN74LV367A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	0	V _{CC}	V
		3-state	0	5.5	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−8		−8		
		V _{CC} = 4.5 V to 5.5 V	−16		−16		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	8		8		
		V _{CC} = 4.5 V to 5.5 V	16		16		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LV367A, SN74LV367A HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS398A – APRIL 1998 – REVISED JULY 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV367A			SN74LV367A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -8 mA	3 V	2.48			2.48			
	I _{OH} = -16 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 8 mA	3 V	0.44			0.44			
	I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V							pF
		5 V							

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV367A		SN74LV367A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF								ns
t _{en} *	$\overline{\text{OE}}$	Y									
t _{dis} *	$\overline{\text{OE}}$	Y									
t _{pd}	A	Y	C _L = 50 pF								ns
t _{en}	$\overline{\text{OE}}$	Y									
t _{dis}	$\overline{\text{OE}}$	Y									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV367A		SN74LV367A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF								ns
t _{en} *	$\overline{\text{OE}}$	Y									
t _{dis} *	$\overline{\text{OE}}$	Y									
t _{pd}	A	Y	C _L = 50 pF								ns
t _{en}	$\overline{\text{OE}}$	Y									
t _{dis}	$\overline{\text{OE}}$	Y									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.



SN54LV367A, SN74LV367A HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV367A		SN74LV367A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$								ns
t_{en}^*	$\overline{OE}$	Y									
t_{dis}^*	$\overline{OE}$	Y									
t_{pd}	A	Y	$C_L = 50\text{ pF}$								ns
t_{en}	$\overline{OE}$	Y									
t_{dis}	$\overline{OE}$	Y									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

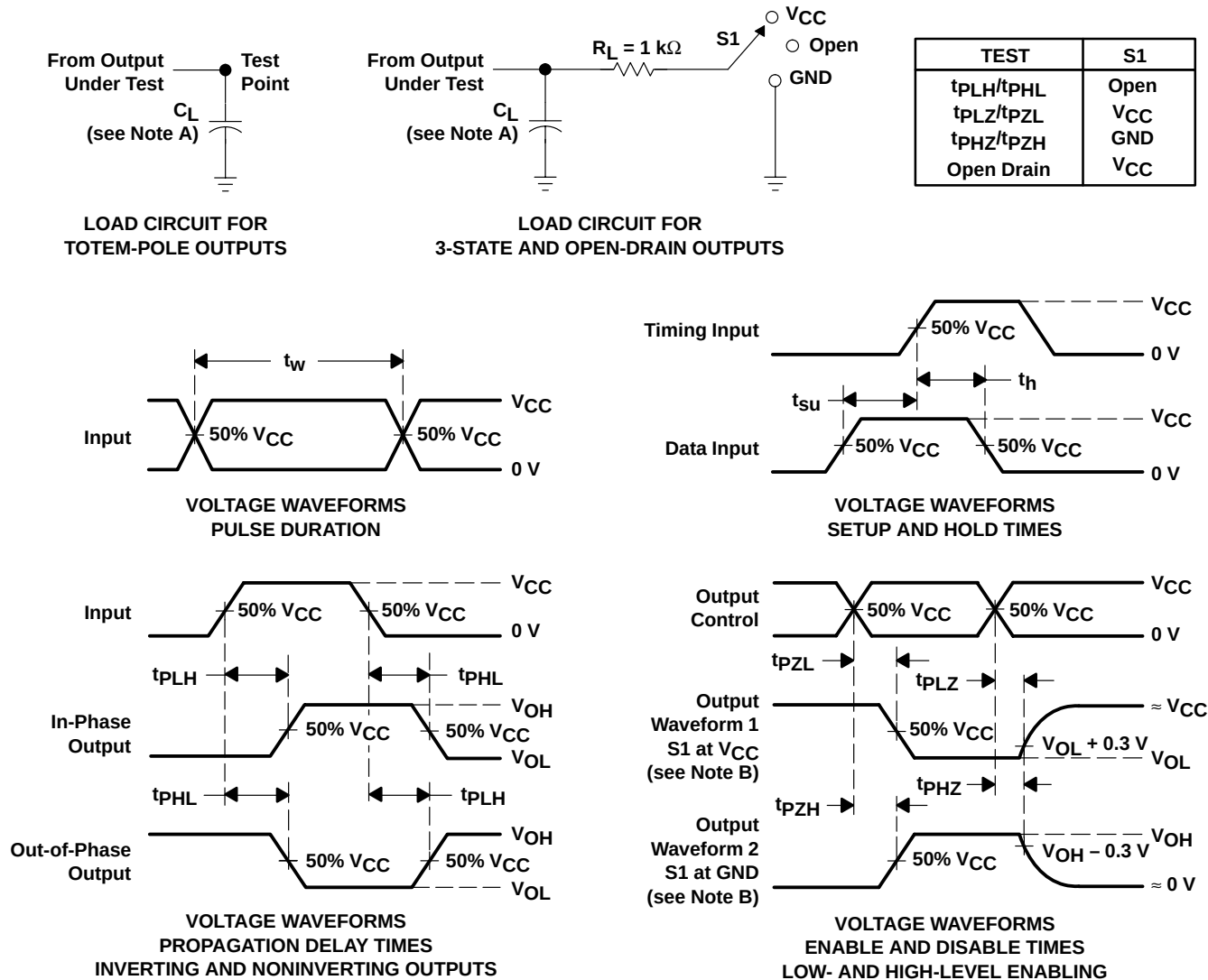
PARAMETER		SN74LV367A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage				V
$V_{IL(D)}$	Low-level dynamic input voltage				V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V		pF
		Outputs disabled				
		Outputs enabled		5 V		
		Outputs disabled				

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV368A, SN74LV368A HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS406A – APRIL 1998 – REVISED JULY 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Inverting Outputs**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

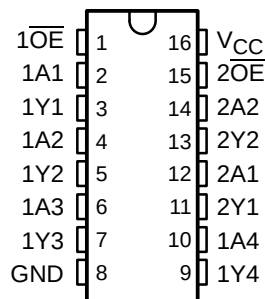
The 'LV368A devices are hex buffers and line drivers designed for 2-V to 5.5-V V_{CC} operation. These devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 'LV368A devices are organized as dual 4-line and 2-line buffers/drivers with active-low output-enable ($\overline{1OE}$ and $\overline{2OE}$) inputs. When $\overline{OE}$ is low, the device passes inverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

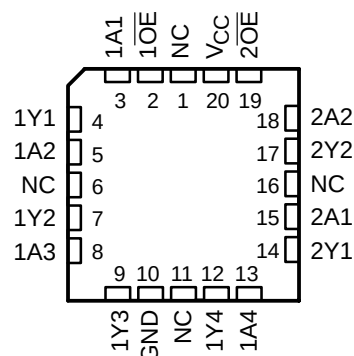
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN54LV368A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV368A is characterized for operation from -40°C to 85°C .

SN54LV368A . . . J OR W PACKAGE
SN74LV368A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV368A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each buffer/driver)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
H	X	Z
L	H	H
L	L	L

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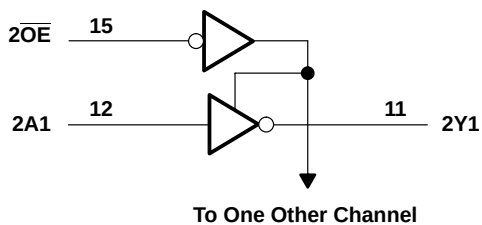
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The diagram illustrates the internal structure of the 74VHC163, showing two 4-bit binary counter blocks. Each block has an enable pin (EN) and a clock input. The top block is configured with inputs 1 (1OE), 2 (1A1), 4 (1A2), 6 (1A3), and 10 (1A4), and outputs 3 (1Y1), 5 (1Y2), 7 (1Y3), and 9 (1Y4). The bottom block is configured with inputs 15 (2OE), 12 (2A1), and 14 (2A2), and outputs 11 (2Y1) and 13 (2Y2).

Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

To Three Other Channels



To One Other Channel

Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

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Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2)	−0.5 V to $V_{CC} + 0.5$ V
Output voltage range applied in high-impedance or power-off state, V_O (see Note 1)	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	−20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	113°C/W
DGV package	180°C/W
DB package	131°C/W
NS package	111°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

NOTES:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV368A, SN74LV368A HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

			SN54LV368A		SN74LV368A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	0	V _{CC}	V
		3-state	0	5.5	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−8		−8		
		V _{CC} = 4.5 V to 5.5 V	−16		−16		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	8		8		
		V _{CC} = 4.5 V to 5.5 V	16		16		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LV368A, SN74LV368A HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS406A – APRIL 1998 – REVISED JULY 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV368A			SN74LV368A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -8 mA	3 V	2.48			2.48			
	I _{OH} = -16 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 8 mA	3 V	0.44			0.44			
	I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V							pF
		5 V							

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV368A		SN74LV368A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF								ns
t _{en} *	$\overline{\text{OE}}$	Y									
t _{dis} *	$\overline{\text{OE}}$	Y									
t _{pd}	A	Y	C _L = 50 pF								ns
t _{en}	$\overline{\text{OE}}$	Y									
t _{dis}	$\overline{\text{OE}}$	Y									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV368A		SN74LV368A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF								ns
t _{en} *	$\overline{\text{OE}}$	Y									
t _{dis} *	$\overline{\text{OE}}$	Y									
t _{pd}	A	Y	C _L = 50 pF								ns
t _{en}	$\overline{\text{OE}}$	Y									
t _{dis}	$\overline{\text{OE}}$	Y									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW



SN54LV368A, SN74LV368A HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS406A – APRIL 1998 – REVISED JULY 1998

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV368A		SN74LV368A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$								ns
t_{en}^*	$\overline{OE}$	Y									
t_{dis}^*	$\overline{OE}$	Y									
t_{pd}	A	Y	$C_L = 50\text{ pF}$								ns
t_{en}	$\overline{OE}$	Y									
t_{dis}	$\overline{OE}$	Y									

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

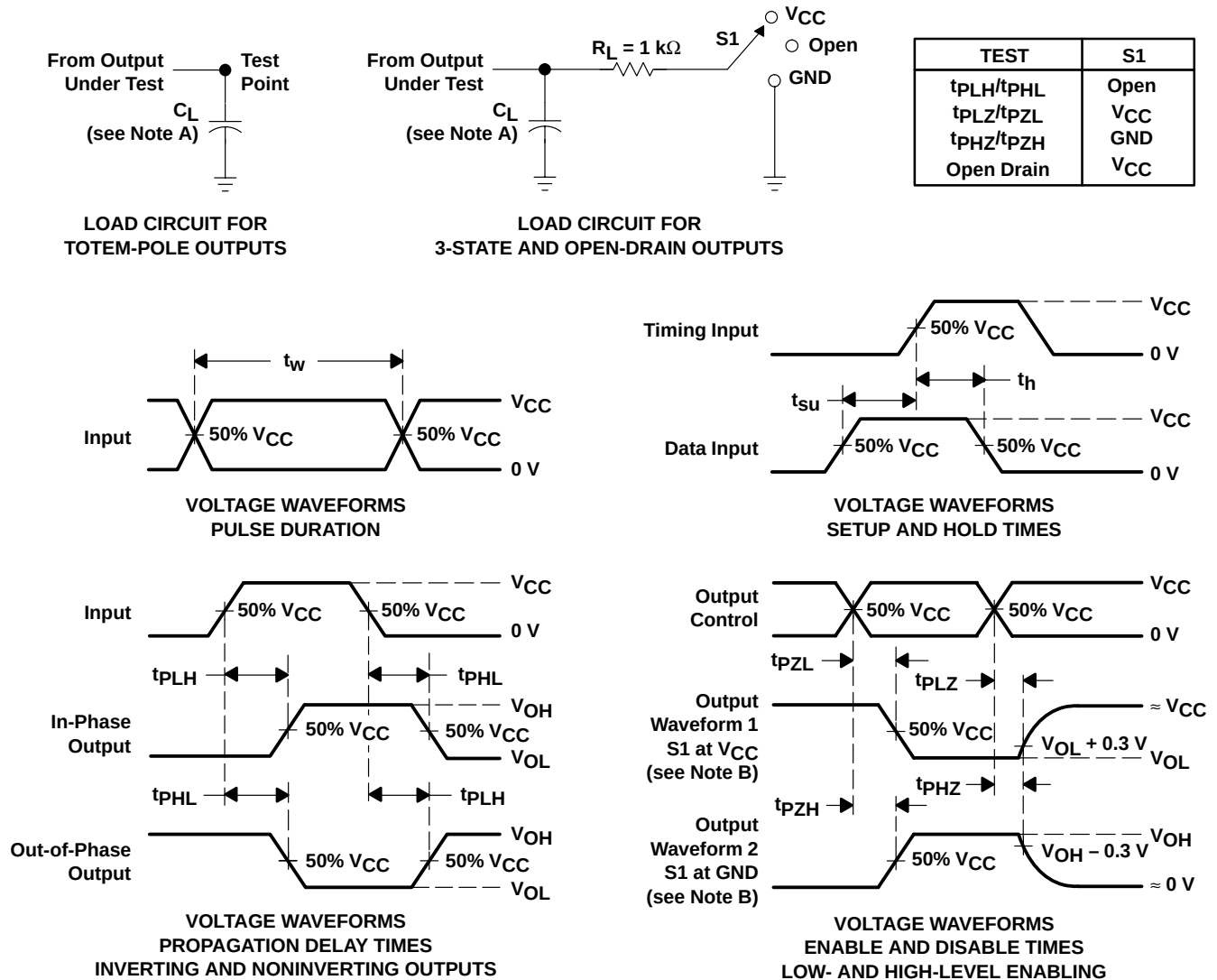
PARAMETER		SN74LV368A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage				V
$V_{IL(D)}$	Low-level dynamic input voltage				V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V		pF
		Outputs disabled				
		Outputs enabled		5 V		
		Outputs disabled				

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV373A, SN74LV373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS407A – APRIL 1998 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 $< 0.8\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 $> 2\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

The 'LV373A devices are octal transparent D-type latches designed for 2-V to 5.5-V V_{CC} operation.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

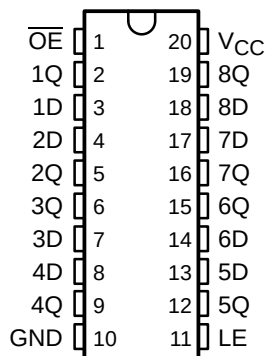
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

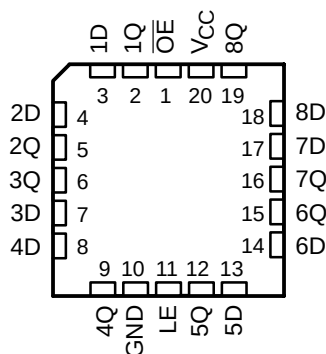
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV373A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV373A is characterized for operation from -40°C to 85°C .

SN54LV373A . . . J OR W PACKAGE
SN74LV373A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV373A . . . FK PACKAGE
(TOP VIEW)



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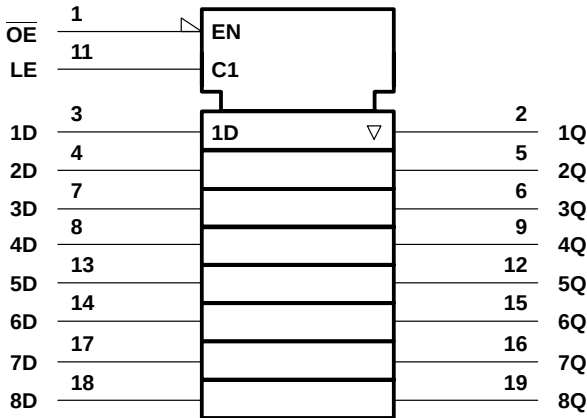
SN54LV373A, SN74LV373A
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCLS407A – APRIL 1998 – REVISED JUNE 1998

FUNCTION TABLE
(each latch)

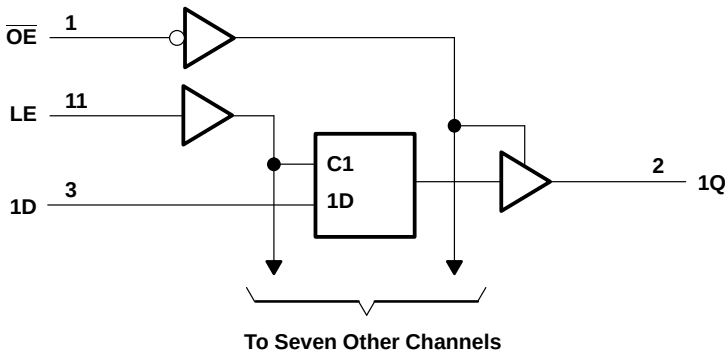
INPUTS			OUTPUT Q
OE	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	−20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3):	
DB package	115°C/W
DGV package	146°C/W
DW package	97°C/W
NS package	100°C/W
PW package	128°C/W
Storage temperature range, T_{Stg}	−65°C to 150°C

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JEDEC 51.

SN54LV373A, SN74LV373A

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

			SN54LV373A		SN74LV373A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	0	V _{CC}	V
		3-state	0	5.5	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−8		−8		
		V _{CC} = 4.5 V to 5.5 V	−16		−16		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	8		8		
		V _{CC} = 4.5 V to 5.5 V	16		16		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV373A			SN74LV373A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = −50 μA	2 V to 5.5 V	V _{CC} −0.1			V _{CC} −0.1			V
	I _{OH} = −2 mA	2.3 V	2			2			
	I _{OH} = −8 mA	3 V	2.48			2.48			
	I _{OH} = −16 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 8 mA	3 V	0.44			0.44			
	I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	2.9			2.9			pF

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SN54LV373A, SN74LV373A
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV373A		SN74LV373A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, LE high		6		6.5		6.5		ns
t_{SU}	Setup time, data before LE↓	High or low	4.5		5		5		ns
t_H	Hold time, data after LE↓	High or low	1.5		1.5		1.5		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV373A		SN74LV373A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, LE high		5		5		5		ns
t_{SU}	Setup time, data before LE↓	High or low	4		4		4		ns
t_H	Hold time, data after LE↓	High or low	1		1		1		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV373A		SN74LV373A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, LE high		5		5		5		ns
t_{SU}	Setup time, data before LE↓	High or low	4		4		4		ns
t_H	Hold time, data after LE↓	High or low	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV373A		SN74LV373A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	D	Q	$C_L = 15\text{ pF}$	8.3	15.2		1	17	1	17	ns
	LE	Q		9.1	15.7		1	19	1	19	
t_{en}^*	$\overline{OE}$	Q		8.9	15.8		1	19	1	19	
t_{dis}^*	$\overline{OE}$	Q		6.2	12.6		1	15	1	15	
t_{pd}	D	Q	$C_L = 50\text{ pF}$	10.4	18		1	21	1	21	ns
	LE	Q		11.1	18.6		1	22	1	22	
t_{en}	$\overline{OE}$	Q		10.9	18.8		1	22	1	22	
t_{dis}	$\overline{OE}$	Q		8.3	17.4		1	19	1	19	
$t_{sk(o)}^\dagger$					2					2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV373A		SN74LV373A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	D	Q	$C_L = 15\text{ pF}$	5.8	11.4		1	13.5	1	13.5	ns
	LE	Q		6.4	11		1	13	1	13	
t_{en}^*	$\overline{OE}$	Q		6.3	11.4		1	13.5	1	13.5	
t_{dis}^*	$\overline{OE}$	Q		4.7	10		1	12	1	12	
t_{pd}	D	Q	$C_L = 50\text{ pF}$	7.3	14.9		1	17	1	17	ns
	LE	Q		7.8	14.5		1	16.5	1	16.5	
t_{en}	$\overline{OE}$	Q		7.7	14.9		1	17	1	17	
t_{dis}	$\overline{OE}$	Q		6	13.2		1	15	1	15	
$t_{sk(o)}^\dagger$				1.5						1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV373A		SN74LV373A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	D	Q	$C_L = 15\text{ pF}$	4.1	7.2		1	8.5	1	8.5	ns
	LE	Q		4.5	7.2		1	8.5	1	8.5	
t_{en}^*	$\overline{OE}$	Q		4.5	8.1		1	9.5	1	9.5	
t_{dis}^*	$\overline{OE}$	Q		3.3	7.2		1	8.5	1	8.5	
t_{pd}	D	Q	$C_L = 50\text{ pF}$	5.1	9.2		1	10.5	1	10.5	ns
	LE	Q		5.5	9.2		1	10.5	1	10.5	
t_{en}	$\overline{OE}$	Q		5.5	10.1		1	11.5	1	11.5	
t_{dis}	$\overline{OE}$	Q		4	9.2		1	10.5	1	10.5	
$t_{sk(o)}^\dagger$				1						1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV373A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.58	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.56	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.86		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	17.4	pF
				5 V	19.5	

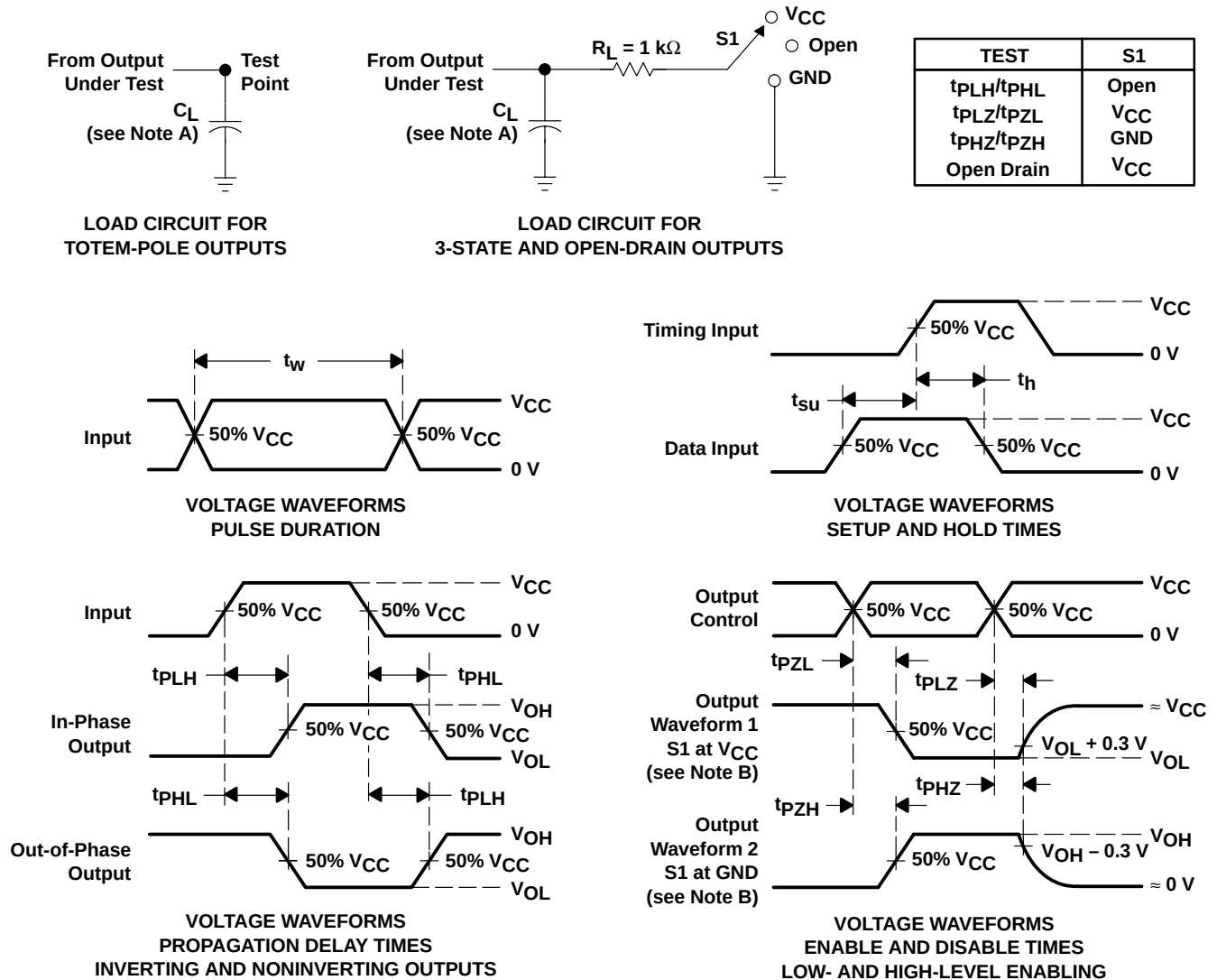
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SN54LV373A, SN74LV373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV374A, SN74LV374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 $< 0.8\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 $> 2\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

The 'LV374A devices are octal edge-triggered D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

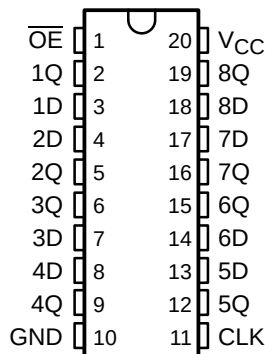
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

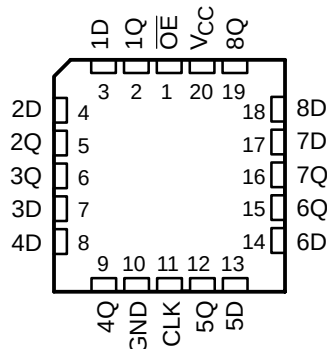
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV374A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV374A is characterized for operation from -40°C to 85°C .

SN54LV374A . . . J OR W PACKAGE
SN74LV374A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV374A . . . FK PACKAGE
(TOP VIEW)



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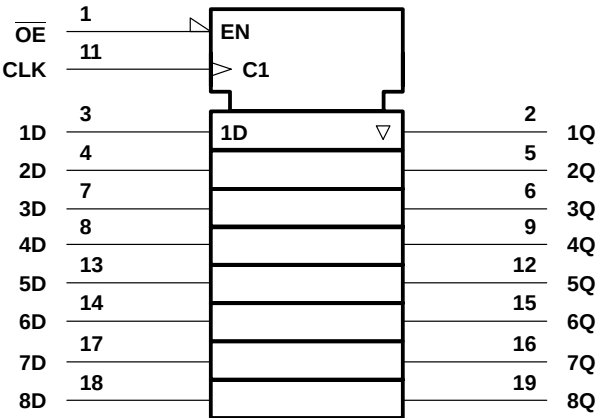
SN54LV374A, SN74LV374A
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each flip-flop)

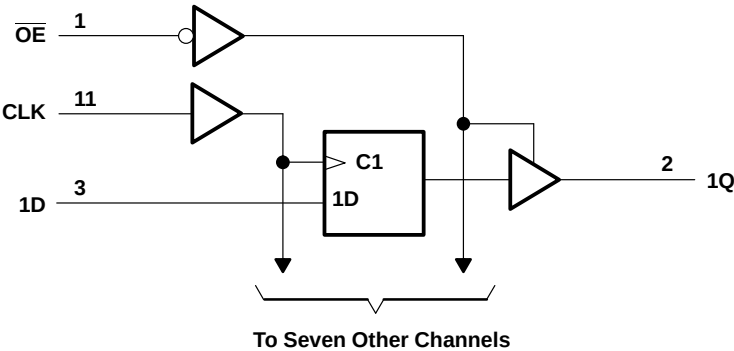
INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3):	
DB package	115°C/W
DGV package	146°C/W
DW package	97°C/W
NS package	100°C/W
PW package	128°C/W
Storage temperature range, T_{Stg}	−65°C to 150°C

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV374A, SN74LV374A

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

			SN54LV374A		SN74LV374A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	0	V _{CC}	V
		3-state	0	5.5	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−8		−8		
		V _{CC} = 4.5 V to 5.5 V	−16		−16		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	8		8		
		V _{CC} = 4.5 V to 5.5 V	16		16		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV374A			SN74LV374A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = −50 μA	2 V to 5.5 V	V _{CC} −0.1			V _{CC} −0.1			V
	I _{OH} = −2 mA	2.3 V	2			2			
	I _{OH} = −8 mA	3 V	2.48			2.48			
	I _{OH} = −16 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 8 mA	3 V	0.44			0.44			
	I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	2.9			2.9			pF

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SN54LV374A, SN74LV374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV374A		SN74LV374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, CLK high or low	6		7		7		ns
t_{SU}	Setup time, data before CLK $\uparrow$	5		5.5		5.5		ns
t_H	Hold time, data after CLK $\uparrow$	2.5		2.5		2.5		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV374A		SN74LV374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, CLK high or low	5		5.5		5.5		ns
t_{SU}	Setup time, data before CLK $\uparrow$	4		4		4		ns
t_H	Hold time, data after CLK $\uparrow$	2		2		2		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV374A		SN74LV374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, CLK high or low	5		5		5		ns
t_{SU}	Setup time, data before CLK $\uparrow$	3		3		3		ns
t_H	Hold time, data after CLK $\uparrow$	2		2		2		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV374A		SN74LV374A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$	60	105		50		50		MHz
			$C_L = 50\text{ pF}$	50	85		40		40		
t_{pd}^*	CLK	Q	$C_L = 15\text{ pF}$	9.7	16.3		1	19	1	19	ns
t_{en}^*	$\overline{OE}$	Q		8.9	15.9		1	19	1	19	
t_{dis}^*	$\overline{OE}$	Q		6.3	12.6		1	15	1	15	
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$	11.8	19.3		1	23	1	23	ns
t_{en}	$\overline{OE}$	Q		10.9	18.8		1	22	1	22	
t_{dis}	$\overline{OE}$	Q		8.2	17.3		1	19	1	19	
$t_{sk(o)}^\dagger$					2					2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

SN54LV374A, SN74LV374A

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

SCLS408A – APRIL 1998 – REVISED JUNE 1998

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV374A		SN74LV374A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$	80	150		70		70		MHz
			$C_L = 50\text{ pF}$	55	110		50		50		
t_{pd}^*	CLK	Q	$C_L = 15\text{ pF}$	6.8	12.7		1	15	1	15	ns
t_{en}^*	$\overline{\text{OE}}$	Q		6.3	11		1	13	1	13	
t_{dis}^*	$\overline{\text{OE}}$	Q		4.7	10.5		1	12.5	1	12.5	
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$	8.3	16.2		1	18.5	1	18.5	ns
t_{en}	$\overline{\text{OE}}$	Q		7.7	14.5		1	16.5	1	16.5	
t_{dis}	$\overline{\text{OE}}$	Q		5.9	14		1	16	1	16	
$t_{\text{sk(o)}}^\dagger$				1.5						1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV374A		SN74LV374A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$	130	205		110		110		MHz
			$C_L = 50\text{ pF}$	85	170		75		75		
t_{pd}^*	CLK	Q	$C_L = 15\text{ pF}$	4.9	8.1		1	9.5	1	9.5	ns
t_{en}^*	$\overline{\text{OE}}$	Q		4.6	7.6		1	9	1	9	
t_{dis}^*	$\overline{\text{OE}}$	Q		3.4	6.8		1	8	1	8	
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$	5.9	10.1		1	11.5	1	11.5	ns
t_{en}	$\overline{\text{OE}}$	Q		5.5	9.6		1	11	1	11	
t_{dis}	$\overline{\text{OE}}$	Q		4	8.8		1	10	1	10	
$t_{\text{sk(o)}}^\dagger$				1						1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV374A			UNIT
		MIN	TYP	MAX	
$V_{\text{OL(P)}}$	Quiet output, maximum dynamic V_{OL}		0.57	0.8	V
$V_{\text{OL(V)}}$	Quiet output, minimum dynamic V_{OL}		−0.53	−0.8	V
$V_{\text{OH(V)}}$	Quiet output, minimum dynamic V_{OH}		2.88		V
$V_{\text{IH(D)}}$	High-level dynamic input voltage	2.31			V
$V_{\text{IL(D)}}$	Low-level dynamic input voltage		0.99		V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	21.1	pF
				5 V	22.8	

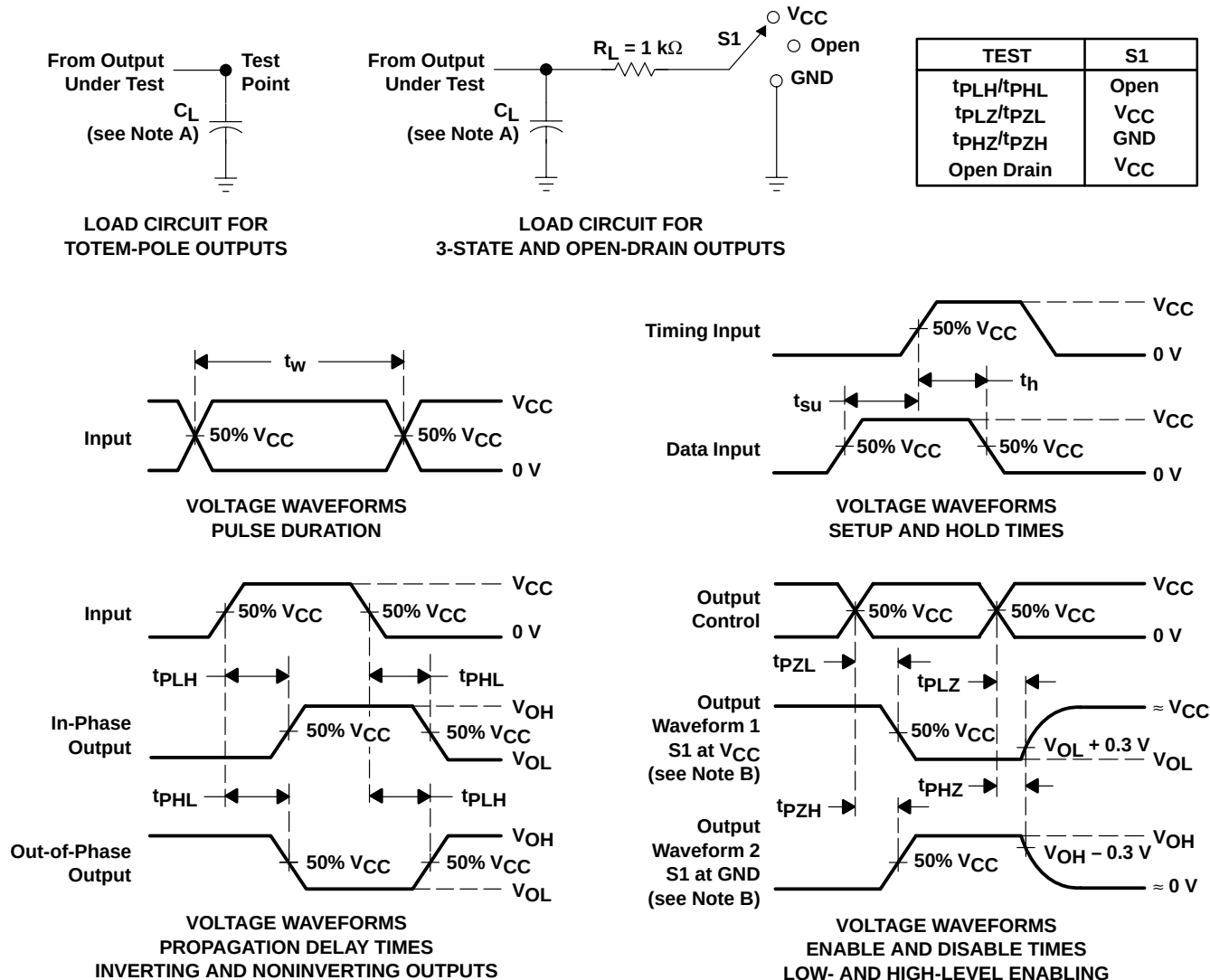
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SN54LV374A, SN74LV374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS408A – APRIL 1998 – REVISED JUNE 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV540A, SN74LV540A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS409A – APRIL 1998 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 $< 0.8\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 $> 2\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

The 'LV540A devices are octal buffers/drivers designed for 2-V to 5.5-V V_{CC} operation.

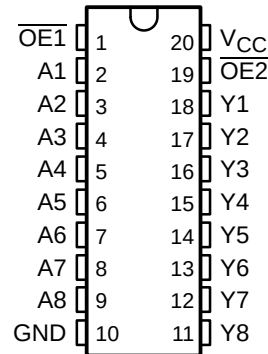
These devices are ideal for driving bus lines or buffer memory address registers. They feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

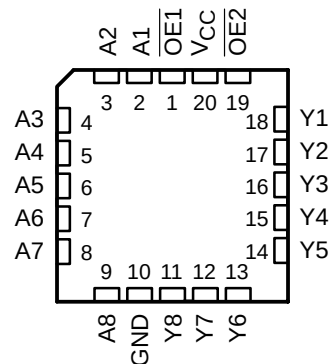
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV540A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV540A is characterized for operation from -40°C to 85°C .

SN54LV540A . . . J OR W PACKAGE
SN74LV540A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV540A . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer/driver)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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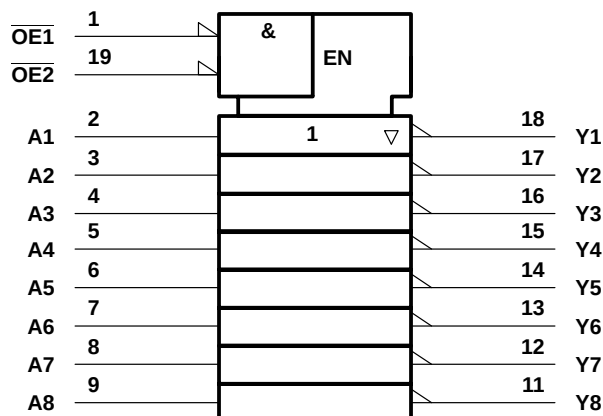
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PRODUCT PREVIEW

SN54LV540A, SN74LV540A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

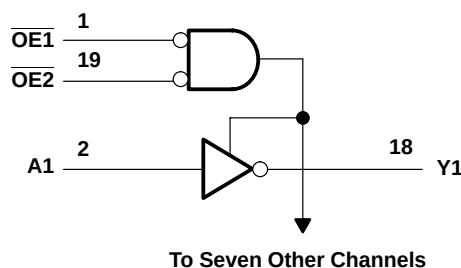
SCLS409A – APRIL 1998 – REVISED JUNE 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range applied in high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DGV package	146°C/W
DW package	97°C/W
NS package	100°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV540A, SN74LV540A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

			SN54LV540A		SN74LV540A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	0	V _{CC}	V
		3-state	0	5.5	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V		–50		–50	μA
		V _{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V _{CC} = 3 V to 3.6 V		–8		–8	
		V _{CC} = 4.5 V to 5.5 V		–16		–16	
I _{OL}	Low-level output current	V _{CC} = 2 V		50		50	μA
		V _{CC} = 2.3 V to 2.7 V		2		2	mA
		V _{CC} = 3 V to 3.6 V		8		8	
		V _{CC} = 4.5 V to 5.5 V		16		16	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW



SN54LV540A, SN74LV540A

OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCLS409A – APRIL 1998 – REVISED JUNE 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV540A			SN74LV540A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –8 mA	3 V	2.48			2.48			
	I _{OH} = –16 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 8 mA	3 V	0.44			0.44			
	I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V							pF
		5 V							

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV540A		SN74LV540A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF								ns
t _{en} *	OE	Y									
t _{dis} *	OE	Y									
t _{pd}	A	Y	C _L = 50 pF								ns
t _{en}	OE	Y									
t _{dis}	OE	Y									
t _{sk(o)} †											

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV540A		SN74LV540A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF								ns
t _{en} *	OE	Y									
t _{dis} *	OE	Y									
t _{pd}	A	Y	C _L = 50 pF								ns
t _{en}	OE	Y									
t _{dis}	OE	Y									
t _{sk(o)} †											

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction



SN54LV540A, SN74LV540A
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCLS409A – APRIL 1998 – REVISED JUNE 1998

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV540A		SN74LV540A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$								ns
t_{en}^*	$\overline{OE}$	Y									
t_{dis}^*	$\overline{OE}$	Y									
t_{pd}	A	Y	$C_L = 50\text{ pF}$								ns
t_{en}	$\overline{OE}$	Y									
t_{dis}	$\overline{OE}$	Y									
$t_{sk(o)}^\dagger$											

† Skew between any two outputs of the same package switching in the same direction

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV540A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage				V
$V_{IL(D)}$	Low-level dynamic input voltage				V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V		pF
		Outputs disabled				
		Outputs enabled		5 V		
		Outputs disabled				

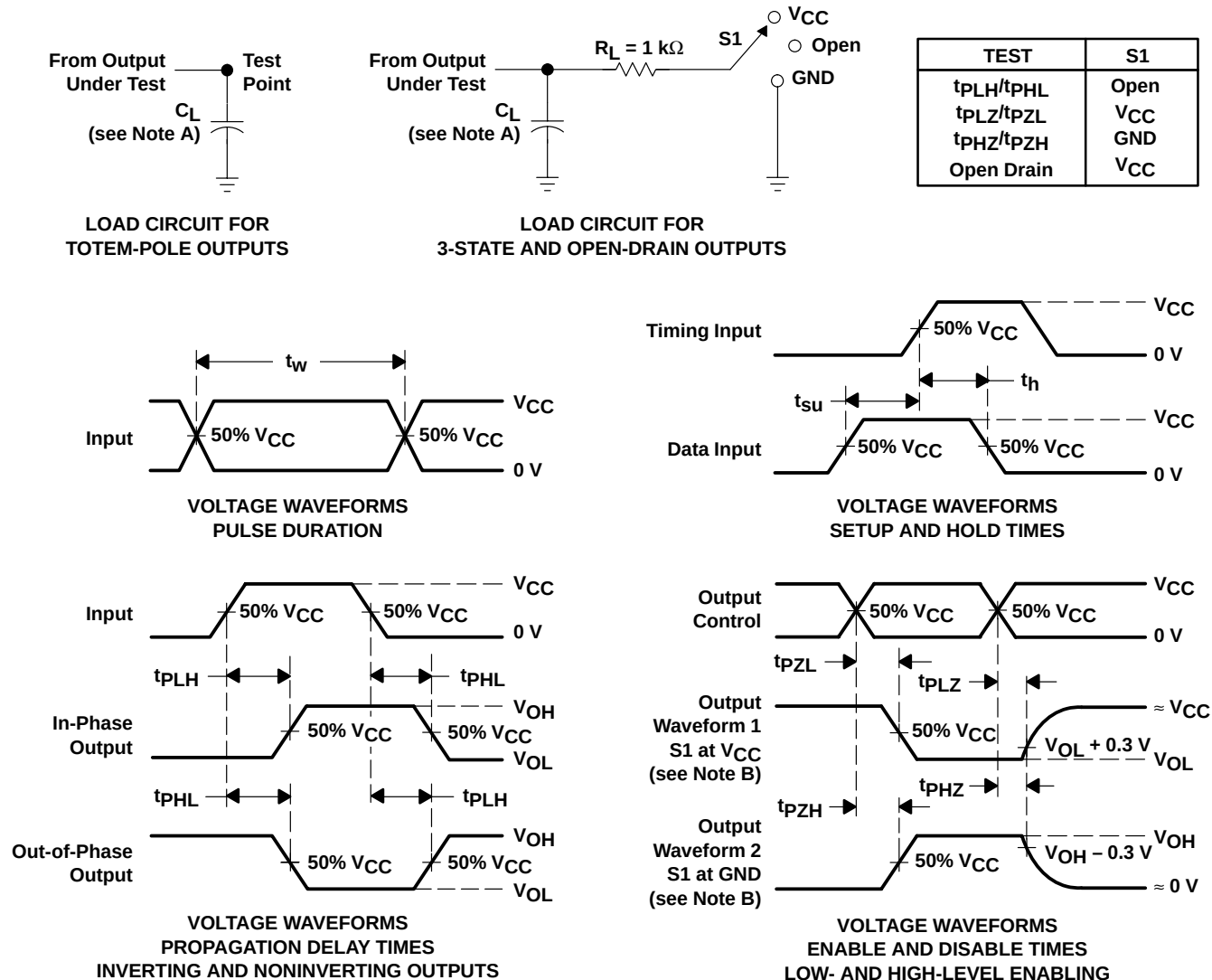
PRODUCT PREVIEW



SN54LV540A, SN74LV540A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS409A – APRIL 1998 – REVISED JUNE 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV541A, SN74LV541A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS410C – APRIL 1998 – REVISED JULY 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 200 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Package, Chip Carriers (FK), and DIPs (J)**

description

The 'LV541A devices are octal buffers/drivers designed for 2-V to 5.5-V V_{CC} operation.

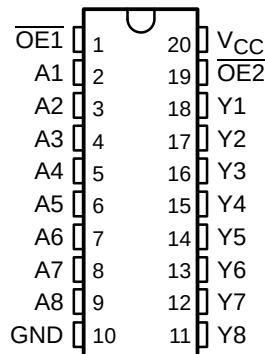
These devices are ideal for driving bus lines or buffer memory address registers. They feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

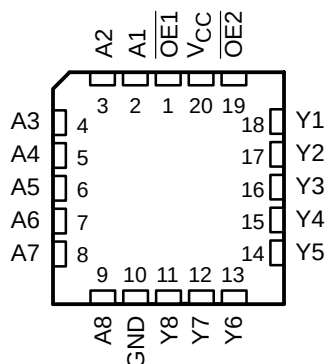
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV541A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV541A is characterized for operation from -40°C to 85°C .

SN54LV541A . . . J OR W PACKAGE
SN74LV541A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV541A . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer/driver)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

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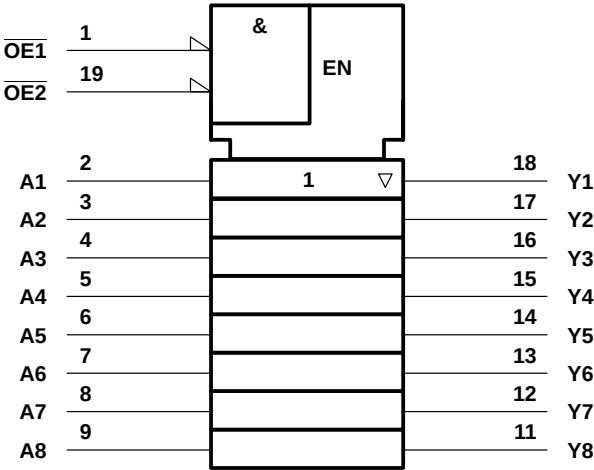
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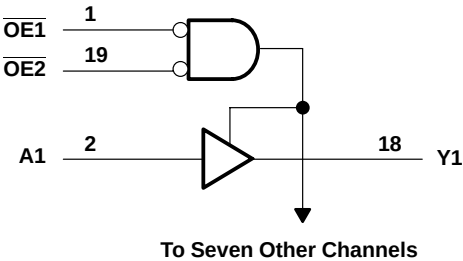
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range applied in high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3):	
DB package	115°C/W
DGV package	146°C/W
DW package	97°C/W
NS package	100°C/W
PW package	128°C/W
Storage temperature range, T_{Stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - This value is limited to 7 V maximum.
 - The package thermal impedance is calculated in accordance with JESD 51.

SN54LV541A, SN74LV541A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

			SN54LV541A		SN74LV541A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	0	V _{CC}	V
		3-state	0	5.5	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−8		−8		
		V _{CC} = 4.5 V to 5.5 V	−16		−16		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	8		8		
		V _{CC} = 4.5 V to 5.5 V	16		16		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LV541A, SN74LV541A

OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV541A			SN74LV541A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = −50 μA	2 V to 5.5 V	V _{CC} −0.1			V _{CC} −0.1			V
	I _{OH} = −2 mA	2.3 V	2			2			
	I _{OH} = −8 mA	3 V	2.48			2.48			
	I _{OH} = −16 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 8 mA	3 V	0.44			0.44			
	I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	1.9			1.9			pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV541A		SN74LV541A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF	6.7	11.3		1	13.5	1	13.5	ns
t _{en} *	OE	Y		8.5	16.6		1	19.5	1	19.5	
t _{dis} *	OE	Y		8.4	13.1		1	15	1	15	
t _{pd}	A	Y	C _L = 50 pF	8.7	15.9		1	18.5	1	18.5	ns
t _{en}	OE	Y		10.5	20.7		1	24	1	24	
t _{dis}	OE	Y		12.3	17.9		1	20	1	20	
t _{sk(o)} †					2					2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV541A		SN74LV541A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A	Y	C _L = 15 pF	4.8	7		1	8.5	1	8.5	ns
t _{en} *	OE	Y		6.1	10.5		1	11	1	11	
t _{dis} *	OE	Y		5.8	11		1	12	1	12	
t _{pd}	A	Y	C _L = 50 pF	6.1	10.5		1	12	1	12	ns
t _{en}	OE	Y		7.4	14		1	16	1	16	
t _{dis}	OE	Y		8.8	15.4		1	17.5	1	17.5	
t _{sk(o)} †					1.5					1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LV541A, SN74LV541A
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV541A		SN74LV541A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A	Y	$C_L = 15\text{ pF}$	3.5	5		1	6	1	6	ns
t_{en}^*	$\overline{OE}$	Y		4.3	7.2		1	8.5	1	8.5	
t_{dis}^*	$\overline{OE}$	Y		3.9	7		1	8	1	8	
t_{pd}	A	Y	$C_L = 50\text{ pF}$	4.3	7		1	8	1	8	ns
t_{en}	$\overline{OE}$	Y		5.3	9.2		1	10.5	1	10.5	
t_{dis}	$\overline{OE}$	Y		5.6	8.8		1	10	1	10	
$t_{sk(o)}^\dagger$					1					1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV541A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.53	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.37	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.86		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

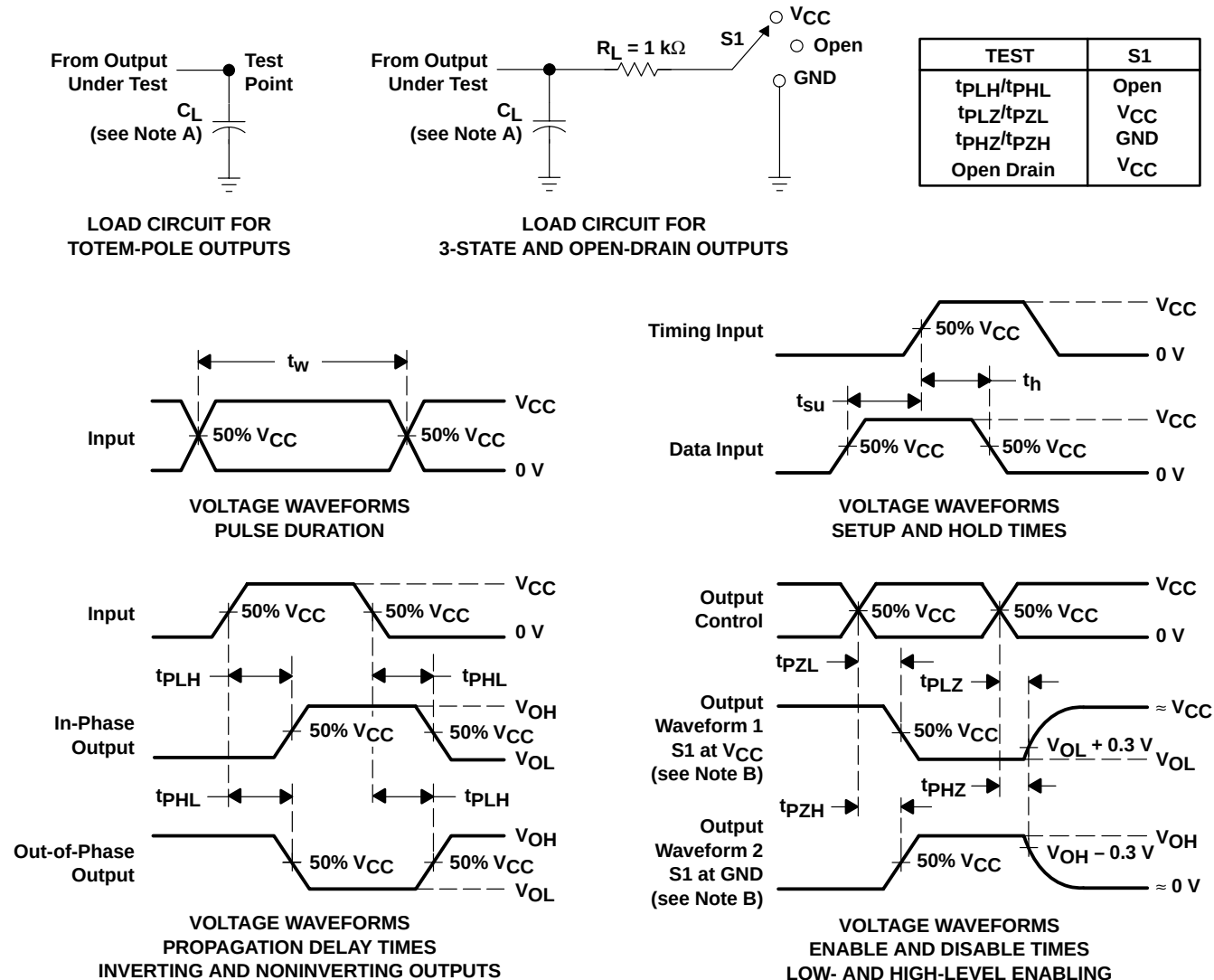
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	16.3	pF
				5 V	17.8	

SN54LV541A, SN74LV541A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV573A, SN74LV573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

The 'LV573A devices are octal transparent D-type latches designed for 2-V to 5.5-V V_{CC} operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

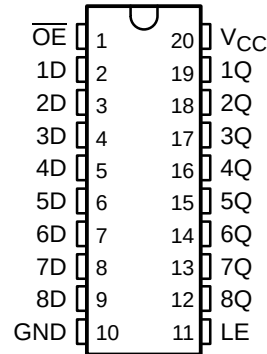
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV573A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV573A is characterized for operation from -40°C to 85°C .

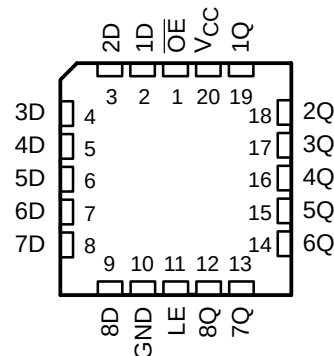
FUNCTION TABLE
(each latch)

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

SN54LV573A . . . J OR W PACKAGE
SN74LV573A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV573A . . . FK PACKAGE
(TOP VIEW)



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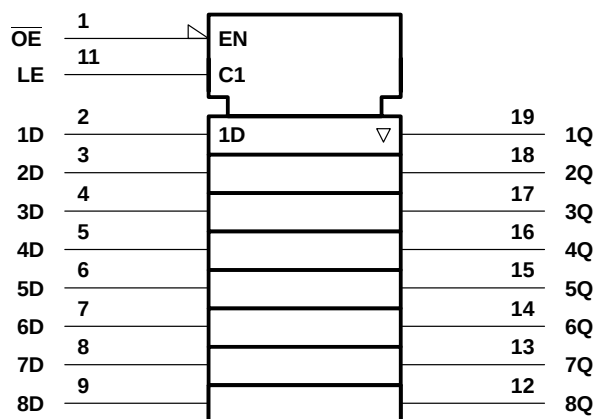
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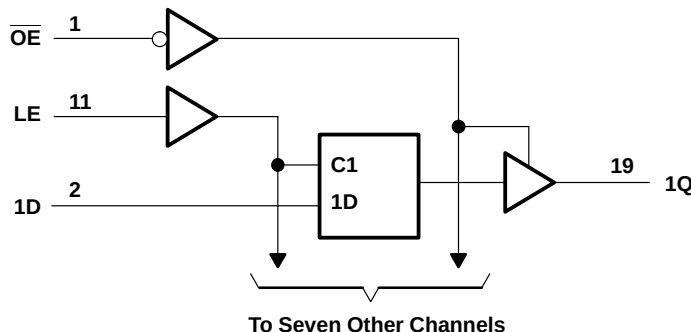
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range applied in high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DGV package	146°C/W
DW package	97°C/W
NS package	100°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV573A, SN74LV573A

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		SN54LV573A		SN74LV573A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.75	V _{CC} × 0.75		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	High or low state	0 V _{CC}	0 V _{CC}		V
		3-state	0 5.5	0 5.5		
I _{OH}	High-level output current	V _{CC} = 2 V	–50	–50		μA
		V _{CC} = 2.3 V to 2.7 V	–2	–2		
		V _{CC} = 3 V to 3.6 V	–8	–8		mA
		V _{CC} = 4.5 V to 5.5 V	–16	–16		
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50		μA
		V _{CC} = 2.3 V to 2.7 V	2	2		
		V _{CC} = 3 V to 3.6 V	8	8		mA
		V _{CC} = 4.5 V to 5.5 V	16	16		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0 200	0 200		ns/V
		V _{CC} = 3 V to 3.6 V	0 100	0 100		
		V _{CC} = 4.5 V to 5.5 V	0 20	0 20		
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV573A			SN74LV573A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –8 mA	3 V	2.48			2.48			
	I _{OH} = –16 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 8 mA	3 V	0.44			0.44			
	I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	1.8			1.8			pF



SN54LV573A, SN74LV573A

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER			$T_A = 25^\circ\text{C}$		SN54LV573A		SN74LV573A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	LE high	6.5		6.5		6.5		ns
t_{SU}	Setup time	Data before LE↓	5		5		5		ns
t_H	Hold time	Data after LE↓	2		2		2		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER			$T_A = 25^\circ\text{C}$		SN54LV573A		SN74LV573A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	LE high	5		5		5		ns
t_{SU}	Setup time	Data before LE↓	3.5		3.5		3.5		ns
t_H	Hold time	Data after LE↓	1.5		1.5		1.5		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER			$T_A = 25^\circ\text{C}$		SN54LV573A		SN74LV573A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	LE high	5		5		5		ns
t_{SU}	Setup time	Data before LE↓	3.5		3.5		3.5		ns
t_H	Hold time	Data after LE↓	1.5		1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV573A		SN74LV573A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	D	Q	$C_L = 15\text{ pF}$	8.9	15.8		1	18	1	18	ns
	LE	Q		9.6	16.2		1	19	1	19	
t_{en}^*	$\overline{OE}$	Q		9.3	16.2		1	19	1	19	
t_{dis}^*	$\overline{OE}$	Q		6.7	12.6		1	15	1	15	
t_{pd}	D	Q	$C_L = 50\text{ pF}$	10.9	18.7		1	21	1	21	ns
	LE	Q		11.6	19.1		1	23	1	23	
t_{en}	$\overline{OE}$	Q		11.4	19		1	22	1	22	
t_{dis}	$\overline{OE}$	Q		8.6	17.3		1	19	1	19	
$t_{sk(o)}^\dagger$					2					2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

PRODUCT PREVIEW



SN54LV573A, SN74LV573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV573A		SN74LV573A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	D	Q	$C_L = 15\text{ pF}$	6.2	11		1	13	1	13	ns
	LE	Q		6.8	11.9		1	14	1	14	
t_{en}^*	$\overline{OE}$	Q		6.6	11.5		1	13.5	1	13.5	
t_{dis}^*	$\overline{OE}$	Q		4.9	11		1	13	1	13	
t_{pd}	D	Q	$C_L = 50\text{ pF}$	7.7	14.5		1	16.5	1	16.5	ns
	LE	Q		8.2	15.4		1	17.5	1	17.5	
t_{en}	$\overline{OE}$	Q		8	15		1	17	1	17	
t_{dis}	$\overline{OE}$	Q		6.2	14.5		1	16.5	1	16.5	
$t_{sk(o)}^\dagger$				1.5						1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV573A		SN74LV573A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	D	Q	$C_L = 15\text{ pF}$	4.3	6.8		1	8	1	8	ns
	LE	Q		4.7	7.7		1	9	1	9	
t_{en}^*	$\overline{OE}$	Q		4.7	7.7		1	9	1	9	
t_{dis}^*	$\overline{OE}$	Q		3.5	7.7		1	9	1	9	
t_{pd}	D	Q	$C_L = 50\text{ pF}$	5.3	8.8		1	10	1	10	ns
	LE	Q		5.7	9.7		1	11	1	11	
t_{en}	$\overline{OE}$	Q		5.7	9.7		1	11	1	11	
t_{dis}	$\overline{OE}$	Q		4.2	9.7		1	11	1	11	
$t_{sk(o)}^\dagger$				1						1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER			SN74LV573A			UNIT
			MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.55	0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.47	−0.8		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.93			V
$V_{IH(D)}$	High-level dynamic input voltage		2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99		V

NOTE 5: Characteristics are for surface-mount packages only.



SN54LV573A, SN74LV573A
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

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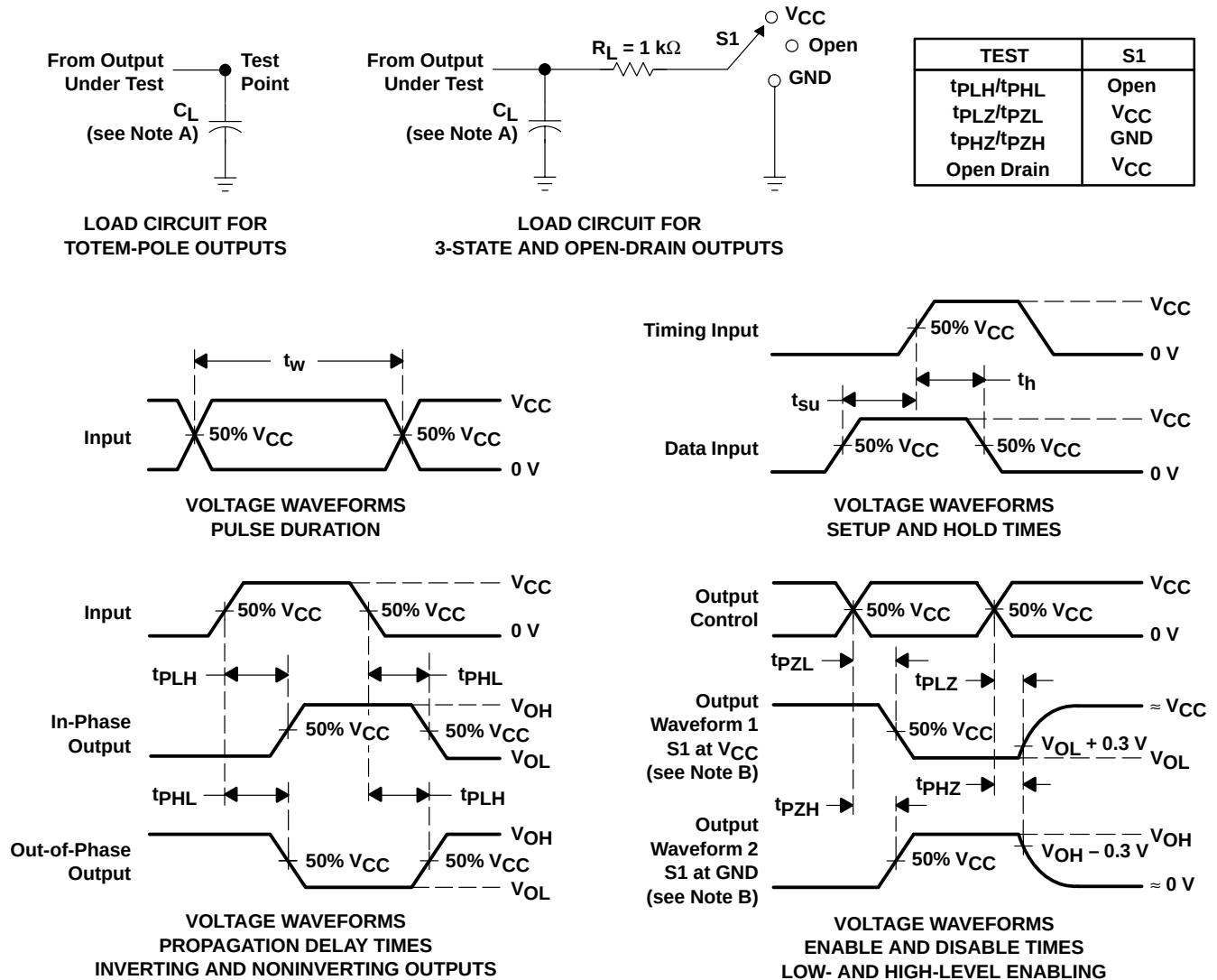
operating characteristics, $T_A = 25^{\circ}\text{C}$

PARAMETER			TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance	Outputs enabled	C _L = 50 pF, f = 10 MHz	3.3 V	16	pF
				5 V	18	
		LE to Q		3.3 V	18.2	
				5 V	21.3	

SN54LV573A, SN74LV573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS412A – APRIL 1998 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

The 'LV574A devices are octal edge-triggered D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

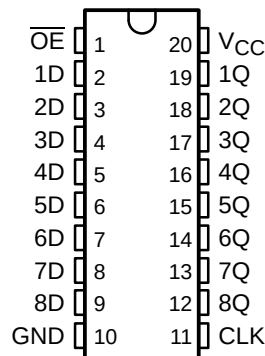
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV574A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV574A is characterized for operation from -40°C to 85°C .

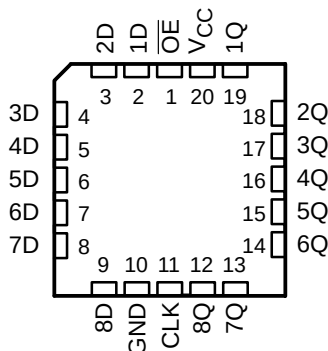
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	H or L	X	Q_0
H	X	X	Z

SN54LV574A . . . J OR W PACKAGE
SN74LV574A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV574A . . . FK PACKAGE
(TOP VIEW)



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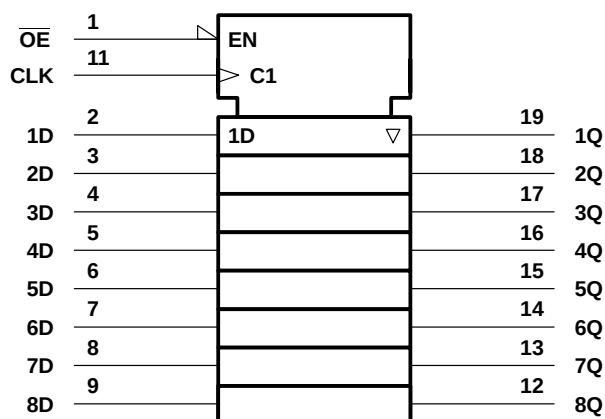
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SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

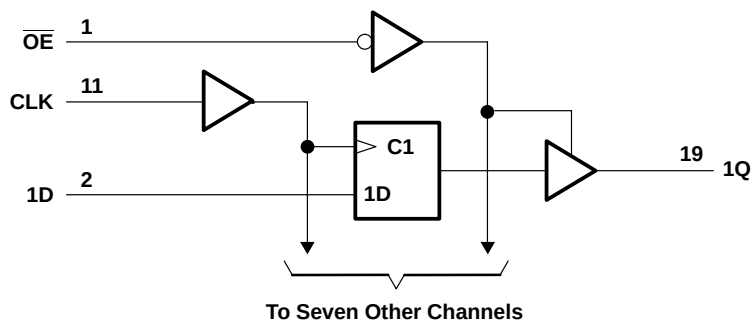
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range applied in high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DGV package	146°C/W
DW package	97°C/W
NS package	100°C/W
PW package	128°C/W

Storage temperature range, T_{stg} –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV574A, SN74LV574A

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		SN54LV574A		SN74LV574A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.75	V _{CC} × 0.75		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	High or low state	0 V _{CC}	0 V _{CC}		V
		3-state	0	5.5	0	
I _{OH}	High-level output current	V _{CC} = 2 V	–50	–50		μA
		V _{CC} = 2.3 V to 2.7 V	–2	–2		
		V _{CC} = 3 V to 3.6 V	–8	–8		
		V _{CC} = 4.5 V to 5.5 V	–16	–16		
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50		μA
		V _{CC} = 2.3 V to 2.7 V	2	2		
		V _{CC} = 3 V to 3.6 V	8	8		
		V _{CC} = 4.5 V to 5.5 V	16	16		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV574A			SN74LV574A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –8 mA	3 V	2.48			2.48			
	I _{OH} = –16 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 8 mA	3 V	0.44			0.44			
	I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	1.8			1.8			pF



SN54LV574A, SN74LV574A

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER			$T_A = 25^\circ\text{C}$		SN54LV574A		SN74LV574A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLK high or low	7		7		7		ns
t_{SU}	Setup time	High or low before CLK $\uparrow$	5.5		5.5		5.5		ns
t_H	Hold time	Data after CLK $\uparrow$	2		2		2		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER			$T_A = 25^\circ\text{C}$		SN54LV574A		SN74LV574A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLK high or low	5		5		5		ns
t_{SU}	Setup time	High or low before CLK $\uparrow$	3.5		3.5		3.5		ns
t_H	Hold time	Data after CLK $\uparrow$	1.5		1.5		1.5		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER			$T_A = 25^\circ\text{C}$		SN54LV574A		SN74LV574A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLK high or low	5		5		5		ns
t_{SU}	Setup time	High or low before CLK $\uparrow$	3.5		3.5		3.5		ns
t_H	Hold time	Data after CLK $\uparrow$	1.5		1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV574A		SN74LV574A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}^*$	60	105		50		50		MHz
			$C_L = 50 \text{ pF}$	50	85		40		40		
t_{PD}^*	CLK	Q	$C_L = 15 \text{ pF}$	9.6	16.6		1	20	1	20	ns
t_{EN}^*	$\overline{OE}$	Q		9.2	16.1		1	19	1	19	
t_{DIS}^*	$\overline{OE}$	Q		6.5	12.8		1	15	1	15	
t_{PD}	CLK	Q	$C_L = 50 \text{ pF}$	11.6	19.6		1	23	1	23	ns
t_{EN}	$\overline{OE}$	Q		10.9	19		1	22	1	22	
t_{DIS}	$\overline{OE}$	Q		8.4	17.5		1	20	1	20	
$t_{sk(o)}^\dagger$					2					2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

PRODUCT PREVIEW



SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS412A – APRIL 1998 – REVISED JUNE 1998

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV574A		SN74LV574A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF*	80	145		65		65		MHz
			C _L = 50 pF	50	120		45		45		
t _{pd} *	CLK	Q	C _L = 15 pF	6.8	13.2		1	15.5	1	15.5	ns
t _{en} *	$\overline{\text{OE}}$	Q		6.4	12.8		1	15	1	15	
t _{dis} *	$\overline{\text{OE}}$	Q		4.8	13		1	15	1	15	
t _{pd}	CLK	Q	C _L = 50 pF	8.1	16.7		1	19	1	19	ns
t _{en}	$\overline{\text{OE}}$	Q		7.7	16.3		1	18.5	1	18.5	
t _{dis}	$\overline{\text{OE}}$	Q		6.1	15		1	17	1	17	
t _{sk(o)} [†]				1.5					1.5		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV574A		SN74LV574A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF*	130	205		110		110		MHz
			C _L = 50 pF	85	175		75		75		
t _{pd} *	CLK	Q	C _L = 15 pF	4.8	8.6		1	10	1	10	ns
t _{en} *	$\overline{\text{OE}}$	Q		4.6	9		1	10.5	1	10.5	
t _{dis} *	$\overline{\text{OE}}$	Q		3.5	9		1	10.5	1	10.5	
t _{pd}	CLK	Q	C _L = 50 pF	5.7	10.6		1	12	1	12	ns
t _{en}	$\overline{\text{OE}}$	Q		5.5	11		1	12.5	1	12.5	
t _{dis}	$\overline{\text{OE}}$	Q		4.1	10.1		1	11.5	1	11.5	
t _{sk(o)} [†]				1					1		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

noise characteristics, $V_{CC} = 3.3 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER			SN74LV574A			UNIT
			MIN	TYP	MAX	
$V_{\text{OL(P)}}$	Quiet output, maximum dynamic V_{OL}		0.65	0.8		V
$V_{\text{OL(V)}}$	Quiet output, minimum dynamic V_{OL}		−0.59	−0.8		V
$V_{\text{OH(V)}}$	Quiet output, minimum dynamic V_{OH}		2.84			V
$V_{\text{IH(D)}}$	High-level dynamic input voltage		2.31			V
$V_{\text{IL(D)}}$	Low-level dynamic input voltage			0.99		V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$	3.3 V	20.4	pF
				5 V	23.8	



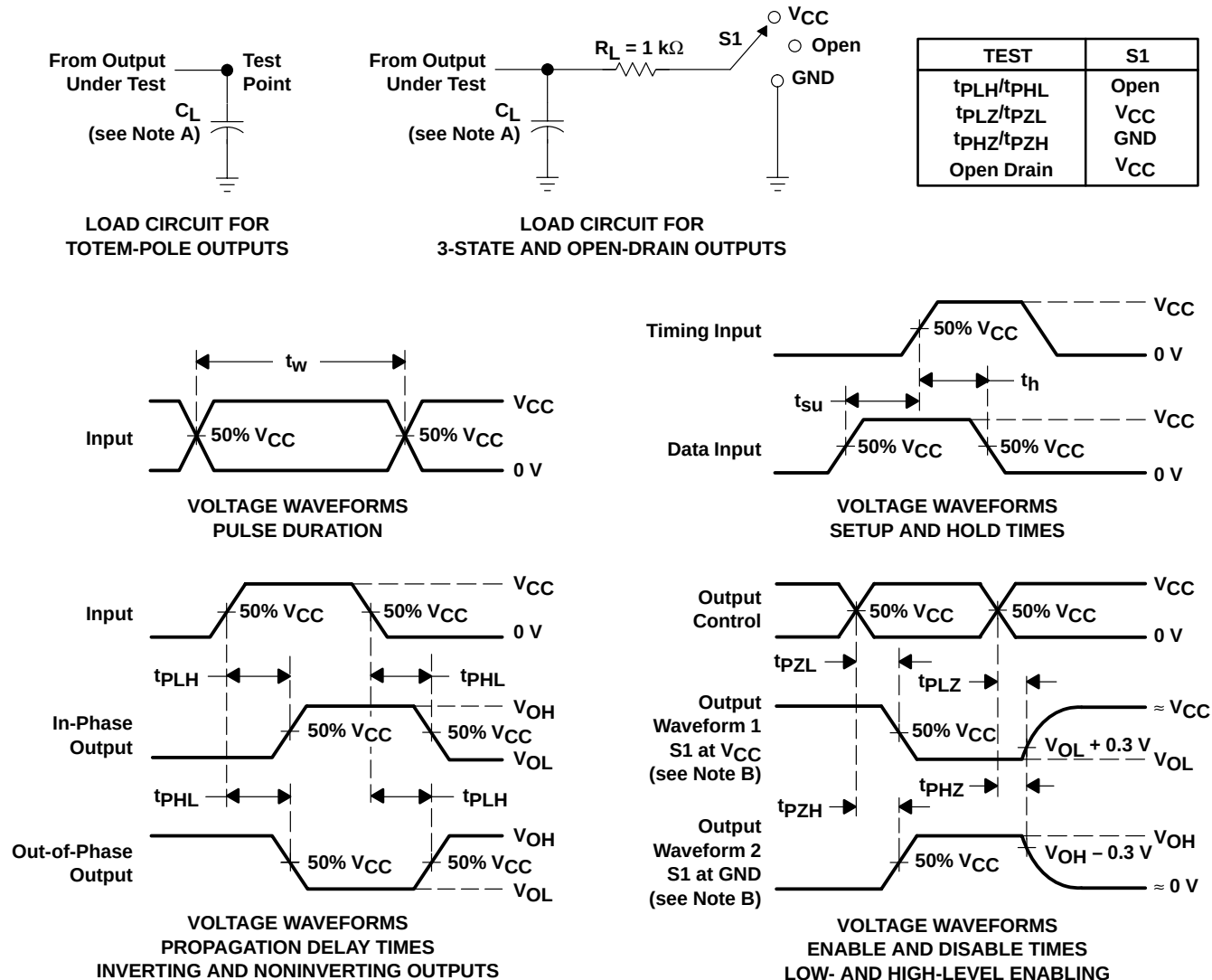
SN54LV574A, SN74LV574A

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

SCLS412A – APRIL 1998 – REVISED JUNE 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV594A, SN74LV594A 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

SCLS413A – APRIL 1998 – JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Both Shift and Storage Registers
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

description

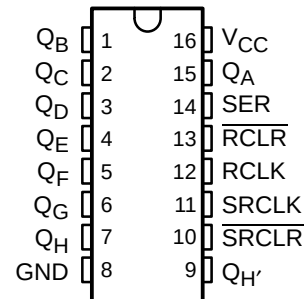
The 'LV594A devices are 8-bit shift registers designed for 2-V to 5.5-V V_{CC} operation.

These devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clock ($RCLK$, $SRCLK$) and direct overriding clear ($RCLR$, $SRCLR$) inputs are provided on both the shift and storage registers. A serial output (Q_H') is provided for cascading purposes.

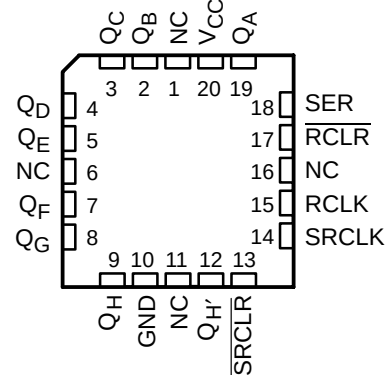
Both the shift-register ($SRCLK$) and storage-register ($RCLK$) clocks are positive-edge triggered. If both clocks are connected together, the shift register is always one count pulse ahead of the storage register.

The SN54LV594A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV594A is characterized for operation from -40°C to 85°C .

SN54LV594A . . . J OR W PACKAGE
SN74LV594A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV594A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

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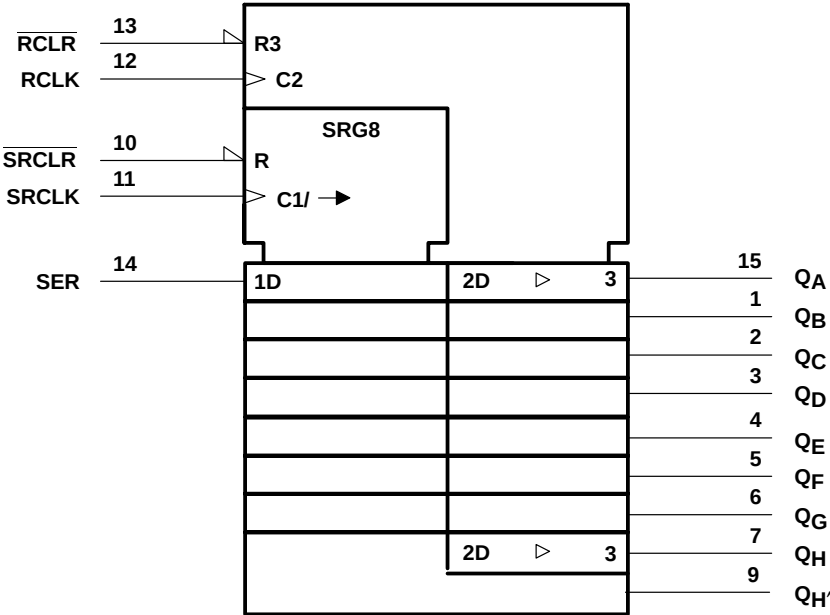
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SN54LV594A, SN74LV594A
8-BIT SHIFT REGISTERS
WITH OUTPUT REGISTERS

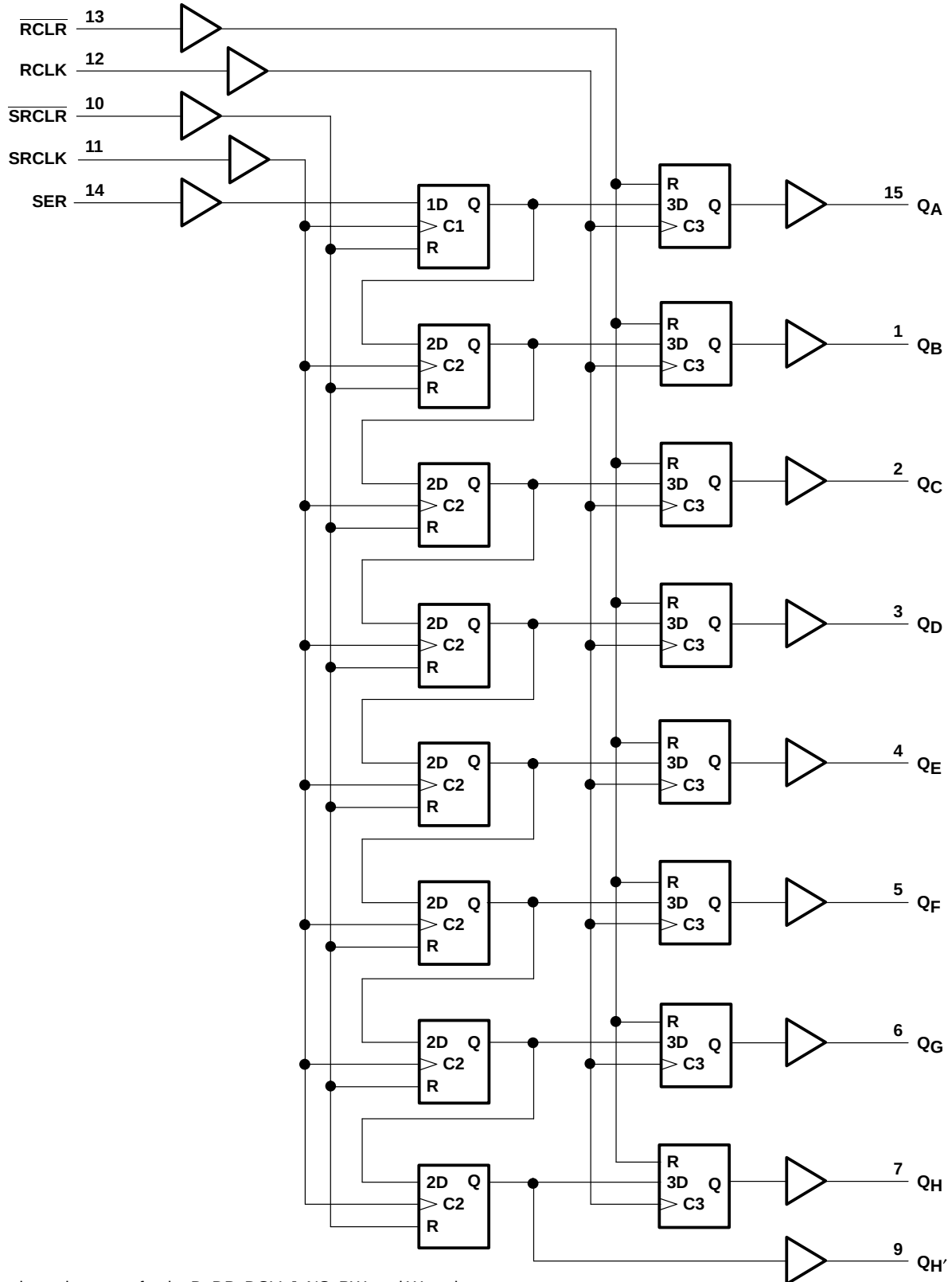
SCLS413A – APRIL 1998 – JUNE 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

PRODUCT PREVIEW

SN54LV594A, SN74LV594A

8-BIT SHIFT REGISTERS

WITH OUTPUT REGISTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
NS package	111°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. This value is limited to 7 V maximum.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV594A		SN74LV594A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−6		−6		
		V _{CC} = 4.5 V to 5.5 V	−12		−12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	6		6		
		V _{CC} = 4.5 V to 5.5 V	12		12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV594A			SN74LV594A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -6 mA	3 V	2.48			2.48			
	I _{OH} = -12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V							pF
		5 V							

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54LV594A		SN74LV594A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	RCLK or SRCLK high or low						ns
		RCLR or SRCLR low						
t _{su}	Setup time	SER before SRCLK↑						ns
		SRCLK↑ before RCLK↑†						
		SRCLR low before RCLK↑						
		SRCLR high (inactive) before SRCLK↑						
		RCLR high (inactive) before RCLK↑						
t _h	Hold time	SER after SRCLK↑						ns

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54LV594A		SN74LV594A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	RCLK or SRCLK high or low						ns
		RCLR or SRCLR low						
t _{su}	Setup time	SER before SRCLK↑						ns
		SRCLK↑ before RCLK↑†						
		SRCLR low before RCLK↑						
		SRCLR high (inactive) before SRCLK↑						
		RCLR high (inactive) before RCLK↑						
t _h	Hold time	SER after SRCLK↑						ns

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

SN54LV594A, SN74LV594A

8-BIT SHIFT REGISTERS

WITH OUTPUT REGISTERS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV594A		SN74LV594A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	RCLK or SRCLK high or low						ns
		$\overline{\text{RCLR}}$ or $\overline{\text{SRCLR}}$ low						
t_{su}	Setup time	SER before $\text{SRCLK}\uparrow$						ns
		$\text{SRCLK}\uparrow$ before $\text{RCLK}\uparrow^\dagger$						
		$\overline{\text{SRCLR}}$ low before $\text{RCLK}\uparrow$						
		$\overline{\text{SRCLR}}$ high (inactive) before $\text{SRCLK}\uparrow$						
		$\overline{\text{RCLR}}$ high (inactive) before $\text{RCLK}\uparrow$						
t_h	Hold time	SER after $\text{SRCLK}\uparrow$						ns

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV594A		SN74LV594A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF*								MHz
			C _L = 50 pF								
t _{PLH} *	RCLK	Q _A –Q _H	C _L = 15 pF								ns
t _{PHL} *											
t _{PLH} *	SRCLK	Q _H '									
t _{PHL} *											
t _{PHL} *	RCL $\overline{\text{R}}$	Q _A –Q _H									
t _{PHL} *	S $\overline{\text{RCLR}}$	Q _H '									
t _{PLH}	RCLK	Q _A –Q _H	C _L = 50 pF								ns
t _{PHL}											
t _{PLH}	SRCLK	Q _H '									
t _{PHL}											
t _{PHL}	RCL $\overline{\text{R}}$	Q _A –Q _H									
t _{PHL}	S $\overline{\text{RCLR}}$	Q _H '									
t _{sk(0)} [‡]											

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

‡ Skew between any two outputs of the same package switching in the same direction

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV594A		SN74LV594A		UNIT		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX			
f _{max}			C _L = 15 pF*								MHz		
			C _L = 50 pF										
t _{PLH} *	RCLK	Q _A –Q _H	C _L = 15 pF								ns		
t _{PHL} *													
t _{PLH} *	SRCLK	Q _H '											
t _{PHL} *													
t _{PHL} *	RCLR	Q _A –Q _H											
t _{PHL} *	SRCLR	Q _H '											
t _{PLH}	RCLK	Q _A –Q _H		C _L = 50 pF									ns
t _{PHL}													
t _{PLH}	SRCLK	Q _H '											
t _{PHL}													
t _{PHL}	RCLR	Q _A –Q _H											
t _{PHL}	SRCLR	Q _H '											
t _{sk(o)} [†]													

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV594A		SN74LV594A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF*								MHz
			C _L = 50 pF								
t _{PLH} *	RCLK	Q _A –Q _H	C _L = 15 pF								ns
t _{PHL} *											
t _{PLH} *	SRCLK	Q _H '									
t _{PHL} *											
t _{PHL} *	RCL $\overline{\text{R}}$	Q _A –Q _H									
t _{PHL} *	S $\overline{\text{RCLR}}$	Q _H '									
t _{PLH}	RCLK	Q _A –Q _H	C _L = 50 pF								ns
t _{PHL}											
t _{PLH}	SRCLK	Q _H '									
t _{PHL}											
t _{PHL}	RCL $\overline{\text{R}}$	Q _A –Q _H									
t _{PHL}	S $\overline{\text{RCLR}}$	Q _H '									
t _{sk(0)} [†]											

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

SN54LV594A, SN74LV594A
8-BIT SHIFT REGISTERS
WITH OUTPUT REGISTERS

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noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

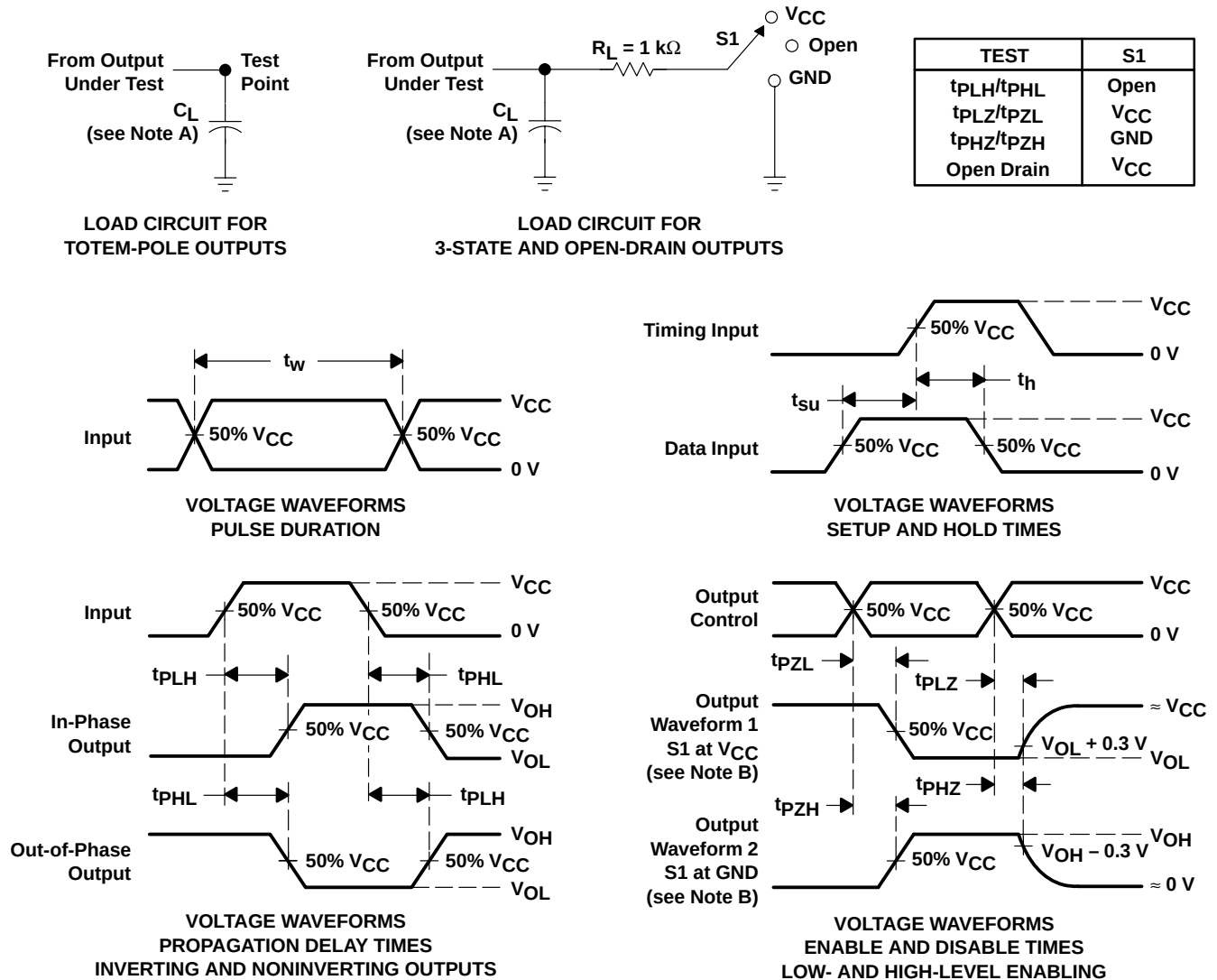
PARAMETER	SN74LV594A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$ High-level dynamic input voltage				V
$V_{IL(D)}$ Low-level dynamic input voltage				V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V		pF
		5 V		

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN54LV595A, SN74LV595A 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

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- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **8-Bit Serial-In, Parallel-Out Shift**
- **Shift Register Has Direct Clear**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

The 'LV595A devices are 8-bit shift registers designed for 2-V to 5.5-V V_{CC} operation.

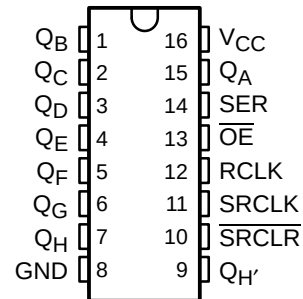
These devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{\text{SRCLR}}$) input, serial (SER) input, and a serial output for cascading. When the output-enable ($\overline{\text{OE}}$) input is high, all outputs except $Q_{H'}$ are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register.

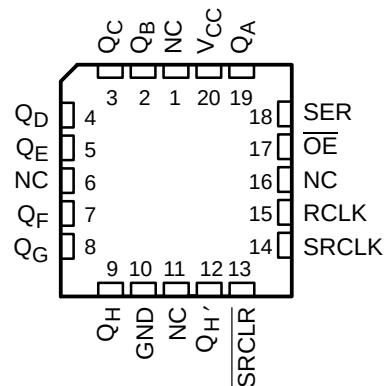
To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV595A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV595A is characterized for operation from -40°C to 85°C .

SN54LV595A . . . J OR W PACKAGE
SN74LV595A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV595A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

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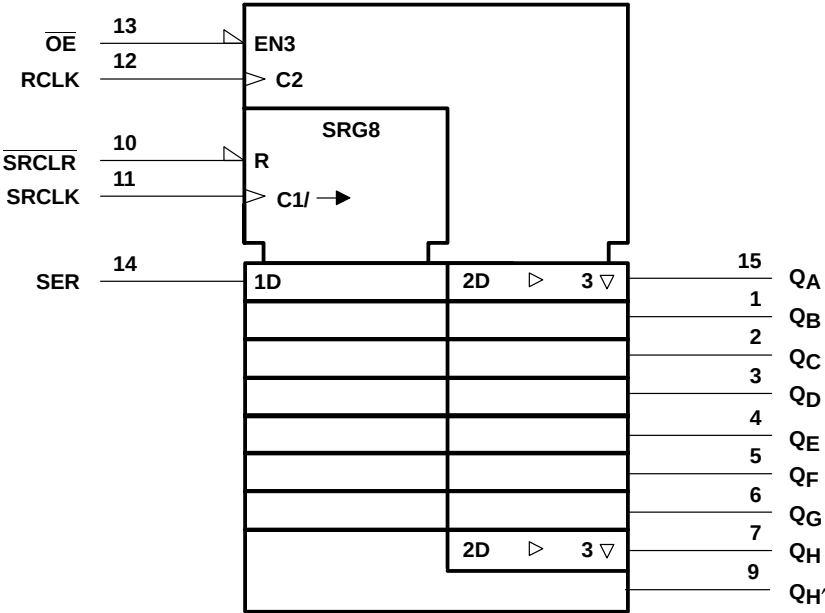
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SN54LV595A, SN74LV595A
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS

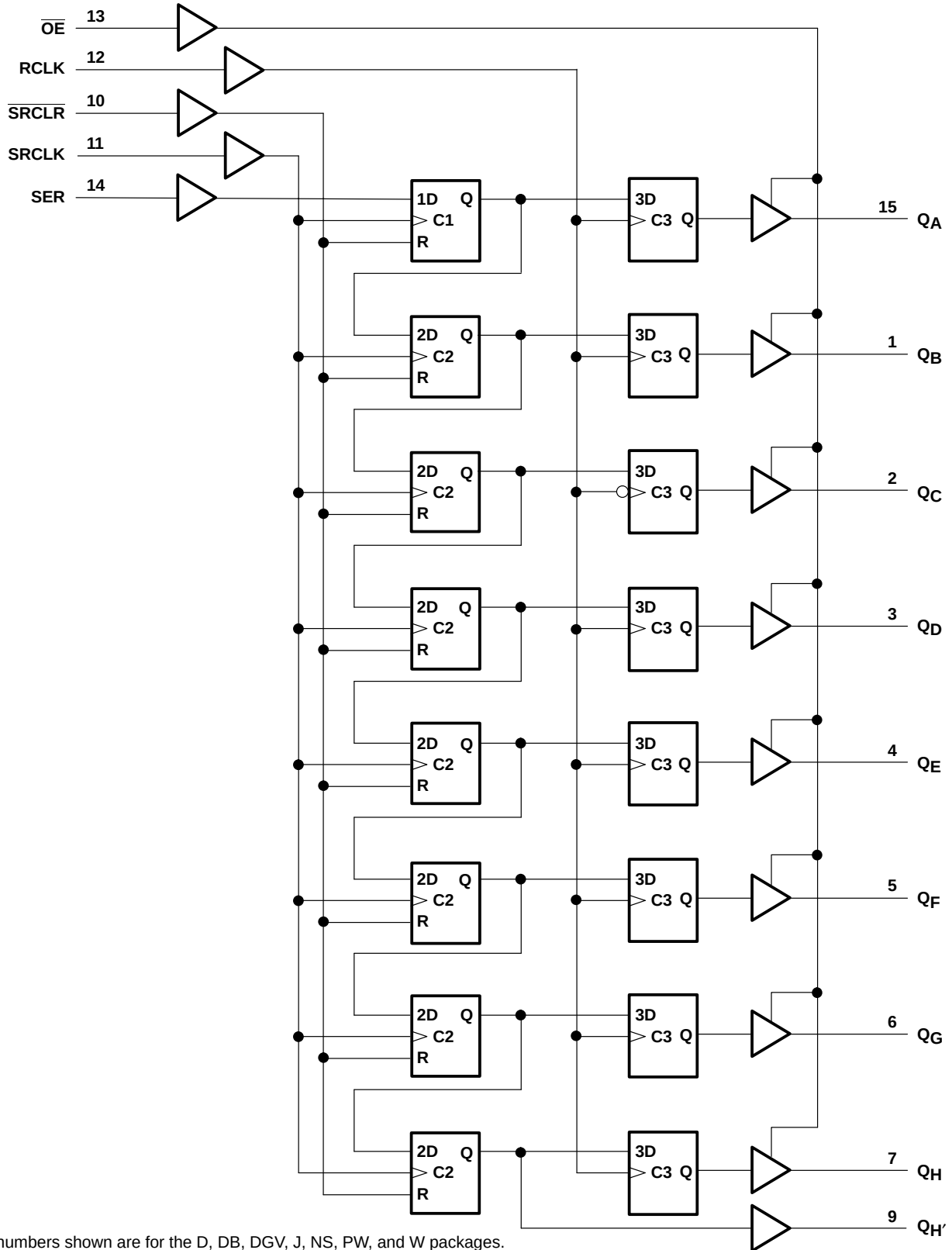
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

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SN54LV595A, SN74LV595A
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range applied in high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
NS package	111°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV595A, SN74LV595A
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS
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recommended operating conditions (see Note 4)

			SN54LV595A		SN74LV595A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	0	V _{CC}	V
		3-state	0	5.5	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V		–50		–50	μA
		V _{CC} = 2.3 V to 2.7 V		–2		–2	
		V _{CC} = 3 V to 3.6 V		–8		–8	
		V _{CC} = 4.5 V to 5.5 V		–16		–16	
I _{OL}	Low-level output current	V _{CC} = 2 V		50		50	μA
		V _{CC} = 2.3 V to 2.7 V		2		2	
		V _{CC} = 3 V to 3.6 V		8		8	
		V _{CC} = 4.5 V to 5.5 V		16		16	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LV595A, SN74LV595A

8-BIT SHIFT REGISTERS

WITH 3-STATE OUTPUT REGISTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	SN54LV595A			SN74LV595A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}		I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
		I _{OH} = -2 mA	2.3 V	2			2			
	Q _H '	I _{OH} = -6 mA	3 V	2.48			2.48			
	Q _A -Q _H	I _{OH} = -8 mA		2.48			2.48			
	Q _H '	I _{OH} = -12 mA	4.5 V	3.8			3.8			
	Q _A -Q _H	I _{OH} = -16 mA		3.8			3.8			
V _{OL}		I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
		I _{OL} = 2 mA	2.3 V	0.4			0.4			
	Q _H '	I _{OL} = 6 mA	3 V	0.44			0.44			
	Q _A -Q _H	I _{OL} = 8 mA		0.44			0.44			
	Q _H '	I _{OL} = 12 mA	4.5 V	0.55			0.55			
	Q _A -Q _H	I _{OL} = 16 mA		0.55			0.55			
I _I		V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{OZ}		V _O = V _{CC} or GND	5.5 V	±5			±5			μA
I _{CC}		V _I = V _{CC} or GND I _O = 0	5.5 V	20			20			μA
I _{off}		V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i		V _I = V _{CC} or GND	3.3 V							pF
			5 V							

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C	SN54LV595A		SN74LV595A		UNIT
			MIN	MAX	MIN	MAX	
t _w	Pulse duration	SRCLK high or low					ns
		RCLK high or low					
		SRCLR low					
t _{su}	Setup time	SER before SRCLK↑					ns
		SRCLK↑ before RCLK↑†					
		SRCLR low before RCLK↑					
		SRCLR high (inactive) before SRCLK↑					
t _h	Hold time	SER after SRCLK↑					ns

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks can be tied together, in which case the output register is one clock pulse behind the shift register.

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV595A		SN74LV595A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	SRCLK high or low						ns
		RCLK high or low						
		SRCLR low						
t_{su}	Setup time	SER before SRCLK $\uparrow$						ns
		SRCLK $\uparrow$ before RCLK $\uparrow\uparrow$						
		SRCLR low before RCLK $\uparrow$						
		SRCLR high (inactive) before SRCLK $\uparrow$						
t_h	Hold time	SER after SRCLK $\uparrow$						ns

[†] This setup time ensures the output register sees stable data from the shift-register outputs. The clocks can be tied together, in which case the output register is one clock pulse behind the shift register.

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV595A		SN74LV595A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	SRCLK high or low						ns
		RCLK high or low						
		SRCLR low						
t_{su}	Setup time	SER before SRCLK $\uparrow$						ns
		SRCLK $\uparrow$ before RCLK $\uparrow\uparrow$						
		SRCLR low before RCLK $\uparrow$						
		SRCLR high (inactive) before SRCLK $\uparrow$						
t_h	Hold time	SER after SRCLK $\uparrow$						ns

[†] This setup time ensures the output register sees stable data from the shift-register outputs. The clocks can be tied together, in which case the output register is one clock pulse behind the shift register.

PRODUCT PREVIEW

SN54LV595A, SN74LV595A 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

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switching characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV595A		SN74LV595A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF*								MHz
			C _L = 50 pF								
t _{PLH} *	RCLK	Q _A –Q _H	C _L = 15 pF								ns
t _{PHL} *											
t _{PLH} *	SRCLK	Q _H '									
t _{PHL} *											
t _{PHL} *	SRCLR	Q _H '									
t _{PZH} *	OE	Q _A –Q _H									
t _{PZL} *											
t _{PHZ} *	OE	Q _A –Q _H									
t _{PLZ} *											
t _{PLH}	RCLK	Q _A –Q _H	C _L = 50 pF								ns
t _{PHL}											
t _{PLH}	SRCLK	Q _H '									
t _{PHL}											
t _{PHL}	SRCLR	Q _H '									
t _{PZH}	OE	Q _A –Q _H									
t _{PZL}											
t _{PHZ}	OE	Q _A –Q _H									
t _{PLZ}											
t _{sk(o)} [†]											

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

SN54LV595A, SN74LV595A
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS
 SCLS414A – APRIL 1998 – REVISED JUNE 1998

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV595A		SN74LV595A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF*								MHz
			C _L = 50 pF								
t _{PLH} *	RCLK	Q _A –Q _H	C _L = 15 pF								ns
t _{PHL} *											
t _{PLH} *	SRCLK	Q _H '									
t _{PHL} *											
t _{PHL} *	$\overline{\text{SRCLR}}$	Q _H '									
t _{PZH} *	$\overline{\text{OE}}$	Q _A –Q _H									
t _{PZL} *											
t _{PHZ} *	$\overline{\text{OE}}$	Q _A –Q _H									
t _{PLZ} *											
t _{PLH}	RCLK	Q _A –Q _H	C _L = 50 pF								ns
t _{PHL}											
t _{PLH}	SRCLK	Q _H '									
t _{PHL}											
t _{PHL}	$\overline{\text{SRCLR}}$	Q _H '									
t _{PZH}	$\overline{\text{OE}}$	Q _A –Q _H									
t _{PZL}											
t _{PHZ}	$\overline{\text{OE}}$	Q _A –Q _H									
t _{PLZ}											
t _{sk(o)} [†]											

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

PRODUCT PREVIEW

SN54LV595A, SN74LV595A 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

SCLS414A – APRIL 1998 – REVISED JUNE 1998

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV595A		SN74LV595A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF*								MHz
			C _L = 50 pF								
t _{PLH} *	RCLK	Q _A –Q _H	C _L = 15 pF							ns	
t _{PHL} *											
t _{PLH} *	SRCLK	Q _H '									
t _{PHL} *											
t _{PHL} *	$\overline{\text{SRCLR}}$	Q _H '									
t _{PZH} *	$\overline{\text{OE}}$	Q _A –Q _H									
t _{PZL} *											
t _{PHZ} *	$\overline{\text{OE}}$	Q _A –Q _H									
t _{PLZ} *											
t _{PLH}	RCLK	Q _A –Q _H	C _L = 50 pF							ns	
t _{PHL}											
t _{PLH}	SRCLK	Q _H '									
t _{PHL}											
t _{PHL}	$\overline{\text{SRCLR}}$	Q _H '									
t _{PZH}	$\overline{\text{OE}}$	Q _A –Q _H									
t _{PZL}											
t _{PHZ}	$\overline{\text{OE}}$	Q _A –Q _H									
t _{PLZ}											
t _{sk(0)} [†]											

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

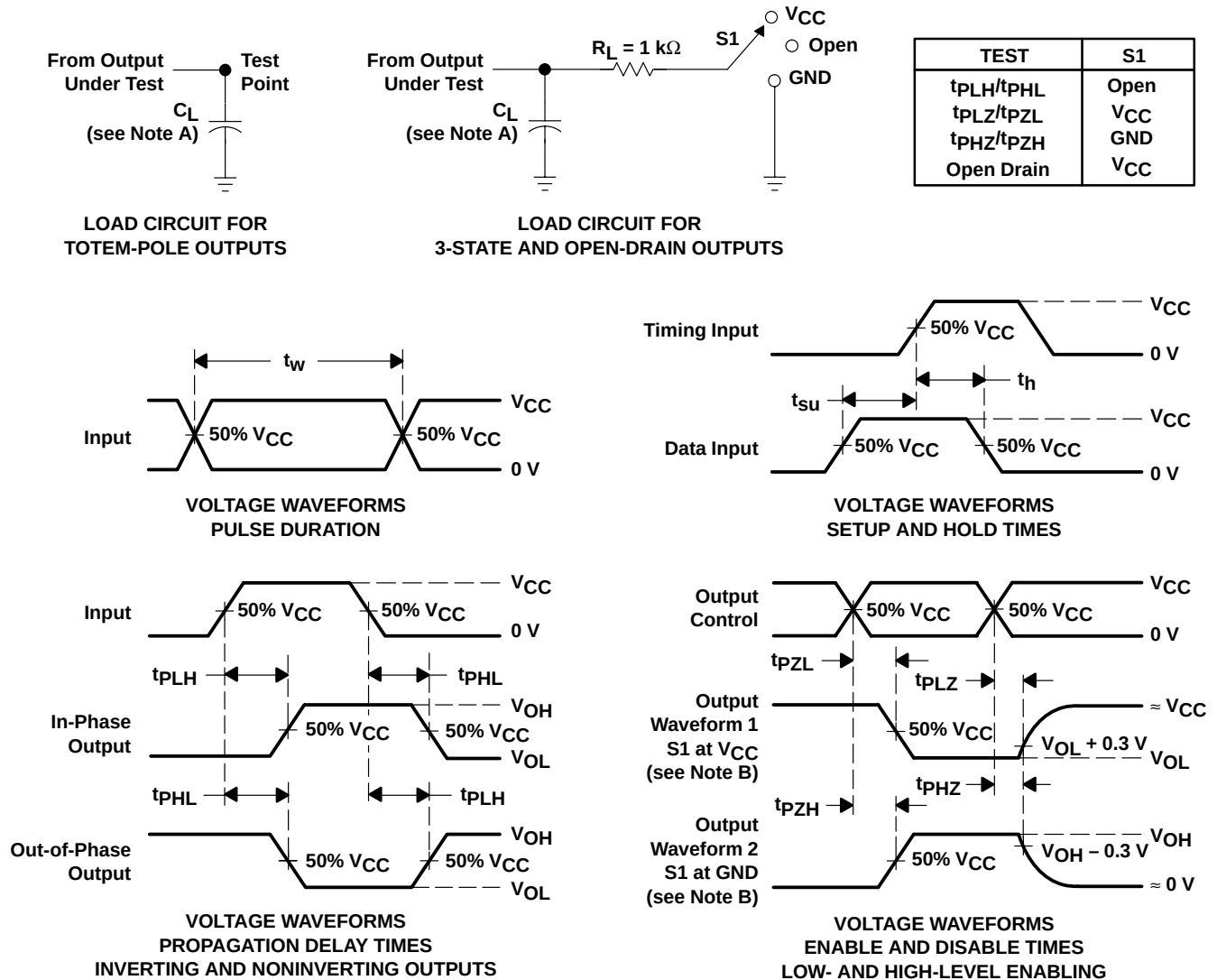
PARAMETER	SN74LV595A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$ High-level dynamic input voltage				V
$V_{IL(D)}$ Low-level dynamic input voltage				V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V		pF
		5 V		

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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Designing With Logic

SDYA009C
June 1997



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Abstract

Data sheets, which usually give information on device behavior only under recommended operating conditions, may only partially answer engineering questions that arise during the development of systems using logic devices. However, information is frequently needed regarding the behavior of the device outside the conditions in the data sheet. Such questions might be: “How does a bus driver behave with reduced (or even switched-off) supply voltage?” or “How does the delay time of a gate with a large capacitive load change?” or “What must be considered when using *backdriving*?”.

This report gives information on a number of questions that frequently arise. In addition, it provides examples that explain phenomena that the designer should be aware of when using devices outside their recommended operating conditions.

1 Introduction

The function and behavior of digital logic devices are described fully in data sheets. Most questions regarding the behavior of the device that arise when developing a system can be answered with the information given. However, the devices might be operated under conditions not covered by the data sheet. This report addresses this issue and provides information on the behavior of devices under such conditions.

Many parameter values in data sheets are not measured when the circuits are tested. The information is based on typical values that have been established experimentally and that are applicable to the majority of devices of the same type or family. In individual cases it might be necessary to interpret data and make measurements to accurately forecast the behavior of the complete system.

2 Behavior With the Supply Voltage Reduced

Although not specifically mentioned in data sheets, additional components, some of them parasitic, influence operational characteristics of devices. These components can affect the function of a system if the devices are not operated within the recommended operating conditions. For example, large systems often require that parts of the system be shut down while other parts continue to operate. Frequent problems occur at the interfaces between subsystems, which are operated with different supply voltages, or whose supply voltages are switched off. This section describes the behavior of digital circuits operated with low supply voltages.

2.1 Behavior With the Supply Voltage Switched Off

Because many circuits can be used with the various logic families, no general rule applies to the behavior of systems with supply voltages switched off. For this reason, only the most important circuits and their behavior are discussed.

2.1.1 Bipolar Circuits

Figure 1 shows the simplified circuit of a TTL device with diode inputs, such as are used with devices in the SN74LS (low-power Schottky TTL) logic family. However, the following comments apply to all other bipolar logic families.

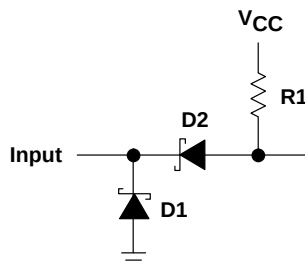


Figure 1. Input Circuit of a Bipolar Device

When the supply voltage in a system is switched off ($V_{CC} = 0$ V), the V_{CC} pin of a logic device is short circuited to ground via the other components in the system. If a voltage is then applied to the input of a device, as shown in Figure 1, and if this voltage lies within the logic-level range ($V_I = 0$ to 5.5 V), diode D2 is blocking and the clamping diode D1 is biased into a blocking state. Therefore, a very small current flows into the device, corresponding to the leakage current of these diodes. The value for this current given in the data sheets for the corresponding input voltage can be used. This statement applies, without exception, to all TTL devices.

Figure 2 shows the output stage of circuits from the SN74 (standard TTL) series. Parasitic collector-substrate diode D2 and diode D3 are in a blocking position between the V_{CC} and GND connections of all devices. If the V_{CC} pin is at GND potential and a positive voltage is applied to the output, diode D1 is blocking and the output is in the high-impedance state.

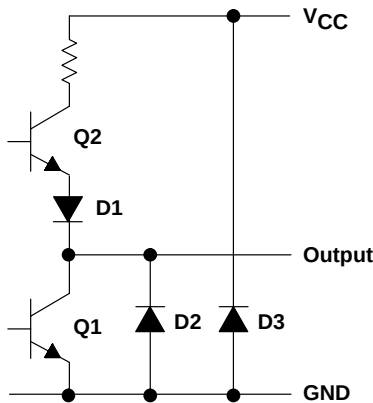


Figure 2. Device Output From SN74 Family (Standard TTL)

Other bias relationships result when supply voltages are switched off to Schottky TTL devices (SN74LS, SN74S, SN74ALS, SN74AS, and SN74F series). Figure 3 shows the important parts of the output stage. If a voltage is applied to the output of the device whose supply voltage is switched off, parasitic diode D1, which is in parallel with resistor R, becomes conductive. The output is then at a low impedance.

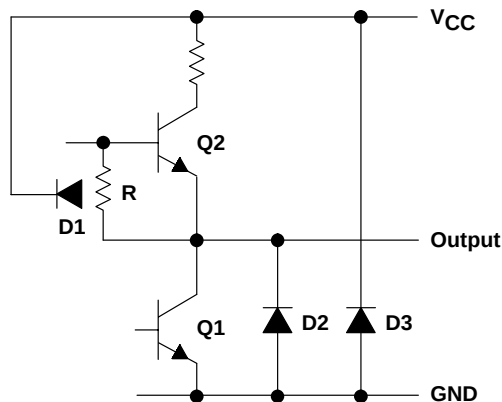


Figure 3. Output of Schottky TTL Devices

If the circuit in Figure 3 is modified for bipolar devices using 3-state outputs, parasitic diode D1 at the output is no longer significant. One possibility is to tie resistor R to GND potential instead of to the output of the circuit (see Figure 4). In this case, the output remains at a high impedance when the supply voltage is switched off.

The outputs of TTL circuits with an open collector are always at a high impedance when the supply voltage is switched off.

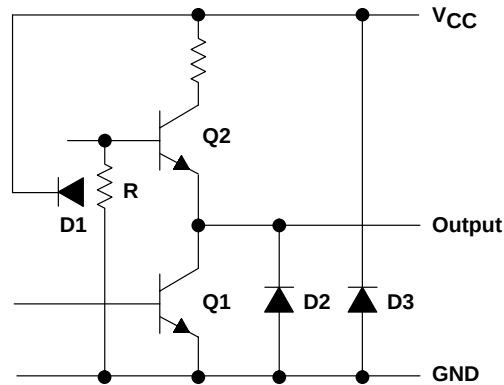


Figure 4. 3-State Output of Schottky TTL Devices

2.1.2 CMOS Circuits

The behavior of CMOS devices when the supply voltage is switched off is essentially determined by the protective circuits at the inputs and outputs. These circuits are intended to protect the device from damage from electrostatic discharge (ESD). Figure 5 shows, in simplified form, the construction of a CMOS circuit with additional diode paths at the input and output. Both the input, via diode D1, and the output, via diode D3, are at a low impedance when the supply voltage is switched off. Diode D3 also exists in circuits having an open drain at the output.

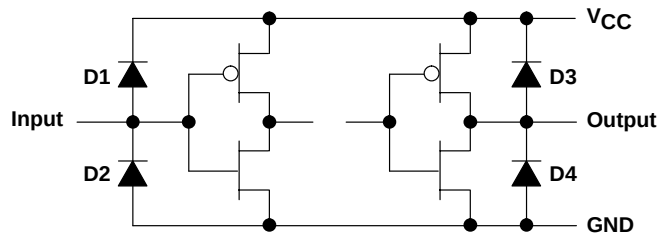


Figure 5. Diode Paths in CMOS Devices

2.2 Behavior With Low Supply Voltages

The behavior of logic devices at low supply voltages is difficult to predict because a detailed knowledge of the internal circuit, including its dimensions, is necessary. An example is the behavior of a noninverting buffer with open-collector outputs (SN7407) when the supply voltage is switched on and off. Figure 6 shows the internal circuit of the SN7407. At supply voltages lower than the forward voltage of the diode path (base-emitter path), all transistors are blocking. Therefore, the output voltage (V_O) first follows the supply voltage (V_{CC}). When the latter reaches about 0.7 V, current flows via resistor R3 into the base of transistor Q4 and the output switches to a low level. If the supply voltage reaches a value of $3 \times V_{be}$, and if a logic high is applied to the input, current flows into the base of transistor Q3 (via transistors Q1 and Q2), which switches. Output transistor Q4 is again switched off, causing the output voltage to rise to the value of V_{CC} . In the previous analysis, the voltage drop necessary for a sufficient base current to switch on the transistor is neglected. TTL devices attain stability with a supply voltage of about 3.5 V, and are fully functional at a typical voltage of 4 V. However, with supply voltages below the minimum specified in data sheets, not all parameters can be attained. This applies to both dc parameters, such as output currents and voltages, and to switching characteristics, such as propagation delay time and maximum clock frequency.

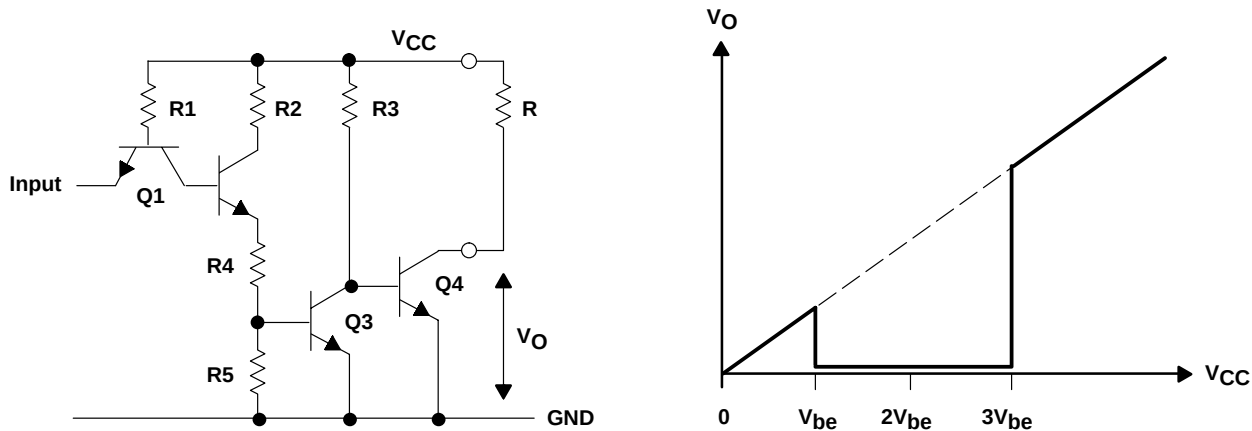


Figure 6. Behavior of a TTL Device at Low Supply Voltages

In a manner similar to TTL devices, CMOS devices also fail to operate at supply voltages below the threshold voltages of the MOS transistors. If the supply voltage is further increased, parts of the circuit are activated (see Figure 6). As previously mentioned, the precise circuit configuration of the device determines the circuit behavior. Full functionality of CMOS devices from the SN74HC family is ensured from $V_{CC} = 2\text{ V}$, whereas the 74AC family can be ensured only from 3 V, although the latter is also stable, with a supply voltage of only 2 V. Since the maximum clock frequency of CMOS devices is dependent on the supply voltage, at a high clock frequency, circuits might not operate reliably during the switch-on or switch-off phases, even though the supply voltage is more than 2 V.

Special design measures have been taken to achieve a defined behavior, even when circuits are operated at supply voltages far below the conditions recommended in data sheets. For example, on bus drivers of the BiCMOS series (SN74ABT/BCT), a voltage-monitoring circuit ensures that the 3-state outputs remain in the high-impedance state at supply voltages below about 3.5 V, regardless of the inputs to these devices. At supply voltages above this threshold voltage, the control inputs (enable and disable) are effective. If a voltage level is applied to these inputs that results in a high impedance at the output, the same state is implemented at the output.

2.3 Supply Voltages Partially Switched Off

In large systems, often part of the voltage supply is switched off, while other parts of the system continue to operate. Then, the critical part of the system is the interface between the device that is supplied and the device that is not supplied with voltage. In such a case, two requirements must be met. First, the part of the system that continues to operate must not be disturbed by the part that is switched off. Second, the switched-off part must not be disturbed by voltages fed back from the operating part.

These requirements can be met with bipolar circuits. As mentioned previously, the inputs of switched-off bipolar circuits are at a high impedance and do not influence parts of the device that are still active. With outputs of switched-off parts of devices that are connected to active parts, only the outputs of bus drivers (e.g., SN74xx240 or SN74xx245) are at a high impedance. Therefore, only such devices should be used for bus lines connecting systems. For unidirectional lines that connect switched-off and active devices, it must be determined in each case whether the operation of the system could be influenced by the outputs being at a low impedance when switched off. If this is not the case, then at this position in the system, any kind of device, including CMOS, can be used.

As mentioned previously, when switching the supply on and off, the logic state of the devices concerned cannot be ensured. Therefore, undefined states can arise during this time at the interfaces and cause malfunction of the system (see Figure 6). The use of SN74ABT/BCT-series bus drivers provides a solution, since the outputs of these parts go into the high-impedance inactive state at supply voltages below about 3.5 V. A difficult situation arises when using CMOS devices. As shown in Figure 5, these parts have protective diodes that are connected to the supply rails at both inputs and outputs. If the supply voltage V_{CC2} of this circuit is switched off (see Figure 7) while the supply voltage V_{CC1} remains switched on, a current (I) flows out of gate G1, via diode D1, into the next circuit. This current can rapidly overload protective diode D1 (the maximum current of the input clamp diodes of CMOS devices is only 20 mA) and destroy the device. Remember that, in general, the next device represents a short circuit and, apart from the output resistance of gate G1, there is no current-limiting circuit element.

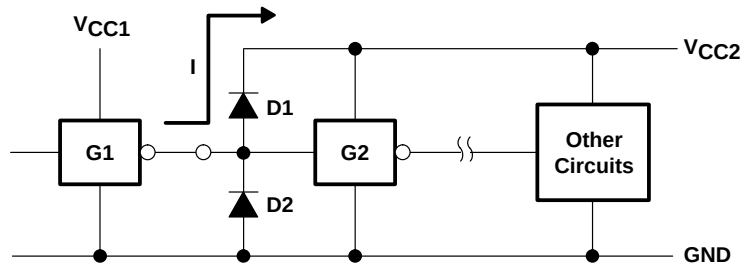


Figure 7. Feeding Back With CMOS Devices

Figure 8 shows recommended design ideas, with reservations, to provide some current limiting. In Figure 8a, the input current of the switched-off device is limited by resistor R. Using this, the input current of the circuit to be protected can be limited to a permissible value. The input current of CMOS devices is extremely low and series resistors of several ohms usually have no negative effect on the function of the part. However, feeding of the next device, via input clamping diode D1, is not prevented entirely.

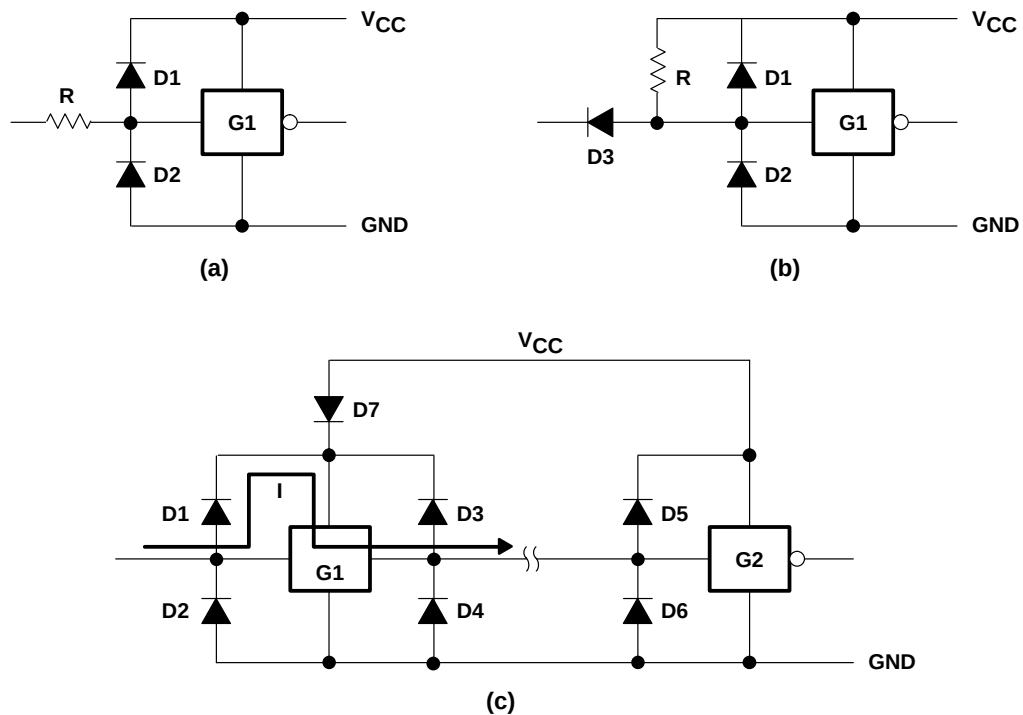


Figure 8. Ideas for Protecting CMOS Devices

In the circuit of Figure 8b, the flow of current into the device to be protected when the supply voltage V_{CC} is switched off, is prevented by diode D3. However, to ensure a high level at the input of gate G1 with normal operation, a pullup resistor is needed, and this significantly increases the power consumption of the CMOS circuit. D3 also shifts the logic level at the input of the gate, and as a result, reduces the noise margin of the circuit. Apart from the noise-margin restriction, this circuit is effective, because it prevents feedback into the switched-off part of the device.

The diode in Figure 8c has no effect if gate G1 has a noninverting function. Even so, the flow of current via clamping diode D1 and the V_{CC} rail of gate G1 into the next circuit is prevented. Instead, the current flows via the output of gate G1, which, in this case, is at a high logic level, and into the following circuit.

2.4 Changing Powered-Up Subsystems

In many applications, to carry out service or repair work without interrupting operation, it must be possible to change individual subsystems. Because of the partial switch off of supply voltage described previously, this is permissible only when circuit design modifications are made that prevent the destruction of semiconductor components and ensure that the operation of the rest of the system is not disturbed.

In the input and output circuits of logic devices, some desired and some parasitic diodes are present. As explained, these components represent additional current paths, and undefined currents may flow into the device, either through the clamping diodes to the inputs and outputs, or through additional parasitic diodes in the devices. To avoid uncontrolled operational states, changing powered-up subsystems is permissible only if the subsystems have a leading GND pin as a reference potential.

If the connection of the GND reference potential is made first when inserting subsystems, and broken only after removing them, the operational state that results when changing subsystems can be limited to the cases previously mentioned. This assumes that parts of the system that have the same reference potential are not supplied with voltage.

The inputs of bipolar logic circuits, including devices in the SN74ABT/BCT series that are in subsystems to be changed, are at a high impedance under all conditions and, therefore, no problems should be expected. The totem-pole outputs of most TTL devices are at a low resistance when the supply voltage is switched off, so when reinserting a subsystem, the line concerned is switched to low, which may be incorrect. Three-state outputs of bipolar devices are at a high impedance when the supply voltage is switched off. However, they can go to a low impedance for a short time during switch on or switch off. This could generate an incorrect logic level because at low supply voltages the internal circuit does not operate properly. The result is that during the change of subsystems, short-duration undefined signals that disturb other systems may appear at the corresponding outputs. This problem can be avoided if devices from the SN74ABT/BCT series are used. With these components, the outputs are switched into the inactive high-impedance state if the supply voltage falls below about 3 V.

The problem of changing subsystems with power supplied can be easily solved, particularly when using devices that include a supply-voltage monitor, but CMOS circuits can be used only under these circumstances with certain restrictions. In this case too, the use of a leading GND pin on the connector is essential. The CMOS inputs of devices on the subsystem to be changed should, in every case, be protected at least with series resistors (see Figure 8a), to prevent excessive currents in the clamping diodes of the input protection circuitry. In extreme cases, depending on the layout of pins on the connector, the current for the complete subsystem could, for a short time, flow through one of these diodes. For the outputs of CMOS devices, no practicable protection circuit can be recommended. Also, the use of protective resistors must be considered to limit the current in the clamping diodes at the output. However, this is not possible in most cases because an unacceptable reduction in the output drive capability would result.

3 Unused Inputs

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used. Such parts should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. A rule that must be observed under all circumstances is:

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating.

The logic level that should be applied to any particular unused input depends on the function of the device. As a result of the input circuits of bipolar devices, a high level is established at open-circuited inputs. The voltage at such an input corresponds to the threshold voltage of the input circuit (about 1.4 V or 1.1 V with devices from the SN74LS family). In a test of the function of such a circuit, this order of voltage at the input, in general, indicates that this circuit is open. CMOS inputs are of such high impedance that the smallest change on the open input can generate any undesired logic level. A slight change of the capacitance at the unconnected input, for example, by bringing the hand close to the package, can so change the effective voltage at the input that a high level can change into a low level, or vice versa. Additionally, for the same reasons mentioned, unconnected inputs may react to all kinds of coupled-in interference voltages, and the behavior of the circuit can no longer be predicted.

With gates, another solution is to connect unused inputs to an input of the same gate that is in use. The function of the device is unaffected. This circuit arrangement can be used equally well with AND (NAND) as with OR (NOR) gates (see Figure 9). Here, connecting the inputs together increases the capacitive load on the driver stage and, with bipolar circuits, also increases the dc current drain.

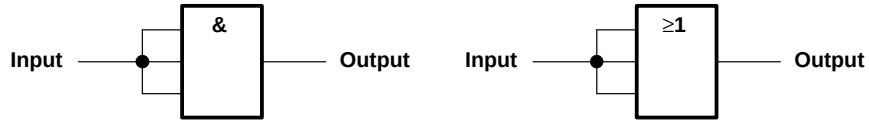


Figure 9. Interconnection of Unused Inputs With AND and OR Gates

In many cases, the simple method shown here cannot be used, especially if the unused inputs are not part of the same gate function. In this case, a defined logic level must be applied to the unused inputs. If a low level is required, the input should be directly connected to GND; if a high level is required, it should be connected with a voltage source corresponding with a high level. In general, this is the positive supply voltage V_{CC} . Figure 10 shows how, in the previously mentioned cases, a fixed potential should be connected to unused inputs. Note that a high level should be applied to the unused inputs of an AND (NAND) function and a low level to unused inputs of an OR (NOR) function.

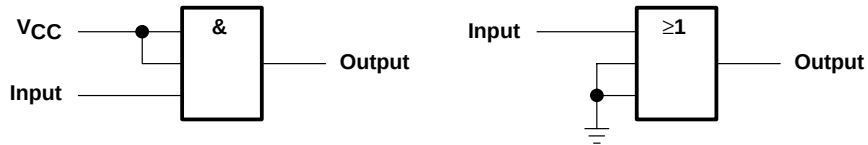


Figure 10. Fixed Potential Connected to Unused Inputs

Devices with multiple-emitter inputs (SN74 and SN74S series) are exceptions. Since no voltage greater than 5.5 V should be applied to the inputs (because if exceeded, the base-emitter junction at the inputs breaks down), the inputs of these devices must be connected to the supply voltage V_{CC} via series resistor R_S (see Figure 11). This resistor should be dimensioned such that the current flowing into the gate or gates, which results from overvoltage, does not exceed 1 mA. But, because the high-level input current of the circuits connected to the gate flows through this resistor, the resistor should be dimensioned so that the voltage drop across it still allows the required high level. Equations 1 and 2 are for dimensioning resistor R_S , and several inputs can be connected to a high level via a single resistor if the following conditions are met:

$$R_{S(\min)} = \frac{V_{CCP} - 5.5 \text{ V}}{1 \text{ mA}} \quad (1)$$

$$R_{S(\max)} = \frac{V_{CC(\min)} - 2.4 \text{ V}}{n \times I_{IH}} \quad (2)$$

Where:

- n = number of inputs connected
- I_{IH} = high input current (typical 40 μA)
- $V_{CC(\min)}$ = minimum supply voltage V_{CC}
- V_{CCP} = maximum peak voltage of the supply voltage V_{CC} (about 7 V)

If part of a device is unused, the unused-input rules should be applied. If, for example, in an application only one flip-flop from a dual flip-flop type SN74ALS74 is used, all inputs of the unused flip-flop should be connected to a defined logic level, which, in this case, could be either low or high.

NOTE:

Unused outputs of a device should not be left unconnected (open).

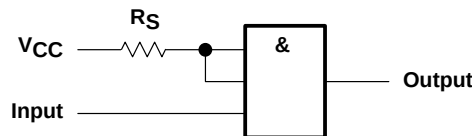


Figure 11. Series Resistor Connected to Unused Inputs of Multiple-Emitter Transistors

4 Excessive Input Currents

All logic devices have protection circuits at outside connections. These diodes, or similar components, are intended to protect the device against destruction by ESD. In addition, clamping diodes at device inputs limit overvoltage and undervoltage resulting from line reflections and divert the currents that flow, in consequence, to either the negative (GND) or positive (V_{CC}) supply rails. Currents that flow in these circuit parts can, under certain circumstances, activate so-called parasitic transistors, which results in incorrect operation of the circuit.

Examples of this are the clamping diodes at the inputs of HCMOS devices, which are intended to limit overvoltages resulting from reflections. These diodes are created with a P-doped region in an N-doped substrate which, in turn, is connected to the positive supply voltage (see Figure 12). Between two adjacent diodes and in conjunction with the substrate, a parasitic PNP transistor is effectively created. A part of the current in one of the two clamping diodes is, therefore, not diverted to the V_{CC} rail but, instead, flows to an adjacent input. The current gain of this transistor is small (about 0.01), so that under normal operating conditions no effect can be expected. If, however, a high positive voltage is applied to the input of a circuit, as in Figure 12, which adapts signal voltages with an amplitude of 24 V to HCMOS circuits, a current flows into the adjacent input, despite the low current gain of the parasitic transistors. The current in the adjacent input may then be sufficient to generate a false input signal. However, destruction or damage to the device (as a result of latch-up) is not likely to occur.

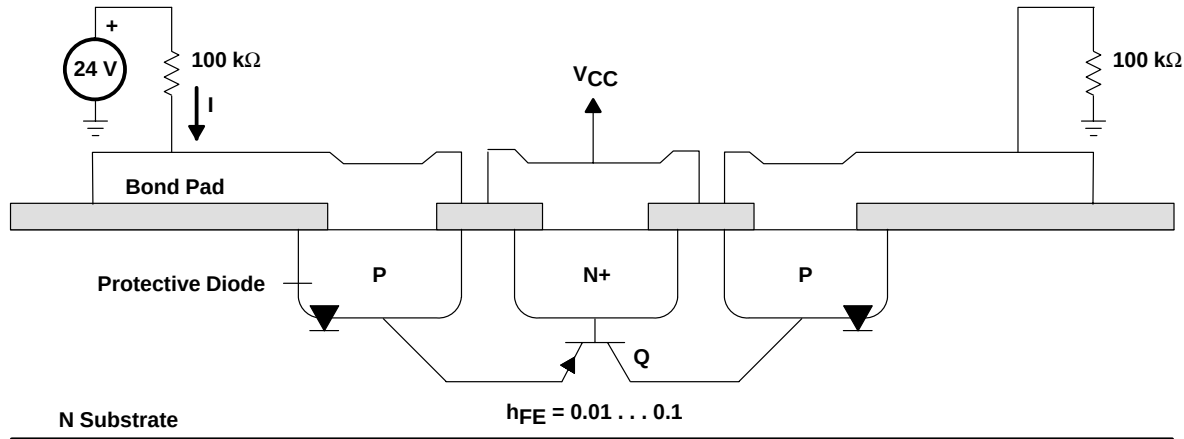


Figure 12. Parasitic Transistors in CMOS Input Stages

Similar effects caused by parasitic transistors also can be observed with bipolar transistors. Figure 13 shows a bipolar input that includes Schottky clamping diodes, realized with an N-doped region covered by a metallic contact. With a small negative input current, the forward voltage of the Schottky diode is about 400 mV, and the current in such an input is diverted, via the diode, to the GND pin of the device. If this current is increased, the forward voltage of the diode increases accordingly, and at a certain amplitude exceeds 700 mV. At this point, the silicon diode (which results from the N-doped region and the P-doped substrate under it, connected to the GND of the device) conducts. Here, also, a parasitic transistor is activated, whereby the whole adjacent N-doped region, comprising the collectors of active transistors, functions as a collector. This collects together a part of the current circulating in the substrate. If the amplitude of the negative current is sufficient, incorrect operation of the circuit can be expected.

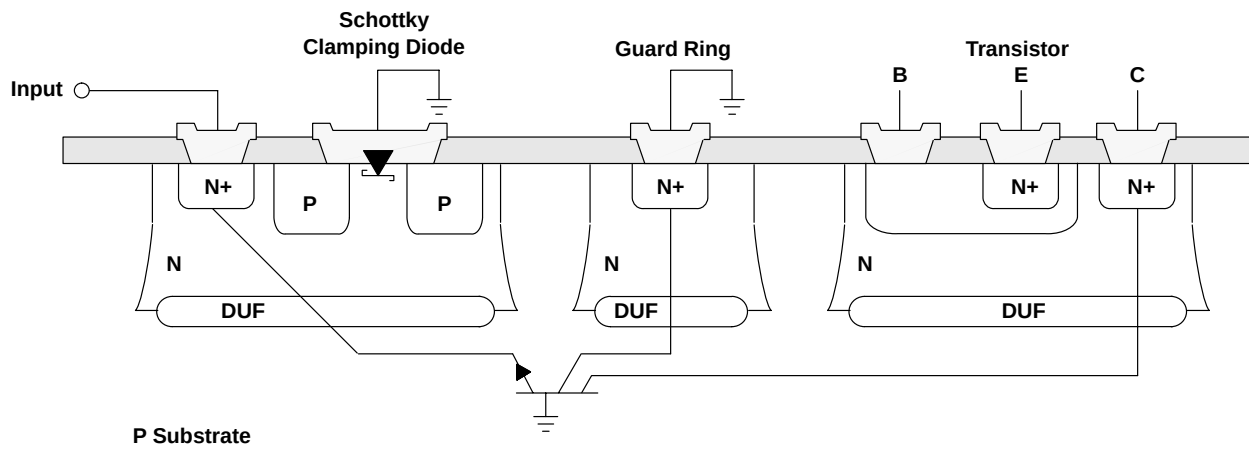


Figure 13. Parasitic Transistors in Bipolar Input Circuits

Negative voltage undershoot of considerable amplitude must be expected in practical operation of logic devices. Therefore, the semiconductor manufacturer must take the steps necessary to ensure reliable operation. Guard rings, which are placed in a ring around the circuit in question (see Figure 13), ensure reliable operation. In this example, these guard rings consist of an N-doped region connected to GND potential, which has the effect of an additional collector for the parasitic transistors, collecting the majority of the current circulating in the substrate and diverting it to GND potential. These guard rings are constructed so that a negative input current of $I_{IN} = -60 \text{ mA}$ with a duration $t = 100 \text{ ns}$ does not cause an incorrect function of the circuit. These values are again reflected in Figure 14. Here, a TTL device with a signal amplitude of 3 V drives a 10-meter-long coaxial cable with a characteristic impedance of $Z = 50 \Omega$, at the end of which the input circuitry (with clamping diode) of the device in question is connected. High-amplitude current pulses, such as those generated by line reflection, are captured with this measuring setup.

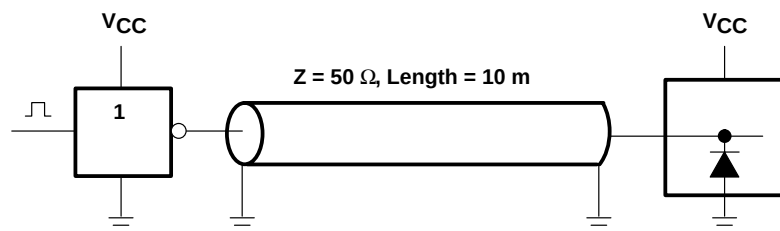


Figure 14. Setup for Generating an Undershoot Pulse ($I = -60 \text{ mA}$, $t = 100 \text{ ns}$)

Negative input currents with an amplitude of only a few milliamperes, but with a duration of several microseconds, can cause incorrect operation of the device. Since the transit frequency of the parasitic transistors is only about 1 MHz, the circuit and dimensioning of guard rings are simplified. A certain duration of the undershoot pulse is necessary to switch on the parasitic transistors, and possibly to cause abnormal operation of the circuit.

5 Transition Times

Correct operation of the circuit can be ensured only if the rise and fall times of the signal at the input do not exceed certain values. With CMOS devices (SN74HC and 74AC/SN74AC), these values are given in the data sheets. For devices from the SN74HC series, a rise and fall time (transition time) less than 500 ns is specified at $V_{CC} = 4.5 \text{ V}$, while for ACL devices (74AC/SN74AC series), a value of 10 ns/V is given. Figure 15 shows this in more detail.

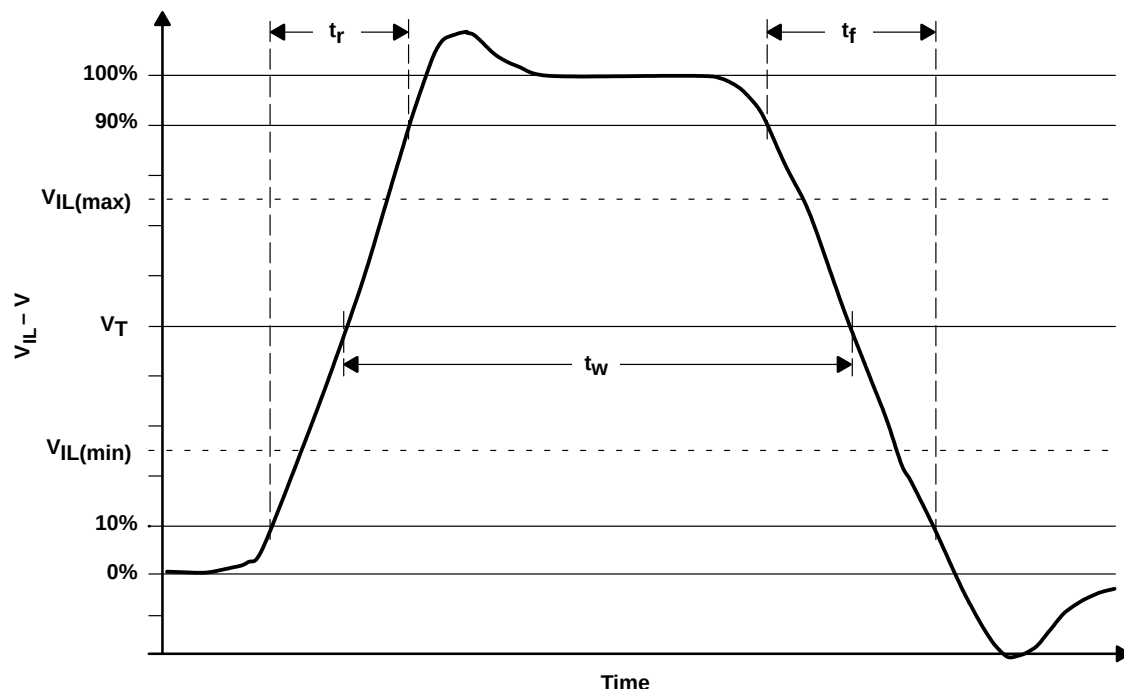


Figure 15. Definition of Signal Amplitude and Pulse Width

The signal amplitude is specified as the difference between the two stable signal levels for high (V_H) and low (V_L); overshoot and undershoot of the signal are not taken into account. The difference $V_H - V_L$ is taken as 100% of the amplitude. The rise time of the signal is defined as the time taken to rise from 10% to 90% of the full amplitude; similarly, the fall time is the time taken to fall from 90% to 10% of the amplitude. The pulse width (t_w) of a signal is measured at 50% of the amplitude. However, these definitions must be used for digital circuits with certain qualifications because, in most cases, the switching threshold (V_T) of the input is not 50% of the amplitude. So, the level needed by the circuit must be considered and, from this, the required signal waveform derived.

The values of voltage that are decisive for the correct operation of the part are the maximum permissible low voltage at the input $V_{IL(max)}$ and the minimum necessary high voltage at the input $V_{IH(min)}$. The following example applies for a device from the SN74HC series:

$$V_{IL(max)} = 0.9 \text{ V}$$

$$V_{IH(min)} = 3.15 \text{ V at } V_{CC} = 4.5 \text{ V}$$

However, the rise and fall times are specified between 10% ($0.1 \times V_{CC} = 0.45 \text{ V}$) and 90% ($0.9 \times V_{CC} = 4.05 \text{ V}$) of the amplitude. The voltage waveform below 0.9 V (low level) and above 3.15 V (high level) has no influence on the function of the device, as long as the absolute maximum ratings are not exceeded. Therefore, it is better to define rise and fall times over the range between $V_{IL(max)}$ and $V_{IH(min)}$, which must be adhered to in order to ensure correct functioning of the device. From the amplitude (4.5 V) and the rise time specified in the data sheet ($t_r = 400 \text{ ns}$), the transition time (dt/dv) rate can be derived as follows:

$$dv/dt = \frac{400 \text{ ns}}{(0.9 \times V_{CC}) - (0.1 \times V_{CC})} = \frac{400 \text{ ns}}{3.6 \text{ V}} = 110 \text{ ns/V} \quad (3)$$

The input signal must cross the region between $V_{IL(max)}$ and $V_{IH(min)}$ (and vice versa) at the transition rate or faster. This value is comparable to the transition rate given in 74AC-series data sheets of $dt/dv = 10 \text{ ns/V}$. The pulse width (t_w) is measured at the actual threshold voltage (V_T) of the circuit and with CMOS devices at 50% of the amplitude. Bipolar and TTL-compatible CMOS devices have a switching threshold that is shifted considerably from the middle of the signal amplitude. This shift must then be taken into account when determining the pulse width. Table 1 shows the necessary minimum transition rise/fall rates for various logic families.

Table 1. Required Minimum Input Rise/Fall Rates for Logic Families

SERIES	V _{CC} (V)	V _{IL(max)} (V)	V _{IH(min)} (V)	V _T (V)	dt/dv (ns/V)
SN74	4.75–5.25	0.8	2	1.4	15
SN74LS	4.75–5.25	0.8	2	1.4	15
SN74S	4.75–5.25	0.8	2	1.4	15
SN74ALS	4.5–5.5	0.8	2	1.4	15
SN74AS	4.5–5.5	0.8	2	1.4	15
SN74F	4.5–5.5	0.8	2	1.4	15
SN74HC	2	0.3	1.5	1.4	625
	4.6	0.9	3.15	2.25	110
	6	1.2	4.2	3	80
SN74HCT	4.5–5.5	0.8	2	1.4	125
74AC	3	0.9	2.1	1.5	10
	4.5	1.35	3.15	2.25	10
	5.5	1.65	3.85	2.75	10
74ACT	4.5–5.5	0.8	2	1.4	10
SN74BCT	4.5–5.5	0.8	2	1.4	10
SN74ABT	4.5–5.5	0.8	2	1.4	5/10
SN74LV	2.7–3.6	0.8	2	≈1.5	100
SN74LVC	2.7–3.6	0.8	2	≈1.5	5/10
SN74LVT	3.0–3.6	0.8	2	1.4	10

The values for the transition rise/fall rates (dt/dv) are understood to be a level that ensures the function of individual components if the circuit is controlled with these rates. This does not necessarily mean that the device operates correctly under all circumstances in a large system. Figure 16 shows this in more detail. It shows two D-type flip-flops connected as a two-stage shift register. The first flip-flop is the TTL-compatible device 74ACT11074 (input threshold voltage = 1.5 V), but the second flip-flop (74AC11074) has CMOS-compatible inputs with an input threshold voltage of $0.5 \times V_{CC}$.

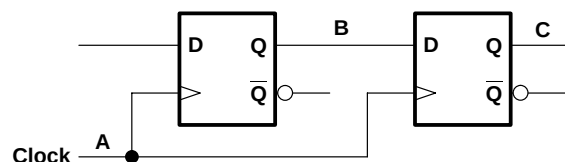


Figure 16. Two-Stage Shift Register

According to Table 1, devices from the 74ACT series must be controlled with a transition rate of at least 10 ns/V, if the function of individual parts is to be ensured. If, however, the behavior with time of the circuit is analyzed, it is found that the shift register does not behave as required (see Figure 17). When the clock signal reaches 1.5 V (having the required transition rate of 10 ns/V), the first flip-flop switches. The output typically reacts about 5 ns later. Only after another 5 ns does the voltage of the clock signal reach a value of 2.5 V, so that the second flip-flop switches. As a result of this late triggering, it accepts incorrect information: namely, the state that the first flip-flop has reached after the switching clock edge, and not the state that the flip-flop had before the clock edge.

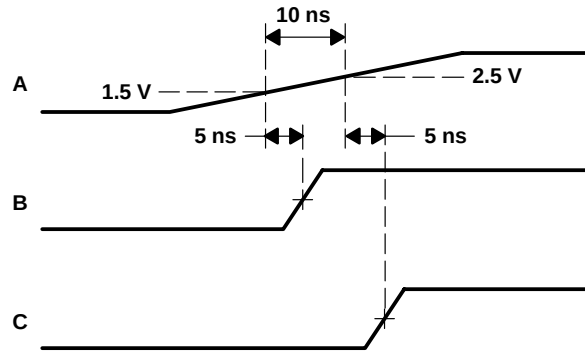


Figure 17. Incorrect Operation of a Shift Register

Under typical operating conditions, the circuitry would, however, operate correctly. The output signals of advanced CMOS devices have a rise time < 5 ns (typical 2 ns). At the clock signal, a voltage change of 1.5 V to 2.5 V takes place in about 1.25 ns. A 74ACT11074 flip-flop has a minimum delay time of 1.5 ns, and under these circumstances correct functioning of the circuit is ensured.

Similarly, problems need not be expected when using devices from other families under similar conditions, as long as the signals have nominal rise and fall times. Under extreme conditions (for example, with unfavorable line routing), the switching times can be so lengthened that faults of the kind just described may occur.

6 Propagation Delay Times

6.1 Propagation Delay Times With Several Outputs Switching Simultaneously

The propagation delay times of circuits given in data sheets apply when only one output switches at a time. The reason for this is that the production equipment used to test circuits can test only one transmission channel at a time. If several outputs switch simultaneously, the propagation delay times given in data sheets can be used only with reservations. The reason for this is that the package inductances (L_p) of the supply-voltage lines, as well the output lines (see Figure 18), have a significant influence on the circuits and, thus, on the delay times. These inductances have the effect that the current in the power supply lines, and consequently in the output of the device, has a limited rate of rise. For this reason, when several outputs switch simultaneously, only a limited output current is available.

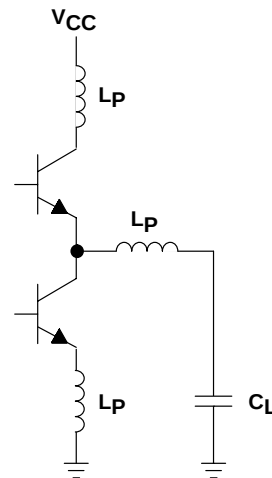


Figure 18. Inductances in the Lines Supplying a Package

Figure 19 shows the influence on the delay time of the number of outputs that are switched simultaneously. When packages having two supply-voltage pins (V_{CC} and GND) are used, as is the case with the majority of digital logic devices, an increase of the delay time of 150 ps to 200 ps for each additional output that is simultaneously switched must be expected. With an octal bus driver, such as an SN74xx240, the delay time is increased by 1 ns to 1.4 ns when all eight outputs switch simultaneously. In those cases where there are several supply-voltage pins, such as the advanced CMOS devices in the 74ACT series from Texas Instruments (TI), the result influences speed of the circuit. As shown in Figure 19, the loss of speed of the components is halved when several outputs switch simultaneously.

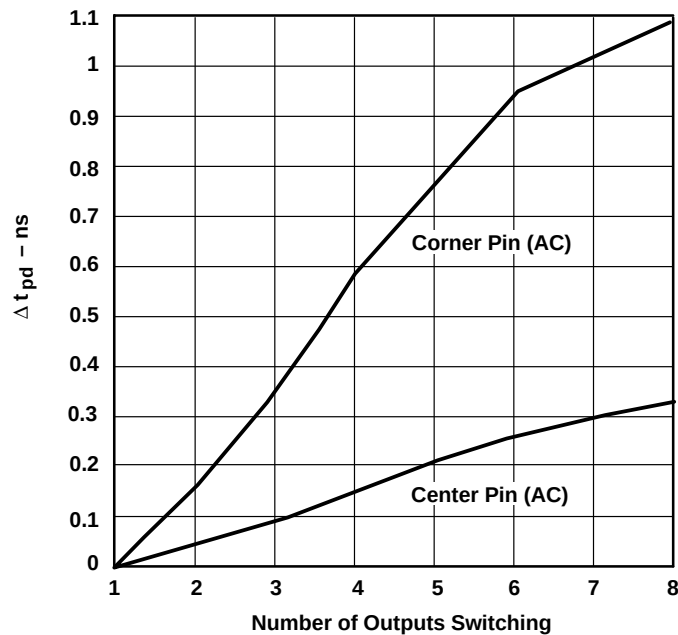


Figure 19. Increase of the Delay Time When Several Outputs Are Switched Simultaneously

With bus drivers and also VLSI circuits that have more than eight outputs that switch simultaneously, an appropriate number of additional supply-voltage pins are provided. A good example is given by the Widebus™ circuits from TI, which are bus drivers with 16, 18, or 20 outputs. To keep the loss of speed (because of so many outputs) within limits, about 25% of all pins of these devices are reserved for the provision of supply voltage. Figure 20 shows the increase of the delay time of a 74AC16240 as a function of the number of outputs that are switched simultaneously.

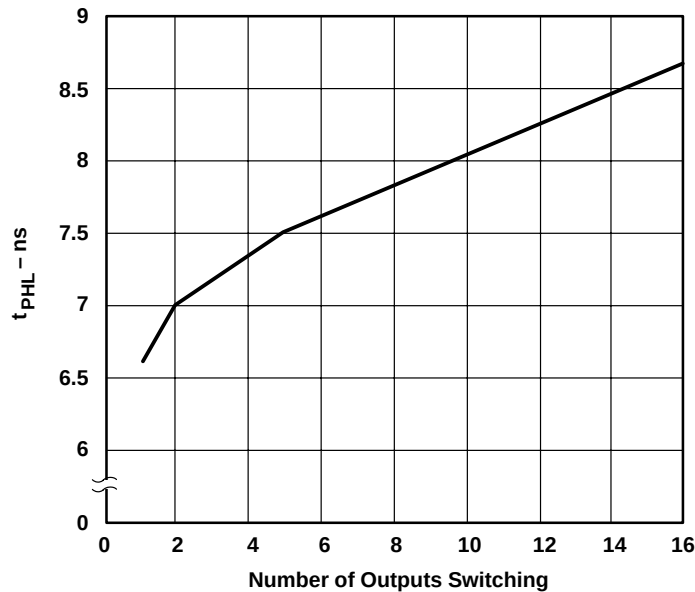


Figure 20. Increase of the Propagation Delay Time With a Widebus™ Circuit (74AC16240)

6.2 Propagation Delay Times With Negative Undershooting at the Outputs

With bipolar circuits, negative voltages caused by undershooting can influence the function of the device. Figure 21 shows this effect. This circuit represents the output stage of a bus driver, which should be in an inactive and high-impedance state. Active bus driver U1 switches the line between the two devices from a high to a low level. As a result of an inadequate termination of the line, there is a negative undershoot on the line, which causes a current (I_X) to flow in the internal circuit of the output stage. This current flows via the collector-base diode of transistor Q5 and Schottky diode D1, in parallel with it and via transistor Q1 to the base node of transistor Q2. Now this node is clamped to a low level. If this output stage should again be switched to the active state (output enable switches from low to high), the output does not follow until the capacitance of the bus line is charged through resistor R to the extent that the collector base diode of transistor Q5 is turned off again, which takes, typically, 5 ns to 10 ns. Apparently, the delay time to again switch on the output stage is increased by approximately this amount.

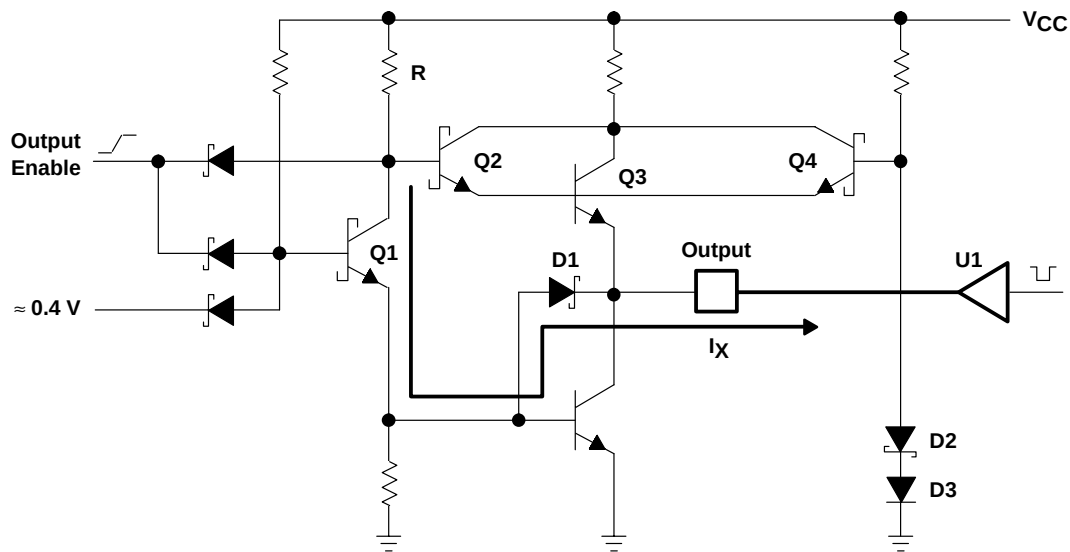


Figure 21. Currents in the Output Stage of a Bus Driver With Negative Undershoot

To prevent this delay, a clamping circuit (D2, D3, and Q4 in Figure 21) is integrated into modern bus drivers. This ensures that, should the output voltage go below -0.3 V , transistor Q3 switches on the output stage and the current I_X is diverted to the positive supply-voltage rail V_{CC} . With ABT devices, clamping is unnecessary and a different circuit that can be more effective is used.

6.3 Propagation Delay Times With Large Capacitive Loads

In digital logic device data sheets, propagation delay times are specified with a capacitive load of 50 pF (15 pF on older logic families). This value represents the capacitive load of the test circuit on the output of the device being tested. This value is also the capacitive load when the output drives five inputs of other circuits and this assumes that the length of the connecting lines is only a few centimeters, as is typically the case on printed circuit boards (PCBs). With such short lines, the first assumption is that the line itself behaves like a capacitor, which additionally loads the output and influences the propagation delay time accordingly. However, with long lines, this assumption leads to errors, because the signal delay is actually determined by the propagation speed of the electrical wavefront along the line. In fact, the propagation delay time of the device is determined by the loading of the output, that is, by the characteristic impedance of the line to which it is connected, not by its length or capacitance. When driving a line terminated at its end with a resistance of $100\ \Omega$, and lengths of 0 (resistor connected directly to the output), 1 m , and 11 m (see Figure 22), an SN74LS00 device has the output waveforms shown in Figure 23. The three resulting output signals are shown staggered, and are practically identical, i.e., the propagation delay time of the device is not influenced. The length of the line and the resulting signal propagation time (5 ns/m) influence the delay time of the system. The propagation time of the wave along an 11-m transmission line is 55 ns . Add the propagation delay time of the SN74LS00 of about 10 ns for a total delay of 65 ns .

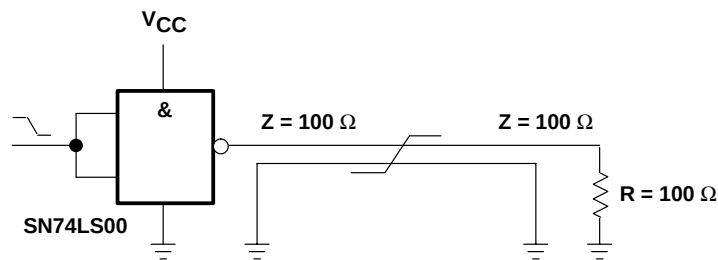


Figure 22. Measurement Setup

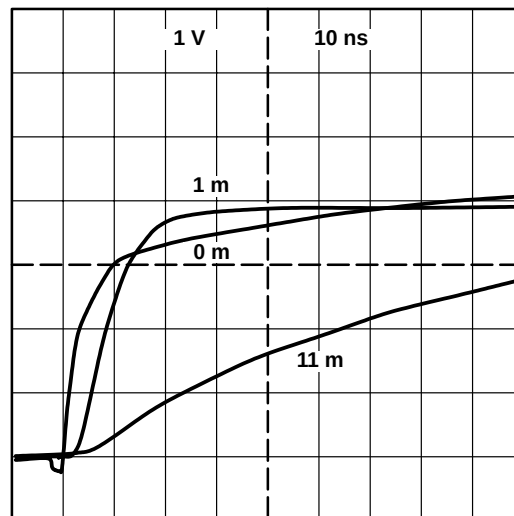


Figure 23. Waveforms for Various Line Lengths

If the capacitive load connected to the output of a device is represented as a single capacitor, the resulting propagation delay time can be calculated. A purely capacitive load can be assumed if the output of the device controls a MOS power transistor with a relatively large input capacitance. To a first approximation, this assumption is correct if an output drives adjacent inputs over a line length of only a few centimeters. The propagation delay times given in data sheets consider the following:

- Propagation delay time through the internal circuitry of the device
- Delay resulting from the switching time of the output stage
- Time needed to charge and discharge the capacitance of the load (typically 50 pF)

The first two considerations are independent of the load that is connected. The last consideration must account for the actual load, of which a load capacitance of $C_L = 50$ pF (15 pF) is already given in data sheets. The time taken to charge the additional capacitance is determined by the current that the device is able to deliver. For the high level, this value can be deduced indirectly from the data sheet. Figure 24 shows the relevant part of the circuit of a bipolar output stage and the resulting output characteristics.

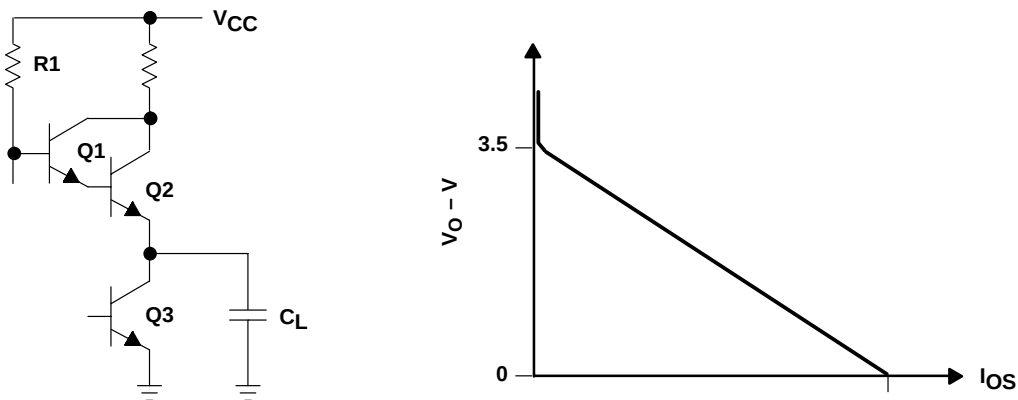


Figure 24. Bipolar Output Stage With Output Characteristics at a High Level

The short-circuit current of the output, when at a high level, is determined by the resistance (R_1) and the saturation voltage of Darlington transistors Q1 and Q2 with collector-path resistance. Using the following equation, the internal resistance (R_O) of a circuit can be determined from the open-circuit output voltage (typically 3.5 V) and from the short-circuit current (I_{OS}) given in the data sheet:

$$R_O = \frac{3.5 \text{ V}}{I_{OS}} \quad (4)$$

With circuits that use MOS transistors in their output stages (SN74HC and 74AC/SN74AC), the output current is determined by the size of the transistors and the potential difference between gate and source. Since there is no linear relationship between this voltage and the output current, only an approximate indication of the output resistance can be made.

Table 2 shows I_{OS} and R_O for the most important device types.

Table 2. Short-Circuit Current and Internal Resistance of Logic Families

TYPE	SHORT-CIRCUIT CURRENT I_{OS} (mA)	INTERNAL RESISTANCE R_O (Ω)
SN7400	35	50
SN7440	45	75
SN74LS00	35	100
SN74LS40	65	53
SN74LS240	70	50
SN74S00	65	53
SN74S40	140	25
SN74S240	60	58
SN74ALS00	50	70
SN74ALS40	60	58
SN74ALS240	100	35
SN74ALS1000	120	29
SN74AS00	100	35
SN74AS240	140	24
SN74AS1000	160	21
SN74F00	85	41
SN74F40	140	25
SN74F240	140	25
SN74BCT240	140	25
SN74BCT25240	700	5
SN74ABT240	120	29
SN74HCT00	60	40–120
SN74HCT240	80	30–100
74ACT11000	220	4–25
74ACT11240	220	4–25
SN74LV00	35	35–100
SN74LV240	55	25–80
SN74LVC00	85	16–40
SN74LVC240	85	16–40
SN74LVT240	400	8

The typical output voltage of a bipolar device at a low level is about $V_{OL} = 0.3$ V. The increase of the delay time resulting from the capacitive load (C_L) is determined by the time until the external load capacitance has been charged by an external voltage source from V_{OL} to the threshold voltage of the circuit, typically $V_S = 1.5$ V. The external voltage source is described by an internal voltage (V_{OH}) and an internal resistance (R_O). In this way, the delay time (t_d) resulting from the load capacitance can be calculated from the following equation:

$$t_d = \ln \frac{V_{OH} - V_{OL}}{V_{OH} - V_S} \times R_O \times C_L = \ln \frac{5.5 \text{ V} - 0.3 \text{ V}}{3.5 \text{ V} - 1.5 \text{ V}} \times R_O \times C_L = 0.5 \times R_O \times C_L \quad (5)$$

Figure 25 shows the waveform of the positive edge at the output of a gate (SN74LS00) with various values of capacitive loads ($C_L = 10 \text{ pF}$, 56 pF , and 616 pF). As expected, the rise time at the output and the resulting increase of the propagation delay time are determined by the time constant $R_O \times C_L$.

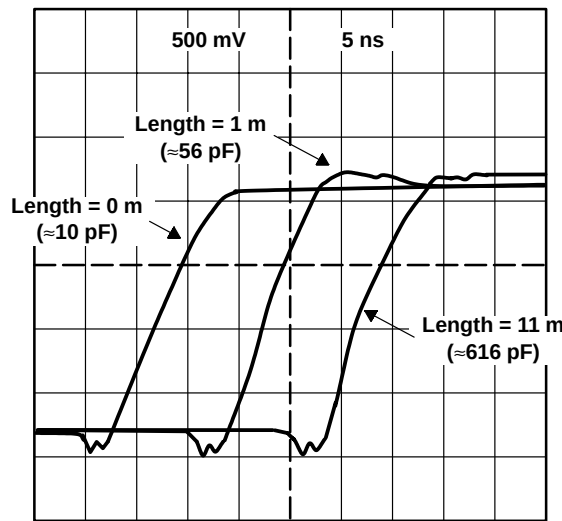


Figure 25. Waveform at SN74LS00 Output ($C_L = 10 \text{ pF}$, 56 pF , and 616 pF)

The values for the low level of a bipolar device cannot be taken directly from data sheets. Transistor Q3 in Figure 24 is responsible for the output current I_{OL} . As with all semiconductor components, this parameter is nonlinear, and is influenced by the distribution of components in the circuit on such parameters as current gain, conductance, and resistance values. For this reason, only a rough calculation of the actual output current at low level is possible. As a first approximation, the internal resistance of the circuit at low level is lower than at high level. It follows that, in the worst case, the increase of the delay time of the negative edge is always smaller than that of the positive edge (see equation 5). The precise value must be determined in individual cases by measurement.

6.4 Input and Output Capacitances of Digital Devices

All digital devices capacitively load the outputs of the circuits driving them. The input and output capacitances are given in Table 3. These are typical average values for the logic families shown. Different circuit configurations are used within a family, depending on the function and application. Therefore, wide variations from the values given in data sheets can occur with individual devices. In specific cases for new families, the values given in data sheets should be taken as a basis. If this data is not available, for example with older families, the user must make appropriate measurements if more precise values are needed.

The capacitances given in Table 3 are measured at the following voltages:

- Bipolar devices: $V = 2.5 \text{ V}$
- CMOS devices: $V = 0 \text{ V}$ and $V = 2.5 \text{ V}$

Table 3. Capacitances of Digital Devices

FAMILY	INPUT CAPACITANCE (pF)	OUTPUT CAPACITANCE (pF)	
		OPEN-COLLECTOR OUTPUT†	BUS DRIVER
SN74	3	5	–
SN74LS	3.5	3.5	5
SN74S	3.5	3.5	9
SN74ALS	2	4	5
SN74AS	4	–	10
SN74F	5	5	9
SN74HC	3	3	9
74AC/SN74AC	4	–	10
SN74BCT	6	–	12
SN74ABT	4	–	8
SN74LV	3	–	8
SN74LVC	4	–	8
SN74LVT	4	–	8

† Open-collector output of gates and other devices with low drive capability (e.g., SN74xx03). Open-collector outputs of bus drivers have the same output capacitance as totem-pole (3-state) outputs.

7 Bus Contention

If several bus drivers with 3-state outputs are connected to a single bus, it often cannot be ensured that during the time when switching from one bus driver to another, both are not simultaneously active for a short time. For this short time, a short circuit of the outputs exists, resulting in an overload of the circuit. This situation is known as *bus contention*.

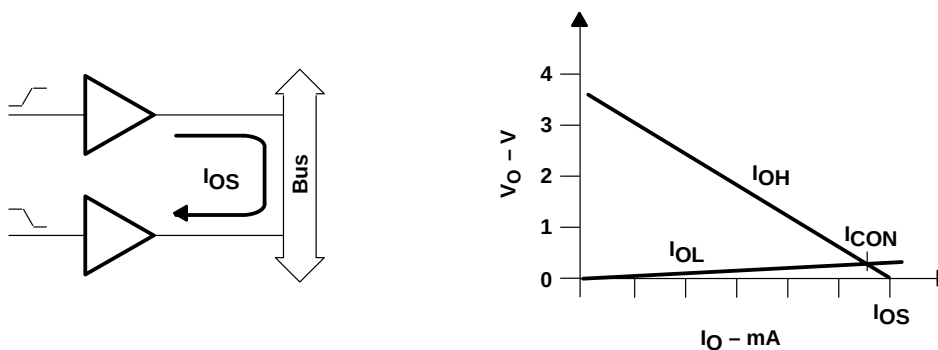


Figure 26. Determining the Short-Circuit Current With Bus Contention

The currents that result from bus contention can be calculated by means of the output characteristics of the devices (see Table 2). As shown in Figure 26, the short-circuit current (I_{OS}) is limited by the high-output current of the devices involved in bus contention. With bus drivers having an output current of $I_{OL} = 64 \text{ mA}$ (SN74AS, SN74F, SN74BCT, SN74ABT, or SN74LVT), a current $I_{OS} = 120 \text{ mA}$ flows in such a case. The power dissipation (P_{conl}) of the output supplying the low level, as shown below, can be ignored.

$$P_{conl} = V_{OL} \times I_{OS} = 0.5 \text{ V} \times 120 \text{ mA} = 60 \text{ mW} \quad (6)$$

Even if all eight outputs of a bus driver are involved in bus contention, the total power dissipation is less than 500 mW. However, the situation is different at the outputs supplying the high level. In this case, the short-circuit power dissipation (P_{conh}) of each output is as follows:

$$P_{\text{conh}} = (V_{\text{CC}} - V_{\text{OL}}) \times I_{\text{OS}} = 4.5 \text{ V} \times 120 \text{ mA} = 0.54 \text{ W} \quad (7)$$

If all eight outputs of a bus driver are involved in this bus contention, the total power dissipation is about 5 W. With Widebus circuits, it is 10 W and more.

To analyze the situation inside a device under these extreme conditions, one has to know that the heat caused by this power dissipation is not immediately spread over the total chip. Rather, one has to consider a certain propagation speed of the heat, which is about $1 \mu\text{m}/\mu\text{s}$. This means that during bus contention with a duration of only a few nanoseconds, the heat is not distributed over all the chip. In the first moment, the affected component inside the device (the transistor or resistor) heats up. The resulting increase in temperature can be calculated by knowing the volume of the component in question and the thermal capacitance of silicon. By using the output stage of an ABT device (see Figure 27), this is shown in detail. Also, all voltages are shown in this circuit diagram that apply when the output, which should provide a high level, is forced to 0.5 V externally.

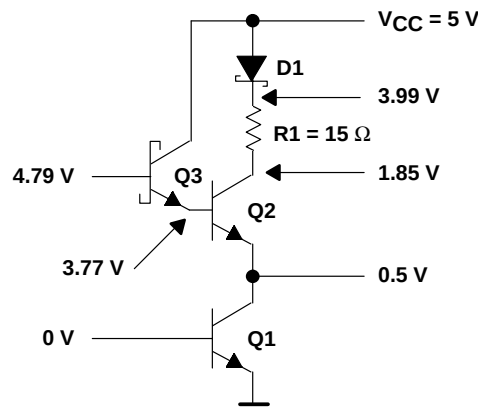


Figure 27. ABT Output-Stage Circuit Diagram

Table 4 shows the conditions in this output stage during bus contention. When calculating the volume of the single components, only that volume was considered that is related to the function of the component. For example, a transistor's total area was taken into account, but only the junction width, where the heat is dissipated, was considered as the component's height.

Table 4. Output-Stage Conditions During Bus Contention

	VOLTAGE V (V)	CURRENT I (mA)	POWER DISSIPATION P (W)	VOLUME V (μm^3)	POWER DISSIPATION/ VOLUME ($\text{W}/\mu\text{m}^3$)
D1	1.01	142	0.156	3200	46×10^{-6}
R1	2.14	142	0.304	3840	79×10^{-6}
Q2	1.35	142	0.192	495	38×10^{-3}

According to this analysis, the highest power dissipation per volume unit is found in transistor Q2. This is because the junction width of only 0.5 μm was considered as the height of this component. Using equation 8, calculate the temperature increase ($\Delta\theta$):

$$\Delta\theta = \frac{P \times t}{V \times c_p} \quad (8)$$

Where:

- c_p = heat capacitance of silicon = $1.631 \times 10^{-3} \text{ Ws/Kmm}^3$
- P = power dissipation
- t = time
- V = volume

Considering a propagation speed of the heat of 1 $\mu\text{m}/\mu\text{s}$ and a junction width of 0.5 μm , one can assume that during the first 500 ns of bus contention the heat is not distributed over the chip, but stays in the transistor junction. Under this condition, $\Delta\theta$ is calculated as follows:

$$\Delta\theta = \frac{0.192 \text{ W} \times 500 \text{ ns}}{495 \mu\text{m}^3 \times 1.631 \times 10^{-3} \frac{\text{W} \times \text{s}}{\text{K} \times \text{mm}^3}} = 119 \text{ K} \quad (9)$$

Short bus contention, with a duration of a few, or of a few tens of nanoseconds, causes a temperature increase of the component in question of about 10°C. Therefore, a degradation of the reliability of the component is unlikely. Furthermore, in well-designed systems, the period of bus contention is high compared to the duration of a single instance of bus contention (period:duration > 10:1). Conservatively, the mean chip temperature should be calculated to ensure that this temperature does not increase beyond 150°C. Beyond this temperature, the thermal expansion coefficient of the plastic material of the package becomes different from the expansion coefficient of silicon. This fact is likely to lead to a mechanical stress at high temperatures, which can result in failure of the bond wire.

The total power dissipation (P_T) of a bus driver is calculated by the following equation:

$$P_T = P_O + (P_S \times t_s + P_C \times 2\tau + P_{\text{con}} \times t_{\text{con}}) \times f \times n \quad (10)$$

Where:

- f = frequency
- n = number of outputs at which bus contention occurs
- P_{con} = power dissipation during bus contention
- P_C = power dissipation when discharging the bus capacitance
- P_O = quiescent power dissipation
- P_S = power dissipation resulting from current spikes when output switches
- t_{con} = duration of bus contention
- t_s = duration of current spike
- τ = signal propagation time on the bus

The power dissipation of a bus driver is calculated in a practical example in accordance with the following assumptions:

- Circuit: SN74F245
- $P_O = 0.45 \text{ W}$ (from data sheet)
- $P_S = 5 \text{ V} \times 30 \text{ mA} = 0.15 \text{ mW}$ with $t_s = 5 \text{ ns}$ (measured)

To calculate the power dissipation (P_C) that occurs when charging the capacitance of the bus line, the voltage waveform at the output with the given load (the line impedance) must be known. The easiest way to determine this is to use the Bergeron diagram. With a line impedance of $30\ \Omega$, a stable state is reached after double the time of the signal propagation with a positive edge. That is, for this time, a current is supplied into the line from the driver circuit. The amplitude of the preceding waveform and the output voltage of the circuit is about $V_O = 2\text{ V}$. The power dissipation during this time and under these load conditions is calculated as follows:

$$P_C = (V_{CC} - V_O) \times \frac{V_O}{Z_O} = (5\text{ V} - 2\text{ V}) \times \frac{2\text{ V}}{30\ \Omega} = 0.2\text{ W} \quad (11)$$

The signal propagation time on a backplane in a 19-inch rack (wire length about 40 cm) is $\tau = 10\text{ ns}$.

Further, assuming a bus cycle time of 100 ns ($f = 10\text{ MHz}$), a bus-contention duration of 10 ns, and that all eight outputs of the device are involved, the resulting total power dissipation is calculated as follows:

$$\begin{aligned} P_T &= 0.45\text{ W} + (0.15\text{ W} \times 5\text{ ns} + 0.2\text{ W} \times 2 \times 10\text{ ns} + 0.53\text{ W} \times 10\text{ ns}) \times 10\text{ MHz} \times 8 \\ &= 0.45\text{ W} + (0.75\text{ nW/s} + 4\text{ nW/s} + 5.3\text{ nW/s}) \times 10\text{ MHz} \times 8 \\ &= 1.29\text{ W} \end{aligned} \quad (12)$$

This power dissipation results in a rise of the temperature of the chip, which, in turn, influences the reliability of the device. The chip temperature can be calculated as follows:

$$T_J = T_A + P_T \times R_{\Theta JA} \quad (13)$$

Where:

$R_{\Theta JA}$ = thermal resistance of package
 T_A = ambient temperature
 T_J = chip temperature

Table 5 shows the typical thermal resistance of the packages, which are mostly used for digital devices. These must be considered as typical values, because a number of factors determine the actual value, including chip size, lead-frame material, composition of the plastic, ambient air flow, and thermal properties of the circuit board. The values given apply if the device is soldered onto a PCB.

Table 5. Thermal Resistance of Plastic Packages in Still Air

NO. OF PINS	THERMAL RESISTANCE (°C/W)	
	DL PACKAGE	SO PACKAGE
14	86	117
16	80	110
20	78	95
24	73	85

According to Table 5, the thermal resistance of a 20-pin DL package is $R_{\Theta JA} = 78^\circ\text{C/W}$. This means that, in equation 8, the chip temperature would be about 100°C above the ambient temperature. The chip temperature must not be allowed to exceed 150°C , because the reliability would be reduced significantly. Therefore, the maximum permissible ambient temperature is, in this case, $150^\circ\text{C} - 100^\circ\text{C} = 50^\circ\text{C}$.

In cases in which bus contention can occur, which is in most bus applications, power dissipation is of particular importance. There is usually nothing that can be done about dynamic conditions (the frequency of operation) without adversely affecting the performance of the system. Also, the overlap of operating states cannot always be prevented if worst-case conditions are taken into account. However, bus contention of a duration of a few, or of a few tens of nanoseconds should not be a problem. The choice of the most suitable components allows control of the quiescent power dissipation. With fast bipolar logic families (SN74S, SN74AS, and SN74F), the permissible total power dissipation might be exceeded because of their high quiescent power dissipation. Better, in this respect, are the SN74LS and SN74ALS series because, with their lower quiescent-current requirements, bus contention does not result in overdissipation in most cases. Even better are devices from the BiCMOS series and all CMOS devices, although in CMOS parts, a part of the advantage of their low quiescent current is lost by their higher dynamic power dissipation.

One critical application area is bus contention during the power-on phase of a system. This bus contention occurs because, during the power-on phase (system reset), the supervising circuit does not provide defined control signals even though the rest of the system may already be functional. Therefore, there is a high probability that various bus drivers might be accidentally activated at the same time. This, again, results in bus contention that can last several 100 ms (duration of the power-on phase or reset time). Because the thermal time constant of a device is about 1 ms to 5 ms, after this time expect the final temperature in the device to be determined by momentary power dissipation. If a total power dissipation of 5 W in an 8-bit device during this bus contention is assumed, a theoretical 500°C overtemperature of the chip must be considered. With Widebus circuits, the theoretical overtemperature is 1000°C. Mostly, these devices are immediately destroyed during these kinds of bus contention. Even if no defect is detected after such bus contention, a dramatic degradation of the device is likely, which leads to a final destruction of the component some time later.

An adequate design of the control logic prevents bus contention during the power-on phase of a system. Preventing bus contention is not easy because no defined supply voltage can be expected during the power-on phase. Therefore, no defined operation of the logic circuits can be expected. The supply-voltage range below 3 V usually is not critical. Many advanced bus drivers contain a supply-voltage monitor that disables the outputs (3-state) as long as the supply voltage is lower than about 3 V. Furthermore, below this voltage, an overload of the devices is unlikely, because under this condition, the drive capability is very limited. Above a supply voltage of 3 V, additional measures are necessary. One method is to connect a pullup resistor between the enable inputs of the bus-interface circuits and the positive supply rail. This may ensure a high level as long as the preceding control logic does not provide a defined logic level, but is not helpful if the control logic delivers a wrong logic level. A reliable solution is to disable all bus-interface circuits in question during the critical time with additional control logic (see Figure 28). In this circuit, a supply-voltage monitor (TLC7705) provides a signal that disables all bus drivers during the critical time period and may reset the main processor, which then resets the control logic of the system. For this kind of application, bus-interface circuits that provide two enable inputs, like the SN74ABT541, are advantageous. One control input controls the normal operation via the system-control logic. The other input is connected to the monitor device to disable the bus logic when an undefined system condition (e.g., during power on) is expected. If no second enable input is available, such as in an SN74ABT245, another gate is required to perform the additional disable function.

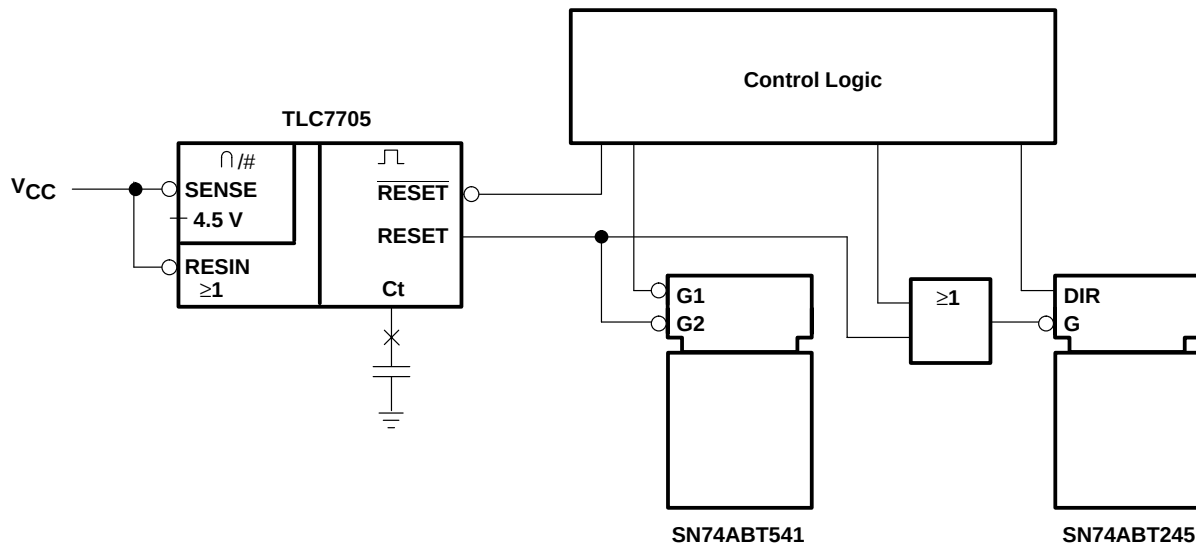


Figure 28. Bus Supervision During Power On

CAUTION:

Since considerably higher currents flow on signal lines during bus contention than with normal operation, the noise margin in the system is reduced accordingly. This can result in faulty operation and care should be taken to avoid bus contention.

8 Backdriving

The testing of highly complex electronic systems must ensure that the system or subsystem operates faultlessly. For this purpose, it is advantageous to install at the system level diagnostic programs that are able to recognize and localize faults. Certain limitations are unavoidable with self-testing because a defective system may no longer be able to seek and localize faults. This method usually breaks down completely when individual component groups are being tested because fault diagnosis on their own is generally too limited. In such cases, additional test equipment that stimulates the component group with special test signals, test samples, or patterns, and analyzes the results is necessary.

If all relevant circuit segments in the component group can be addressed via a defined interface, e.g., built-in testability (BIT), testing can be performed without additional test circuits and adapters. Test bus IEEE Std 1149.1 (JTAG), with an appropriate device interface, allows testing of all circuits, the connections between them, and the complete subsystem.

If this option is not available, appropriate signals can be injected into the circuit from outside to achieve the required circuit stimulation. For this, the inputs to the circuits to be tested must be supplied with the necessary voltages (e.g., logic low or high) via nail-bed adapters and the reaction at the outputs of these circuits is monitored. In this way, the functions of complex systems can be tested step by step and the most common faults recognized, such as:

- Solder bridges and broken metallization
- Incorrect, faulty, damaged, or missing devices
- Functional disturbances and signal-processing faults

Because only a few single devices are accessed at a time, only the special, appropriate functions (e.g., the truth table of a gate) need to be known, not the function of the complete device group. In this way, standard test program libraries can be used to put together the complete test program. With this method, large systems also can be tested step by step without using excessively complex test procedures.

The stimulation of the circuit to be tested might present a problem. For example, the inputs of gate G3 (see Figure 29) must be switched to a particular potential. These same inputs are already controlled by other devices (G1 and G2), which supply their own signals to the gates to be tested. The test equipment must be able to force another voltage on to the same node as is supplied by the existing circuit. The expression commonly used here is *backdriving* or *node forcing*. The output of a device is forced from outside into a state not corresponding to its normal control-logic state.

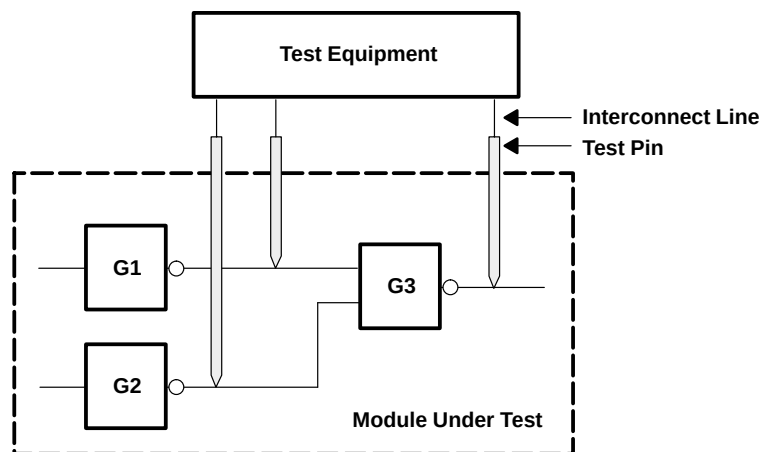


Figure 29. Feeding Test Signals Into a Node Test Point

The test equipment must have substantial drive capability to force the device into another logic state. Table 2 gives the short-circuit current at high level of the most important logic families. The situation in which the test equipment must force an output to low level is not the most demanding requirement. Currents of up to several-hundred milliamperes must be provided to force from outside an output that is supplying a low level into a high-level state.

Serious interference arises when the high currents are switched on or off and line reflections occur on the lines connecting the test equipment and the circuit being tested. All these effects can result in a real or apparent malfunction of the circuit being tested. This test method is of limited use when the precise timing of fast circuits must be assessed.

When injecting the test-signal current into the outputs, which then must be forced into an inverted state, the devices usually are driven far outside their maximum permissible ratings. This can damage or destroy the devices. At the very least, their reliability and, therefore, their operating life, is adversely affected. In recent years, the drive capability (maximum output currents) of devices has been steadily increased in the interest of improved technical performance. Modern bus-driver currents of 500 mA and more are needed to force the outputs of devices to particular logic levels (see Figure 30). The high current densities in the internal connections of devices can cause a drift of metallic ions, or so-called electromigration. This effect begins at current densities of 3×10^5 to 10^6 A/cm². Metallic ions are released from the grain boundaries and then drift in the inverse direction of current flow (in the direction of the electron flow). If the excessive current density lasts long enough, the interconnections are eroded.

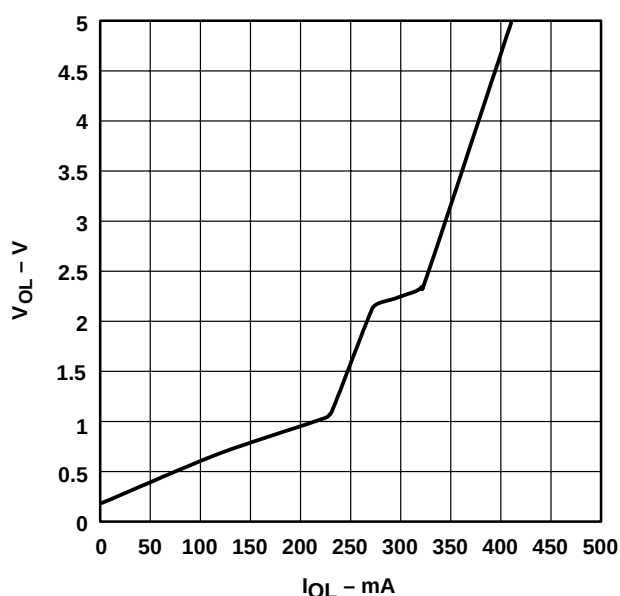


Figure 30. Low-Logic-Level Output Characteristics of SN74AS645

When backdriving, the most important effect is the extreme rise in temperature that occurs in the chip during the test. The heat that results must be conducted away via the package. The equivalent circuit of Figure 31 shows the thermal relationships in the package.

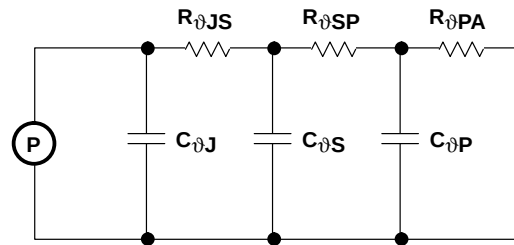


Figure 31. Thermal Resistances in a Device

The thermal source (P) first fills up the thermal capacitance of the semiconductor junction. The heat spreads, via $R_{\theta JS}$, in the complete substrate (chip) of the device. From there, the heat flows, via the resistance ($R_{\theta SP}$), into the package and then, via the resistance ($R_{\theta PA}$), to the ambient environment. Only the sum of the thermal resistances $R_{\theta JU} = R_{\theta JS} + R_{\theta SP} + R_{\theta PA}$ (thermal-resistance junction ambient) is given in data books (see Table 5). This resistance is not helpful for the problem under consideration but it can be used to calculate the temperature in a stable state. Rapid temperature increases, such as result from backdriving, cannot be calculated from the sum of thermal resistances. The thermal capacitance and thermal conductivity of the chip can be calculated, but it is better to determine the thermal behavior through measurements (see Figure 32).

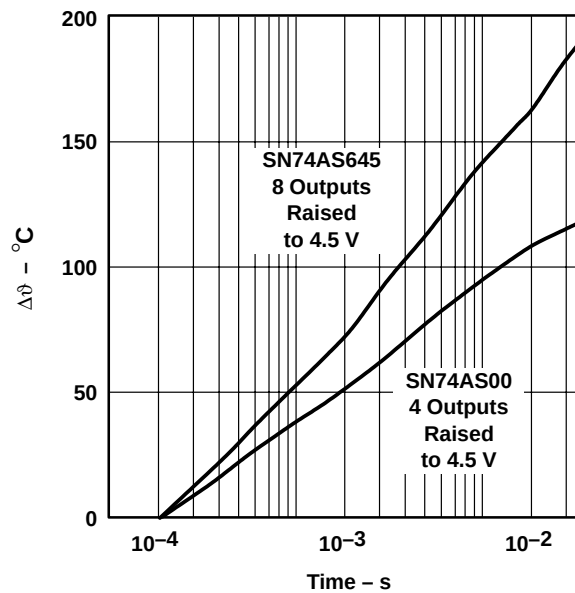


Figure 32. Device Thermal Behavior

Figure 32 shows that, with an SN74AS645, a temperature rise in the chip of 100°C must be expected after 2 ms. After 10 ms, temperatures are attained that are not permissible in plastic packages. CMOS and BiCMOS circuits have a very low power dissipation and do not behave better in this particular case. With these modern components, expect at least the same driving capability. The short-circuit current at the output of an ACL logic device is >250 mA. It is ultimately these currents that are responsible for the high power dissipation during backdriving.

The following rules always should be observed when using the test methods discussed:

- Backdriving should be used only when the state required at the node point in question can be reached in no other way.
- The maximum permissible power dissipation of a device should not, under any circumstances, be exceeded.
- Outputs that are at a low-level state, as a result of their logic functions, can be raised to a level of $V_O = 3\text{ V}$ for a short period by backdriving. The energy, which as a result of this backdriving is injected into the device ($V_O \times I_{OL} \times t_{pd}$), must not exceed 25 mW/s. The current that results in an output should not exceed a value of $I_{OL} = 300\text{ mA}$. The pulse duration must not exceed $t_d = 100\text{ ms}$. To keep the thermal stress within acceptable limits, the duty cycle of the pulses (duration of the pulse ÷ duration of the period) should be less than 1:10.
- Outputs that are in a high-level state as a result of their logic functions can be lowered to a level of 0 V for a short time by means of backdriving. One output of a device can be short circuited to ground, in such a case, for maximum $t_d = 100\text{ ms}$. The product of the output current, the supply voltage, and the pulse duration ($I_{OH} \times V_{CC} \times t_{pd}$) must not exceed 25 mW/s. If n outputs are simultaneously short circuited to ground, limit the total energy injected into the device under test ($I_{OH} \times V_{CC} \times t_{pd}$) to 25 mW/s. To keep the thermal stress within reasonable limits, the duty cycle of the short circuit (short-circuit duration ÷ repetition time) should be less than 1:10.
- All voltages, including peak voltages of overshoots/undershoots, must be within the absolute maximum ratings on data sheets.
- Simultaneous backdriving of several outputs in parallel (wired OR) with a common current source is not permissible. Since current sharing cannot be predicted, there is danger of overloading the circuit.
- The chip temperature of the circuit under test must not exceed 125°C.
- Open-circuit (unterminated) lines should be avoided to prevent faults caused by reflection.

Semiconductor device manufacturers consider testing with backdriving as involving a measure of risk. The danger of overloading devices cannot be excluded since they are operated in regions that can lie far outside those for which they were designed. For this reason, no statement about the reliability of devices that are subjected to this test procedure can be made. TI does not use such test methods. Such test methods are not permissible in many (e.g., military) areas of application.

9 Summary

This report provides the designer of digital systems information that is not found in data books, but which is of interest and necessary in many applications. The differences between individual circuit families have been discussed. The circuit design techniques used with various devices, combined with the different technologies used to manufacture them, often make it difficult to give specific design rules; in many cases it is possible to give only very general guidance. In practice, few parameters are actually measured, particularly with older devices. In all such cases, this report provides guidelines that enable the designer to predict the behavior of circuits in a system.

Acknowledgment

The author of this document is Eilhard Haseloff.

Bus-Interface Devices With Output-Damping Resistors or Reduced-Drive Outputs

SCBA012A
August 1997



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Introduction

The spectrum of bus-interface devices with damping resistors or balanced/light output drive currently offered by various logic vendors is confusing at best. Inconsistencies in naming conventions and methods used for implementation make it difficult to identify the best solution for a given application. This report attempts to clarify the issue by looking at several vendors' approaches and discussing the differences.

Output-Damping Resistors

The purpose of integrating output-damping resistors in line buffers and drivers is to suppress signal undershoots and overshoots on the transmission line through what is usually referred to as line-impedance matching (see Figure 1). The effective output impedance of the line driver (Z_O) is matched with the line impedance (Z_L). Thus, no signal reflection occurs at the line start ($Z_O = Z_L$; reflection coefficient at point A is 0). The input impedance of the receiving device (Z_I) is assumed to be several orders of magnitude higher than the line impedance. This is valid for CMOS and BiCMOS devices. In this case, the reflection coefficient at point B is approximately 1, such that almost all of the wave energy is reflected at the end of the line.

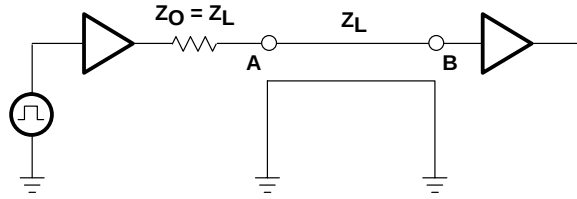


Figure 1. Line-Impedance Matching

Figure 2 illustrates the signal waveforms for a high-to-low transition for a line driver without and with output-damping resistors under these conditions. T is the line signal-transmission time, i.e., the time it takes for the signal wave to travel from point A to point B, or vice versa. The high-level signal prior to the output transition of the line driver has a level of about 3.3 V, typical for 5-V TTL-level devices, such as ABT or FCT-T, as well as for all 3.3-V logic devices. The line impedance is assumed to be $33\ \Omega$.

Without the damping resistor (see Figure 2a), a driver output impedance of $5\ \Omega$ is assumed. The incident wave at point A and $t = 0$ establishes a signal level of:

$$V_A = 3.3\text{ V} \times \left(1 - \frac{33\ \Omega}{5\ \Omega + 33\ \Omega}\right) = 0.43\text{ V} \quad (1)$$

Due to the reflection at the line end, the receiver (point B) sees the initial line level dropping to

$$V_B = 3.3\text{ V} - 2 \times (3.3\text{ V} - 0.43\text{ V}) = -2.44\text{ V} \quad (2)$$

which represents a considerable undershoot. With a damping resistor, the effective output impedance is assumed to be $33\ \Omega$, thus matching the line impedance. In this case, while there is a step in the signal at the driver output (point A), the receiver side (point B) sees a very clean signal transition without any significant undershoot or overshoot. Signal waveforms are analogous to this for a low-to-high transition, in which case the line without damping resistors shows significant signal overshoot.

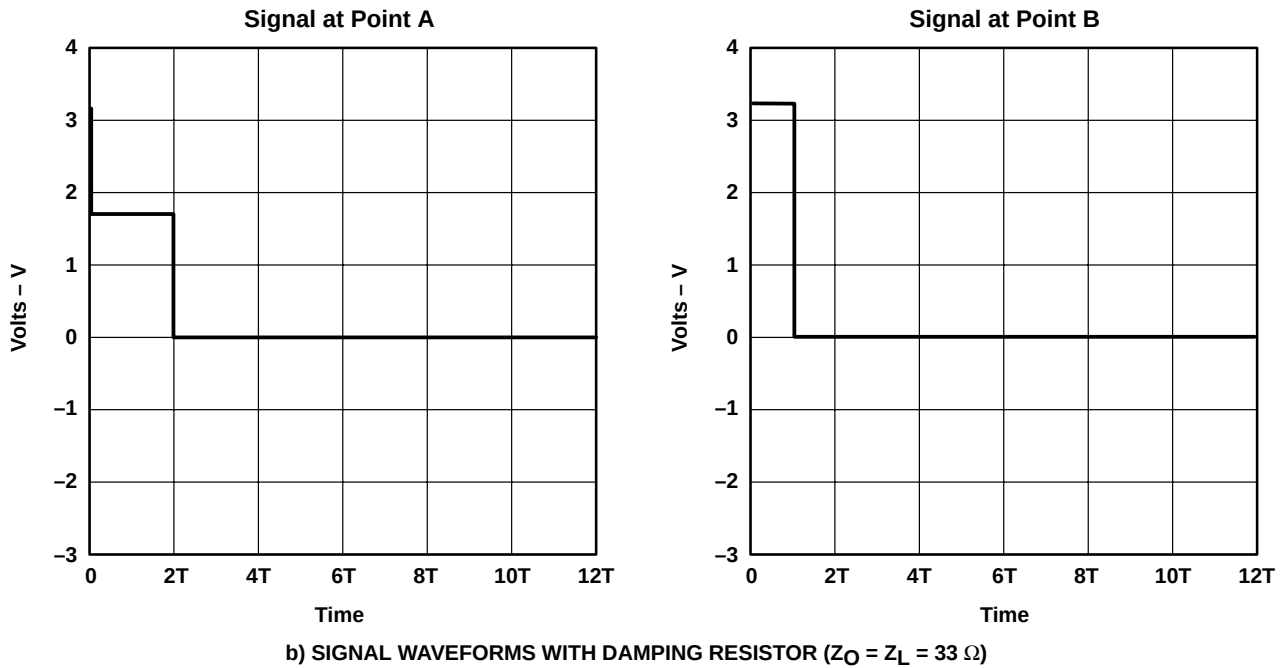
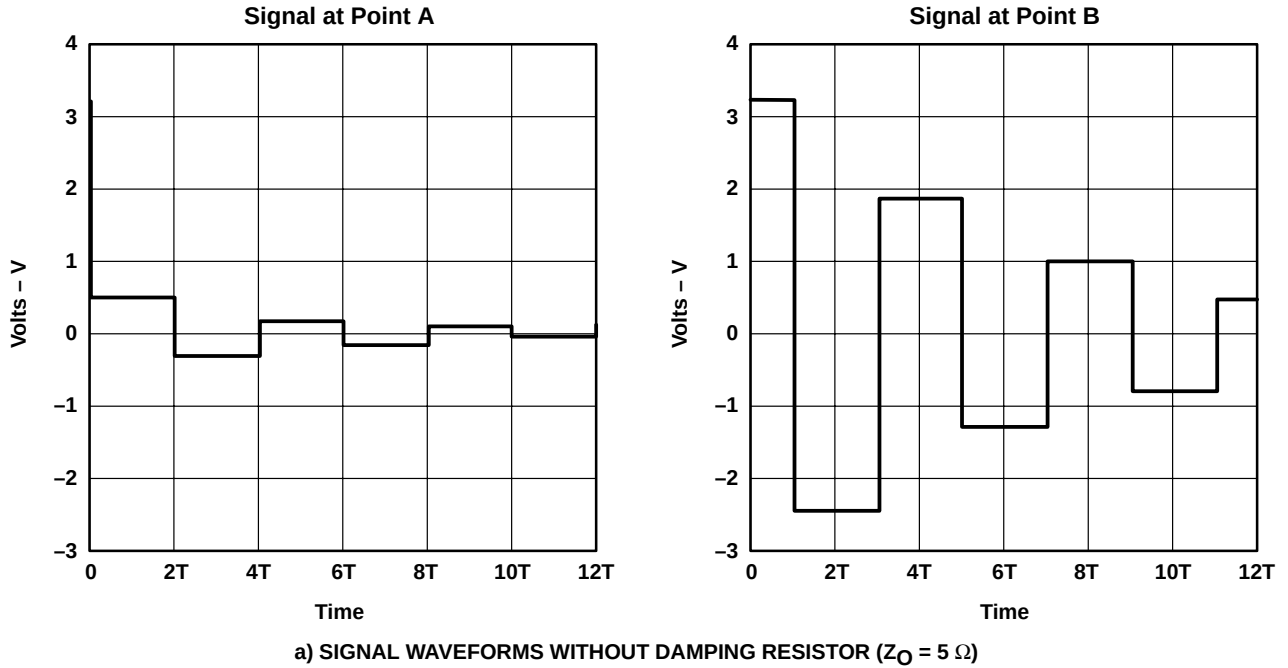


Figure 2. Signal Waveforms Showing Effect of Damping Resistors

The damping-resistor solution is particularly important when designing memory arrays because excessive undershoots and overshoots can cause data loss in memory devices. Although line-impedance matching is optimized for point-to-point transmission where it helps establish near-perfect signal waveforms, it also works fine in most memory-array configurations where there is one driver and many receiving modules. Some of the modules may see a step in the signal waveform (see Figure 2b), but this is only for a short period of time (typically less than 1 ns) and does not affect data transmission. The goal to prevent excessive undershoots and overshoots is still fully accomplished.

Texas Instruments (TI), Philips, and a number of other manufacturers implement output-damping-resistor options in several logic families. The device nomenclature used by all these vendors is a “2” added in front of the device number, that is, the damping-resistor version of the popular ’244 octal buffer is referred to as a ’2244. Having been the first to introduce a ’2244 function with the SN74ALS2244 in the mid-1980s, TI quickly expanded its spectrum of devices with output-damping resistors. Today, it covers the ALS, F, BCT, ABT, LVT, LVC, and ALVC product lines as well as other specialized bus-interface devices.

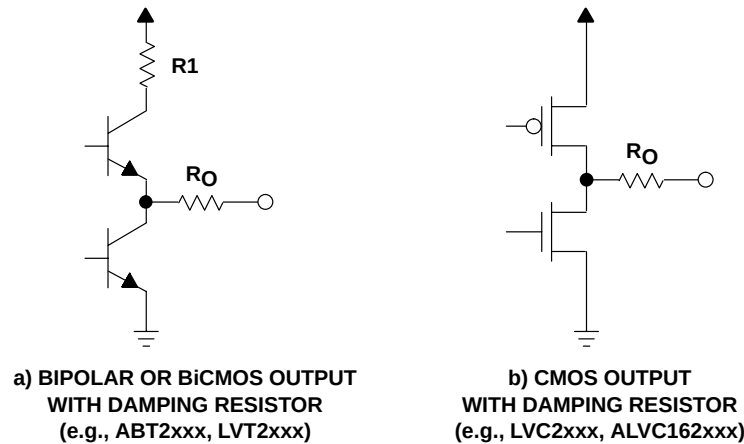


Figure 3. Damping-Resistor Implementation

Figure 3 shows simplified output diagrams that illustrate how damping-resistor outputs are implemented in the ABT/LVT and LVC/ALVC families, respectively.^{2,3} The value of the output-damping resistor (R_O) typically is about $25\ \Omega$. The resistor value in the upper output stage of the bipolar/BiCMOS output, R_1 , is only a few ohms. Together with the impedance of the output stage itself, this leads to an effective total output impedance of about $33\ \Omega$ for all of these circuits. Because line impedance in memory systems is usually around $20\ \Omega$ to $50\ \Omega$ and some level of impedance mismatch is acceptable, this output impedance value covers almost all practical uses. A good rule of thumb is that a mismatch up to a factor of two has little effect on signal characteristics. Figures 4 and 5 show the signal condition for an output-damping-resistor device with a $33\text{-}\Omega$ output impedance and line impedance of $20\ \Omega$ and $50\ \Omega$, respectively. Signal distortion is still acceptable in both cases.

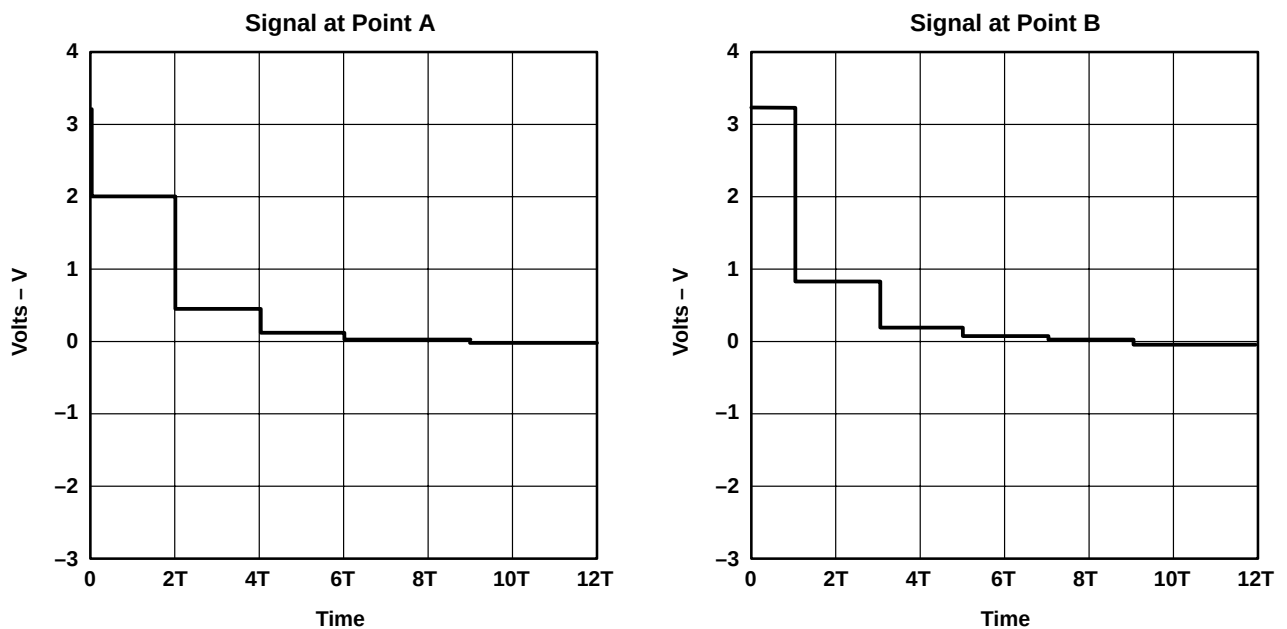


Figure 4. Signal Waveforms With Impedance Mismatch ($Z_O = 33\ \Omega$, $Z_L = 20\ \Omega$)

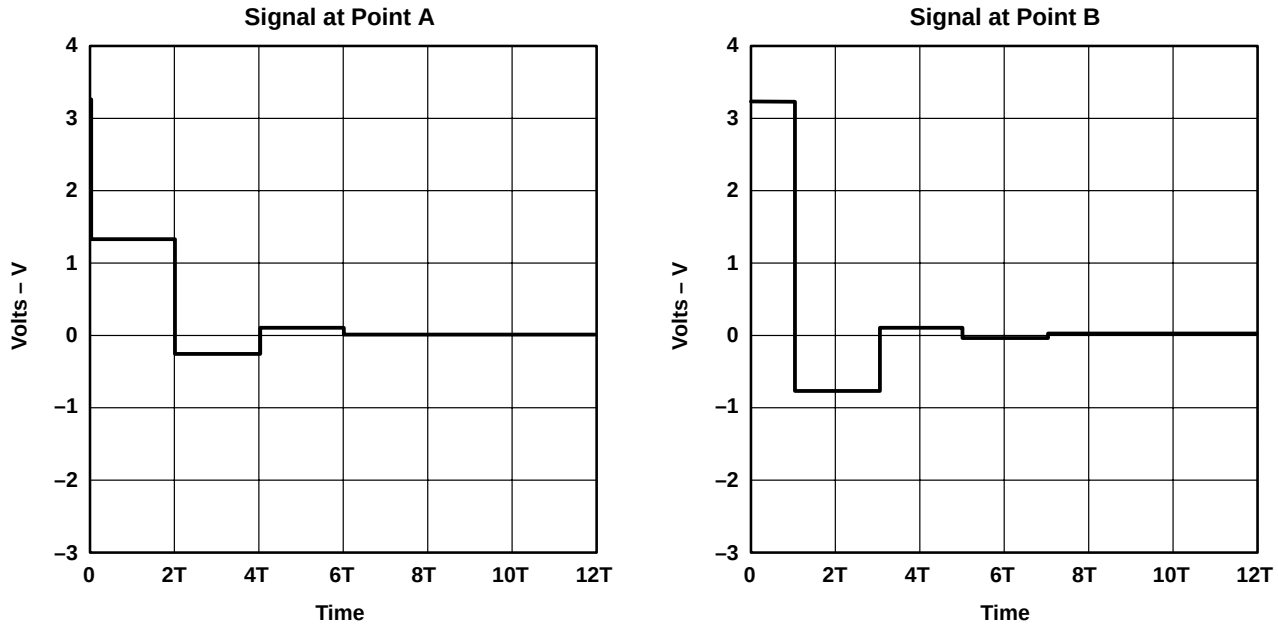


Figure 5. Signal Waveforms With Impedance Mismatch ($Z_O = 33 \Omega$, $Z_L = 50 \Omega$)

The output-stage dimensioning of devices with damping resistors usually remains unchanged. The introduction of the damping resistor reduces the nominal output drive currents, but still leaves a drive capability sufficient for most applications. Table 1 shows low- and high-level output drive specifications for the families previously mentioned. Note that I_{OH} and I_{OL} are balanced on all '2xxx devices.

Table 1. Low- and High-Level Output Drive Specifications for Selected TI Logic Devices

TECHNOLOGY	OUTPUT CURRENT (mA)	
	I_{OH}	I_{OL}
ABTxxx/LVTxxx	-32	64
ABT2xxx/LVT2xxx	-12	12
LVCxxx/ALVC16xxx [†]	-24	24
LVC2xxx/ALVC162xxx [†]	-12	12

[†] ALVC devices are available in Widebus™ versions (16xxx/162xxx) only. All other technologies listed are available in octal and Widebus versions.

Reduced-Drive Outputs

Some vendors refer to balanced- and light-drive outputs. The idea behind these is based on a concept that is different from the damping resistor. While the basic device characteristics remain unchanged and no line termination is added, a balanced- or light-drive device shows significantly reduced output drive currents when compared with its standard high-drive equivalent. In essence, this supports the finding that lower drive currents result in a reduction in undershoot and overshoot.

Figure 6 shows implementations of this approach for FCT16xxx devices.⁴ The impedance values given include the impedance of the FETs. Some manufacturers achieve reduced drive solely by reducing the dimensions of the output FETs, which, in turn, increases their impedance. In this case, no series resistors are added. This helps to reduce the amount of energy (that contributes to undershoots and overshoots), but does not necessarily establish true line-impedance matching because output impedance may remain too low (for example, see the lower output path in Figure 6b).

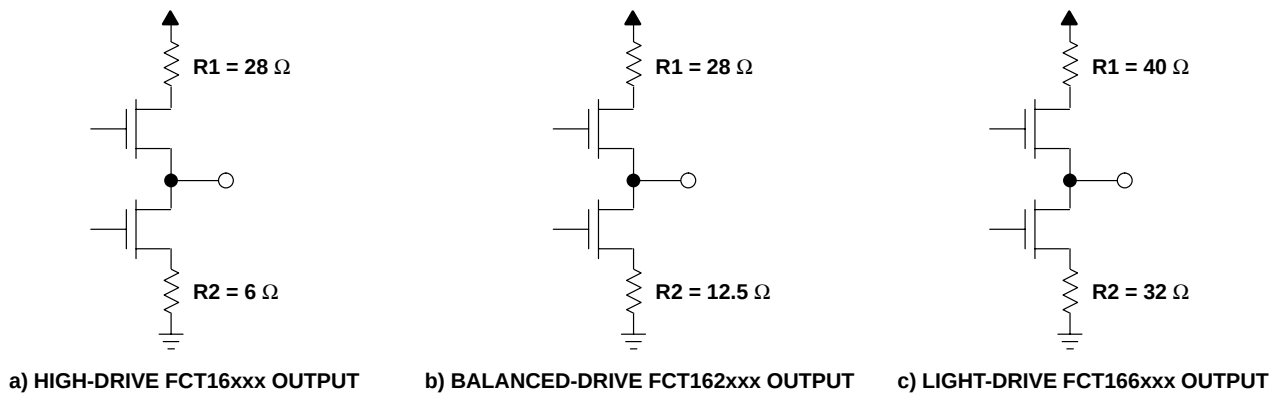


Figure 6. Implementation of Various Drive Concepts

Table 2 shows the resulting nominal output drive specifications.

Table 2. Low- and High-Level Output Drive Specifications for FCT16xxx Logic Devices

DRIVE TYPE		OUTPUT CURRENT (mA)	
		I _{OH}	I _{OL}
FCT16xxx	High drive	–32	64
FCT162xxx	Balanced drive	–24	24
FCT166xxx	Light drive	–8	8

Based on a line with $Z_L = 33 \Omega$ (see Figure 7) showing a high-to-low signal transition, Figures 8 through 10 illustrate the effect on signal undershoot and overshoot. As illustrated in Figure 6, the output impedance of the driver, Z_O , is 6Ω , 12.5Ω , or 32Ω , for high-, balanced-, and light-drive outputs, respectively.

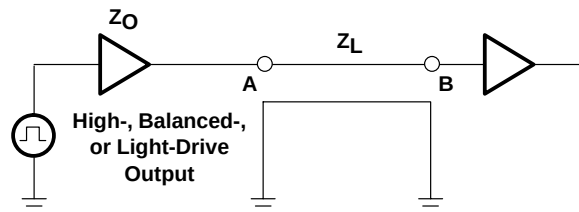


Figure 7. Line Driven by High-, Balanced-, or Light-Drive Device

As expected, the high-drive version (see Figure 8) exhibits signal characteristics very similar to those shown for a standard bus driver without an output-damping resistor (see Figure 2a).

Similarly, signal waveforms with the light-drive version (see Figure 10) resemble those of a bus driver with an output-damping resistor (see Figure 2b). The low nominal output drive of ± 8 mA limits the applicability of these devices to systems where the output drives one or a few receivers only.

While not quite as severe as the high-drive version, the balanced-drive device (see Figure 9) still causes considerable undershoots because its low-level output impedance of 12.5Ω is too low to match the line impedance. It becomes worse if line impedance is higher than 33Ω . Figure 11 demonstrates this, assuming a line impedance of 50Ω .

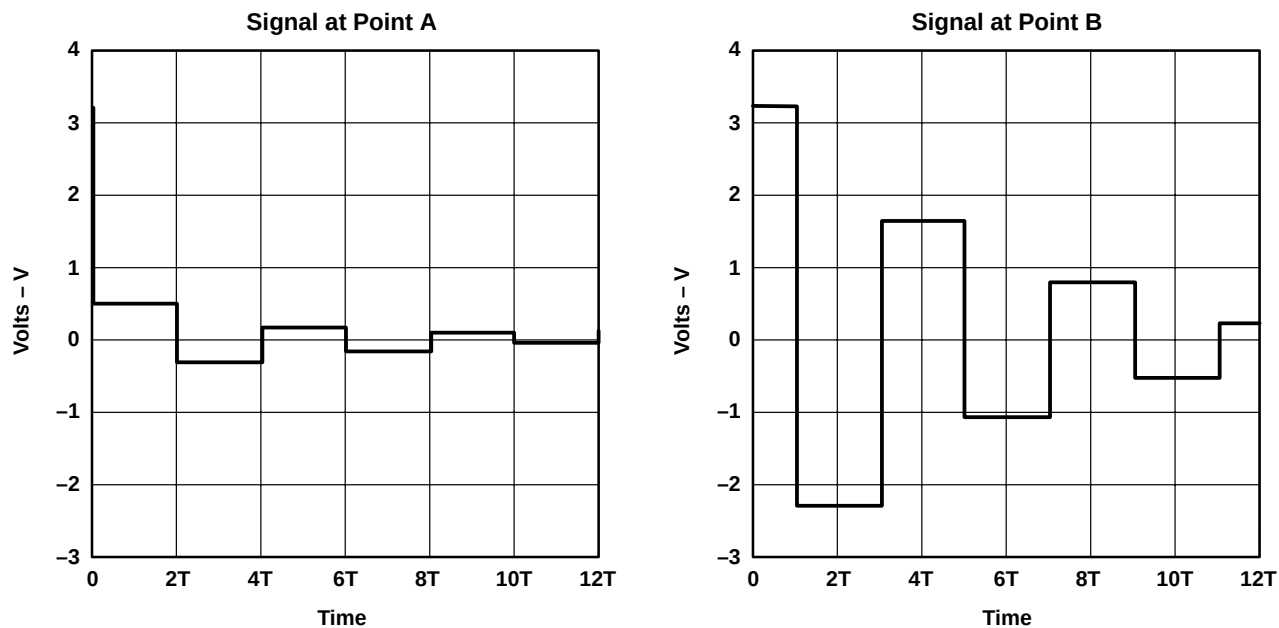


Figure 8. Signal Waveforms With High Drive ($Z_O = 6 \Omega$, $Z_L = 33 \Omega$)

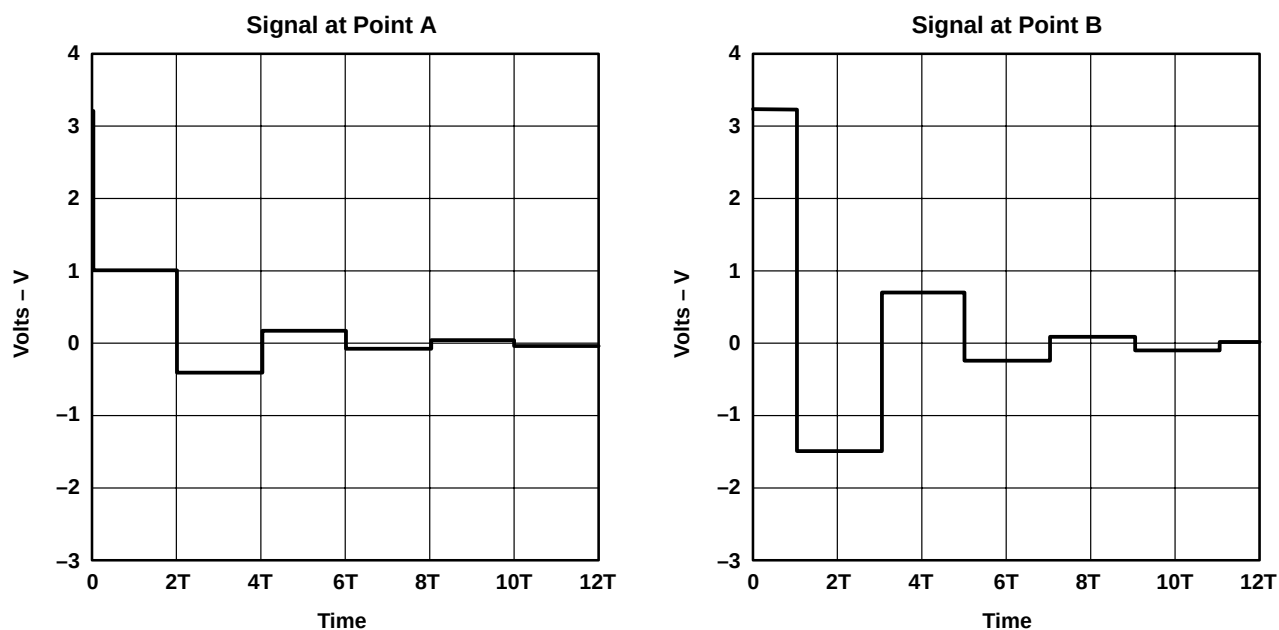


Figure 9. Signal Waveforms With Balanced Drive ($Z_O = 12.5 \Omega$, $Z_L = 33 \Omega$)

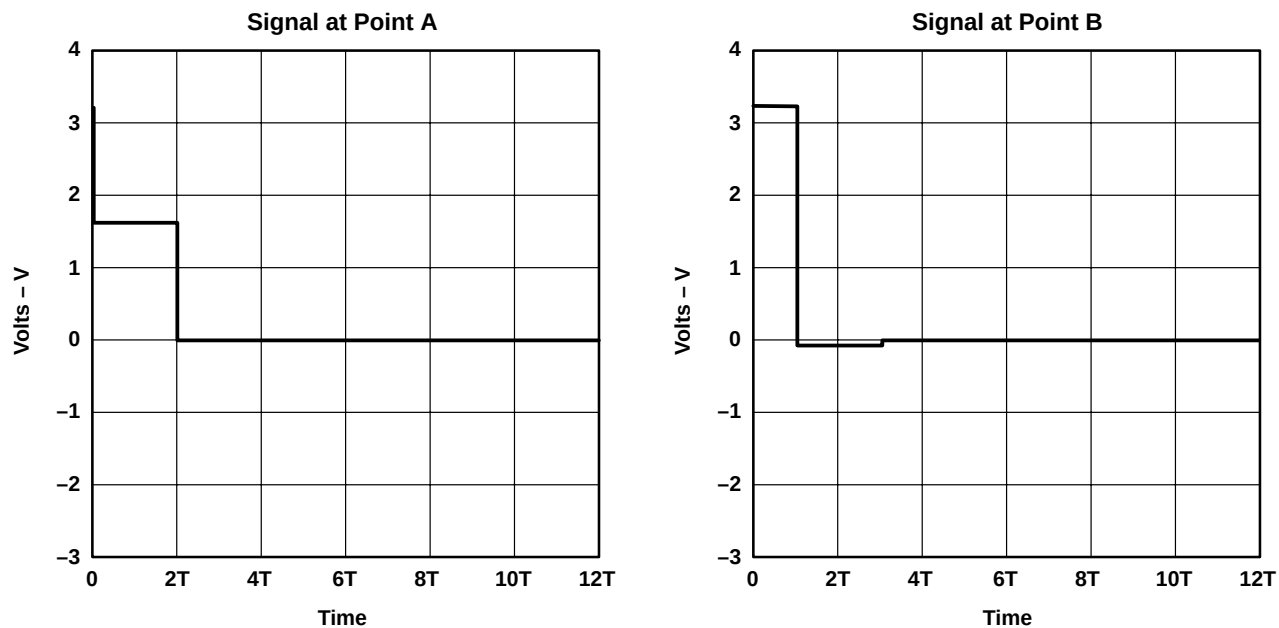


Figure 10. Signal Waveforms With Light Drive ($Z_O = 32 \Omega$, $Z_L = 33 \Omega$)

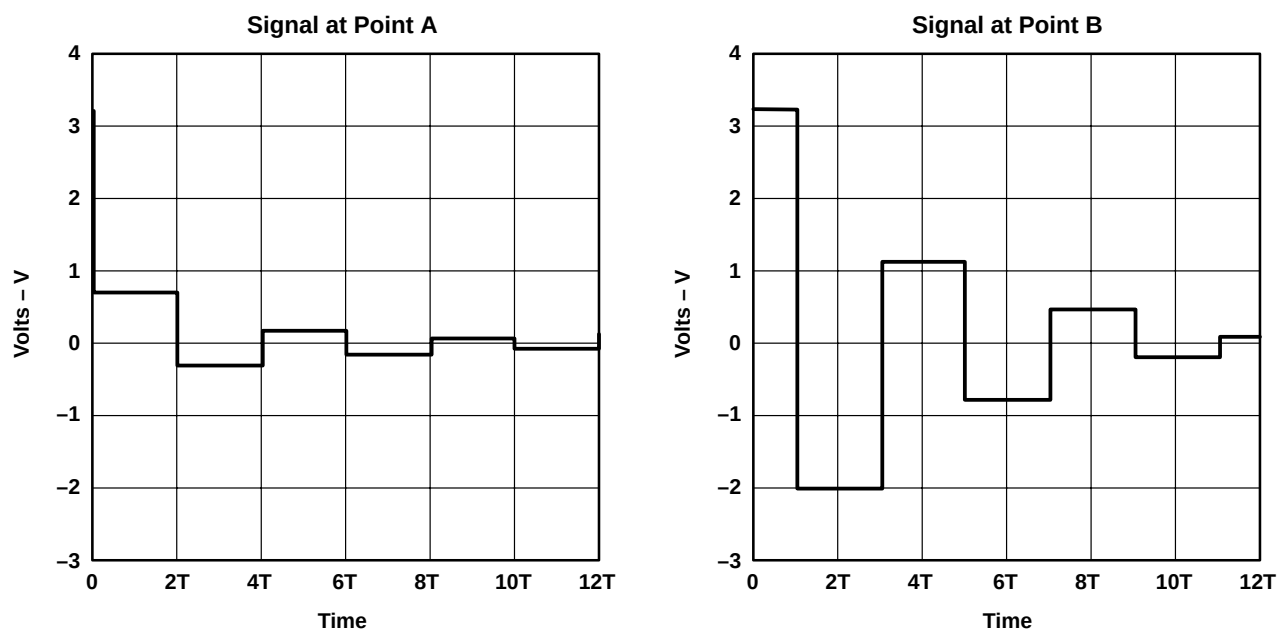


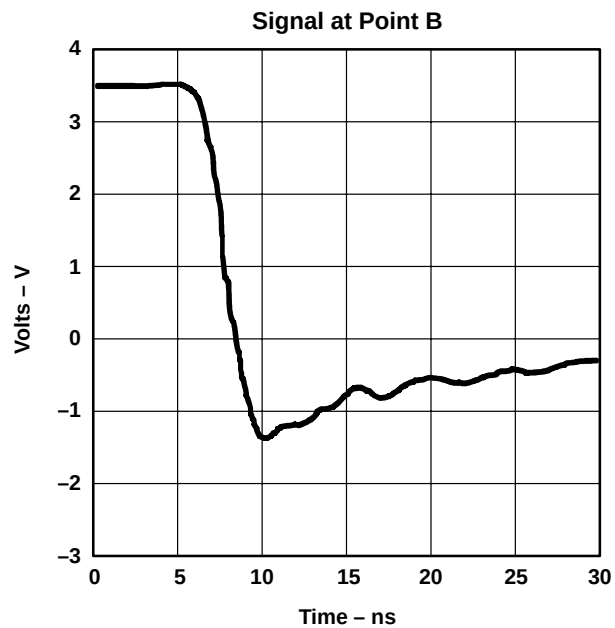
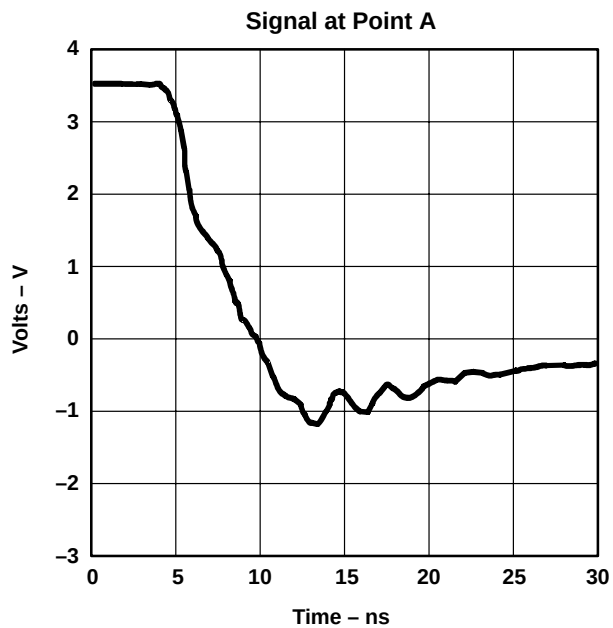
Figure 11. Signal Waveforms With Balanced Drive ($Z_O = 12.5 \Omega$, $Z_L = 50 \Omega$)

Practical Applicability of Wave Theory to Predict Signal Waveform Curves

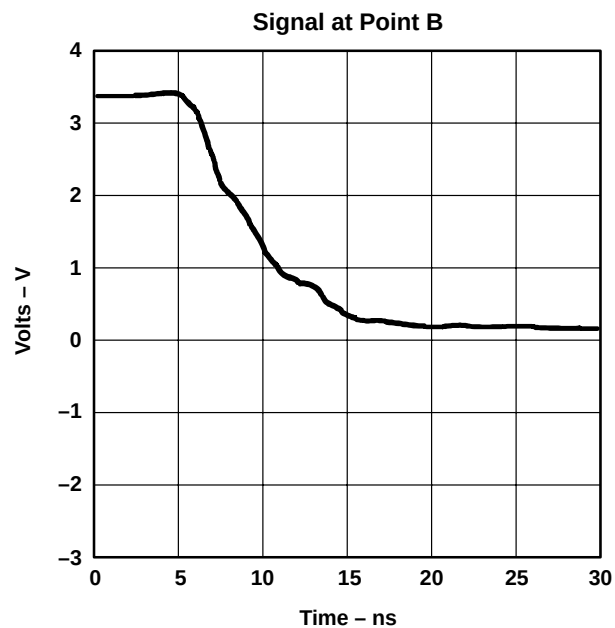
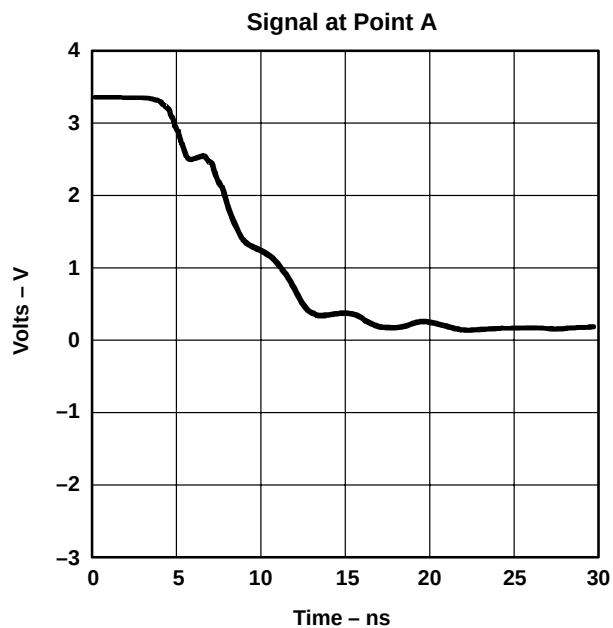
Obviously, all signal waveforms shown in Figures 2, 4, 5, and 8 through 11 are derived from wave theory. They assume a line without terminating impedance, which is an acceptable approximation when using today's CMOS receivers with their very high input impedances, but ignores the output loading effects by the capacitive loads that receiver inputs, connectors, traces, etc., represent. While these theoretical curves help in understanding the influence of output and line impedances, a necessary question is, therefore, whether the curves reflect real-world signal waveforms closely enough to be useful.

With heavily loaded outputs, typically with line impedances of $30\ \Omega$ or below, in practice, heavily distorted signal waveforms are found. Damping-resistor outputs do not improve this much. Other termination techniques may be more appropriate but lead to acceptable signal waveforms only of a line driver with very-high-output drive capability. The signal distortion often results in extended signal-propagation times because one or more reflections are needed before a well-defined signal level is established. Sometimes, slow signal slew rates prevent excessive signal bounces such that undershoots and overshoots do not reach critical levels. However, relying upon this to suppress undershoot and overshoots is not a good design practice. Figure 12 shows measured curves derived from SN74ABT244 and SN74ABT2244 devices, respectively, driving a SIMM memory module with 18 memory devices. As before, the driver output is referred to as point A and the receiver, in this case the memory device that is the farthest away from the driver, as point B. The curves illustrate quite well how the strong capacitive loading represented by the memories distorts the reflected waves. Signal undershoot on the receiver side is still overcritical in the standard device without a damping resistor, while the damping-resistor version ensures that no undershoot occurs.

Lightly loaded lines represent another problematic application for devices that do not have an output-damping resistor. Here, the aforementioned slew-rate reduction can be expected to improve things only marginally. Therefore, with line impedances of $50\ \Omega$ or more, that is, in applications where there are only a few receiving devices connected to the line, in practice, waveforms usually are very similar to theoretical ones. Large undershoots and overshoots occur if the line is left unterminated.



a) SN74ABT244 (WITHOUT DAMPING RESISTOR)



b) SN74ABT2244 (WITH DAMPING RESISTOR)

Figure 12. Signal Waveforms for SN74ABT244 and SN74ABT2244 Driving a SIMM Module

Overview of Technologies and Application Areas

As mentioned before, the spectrum of available bus-interface devices with damping resistors or reduced output drive currently offered by various logic vendors is very confusing. This is mainly because similar naming conventions are being used for different approaches. Tables 3 and 4 give an overview of advanced 5-V and 3.3-V logic families. Please note that the device series field ignores other vendor-specific parts of device names, such as device revisions or indicators for bus-hold device inputs.

Table 3. Advanced 5-V Buffers With Damping Resistor or Reduced-Drive Options

DEVICE SERIES	VENDOR	TYPE	I _{OH} (mA)	I _{OL} (mA)	COMMENTS
ABTxxx	TI, Philips, et al.	High drive	−32	64	
ABT16xxx	TI, Philips, et al.	High drive	−32	64	Same as octal version (ABTxxx)
ABT2xxx	TI, Philips, et al.	Damping resistor	−12	12	
ABT162xxx	TI, Philips, et al.	Damping resistor	−12	12	Same as octal version (ABT2xxx)
AC/ACTxxx	TI, Motorola, et al.	Balanced drive	−24	24	
AC/ACT16xxx	TI	Balanced drive	−24	24	Same as octal version (AC/ACTxxx)
AHC/AHCTxxx	TI, Philips, et al.	Light drive	−8	8	
FCTxxx	IDT, QSI, et al.	High drive	−15	64	
FCT16xxx	IDT, QSI, et al.	High drive	−32	64	I _{OH} differs from octal version (FCTxxx)
FCT2xxx	IDT, QSI, et al.	Balanced drive	−15	12	
FCT162xxx	IDT, QSI, et al.	Balanced drive	−24	24	I _{OH} , I _{OL} differ from octal version (FCT2xxx)
FCT162Qxxx	Pericom	Damping resistor	−12	12	No octal version
FCT166xxx	IDT	Light drive	−8	8	No octal version

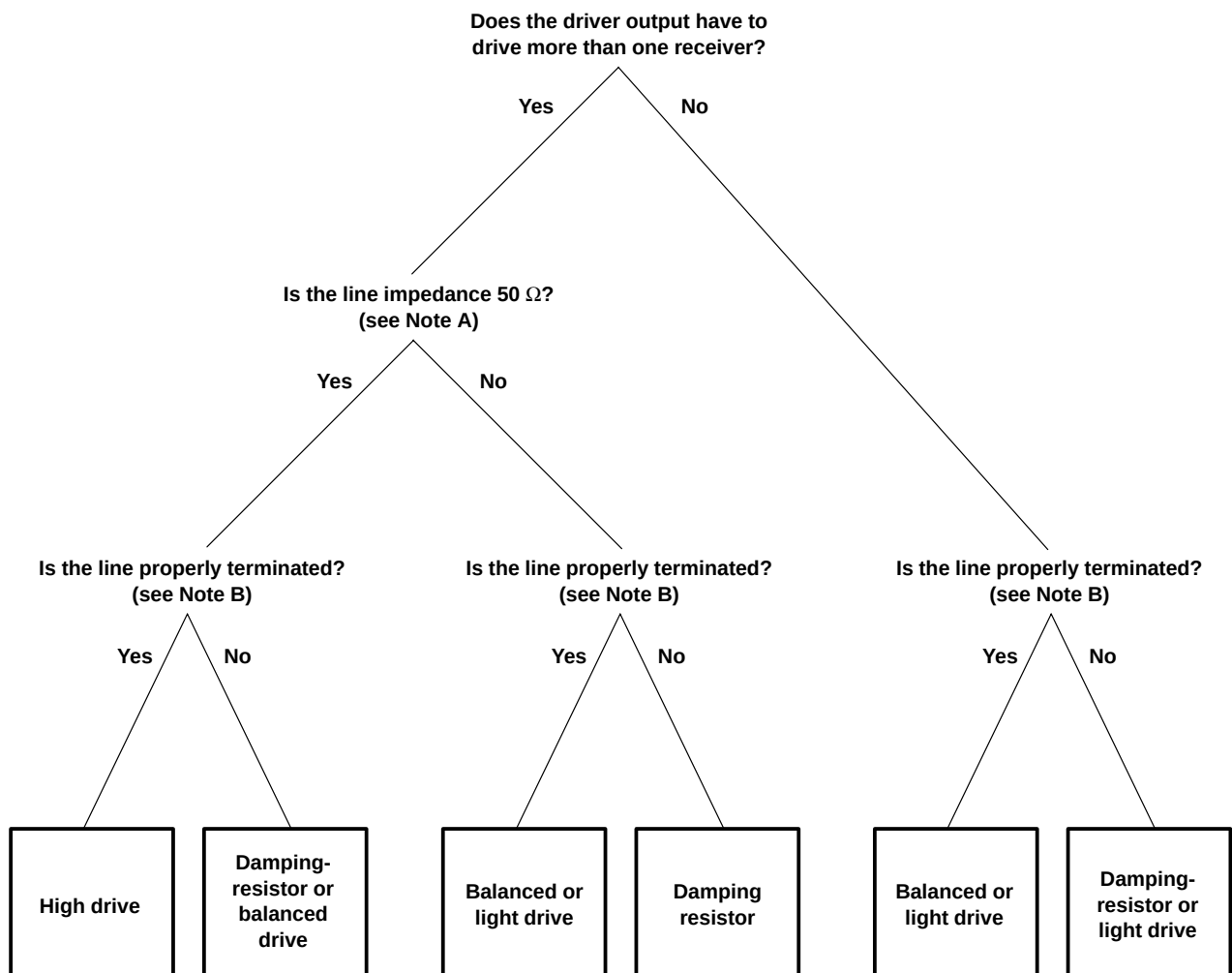
While FCT16xxx versions have the same output drive as ABT, FCT162xxx corresponds to technologies such as AC and ACT. FCT166xxx has the low output drive of families like HC/HCT or AHC/AHCT. Note that FCT characteristics are different for octals and 16-bit versions. This may lead to different signal waveforms in practical applications. All TI logic families have identical characteristics for octal and Widebus devices.

Table 4. Advanced 3.3-V Buffers With Damping Resistor or Reduced-Drive Options

DEVICE SERIES	VENDOR	TYPE	I _{OH} (mA)	I _{OL} (mA)	COMMENTS
LVTxxx	TI, Philips, et al.	High drive	−32	64	
LVT16xxx	TI, Philips, et al.	High drive	−32	64	Same as octal version (LVTxxx)
ALVT16xxx	TI, Philips, et al.	High drive	−32	64	No octal version
LVT2xxx	TI, Philips, et al.	Damping resistor	−12	12	
LVT162xxx	TI, Philips, et al.	Damping resistor	−12	12	Same as octal version (LVT2xxx)
ALVT162xxx	TI, Philips, et al.	Damping resistor	−12	12	No octal version
LVCxxx	TI, Philips, et al.	Balanced drive	−24	24	
LVC16xxx	TI, Philips, et al.	Balanced drive	−24	24	Same as octal version (LVCxxx)
LVC2xxx	TI	Damping resistor	−12	12	
LVC162xxx	TI	Damping resistor	−12	12	Same as octal version (LVC2xxx)
ALVC16xxx	TI, Philips, et al.	Balanced drive	−24	24	No octal version
ALVC162xxx	TI	Damping resistor	−12	12	No octal version
LVxxx	TI, Philips, et al.	Light drive	−8	8	
LCXxxx	Fairchild, et al.	Balanced drive	−24	24	No reduced-drive versions available
LCX16xxx	Fairchild, et al.	Balanced drive	−24	24	Same as octal version (LCXxxx)
FCT3xxx	IDT, QSI, et al.	Reduced, unbalanced drive	−8	24	No high-drive versions available
FCT163xxx	IDT, QSI, et al.	Reduced, unbalanced drive	−8	24	Same as octal version (FCT3xxx)

LVT and ALVT are the only high-drive 3.3-V logic families available in the market. For 3.3 V, only the LVT, ALVT, LVC, and ALVC product families offer true damping-resistor options. FCT3xxx and FCT163xxx devices have significantly lower drive capability than their 5-V equivalents. Also, their I_{OH}/I_{OL} drive currents are unbalanced, which limits their use in certain applications.

Application areas for damping-resistor and reduced-drive line buffers and transceivers cover many different types of end equipment. In addition to required device function, output loading (line impedance) and available termination are the decisive factors when choosing a device. The decision tree shown in Figure 13 provides a general guideline. However, specific requirements may represent further constraints.



- NOTES: A. If exact line impedance is unknown, a good rule of thumb is that line impedance is lower than 50 Ω if more than four or five receiver inputs are connected to the line.
- B. Examples of other line-termination methods are a split-resistor (Thevenin) network, an R-C combination, or clamping diodes. A more detailed discussion of advantages and disadvantages of these and other termination methods is found in reference 3.

Figure 13. Decision Tree for Selecting Driver Output Type

Transceivers With Output-Damping Resistors or Reduced-Drive Outputs

So far, this report has dealt with buffers and line drivers only, and has shown that several different output versions support a wide range of output load configurations.

The number of choices is even larger when looking at transceivers because any combination of output versions can be chosen independently for the A port and B port of the device. Not all possible combinations are being offered in the market, but the list of drive types is extensive.

1. High-drive outputs on both ports
2. High-drive outputs on one port and damping-resistor outputs on the other port
3. Balanced-drive outputs on one port and damping-resistor outputs on the other port
4. Balanced-drive outputs on both ports
5. Damping-resistor outputs on both ports
6. Light-drive outputs on both ports
7. Reduced-, unbalanced-drive outputs on both ports

The best combination for a particular application can be determined using the decision tree in Figure 13 independently for the A and B ports of the transceiver. In general, applications that require a transceiver between a backplane and a local board require types 1 or 2 (type 3 may work in some applications). Applications with more lightly loaded local buses on both sides require any one of types 2 through 5, while type 6 addresses point-to-point transmission requirements.

The spectrum of devices offered in the market is complex and difficult to comprehend. Tables 5 through 11 show the options available for each type.

Table 5. Advanced Transceivers With High-Drive Outputs on Both Ports (Type 1)

DEVICE	V _{CC}	VENDOR	COMMENTS
ABTxxx	5 V	TI, Philips, et al.	
ABT16xxx	5 V	TI, Philips, et al.	
FCTxxx	5 V	IDT, QSI, et al.	
FCT16xxx	5 V	IDT, QSI, et al.	I _{OH} differs from octal version (FCTxxx)
LVTxxx	3.3 V	TI, Philips, et al.	
LVT16xxx	3.3 V	TI, Philips, et al.	

Table 6. Advanced Transceivers With High-Drive Outputs on One Port and Damping-Resistor Outputs on the Other Port (Type 2)

DEVICE	V _{CC}	VENDOR
ABT2xxx	5 V	TI
ABT162xxx	5 V	TI
LVT2xxx	3.3 V	TI
LVT162xxx	3.3 V	TI
ALVT162xxx	3.3 V	TI

Table 7. Advanced Transceivers With Balanced-Drive Outputs on One Port and Damping-Resistor Outputs on the Other Port (Type 3)

DEVICE	V _{CC}	VENDOR
LVC2xxx	3.3 V	TI
LVC162xxx	3.3 V	TI
ALVC162xxx	3.3 V	TI

Table 8. Advanced Transceivers With Balanced-Drive Outputs on Both Ports (Type 4)

DEVICE	V _{CC}	VENDOR	COMMENTS
AC/ACTxxx	5 V	TI, Motorola, et al.	
AC/ACT16xxx	5 V	TI	
FCT2xxx	5 V	IDT, QSI, et al.	
FCT162xxx	5 V	IDT, QSI, et al.	I _{OH} , I _{OL} differ from octal version (FCT2xxx)
LVCxxx	3.3 V	TI, Philips, et al.	
LVC16xxx	3.3 V	TI, Philips, et al.	
ALVC16xxx	3.3 V	TI, Philips, et al.	
LCXxxx	3.3 V	Fairchild, et al.	
LCX16xxx	3.3 V	Fairchild, et al.	

Table 9. Advanced Transceivers With Damping-Resistor Outputs on Both Ports (Type 5)

DEVICE	V _{CC}	VENDOR	COMMENTS
ABTRxxx	5 V	TI	Same nomenclature, but different type from TI ABT162xxx
ABT162xxx	5 V	Philips	
FCT162Qxxx	5 V	Pericom	
LVC162xxx	3.3 V	TI	
LVC162xxx	3.3 V	TI	
ALVC162xxx	3.3 V	TI	
ALVC162xxx	3.3 V	Philips	Same nomenclature, but different type from TI ALVC162xxx
LVT162xxx	3.3 V	Philips	Same nomenclature, but different type from TI LVT162xxx
ALVT162xxx	3.3 V	Philips	Same nomenclature, but different type from TI ALVT162xxx

Table 10. Advanced Transceivers With Light-Drive Outputs on Both Ports (Type 6)

DEVICE	V _{CC}	VENDOR
AHC/AHCTxxx	5 V	TI, Philips, et al.
FCT166xxx	5 V	IDT
LVxxx	3.3 V	TI, Philips, et al.

Table 11. Advanced Transceivers With Reduced-, Unbalanced-Drive Outputs on Both Ports (Type 7)

DEVICE	V _{CC}	VENDOR	COMMENTS
FCT3xxx	3.3 V	IDT, QSI, et al.	
FCT163xxx	3.3 V	IDT, QSI, et al.	I _{OH} , I _{OL} differ from octal version (FCT3xxx)

The majority of solutions offered are symmetrical, that is, they use the same output type on the A port and on the B port. While this may appear logical, it does not address the needs of most backplane-based applications where the backplane usually requires a high-drive output. TI was the first to introduce a transceiver with output-damping resistors, the SN74BCT2245, and since then has used the AAA2xxx or AAA162xxx concept (AAA = family indicator, xxx = device number) to indicate a device with standard (high or balanced) drive on one side and damping-resistor outputs on the other side. Others, including Philips, use the same nomenclature to indicate both output sides having damping resistors. TI uses AAAR2xxx or AAAR162xxx for this arrangement.

Conclusion

While buffers or transceivers with integrated output-damping resistors or reduced-drive outputs are required by many applications, the system designer needs to carefully choose a solution because vendors' denomination methods for these devices may be confusing. In particular, the difference between true damping resistors, i.e., integrated series resistors in the output path, and reduced-drive outputs, where the output drive is limited through changing the dimensioning and/or adding a resistor to the upper and lower transistor of the output stage, needs to be understood relative to different applications.

TI is the only vendor who offers 5-V and 3.3-V versions of all driver output types discussed in this report.

Acknowledgment

The author of this document is Lothar Katz.

References

- 1 Curtis, Rick; Forstner, Peter; "Memory Driver Application Report", EB 205E, Texas Instruments (www.ti.com/sc/docs/asl/lit/eb205.htm).
- 2 Texas Instruments, "ABT Enables Optimal System Design", SCBA001 (www.ti.com/sc/docs/psheets/appnote.htm).
- 3 Texas Instruments, "Proper Termination of Outputs", *LVC Designer's Guide*, SCBA010, page 1–27ff.
- 4 Hronik, Stanley, "Effective Use of Line Termination in High Speed Logic", Integrated Device Technology, Inc., Conference Paper CP-23 (www.idt.com/cgi-bin/dsq.pl?mkgkey=logicgen).
- 5 Texas Instruments, SN74ABTxxx, SN74LVCxxx, SN74ALVCxxx, and SN74LVTxxx data sheets (www.sc.ti.com/sc/docs/psheets/pids2.htm).
- 6 Integrated Device Technology, IDT54/74FCTxxx data sheets (www.idt.com/logic/Welcome.html).
- 7 Pericom, PI74FCTxxx data sheets (www.pericom.com/products/sinter).
- 8 Philips Semiconductors, 74ABTxxx, 74LVCxxx, 74ALVCxxx, and 74ALVTxxx data sheets (www.semiconductors.philips.com/philips54.html#3).

Migration From 3.3-V to 2.5-V Power Supplies for Logic Devices

SCEA005
December 1997



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Introduction

Powering systems at the 5-V level has been a standard practice for approximately 30 years. Power consumption is always a concern in system design and, because reducing the supply voltage yields an exponential decrease in power consumption, lower supply voltages are commonly used. Thus, a transition from the common 5-V power-supply level to the 3.3-V level is occurring. Furthermore, the next voltage level for which specified switching levels have been defined is 2.5 V. During this transition, parts of a system may be designed for a lower supply voltage while other parts may not. This raises concerns of input-voltage tolerance, interfacing or translating, and level shifting. This application report explores the possibilities for migrating to 3.3-V and 2.5-V power supplies and discusses the implications.

Customers are successfully using a wide range of low-voltage, 3.3-V logic devices. These devices are within Texas Instruments (TI™) advanced low-voltage CMOS (ALVC), crossbar technology (CBT), crossbar technology with integrated diode (CBTD), low-voltage crossbar technology (CBTLV) and low-voltage CMOS “A” revision (LVC-A) logic families. Additionally, TI plans to release a level shifter that generates valid 3.3-V and 2.5-V signals.

The transition from 5-V to 3.3-V logic began with core logic converting first to the lower power-supply level. Although memory is still primarily at the 5-V level, it is being converted to 3.3 V, and this conversion will continue. The same method of migration is expected for 3.3 V to 2.5 V, with memory logic following core logic by several years.

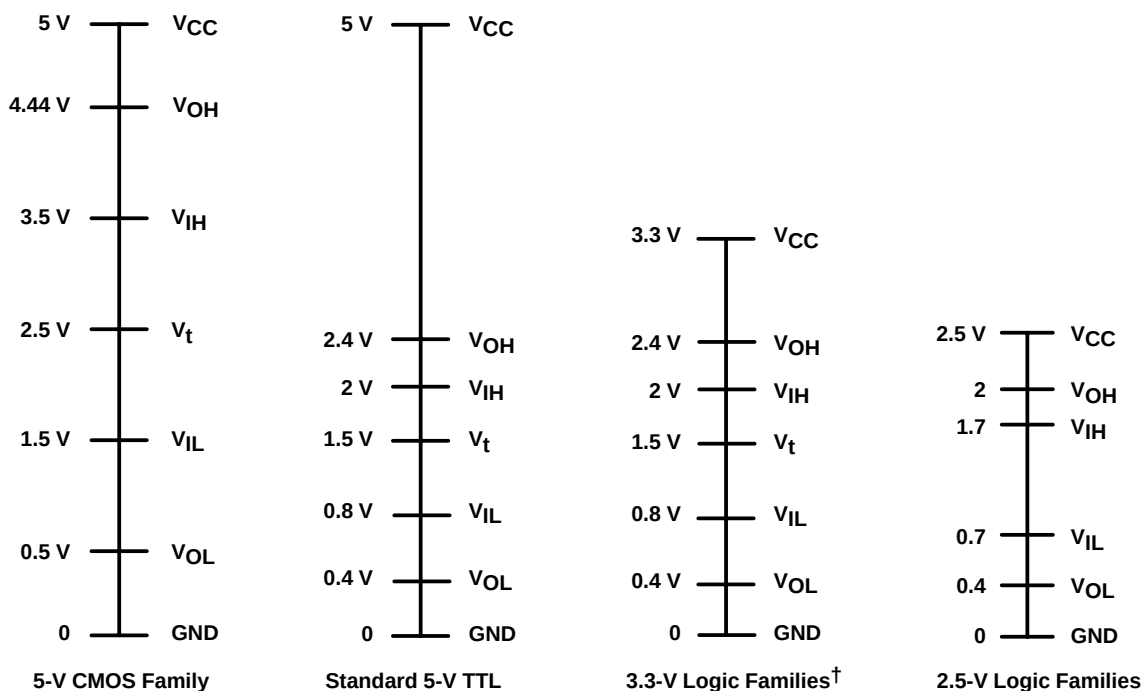
The main topics in this application report are:

- Background
- Technology
- Features and Uniqueness of Devices
- Typical Design Applications
- Laboratory Testing
- Results
- SPICE/IBIS Models
- Package Information
- Frequently Asked Questions
- Conclusion
- Glossary
- Bibliography

Background

The transition from one power-supply level to a lower one is driven primarily by a desire to reduce power consumption. For approximately the last 30 years, 5-V power supplies have been the standard for both core and memory logic. However, core logic has begun to migrate to 3.3-V power-supply levels, and memory has followed. The next commonly accepted power-supply level is 2.5 V and designers are beginning to incorporate it in their systems. This sets the stage for 1.8-V logic, for which a standard has not been established.

For each power-supply level, a standard exists for defining commonly agreed-upon levels of input and output voltages. Figure 1 shows the appropriate switching levels for 5-V, 3.3-V, and 2.5-V V_{CC} families.



† In accordance with JEDEC Standard 8-A for LV interface levels

Figure 1. Switching Levels for 5-V, 3.3-V, and 2.5-V V_{CC} Families

Technology

Table 1 lists the logic families TI produces that operate at 3.3-V V_{CC} . The process, the power-supply level for which the device was designed and optimized, and whether the device can operate at 3.3-V and 2.5-V V_{CC} levels are included.

Table 1. Logic Family Technology Summary

LOGIC FAMILY	PROCESS	OPTIMIZED POWER SUPPLY LEVEL	OPERATIONAL AT $V_{CC} = 3.3\text{ V}$	OPERATIONAL AT $V_{CC} = 2.5\text{ V}$
AHC	CMOS	5 V	Yes	Yes
ALVC	CMOS	3.3 V	Yes	Yes
CBT	CMOS [†]	5 V	Yes	Yes
CBTD	CMOS	5 V	Yes	Yes
CBTLV	CMOS	3.3 V	Yes	Yes
LVC-A	CMOS	3.3 V	Yes	Yes

[†] The CBT16232, CBT16233, and CBT16390 devices are BiCMOS.

In Table 1, CMOS process indicates that the devices contain solely CMOS circuitry. The BiCMOS process indicates that a combination of bipolar and CMOS transistors may be implemented in the circuitry.

Features and Uniqueness of Devices

When discussing interactions between different power-supply levels, the distinction between input-voltage tolerance, interfacing or translating, and level shifting is important. Input-voltage tolerance applies when a device with a lower power supply can withstand the presence of a higher voltage without being damaged. For example, a 3.3-V device drives a 2.5-V device without harming the receiver. Under this concept, there is no implication about the device being able to produce a signal compatible with the higher power-supply level. Interfacing or translating implies that a device can generate valid input and output voltage levels, even though a single power-supply level is being used. A device is a level shifter when it implements two power supplies and can produce signals that conform to the switching requirements of both the lower-voltage power supply and the higher-voltage power supply.

All devices in the families listed in Table 1 operate and function correctly when powered at 3.3-V and 2.5-V V_{CC} . The following paragraphs address how the devices interact when they are operated at one power-supply level and are exposed to signals from a device operated at a different power-supply level.

Figure 1 illustrates that a 3.3-V device can adequately drive a 2.5-V device. $V_{OL}(3.3\text{-V logic})$ (0.4 V) is less than $V_{IL}(2.5\text{-V logic})$ (0.7 V), which allows a 300-mV noise margin. Similarly, $V_{OH}(3.3\text{-V logic})$ (2.4 V) is greater than $V_{IH}(2.5\text{-V logic})$ (1.7 V), which allows for a 700-mV noise margin. Table 2 summarizes the compatibility between 3.3-V and 2.5-V devices when both are powered at 3.3-V V_{CC} .

Table 2. 3.3-V to 2.5-V Compatibility When $V_{CC} = 3.3\text{ V}$

LOGIC FAMILY	2.5-V TOLERANT	2.5-V SWITCHING LEVELS GENERATED
AHC	Yes	Yes
ALVC	Yes	Yes
CBT [†]	Yes	Yes
CBTD [†]	Yes	Yes
CBTLV [†]	Yes	Yes
LVC-A	Yes	Yes

[†] CBT, CBTD, and CBTLV families are limited by the input voltage.

A 2.5-V device cannot adequately drive a 3.3-V device. $V_{OL}(2.5\text{-V logic})$ (0.4 V) is less than $V_{IL}(3.3\text{-V logic})$ (0.8 V), which allows a 400-mV noise margin. However, $V_{OH}(2.5\text{-V logic})$ (2 V) is approximately equal to $V_{IH}(3.3\text{-V logic})$ (2 V), which theoretically allows no noise margin. Therefore, 2.5-V devices should not be used to drive 3.3-V devices. Table 3 summarizes the compatibility between 2.5-V and 3.3-V devices when both are powered at 2.5-V V_{CC} .

Table 3. 2.5-V to 3.3-V Compatibility When $V_{CC} = 2.5\text{ V}$

LOGIC FAMILY	3.3-V TOLERANT	3.3-V SWITCHING LEVELS GENERATED
AHC	Yes	No
ALVC	No	No
CBT	Yes	No
CBTD	Yes	No
CBTLV	Yes	No
LVC-A	Yes	No

Typical Design Applications

When migrating from 5-V power supplies to 3.3-V power supplies, migration from 3.3 V to 2.5 V is expected to occur in stages. Specifically, core logic will make the transition to 2.5 V, while memory and I/Os probably will lag. The configuration in Figure 2 likely will be commonplace.

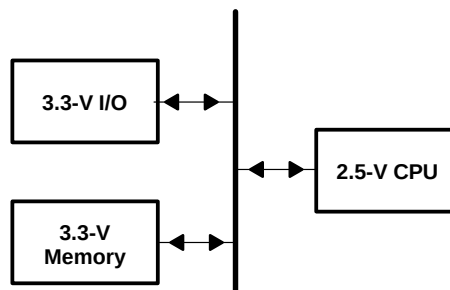


Figure 2. Typical Anticipated 3.3-V/2.5-V Architecture

The CPU operates at 2.5-V V_{CC} and must communicate with a 3.3-V V_{CC} memory and I/O. For all unidirectional data flow from the memory and I/O to the CPU, e.g., reading from memory and receiving input from the I/O, any device that is powered at 3.3-V V_{CC} is acceptable. However, for all communication and data transfer from the CPU to memory or the I/O, such as address buffering and printing, only a device with level-shifting capabilities that can generate true 3.3-V signals from a 2.5-V input should be used.

Laboratory Testing

To demonstrate the ability of TI devices to operate at both 3.3-V and 2.5-V V_{CC} levels, several devices were tested to determine typical propagation delay times. Because typical values were desired, V_{CC} was set to 3.3 V and 2.5 V, and the ambient temperature was 25°C. Tables 4 and 5 show the conditions under which the measurements were taken and the results obtained.

Results

Data in Tables 4 and 5 show that under the same conditions a device's propagation delay increases as V_{CC} is reduced and decreases as the capacitive load is decreased.

Table 4. Typical Propagation Delays When $V_{CC} = 3.3$ V

LOGIC FAMILY	DIRECTION	CAPACITIVE LOAD (pF)	t_{pd} OR t_{PLH}/t_{PHL} (TYPICAL)
AHC245	A $\longleftrightarrow$ B	30	4.3/3.7 ns
		50	4.6/3.9 ns
AHC16245	A $\longleftrightarrow$ B	30	4.3/3.7 ns
		50	6.8/5.6 ns
ALVC16245	A to B	30	1.4/1.7 ns
		50	1.8/2.2 ns
CBT	A $\longleftrightarrow$ B	50	750 ps
CBTD	A $\longleftrightarrow$ B	50	750 ps
CBTLV3245	A $\longleftrightarrow$ B	50	600 ps
LVCH245A	A $\longleftrightarrow$ B	50	2.7/3.1 ns
LVCH16245A	A to B	30	2.1/2.2 ns
		50	2.8/2.5 ns

Table 5. Typical Propagation Delays When $V_{CC} = 2.5\text{ V}$

LOGIC FAMILY	DIRECTION	CAPACITIVE LOAD (pF)	t_{pd} OR t_{PLH}/t_{PHL} (TYPICAL)
AHC245	A $\longleftrightarrow$ B	30	5.6/4.6 ns
		50	6/5 ns
AHC16245	A $\longleftrightarrow$ B	30	5.6/4.5 ns
		50	9.4/7.2 ns
ALVCH16245	A to B	30	2.4/2.5 ns
		50	3.6/2.8 ns
CBT	A $\longleftrightarrow$ B	50	900 ps
CBTD	A $\longleftrightarrow$ B	50	900 ps
CBTLV3245	A $\longleftrightarrow$ B	30	500 ps
		50	700 ps
LVCH245A	A to B	50	3.1/3.6 ns
	B to A		3.1/3.5 ns
LVCH16245A	A to B	30	2.8/2.7 ns
		50	4.1/3.1 ns

SPICE/IBIS Models

SPICE and IBIS models are available for certain devices. Appendix A lists SPICE and IBIS models for given functions within a logic family.

The SPICE model is a level-13 model that consists of the input and output stages and can be obtained by contacting your local TI Sales Representative. The IBIS model consists of the input and output stages and can be obtained at the TI web site <http://www.ti.com/sc/docs/asl/models/ibis.htm>.

Package Information

The devices discussed in this application report are available in a variety of packages, including plastic dual-in-line package (PDIP), quarter-size outline package (QSOP), small-outline integrated circuit (SOIC), small-outline transistor (SOT), shrink small-outline package (SSOP), thin shrink small-outline package (TSSOP), and thin very small-outline package (TVSOP). TI's Logic Selection Guide, literature number SDYU001, lists devices and packages in which they are available.

Frequently Asked Questions

- Question:** How do I reconcile differences between the 3.3-V part of my system and the 2.5-V part?
- Answer:** When designing with multiple power-supply levels in a single system, ensure that the devices that are powered with the lower-voltage power supply are not damaged when interfacing with the part of the system that is powered by the higher-voltage power supply. This is accomplished by ensuring that all devices are voltage tolerant of the other devices. For the purposes of this application report, any 2.5-V device must be 3.3-V tolerant to ensure that no damage occurs to the 2.5-V device.
- Question:** With the CBT logic family, I could interface the 5-V part of my system with the 3.3-V part of my system by adding a diode between the external V_{CC} and the output-enable terminals. Can I use a similar method with the CBTLV family to interface between the 3.3-V part and 2.5-V part of my system?
- Answer:** To drive the CBTLV output levels fully to the rail, a PMOS transistor was added to the circuitry. This PMOS and its associated circuitry prevent the CBTLV family of devices from level translating between 3.3 V and 2.5 V. However, the CBT family is capable of performing this function. Please see item 1 in the bibliography.
- Question:** How do I get a copy of the SPICE and IBIS models?
- Answer:** The SPICE models can be obtained by contacting your local TI Sales Representative. The IBIS models can be obtained at <http://www.ti.com/sc/docs/asl/models/ibis.htm>.

Conclusion

As systems migrate from 3.3-V to 2.5-V power supplies, issues of input-voltage tolerance, interfacing or translating, and level shifting must be addressed. A 3.3-V device can drive a 2.5-V device, but a 2.5-V device cannot drive a 3.3-V device due to switching-level incompatibilities. TI offers a variety of logic families that are capable of operating at 3.3-V and 2.5-V V_{CC} levels.

Glossary

AHC	Advanced High-Speed CMOS
ALVC	Advanced Low-Voltage CMOS
CBT	Crossbar Technology
CBTLV	Low-Voltage Crossbar Technology
CPU	Central Processing Unit
IBIS	I/O Buffer Information Specification
I/O	Input/Output
LVC-A	Low-Voltage CMOS “A” Revision
LVTTL	Low-Voltage Transistor-Transistor Logic
PDIP	Plastic Dual-In-line Package
QSOP	Quarter-Size Outline Package
SOIC	Small-Outline Integrated Circuit
SOT	Small-Outline Transistor
SPICE	Simulation Program With Integrated-Circuit Emphasis
SSOP	Shrink Small-Outline Package
TI	Texas Instruments
TSSOP	Thin Shrink Small-Outline Package
TVSOP	Thin Very Small-Outline Package

Bibliography

1. 3.3-V to 2.5-V Translation with Texas Instruments Crossbar Technology, literature number SCDA004
2. Advanced Bus Interface SPICE I/O Models, 1995, literature number SCBD004A
3. AHC/AHCT, HC/HCT, and LV CMOS Logic Data Book, 1996, literature number SCLD004
4. CBT Bus Switches, Crossbar Technology Data Book, 1996, literature number SCDD001A
5. Logic Selection Guide, literature number SDYU001 (revised quarterly)
6. Low-Voltage CMOS Logic Data Book, 1997, literature number SCBD152
7. Low-Voltage Logic Data Book, 1996, literature number SCBD003B
8. Semiconductor Group Package Outlines Reference Guide, literature number SSYU001

Appendix A

Available SPICE and IBIS Models

LOGIC FUNCTION	LOGIC FAMILY [†]			
	AHC	ALVC	CBT	LVC-A
'00	S	NA	NA	S/I
'02	S	NA	NA	S/I
'04	S	NA	NA	S/I
'08	S	NA	NA	S/I
'10	NA	NA	NA	S/I
'14	S	NA	NA	S/I
'32	—	NA	NA	S/I
'74	—	NA	NA	S/I
'86	—	NA	NA	S/I
'112	NA	NA	NA	S/I
'125	S	NA	NA	S/I
'126	S	NA	NA	S
'137	NA	NA	NA	S/I
'138	—	NA	NA	S/I
'139	—	NA	NA	S
'157	—	NA	NA	S/I
'158	NA	NA	NA	S
'240	—	NA	NA	S
'241	NA	NA	NA	S
'244	—	NA	NA	S/I
'245	—	NA	NA	S
'257	NA	NA	NA	S/I
'258	NA	NA	NA	S
'373	—	NA	NA	S
'374	—	NA	NA	S/I
'540	—	NA	NA	S
'541	—	NA	NA	S
'543	NA	NA	NA	S/I
'544	NA	NA	NA	S
'573	—	NA	NA	S
'574	—	NA	NA	S
'646	NA	NA	NA	S/I
'652	NA	NA	NA	S/I
'821	NA	NA	NA	S
'823	NA	NA	NA	S
'827	NA	NA	NA	S
'828	NA	NA	NA	S

LOGIC FUNCTION	LOGIC FAMILY [†]			
	AHC	ALVC	CBT	LVC-A
'841	NA	NA	NA	S
'843	NA	NA	NA	S
'861	NA	NA	NA	S
'863	NA	NA	NA	S
'2952	NA	NA	NA	S/I
'16233	NA	NA	S	NA
'16240	—	S	NA	S/I
'162240	NA	S	NA	NA
'16241	NA	NA	NA	S
'16244	—	S/I	NA	S/I
'162244	NA	S/I	NA	S/I
'16245	—	S/I	NA	S/I
'162245	NA	S	NA	—
'16260	NA	S	NA	NA
'162260	NA	S	NA	NA
'162268	NA	S	NA	NA
'16269	NA	S	NA	NA
'162269	NA	—	NA	NA
'16270	NA	S	NA	NA
'16271	NA	S	NA	NA
'16272	NA	S	NA	NA
'16280	NA	S	NA	NA
'162280	NA	—	NA	NA
'16282	NA	S	NA	NA
'162282	NA	—	NA	NA
'16334	NA	S/I	NA	NA
'162334	NA	S/I	NA	NA
'16344	NA	S	NA	NA
'162344	NA	S	NA	NA
'16373	—	S	NA	S/I
'162373	NA	S	NA	NA
'16374	—	S/I	NA	S/I
'162374	NA	S	NA	NA
'16409	NA	S	NA	NA
'162409	NA	—	NA	NA
'16500	NA	S	NA	NA
'16501	NA	S	NA	NA

[†] S = SPICE model exists; I = IBIS model exists; NA = Not applicable, indicating that the device does not exist for that particular family; — = neither SPICE nor IBIS model exists.

Available SPICE and IBIS Models (Continued)

LOGIC FUNCTION	LOGIC FAMILY [†]			
	AHC	ALVC	CBT	LVC-A
'16524	NA	—	NA	NA
'16525	NA	—	NA	NA
'16540	—	S	NA	S/I
'162540	NA	S	NA	NA
'16541	—	S	NA	S/I
'162541	NA	S	NA	NA
'16543	NA	S	NA	S/I
'16600	NA	S	NA	NA
'16601	NA	S	NA	NA
'162601	NA	S/I	NA	NA
'16646	NA	S	NA	S/I
'16652	NA	S	NA	S/I
'16721	NA	S/I	NA	NA
'162721	NA	S/I	NA	NA
'16820	NA	S	NA	NA
'162820	NA	S/I	NA	NA
'16821	NA	S/I	NA	NA
'16823	NA	S/I	NA	NA
'16825	NA	S	NA	NA

LOGIC FUNCTION	LOGIC FAMILY [†]			
	AHC	ALVC	CBT	LVC-A
'16827	NA	S/I	NA	NA
'162827	NA	S/I	NA	NA
'16828	NA	S	NA	NA
'16830	NA	S/I	NA	NA
'162830	NA	—	NA	NA
'16831	NA	—	NA	NA
'162831	NA	—	NA	NA
'16832	NA	—	NA	NA
'162832	NA	—	NA	NA
'16835	NA	S/I	NA	NA
'162835	NA	S/I	NA	NA
'16836	NA	S/I	NA	NA
'162836	NA	S/I	NA	NA
'16841	NA	S	NA	NA
'162841	NA	—	NA	NA
'16843	NA	S	NA	NA
'16863	NA	—	NA	NA
'16901	NA	S	NA	NA
'16952	NA	S	NA	S/I

[†] S = SPICE model exists; I = IBIS model exists; NA = Not applicable, indicating that the device does not exist for that particular family; — = neither SPICE nor IBIS model exists.

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Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading, regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a type number as explained in the following example.

EXAMPLE: SN 74LVC244A DW R

Prefix

SN = Standard prefix
SNJ = Compliant to MIL-PRF-38535 (QML)

Unique Circuit Description

MUST CONTAIN SEVEN TO FOURTEEN CHARACTERS

Examples: 74LV00A
74LVC16373A
74LVCHR162245A

Package

MUST CONTAIN ONE TO THREE LETTERS

D, DW, NS = plastic small-outline package (SOIC)
DB, DL = plastic shrink small-outline package (SSOP)
DBV, DCK = plastic small-outline transistors (SOT)
DGG, PW = plastic thin shrink small-outline package (TSSOP)
DGV = plastic thin very small-outline package (TVSOP)
FK = leadless ceramic chip carrier (LCCC)
J = ceramic dual-in-line package (CDIP)
W = ceramic flat package (CFP)
(from pin-connection diagram on individual data sheet)

Tape and Reel Packaging

Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

Blank = Not taped and reeled
R = Standard tape and reel[†] (DGG and DGV are supplied in tape and reel only)

The purpose of tape-and-reel packing is to position components so they can be placed automatically. Components such as, but not limited to, diodes, capacitors, resistors, transistors, inductors, and integrated circuits can be packed in this manner.

The packing materials include a carrier tape, cover tape, and a reel. The normal dimensions for these items are listed in Table 1.

[†] All reeled material previously designated LE is reeled left embossed, but an R designator is used.

Table 1. Normal Dimensions of Packing Materials

CARRIER-TAPE WIDTH (mm)	COVER-TAPE WIDTH (mm)	REEL WIDTH (mm)	REEL DIAMETER (mm)
8	5.4	9.0	178
12	9.2	12.4	330
16	13.3	16.4	330
24	21.0	24.4	330
32	25.5	32.4	330
44	37.5	44.4	330
56	49.5	56.4	330

All material meets or exceeds industry guidelines for ESD protection.

Dimensions are selected based on package size and design configurations. All dimensions are established to be within the recommendations of the Electronics Industry Association Standard EIA-481-1,2,3.

Common dimensions are carrier-tape width, pocket pitch, and quantity per reel (see Figure 1 and Table 2).

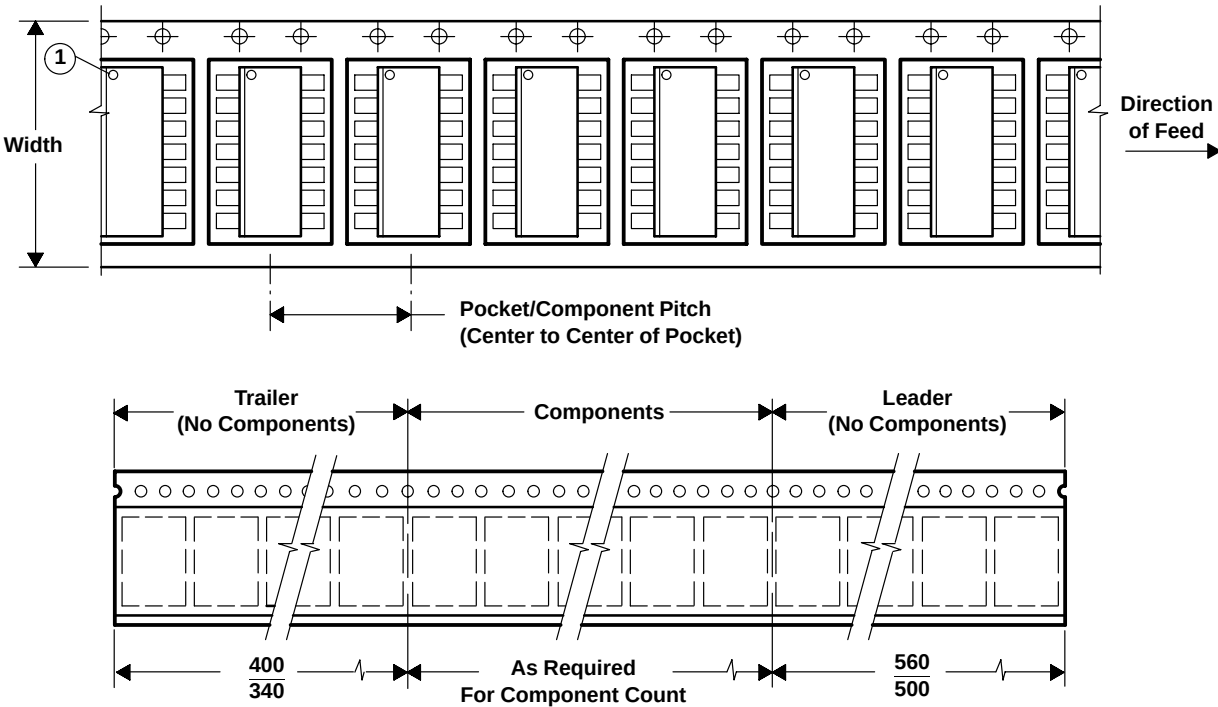


Figure 1. Typical Carrier-Tape Design

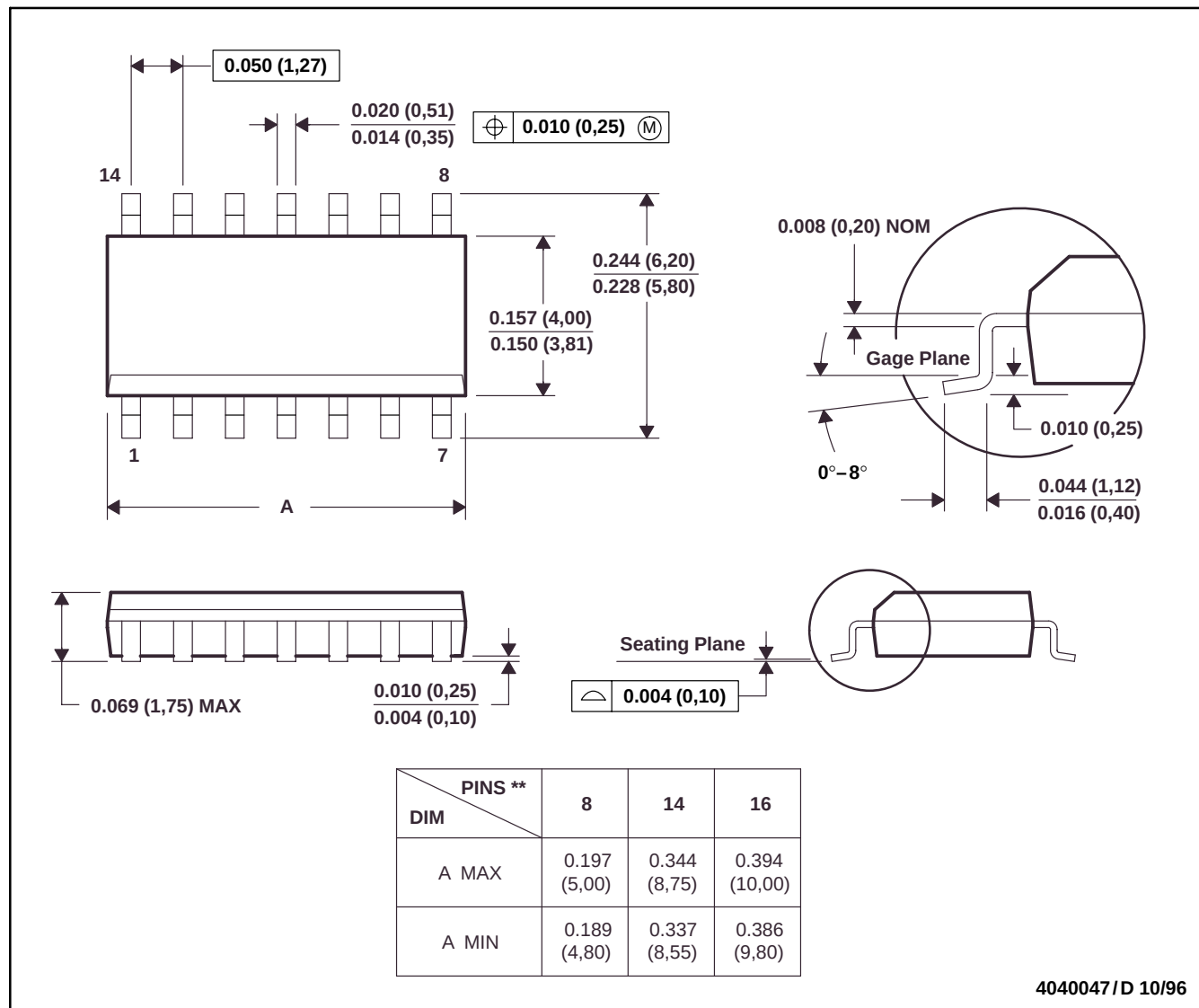
Table 2. Selected Tape-and-Reel Specifications

PACKAGE		NO. OF PINS	CARRIER-TAPE WIDTH (mm)	POCKET PITCH (mm)	QTY/REEL
SOIC	D	14	16.00	8.00	2500
		16	16.00	8.00	2500
	DW	16	16.00	8.00/12.00	2000
		20/24	24.00	12.00	2000
SOT	DBV	5	8.00	4.00	3000
	DCK	5	8.00	4.00	3000
SSOP	DB	14/16	16.00	12.00	2000
		20	16.00	12.00	2000
	DL	48	32.00	16.00	1000
TSSOP	DGG	48	24.00	12.00	2000
	PW	8	16.00	8.00	2000
		14/16	16.00	8.00	2000
		20	16.00	8.00	2000
TVSOP	DGV	14	16.00	8.00	2000
		16	16.00	8.00	2000
		20	16.00	8.00	2000
		48	16.00	8.00	2000

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



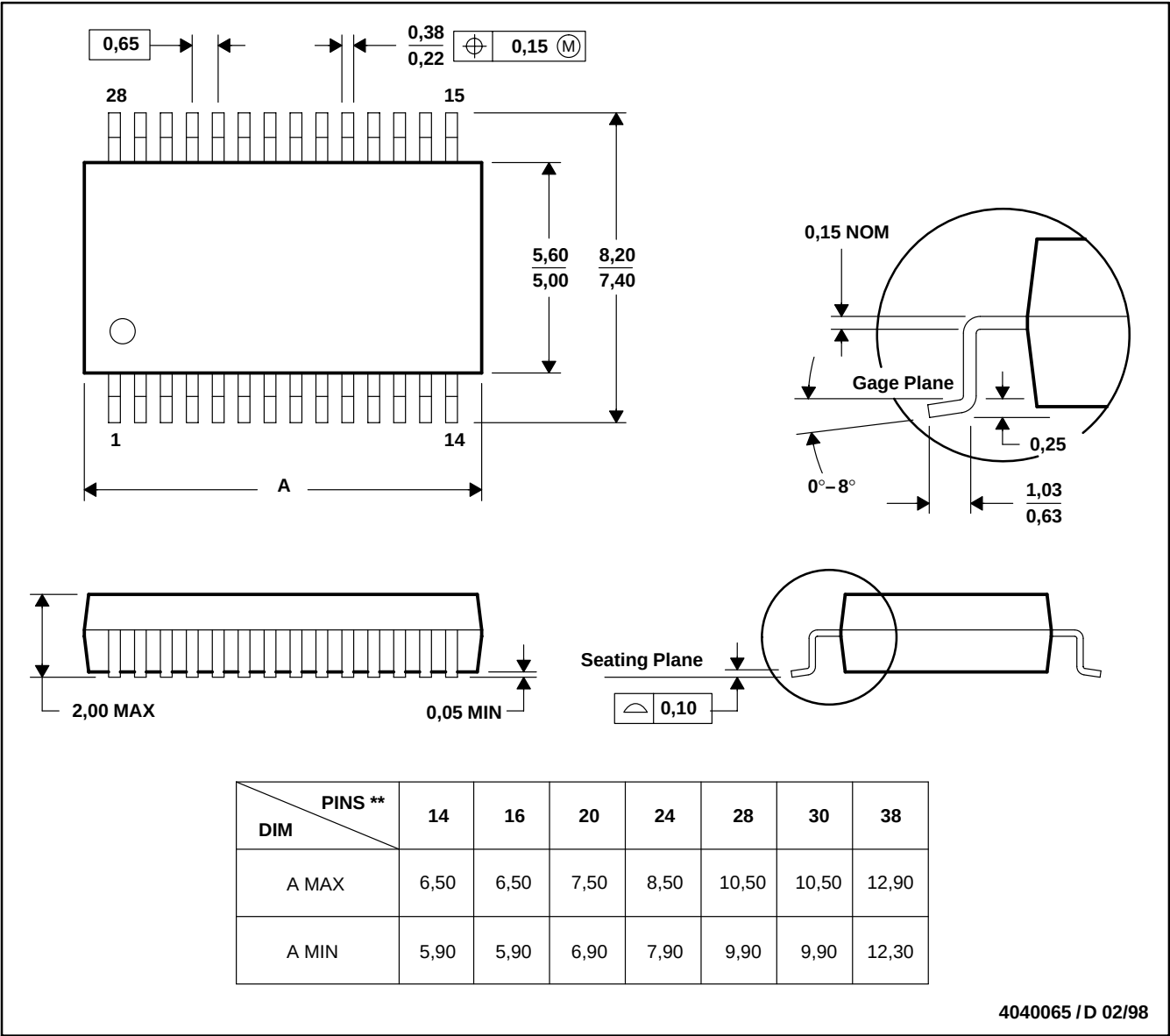
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012

MECHANICAL DATA

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

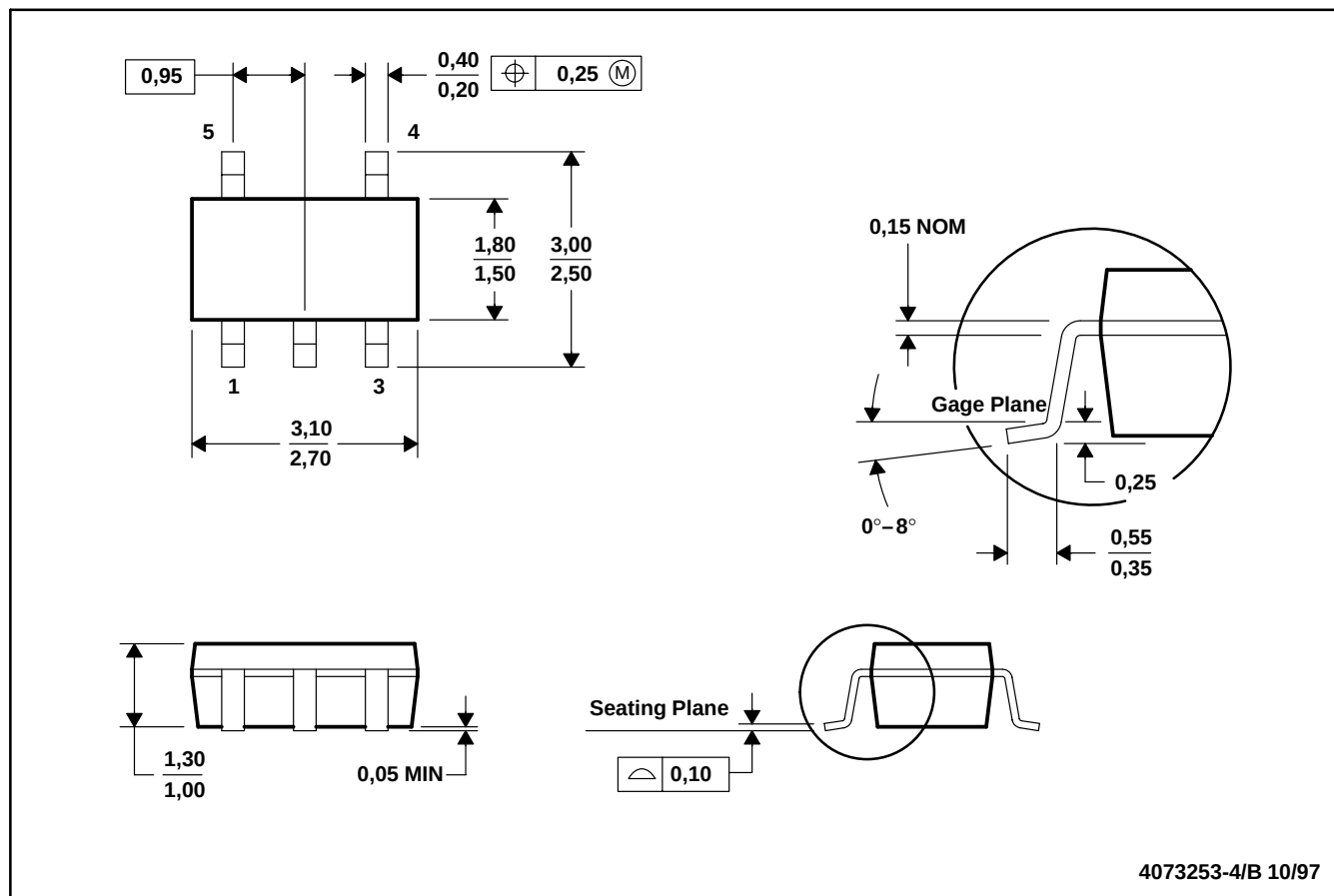
28 PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

DBV (R-PDSO-G5)

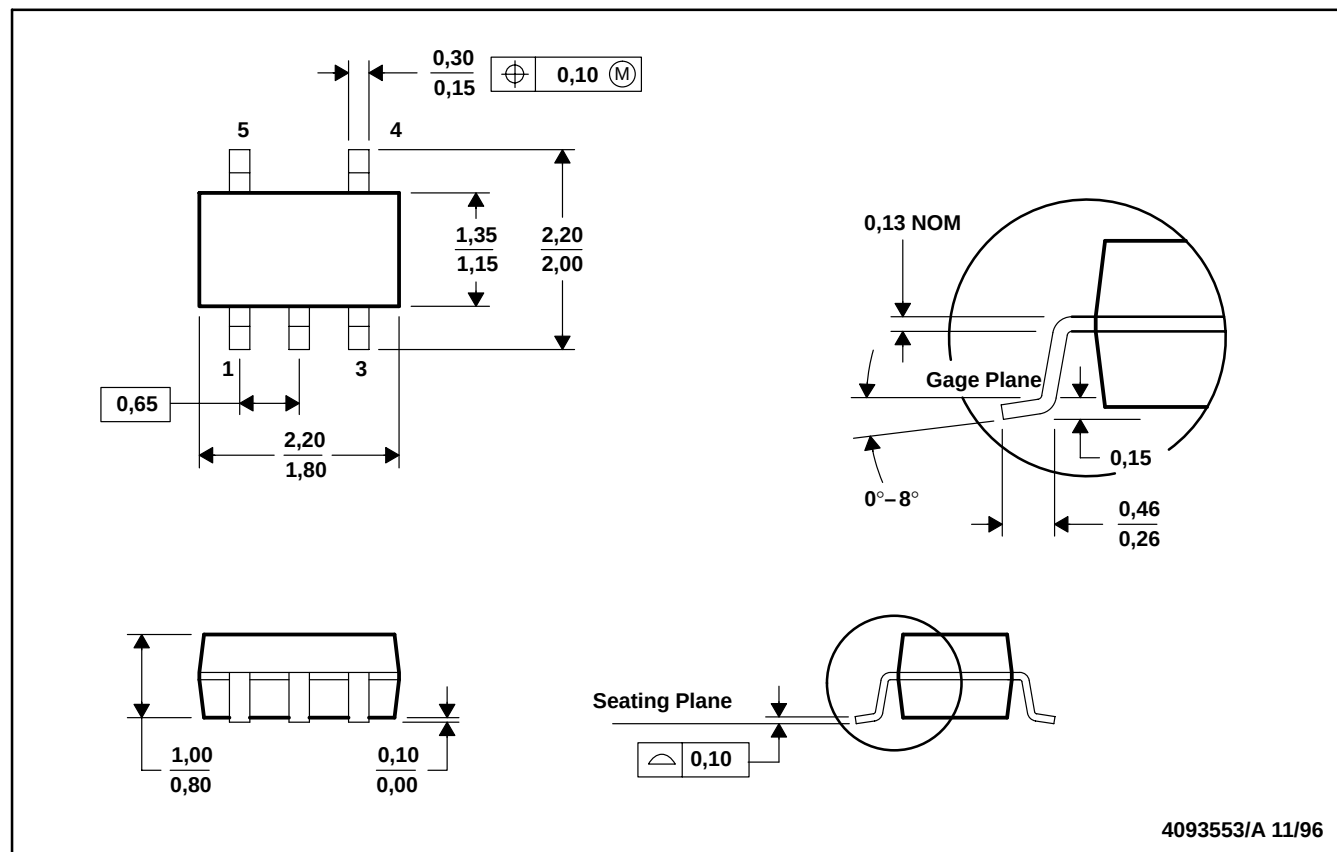
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions include mold flash or protrusion.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

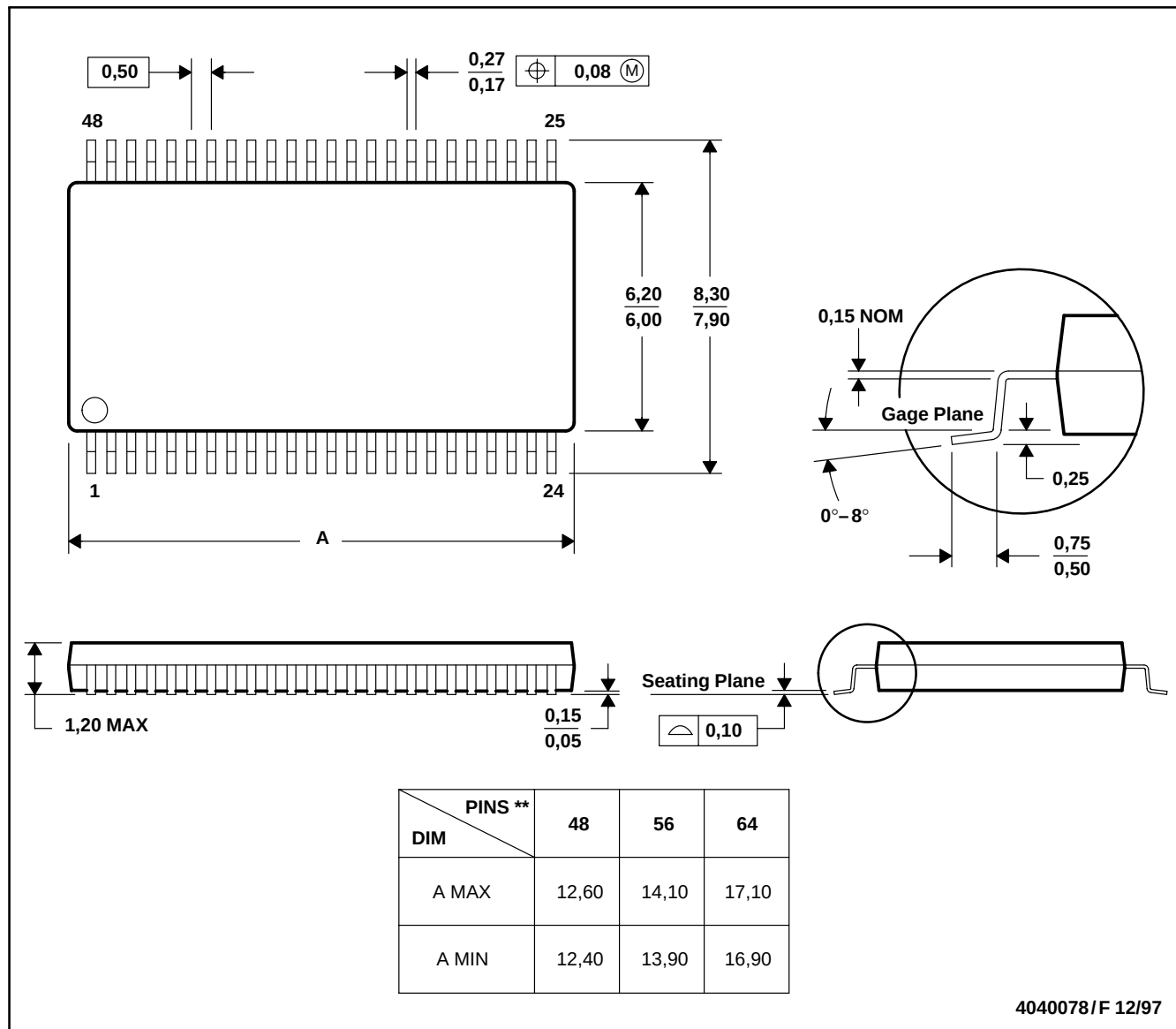


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions include mold flash or protrusion.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN

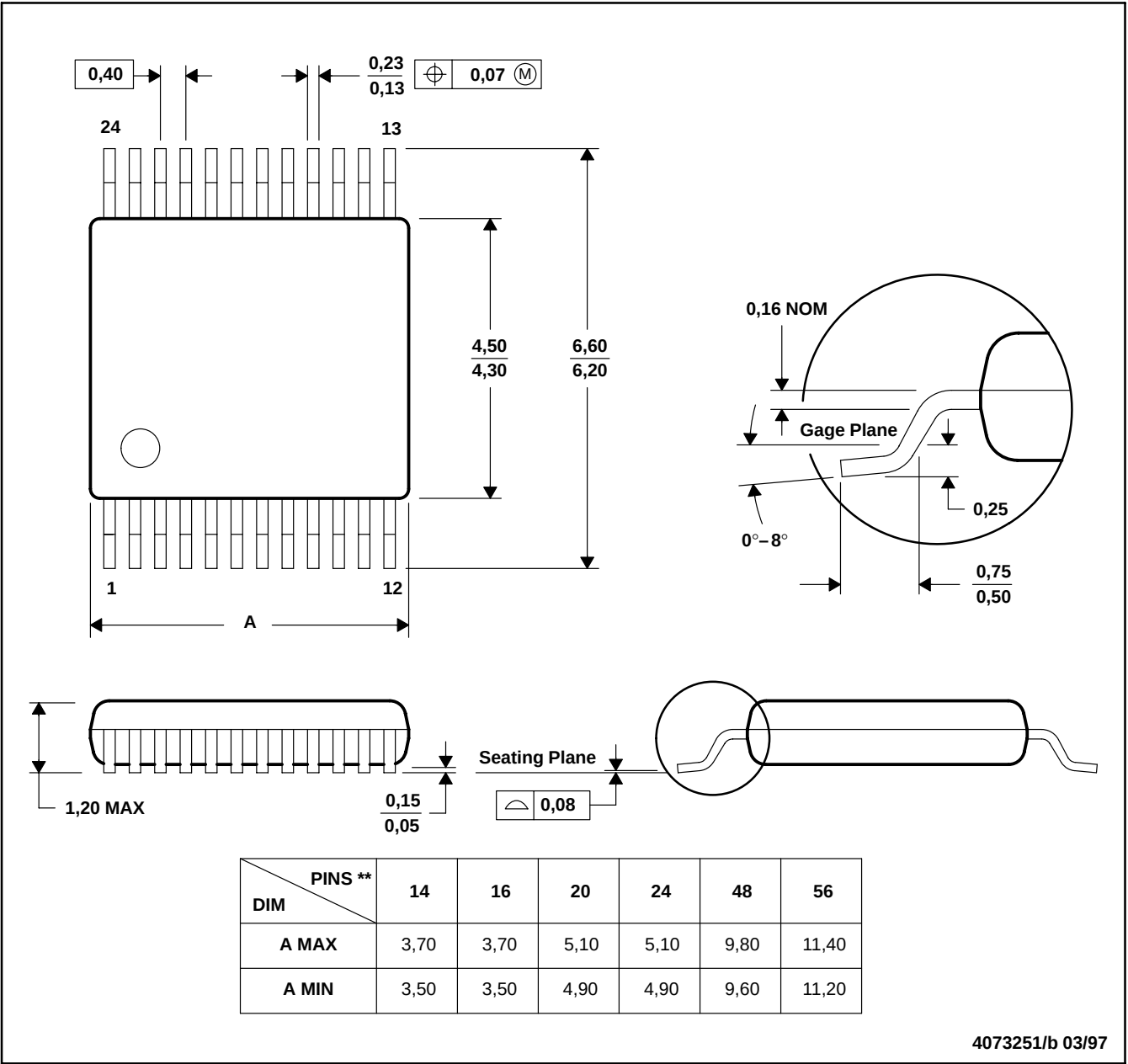


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

24 PIN SHOWN

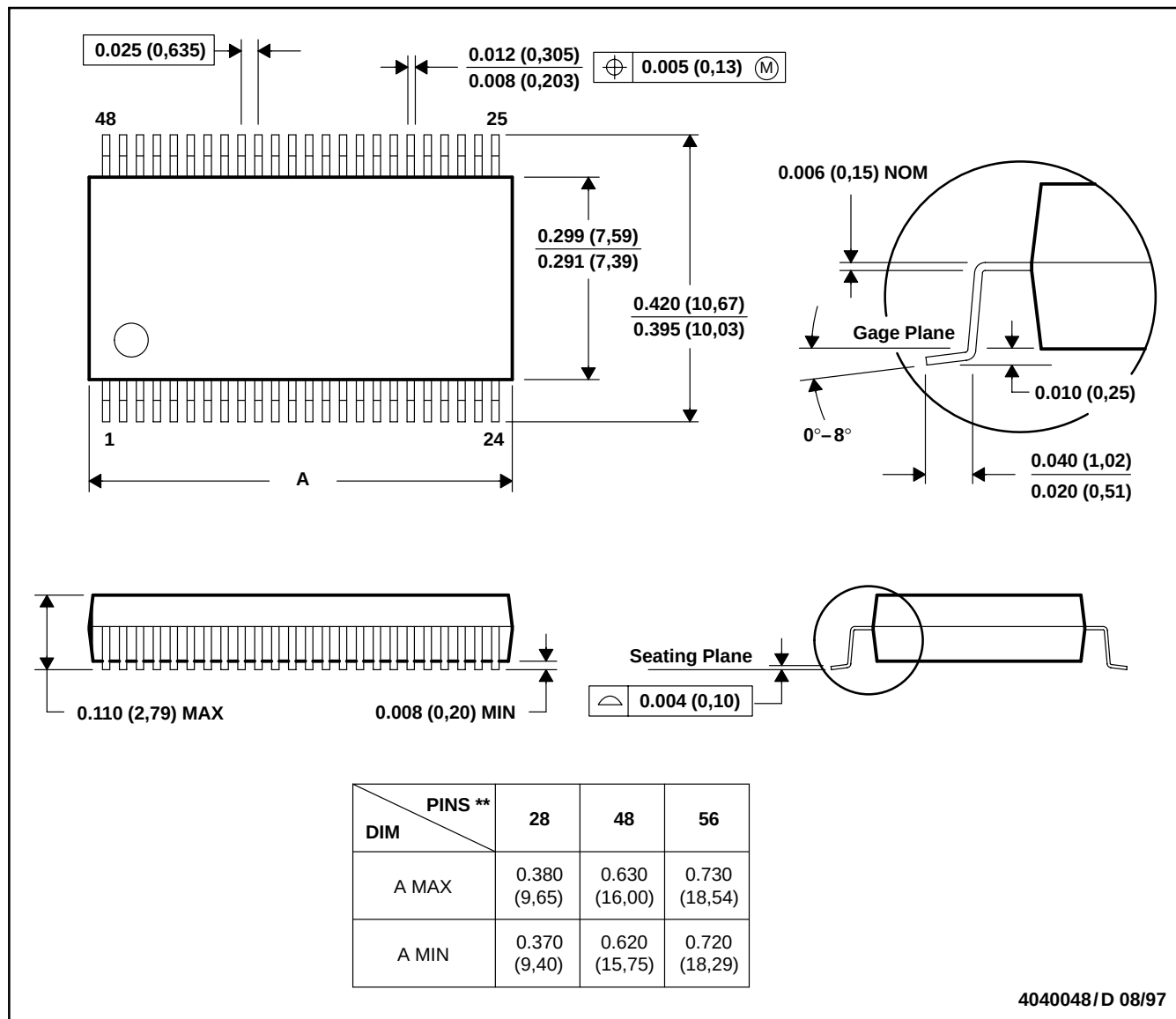


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 - D. The 24 and 48 pins falls within JEDEC MO-153 and the 14, 16, 20, and 56 pins falls within JEDEC MO-194.

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48-PIN SHOWN

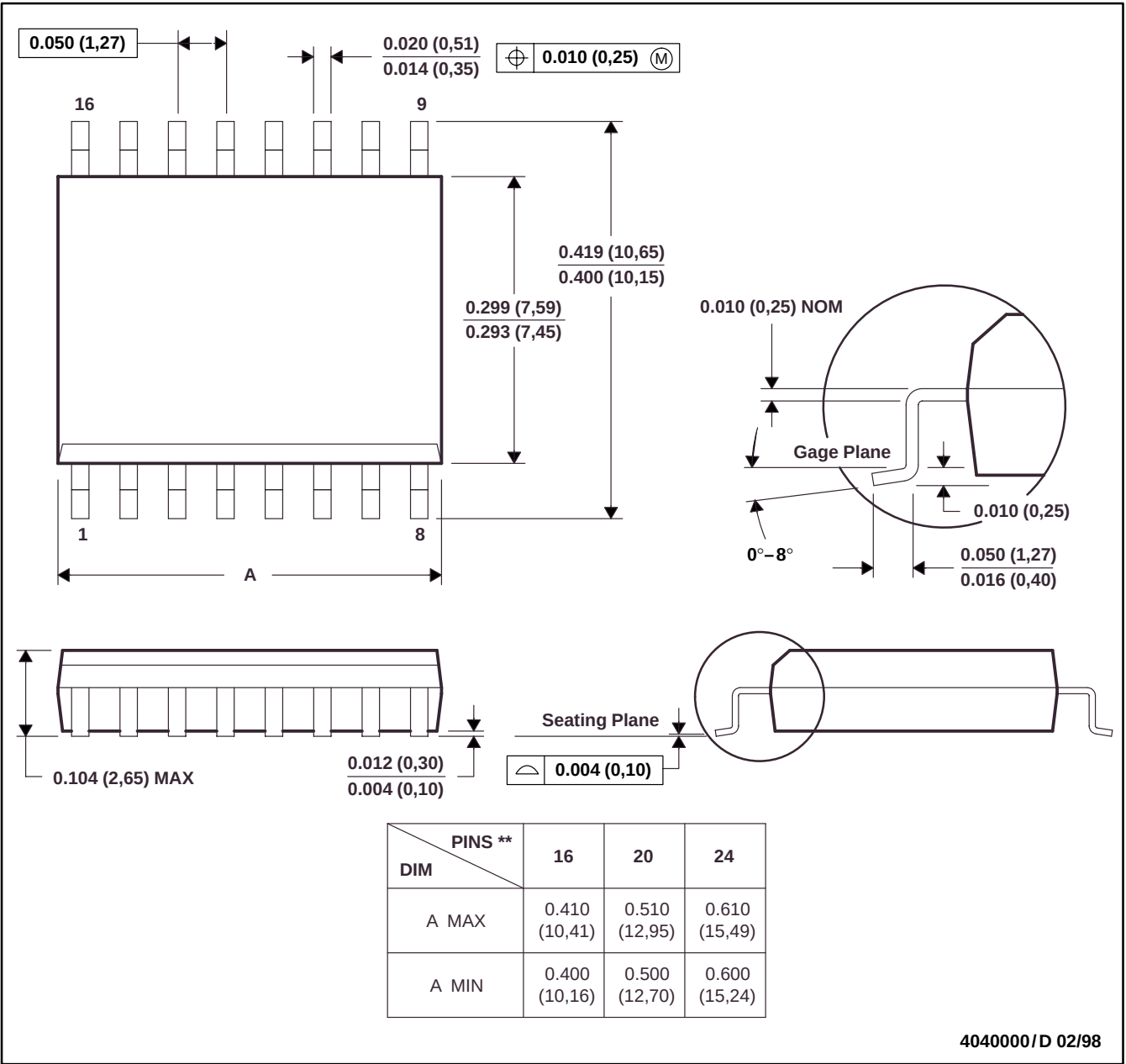


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN

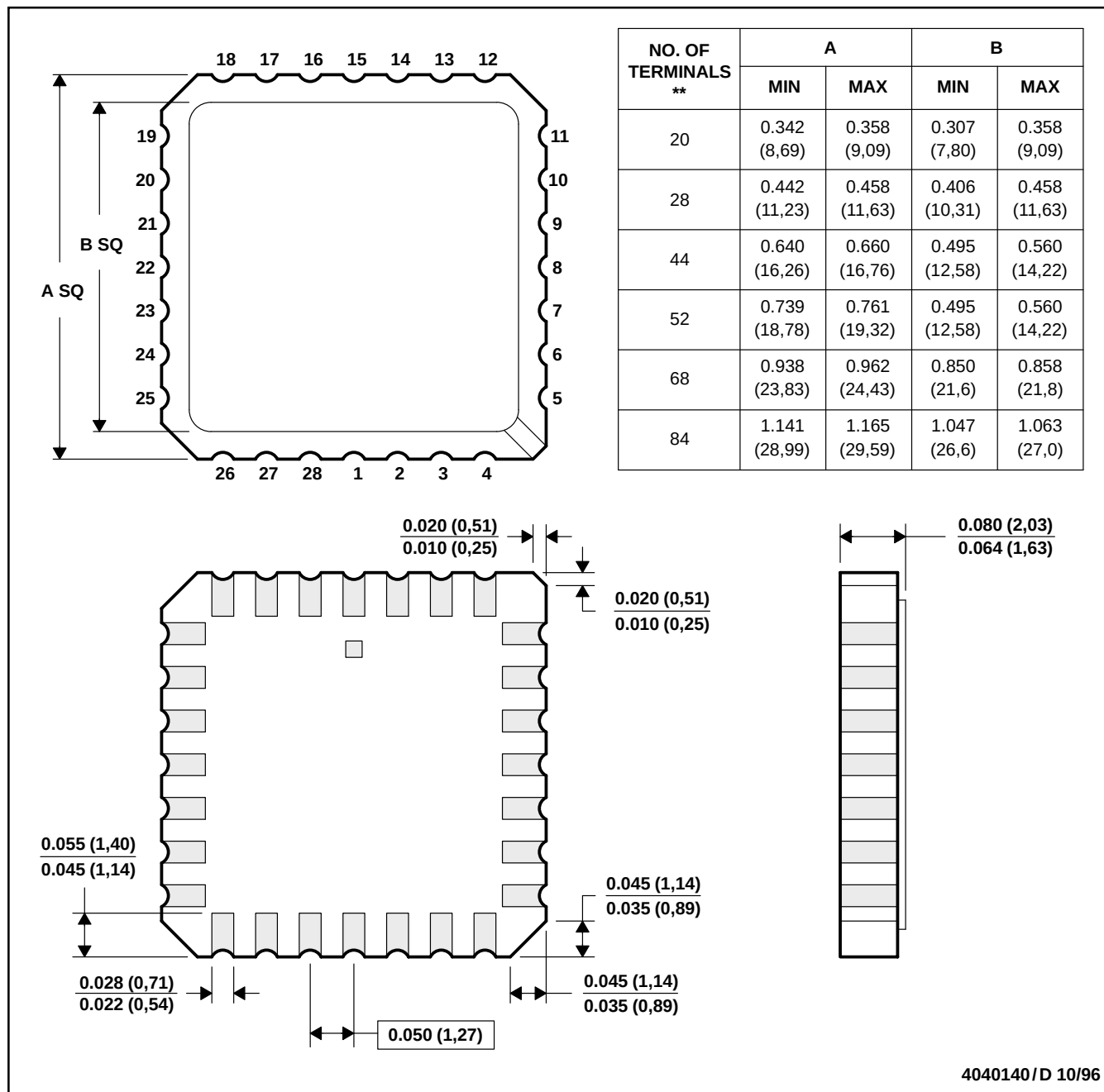


- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

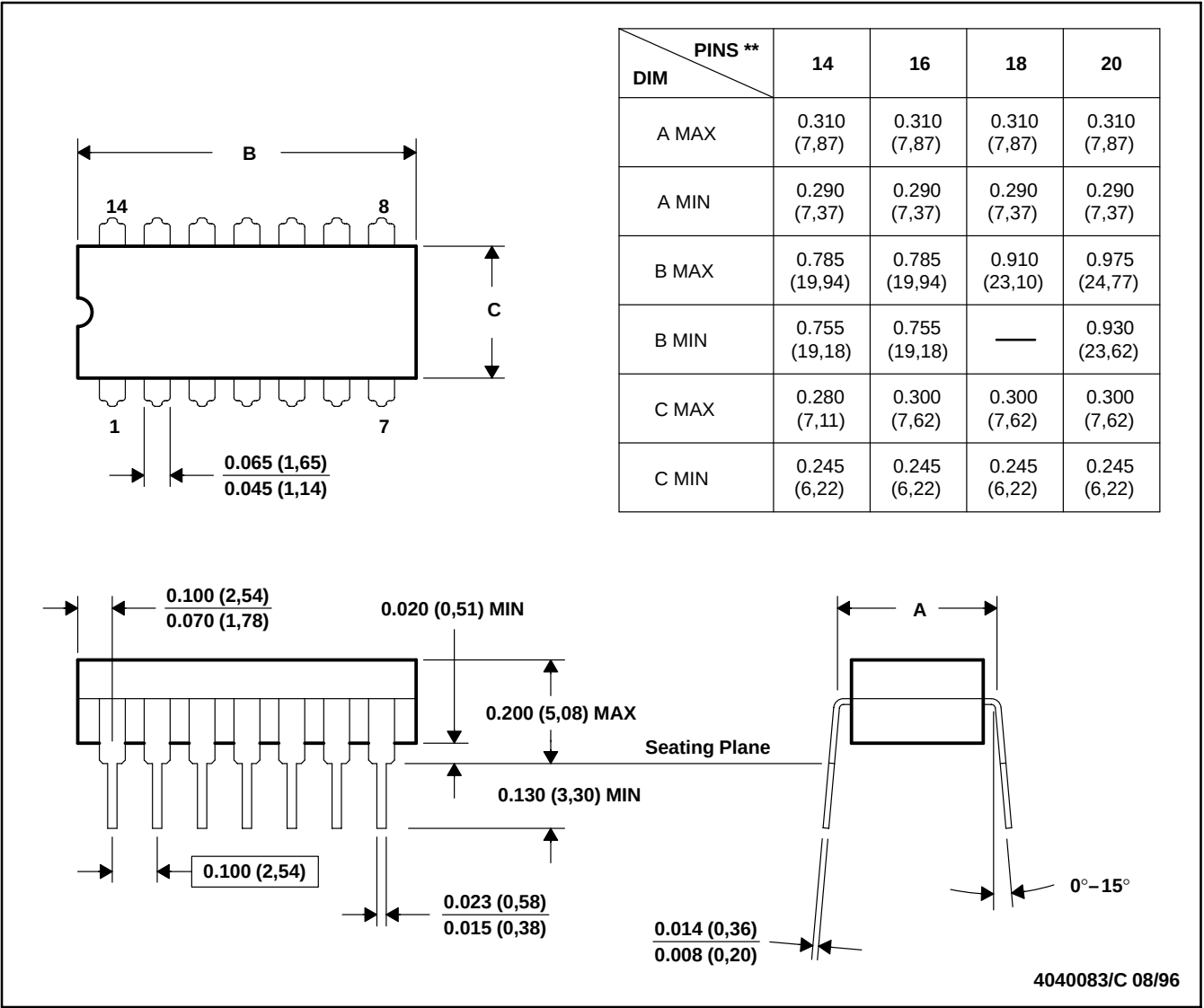


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

14 PIN SHOWN

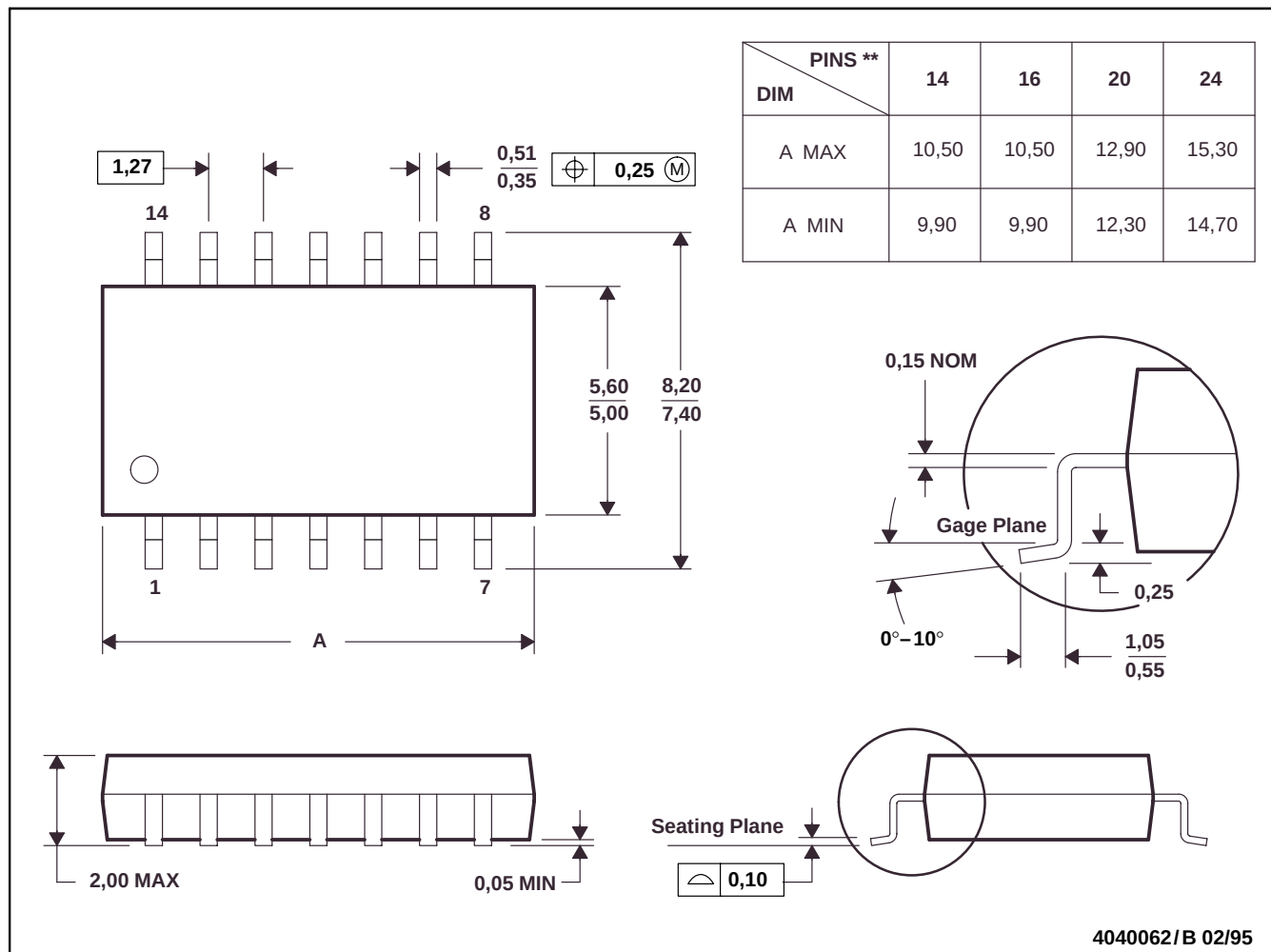


- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, and GDIP1-T20

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN

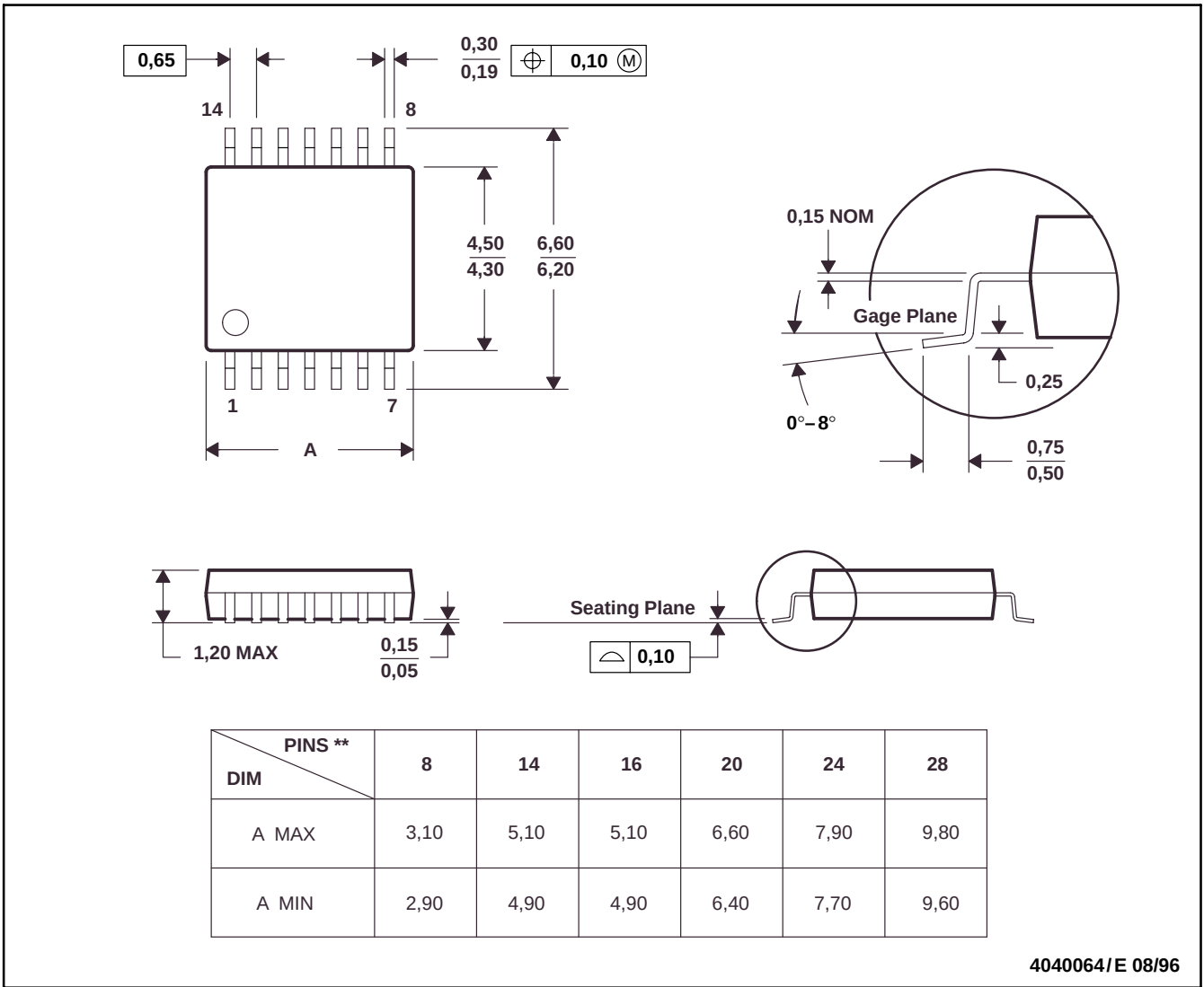


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

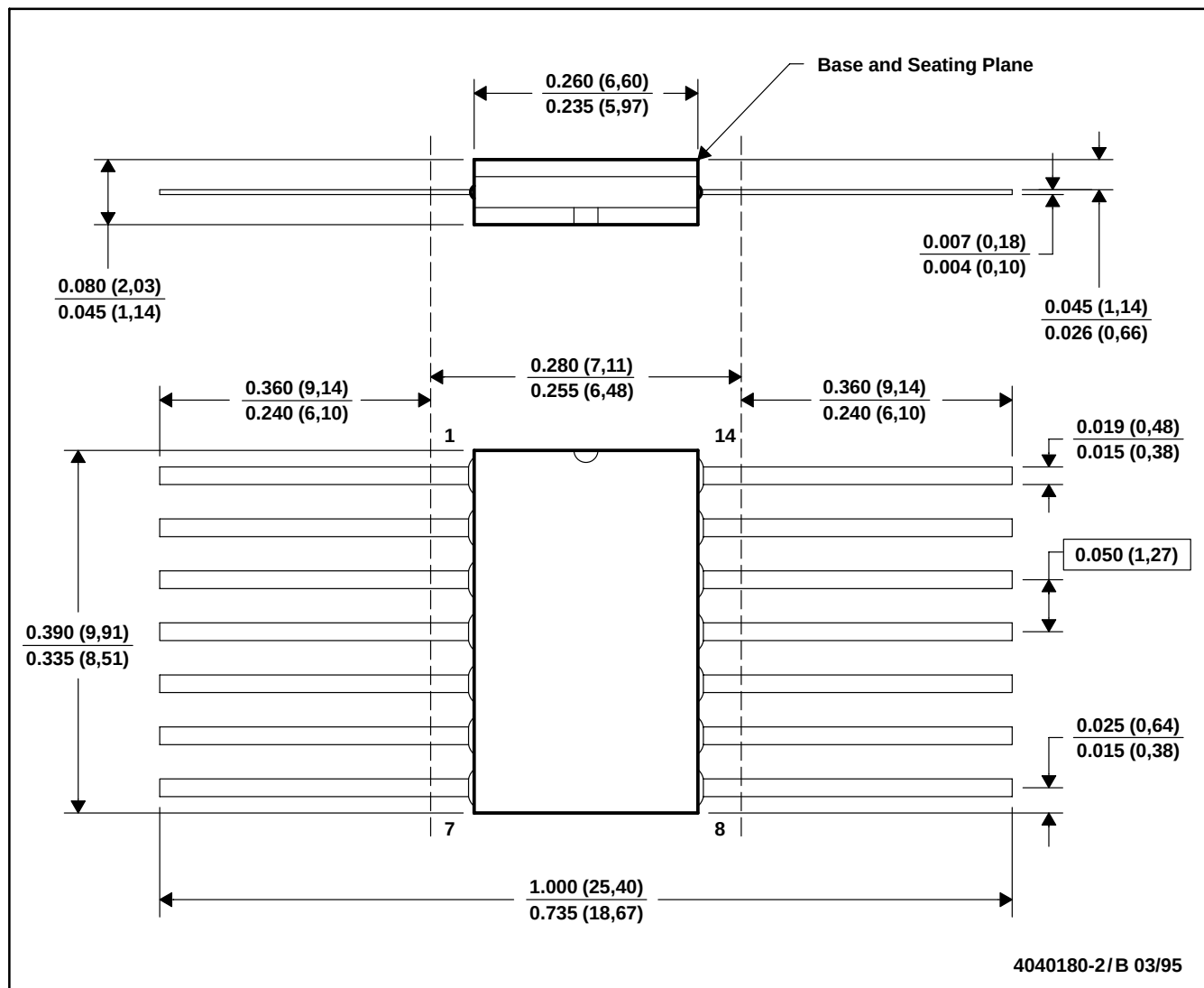
14 PIN SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. Falls within JEDEC MO-153

W (R-GDFP-F14)

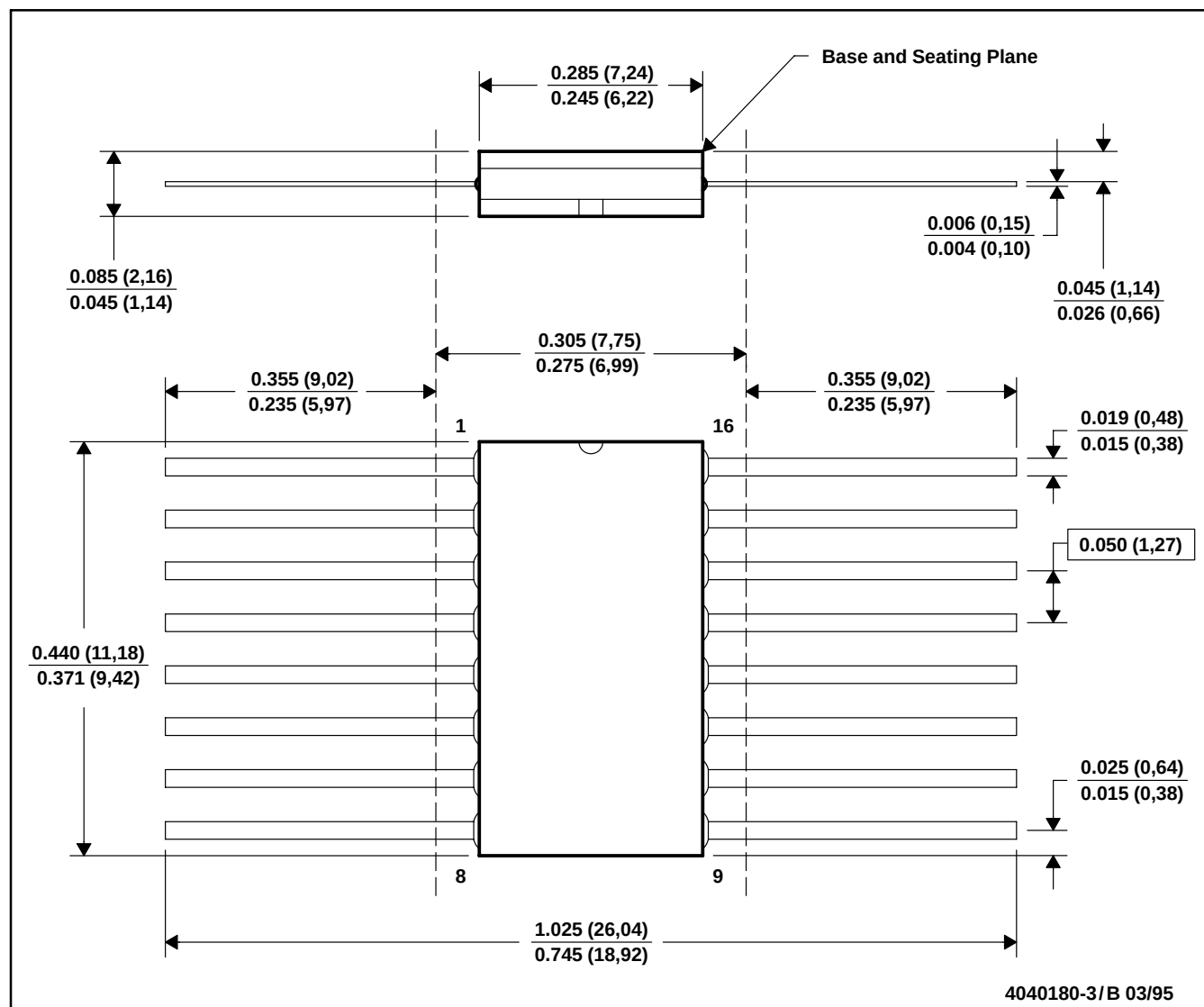
CERAMIC DUAL FLATPACK



MECHANICAL DATA

W (R-GDFP-F16)

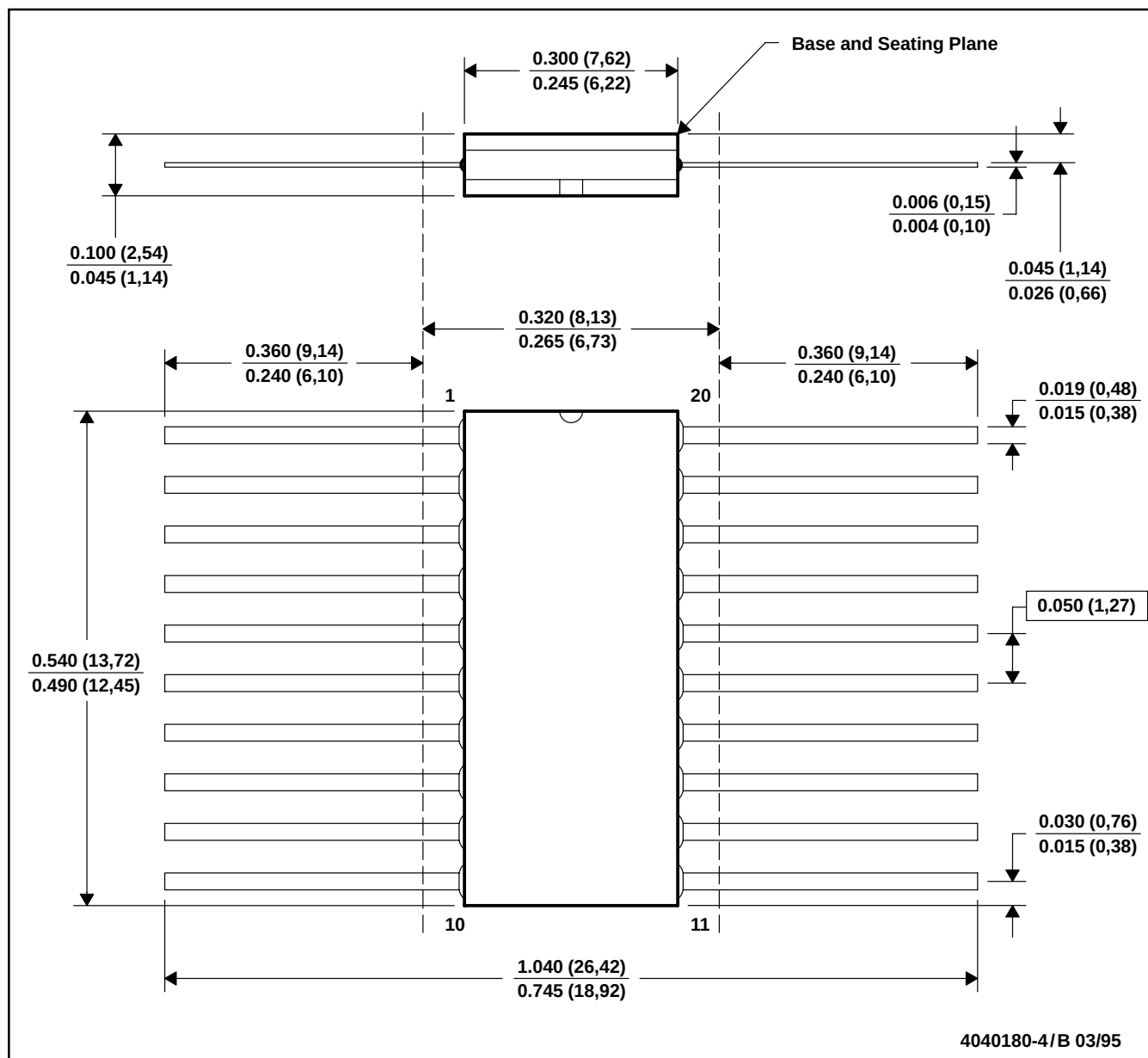
CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL-STD-1835 GDFFP1-F16 and JEDEC MO-092AC

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL-STD-1835 GDFP2-F20