LV8746V

Bi-CMOS LSI

PWM Current Control Stepping Motor Driver Application Note

ON Semiconductor®

http://onsemi.com

Overview

LV8746V is 2-channel H-bridge driver IC that can switch a stepping motor driver, which is capable of micro-step drive and supports Full-step, Half-step (full torque), Half-step, and Quarter-step resolution, which can select the CLK-IN input and the parallel input. This is best suited for driving of the stepping motor for OA and amusement.

Function

- PWM current control stepping motor driver
- BiCDMOS process IC
- On resistance (upper side: 0.84Ω, lower side: 0.7Ω, total of upper and lower: 1.54Ω; Ta=25˚C, I_O=1A)
- Micro step mode can be set to full-step, half-step (full torque), half-step, and quarter-step mode
- CLK-IN input and parallel input selectable
- Motor current selectable in four steps
- Output short-circuit protection circuit incorporated
- Unusual condition warning output pins
- Built-in thermal shutdown circuit
- No control power supply required

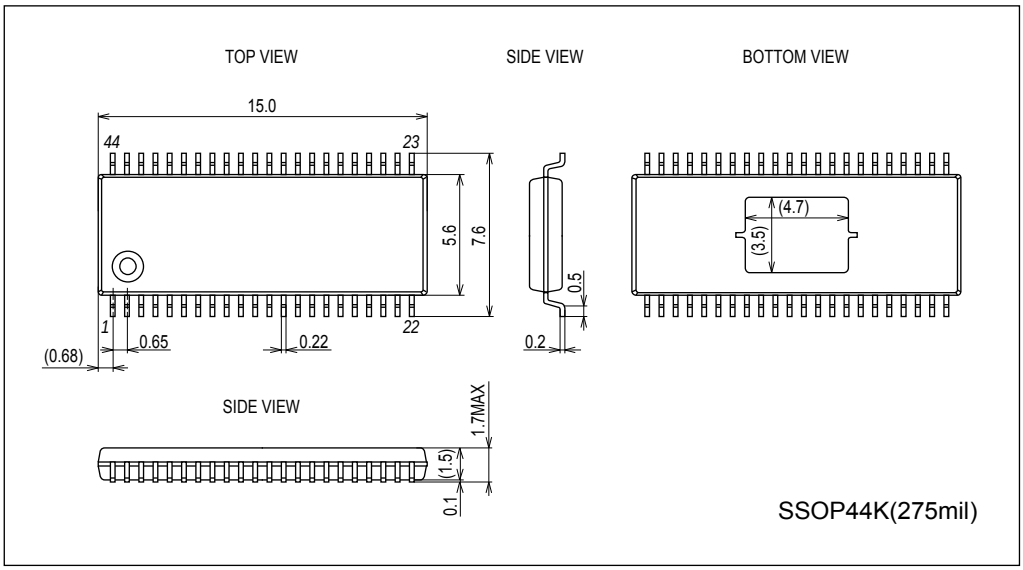
Typical Applications

- MFP (Multi Function Printer)
- PPC (Plain Paper Copier)
- LBP (Laser Beam Printer)
- Photo printer
- Scanner
- Industrial
- Cash Machine
- Amusement
- Textile

Semiconductor Components Industries, LLC, 2013

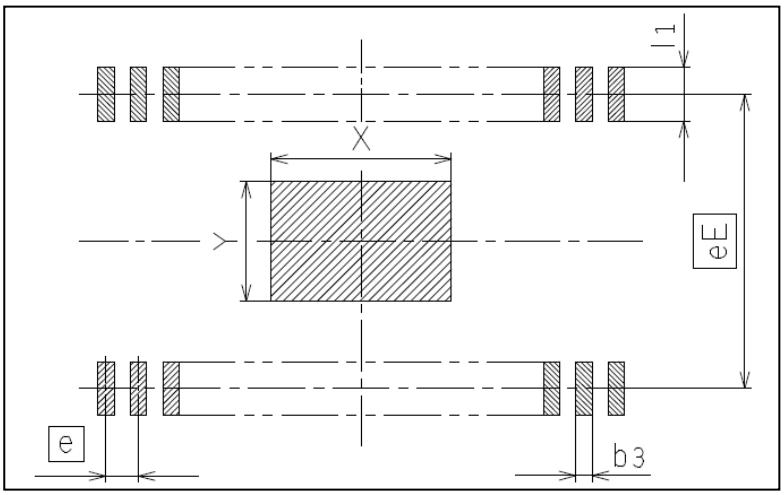
Package Dimensions

unit : mm (typ)



Caution: The package dimension is a reference value, which is not a guaranteed value.

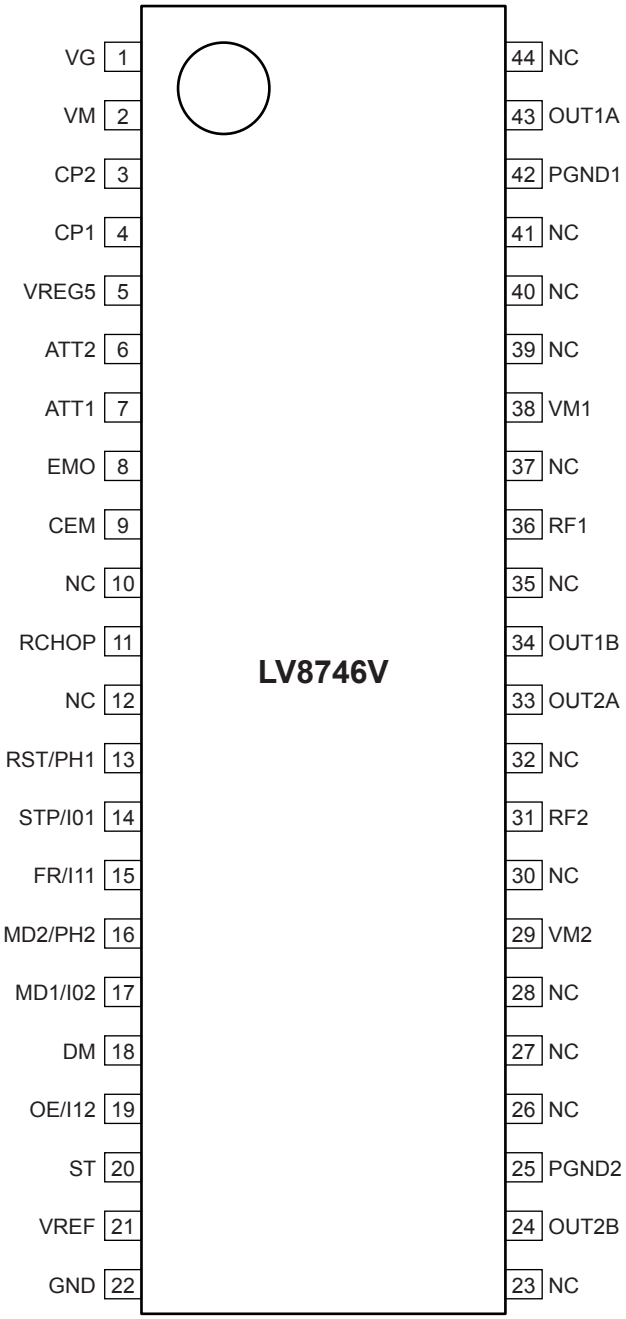
Recommended Soldering Footprint



(Unit:mm)

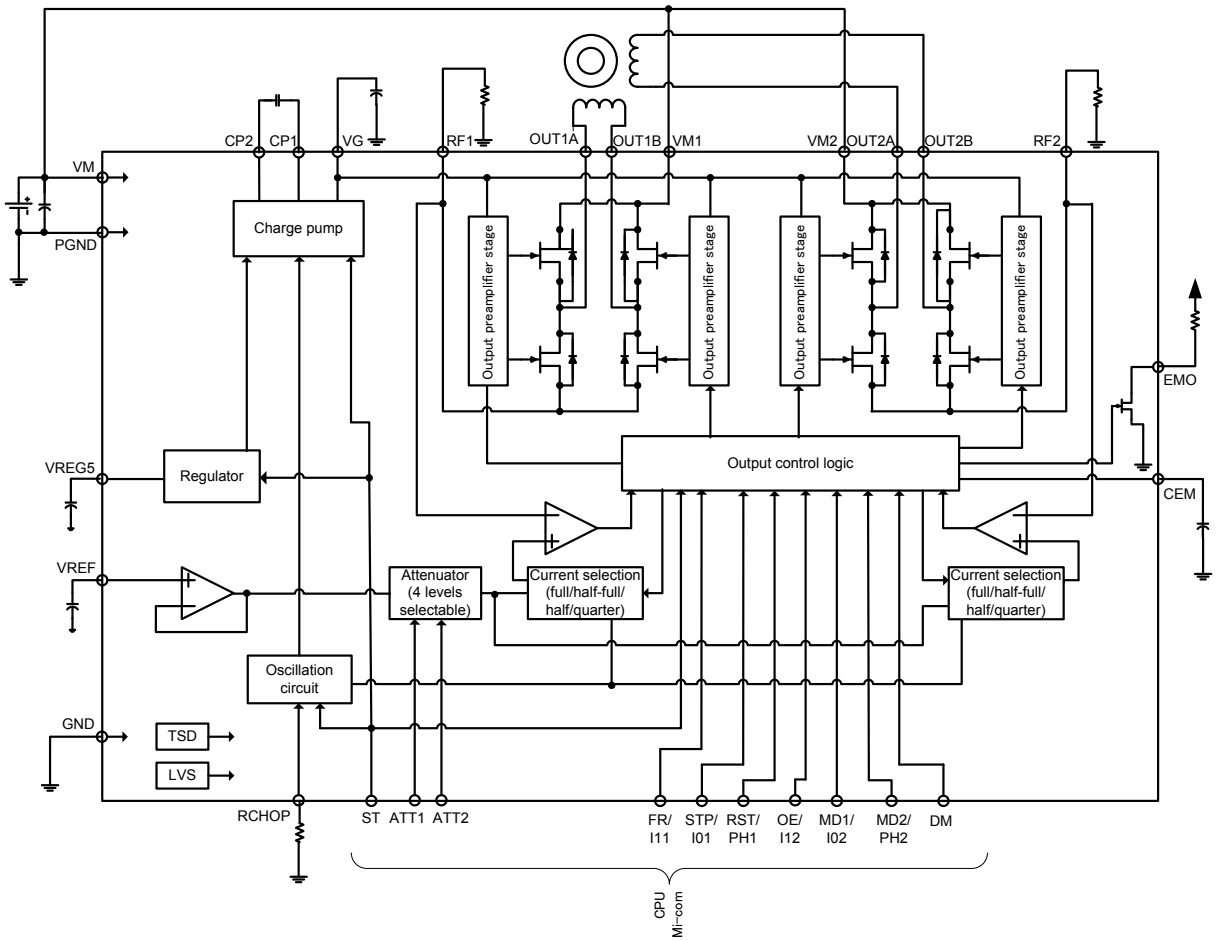
Reference symbol	SSOP44K(275mil)
eE	7.00
e	0.65
b3	0.32
l1	1.00
X	(4.7)
Y	(3.5)

Pin Assignment



Top view

Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VM max		38	V
Output peak current	I_O peak	tw ≤ 10ms, duty 20%	1.2	A
Output current	I_O max		1	A
Logic input voltage	V_{IN}		-0.3 to +6	V
EMO input voltage	Vemo		-0.3 to +6	V
Allowable power dissipation	Pd max	Ta ≤ 85°C *	3.1	W
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage range	VM		9		35	V
Logic input voltage	V_{IN}		0		5.5	V
VREF input voltage range	VREF		0		3	V

Electrical Characteristics at Ta = 25°C, VM = 24V, VREF = 1.5V

Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Standby mode current drain		IMst	ST = "L"		190	300	μA
Current drain		IM	ST = "H", OE = "L", with no load		3.3	5	mA
VREG5 output voltage		Vreg5	I_O = -1mA	4.5	5	5.5	V
Thermal shutdown temperature		TSD	Design guarantee	150	180	210	°C
Thermal hysteresis width		ΔTSD	Design guarantee		40		°C
Motor driver							
Output on resistance		Ronu	I_O = 1A, Upper-side on resistance		0.84	1.1	Ω
		Rond	I_O = 1A, Lower-side on resistance		0.7	0.9	Ω
Output leakage current		$I_O$leak				50	μA
Diode forward voltage		VD	ID = -1A		1.0	1.3	V
Logic pin input current(ST)		I_{IN}L	V_{IN} = 0.8V	3	8	15	μA
		I_{IN}H	V_{IN} = 5V	50	78	110	μA
Logic pin input current(other ST)		I_{IN}L	V_{IN} = 0.8V	3	8	15	μA
		I_{IN}H	V_{IN} = 5V	30	50	70	μA
Logic high-level input voltage		V_{IN}H		2.0			V
Logic low-level input voltage		V_{IN}L				0.8	V
Current setting comparator threshold voltage (CLK-IN input)	Quarter-step drive	Vtdac0_W	Step 0 (When initialized : channel 1 comparator level)	0.29	0.3	0.31	V
		Vtdac1_W	Step 1 (Initial state+1)	0.29	0.3	0.31	V
		Vtdac2_W	Step 2 (Initial state+2)	0.185	0.2	0.215	V
		Vtdac3_W	Step 3 (Initial state+3)	0.09	0.1	0.11	V
	Half-step drive	Vtdac0_M	Step 0 (When initialized : channel 1 comparator level)	0.29	0.3	0.31	V
		Vtdac2_M	Step 2 (Initial state+1)	0.185	0.2	0.215	V
	Half-step (full torque) drive	Vtdac0_H	Step 0 (When initialized : channel 1 comparator level)	0.29	0.3	0.31	V
		Vtdac2_H	Step 2 (Initial state+1)	0.29	0.3	0.31	V
	Full-step drive	Vtdac2_F	Step 2	0.29	0.3	0.31	V

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current setting comparator threshold voltage (parallel input)	Vtdac11	I01 = H , I11 = H	0.29	0.3	0.31	V
	Vtdac01	I01 = L , I11 = H	0.185	0.2	0.215	V
	Vtdac10	I01 = H , I11 = L	0.09	0.1	0.11	V
Current setting comparator threshold voltage (current attenuation rate switching)	Vtatt00	ATT1 = L, ATT2 = L	0.29	0.3	0.31	V
	Vtatt01	ATT1 = H, ATT2 = L	0.185	0.2	0.215	V
	Vtatt10	ATT1 = L, ATT2 = H	0.135	0.15	0.165	V
	Vtatt11	ATT1 = H, ATT2 = H	0.09	0.1	0.11	V
Chopping frequency	Fchop	Rchop = 20KΩ	45	62.5	75	kHz
VREF pin input current	Iref	VREF = 1.5V	-0.5			μA
Charge pump						
VG output voltage	VG		28	28.75	30	V
Rise time	tONG	VG = 0.1μF			0.5	mS
Oscillator frequency	Fosc	Rchop = 20KΩ	90	125	150	kHz
Output short-circuit protection						
EMO pin saturation voltage	Vsatemo	Iemo = 1mA		80	160	mV
CEM pin charge current	Icem	Vcem = 0V	7	10	13	μA
CEM pin threshold voltage	Vthcem		0.8	1.0	1.2	V

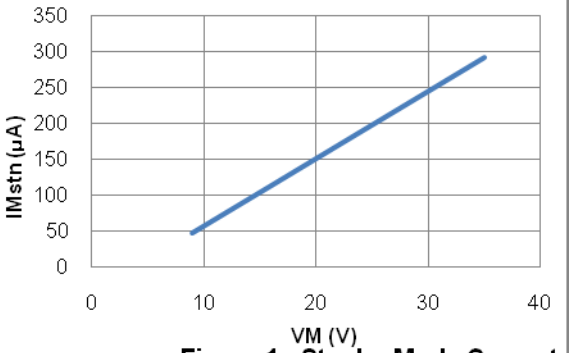


Figure 1. Stanby Mode Current Drain vs. VM Voltage

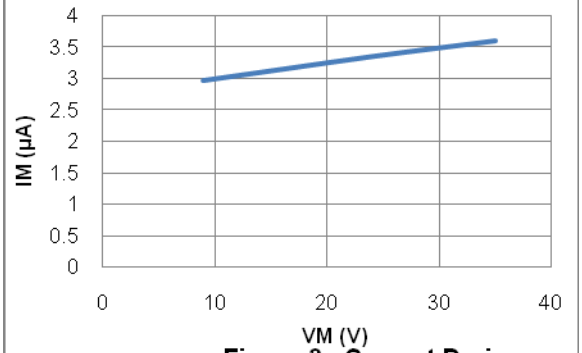


Figure 2. Current Drain vs. VM Voltage

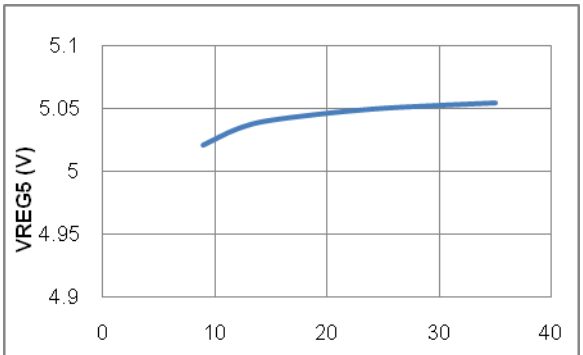


Figure 3. VREG5 Output Voltage vs. VM Voltage

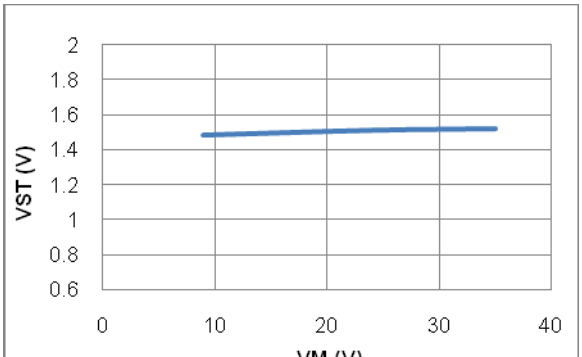


Figure 4. ST pin Threshold Voltage vs. VM Voltage

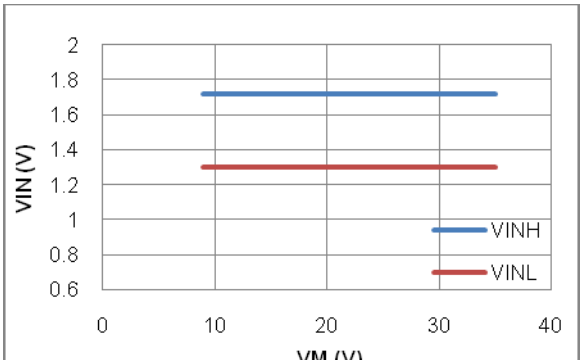


Figure 5. Logic High/Low-level input Voltage vs. VM Voltage

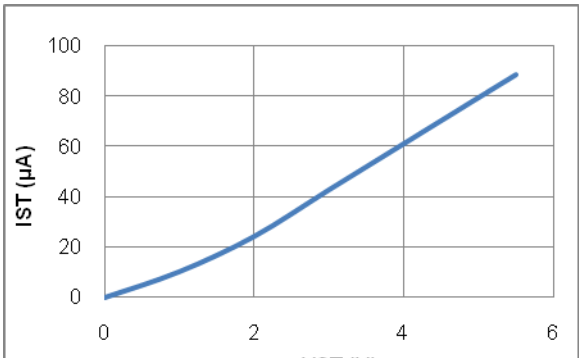


Figure 6. ST pin input Current vs. Logic input Voltage

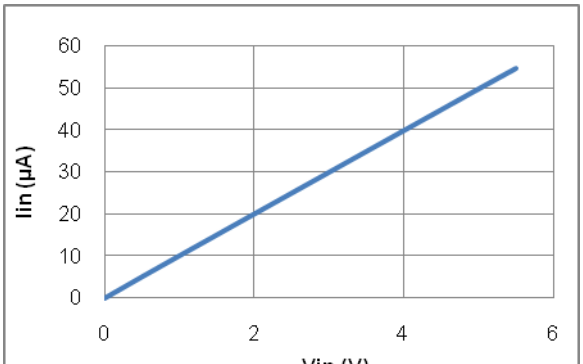


Figure 7. Logic pin input Current vs. Logic input Voltage

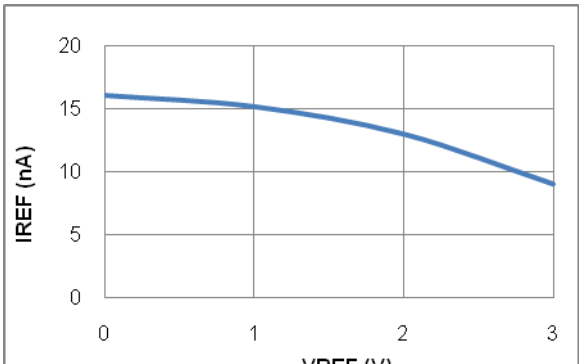


Figure 8. VREF pin input Current vs. VREF Voltage

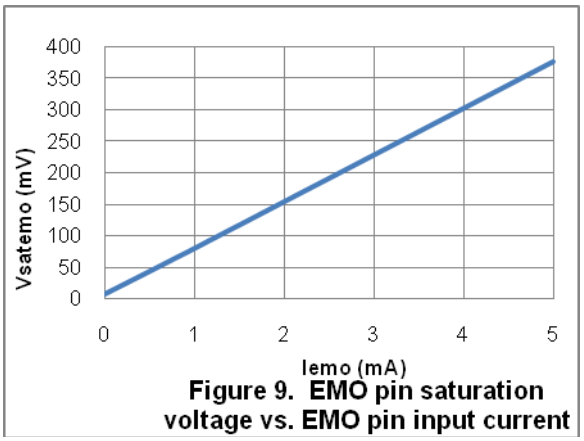


Figure 9. EMO pin saturation voltage vs. EMO pin input current

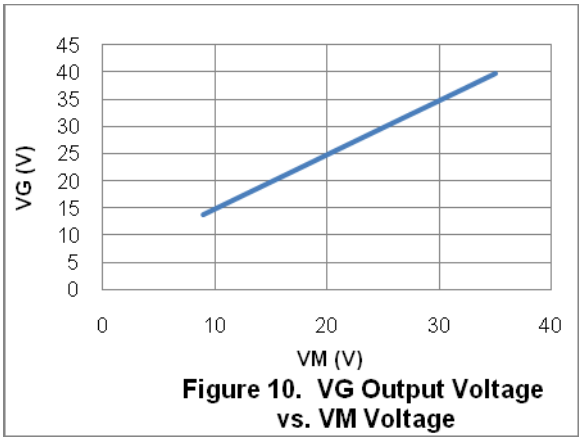


Figure 10. VG Output Voltage vs. VM Voltage

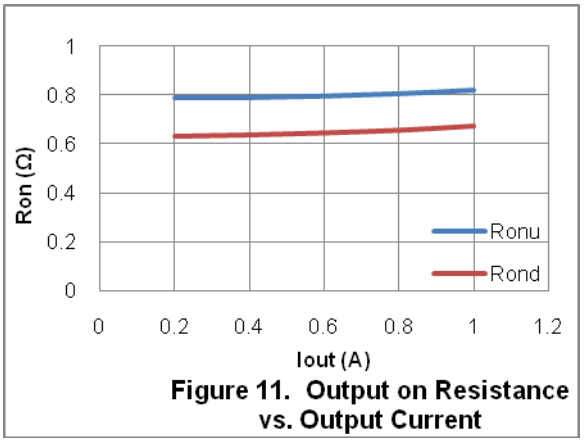


Figure 11. Output on Resistance vs. Output Current

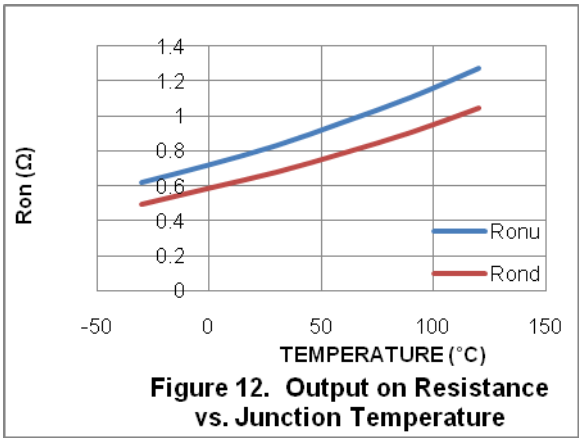


Figure 12. Output on Resistance vs. Junction Temperature

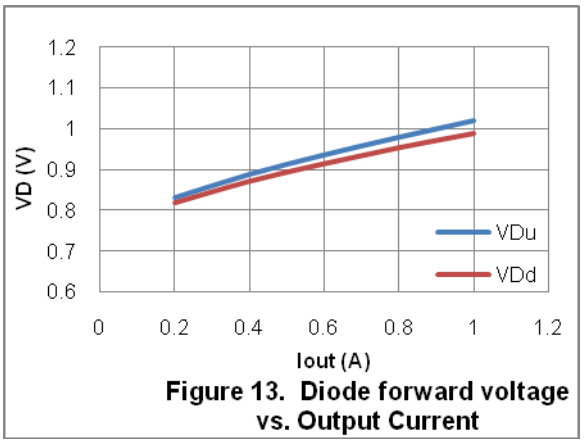
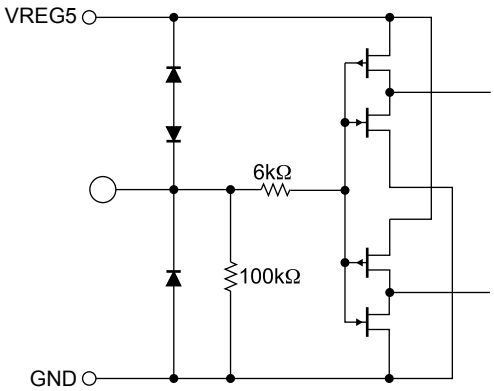
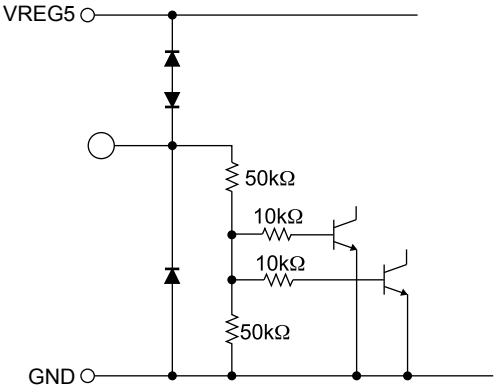
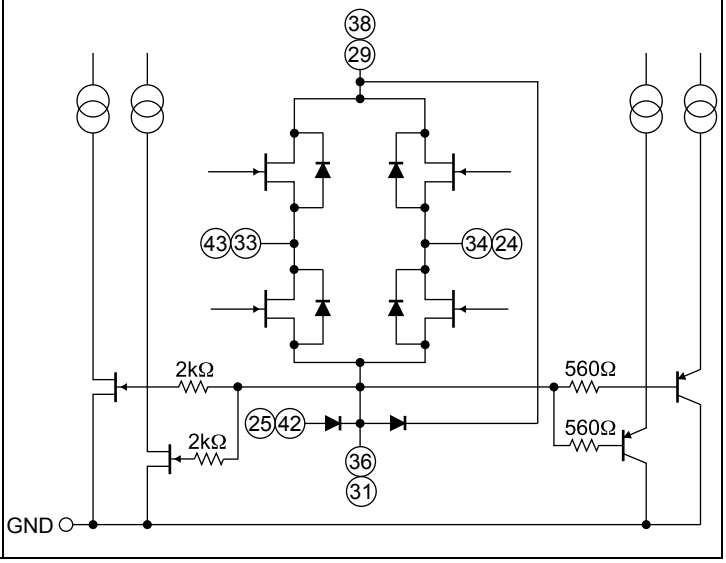


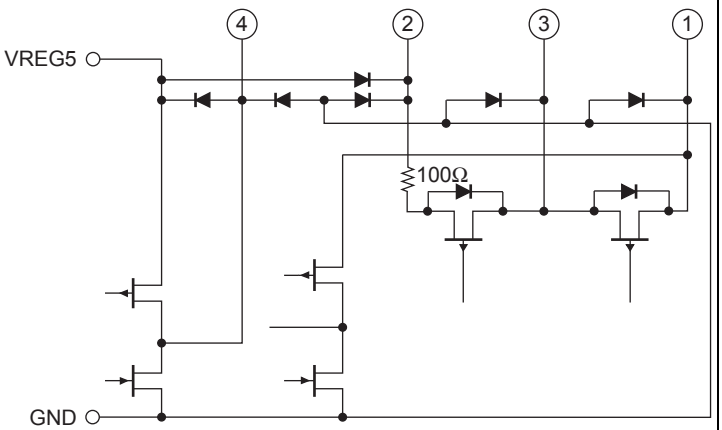
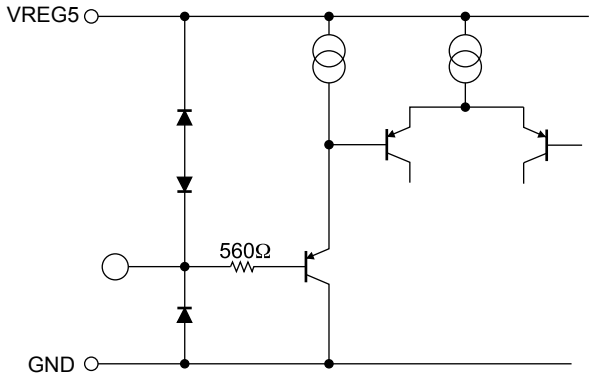
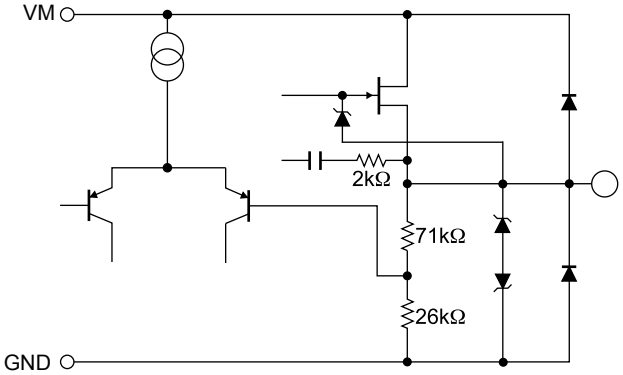
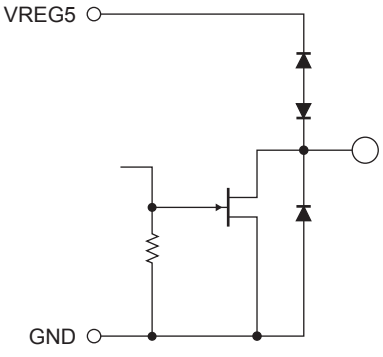
Figure 13. Diode forward voltage vs. Output Current

Pin Functions

Pin No.	Pin Name	Pin Function	Equivalent Circuit
6	ATT2	Motor holding current switching pin.	
7	ATT1	Motor holding current switching pin.	
13	RST/PH1	CLK-IN is input , RESET input pin / Parallel is input , Channel 1 forward/reverse rotation pin.	
14	STP/I01	CLK-IN is input , STEP signal input pin / Parallel is input , Channel 1 output control input pin.	
15	FR/I11	CLK-IN is input , forward/reverse signal input pin / Parallel is input , Channel 1 output control input pin.	
16	MD2/PH2	CLK-IN is input , Excitation mode switching pin / Parallel is input , Channel 2 forward/reverse rotation pin.	
17	MD1/I02	CLK-IN is input , Excitation mode switching pin / Parallel is input , Channel 2 output control input pin.	
18	DM	Drive mode switching pin.	
19	OE/I12	CLK-IN is input , output enable signal input pin / Parallel is input , Channel 2 output control input pin.	
20	ST	Chip enable pin.	
24	OUT2B	Channel 2 OUTB output pin.	
25	PGND2	Power system ground pin2.	
42	PGND1	Power system ground pin1.	
29	VM2	Channel 2 motor power supply connection pin.	
31	RF2	Channel 2 current-sense resistor connection pin.	
33	OUT2A	Channel 2 OUTA output pin.	
34	OUT1B	Channel 1 OUTB output pin.	
36	RF1	Channel 1 current-sense resistor connection pin.	
38	VM1	Channel 1 motor power supply pin.	
43	OUT1A	Channel 1 OUTA output pin.	

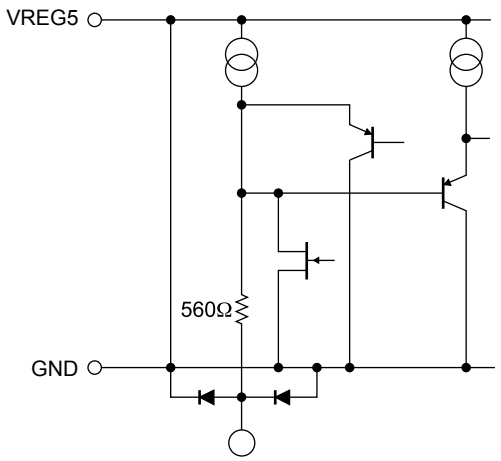
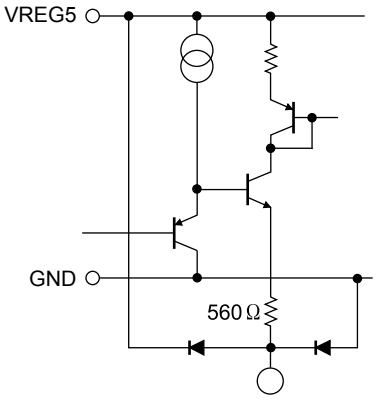
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Pin No.	Pin Name	Pin Function	Equivalent Circuit
1 2 3 4	VG VM CP2 CP1	Charge pump capacitor connection pin. Motor power supply connection pin. Charge pump capacitor connection pin. Charge pump capacitor connection pin.	
21	VREF	Constant current control reference voltage input pin.	
5	VREG5	Internal power supply capacitor connection pin.	
8	EMO	Output short-circuit state warning output pin.	

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Pin No.	Pin Name	Pin Function	Equivalent Circuit
9	CEM	Pin to connect the output short-circuit state detection time setting capacitor.	
11	RCHOP	Chopping frequency setting resistor connection pin.	
22	GND	Ground.	
10,12 23,26 27,28 30,32 35,37 39,40 41,44	NC	No Connection (No internal connection to the IC)	

Description of operation

Input Pin Function

The function to prevent including the turn from the input to the power supply is built into each input pin. Therefore, the current turns to the power supply even if power supply (VM) is turned off with the voltage impressed to the input pin and there is not crowding.

(1) Chip enable function

This IC is switched between standby and operating mode by setting the ST pin. In standby mode, the IC is set to power-save mode and all logic is reset. In addition, the internal regulator circuit and charge pump circuit do not operate in standby mode.

ST	Mode	Internal regulator	Charge pump
Low or Open	Standby mode	Standby	Standby
High	Operating mode	Operating	Operating

(2) Input control method switching pin function

The IC input control method is switched by setting the DM pin. The CLK-IN input control and the parallel input control can be selected by setting the DM pin.

DM	Input control method
Low or Open	CLK-IN input control
High	Parallel input control

(3) Setting constant-current control reference current

This IC is designed to automatically exercise PWM constant-current chopping control for the motor current by setting the output current. Based on the voltage input to the VREF pin and the resistance connected between RF and GND, the output current that is subject to the constant-current control is set using the calculation formula below:

I_{OUT} = (VREF/5)/RF resistance

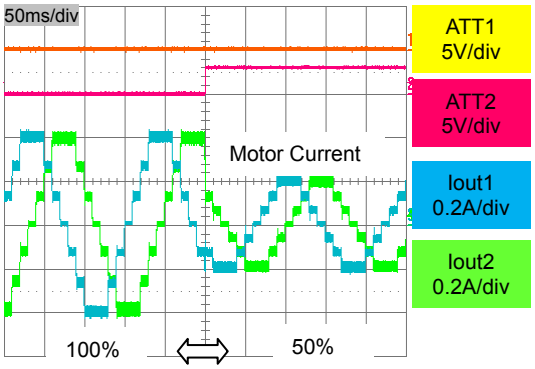
* The above setting is the output current at 100% of each excitation mode.

If VREF is open or the setting is out of the recommendation operating range, VREF is set around 5V. As a result, output current will increase and you cannot set constant current under normal condition. Hence, make sure that VREF is set in accordance with the specification.
However, if current control is not performed (if the IC is used without saturation drive or current limit) make sure that the setting is as follows: VREF=5V or VREF=VREG5

The voltage input to the VREF pin can be switched to four-step settings depending on the statuses of the two inputs, ATT1 and ATT2. This is effective for reducing power consumption when motor holding current is supplied.

Attenuation function for VREF input voltage

ATT1	ATT2	Current setting reference voltage attenuation ratio
Low	Low	100%
High	Low	66.7%
Low	High	50%
High	High	33.3%



VM=24V
VREF=1V
RF=0.47Ω

The formula used to calculate the output current when using the function for attenuating the VREF input voltage is given below.

I_{OUT} = (VREF/5) × (attenuation ratio)/RF resistance

Example: At VREF of 1.41V, a reference voltage setting of 100% [(ATT1, ATT2) = (L, L)] and an RF resistance of 0.47Ω, the output current is set as shown below.

I_{OUT} = 1.41V/5 × 100%/0.47Ω = 0.6A

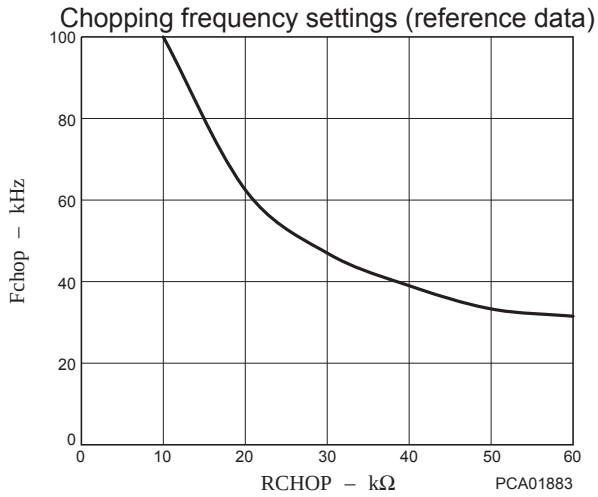
If, in this state, (ATT1, ATT2) is set to (H, H), IOUT will be as follows:

I_{OUT} = 0.6A × 33.3% = 0.2A

In this way, the output current is attenuated when the motor holding current is supplied so that power can be conserved.

(4) Setting the chopping frequency

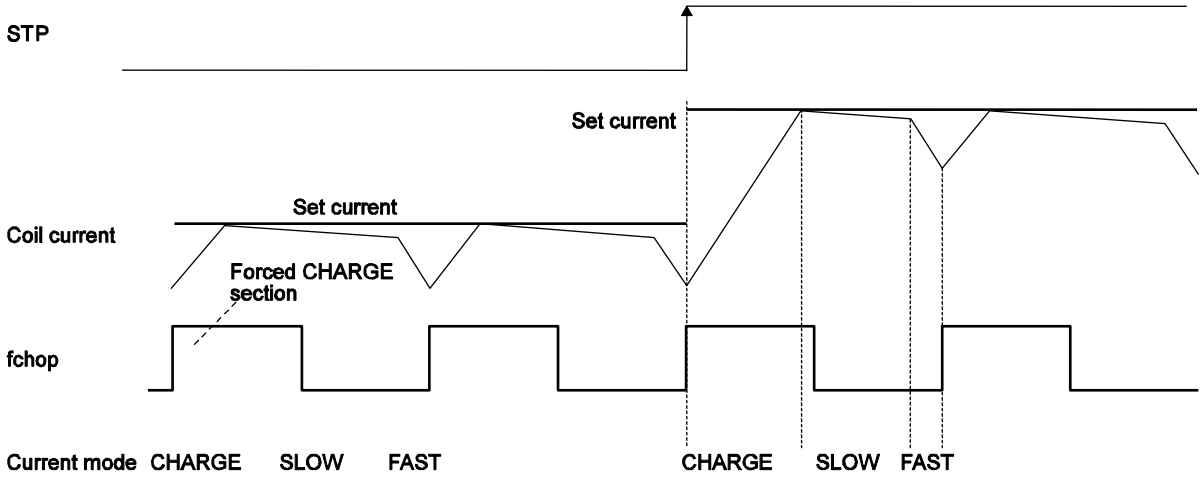
For constant-current control, chopping operation is made with the frequency determined by the external resistor (connected to the RCHOP pin).
The chopping frequency to be set with the resistance connected to the RCHOP pin (pin 11) is as shown below.



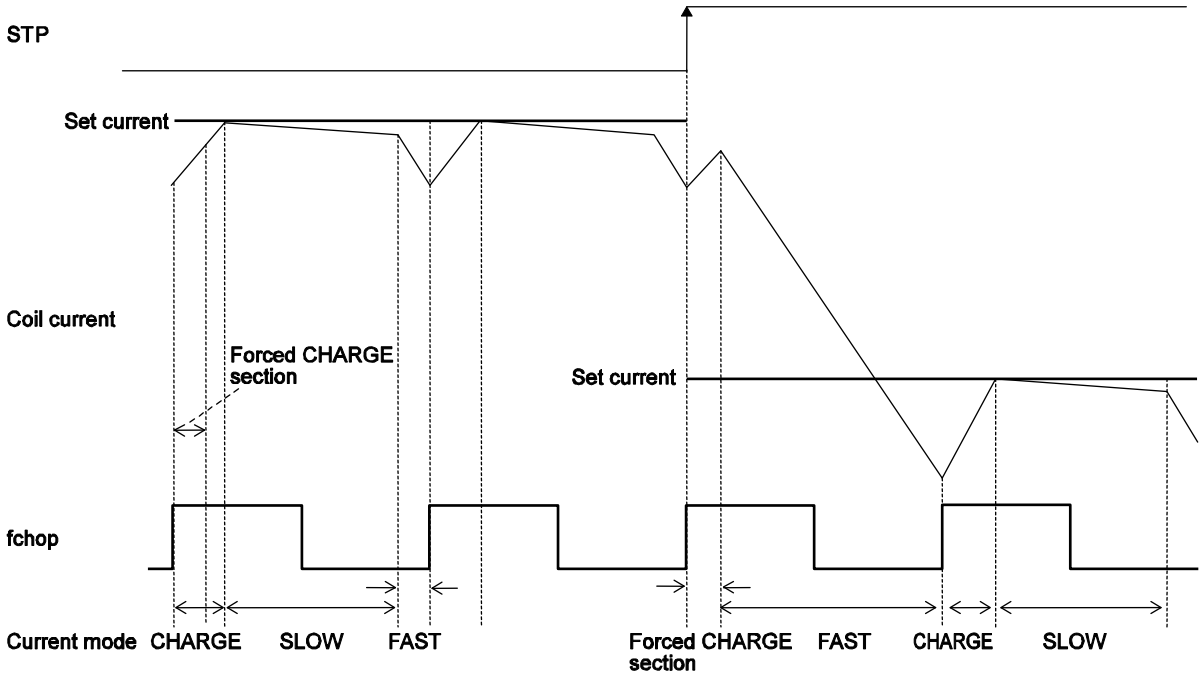
(5) Blanking period

If, when exercising PWM constant-current chopping control over the motor current, the mode is switched from decay to charge, the recovery current of the parasitic diode may flow to the current sensing resistance, causing noise to be carried on the current sensing resistance pin, and this may result in erroneous detection. To prevent this erroneous detection, a blanking period is provided to prevent the noise occurring during mode switching from being received. During this period, the mode is not switched from charge to decay even if noise is carried on the current sensing resistance pin.
In this IC, the blanking time is fixed at 1/16 of one chopping cycle.

(6) Current control operation specification
(Sine wave increasing direction)



(Sine wave decreasing direction)

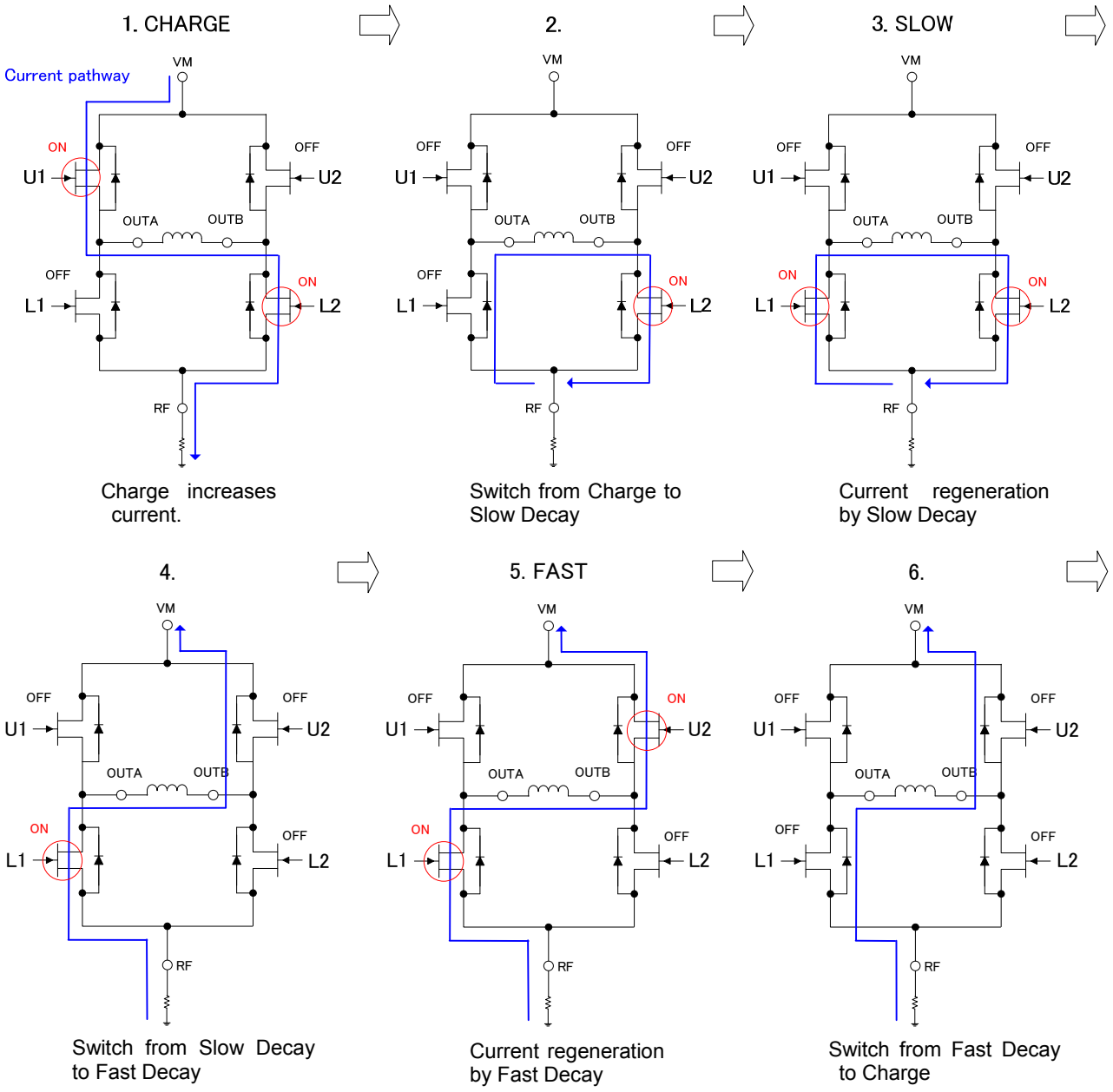


In each current mode, the operation sequence is as described below:

- At rise of chopping frequency, the CHARGE mode begins. (The section in which the CHARGE mode is forced regardless of the magnitude of the coil current (ICOIL) and set current (IREF) exists for 1/16 of one chopping cycle.)
- The coil current (ICOIL) and set current (IREF) are compared in this forced CHARGE section.
  When (ICOIL<IREF) state exists in the forced CHARGE section;
  CHARGE mode up to ICOIL ≥ IREF, then followed by changeover to the SLOW DECAY mode, and finally by the FAST DECAY mode for the 1/16 portion of one chopping cycle.
  When (ICOIL<IREF) state does not exist in the forced CHARGE section;
  The FAST DECAY mode begins. The coil current is attenuated in the FAST DECAY mode till one cycle of chopping is over.

Above operations are repeated. Normally, the SLOW (+FAST) DECAY mode continues in the sine wave increasing direction, then entering the FAST DECAY mode till the current is attenuated to the set level and followed by the SLOW DECAY mode.

(7) Output Transistor Operation Mode



This IC controls constant current by performing chopping to output transistor.
As shown above, by repeating the process from 1 to 6, setting current is maintained.
Chopping consists of 3 modes: Charge/ Slow decay/ Fast decay. In this IC, for switching mode (No.2, 4, 6), there are between the transistors. This off period is set to be constant (≈ 0.5μs) which is controlled by the internal logic. The diagrams show parasitic diode generated due to structure of MOS transistor. When the transistor is off, output current is regenerated through this parasitic diode.

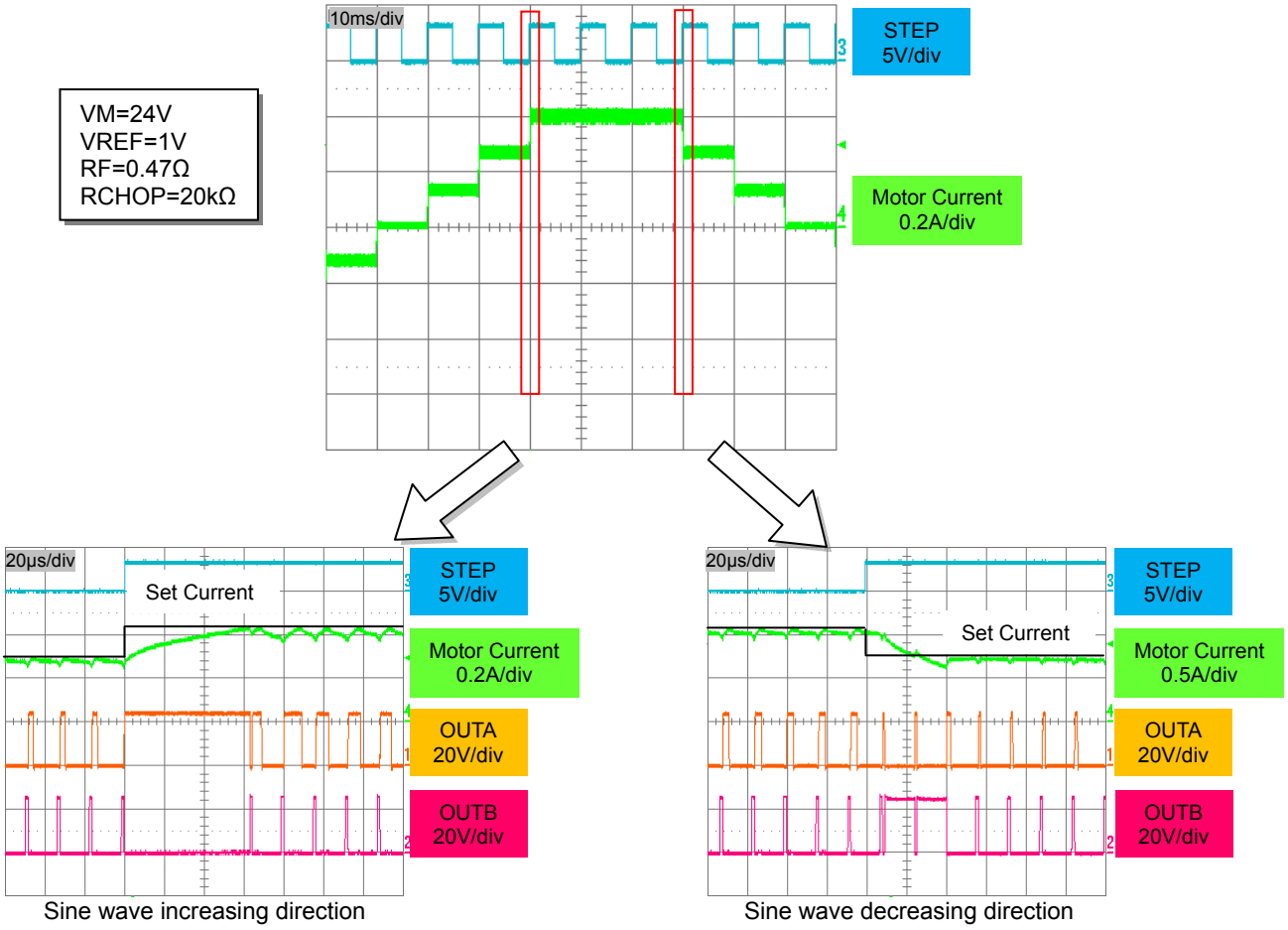
Output Transistor Operation Function

OUTA→OUTB (CHARGE)

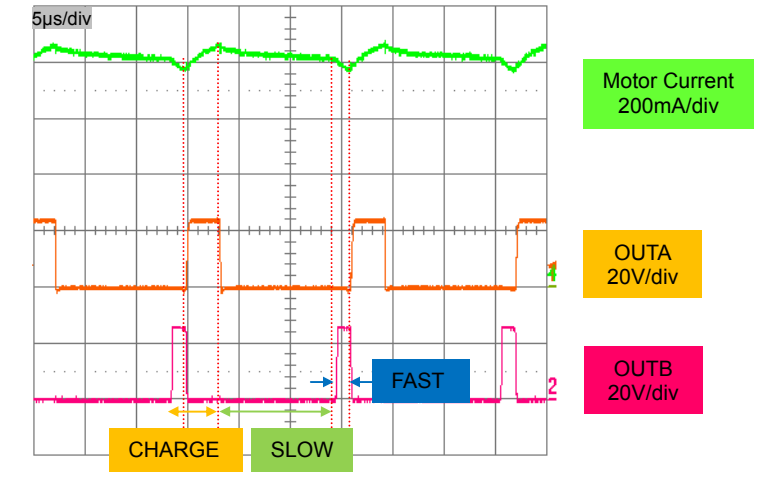
Output Tr	**CHARGE**	**SLOW**	**FAST**
U1	ON	OFF	OFF
U2	OFF	OFF	ON
L1	OFF	ON	ON
L2	ON	ON	OFF

OUTB→OUTA (CHARGE)

Output Tr	**CHARGE**	**SLOW**	**FAST**
U1	OFF	OFF	ON
U2	ON	OFF	OFF
L1	ON	ON	OFF
L2	OFF	ON	ON



Current mode



When the motor current reaches to the setting current, it is switched to Slow Decay mode.
Motor current switches from Slow Decay mode to Fast Decay mode for 1/16 of one chopping cycle.

CLK-IN input control (DM = Low or Open)

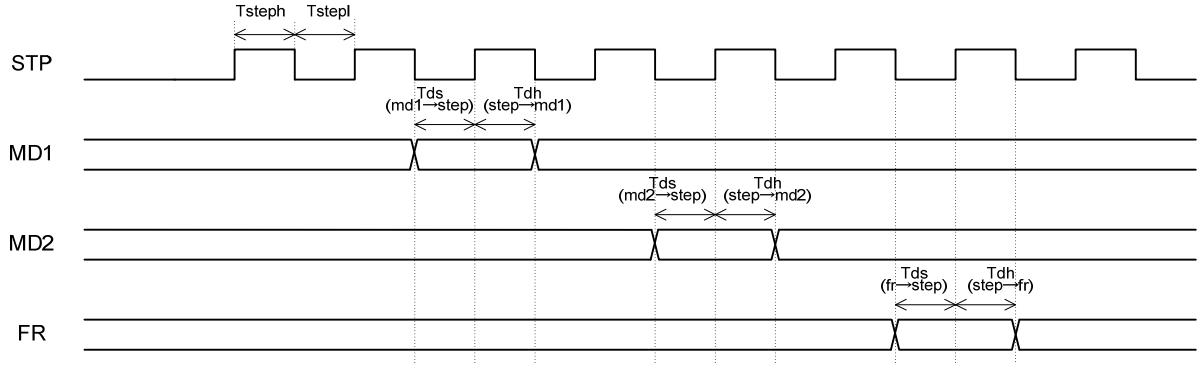
(1) STP pin function

The excitation step progresses by inputting the step signal to the STP pin.

Input		Operating mode
ST	STP	
Low	*	Standby mode
High		Excitation step proceeds
High		Excitation step is kept

STP input MIN pulse width (common in H/L): 500ns (MAX input frequency: 1MHz)
However, constant current control is performed by PWM during chopping period, which is set by the resistor connected between RCHOP and GND. You need to perform chopping more than once per step. For this reason, for the actual STP frequency, you need to take chopping frequency and chopping count into consideration.
For example, if chopping frequency is 62.5kHz (16μs) and chopping is performed twice per step, the maximum STP frequency is obtained as follows: f=1/(16μs×2) = 31kHz.

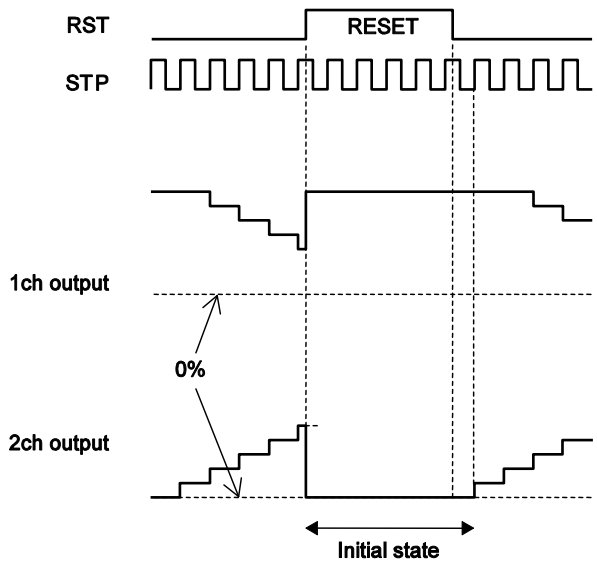
(2) Input timing



TstepH/TstepL : Clock H/L pulse width (min 500ns)
Tds : Data set-up time (min 500ns)
Tdh : Data hold time (min 500ns)

(3) Reset function

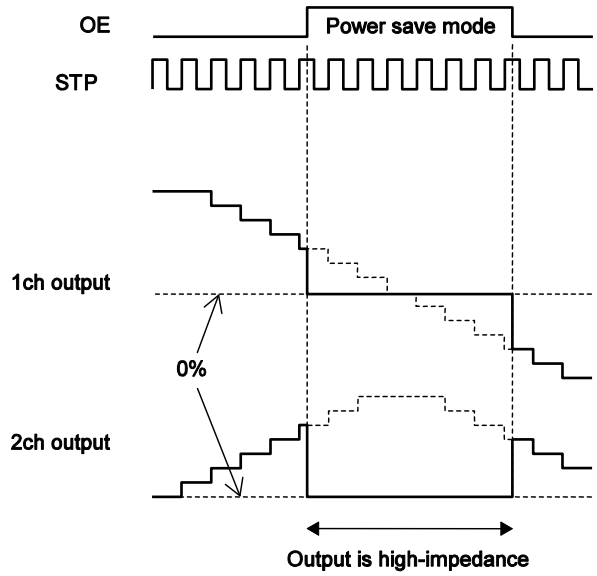
RST	Operating mode
Low	Normal operation
High	Reset state



When the RST pin is set to High, the excitation position of the output is forcibly set to the initial state. When RST is then set to Low, the excitation position is advanced by the next STP input.

(4) Output enable function

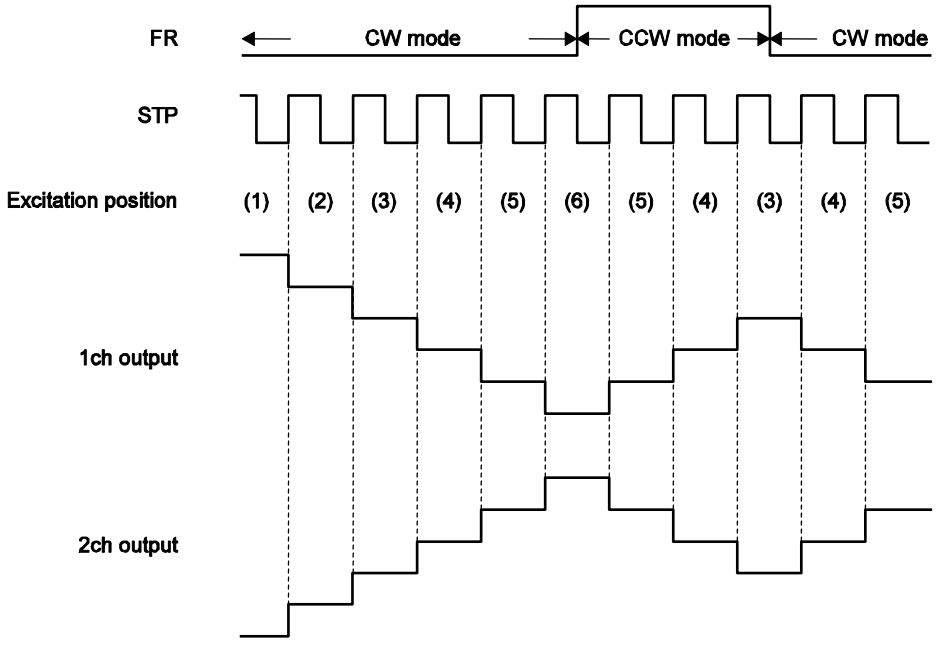
OE	Operating mode
High	Output OFF
Low	Output ON



When the OE pin is set High, the output is forced OFF and goes to high impedance.
However, the internal logic circuits are operating, so the excitation position proceeds when the STEP signal is input to the STP pin. Therefore, when OE is returned to Low, the output level conforms to the excitation position proceeded by the STEP input.

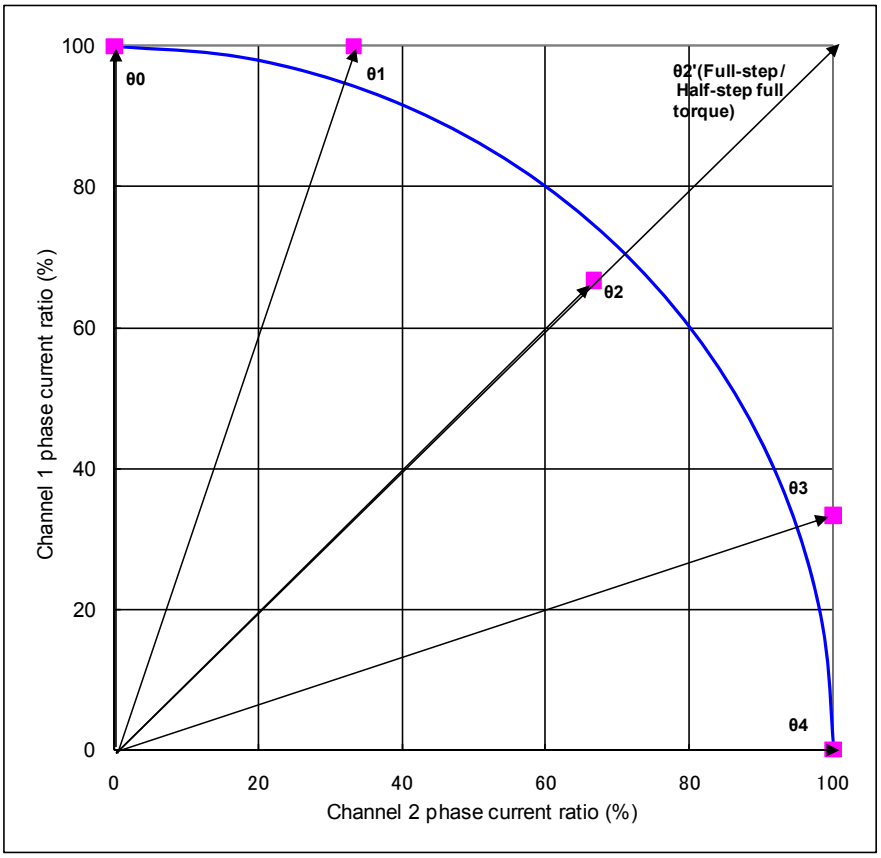
(5) Forward/reverse switching function

FR	Operating mode
Low	Clockwise (CW)
High	Counter-clockwise (CCW)



The internal D/A converter proceeds by one bit at the rising edge of the input STEP pulse.
In addition, CW and CCW mode are switched by setting the FR pin.
In CW mode, the channel 2 current phase is delayed by 90° relative to the channel 1 current.
In CCW mode, the channel 2 current phase is advanced by 90° relative to the channel 1 current.

(6) Output current vector locus (one step is normalized to 90 degrees)



Setting current ration in each excitation mode

STEP	Quarter Step (%)		Half Step (%)		Half Step (full torque) (%)		Full Step (%)	
	Channel 1	Channel 2	Channel 1	Channel 2	Channel 1	Channel 2	Channel 1	Channel 2
θ0	100	0	100	0	100	0		
θ1	100	33.3						
θ2	66.7	66.7	66.7	66.7	100	100	100	100
θ3	33.3	100						
θ4	0	100	0	100	0	100		

(7) Excitation mode setting function

The excitation mode of the stepping motor can be set as follows by setting the MD1 pin and the MD2 pin.

MD1	MD2	Microstep Resolution	Excitation mode	Initial position	
				Channel 1	Channel 2
Low	Low	Full Step	2 phase	100%	-100%
High	Low	Half Step (full torque)	1-2 phase (full torque)	100%	0%
Low	High	Half Step	1-2 phase	100%	0%
High	High	Quarter Step	W1-2 phase	100%	0%

This is the initial position of each excitation mode in the initial state after power-on and when the counter is reset.

(8) Excitation mode switching operation

When excitation mode is switched while the motor is rotating, each drive mode operates with the following sequence.

Clockwise mode

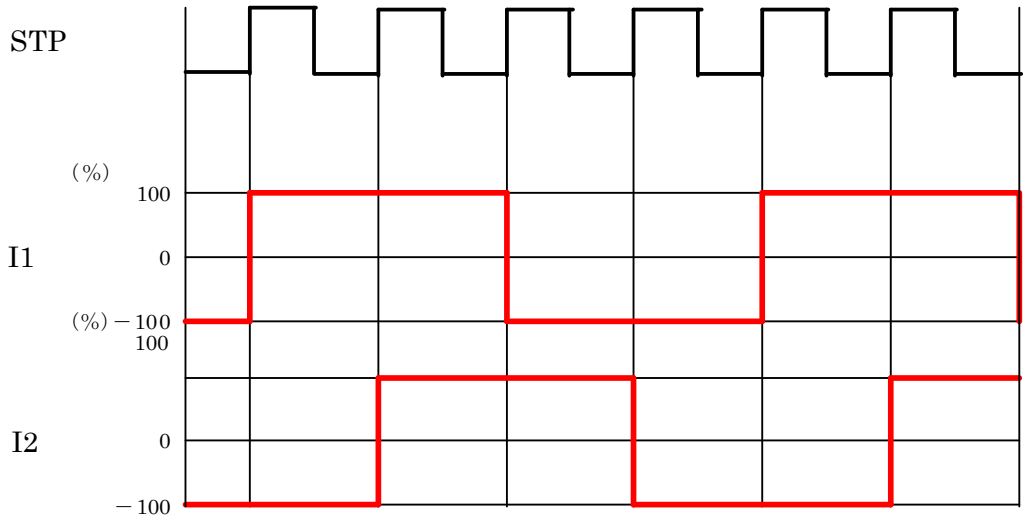
Before the Microstep Resolution changes		Position after the Microstep Resolution is changed			
Microstep Resolution	Position	Quarter Step	Half Step	Half Step (full torque)	Full Step
Quarter Step	θ0		θ2	θ2'	θ2'
	θ1		θ2	θ2'	θ2'
	θ2		θ4	θ4	θ2'
	θ3		θ2	θ2'	θ2'
	θ4		-θ2	-θ2'	-θ2'
Half Step	θ0	θ1		θ2'	θ2'
	θ2	θ3		θ2'	θ2'
	θ4	-θ3		-θ2'	-θ2'
Half Step (full torque)	θ0	θ1	θ2'		θ2'
	θ2'	θ3	θ4		θ2'
	θ4	-θ3	-θ2		-θ2'
Full Step	θ2'	θ3	θ4	θ4	

*As for θ0 to θ4, please refer to the step position of current ratio setting.

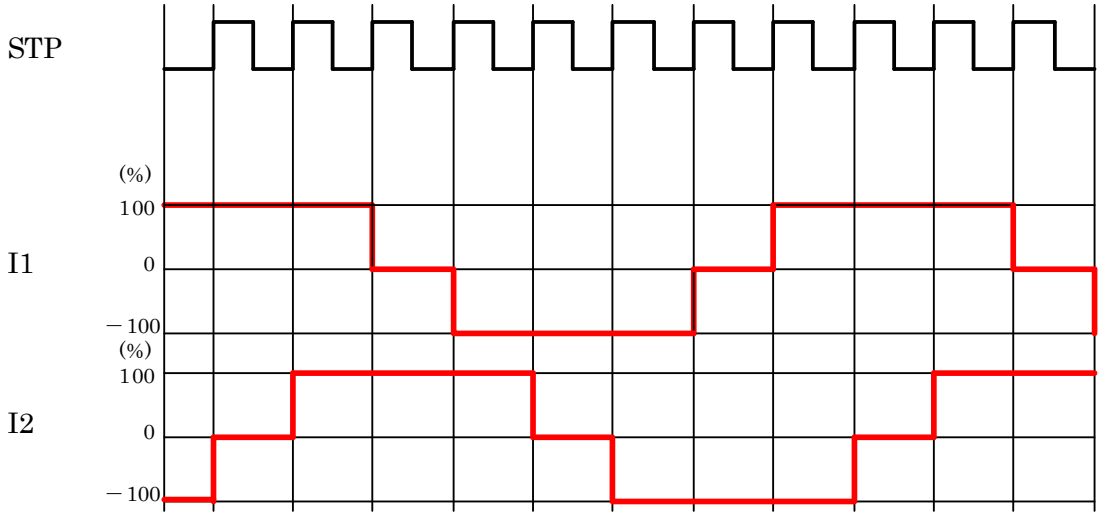
If you switch microstep mode while the motor is driving, the mode setting will be reflected from the next STEP and the motor advances to the closest excitation position at switching operation.

(9) Typical current waveform in each excitation mode

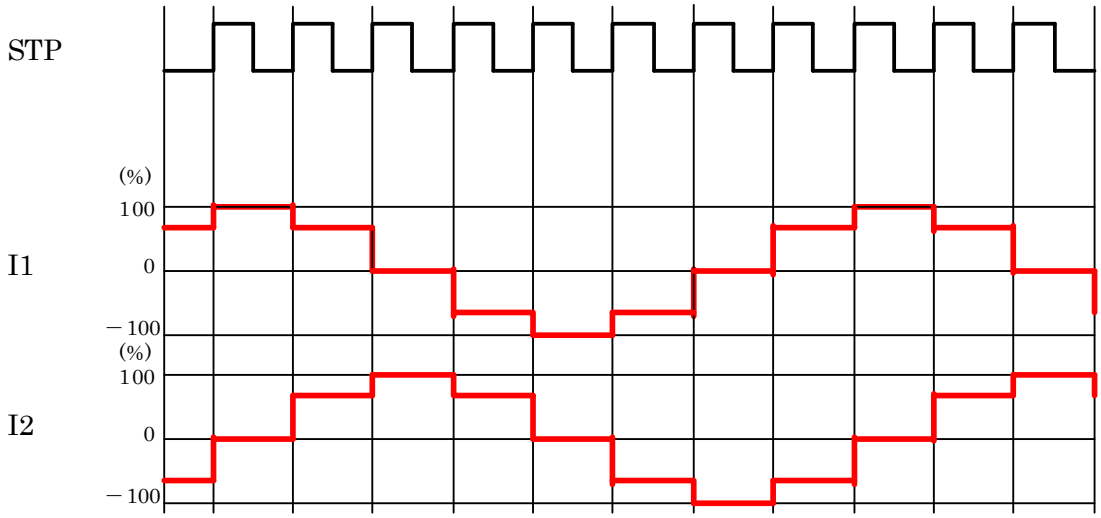
Full Step (CW mode)



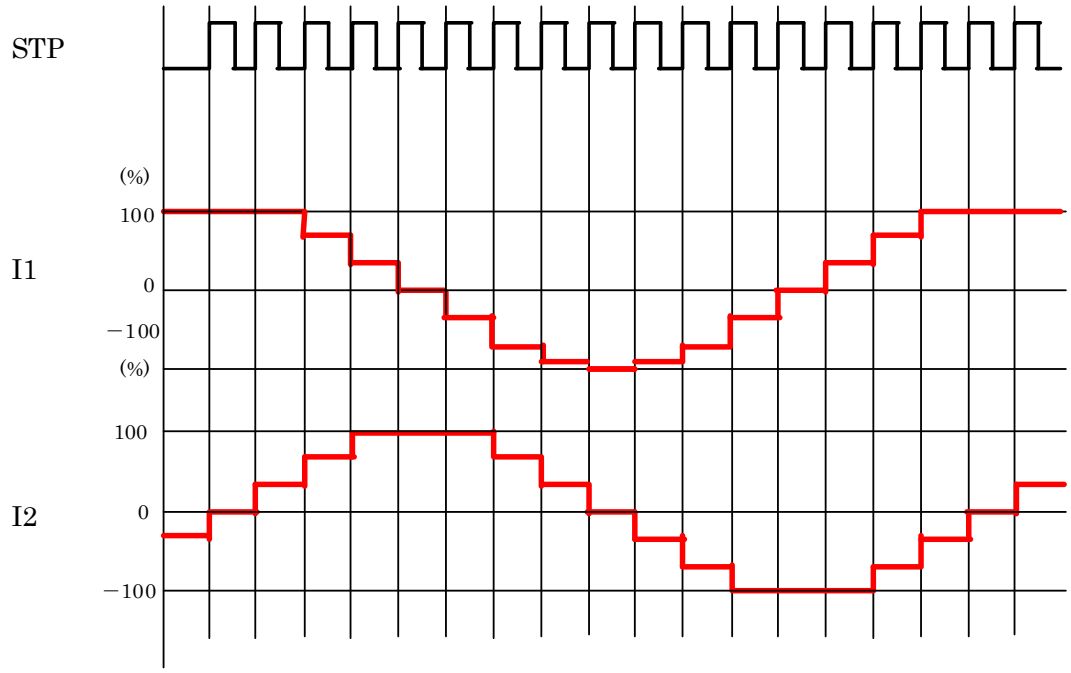
Half Step (full torque (CW mode))



Half steprg (CW mode)



Quarter Step (CW mode)



Parallel input Mode (DM-High)

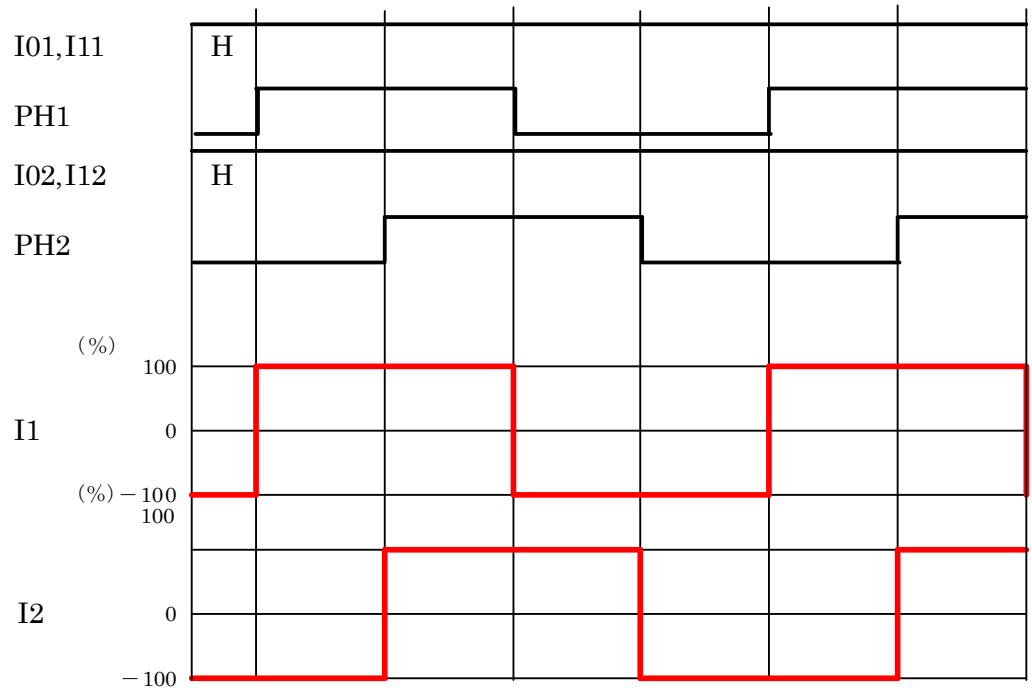
(1) Parallel input control logic

I01(02)	I11(12)	Output current (I_O)
Low	Low	0
High	Low	I_O = ((VREF/5)/RF)×1/3
Low	High	I_O = ((VREF/5)/RF)×2/3
High	High	I_O = (VREF/5)/RF

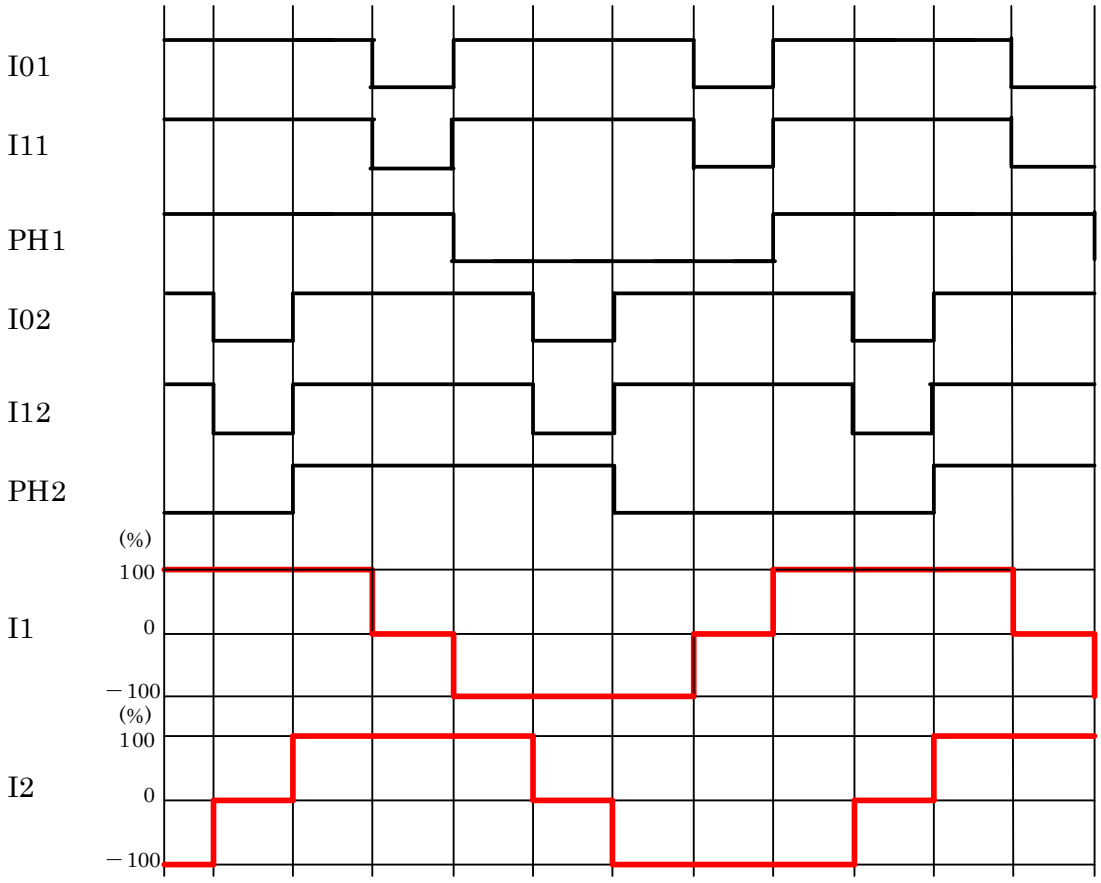
PH1(2)	current direction
Low	OUTB → OUTA
High	OUTA → OUTB

(2) Typical current waveform in each excitation mode when stepping motor parallel input control

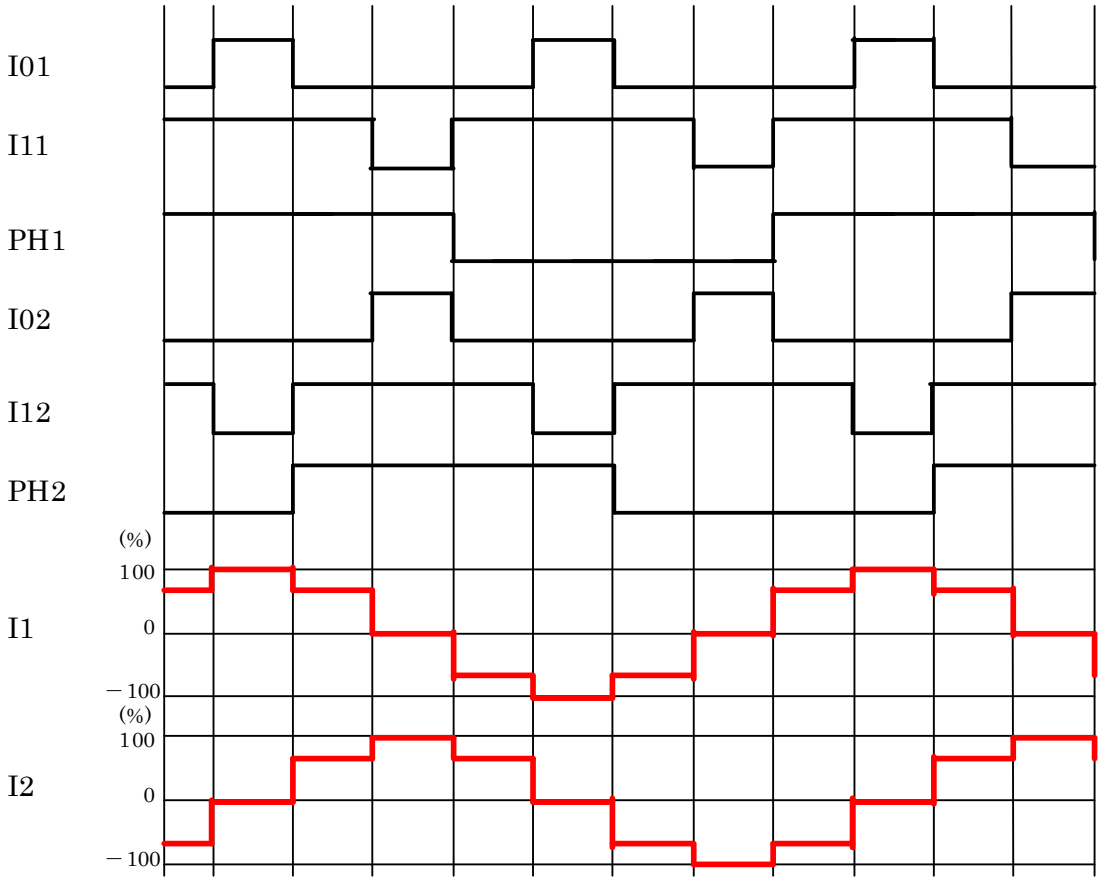
Full Step (CW mode)



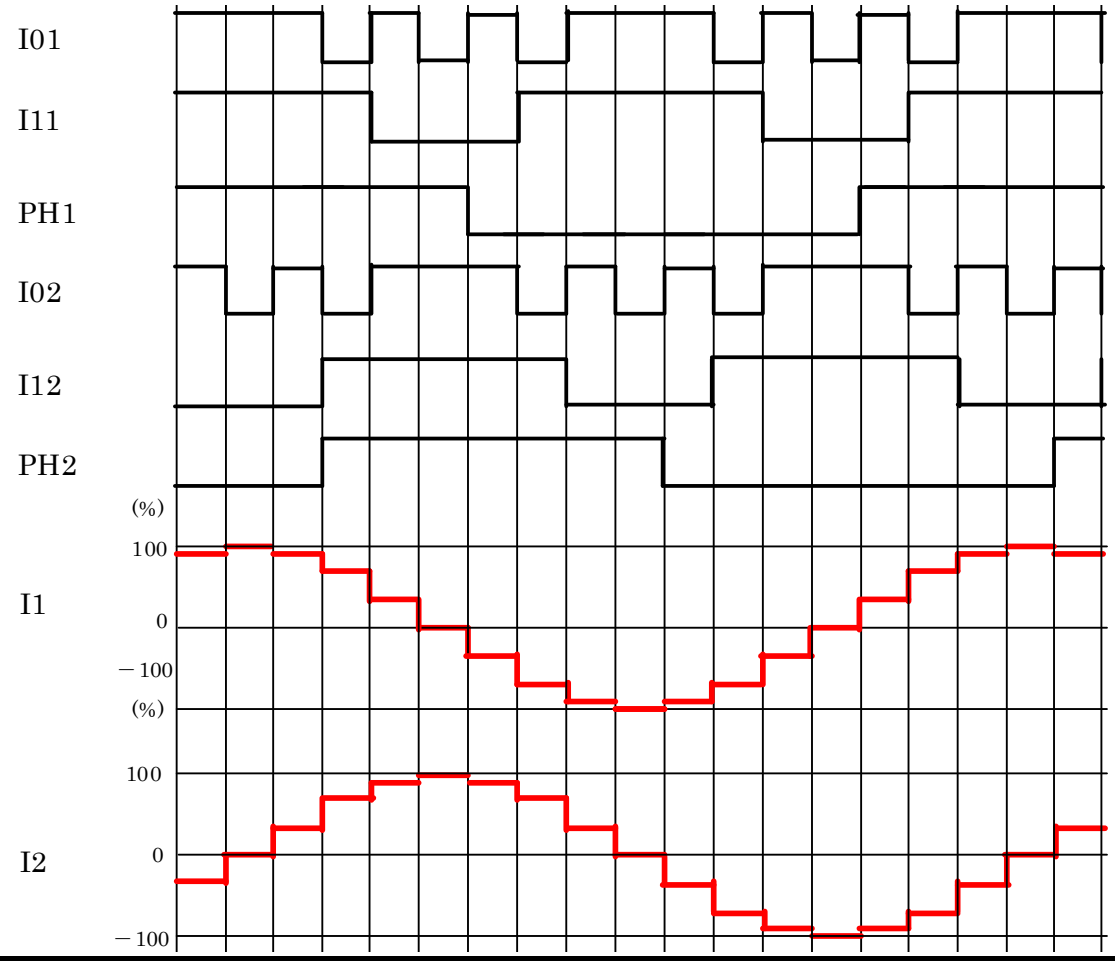
Half Step (full torque (CW mode))



Half Step (CW mode)

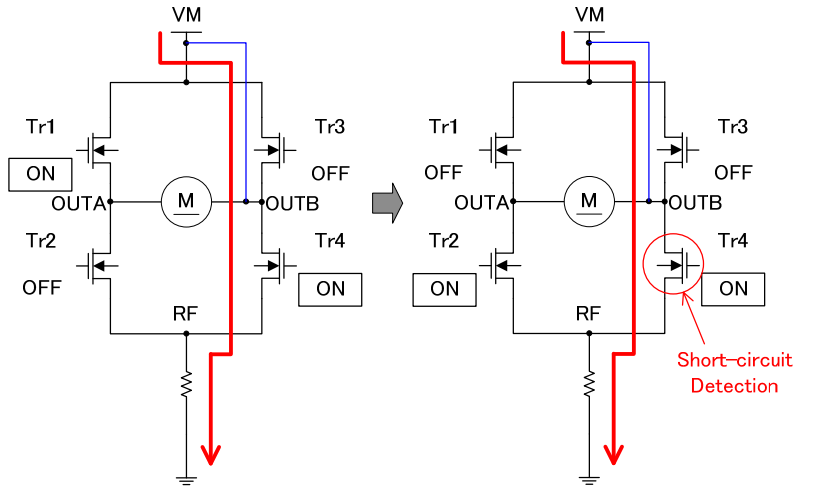
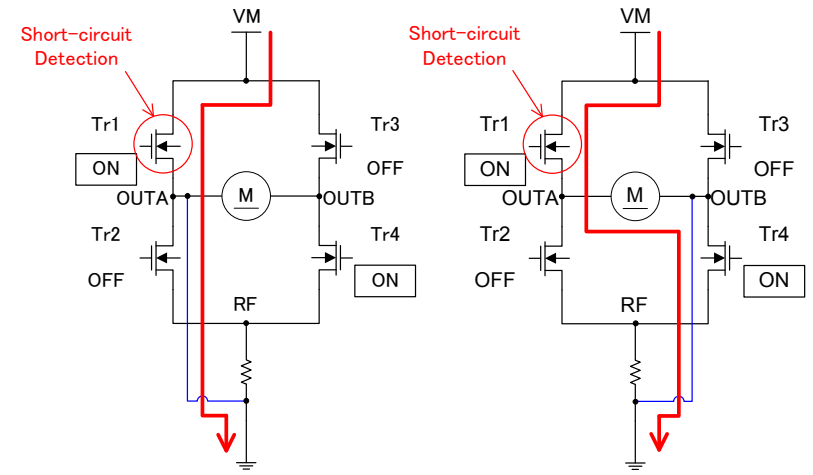
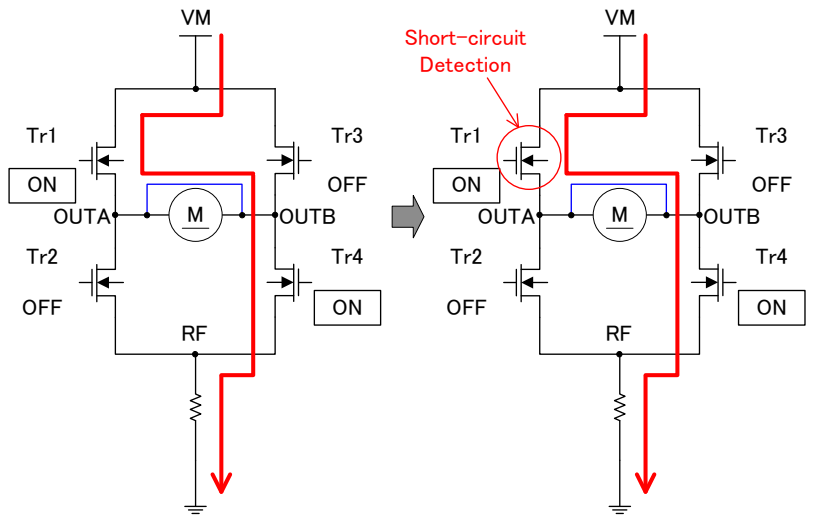


Quarter Step (CW mode)



Output short-circuit protection function

This output short protection circuit that makes the output a standby mode to prevent the thing that IC destroys when the output is short-circuited by a voltage short and the earth fault, etc. , and turns on the warning output to IC is built into.

VM short 	1.High current flows if Tr1 and Tr4 are ON. 2.If RF voltage> setting voltage, then the mode switches to SLOW decay. 3.If the voltage between D and S of Tr4 exceeds the reference voltage for 4μs, short status is detected.
VM short 	(left schematic) 1.High current flows if Tr1 and Tr4 are ON 2. If the voltage between D and S of Tr1 exceeds the reference voltage for 2μs, short status is detected. (right schematic) 1.Without going through RF resistor, current control does not operate and current will continue to increase in CHARGE mode. 2. If the voltage between D and S of Tr1 exceeds the reference voltage for 4μs, short status is detected.
Load short 	1.Without L load, high current flows. 2. If RF voltage> setting voltage, then the mode switches to SLOW decay. 3.During load short status in SLOW decay mode, current does not flow and overcurrent state is not detected. Then the mode is switched to FAST decay according to chopping cycle. 4. Since FAST state is short (≈1μs), switches to CHARGE mode before short is detected. 5.If voltage between D and S exceeds the reference voltage continuously during blanking time at the start of CHARGE mode (Tr1), CHARGE state is fixed (even if RF voltage exceeds the setting voltage, the mode is not switched to SLOW decay). After 4us or so, short is detected.

(6) Detect current

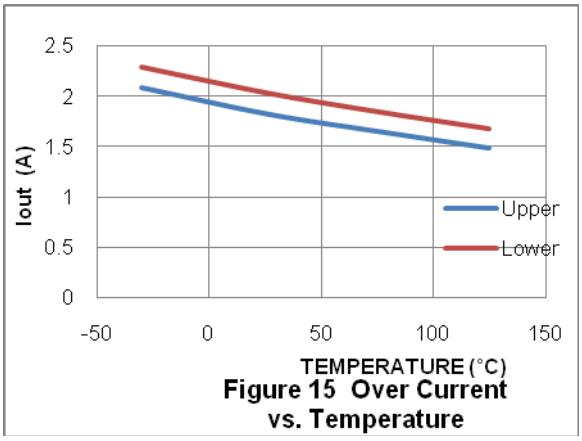
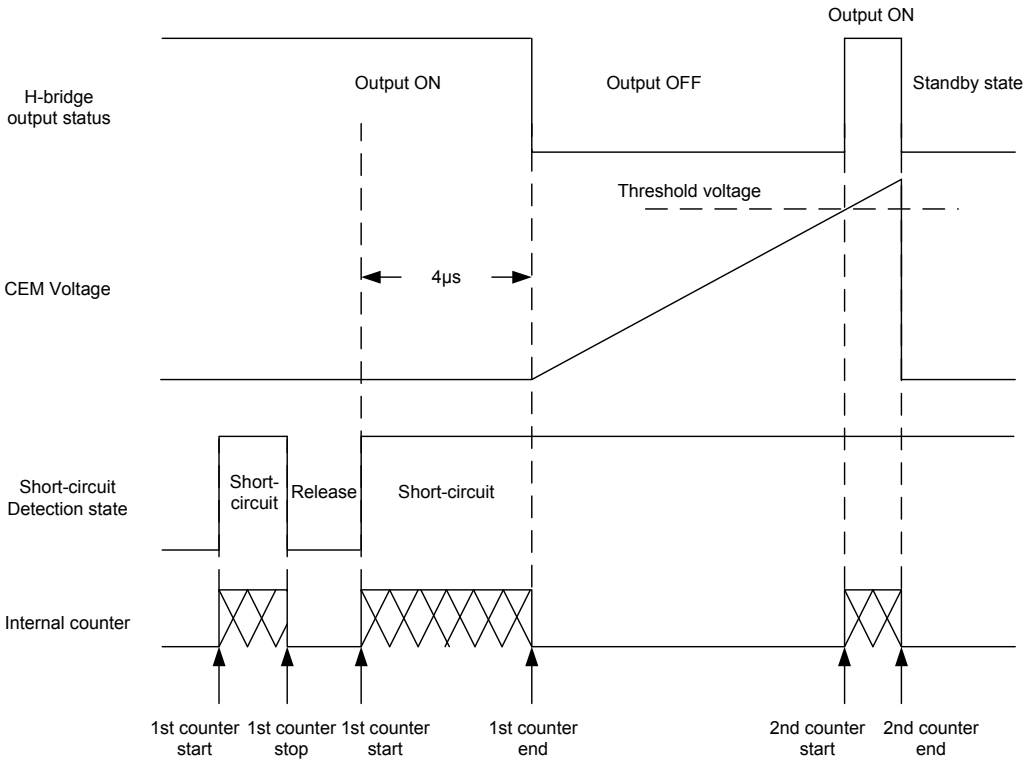


Figure 15 Over Current vs. Temperature

(1) Protection function operation (Latch type)

In the latch mode, the output is turned off when the output current exceeds the detection current, and the state is maintained.

The output short protection circuit starts operating so that IC may detect a short output. When short-circuit is the consecutive between internal timers (≈4μs), the output where short-circuit is first detected is turned off. Even if the following time (Tcem) of the timer latch is exceeded, the output is turned ON again, and afterwards, when short-circuit is detected, all the outputs of correspondence ch side are still switched to the standby mode, and the state is maintained. This state is released by making it to ST ="L".



(2) Abnormal state warning output pin

When IC operates the protection circuit detecting abnormality, the EMO pin has been installed as a terminal that outputs this abnormality to CPU side. This pin is an open drain output, and if abnormality is detected, the EMO output becomes (EMO="L") of ON.

EMO pin enters on a state in the following.

- When a voltage short, the earth fault or the load is short-circuited and the output short-circuit protection circuit operates, the output pin
- When the junction temperature of IC rises, and the overheating protection circuit operates

Unusual condition	EMO	Channel 1 Output	Channel 2 Output
Channel 1 short-circuit detected	ON	OFF	-
Channel 2 short-circuit detected	ON	-	OFF
Overheating condition detected	ON	OFF	OFF

(3) Timer latch time (Tcem)

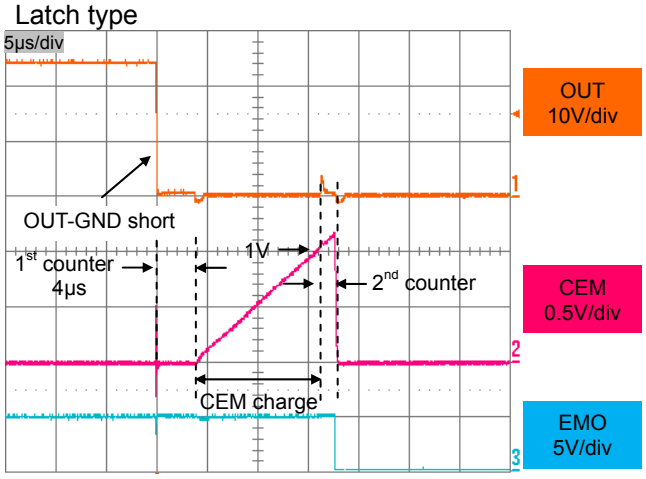
The time to output OFF when an output short-circuit occurs can be set by the capacitor connected between the CEM pin and GND. The capacitor (Ccem) value can be determined as follows :

Timer latch: Tcem $Tcem \approx C \times V/I$ [sec]

V : Threshold voltage of comparator TYP 1V

I : CEM charge current TYP 10μA

Latch type



Thermal shutdown function

The thermal shutdown circuit is incorporated and the output is turned off when junction temperature Tj exceeds 180°C and the abnormal state warning output is turned on. As the temperature falls by hysteresis, the output turned on again (automatic restoration).

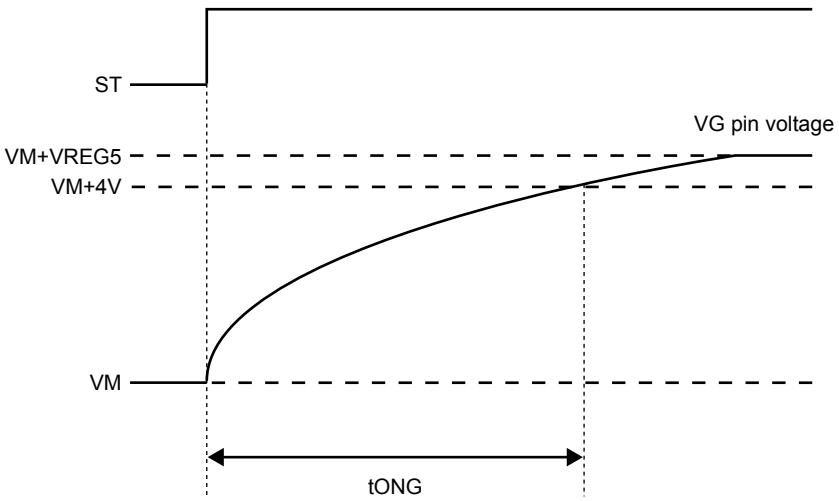
The thermal shutdown circuit does not guarantee the protection of the final product because it operates when the temperature exceed the junction temperature of Tjmax=150°C.

TSD = 180°C (typ)

ΔTSD = 40°C (typ)

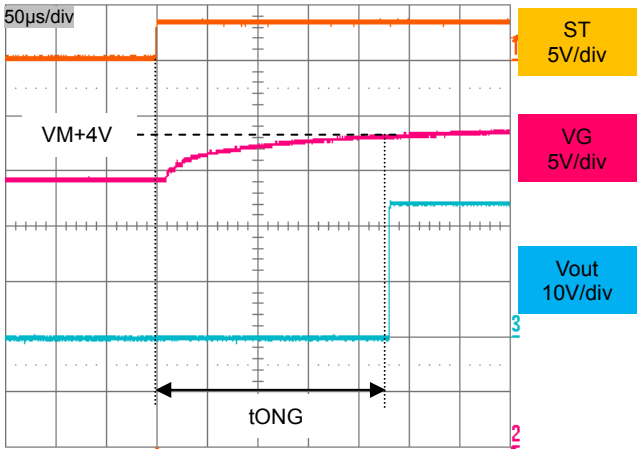
Charge Pump Circuit

When the ST pin is set High, the charge pump circuit operates and the VG pin voltage is boosted from the VM voltage to the VM + VREG5 voltage. I will recommend the drive of the motor to put the time of tONG or more after the ST pin is made "H", and to begin because I cannot control the output if there is no pressure voltage of the voltage of the VG pin enough.



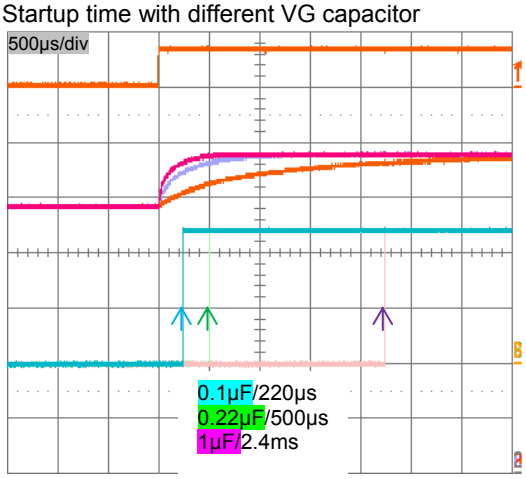
VG Pin Voltage Schematic View

tONG



VM=24V
CP1-CP2=0.1µF
VG=0.1µF

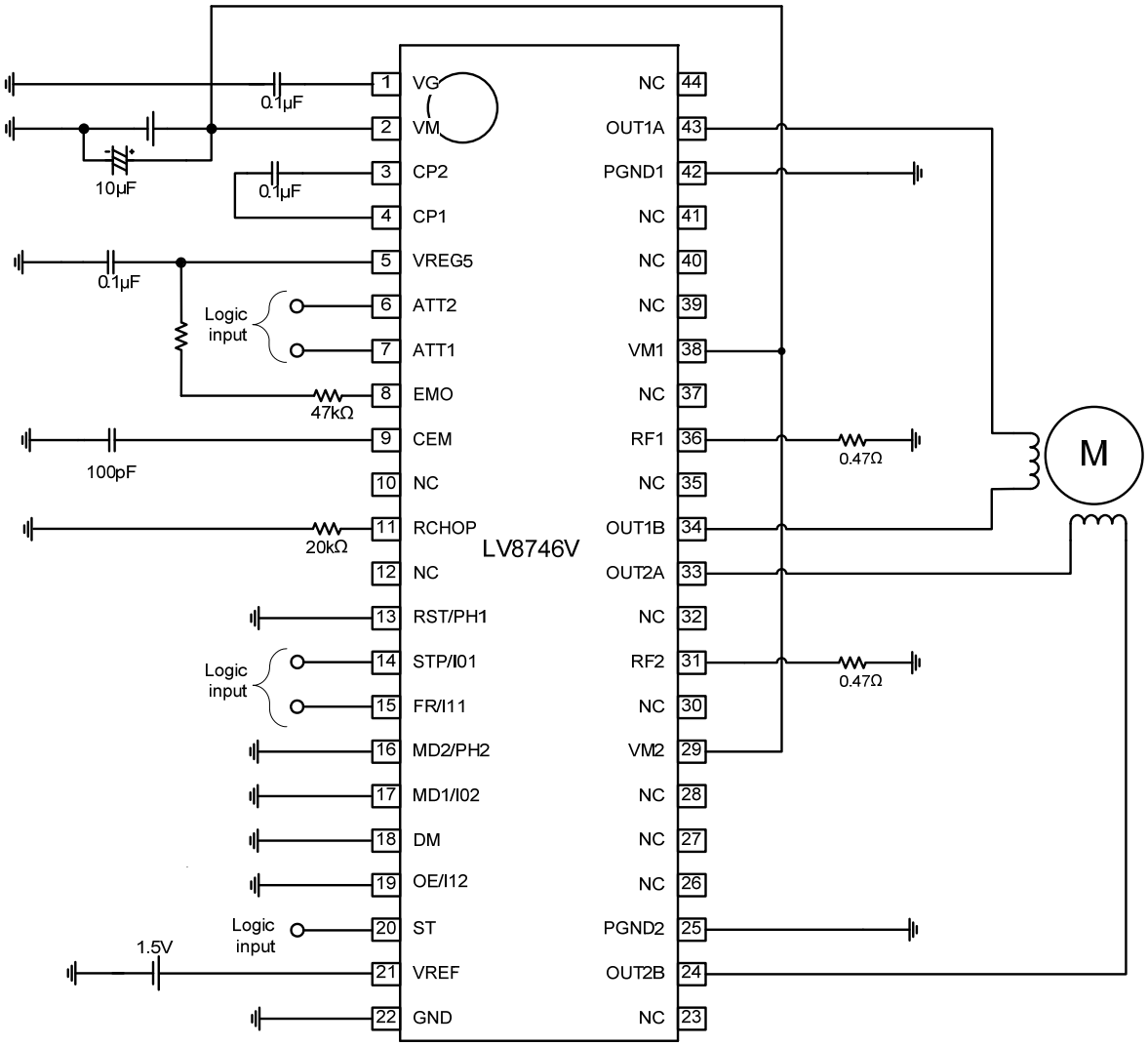
Startup time with different VG capacitor



VM=24V
CP1-CP2=0.1µF
VG=0.1µF/0.22µF/1µF

Application Circuit Example

• Clock input control mode application circuit (DM=Low)



The setting conditions for the above circuit diagram example are as follows :

- Full-step drive (MD1/I02 = Low, MD2/PH2 = Low)
- Reset function fixed to normal operation (RST = Low)
- Chopping frequency : 62.5kHz (RCHOP = 20kΩ)

ATT1	ATT2	Current setting reference voltage
Low	Low	VREF/5×100%
High	Low	VREF/5×67%
Low	High	VREF/5×50%
High	High	VREF/5×33%

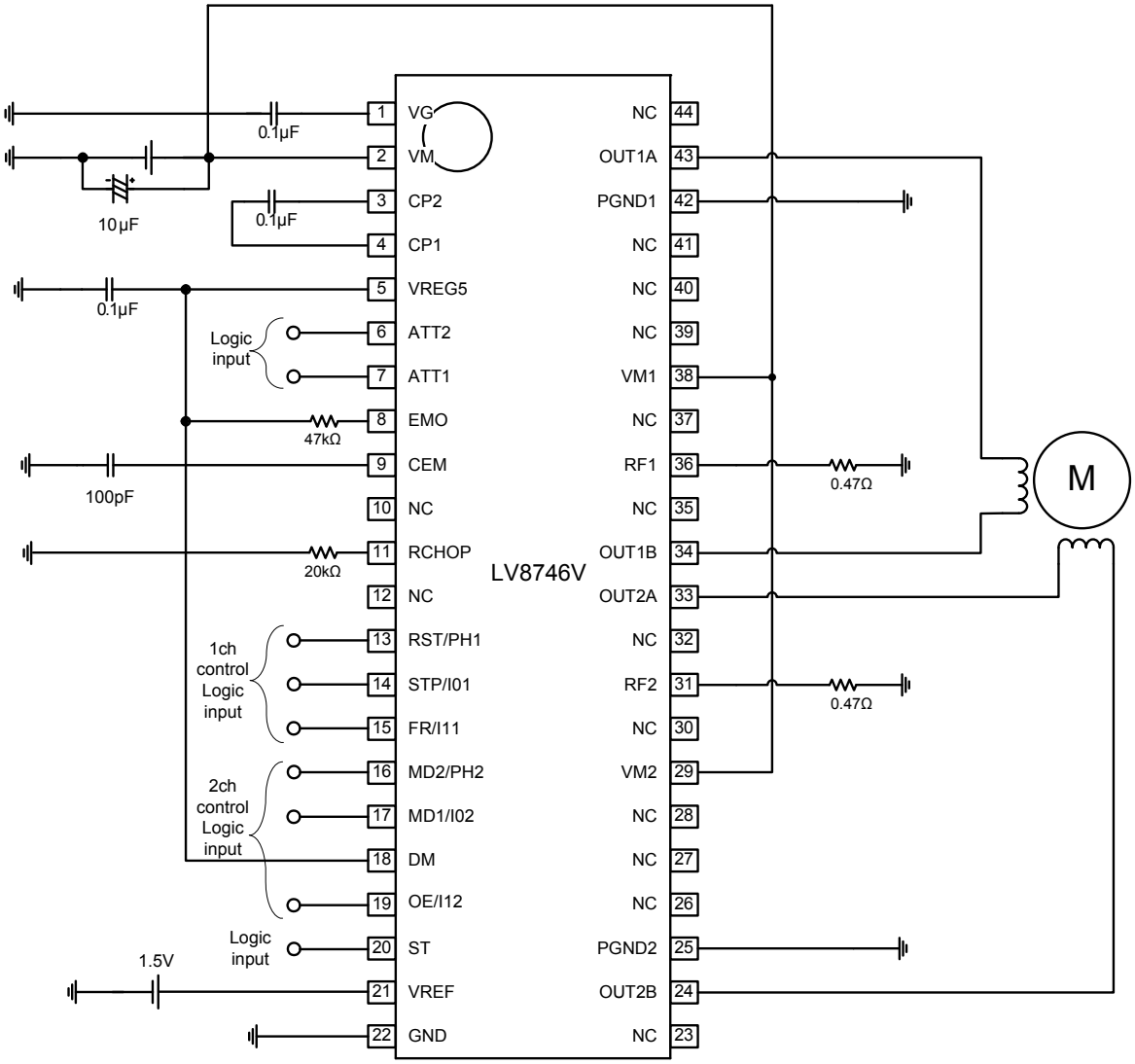
The set current value is as follows :

I_{OUT} = (VREF/5× Voltage setting ratio) / RF

Example: When ATT=Low, ATT2=Low (VREF = 1.5V, RF=0.47Ω)

I_{OUT} = (1.5V / 5 × 1) / 0.47Ω = 0.64A

• Parallel input control mode application circuit (DM = High)



The setting conditions for the above circuit diagram example are as follows :

● Chopping frequency : 62.5kHz (RCHOP = 20kΩ)

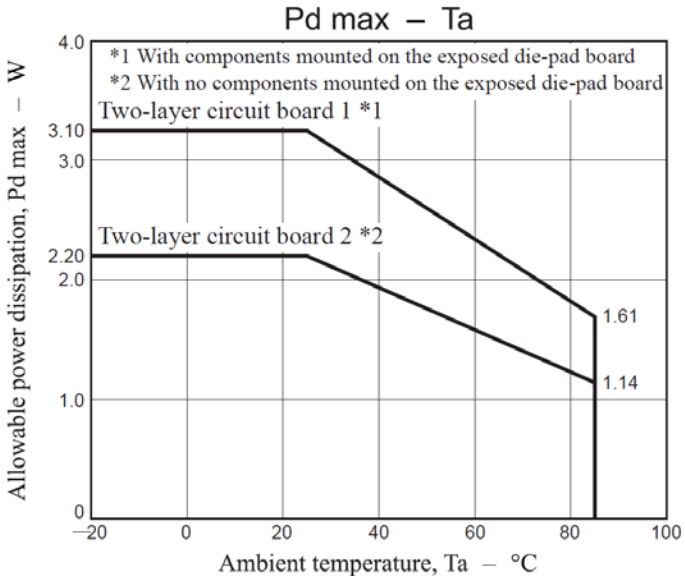
I01(02)	I11(12)	Output current (I_O)
Low	Low	0
High	Low	I_O = ((VREF/5) / RF) × 1/3
Low	High	I_O = ((VREF/5) / RF) × 2/3
High	High	I_O = (VREF/5) / RF

Example: When ATT=Low, ATT2=Low, I01(02)=High, I11(12)=High (VREF = 1.5V, RF=0.47Ω)

I_{OUT} = (1.5V / 5 × 1) / 0.47Ω = 0.64A

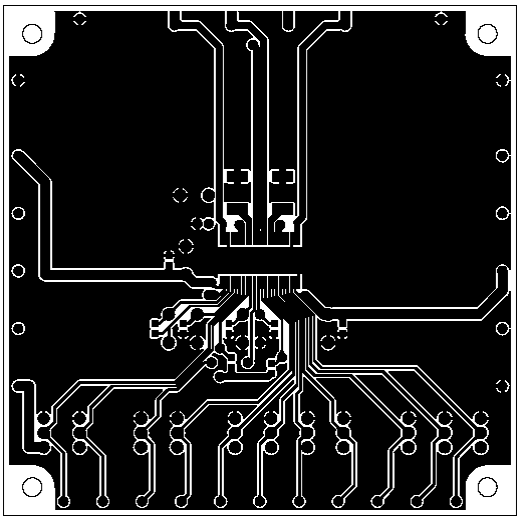
PH1(2)	Electrical current direction
Low	OUTB → OUTA
High	OUTA → OUTB

Allowable power dissipation

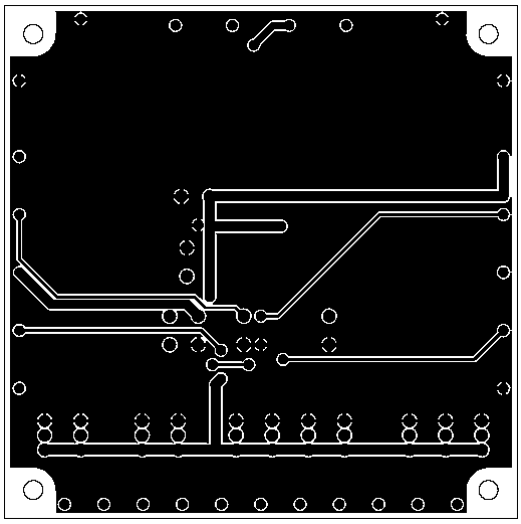


Substrate Specifications (Substrate recommended for operation of LV8746V)

Size	: 90mm × 90mm × 1.6mm
Material	: Glass epoxy
Copper wiring density	: L1 = 85% / L2 = 90%



L1 : Copper wiring pattern diagram



L2 : Copper wiring pattern diagram

Cautions

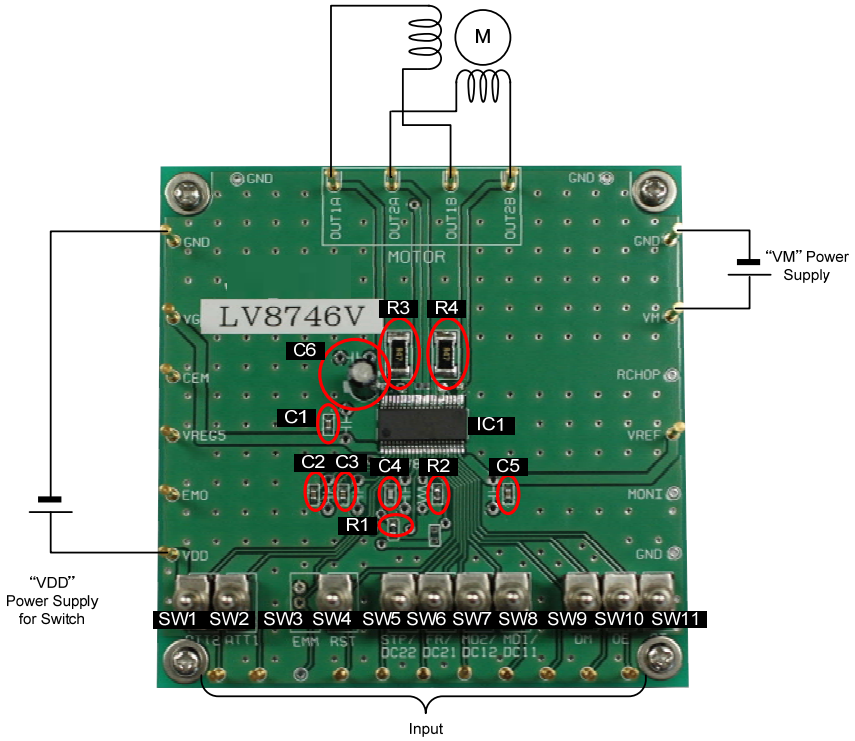
1) The data for the case with the Exposed Die-Pad substrate mounted shows the values when 90% or more of the Exposed Die-Pad is wet.

2) For the set design, employ the derating design with sufficient margin.
Stresses to be derated include the voltage, current, junction temperature, power loss, and mechanical stresses such as vibration, impact, and tension.
Accordingly, the design must ensure these stresses to be as low or small as possible.
The guideline for ordinary derating is shown below:
(1)Maximum value 80% or less for the voltage rating
(2)Maximum value 80% or less for the current rating
(3)Maximum value 80% or less for the temperature rating

3) After the set design, be sure to verify the design with the actual product.
Confirm the solder joint state and verify also the reliability of solder joint for the Exposed Die-Pad, etc.
Any void or deterioration, if observed in the solder joint of these parts, causes deteriorated thermal conduction, possibly resulting in thermal destruction of IC.

Evaluation board

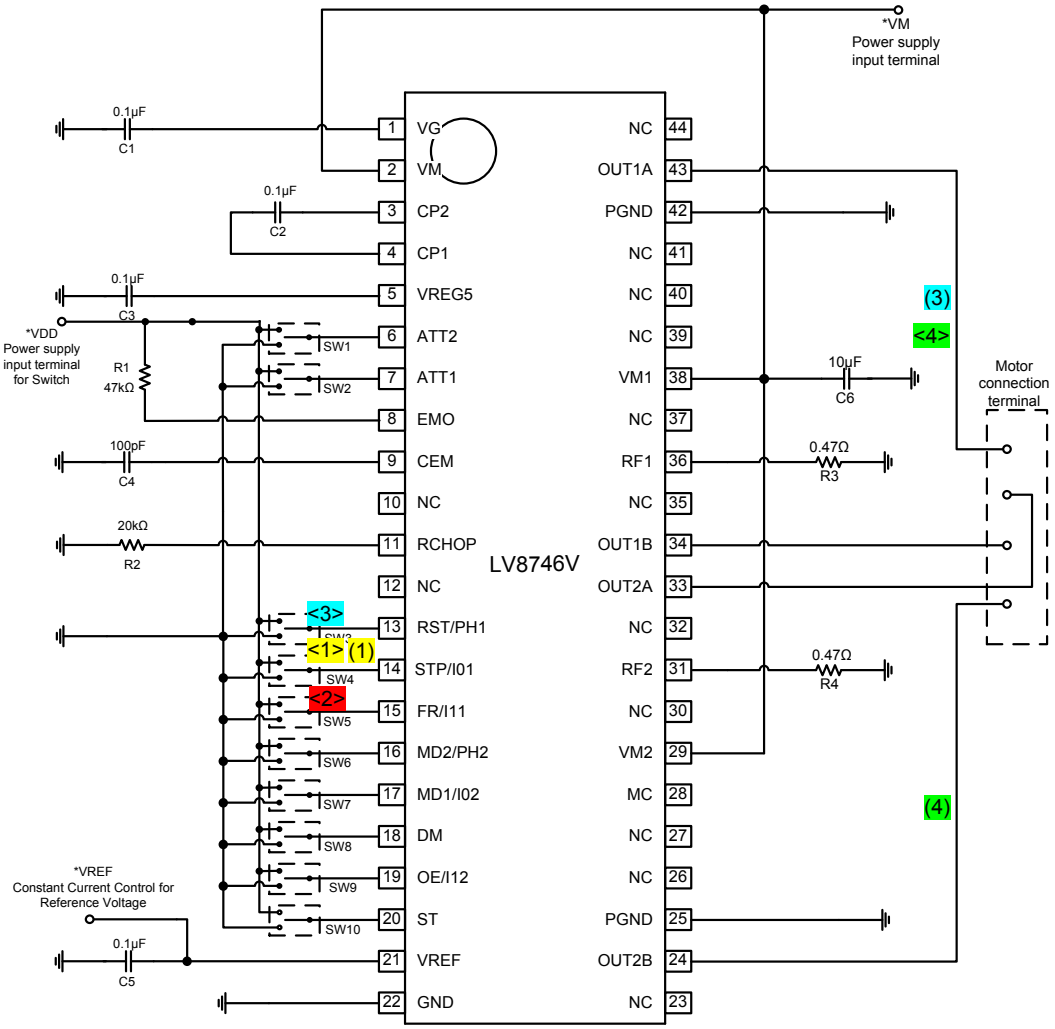
LV8746V (90.0mm×90.0mm×1.6mm, glass epoxy 2-layer board, with backside mounting)



Bill of Materials for LV8746V Evaluation Board

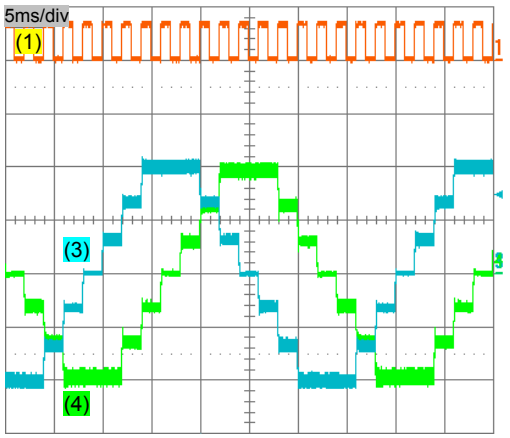
Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Lead Free
C1	1	Capacitor for Charge pump	0.1μF, 100V	±10%		Murata	GRM188R72A104KA35*	Yes	Yes
C2	1	Capacitor for Charge pump	0.1μF, 100V	±10%		Murata	GRM188R72A104KA35*	Yes	Yes
C3	1	5VREG stabilization Capacitor	0.1μF, 100V	±10%		Murata	GRM188R72A104KA35*	Yes	Yes
C4	1	Capacitor to set CEM timer	100pF, 50V	±5%		Murata	GRM1882C1H101JA01*	Yes	Yes
C5	1	VREF stabilization Capacitor	0.1μF, 100V	±10%		Murata	GRM188R72A104KA35*	Yes	Yes
C6	1	VM Bypass Capasitor	10μF, 50V	±20%		SUN Electronic Industries	50ME10HC	Yes	Yes
R1	1	Pull-up Resistor for for terminal EMO	47kΩ, 1/10W	±5%		KOA	RK73B1JT**473J	Yes	Yes
R2	1	Resistor to set chopping frequency	20kΩ, 1/10W	±5%		KOA	RK73B1JT**203J	Yes	Yes
R3	1	Channel 1 output current detective Resistor	0.47Ω, 1W	±5%		ROHM	MCR100JZHJLR47	Yes	Yes
R4	1	Channel 2 output current detective Resistor	0.47Ω, 1W	±5%		ROHM	MCR100JZHJLR47	Yes	Yes
IC1	1	Motor Driver			SSOP44K (275mil)	ON Semiconductor	LV8746V	No	Yes
SW1-SW10	10	Switch				MIYAMA	MS-621C-A01	Yes	Yes
TP1-TP23	23	Test Point				MAC8	ST-1-3	Yes	Yes

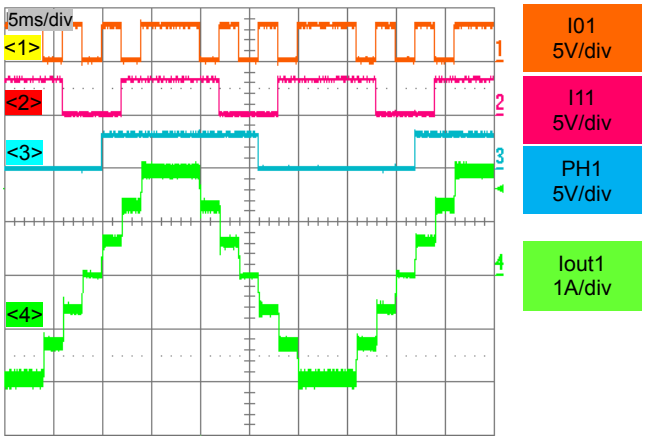
Evaluation board circuit



[Clock input control]
VM=24V,VDD=3.3V,VREF=1.5V
ST=H,DM=L
EMM=L,RST/PH1=L,OE/I12=L
ATT1=ATT2=L,
FR/I11=L
MD1/I02=MD2/PH2=H
STP/I01=500Hz(Duty50%)

[Parallel input control(OUT1A-OUT1B)]
VM=24V,VDD=3.3V,VREF=1.5V
ST=H,DM=H
EMM=L,ATT1=ATT2=L,





Evaluation Board Manual

[Supply Voltage] VM (9 to 35V): Power Supply for LSI
VREF (0 to 3V): Const. Current Control for Reference Voltage
VDD (2 to 5V): Logic “High” voltage for toggle switch

[Toggle Switch State] Upper Side: High (VDD)
Middle: Open, enable to external logic input
Lower Side: Low (GND)

[Operation Guide]

For clock input control

1. **Initial Condition Setting:** Set “Open” the toggle switch STP/I01, and “Open or Low” the other switches
2. **Motor Connection:** Connect the Motors between OUT1A and OUT1B, between OUT2A and OUT2B.
3. **Power Supply:** Supply DC voltage to VM, VREF and VDD.
4. **Ready for Operation from Standby State:** Turn “High” the ST terminal toggle switch. Channel 1 and 2 are into full-step initial position (100%, -100%).
5. **Motor Operation:** Input the clock signal into the terminal STP/I01.
6. **Other Setting**
   i. ATT1, ATT2: Motor current attenuation.
   ii. EMM: Short circuit protection mode change.
   iii. RST/PH1: Initial Mode.
   iv. FR/I11: Motor rotation direction (CW / CCW) setting.
   v. MD1/I02, MD2/PH2: Excitation mode.
   vi. OE/I12: Output Enable.

For parallel input control

1. **Initial Condition Setting:** Set “Open” the toggle switch DM, and “Open or Low” the other switches
2. **Motor Connection:** Connect the Motors between OUT1A and OUT1B, between OUT2A and OUT2B.
3. **Power Supply:** Supply DC voltage to VM, VREF and VDD.
4. **Ready for Operation from Standby State:** Turn “High” the ST and DM terminal toggle switch.
5. **Motor Operation:** Set STP/I01, MD1/I02, RST/PH1, MD1/I02, OE/I12 and MD2/PH2 terminals according to the purpose
6. **Other Setting**
   i. ATT1, ATT2: Motor current attenuation.

[Setting for External Component Value]

1. Constant Current (100%)
   At VREF=1.5V
   Iout =VREF [V] / 5 / RF [Ω]
   =1.5 [V] / 5 / 0.47 [Ω]
   =0.64 [A]
2. Chopping frequency setting.
   62.5kHz (RCHOP=20kΩ)
3. Short Protection Latch Time
   Tscp =CEM [pF] x Vt[V] / Ichg [μA]
   =100 [pF] x 1 [V] / 10 [μA]
   =10 [μS]

Warning:

●Power supply connection terminal [VM, VM1, VM2]
- ✓ Make sure to short-circuit VM, VM1 and VM2.For controller supply voltage, the internal regulator voltage of VREG5 (typ 5V) is used.
- ✓ Make sure that supply voltage does not exceed the absolute MAX ratings under no circumstance. Noncompliance can be the cause of IC destruction and degradation.
- ✓ Caution is required for supply voltage because this IC performs switching.
- ✓ The bypass capacitor of the power supply should be close to the IC as much as possible to stabilize voltage. Also if you intend to use high current or back EMF is high, please augment enough capacitance.

●GND terminal [GND, PGND1, PGND2, Exposed Die-Pad]
- ✓ Since GND is the reference of the IC internal operation, make sure to connect to stable and the lowest possible potential. Since high current flows into PGND, connect it to one-point GND.
- ✓ The exposed die-pad is connected to the board frame of the IC. Therefore, do not connect it other than GND. Independent layout is preferable. If such layout is not feasible, please connect it to signal GND. Or if the area of GND and PGND is larger, you may connect the exposed die pad to the GND.

  (The independent connection of exposed die pad to PGND is not recommended.)

●Internal power supply regulator terminal [VREG5]
- ✓ VREG5 is the power supply for logic (typ 5V).
- ✓ When VM supply is powered and ST is ”H”, VREG5 operates.
- ✓ Please connect capacitor for stabilize VREG5. The recommendation value is 0.1uF.
- ✓ Since the voltage of VREG5 fluctuates, do not use it as reference voltage that requires accuracy.

●Input terminal
- ✓ The logic input pin incorporates pull-down resistor (100kΩ).
- ✓ When you set input pin to low voltage, please short it to GND because the input pin is vulnerable to noise.
- ✓ The input is TTL level (H: 2V or higher, L: 0.8V or lower).
- ✓ VREF pin is high impedance.

●OUT terminal [OUT1A, OUT1B, OUT2A, OUT2B]
- ✓ During chopping operation, the output voltage becomes equivalent to VM voltage, which can be the cause of noise. Caution is required for the pattern layout of output pin.
- ✓ The layout should be low impedance because driving current of motor flows into the output pin.
- ✓ Output voltage may boost due to back EMF. Make sure that the voltage does not exceed the absolute MAX ratings under no circumstance. Noncompliance can be the cause of IC destruction and degradation.

●Current sense resistor connection terminal [RF1, RF2]
- ✓ To perform constant current control, please connect resistor to RF pin.
- ✓ To perform saturation drive (without constant current control), please connect RF pin to GND.
- ✓ If RF pin is open, then short protector circuit operates. Therefore, please connect it to resistor or GND.
- ✓ The motor current flows into RF – GND line. Therefore, please connect it to common GND line and low impedance line.

●NC terminal
- ✓ NC pin is not connected to the IC.
- ✓ If VM line and output line are wide enough in your layout, please use NC

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