



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

Bi-CMOS IC

LV5876MX — Step-down Switching Regulator

Overview

LV5876MX is a 1ch step-down switching regulator. With built-in 0.25Ω power MOSFET switch, it achieves high output current and high efficiency. With low-heat resistance, miniature package MFP8 (200mil) with heat-sink is adopted. Since it is Current mode control type, it has good load current response, and phase compensation is easy. With ON/OFF pin, operating can be less than $90\mu\text{A}$ at stand-by mode. It has cycle-by-cycle over current protection for load devices. With external capacitor, it achieves soft start.

Functions

- 2.0A 1ch step-down regulator
- Small package: MFP8 (200mil) with heat sink
- High efficiency (88% $I_{\text{OUT}} = 1\text{A}$, $V_{\text{IN}} = 12\text{V}$, $V_{\text{O}} = 5\text{V}$)
- Standby mode
- Over-current protection
- Thermal shutdown protection
- Reference voltage: 0.8V
- Inside frequency: 950kHz
- Soft start
- Wide input dynamic range (4.75 to 18V)

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum input V_{IN} voltage	$V_{\text{IN max}}$		20	V
BOOT pin maximum voltage	$V_{\text{BT max}}$		25	V
SW pin maximum voltage	$V_{\text{SW max}}$		$V_{\text{IN max}}$	V
BOOT pin-SW pin maximum voltage	$V_{\text{BS-SW max}}$		7	V
EN Maximum Voltage	$V_{\text{EN max}}$		20	V
FB, COMP, SS pin maximum voltage	$V_{\text{fs max}}$		7	V
Allowable power dissipation	$P_d \text{ max}$	Mount on a specified board *1	2.05	W
Junction temperature	$T_j \text{ max}$		150	$^\circ\text{C}$
Operating temperature	T_{opr}		-20 to 80	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to 150	$^\circ\text{C}$

*1: 46.4mm x 31.8mm x 1.7mm Four layers glass epoxy substrate.

Note: Plan the maximum voltage while including coil and surge voltages, so that the maximum voltage is not exceeded even for an instant.

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LV5876MX

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V _{IN} pin voltage	V _{IN}		4.75 to 18	V
BOOT pin voltage	V _{BT}		-0.3 to 23	V
SW pin voltage	V _{SW}		-0.4 to V _{IN}	V
BOOT pin-SW pin voltage	V _{BS-SW}		6.5	V
EN voltage	V _{EN}		18	V
FB, COMP, SS pin voltage	V _{FSO}		6	V

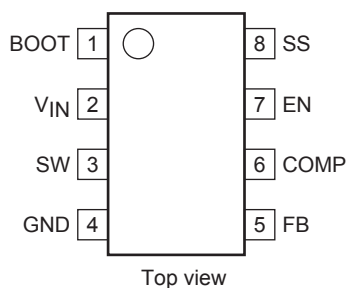
Electrical Characteristics at Ta = 25°C, V_{IN} = 12V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
IC current drain at standby	I _{CC1}	EN=0V		90		μA
IC current drain in operation	I _{CC2}	EN=5V, FB=1V		2.3		mA
Efficiency	Effcy	V _{IN} =12V, I _{OUT} =1A, V _o =5V, Design target *2		88		%
Reference voltage	V _{ref}	V _{IN} =4.75V to 28V	-2%	0.8	+2%	V
FB pin bias current	I _{ref}	FB=0.8V		20	200	nA
High-side ON resistance	R _{onH}	BOOT=5V, I _{OUT} =1A		0.25		Ω
Low-side ON resistance	R _{onL}			5		Ω
Oscillation frequency	f _{OSC}		760	950	1140	kHz
Oscillatory frequency when short-circuit is protected	f _{OSCS}		255	340	425	kHz
EN high-threshold voltage	V _{ENH}		0.9	1.8	2.7	V
EN low-threshold voltage	V _{ENL}		0.7	1.35	2.0	V
Maximum ON DUTY	D max			80		%
SW Peak Current limit 1	I _{cl1}	V _{IN} =12V, V _{OUT} =1.2V, L=2.2μH	3.1		5.7	A
SW Peak Current limit 2	I _{cl2}	V _{IN} =12V, V _{OUT} =3.3V, L=2.2μH	2.8		5.4	A
SW Peak Current limit 3	I _{cl3}	V _{IN} =12V, V _{OUT} =5V, L=2.2μH	2.5		5.1	A
Thermal shutdown temperature	T _{tsd}	*Design guarantee *3		160		°C
Thermal shutdown temperature hysteresis	D _{tsd}	*Design guarantee *3		40		°C
Soft start current	I _{SS}	SS=0V	3	5	7	μA
UVLO threshold voltage	V _{UVLO}	V _{IN} Rising	3.9	4.2	4.5	V
UVLO hysteresis	V _{HYS}			0.2		V

*2: Reference value (not tested IC unit)

*3: Design guarantee (value guaranteed by design and not tested IC unit)

Pin Assignment

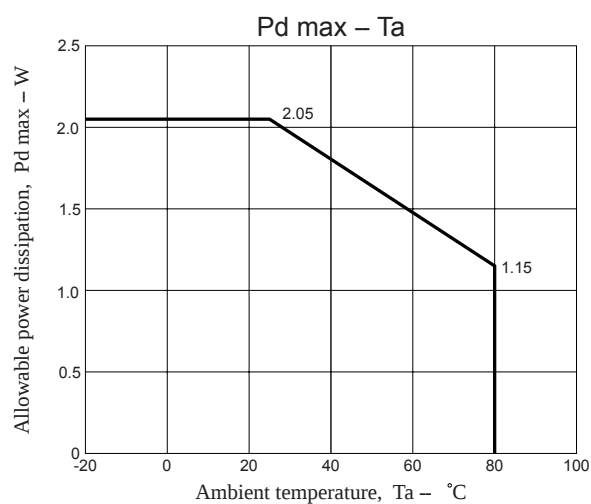
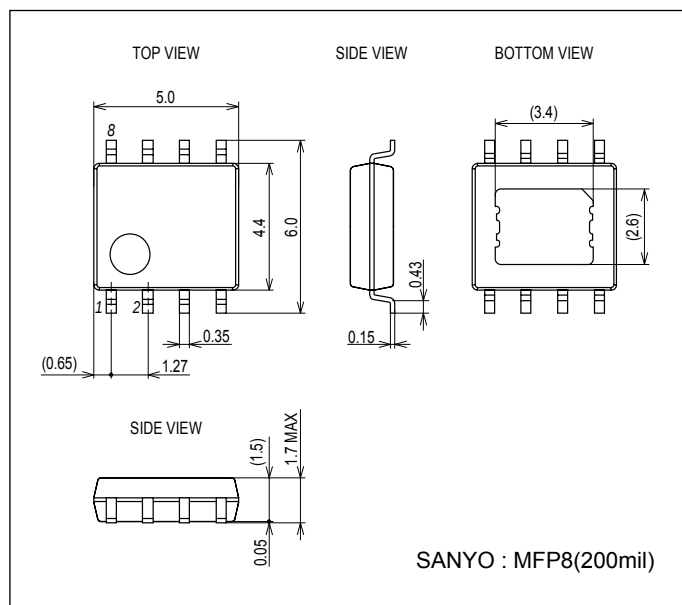


LV5876MX

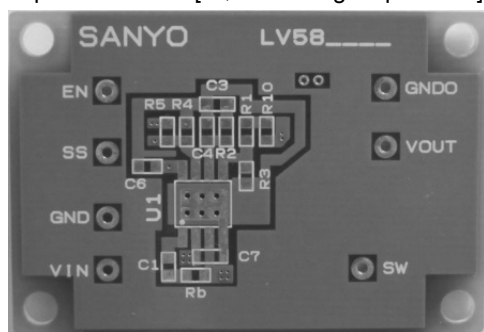
Package Dimensions

unit : mm (typ)

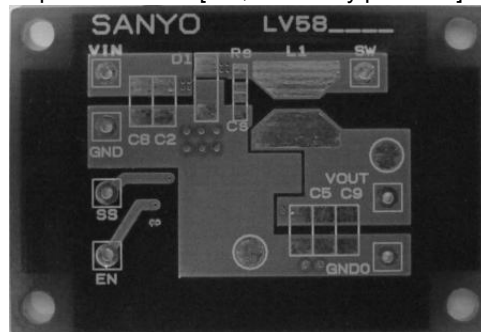
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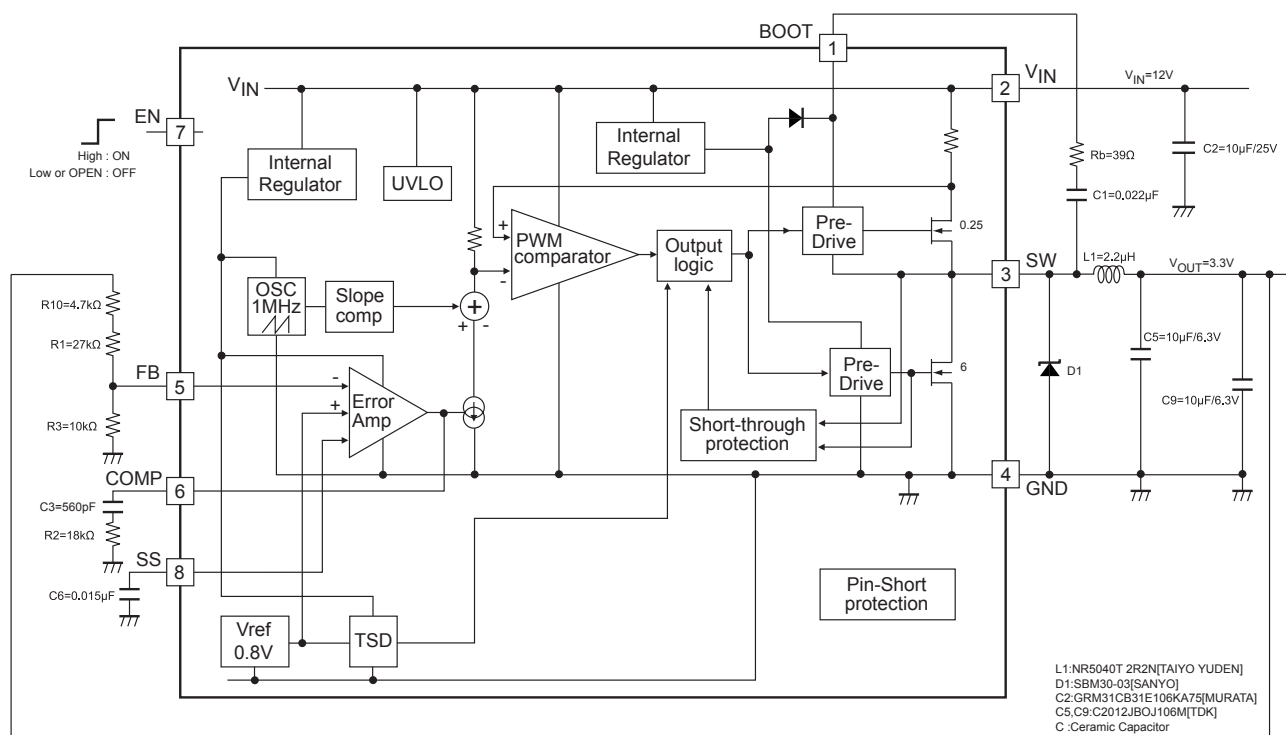
Specified Board [IC, Small signal part side]



Specified Board [coil, Schottky part side]



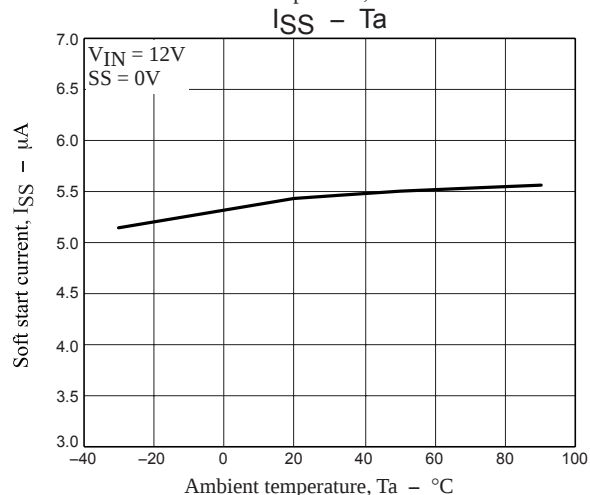
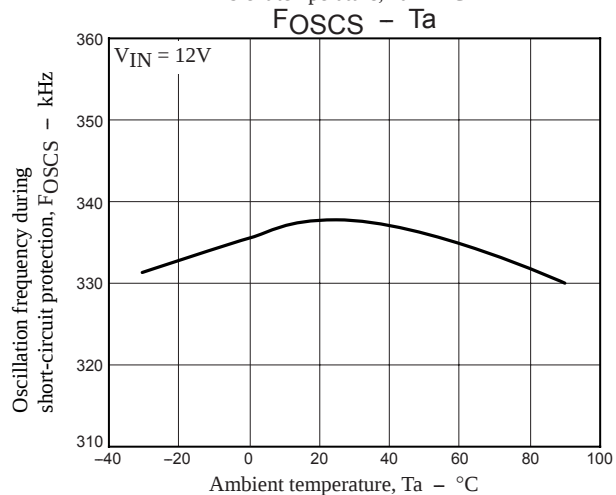
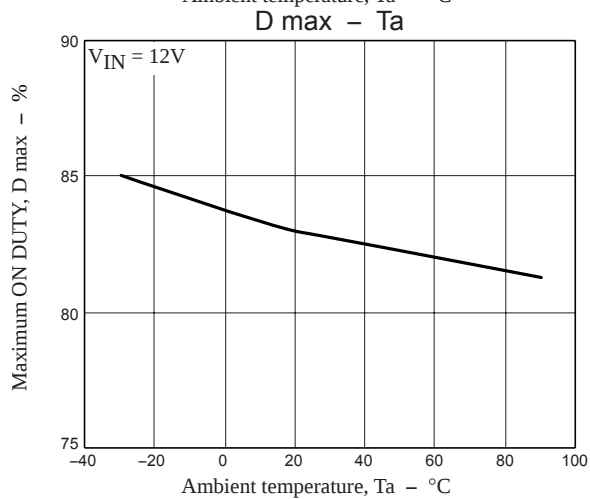
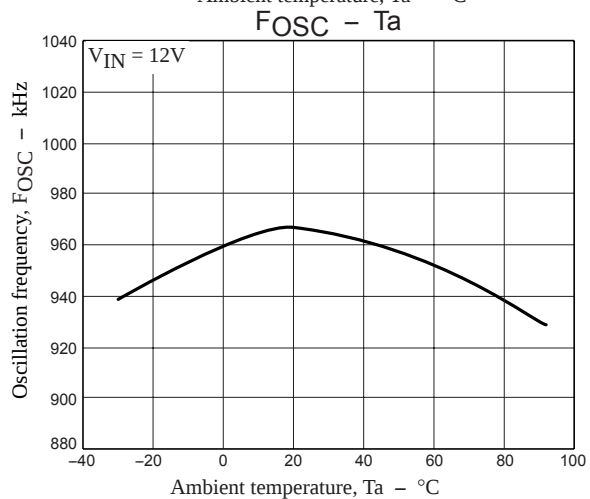
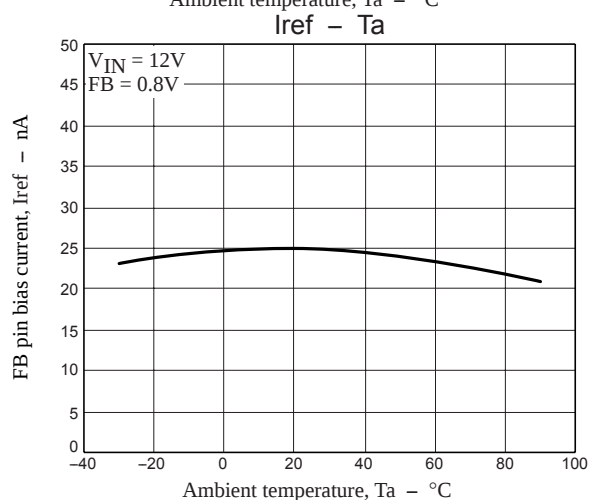
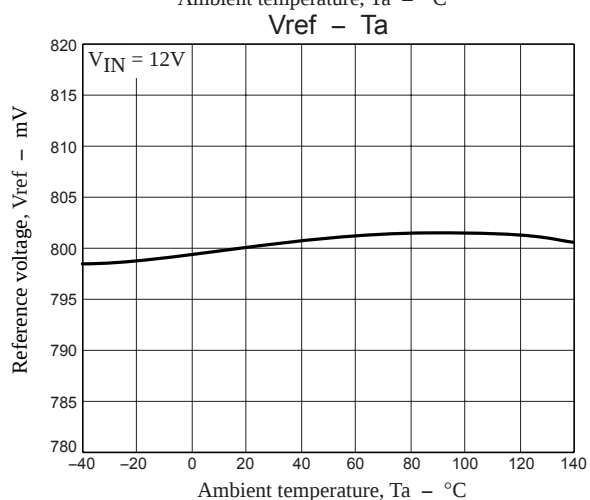
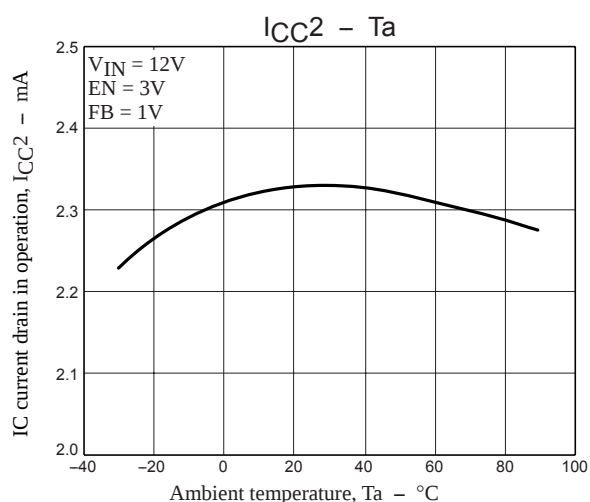
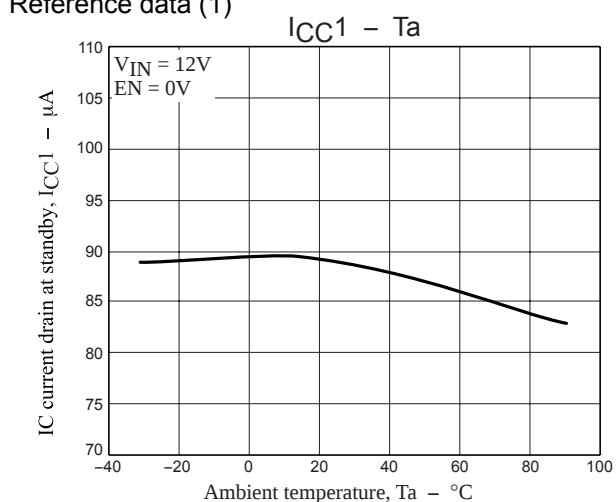
Block Diagram and Sample Application Circuit

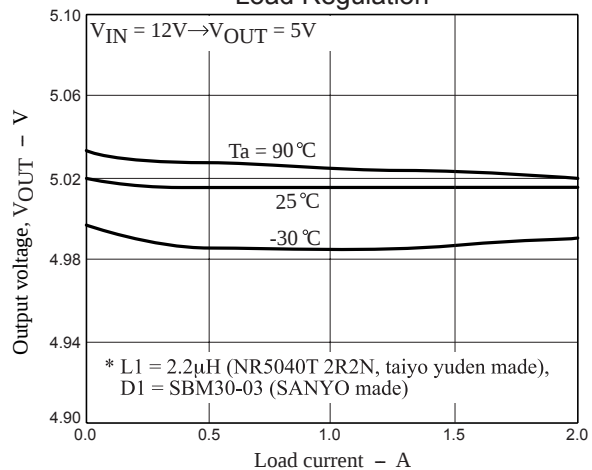
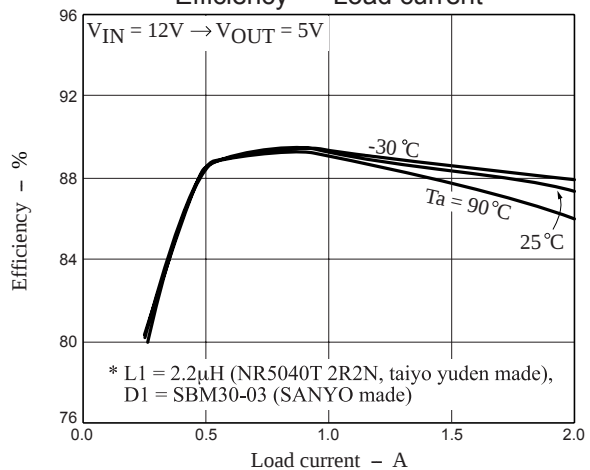
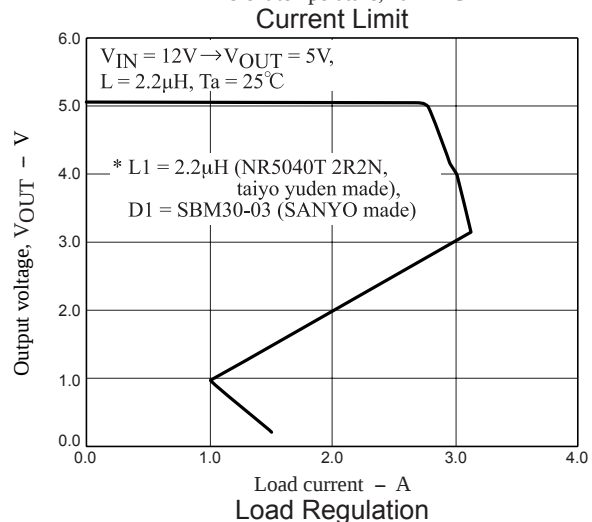
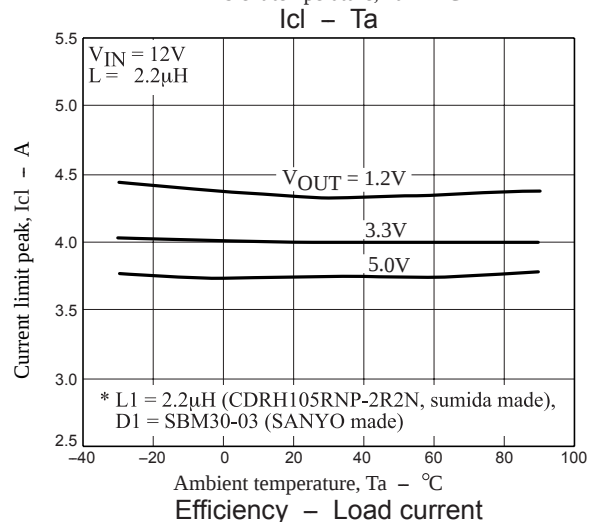
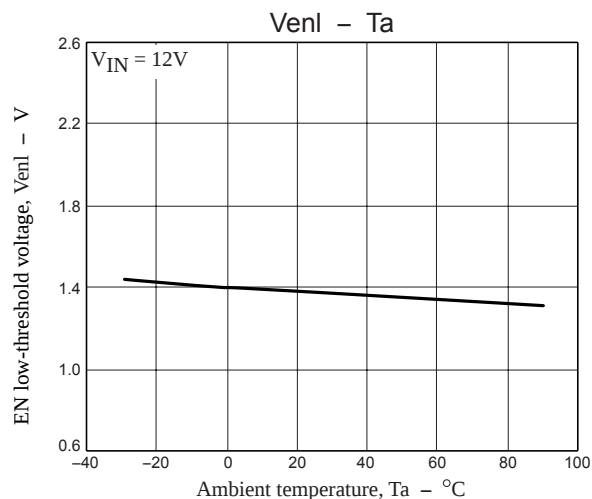
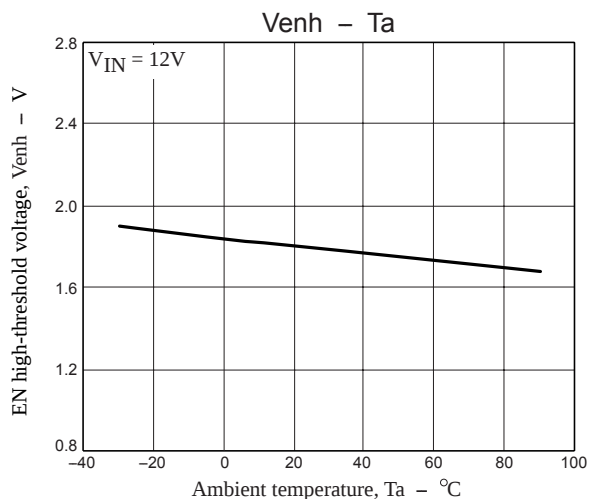


Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	BOOT	Upper MOS transistor boot strap capacitance connection pin. Connect the boot capacitance of about 0.022uF between SW pins. To protect the SW pin's absolute maximum rating, to ensure stable operation, and to eliminate noise, the boot capacitance serial resistance (about 100Ω) Rb proves effective.	
2	V _{IN}	Input Voltage Pin. Connect substantially large (10uF more) capacitance between this pin and GND.	
3	SW	Power Switch pin. Connect the output LC filter. Connect the above capacitance between this pin and BOOT pin.	
4	GND	Ground pin.	
5	FB	Feedback pin. Set the output voltage by means of split resistor in the section of the output voltage VOUT-FB-GND. VOUT setting is made as calculated below. $V_{OUT} = V_{ref} \times \left\{ 1 + \frac{(R1 + R10)}{R3} \right\}$ $V_{ref} = 0.8V$ Example: 3.3V output voltage (See, Block Diagram and Application example) $V_{OUT} = 0.8 \times \left\{ 1 + \frac{(27k + 4.3k)}{10k} \right\}$ $= 3.304V$	
8	SS	Soft start pin. Sets the soft start time by means of the built-in 5uA source voltage and external soft start capacity. The soft start capacity C _{SS} can be set as follows: $C_{SS} = 5\mu A \times \frac{T_{ss}}{V_{ref}}$ Where, T _{ss} is the soft start time and V _{ref} is the reference voltage. Example: 2.4ms soft start time achieved $C_{SS} = 5\mu A \times \frac{2.4ms}{0.8V} = 0.015\mu F$	
6	COMP	Phase compensation pin. Connects with the phase compensation external capacitance and resistance of DC/DC converter close loop.	
7	EN	Enable pin. Converter enabled when set to the HIGH voltage and disabled when GND or OPEN state.	

Reference data (1)

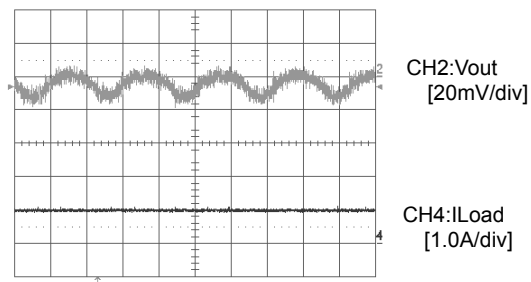




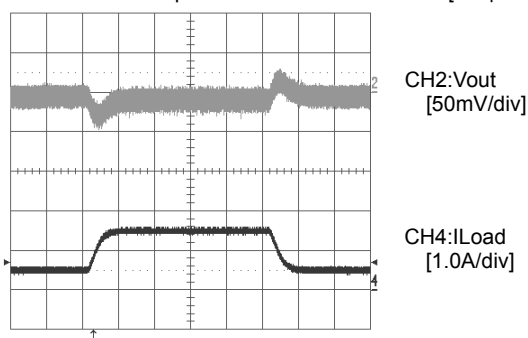
Reference data (2)

(* measurement circuit is shown in “Block Diagram and Sample Application circuit”)

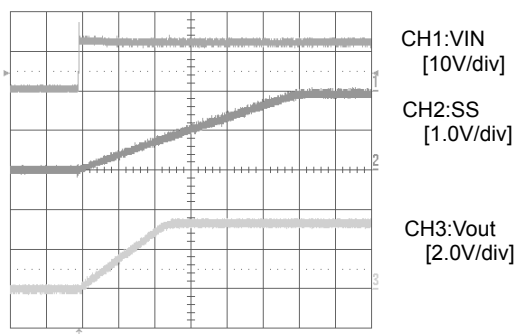
•Output voltage ripple I_{Load}=1.0A [0.5μsec/div]



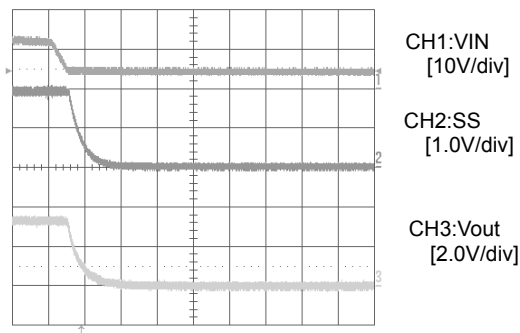
•Load transient response I_{Load} = 0.5A ↔ 1.5A [100μsec/div]



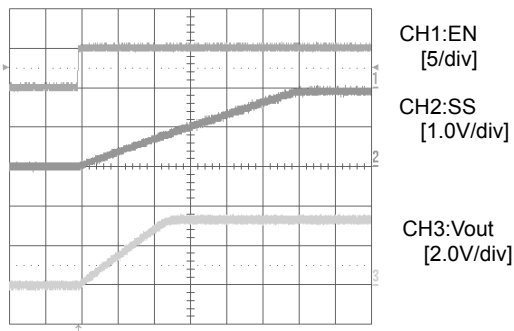
•V_{IN} start up waveform Rload = 3.3Ω [1msec/div]



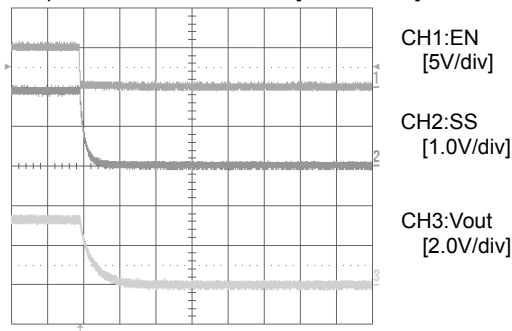
•V_{IN} stop waveform Rload = 3.3Ω [0.2msec/div]



•EN start up waveform Rload = 3.3Ω [1msec/div]



•EN stop waveform Rload = 3.3Ω [0.2msec/div]



Considerations for the design

- Insertion of serial beads in the Schottky diode for removal of noise may cause generation of the negative voltage deviating from the absolute maximum rating at the SW pin, resulting in failure of normal operation. In such an event, do not insert beads as above described and, instead, remove noise by means of the BOOT resistance Rb

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