LV52207NXB

LED Boost Driver, Dual channel, PWM, 1-Wire Dimming

ON Semiconductor®

www.onsemi.com

Overview

The LV52207NXB is a high voltage boost driver for LED drive with 2 channels adjustable constant current sources.

Features

- Operating Voltage from 2.7V to 5.5V
- Integrated 40V MOSFET
- 1-Wire 255 level digital and PWM dimming
- Supports CABC
- 600kHz Switching Frequency
- 37.5V OverVoltage Protection (OVP) Threshold

Typical Applications

LED Display Backlight Control

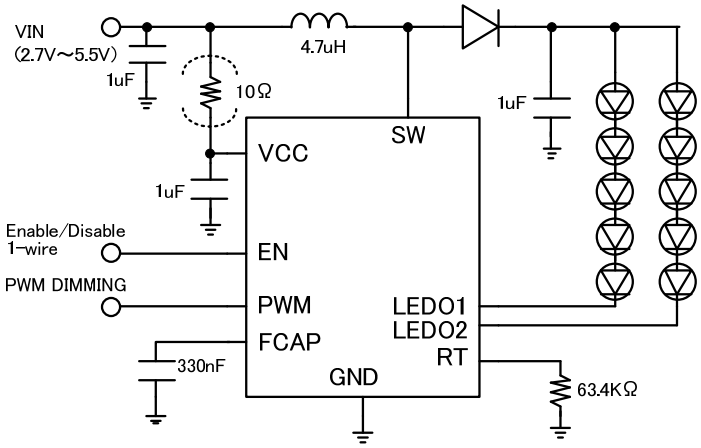
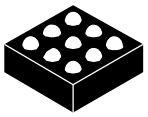
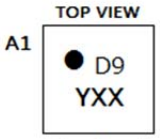


Fig1. 5x2 LED Application



WLP9J, 1.31x1.31, 0.4mm pitch
(1.31mm x 1.31mm, Amax=0.65 mm)

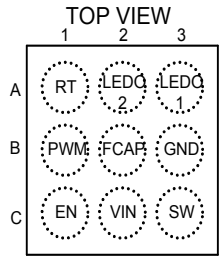
MARKING DIAGRAM



D9 = Device Code
YXX = Assembly Lot Code

OPTION:BACKSIDE COATING

PIN CONNECTION



ORDERING INFORMATION

Ordering Code:
LV52207NXB-VH

Package
WLP9J (1.31x1.31)
(Pb-Free / Halogen Free)

Shipping (Qty / packing)
5000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

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Specifications

Absolute Maximum Ratings at Ta = 25°C (Note 1)

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	V_{CC}	6	V
Maximum Pin voltage1	V1 max	SW	40	V
Maximum Pin voltage2	V2 max	Other pin	5.5	V
Allowable power dissipation	Pd max	Ta=25°C (Note 2)	1.05	W
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−55 to +125	°C

1. Stresses exceeding those listed in the Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Mounted on the following board: 70mm×70mm×1.6mm (4 layer glass epoxy)
3. Absolute maximum ratings represent the values which cannot be exceeded for any length of time.
4. When the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be decrease. Please contact ON Semiconductor for the further details.

Recommended Operating Conditions at Ta = 25°C (Note 5)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range1	V_{CC} op	VCC	2.7 to 5.5	V
PWM frequency	F_{PWM}	PWM pin input signal	300 to 100k	Hz
Min. Duty% on PWM pin	$D_{MIN\ PWM}$	PWM pin input signal	0.9%	

5. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics Analog block (Note 6)

at Ta=25°C, VCC=3.6V, RT resistor=63.4KΩ unless otherwise specified

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby current dissipation	Icc1	EN=PWM=L		0	2.0	μA
DC/DC current dissipation1	Icc2	Device enable, switching 0.6 MHz and no load		0.7	1.2	mA
Feedback Voltage	V_{FB}	LEDO1, 2=20mA		0.2		V
Output Current1	I_{O1}	LEDO1, LEDO2, LEDISET=20mA Duty=100%	19.6	20	20.4	mA
Output Current Matching1	I_{OM1}	LEDO1, LEDO2, LEDISET=20mA Duty=100% (IMAX – IAVG) / IAVG		0.3	2.0	%
LEDO1, 2 max current	I_{MAX}	LEDO1 LEDO2	40			mA
LEDO1, 2 leak current	I_{LEAK}	LEDO1 LEDO2			1.0	μA
OVP Voltage	V_{OVP}	SW_pin over voltage threshold	36	37.5	39	V
LEDO_OVP Voltage	$V_{OVP,LED}$	LEDO_pin over voltage threshold LEDO_DC rising	4.2	4.5	5.0	V
SW_{OUT} ON resistance	R_{ON}	I_L=100mA		300		mΩ
NMOS Switch Current Limit	I_{LIM}		1.0	1.5		A
OSC Frequency	F_{OSC}		500	600	750	kHz
High level input voltage	V_{INH}	EN PWM	1.2		V_{CC}	V
Low level input voltage	V_{INL}	EN PWM	0		0.4	V
Under Voltage Lockout	V_{UVLO}	VIN falling		2.2		V
EN pin output voltage for Acknowledge	V_{ACK}	$R_{PULL-UP}$ =15kΩ			0.4	V

6. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

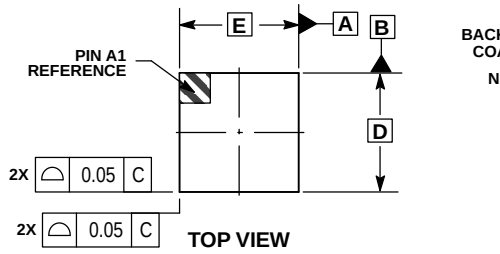
Recommended EN PWM Timing at Ta=25°C, V_{CC}=3.6V, unless otherwise specified

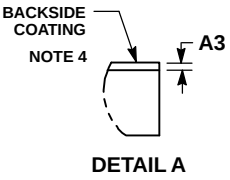
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Dimming mode selectable time	T_{SEL}		1.0		2.2	ms
Delay time to start digital mode detection	T_{w0}		100			μs
Low time to switch to digital mode	T_{w1}		260			μs
EN pin low time to shutdown	$T_{OFF, EN}$		2.5			ms
PWM pin low time to shutdown	$T_{OFF, PWM}$		20			ms
1-wire start time for digital mode programming	T_{START}		2.0			μs
1-wire end time for digital mode programming	T_{END}		2.0		360	μs
1-wire High time of bit 0	T_{H0}	Bit detection=0	2.0		180	μs
1-wire Low time of bit 0	T_{L0}	Bit detection=0	Th0 × 2		360	μs
1-wire High time of bit 1	T_{H1}	Bit detection=1	Tl1 × 2		360	μs
1-wire Low time of bit1	T_{L1}	Bit detection=1	2.0		180	μs
DCDC startup delay	T_{DEL}			5		ms
Delay time of Acknowledge	T_{ACKD}				2	μs
Duration of Acknowledge	T_{ACK}				512	μs

Package Dimensions

unit : mm

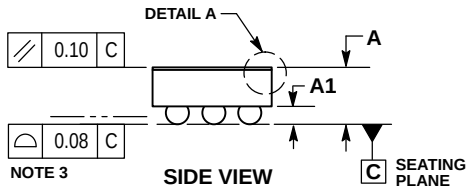
WLCSP9, 1.31x1.31
CASE 567HX
ISSUE C

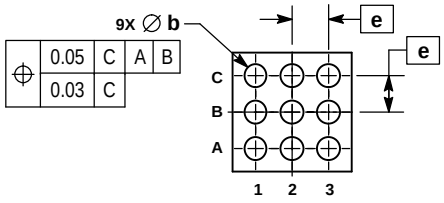




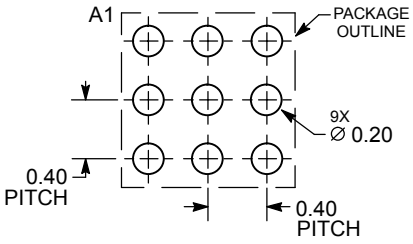
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. BACKSIDE COATING IS OPTIONAL.

DIM	MILLIMETERS MIN	MAX
A	---	0.65
A1	0.16	0.26
A3	0.025 REF	
b	0.21	0.31
D	1.31 BSC	
E	1.31 BSC	
e	0.40 BSC	





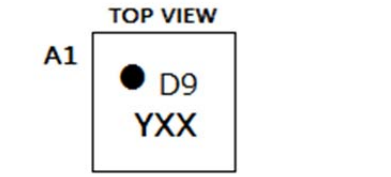
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

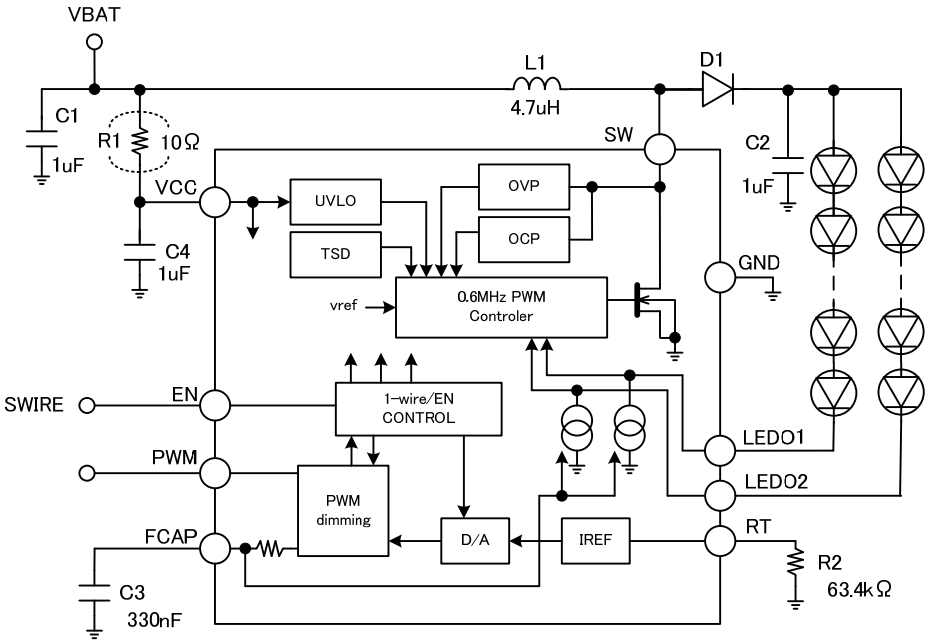
MARKING DIAGRAM



D9 = Device Code
YXX = Assembly Lot Code

OPTION:BACKSIDE COATING

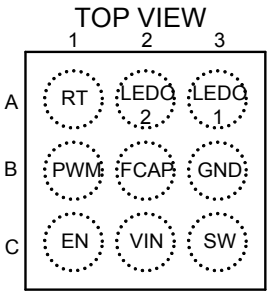
Block Diagram



L1 : VLS3012E-4R7M (TDK), VLF504015-4R7 (TDK)
VLS3012E-100M (TDK), VLF504015-100M (TDK)
D1 : MBR0540T1 (ON Semiconductor), NSR05F40 (ON Semiconductor)
C2 : GRM21BR71H105K (Murata), C1608X5R1H105K (TDK)

Fig2. Block Diagram

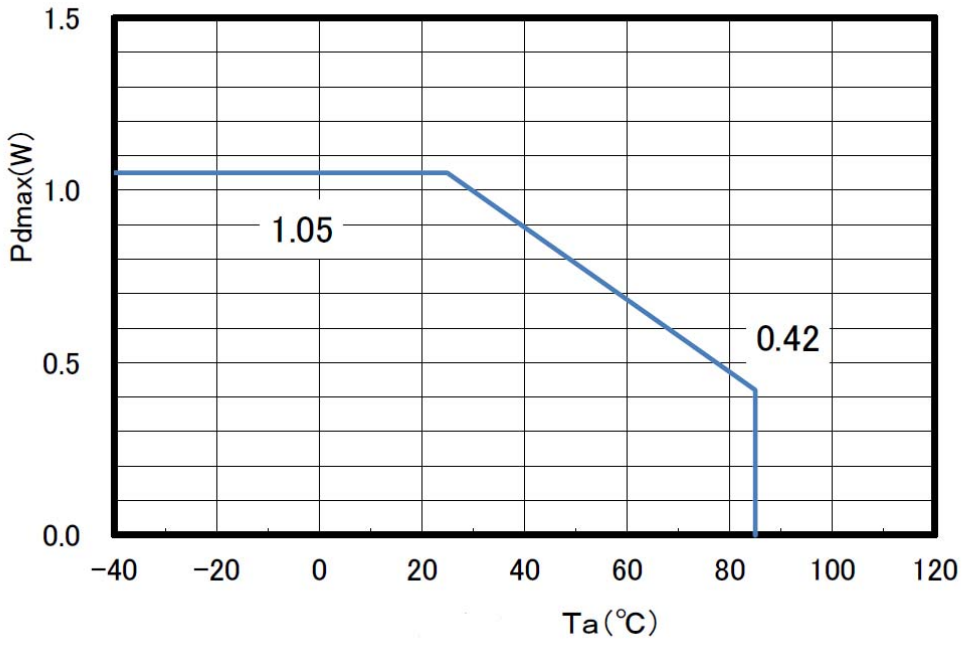
Pin Connection



Pin Function

PIN #	Pin Name	Description
A1	RT	Connecting a resistor terminal for Full scale LED current setting
A2	LEDO2	Constant Current Output_pin2
A3	LEDO1	Constant Current Output_pin1
B1	PWM	PWM dimming input (active High).
B2	FCAP	Filtering capacitor terminal for PWM mode
B3	GND	Ground
C1	EN	1-wire control and Enable control input (active High).
C2	VIN	Supply voltage.
C3	SW	Switch pin. Drain of the internal power FET.

Pd-Max



Mounted on the following board : 70 mm × 70 mm × 1.6 mm (4 layer glass epoxy)

LED Current Setting (max sink current)

LED_full current is set by an external resistor connected between the RT pin and ground.

$$I_{LED_Full} = 2113 * \frac{V_{RT}}{R_{RT}}$$

V_{RT}: RT pin DC Voltage; typically 0.6 V
R_{RT}: RT pin resistor to ground

Eg: RT_res= 63.4 kΩ at typical V_{RT}

$$I_{LED_Full} = 2113 * \frac{V_{RT}}{R_{Rt}} = 2113 * \frac{0.6\ V}{63.4\ k\Omega} = 19.99\ mA \cong 20\ mA$$

BRIGHTNESS CONTROL

The LV52207NXB controls the DC current of the dual channels. The DC current control is normally referred to as analog dimming mode.
The LV52207NXB can receive digital commands at the EN pin (1-wire digital interface, known as **Digital Mode**) and the PWM signals at the PWM pin (PWM interface, known as **PWM Mode**) for brightness dimming.

Dimming Mode Selection

Dimming Mode is selected by a specific pattern of the EN pin within T_{SEL} of 1.0 ms from the startup of the device every time.

Digital Mode

To enter Digital Mode, EN pin should be taken high for more than T_{w0} =100µs from the first rising edge and keep low state for T_{W1} = 260µs before T_{SEL}=1ms.

When using Digital mode, the PWM pin should be kept high.
It is required sending the device address byte and the data byte to select LEDI. The bit detection is determined by the ratio of T_H and T_L(See Fig5). The start condition for the bit transmission required EN pin high for at least Tstart. The end condition is required EN pin low for at least Tend. When data is not being transferred, EN pin is set in the "H" state. These registers are initialized with shutdown.

Start up and Shutdown

The device becomes enabled when EN pin is initially taken high. The dimming mode is determined within T_{SEL} and the boost converter start up after T_{DEL}. To place the device into shutdown mode, the SWIRE must be held low for T_{OFF}. For specific timings please refer to the **Recommended EN PWMIN Timing** Table on page 3 or the below figures.

Digital MODE

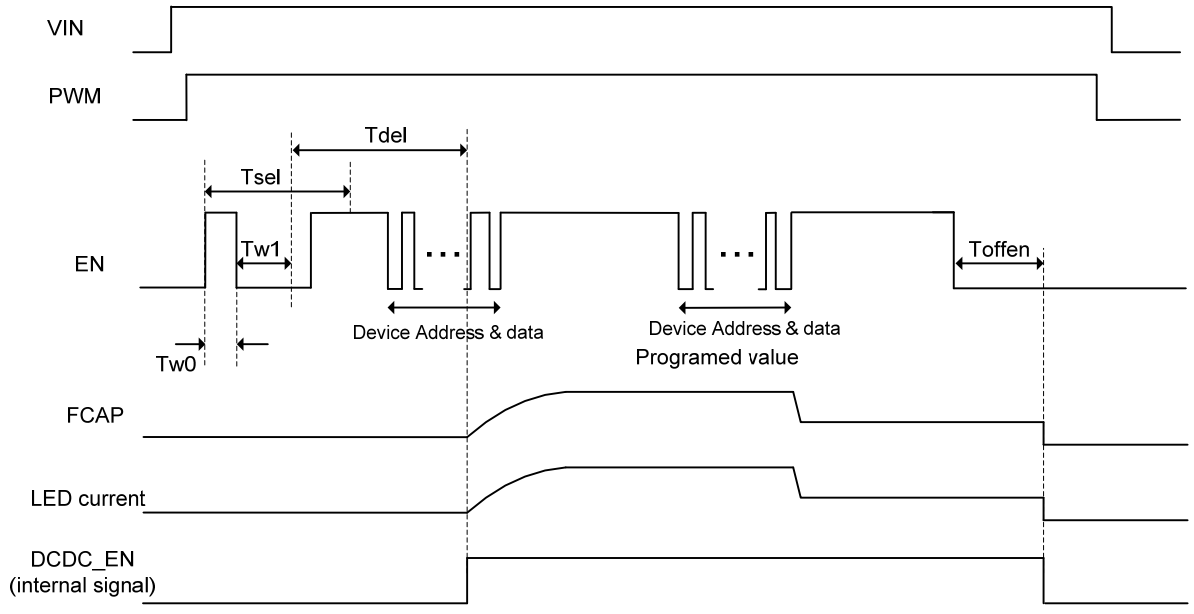


Fig3. Start up and shutdown diagram **(DIGITAL MODE)**

1-Wire Programming

Figure 15 and Table 2 give an overview of the protocol used by LV52207NXB. A command consists of 24 bits, including an 8-bit device address byte and a 16-bit data byte. All of the 24 bits should be transmitted together each time, and the LSB bit should be transmitted first. In the LV52207NXB, the device address (DA7(MSB)to DA0(LSB)) is specified as “10001111”. AKct is setting for the acknowledge response. If the device address and the data byte are transferred on AKct=1, the ACK signal is sent from the receive side to the send side. The acknowledge signal is issued when EN pin on the send side is released and EN pin on the receive side is set to low state.

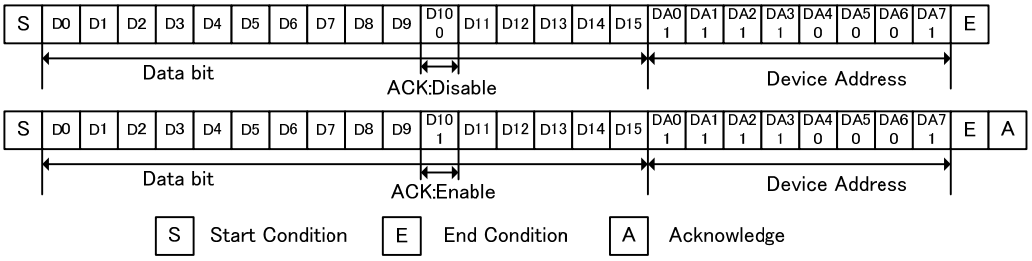


Fig4. Example of writing data

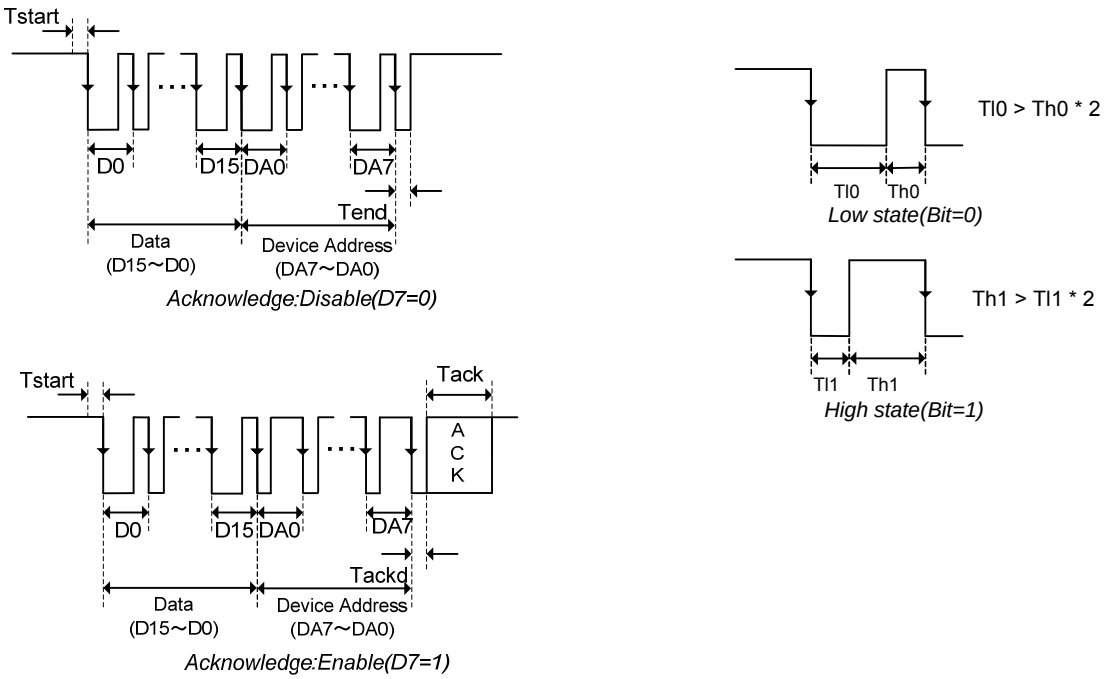


Fig5. Bit detection Diagram

BITE	Register	BIT	Description
Device Address (0x8F)	DA7	23(MSB)	1
	DA6	22	0
	DA5	21	0
	DA4	20	0
	DA3	19	1
	DA2	18	1
	DA1	17	1
	DA0	16	1
Data	D15	15	Data bit 15 No information. Write 0 to this bit.
	D14	14	Data bit 14 No information. Write 0 to this bit.
	D13	13	Data bit 13 No information. Write 0 to this bit.
	D12	12	Data bit 12 No information. Write 0 to this bit.
	D11	11	Data bit 11 No information. Write 0 to this bit.
	AKct(D10)	10	0 = Acknowledge disabled 1 = Acknowledge enabled
	D9	9	Data bit 9
	D8	8	Data bit 8
	D7	7	Data bit 7
	D6	6	Data bit 6
	D5	5	Data bit 5
	D4	4	Data bit 4
	D3	3	Data bit 3
	D2	2	Data bit 2
	D1	1	Data bit 1 LSB of brightness code
	D0	0(LSB)	Data bit 0 No information.

Table1. Bit Description

LED Current setting RT resistor= 63.4KΩ (for $I_{LED\ Full}$ = 20 mA)
NOTE: If you change the RT resistor, the LED Currents will all change.
$I_{LED} = I_{LED_FULL} * \frac{code\#}{255}$; Where I_{LED_FULL} is the current calculated above
$I_{LED} = I_{LEDO1} = I_{LEDO2}$

code	D8	D7	D6	D5	D4	D3	D2	D1	LED Current(mA)
0	0	0	0	0	0	0	0	0	0 Unavailable
1	0	0	0	0	0	0	0	1	0.22
2	0	0	0	0	0	0	1	0	0.30
3	0	0	0	0	0	0	1	1	0.38
4	0	0	0	0	0	1	0	0	0.47
5	0	0	0	0	0	1	0	1	0.55
6	0	0	0	0	0	1	1	0	0.63
7	0	0	0	0	0	1	1	1	0.70
8	0	0	0	0	1	0	0	0	0.78
9	0	0	0	0	1	0	0	1	0.86
10	0	0	0	0	1	0	1	0	0.94
. .	.								. .
246	1	1	1	1	0	1	1	0	19.30
247	1	1	1	1	0	1	1	1	19.38
248	1	1	1	1	1	0	0	0	19.46
249	1	1	1	1	1	0	0	1	19.54
250	1	1	1	1	1	0	1	0	19.61
251	1	1	1	1	1	0	1	1	19.69
252	1	1	1	1	1	1	0	0	19.77
253	1	1	1	1	1	1	0	1	19.84
254	1	1	1	1	1	1	1	0	19.93
255	1	1	1	1	1	1	1	1	20 *Default

Table2. Data Register vs LED current sink

PWM Mode

The dimming mode is set to PWM mode when it is not recognized as a digital mode within T_{sel}. The LV52207NXB can receive the PWM signals at the PWM pin (PWM interface, also known as**PWM Mode**) for brightness dimming. When using PWM interface, the EN pin should be kept high. If EN pin is High, PWM pin alone is used to enable and disable the IC. When EN pin is High and PWM pin is High , this IC is enabled. When EN pin is Low for more than 2.5 ms or when PWM pin is Low for more than 20 ms, the IC is disabled.

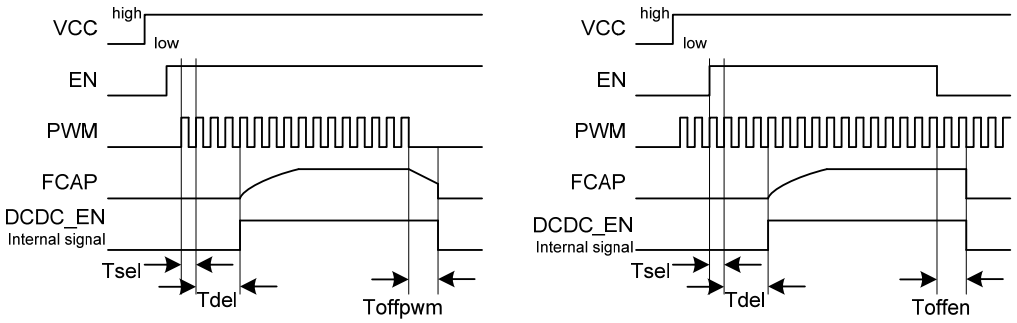


Fig6. Start up and shutdown diagram **(PWM MODE)**

LEDO1 or LEDO2 UNUSED

If only one channel is used, a user can turn OFF a branch current by connecting the unused channel to ground.
If both LEDO1 pin and LEDO2 pin are connected to ground, boost converter will not start up.

Over Voltage Protection (SW OVP)

SW pin over-voltage protection is set at 37.5 V. **This IC monitors the Voltage at SW pin**. When the voltage exceeds OVP threshold the switching converter stops switching.
If SW terminal voltage exceeds a threshold V_{OVP} = 37.5 V typ. for 8 cycles, boost converter enters shutdown mode. In order to restart the IC, SWIRE signal must be used again.

Over Voltage Protection (LEDO OVP)

LED pin over-voltage protection is set at 4.5 V (rising) and 3.5 V (falling). **This IC monitors the Voltage at LEDO1 pin and LEDO2 pin**. When the voltage exceeds LEDO OVP threshold the switching converter stops switching. LED current sink keep.

Open LED Protection

When one LED string becomes open:
If one LED string is open, open channel voltage is approximately ground, the boost output voltage is increased and other LEDO channel voltage is increased. When SW pin voltage is reached the SW OVP threshold the LV52207NXB's switching converter stops switching. When the other LEDO pin voltage reaches the LEDO OVP threshold the LV52207NXB's switching converter stops switching.

When both LED strings become open:
If both LED strings are open, LEDO1 pin voltage and LEDO2 pin voltage are approximately ground and the boost output voltage is increased When SW pin voltage is reached the SW OVP threshold the LV52207NXB's switching converter stops switching.

Over Current Protection

Current limit value for built-in power MOS is around 1.5 A. The power MOS is turned off for each switching cycle when peak drain current exceeds the limit value.

Under Voltage Lock Out (UVLO)

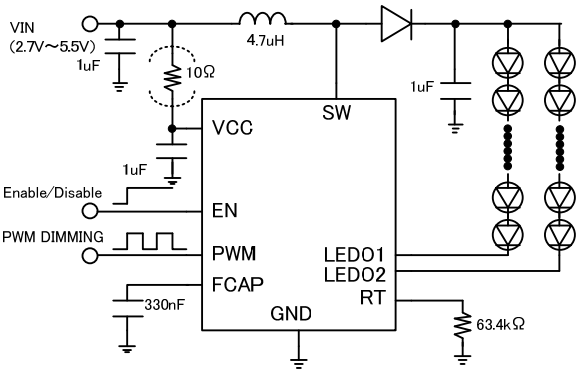
UVLO operation works when VIN terminal voltage is below 2.2 V.

Thermal Shutdown

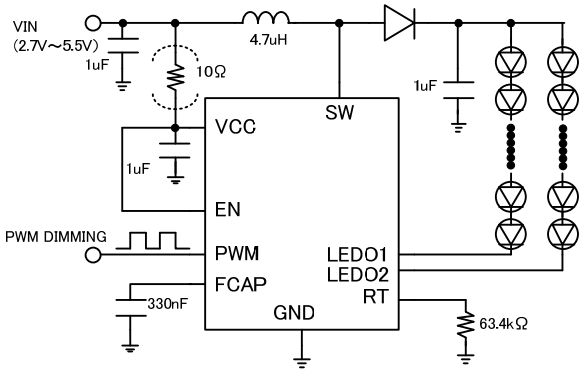
When chip temperature is too high, boost converter is stopped.

Application Circuit Diagram

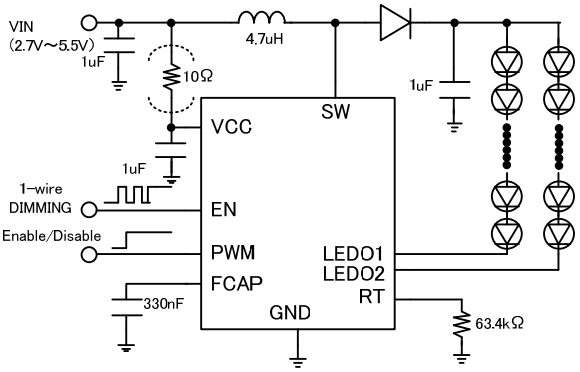
PWM dimming mode
EN pin can be used to enable or disable



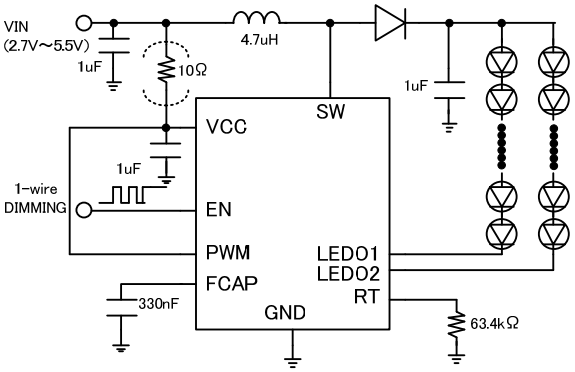
PWM dimming mode
PWM pin can be used to enable or disable



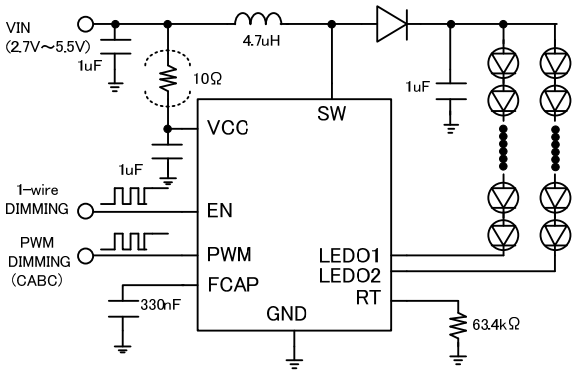
1-wire dimming mode
PWM pin can be used to enable or disable



1-wire dimming mode
EN pin can be used to enable or disable



1-wire dimming mode and PWM dimming mode (CABC)

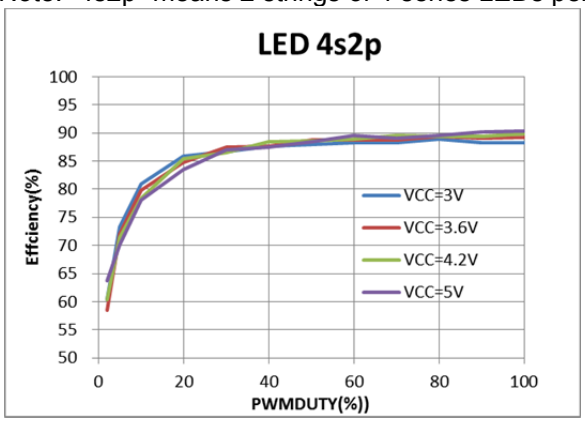


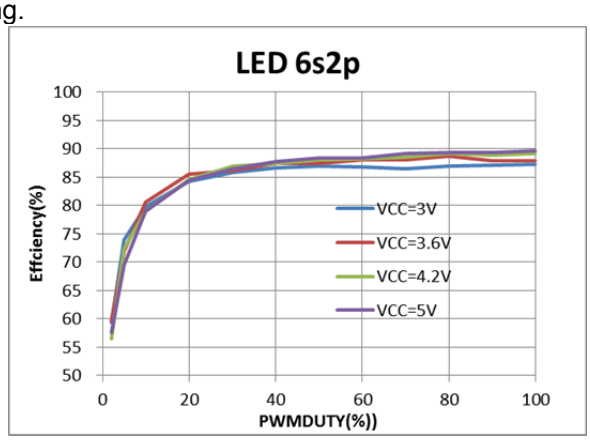
Note: **Start-up Sequence**
During Tw0 period of 1-wire, it is necessary to hold PWM "High".

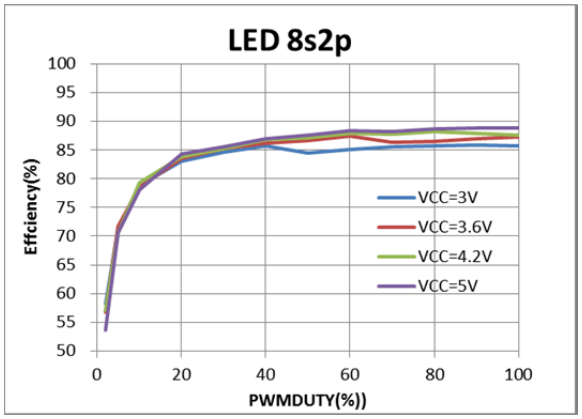
Fig7. Various application circuit diagrams

Typical Characteristics (VIN=3.6 V, L=10 μH, T=25°C, unless otherwise specified)

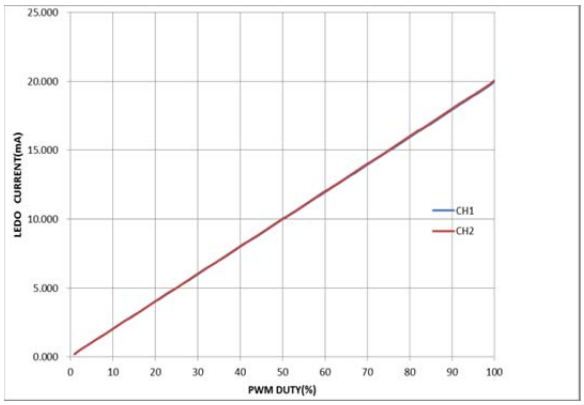
Efficiency vs PWM DIMMING (20 mA/string)
Note: “4s2p” means 2 strings of 4 series LEDs per string.



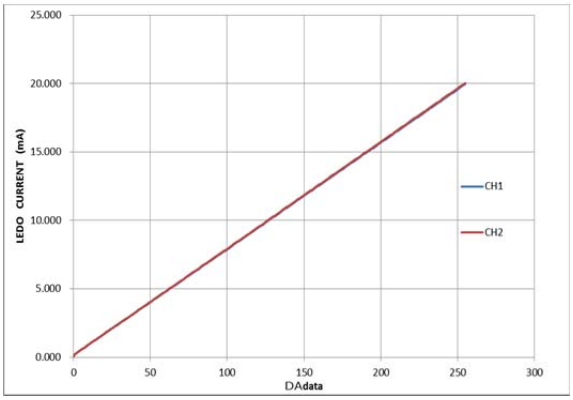




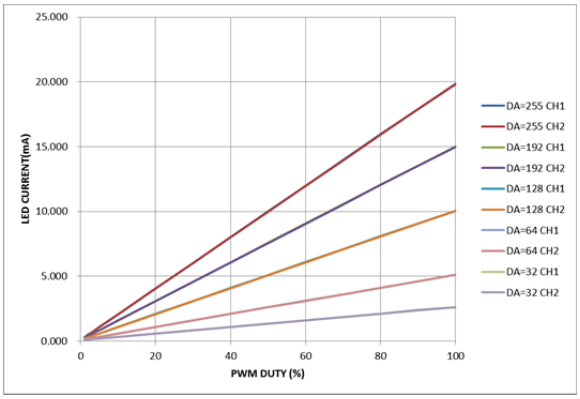
PWM DIMMING



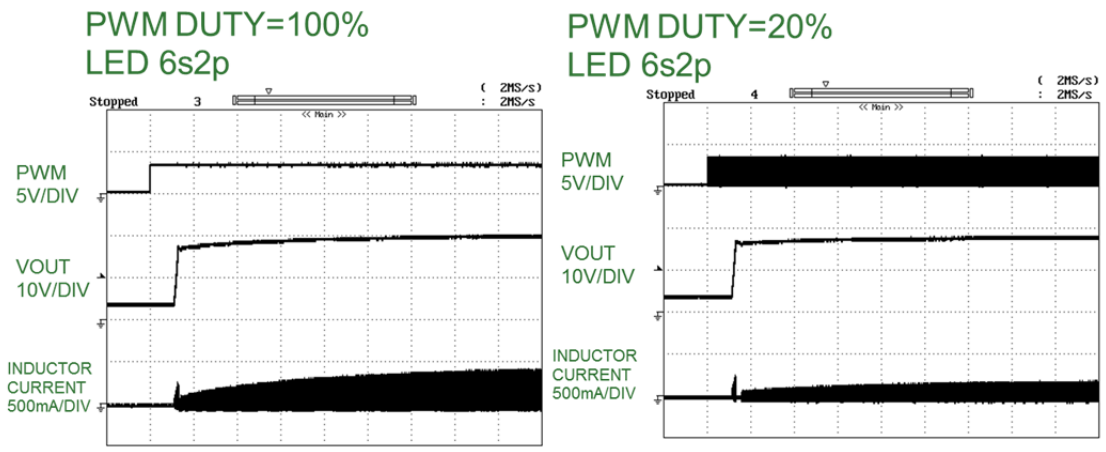
1-wire DIMMING



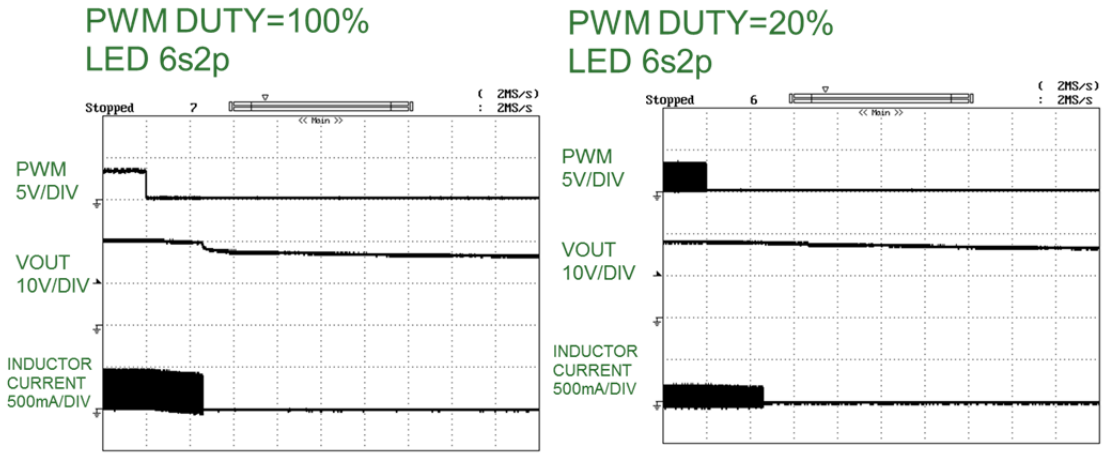
CABC DIMMING



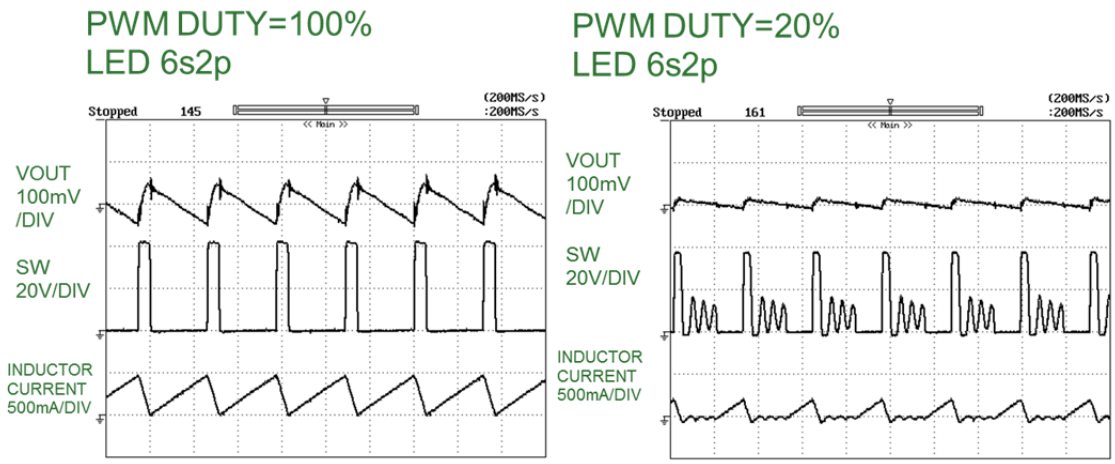
START UP WAVEFORM



SHUTDOWN WAVEFORM



SWITCHING WAVEFORM

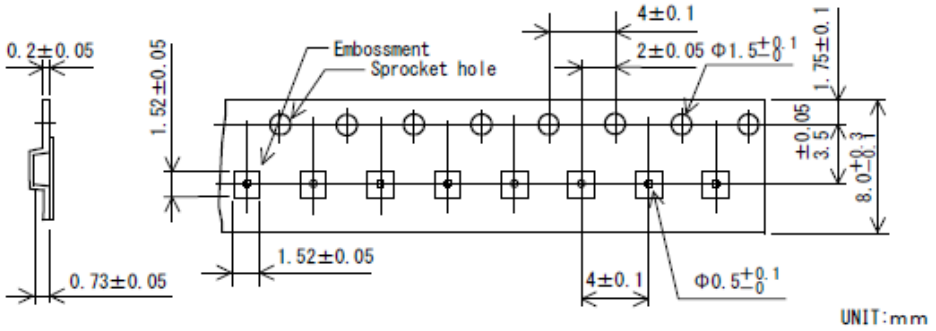


Packing Specification of Embossed Carrier Taping

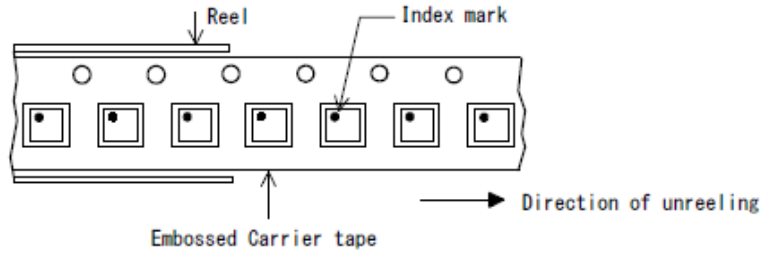
WLP9/9J (1.31×1.31) mm / (1.39 × 1.21) mm

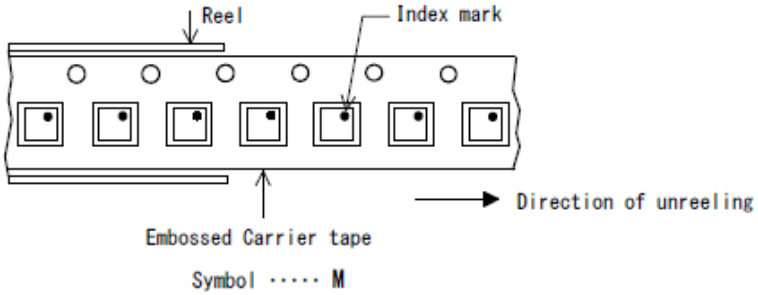
1. EMBOSS CARRIER TAPING

1-1. Emboss carrier tape dimensions

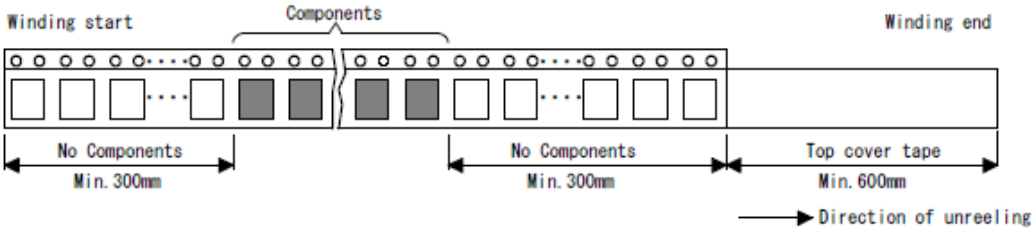


1-2. Tape mounting direction





1-3. Reel winding start and reel winding end



2. TAPE STRENGTH

2-1. Tensile strength of the carrier tape : Min. 10N

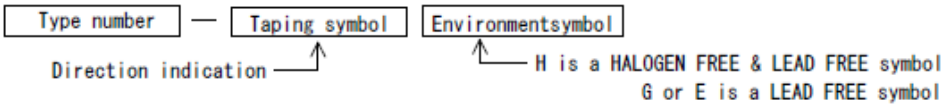
2-2. Peel strength of the top cover tape

(a) Peel angle: 165° to 180° relative to the tape adhesive surface

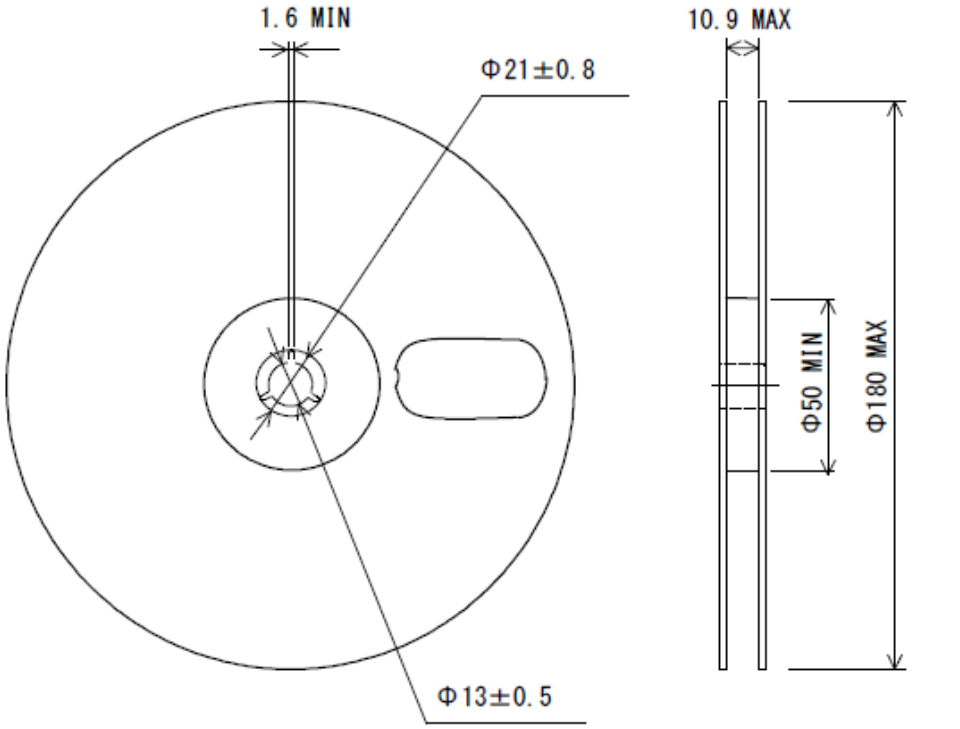
(b) Peel rate: 300mm / minute

(c) Peel of strength : 0.1N to 1.0N

3. PARTS No. ON BAR CODE LABEL



4. REEL DIMENSIONS

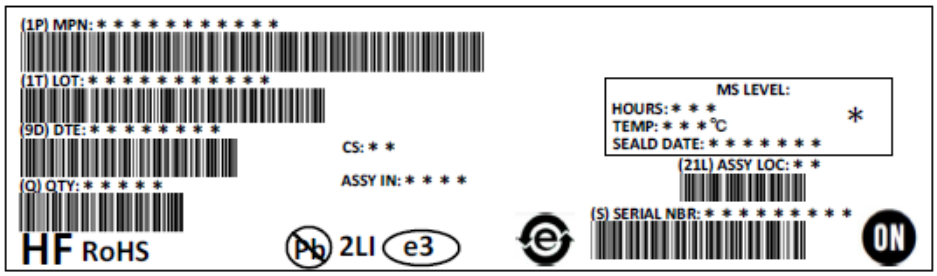


MODEL : RRM-08B

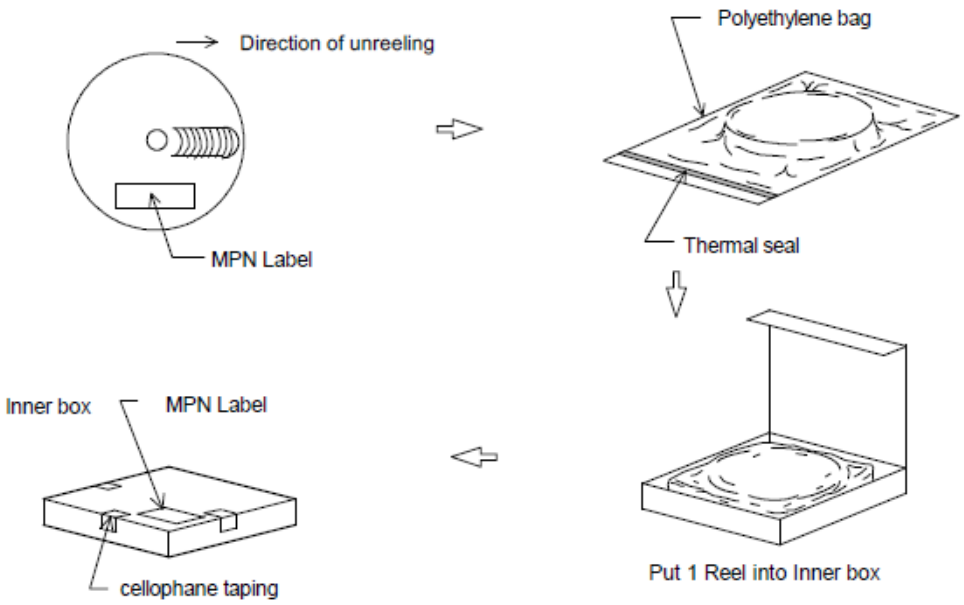
UNIT : mm

Carrier tape type number	Package code	Maximum number of ICs contained (pcs.)		Packing form
		Reel	Inner box	Inner box. BOX(TE-1208)
CARR(BD0145X0145)	WLP9/9J(1.31X1.31) WLP9 (1.39X1.21)	5,000	5,000	1 Reels contained Dimensions:mm 190×37×190

MPN Label



Packing Method



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