12-Bit Digital Pre-Distortion µModule Receiver Subsystem

FEATURES

- **Fully Integrated Receiver Subsystem for Digital Pre-Distortion Applications**
- **Down-Converting Mixer with Wide RF Frequency Range: 400MHz to 3.8GHz**
- **125MHz Wide Bandpass Filter, <0.5dB Passband Ripple**
- **Low Power ADC with Up to 12-Bit Resolution, 250Msps Sample Rate**
- **–145.5dBm/Hz Input Noise Floor, 25.6dBm IIP3**
- 1.5W Total Power Consumption
- 50Ω Single-Ended RF and LO Ports
- Internal Bypass Capacitance, No External Components
- ADC Clock Duty Cycle Stabilizer
- 11.25mm × 15mm LGA package

APPLICATIONS

- Transmit Observation Path Receivers
- Digital Pre-Distortion (DPD) Receivers
- Wideband Receiver
- Wideband Instrumentation

DESCRIPTION

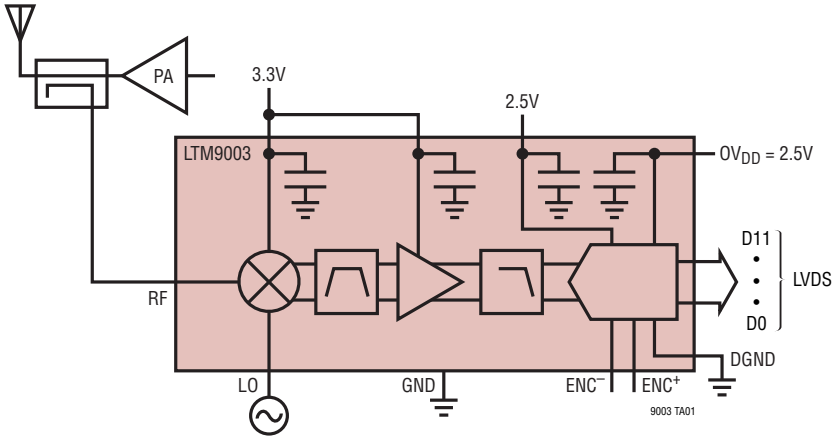
The LTM®9003 is a 12-bit digital pre-distortion µModule® receiver subsystem for the transmit path of cellular basestations. Utilizing an integrated system in a package (SiP) technology, it includes a downconverting mixer, wideband filter and analog-to-digital converter (ADC). The system is tuned for an intermediate frequency (IF) of 184MHz and a signal bandwidth of up to 125MHz. The 12-bit ADC samples at rates up to 250Msps. Contact Linear Technology regarding customization.

The high signal level downconverting active mixer is optimized for high linearity, wide dynamic range IF sampling applications. It includes a differential LO buffer amplifier driving a double-balanced mixer. Broadband, integrated transformers on the RF and LO inputs provide single ended 50Ω interfaces. The RF and LO inputs are internally matched to 50Ω from 1.1GHz to 1.8GHz.

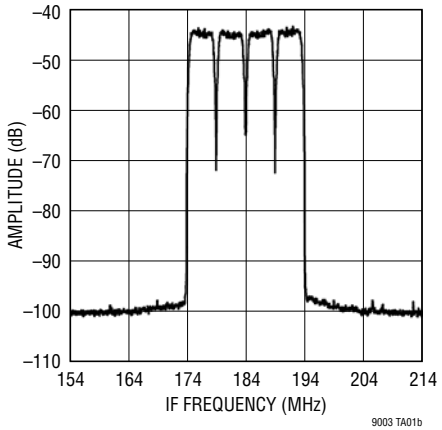
The CLK input controls converter operation and may be driven differentially or single-ended. An optional clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

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TYPICAL APPLICATION



FFT of 4-Channel WCDMA Input at 2.14GHz



ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

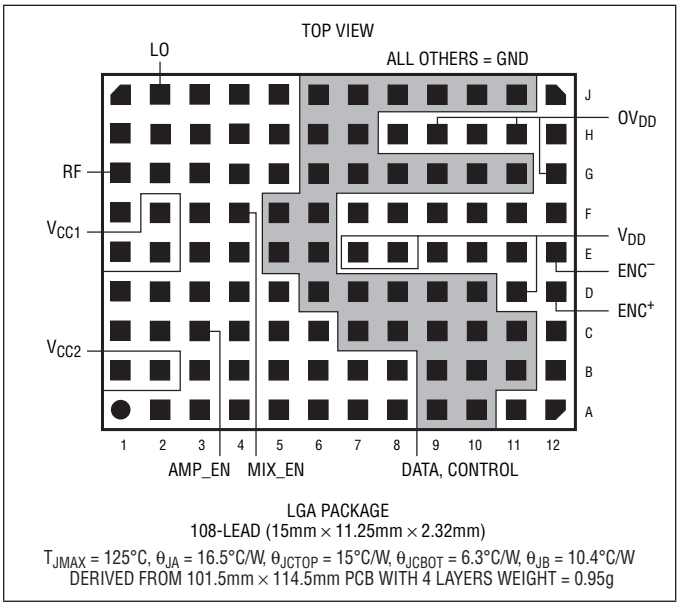
Supply Voltage (V_{CC1})
- LTM9003-AA ..... –0.3V to 4V
- LTM9003-AB ..... –0.3V to 5.5V

Supply Voltage (V_{CC2}) ..... –03V to 5.5V
Supply Voltage (V_{DD}, OV_{DD}) ..... –0.3V to 2.8V
Digital Output Ground Voltage (OGND) ..... –0.3V to 1V
LO Input Power (380MHz to 4.2GHz) 10dBm
LO Input DC Voltage ..... –1V to (V_{CC1} + 1V)
RF Input Power (400MHz to 3.8GHz) 15dBm
RF Input DC Voltage ..... ±0.1V
MIX_EN Voltage ..... –0.3V to (V_{CC1} + 0.3V)
AMP_EN Input Current ..... ±10mA
Digital Input Voltage ..... –0.3V to (V_{DD} + 0.3V)
Digital Output Voltage ..... –0.3V to (OV_{DD} + 0.3V)
Operating Ambient Temperature Range
- LTM9003CV ..... 0°C to 70°C
- LTM9003IV ..... –40°C to 85°C

Storage Temperature Range ..... –40°C to 125°C
Maximum Junction Temperature ..... 125°C

CAUTION: The RF and LO inputs are sensitive to electrostatic discharge (ESD). It is very important that proper ESD precautions be observed when handling the LTM9003.

PIN CONFIGURATION



LGA PACKAGE
108-LEAD (15mm × 11.25mm × 2.32mm)

T_{JMAX} = 125°C, θ_{JA} = 16.5°C/W, θ_{JCTOP} = 15°C/W, θ_{JCBOT} = 6.3°C/W, θ_{JB} = 10.4°C/W
DERIVED FROM 101.5mm × 114.5mm PCB WITH 4 LAYERS WEIGHT = 0.95g

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM9003CV-AA#PBF	LTM9003CV-AA#PBF	LTM9003V AA	108-Lead (11.25mm × 15mm × 2.3mm) LGA	0°C to 70°C
LTM9003IV-AA#PBF	LTM9003IV-AA#PBF	LTM9003V AA	108-Lead (11.25mm × 15mm × 2.3mm) LGA	–40°C to 85°C
LTM9003CV-AB#PBF	LTM9003CV-AB#PBF	LTM9003V AB	108-Lead (11.25mm × 15mm × 2.3mm) LGA	0°C to 70°C
LTM9003IV-AB#PBF	LTM9003IV-AB#PBF	LTM9003V AB	108-Lead (11.25mm × 15mm × 2.3mm) LGA	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF Input Frequency Range	LTM9003-AA No External Matching (Midband) With External Matching (Low Band or High Band)		 400	 1100 to 1800 	 3800	 MHz MHz
	LTM9003-AB No External Matching (Midband) With External Matching (Low Band or High Band)		 400	 1100 to 1800 	 3700	 MHz MHz
LO Input Frequency Range	LTM9003-AA No External Matching With External Matching		 380	 800 to 3500 	 	 MHz MHz
	LTM9003-AB No External Matching With External Matching		 380	 900 to 3500 	 	 MHz MHz
RF Input Return Loss	Z_O = 50Ω, 1100MHz to 1800MHz (No External Matching) LTM9003-AA LTM9003-AB		 	 >12 >12	 	 dB dB
LO Input Return Loss	Z_O = 50Ω, 900MHz to 3500MHz (No External Matching) LTM9003-AA LTM9003-AB		 	 >10 >10	 	 dB dB
RF Input Power for –1dBFS	LTM9003-AA LTM9003-AB		 	 –1.7 –1.7	 	 dBm dBm
LO Input Power	1200MHz to 4200MHz, LTM9003-AA or 1200MHz to 3500MHz, LTM9003-AB 380MHz to 1200MHz		 –8 –5	 –3 0	 2 5	 dBm dBm
LO to RF Leakage	LTM9003-AA f_{LO} = 380MHz to 1600MHz f_{LO} = 1600MHz to 4000MHz		 	 <–50 <–45	 	 dBm dBm
	LTM9003-AB f_{LO} = 400MHz to 2100MHz f_{LO} = 2100MHz to 3200MHz		 	 <–44 <–36	 	 dBm dBm
RF to LO Isolation	LTM9003-AA f_{RF} = 400MHz to 1700MHz f_{RF} = 1700MHz to 3800MHz		 	 >50 >42	 	 dB dB
	LTM9003-AB f_{RF} = 400MHz to 2200MHz f_{RF} = 2200MHz to 3700MHz		 	 >43 >38	 	 dB dB

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error (Note 4)	IF = 184.32MHz			±1		LSB
Differential Linearity Error	IF = 184.32MHz			±0.4		LSB

FILTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency				184.32		MHz
Lower 3dB Bandedge				84		MHz
Upper 3dB Bandedge				304		MHz
Lower 20dB Stopband				40		MHz
Upper 20dB Stopband				450		MHz
Passband Flatness	129MHz to 239.6MHz 174MHz to 194MHz			0.5 0.15		dB dB
Group Delay Flatness	129MHz to 239.6MHz 174MHz to 194MHz			1.2 0.1		ns ns
Absolute Delay				2.7		ns

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio at –1dBFS	RF = 1889MHz, LO = 1766MHz RF = 1950MHz, LO = 1766MHz RF = 2011MHz, LO = 1766MHz	 ● 	 141 	143.6 143.6 143.6		dB/Hz dB/Hz dB/Hz
IIP3	Input 3rd Order Intercept, 2-Tone	LTM9003-AA RF = 1948MHz, 1952MHz, LO = 1766MHz			27		dBm
		LTM9003-AB RF = 1948MHz, 1952MHz, LO = 1766MHz			28		dBm
IIP2	Input 2nd Order Intercept, 1-Tone	LTM9003-AA RF = 1950MHz, LO = 1766MHz			61		dBm
		LTM9003-AB RF = 1950MHz, LO = 1766MHz			61.4		dBm
SFDR	Spurious Free Dynamic Range, 2nd or 3rd Harmonic at –1dBFS	LTM9003-AA RF = 1889MHz, LO = 1766MHz RF = 1950MHz, LO = 1766MHz RF = 2011MHz, LO = 1766MHz	 ● 	 50.7 	 54.1 58.8 63.6		 dB dB dB
		LTM9003-AB RF = 1889MHz, LO = 1766MHz RF = 1950MHz, LO = 1766MHz RF = 2011MHz, LO = 1766MHz	 ● 	 52.0 	 57.3 62.4 66.3		 dB dB dB
SFDR	Spurious Free Dynamic Range, 4th or Higher at –1dBFS	RF = 1889MHz, LO = 1766MHz RF = 1950MHz, LO = 1766MHz RF = 2011MHz, LO = 1766MHz	 ● 	 66.5 	74 82 87		dB dB dB
S/(N+D)	Signal-to-Noise Plus Distortion Ratio at –1dBFS	RF = 1889MHz, LO = 1766MHz RF = 1950MHz, LO = 1766MHz RF = 2011MHz, LO = 1766MHz	 ● 	 50.3 	54 58 60		dB dB dB
IMD3	Intermodulation Distortion at –7dBFS per Tone	RF = 1950MHz, LO = 1766MHz			–58		dB
ACPR	Adjacent Channel Power Ratio at 2.4dBm per Carrier, Four Carriers				58.5		dB
ALTCPR	Alternate Channel Power Ratio at 2.4dBm per Carrier, Four Carriers				63.3		dB

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Encode Inputs (ENC⁻, ENC⁺)							
V_{ID}	Differential Input Voltage	(Note 5)		0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 5)	 ●	 1.2	1.5 1.5	 2	V V
R_{IN}	Input Resistance	Single-Ended			4.8		Ω
$R_{IN(DIFF)}$	Input Resistance	Differential			100		Ω
C_{IN}	Input Capacitance				2		pF
Logic Inputs ($\overline{OE}$, SHDN)							
V_{IH}	High Level Input Voltage	V_{DD} = 2.5V	●	1.7			V
V_{IL}	Low Level Input Voltage	V_{DD} = 2.5V	●			0.7	V
I_{IN}	Input Current	V_{IN} = 0V to V_{DD}	●	–10		10	µA
C_{IN}	Input Capacitance	(Note 5)				3	pF
Mixer Enable							
V_{IH}	High Level Input Voltage	V_{CC1} = 3.3V, LTM9003-AA V_{CC1} = 5V, LTM9003-AB	● ●	2.7 3			V V
V_{IL}	Low Level Input Voltage	V_{CC1} = 3.3V, LTM9003-AA V_{CC1} = 5V, LTM9003-AB	● ●			0.3 0.3	V V
I_{IN}	Input Current	V_{IN} = 0V to V_{CC1}, LTM9003-AA	●		53	90	µA
	Turn-On Time				2.8		ms
	Turn-Off Time				2.9		ms
Amplifier Enable							
V_{IH}	High Level Input Voltage	V_{CC2} = 3.3V	●	2			V
V_{IL}	Low Level Input Voltage	V_{CC2} = 3.3V	●			0.8	V
I_{IN}	Input Current	V_{IN} = 0.8V V_{IN} = 2V	● ●	–200 –150	–85 –30	0 0	µA µA
Control Inputs (SENSE, MODE, LVDS)							
I_{SENSE}	SENSE Input Leakage	0V < SENSE < 1V	●	–1		1	µA
I_{MODE}	MODE Pull-Down Current to GND	See Pin Functions for Voltage Levels			7		µA
I_{LVDS}	LVDS Pull-Down Current to GND	See Pin Functions for Voltage Levels			7		µA
Logic Outputs (LVDS Mode)							
OV_{DD} = 2.5V							
V_{OD}	Differential Output Voltage	100Ω Differential Load	●	247	350	454	mV
V_{OS}	Output Common Mode Voltage	100Ω Differential Load	●	1.125	1.250	1.375	V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC1}	Mixer Supply Range	LTM9003-AA (Note 6) LTM9003-AB (Note 6)	● ●	2.9 4.5	3.3 5	3.6 5.25	V V
V_{CC2}	Amplifier Supply Range	(Note 6)	●	2.8	3.3	5.25	V
V_{DD}	ADC Analog Supply Voltage	(Note 6)	●	2.375	2.5	2.625	V
I_{CC1}	Mixer Supply Current	MIX_EN = 3V, LTM9003-AA MIX_EN = 5V, LTM9003-AB	●		80 82	92 92	mA mA
$I_{CC1(SHDN)}$	Mixer Shutdown Supply Current	MIX_EN = 0V	●			100	µA
I_{CC2}	Amplifier Supply Current	AMP_EN = 3V	●		104	140	mA
$I_{CC2(SHDN)}$	Amplifier Shutdown Supply Current	AMP_EN = 0V	●		3	5	mA
$I_{DD(ADC)}$	ADC Supply Current		●		285	320	mA
$P_{D(SHDN)}$	ADC Shutdown Power	SHDN = V_{DD}, $\overline{OE}$ = V_{DD}, No CLK			1.5		mW
$P_{D(NAP)}$	ADC Nap Mode Power	SHDN = V_{DD}, $\overline{OE}$ = 0V, No CLK			30		mW
LVDS Output Mode							
OV_{DD}	ADC Digital Output Supply Voltage		●	2.375	2.5	2.625	V
$I_{OVDD(ADC)}$	ADC Digital Output Supply Current		●		58	74	mA
$P_{D(ADC)}$	ADC Power Dissipation		●		858	985	mW
$P_{D(TOTAL)}$	Total Power Dissipation	SHDN = 0V, MIX_EN = AMP_EN = 3V, f_{SAMPLE} = MAX (LTM9003-AA) (LTM9003-AB)			 1465 1611		 mW mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_s	Sampling Frequency	(Note 6)	●	1		250	MHz
t_L	ENC Low Time	Duty Cycle Stabilizer Off (Note 5) Duty Cycle Stabilizer On (Note 5)	● ●	1.9 1.5	2 2	500 500	ns ns
t_H	ENC High Time	Duty Cycle Stabilizer Off (Note 5) Duty Cycle Stabilizer On (Note 5)	● ●	1.9 1.5	2 2	500 500	ns ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Time Jitter				95		fs_{RMS}
t_{AP}	Sample-and-Hold Aperture Delay				0		ns
$t_{\overline{OE}}$	Output Enable Delay	(Note 5)	●		5	10	ns
LVDS Output Mode							
t_D	ENC to DATA delay	(Note 5)	●	1	1.7	2.8	ns
t_C	ENC to CLKOUT Delay	(Note 5)	●	1	1.7	2.8	ns
	DATA to CLKOUT Skew	(t_C – t_D) (Note 5)	●	–0.6	0	0.6	ns
	Rise Time				0.5		ns
	Fall Time				0.5		ns
	Pipeline Latency				5		Cycles

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with GND and OGND wired together (unless otherwise noted).

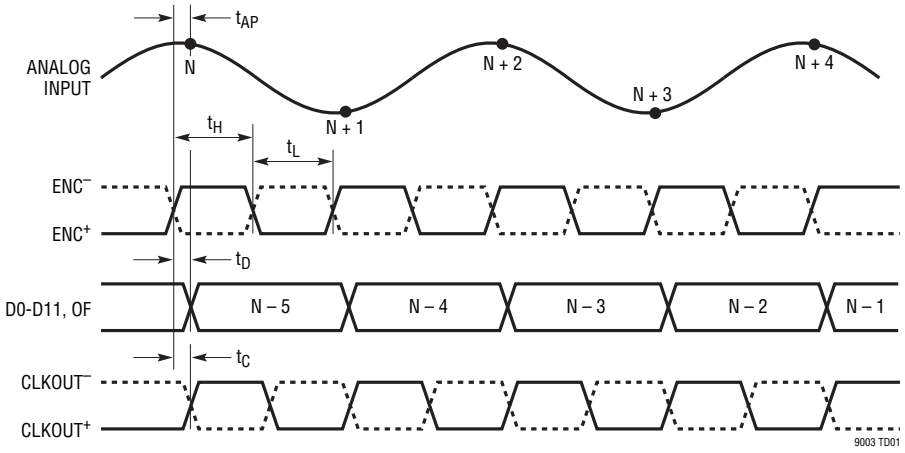
Note 3: V_{CC1} = V_{CC2} = 3.3V (LTM9003-AA) or V_{CC1} = 5V, V_{CC2} = 3.3V (LTM9003-AB), V_{DD} = 2.5V, OV_{DD} = 2.5V, f_{SAMPLE} = 250MHz, input range = –1dBFS, differential ENC^+/ENC^- = $2V_{P-P}$ sine wave, unless otherwise noted.

Note 4: Integral nonlinearity is defined as the deviation of a code from a "best straight line" fit to the transfer curve. The deviation is measured from the center of the quantization band.

Note 5: Guaranteed by design, not subject to test.

Note 6: Recommended operating conditions.

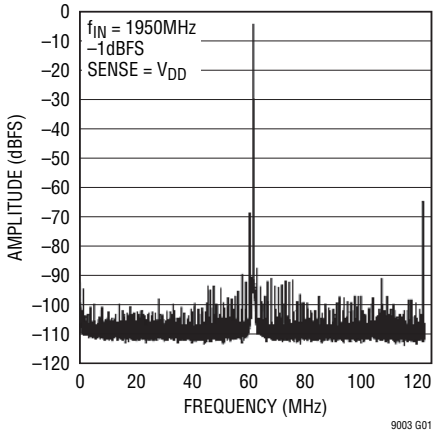
TIMING DIAGRAM



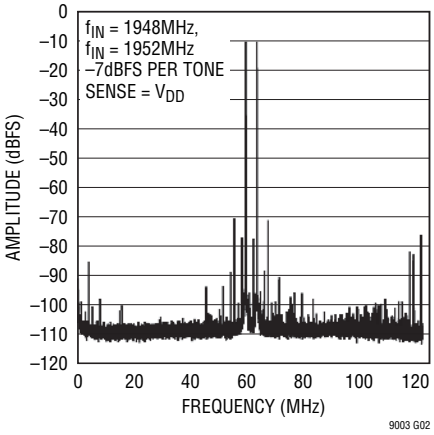
LVDS Output Mode Timing
All Outputs Are Differential and Have LVDS Levels

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C.

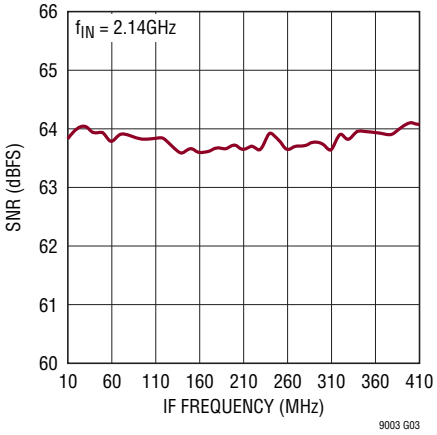
64k Point FFT, LTM9003-AA



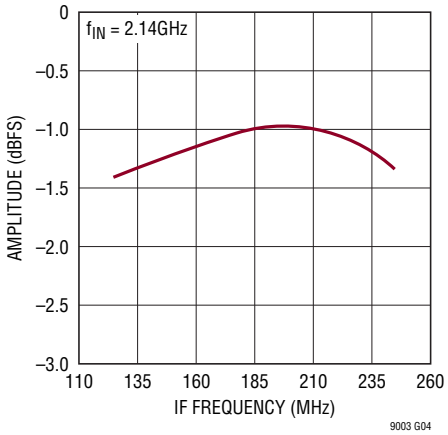
64k Point 2-Tone FFT, LTM9003-AA



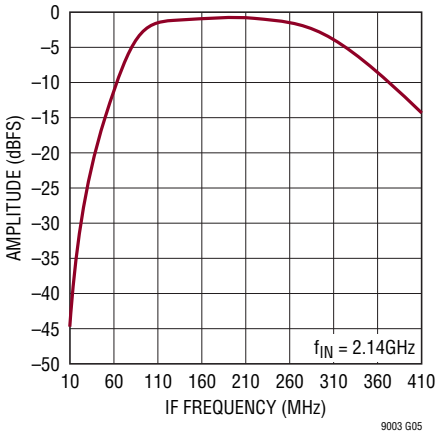
SNR vs Frequency, LTM9003-AA



IF Frequency Response, LTM9003-AA

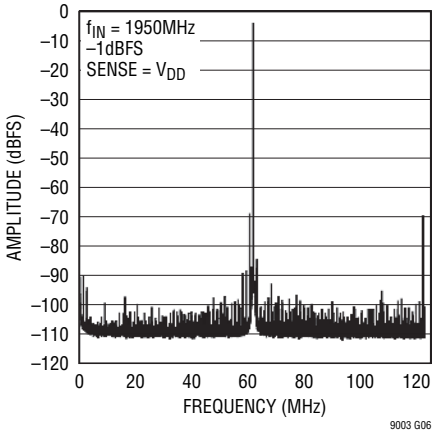


IF Frequency Response, LTM9003-AA

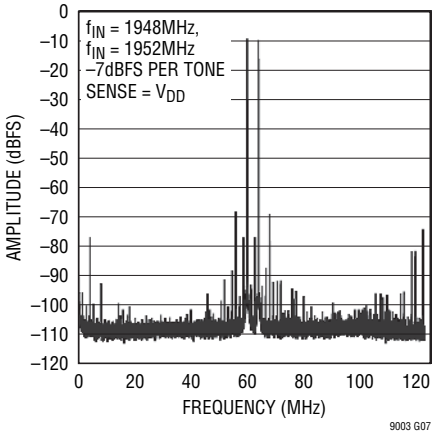


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C.

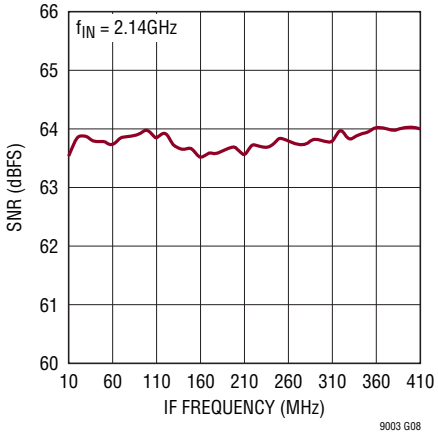
64k Point FFT, LTM9003-AB



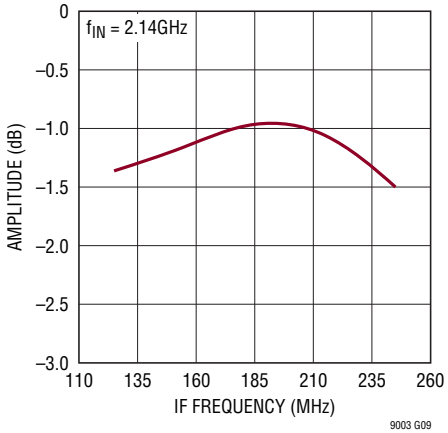
64k Point 2-Tone FFT, LTM9003-AB



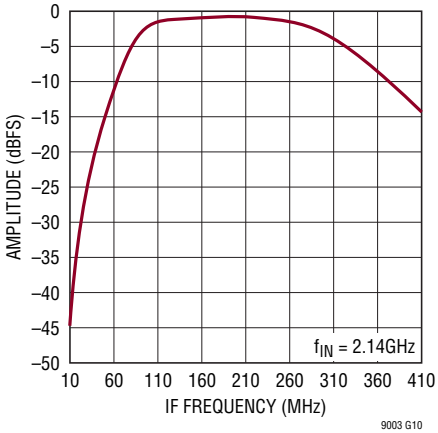
SNR vs Frequency, LTM9003-AB



IF Frequency Response, LTM9003-AB



IF Frequency Response, LTM9003-AB



PIN FUNCTIONS

V_{CC1} (Pins E1, E2, F2): 3.3V (LTM9003-AA) or 5V (LTM9003-AB) Supply Voltage for the Mixer. V_{CC1} is internally bypassed to GND.

V_{CC2} (Pins B1, B2): 3.3V Supply Voltage for the Amplifier. V_{CC2} is internally bypassed to GND.

V_{DD} (Pins D11, E7, E8): 2.5V Supply Voltage for ADC. V_{DD} is internally bypassed to GND.

OV_{DD} (Pins G12, H9, H11): 2.5V Supply for the Output Drivers. OV_{DD} is internally bypassed to OGND.

GND (See Table for Locations): Module Ground.

OGND (Pins F12, H8, H10, H12, J12): Output Driver Ground.

RF (Pin G1): Single-Ended Input for the RF Signal. This pin is internally connected to the primary side of the RF input transformer, which has low DC resistance to ground. If the RF source is not DC blocked, then a series blocking capacitor must be used. The RF input is internally matched from 1.1GHz to 1.8GHz. Operation down to 400MHz or up to 3.8GHz is possible with simple external matching.

LO (Pin J2): Single-Ended Input for the Local Oscillator Signal. This pin is internally connected to the primary side of the LO transformer, which is internally DC blocked. An external blocking capacitor is not required. The LO input is internally matched from 0.9GHz to 3.5GHz. Operation down to 380MHz is possible with simple external matching.

MIX_EN (Pin F4): Mixer Enable Pin. Connecting MIX_EN to V_{CC1} results in normal operation. Connecting MIX_EN to GND disables the mixer. The MIX_EN pin should not be left floating.

AMP_EN (Pin C3): Amplifier Enable Pin. This pin is internally pulled high by a typically 30k resistor to V_{CC2}. Connecting AMP_EN to V_{CC2} results in normal operation. Connecting AMP_EN to GND disables the amplifier.

ENC^+ (Pin D12): ADC Encode Input. Conversion starts on the positive edge.

ENC^- (Pin E12): ADC Encode Complement Input. Conversion starts on the negative edge. Bypass to ground with 0.1µF ceramic for single-ended ENCODE signal.

SHDN (Pin B11): ADC Shutdown Mode Selection Pin. Connecting SHDN to GND and $\overline{OE}$ to GND results in normal operation with the outputs enabled. Connecting SHDN to GND and $\overline{OE}$ to V_{DD} results in normal operation with the outputs at high impedance. Connecting SHDN to V_{DD} and $\overline{OE}$ to GND results in nap mode with the outputs at high impedance. Connecting SHDN to V_{DD} and $\overline{OE}$ to V_{DD} results in sleep mode with the outputs at high impedance.

$\overline{OE}$ (Pin C11): Output Enable Pin. Refer to SHDN pin function.

MODE (Pin C7): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to GND selects offset binary output format and turns the clock duty cycle stabilizer off. 1/3 V_{DD} selects offset binary output format and turns the clock duty cycle stabilizer on. 2/3 V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer on. V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer off.

SENSE (Pin G7): Reference Programming Pin. Connecting SENSE to 1.25V selects the internal reference and a ±0.5V input range. V_{DD} selects the internal reference and a ±1V input range. An external reference greater than 0.5V and less than 1V applied to SENSE selects an input range of $\pm V_{SENSE}$. ±1V is the largest valid input range.

LVDS (Pin D7): Output Mode Selection Pin. Connect LVDS to V_{DD}.

Digital Outputs

$D0^-/D0^+$ – $D11^-/D11^+$ (See Table for Locations): LVDS Digital Outputs. All LVDS outputs require differential 100Ω termination resistors at the LVDS receiver. $D11^-/D11^+$ is the MSB.

$CLKOUT^-/CLKOUT^+$ (Pins J10/J11): LVDS Data Valid Output. Latch data on rising edge of $CLKOUT^-$, falling edge of $CLKOUT^+$.

OF^-/OF^+ (Pins E5/F5): LVDS Over/Under Flow Output. High when an over or under flow has occurred.

PIN FUNCTIONS

Pin Configuration

J	GND	LO	GND	GND	GND	D9+	D8–	D6+	D6–	CLKOUT+	CLKOUT–	OGND
H	GND	GND	GND	GND	GND	D9–	D8+	OGND	OV_{DD}	OGND	OV_{DD}	OGND
G	RF	GND	GND	GND	GND	D10–	SENSE	D7+	D7–	D5+	D5–	OV_{DD}
F	GND	V_{CC1}	GND	MIX_EN	OFP	D10+	GND	GND	GND	GND	GND	OGND
E	V_{CC1}	V_{CC1}	GND	GND	OFN	D11–	V_{DD}	V_{DD}	GND	GND	GND	ENC^-
D	GND	GND	GND	GND	GND	D11+	LVDS	D4+	D3+	D1+	V_{DD}	ENC^+
C	GND	GND	AMP_EN	GND	GND	GND	MODE	D4–	D3–	D1–	$\overline{OE}$	GND
B	V_{CC2}	V_{CC2}	GND	GND	GND	GND	GND	GND	D2+	D0+	SHDN	GND
A	GND	GND	GND	GND	GND	GND	GND	GND	D2–	D0–	GND	GND
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**

Top View of LGA Package (Looking Through Component)

BLOCK DIAGRAM

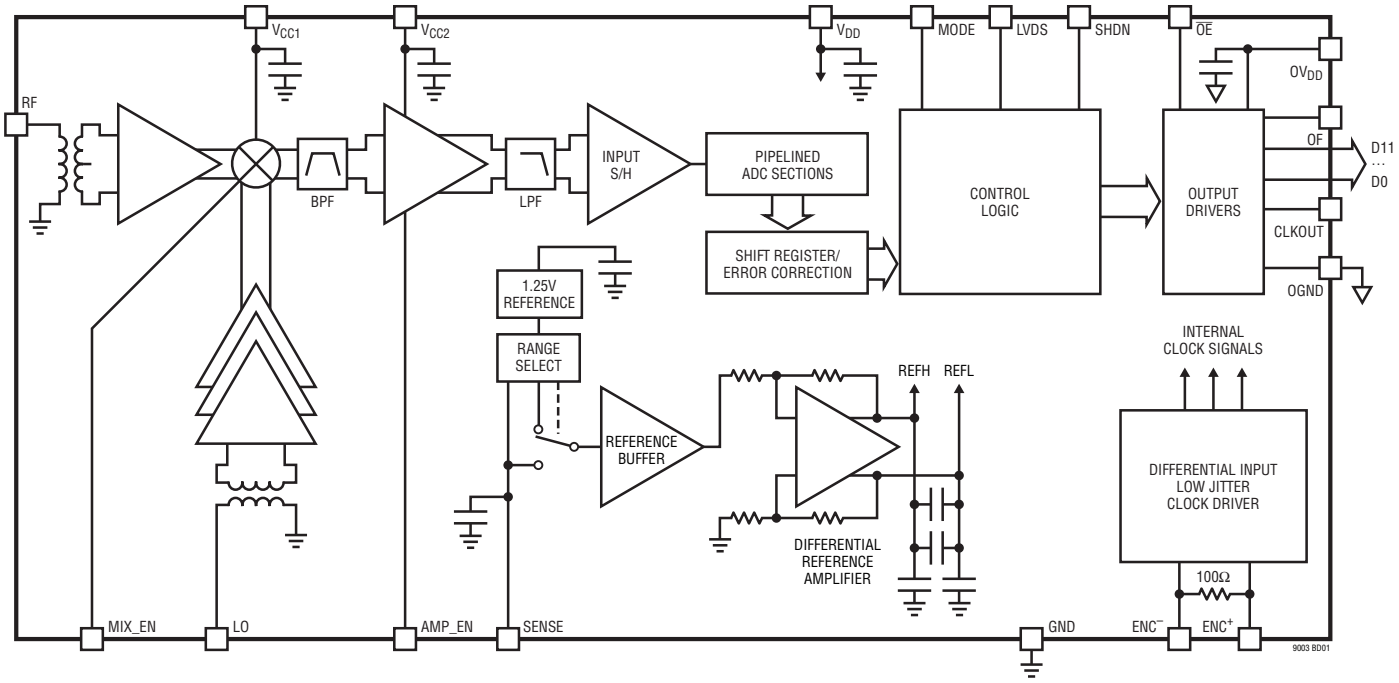


Figure 1. Simplified Block Diagram

OPERATION

DESCRIPTION

The LTM9003 is an integrated system in a package (SiP) that includes a high-speed 12-bit A/D converter, a wideband filter and an active mixer. The LTM9003 is designed for IF sampling, digital pre-distortion (DPD) applications, also known as transmit observation path receivers, with RF input frequencies up to 3.8GHz. Typical applications include multi-carrier base stations and telecom test instrumentation.

Digital pre-distortion is a technique often used in third-generation (3G) wireless base stations to improve the linearity of power amplifiers (PA). Improved PA linearity allows for a lower power PA to be used and therefore save a significant amount of power in the base station. The DPD receiver captures the PA output, digitizes it and feeds it back where the distortion can be analyzed. A complementary distortion is then introduced to the transmit DAC thereby pre-distorting the signal.

A significant factor in PA linearity is the distortion caused by the odd order intermodulation (IM) products. The bandwidth to be digitized is equivalent to the signal bandwidth multiplied by the order of the IM product to be canceled. For example, four carrier WCDMA consumes 20MHz of signal bandwidth; therefore, to capture the fifth order IM product requires 100MHz. The Nyquist theory requires that the ADC sample rate be at least twice that frequency.

However, simply doubling the captured bandwidth to set the sample rate may not be the best choice. Selecting the exact ADC sample rate and intermediate frequency (IF) depends on other factors within the system. To simplify filtering, the sample rate is often set at a multiple of the chip rate. The chip rate for WCDMA is 3.84MHz; selecting an ADC sample rate of 64 times the chip rate gives 245.76Msps. Placing the IF at 3/4ths the sample rate (f_S) gives 184.32MHz and allows the entire bandwidth to fall within the second Nyquist zone. Many other frequency plans may be acceptable.

The following sections describe in further detail the operation of each functional element of the LTM9003. The SiP technology allows the LTM9003 to be customized and this is described in the Semi-Custom Options section. The outline of the remaining sections follows the basic functional elements as shown in Figure 2.

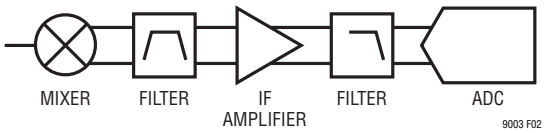


Figure 2. Basic Functional Elements

The mixer dominates the noise figure calculation as would be expected. The overall gain is optimized for the dynamic range of the ADC relative to the RF input level allowed by the mixer. The equivalent cascaded noise figure is 9.1dB (LTM9003-AA) and 9.9dB (LTM9003-AB). The bandpass filter is a second order L-C filter following the mixer and a lowpass filter following the amplifier provides anti-alias and noise limiting.

SEMI-CUSTOM OPTIONS

The µModule construction affords a new level of flexibility in application-specific standard products. Standard ADC and amplifier components can be integrated regardless of their process technology and matched with passive components to a particular application. The LTM9003-AA, as the first example, is configured with a 12-bit ADC sampling at rates up to 250Msps. The total system gain is approximately 10.8dB. The IF is fixed by the bandpass filter at 184MHz with 125MHz bandwidth. The RF range is matched for 1.1GHz to 1.8GHz with low side LO.

However, other options are possible through Linear Technology's semi-custom development program. Linear Technology has in place a program to deliver other speed, resolution, IF range, gain and filter configurations for nearly any specified application. These semi-custom designs are based on existing ADCs and amplifiers with an appropriately modified matching network. The final subsystem is then tested to the exact parameters defined for the application. The final result is a fully integrated, accurately tested and optimized solution in the same package. For more details on the semi-custom receiver subsystem program, contact Linear Technology.

Down-Converting Mixer

The mixer stage consists of a high linearity double-balanced mixer, RF buffer amplifier, high speed limiting LO buffer amplifier and bias/enable circuits. The RF and LO

OPERATION

inputs are both single ended. Low side or high side LO injection can be used.

The mixer's RF input consists of an integrated transformer and a high linearity differential amplifier. The primary terminals of the transformer are connected to the RF input (Pin G1) and ground. The secondary side of the transformer is internally connected to the amplifier's differential inputs.

The mixer's LO input consists of an integrated transformer and high speed limiting differential amplifiers. The amplifiers are designed to precisely drive the mixer for the highest linearity and the lowest noise figure.

Wideband Filter

Most of the IF filtering is done between the mixer and the IF amplifier. This network is a 2nd order Chebychev bandpass section, designed for 0.1dB passband ripple. The 3dB bandwidth is 220MHz, centered at 184MHz, see Figure 3. Additional lowpass filtering is done just before the ADC. This filter serves to bandlimit the out of band noise entering the converter, as well as to isolate the output of the IF amplifier from the sampling action of the converter.

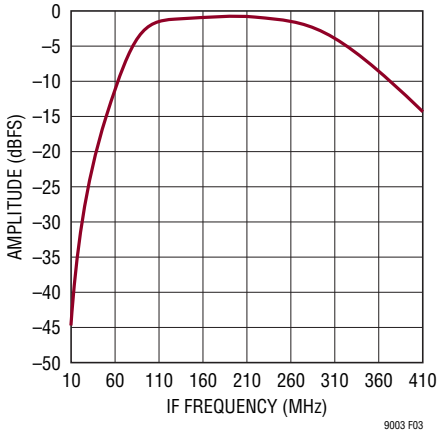


Figure 3. IF Filter Response

Analog to Digital Converter

As shown in Figure 1, the analog-to-digital converter (ADC) is a CMOS pipelined multistep converter. The converter has five pipelined ADC stages; a sampled analog input will result in a digitized value five cycles later (see the Timing Diagram section). The encode input is differential for improved common mode noise immunity. The ADC has two phases of operation, determined by the state of the differential ENC^+/ENC^- input pins. For brevity, the text will refer to ENC^+ greater than ENC^- as ENC high and ENC^+ less than ENC^- as ENC low.

Each pipelined stage shown in Figure 1 contains an ADC, a reconstruction DAC and an interstage residue amplifier. In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when the odd stages are outputting their residue, the even stages are acquiring that residue and visa versa.

When ENC is low, the analog input is sampled differentially directly onto the input sample-and-hold capacitors, inside the "Input S/H" shown in the Block Diagram. At the instant that ENC transitions from low to high, the sampled input is held. While ENC is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H during this high phase of ENC. When ENC goes back low, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When ENC goes back high, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the third and fourth stages, resulting in a fourth stage residue that is sent to the fifth stage ADC for final evaluation.

Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally synchronized such that the results can be properly combined in the correction logic before being sent to the output buffer.

APPLICATIONS INFORMATION

RF Input Port

The mixer's RF input is shown in Figure 4 and is internally matched from 1.1GHz to 1.8GHz, requiring no external components over this frequency range. The input return loss, shown in Figure 5, is typically 12dB at the band edges. The input match at the lower band edge can be optimized with a shunt 3.3pF capacitor at Pin G1, which improves the 0.8GHz return loss to greater than 25dB. Likewise, the 2GHz match can be improved to greater than 25dB with a series 3.9nH inductor and a 1pF shunt capacitor. Measured RF input return losses for these three cases are plotted in Figure 5.

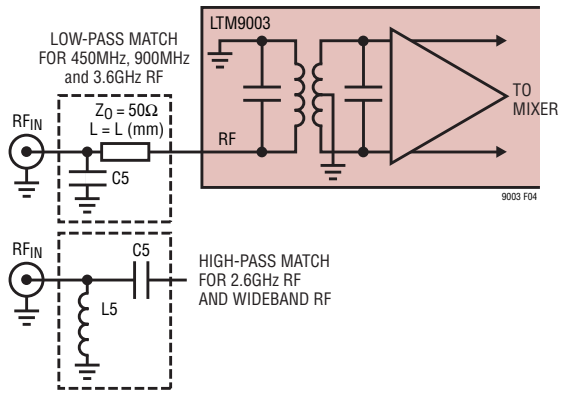


Figure 4. RF Input Schematic

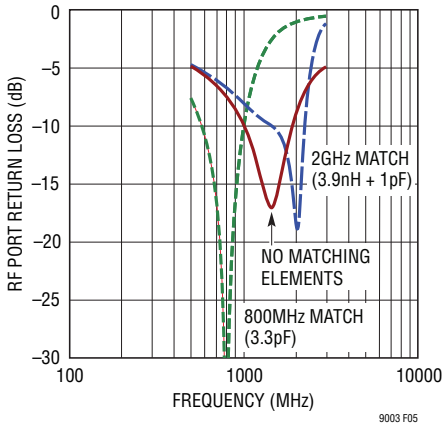


Figure 5. RF Input Return Loss with and without Matching

This series transmission line/shunt capacitor matching topology allows the LTM9003 to be used for multiple frequency standards without circuit board layout modifications. The series transmission line can also be replaced with a series chip inductor for a more compact layout.

RF input impedance and S11 versus frequency (with no external matching) are listed in Table 1 and referenced to Pin G1. The S11 data can be used with a microwave circuit simulator to design custom matching networks and simulate board-level interfacing to the RF input filter.

Table 1a. RF Input Impedance vs Frequency (LTM9003-AA)

FREQUENCY (MHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
500	20.3 + j7	0.57	143
600	23.6 + j6.7	0.53	137.9
700	27.1 + j6.1	0.48	132.7
800	30.8 + j5.3	0.43	127
900	34.9 + j4.2	0.38	120.4
1000	39.4 + j2.9	0.33	112.6
1100	44.6 + j1.4	0.28	102.8
1200	50.1	0.22	89.8
1300	56 – j1	0.17	70.4
1400	61.5 – j1.2	0.14	42.2
1500	66 – j0.3	0.14	6.6
1600	68.7 + j1.4	0.17	–21.5
1700	69 + j3.2	0.22	–41
1800	67.5 + j4.5	0.27	–54
1900	64.3 + j4.7	0.32	–64.3
2000	60.8 + j4.1	0.36	–72.2
2100	56.7 + j2.8	0.4	–79.5
2200	52.7 + j1.2	0.43	–85.8
2300	48.6 – j0.6	0.46	–92.1
2400	44.7 – j2.3	0.48	–98
2500	40.8 – j4	0.5	–104.3
2600	37 – j5.3	0.51	–110.5
2700	33.1 – j6.3	0.52	–117.2
2800	29.4 – j6.9	0.53	–124.3
2900	26 – j7	0.53	–131.7
3000	22.9 – j6.7	0.53	–139.6

APPLICATIONS INFORMATION

Table 1b. RF Input Impedance vs Frequency (LTM9003-AB)

FREQUENCY (MHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
500	19.8 + j7.3	0.59	143
600	22.7 + j7	0.55	138.4
700	25.7 + j6.6	0.51	133.9
800	28.8 + j5.9	0.47	129.2
900	32.3 + j5.1	0.42	123.9
1000	36.1 + j3.9	0.38	117.9
1100	40.5 + j2.6	0.32	110.6
1200	45.4 + j1.1	0.26	101.3
1300	50.8 – j0.2	0.2	87.6
1400	56.3 – j0.9	0.15	65.6
1500	61.4 – j0.7	0.12	27.5
1600	65.3 + j0.5	0.14	–13.1
1700	67.4 + j2.4	0.19	–37.9
1800	67.3 + j4.1	0.25	–52.4
1900	65.7 + j5.1	0.31	–61.9
2000	63.2 + j5.2	0.37	–68.9
2100	60.4 + j4.7	0.42	–74.4
2200	57.6 + j3.7	0.46	–79.1
2300	55 + j2.6	0.49	–83
2400	52.4 + j1.3	0.51	–86.7
2500	49.9	0.53	–90.1
2600	47.4 – j1.4	0.54	–93.7
2700	44.8 – j2.7	0.55	–97.3
2800	41.9 – j3.9	0.55	–101.6
2900	39 – j5	0.55	–106.3
3000	35.7 – j5.9	0.54	–111.9

LO Input Port

The mixer's LO input, shown in Figure 6, is internally matched from 0.9GHz to 3.5GHz. LO input matching near 600MHz requires the series inductor (L4)/shunt capacitor (C4) network shown in Figure 6. Likewise, the 2GHz match can be improved by using L4 = 2.7µH, C4 = 0.5pF. Measured LO input return losses for these three cases are plotted in Figure 7.

The optimum LO drive is –3dBm for LO frequencies above 1.2GHz, although the amplifiers are designed to accommodate several dB of LO input power variation without significant mixer performance variation. Below 1.2GHz, 0dBm LO drive is recommended for optimum noise figure, although –3dBm will still deliver good conversion gain and linearity.

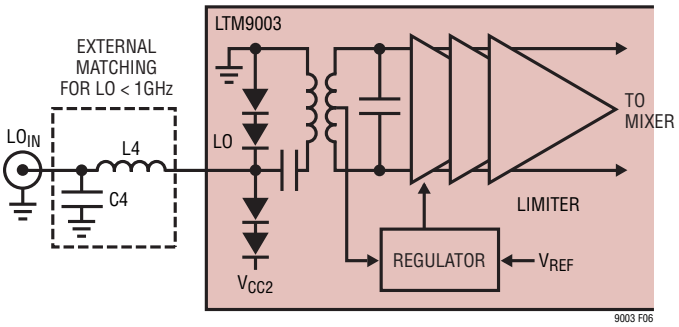


Figure 6. LO Input Schematic

Custom matching networks can be designed using the port impedance data listed in Table 2. This data is referenced to the LO pin with no external matching.

Table 2a. LO Input Impedance vs Frequency (LTM9003-AA)

FREQUENCY (MHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
500	10.3 – j6.1	0.73	–159.1
600	9.7 + j2.2	0.68	172.4
700	18.7 + j8.2	0.64	141.8
800	37 + j6.2	0.6	108.4
900	64.5 – j9.9	0.59	72.7
1000	109.7 – j42.2	0.6	38.3
1100	206.6 – j35.9	0.63	7.9
1200	183.8 + j70	0.66	–17.1
1300	115.4 + j59.4	0.68	–37.3
1400	86.7 + j35.2	0.7	–53.7
1500	70.7 + j18.5	0.71	–67.4
1600	59.3 + j7.4	0.7	–79.2
1700	50.2 + j0.2	0.7	–89.7
1800	42.6 – j4.5	0.68	–99.6
1900	35.9 – j7.2	0.66	–109.2
2000	30.2 – j8.3	0.63	–118.9
2100	25.6 – j8.1	0.59	–129.2
2200	22.4 – j6.7	0.54	–140.3
2300	20.8 – j4.6	0.48	–152.3
2400	21.5 – j2.1	0.42	–165.5
2500	24.2	0.35	–179.8
2600	28.9 + j1.3	0.28	163.9
2700	35.3 + j1.5	0.21	145.1
2800	42.6 + j0.9	0.16	121.1
2900	50.3	0.12	88.6
3000	57.7 – j0.6	0.1	45.8

APPLICATIONS INFORMATION

Table 2b. LO Input Impedance vs Frequency (LTM9003-AB)

FREQUENCY (MHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
500	14.3 – j7.5	0.68	–150.6
600	12.6 – j2.4	0.61	–170.4
700	15.8 + j1.9	0.53	170.8
800	22.7 + j4.1	0.44	151.5
900	32.5 + j3.8	0.35	130.2
1000	44.2 + j1.3	0.25	104.9
1100	56.3 – j1.2	0.18	70.3
1200	66 – j1.3	0.15	26.4
1300	70.7 + j1	0.18	–12.8
1400	69.9 + j3.1	0.21	–37.8
1500	66 + j3.7	0.25	–54.1
1600	61.8 + j3.3	0.27	–65.5
1700	58.1 + j2.4	0.28	–73.4
1800	54.9 + j1.5	0.29	–79.8
1900	52.7 + j0.8	0.28	–84.2
2000	50.7 + j0.2	0.28	–88.5
2100	49.4 – j0.2	0.27	–91.4
2200	47.8 – j0.5	0.25	–95.5
2300	46.7 – j0.7	0.23	–98.9
2400	45.7 – j0.8	0.2	–103.3
2500	45.5 – j0.7	0.17	–106.8
2600	46.4 – j0.4	0.13	–107.1
2700	48.7 – j0.1	0.1	–97.9
2800	50.9 + j0.1	0.09	–84.2
2900	52.9 + j0.3	0.09	–72.5
3000	54.6 + j0.5	0.11	–66.7

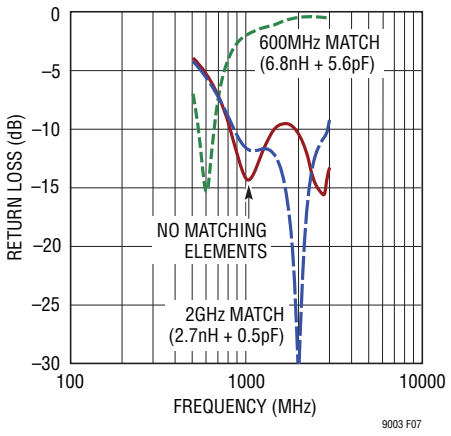


Figure 7. LO Input Return Loss with and without Matching

Mixer Enable Interface

The voltage necessary to turn on the mixer is 2.7V. To disable the mixer, the enable voltage must be less than 0.3V. If the MIX_EN pin is allowed to float, the mixer will tend to remain in its last operating state. Thus it is not recommended that the enable function be used in this manner. If the shutdown function is not required, then the MIX_EN pin should be connected directly to V_{CC1}.

Amplifier Enable Interface

The AMP_EN pin self-biases to V_{CC2} through a 30k resistor. The pin must be pulled below 0.8V in order to disable the amplifier.

Driving the ADC Clock Input

The noise performance of the ADC can depend on the encode signal quality as much as on the analog input. The ENC^+/ENC^- inputs are intended to be driven differentially, primarily for noise immunity from common mode noise sources. Each input is biased through a 4.8k resistor to a 1.5V bias. The bias resistors set the DC operating point for transformer coupled drive circuits and can set the logic threshold for single-ended drive circuits.

Any noise present on the encode signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

In applications where jitter is critical (high input frequencies) take the following into consideration:

1. Differential drive should be used.
2. Use as large an amplitude as possible; if transformer coupled use a higher turns ratio to increase the amplitude.
3. If the ADC is clocked with a sinusoidal signal, filter the encode signal to reduce wideband noise.
4. Balance the capacitance and series resistance at both encode inputs so that any coupled noise will appear at both inputs as common mode noise. The encode inputs have a common mode range of 1.2V to 2.0V. Each input may be driven from ground to V_{DD} for single-ended drive.

APPLICATIONS INFORMATION

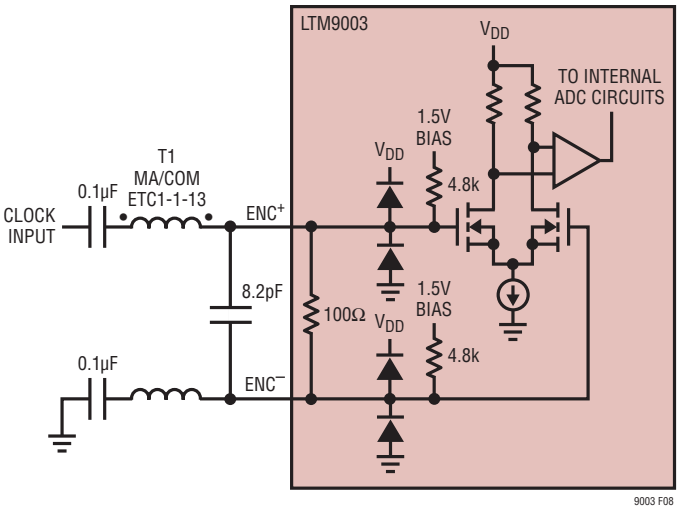


Figure 8. Transformer Driven ENC+/ENC–

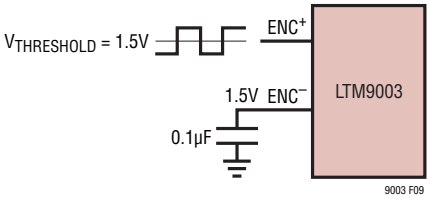


Figure 9. Single-Ended ENC Driver, Not Recommended for Low Jitter

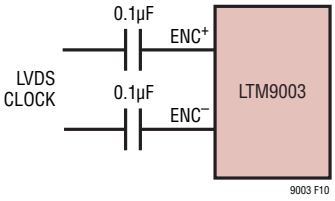


Figure 10. ENC Drive Using LVDS

Maximum and Minimum Conversion Rates

The maximum conversion rate for the ADC is 250Msps. For the ADC to operate properly, the encode signal should have a 50% (±5%) duty cycle. Each half cycle must have at least 1.9ns for the ADC internal circuitry to have enough settling time for proper operation. Achieving a precise 50% duty cycle is easy with differential sinusoidal drive using a transformer or using symmetric differential logic such as PECL or LVDS.

The lower limit of the sample rate is determined by the droop of the sample-and-hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTM9003 is 1Msps.

Clock Duty Cycle Stabilizer

An optional clock duty cycle stabilizer circuit can be used if the input clock has a non 50% duty cycle. This circuit uses the rising edge of the ENC+ pin to sample the analog input. The falling edge of ENC+ is ignored and the internal falling edge is generated by a phase-locked loop. The input clock duty cycle can vary from 40% to 60% and the clock duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require one hundred clock cycles for the PLL to lock onto the input clock. To use the clock duty cycle stabilizer, the MODE pin should be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using external resistors.

Clock Sources for Undersampling

Undersampling is especially demanding on the clock source and the higher the input frequency, the greater the sensitivity to clock jitter or phase noise. A clock source that degrades SNR of a full-scale signal by 1dB at 70MHz will degrade SNR by 3dB at 140MHz, and 4.5dB at 190MHz.

In cases where absolute clock frequency accuracy is relatively unimportant and only a single ADC is required, a canned oscillator from vendors such as Saronix or Vectron can be placed close to the ADC and simply connected directly to the ADC. If there is any distance to the ADC, some source termination to reduce ringing that may occur even over a fraction of an inch is advisable. You must not allow the clock to overshoot the supplies or performance will suffer. Do not filter the clock signal with a narrow band filter unless you have a sinusoidal clock source, as the rise and fall time artifacts present in typical digital clock signals will be translated into phase noise.

APPLICATIONS INFORMATION

The lowest phase noise oscillators have single-ended sinusoidal outputs, and for these devices the use of a filter close to the ADC may be beneficial. This filter should be close to the ADC to both reduce roundtrip reflection times, as well as reduce the susceptibility of the traces between the filter and the ADC. If the circuit is sensitive to close-in phase noise, the power supply for oscillators and any buffers must be very stable, or propagation delay variation with supply will translate into phase noise. Even though these clock sources may be regarded as digital devices, do not operate them on a digital supply. If your clock is also used to drive digital devices such as an FPGA, you should locate the oscillator, and any clock fan-out devices close to the ADC, and give the routing to the ADC precedence. The clock signals to the FPGA should have series termination at the driver to prevent high frequency noise from the FPGA disturbing the substrate of the clock fan-out device. If you use an FPGA as a programmable divider, you must re-time the signal using the original oscillator, and the re-timing flip-flop as well as the oscillator should be close to the ADC, and powered with a very quiet supply.

For cases where there are multiple ADCs, or where the clock source originates some distance away, differential clock distribution is advisable. This is advisable both from the perspective of EMI, but also to avoid receiving noise from digital sources both radiated, as well as propagated in the waveguides that exist between the layers of multilayer PCBs. The differential pairs must be close together and distanced from other signals. The differential pair should be guarded on both sides with copper distanced at least 3x the distance between the traces, and grounded with vias no more than 1/4 inch apart.

Digital Outputs

Table 3 shows the relationship between the analog input voltage, the digital data bits, and the overflow bit.

Table 3. Output Codes vs Input Voltage

INPUT (SENSE = V_{DD})	OF	D11 – D0 (OFFSET BINARY)	D11 – D0 (2'S COMPLEMENT)
Overvoltage	1	1111 1111 1111	0111 1111 1111
Maximum	0 0	1111 1111 1111 1111 1111 1110	0111 1111 1111 0111 1111 1110
0.000000V	0 0 0 0	1000 0000 0001 1000 0000 0000 0111 1111 1111 0111 1111 1110	0000 0000 0001 0000 0000 0000 1111 1111 1111 1111 1111 1110
Minimum	0 0	0000 0000 0001 0000 0000 0000	1000 0000 0001 1000 0000 0000
Undervoltage	1	0000 0000 0000	1000 0000 0000

Digital Output Buffers

Figure 11 shows an equivalent circuit for a differential output pair in the LVDS output mode. A 3.5mA current is steered from OUT+ to OUT– or vice versa which creates a ±350mV differential voltage across the 100Ω termination resistor at the LVDS receiver. A feedback loop regulates the common mode output voltage to 1.25V. For proper operation each LVDS output pair needs an external 100Ω

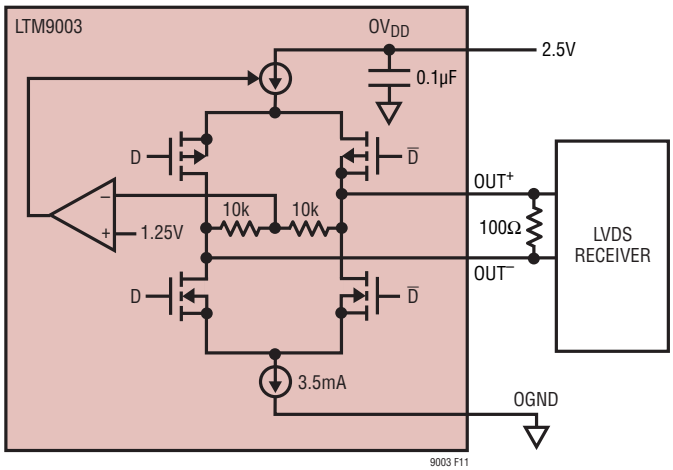


Figure 11. Digital Output in LVDS Mode

APPLICATIONS INFORMATION

termination resistor, even if the signal is not used (such as OF^+/OF^- or $CLKOUT^+/CLKOUT^-$). To minimize noise the PC board traces for each LVDS output pair should be routed close together. To minimize clock skew all LVDS PC board traces should have about the same length.

Data Format

The LTM9003 parallel digital output can be selected for offset binary or 2's complement format. The format is selected with the MODE pin. Connecting MODE to GND or $1/3V_{DD}$ selects offset binary output format. Connecting MODE to $2/3V_{DD}$ or V_{DD} selects 2's complement output format. An external resistor divider can be used to set the $1/3V_{DD}$ or $2/3V_{DD}$ logic values. Table 4 shows the logic states for the MODE pin.

Table 4. MODE Pin Function

MODE PIN	OUTPUT FORMAT	CLOCK DUTY CYCLE STABILIZER
0	Straight Binary	Off
$1/3V_{DD}$	Straight Binary	On
$2/3V_{DD}$	2's Complement	On
V_{DD}	2's Complement	Off

Overflow Bit

An overflow output bit indicates when the converter is overranged or underranged. A differential logic high on the OF^+/OF^- pins indicates an overflow or underflow.

Output Clock

The LTM9003 has a delayed version of the ENC^+ input available as a digital output, CLKOUT. The CLKOUT pin can be used to synchronize the converter data to the digital system. This is necessary when using a sinusoidal encode. Data will be updated just after $CLKOUT^+/CLKOUT^-$ rises and can be latched on the falling edge of $CLKOUT^+/CLKOUT^-$.

Output Driver Power

OV_{DD} should be connected to a 2.5V supply and OGND should be connected to GND.

Output Enable

The outputs may be disabled with the output enable pin, $\overline{OE}$. In LVDS output mode $\overline{OE}$ high disables all data outputs including OF and CLKOUT. The data access and bus relinquish times are too slow to allow the outputs to be enabled and disabled during full speed operation. The output Hi-Z state is intended for use during long periods of inactivity.

The Hi-Z state is not a truly open circuit; the output pins that make an LVDS output pair have a 20k resistance between them.

Sleep and Nap Modes

The converter may be placed in shutdown or nap modes to conserve power. Connecting SHDN to GND results in normal operation. Connecting SHDN to V_{DD} and $\overline{OE}$ to V_{DD} results in sleep mode, which powers down all circuitry including the reference and the ADC typically dissipates 1.5mW. When exiting sleep mode, it will take milliseconds for the output data to become valid because the reference capacitors have to recharge and stabilize. Connecting SHDN to V_{DD} and $\overline{OE}$ to GND results in nap mode and the ADC typically dissipates 30mW. In nap mode, the on-chip reference circuit is kept on, so that recovery from nap mode is faster than that from sleep mode, typically taking 100 clock cycles. In both sleep and nap modes, all digital outputs are disabled and enter the Hi-Z state.

Supply Sequencing

The V_{CC1} and V_{CC2} pins provide the supply to the mixer and amplifier, respectively, and the V_{DD} pin provides the supply to the ADC. The mixer, amplifier and ADC are separate integrated circuits within the LTM9003. Separate linear regulators can be used without additional supply sequencing circuitry if they have common input supplies.

APPLICATIONS INFORMATION

Grounding and Bypassing

The LTM9003 requires a printed circuit board with a clean unbroken ground plane; a multilayer board with an internal ground plane is recommended. The pinout of the LTM9003 has been optimized for a flow-through layout so that the interaction between inputs and digital outputs is minimized. Ample ground pads facilitate a layout that ensures that digital and analog signal lines are separated as much as possible.

The LTM9003 is internally bypassed with the ADC (V_{DD}), amplifier (V_{CC2}) and mixer (V_{CC1}) supplies returning to a common ground (GND). The digital output supply (OV_{DD}) is returned to OGND. Additional bypass capacitance is optional and may be required if power supply noise is significant.

Heat Transfer

Most of the heat generated by the LTM9003 is transferred through the bottom-side ground pads. For good electrical and thermal performance, it is critical that all ground pins are connected to a ground plane of sufficient area with as many vias as possible.

Recommended Layout

The high integration of the LTM9003 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for ground. This helps to dissipate heat in the package through the board and also helps to shield sensitive on-board analog signals. Common ground (GND) and output ground (OGND) are electrically isolated on the LTM9003, but can be connected on the PCB underneath the part to provide a common return path.

- Use multiple ground vias. Using as many vias as possible helps to improve the thermal performance of the board and creates necessary barriers separating analog and digital traces on the board at high frequencies.

- Separate analog and digital traces as much as possible, using vias to create high-frequency barriers. This will reduce digital feedback that can reduce the signal-to-noise ratio (SNR) and dynamic range of the LTM9003.

Figures 12 through 15 give a good example of the recommended layout.

The quality of the paste print is an important factor in producing high yield assemblies. It is recommended to use a type 3 or 4 printing no-clean solder paste. The solder stencil design should follow the guidelines outlined in Application Note 100.

The LTM9003 employs gold-finished pads for use with Pb-based or tin-based solder paste. It is inherently Pb-free and complies with the JEDEC (e4) standard. The materials declaration is available online at http://www.linear.com/leadfree/mat_dec.jsp.

APPLICATIONS INFORMATION

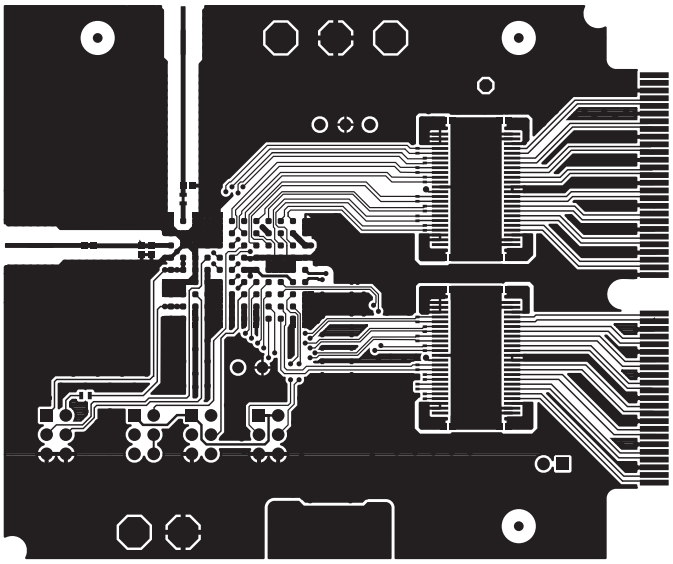


Figure 12. Layer 1 Component Side

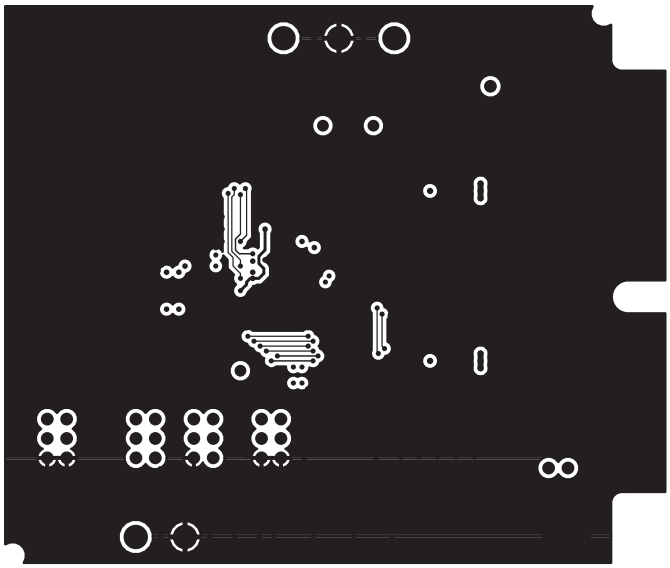


Figure 13. Layer 2

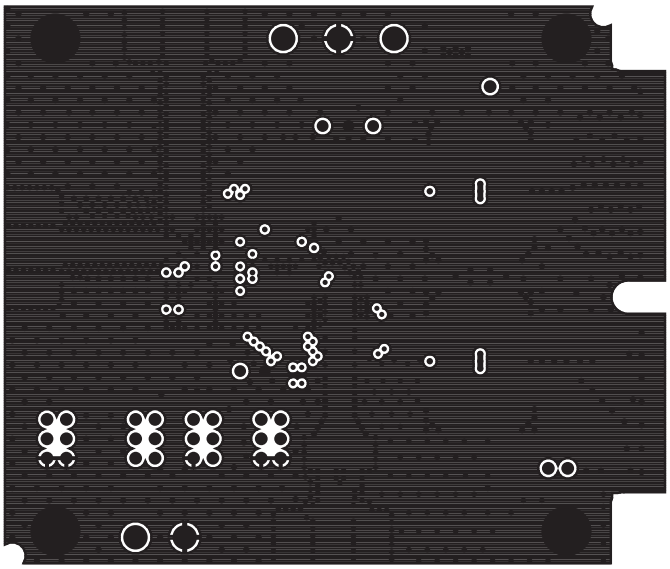


Figure 14. Layer 3

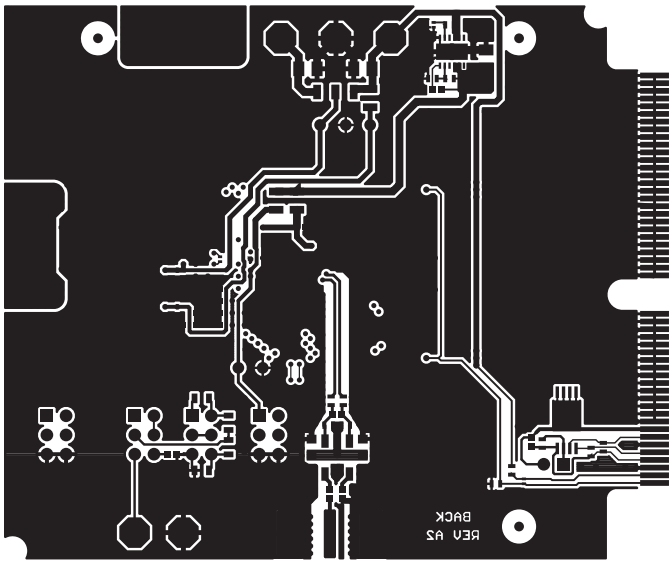
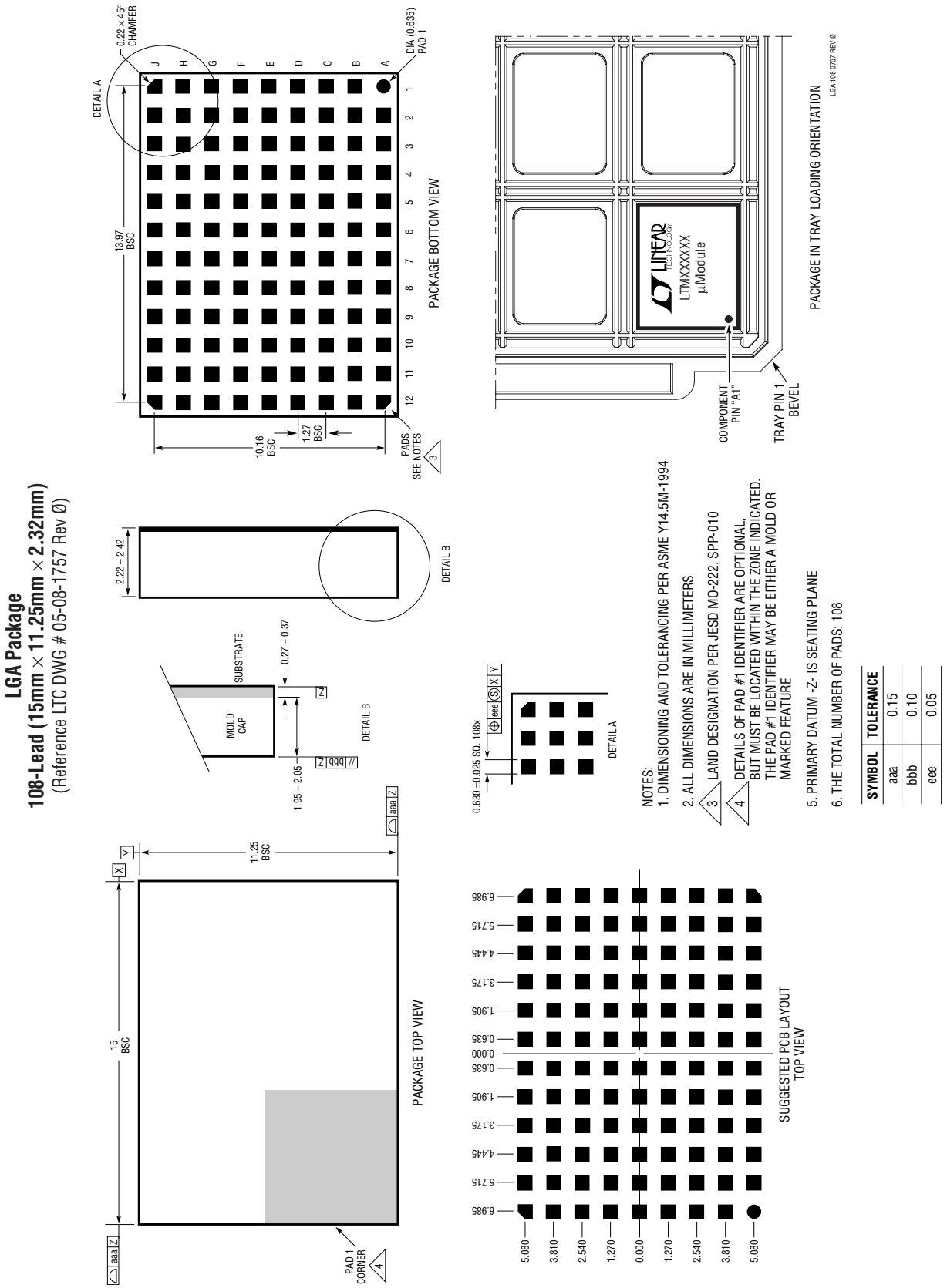


Figure 15. Backside

PACKAGE DESCRIPTION



Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2240-10	10-Bit, 170Msps, 2.5V ADC, LVDS Outputs	445mW, 60.6dB SNR, 78dB SFDR, 64-Pin QFN
LTC2240-12	12-Bit, 170Msps, 2.5V ADC, LVDS Outputs	445mW, 65.5dB SNR, 80dB SFDR, 64-Pin QFN
LTC2241-10	10-Bit, 210Msps, 2.5V ADC, LVDS Outputs	585mW, 60.6dB SNR, 78dB SFDR, 64-Pin QFN
LTC2241-12	12-Bit, 210Msps, 2.5V ADC, LVDS Outputs	585mW, 65.5dB SNR, 78dB SFDR, 64-Pin QFN
LTC2242-10	10-Bit, 250Msps, 2.5V ADC, LVDS Outputs	740mW, 60.5dB SNR, 78dB SFDR, 64-Pin QFN
LTC2242-12	12-Bit, 250Msps, 2.5V ADC, LVDS Outputs	740mW, 65.4dB SNR, 78dB SFDR, 64-Pin QFN
LTC6410	Differential IF Amplifier with Configurable Input Impedance	1.4GHz, –3dB BW, 6dB Fixed Voltage Gain (50Ω System), 36dBm OIP3
LT5527	400MHz to 3.7GHz, 5V High Signal Level Downconverting Mixer	23.5dBm IIP3 at 1.9GHz, NF = 12.5dB, Single-Ended RF and LO Ports
LT5557	400MHz to 3.8GHz, 3.3V High Signal Level Downconverting Mixer	24.7dBm IIP3 at 1.9GHz, NF = 11.7dB, Single-Ended RF and LO Ports, 3.3V Supply
LTM9001-AA	16-Bit, IF/Baseband Receiver Subsystem	16-Bit, 130Msps ADC, 20dB Gain Amplifier, Anti-Alias Filter, Internal Bypass Capacitance
LTM9002-AA	Dual 14-Bit, IF/Baseband Receiver Subsystem	Dual 14-Bit, 125Msps ADC, Dual 26dB Gain Amplifiers, Anti-Alias Filters, Auxiliary DAC for Gain Adjustment, Internal Bypass Capacitance

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