40V_{IN}, 2A Silent Switcher µModule Regulator

FEATURES

- **Low Noise Silent Switcher® Architecture**
- **Wide Input Voltage Range: 3.2V to 40V**
- **Wide Output Voltage Range: 0.8V to 15V**
- **2A Continuous Output Current at 12V_{IN}, 5V_{OUT}, T_A = 85°C**
- **2.5A Peak Current**
- Selectable Switching Frequency: 200kHz to 2.2MHz
- External Synchronization
- Configurable as an Inverter
- 6.25mm × 4mm × 2.22mm BGA Package

APPLICATIONS

- Automotive Battery Regulation
- Power for Portable Products
- Distributed Supply Regulation
- Industrial Supplies
- Wall Transformer Regulation

DESCRIPTION

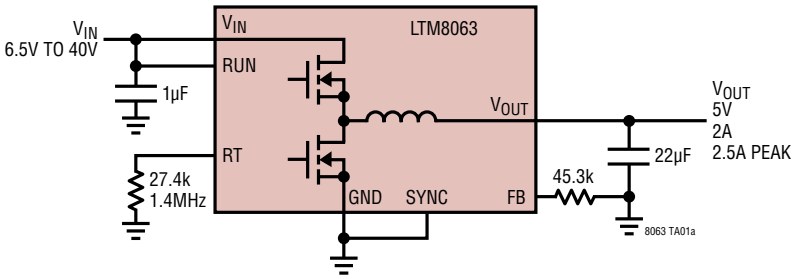
The LTM®8063 is a 40V_{IN}, 2A continuous, 2.5A peak, step-down µModule® (power module) regulator. Included in the package are the switching controller, power switches, inductor, and all support components. Operating over an input voltage range of 3.2V to 40V, the LTM8063 supports an output voltage range of 0.8V to 15V and a switching frequency range of 200kHz to 2.2MHz, each set by a single resistor. Only the input and output filter capacitors are needed to finish the design.

The low profile package enables utilization of unused space on the bottom of PC boards for high density point of load regulation. The LTM8063 is packaged in a thermally enhanced, compact over-molded ball grid array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8063 is RoHS compliant.

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TYPICAL APPLICATION

5V_{OUT} from 6.5V_{IN} to 40V_{IN} Step-Down Converter



PINS NOT USED IN THIS CIRCUIT: TR/SS, PG

Efficiency vs Load Current

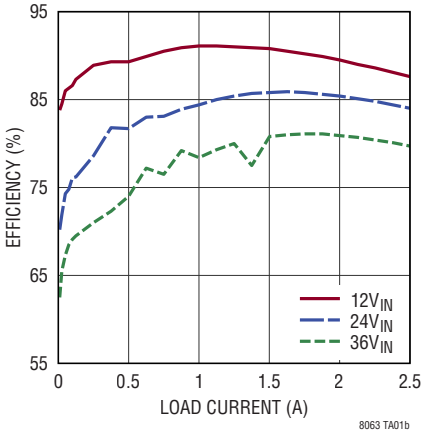


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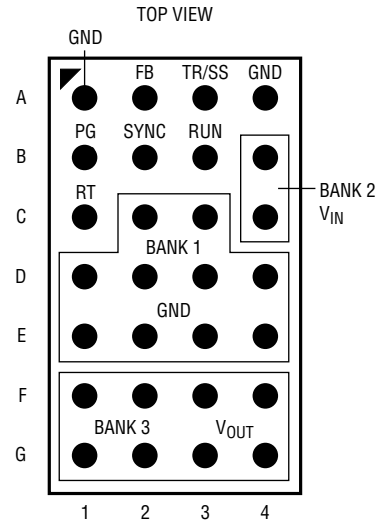
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ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{IN}, RUN, PG Voltage 42V
V_{OUT} Voltage 19V
FB, TR/SS Voltage 4V
SYNC Voltage 6V
Maximum Internal Temperature ..... 125°C
Storage Temperature ..... –55°C to 125°C
Peak Reflow Solder Body Temperature ..... 260°C

PIN CONFIGURATION



BGA PACKAGE
28-LEAD (6.25mm × 4mm × 2.22mm) BGA PACKAGE
T_{JMAX} = 125°C, θ_{JA} = 41.5°C/W, $\theta_{JCbottom}$ = 13°C/W
θ_{JCtop} = 52.4°C/W, θ_{JB} = 16.3°C/W, WEIGHT = 0.14g
θ VALUES DETERMINED PER JEDEC51-9, 51-12

ORDER INFORMATION

PART NUMBER	TERMINAL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE
		DEVICE	FINISH CODE			
LTM8063EY#PBF	SAC305 (RoHS)	8063	v	BGA	3	–40°C to 125°C
LTM8063IY#PBF						
LTM8063IY	SnPb (63/37)		•			

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- BGA Package and Tray Drawings
- This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to Recommended BGA PCB Assembly and Manufacturing Procedures.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 12V, RUN = 2V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage	V_{IN} Rising	●			3.2	V
Output DC Voltage	R_{FB} Open R_{FB} = 13.7kΩ, V_{IN} = 40V			0.8 15		V V
Peak Output DC Current	V_{OUT} = 3.3V, f_{SW} = 1MHz		2.5			A
Quiescent Current into V_{IN}	RUN = 0V No Load, SYNC = 0V, Not Switching				3 8	µA µA
Line Regulation	5.5V < V_{IN} < 36V, I_{OUT} = 1A			0.5		%
Load Regulation	0.1A < I_{OUT} < 2A			0.5		%
Output Voltage Ripple	I_{OUT} = 2A			15		mV
Switching Frequency	R_T = 232kΩ, V_{IN} = 8V R_T = 41.2kΩ R_T = 15.8kΩ			200 1 2.2		kHz MHz MHz
Voltage at FB		●	760	774	786	mV
RUN Threshold Voltage			0.9		1.2	V
RUN Current					1	µA
TR/SS Current	TR/SS = 0V			2		µA
TR/SS Pull Down	TR/SS = 0.1V			300		Ω
PG Threshold Voltage at FB (Upper)	FB Falling (Note 5)			0.84		V
PG Threshold Voltage at FB (Lower)	FB Rising (Note 5)			0.7		V
PG Leakage Current	PG = 42V				1	µA
PG Sink Current	PG = 0.1V			150		µA
SYNC Threshold Voltage	Synchronization		0.4		1.5	V
SYNC Voltage	To Enable Spread Spectrum		2.9		4.2	V
SYNC Current	SYNC = 2V				5	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Unless otherwise noted, the absolute minimum voltage is zero.

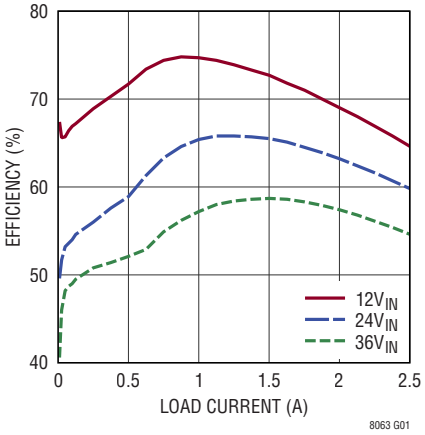
Note 3: The LTM8063E is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8063I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 4: The LTM8063 contains overtemperature protection that is intended to protect the device during momentary overload conditions. The internal temperature exceeds the maximum operating junction temperature when the overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

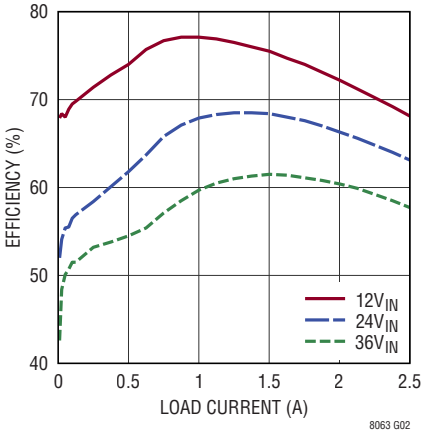
Note 5: PG transitions from low to high.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

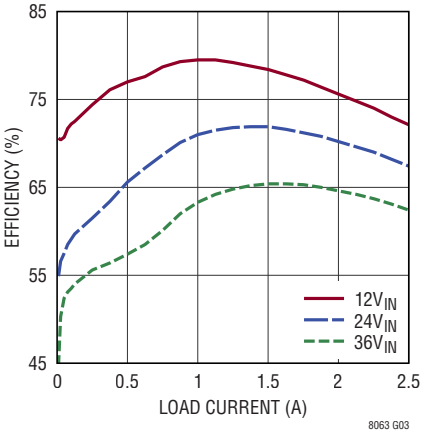
Efficiency, V_{OUT} = 1V



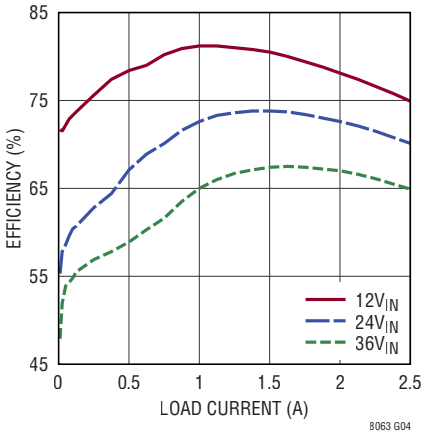
Efficiency, V_{OUT} = 1.2V



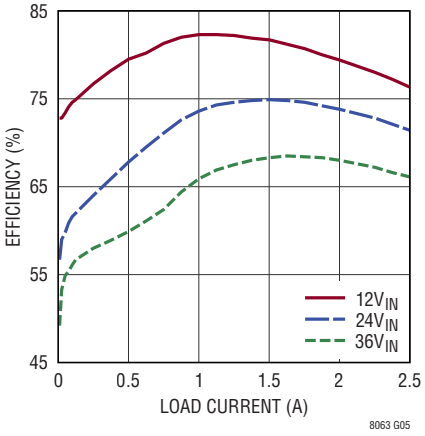
Efficiency, V_{OUT} = 1.5V



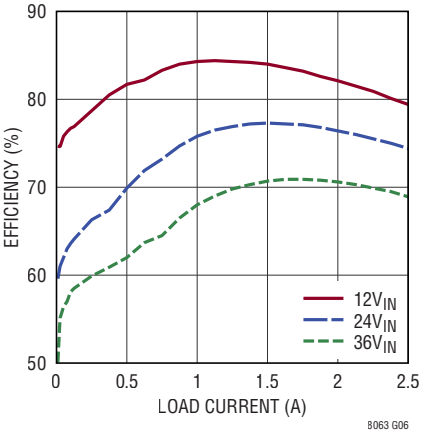
Efficiency, V_{OUT} = 1.8V



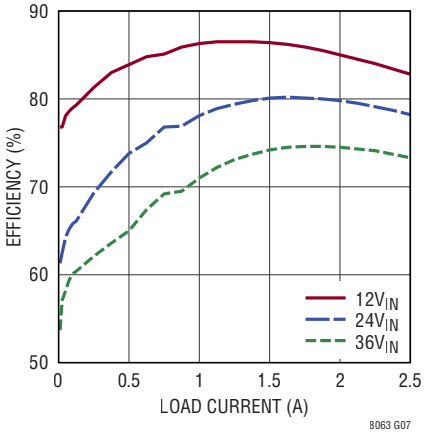
Efficiency, V_{OUT} = 2V



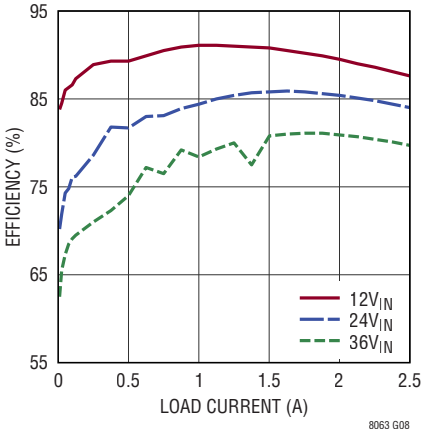
Efficiency, V_{OUT} = 2.5V



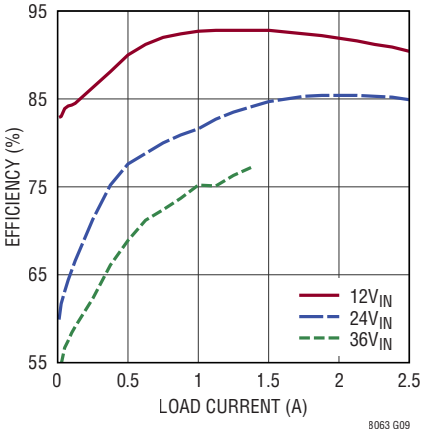
Efficiency, V_{OUT} = 3.3V



Efficiency, V_{OUT} = 5V

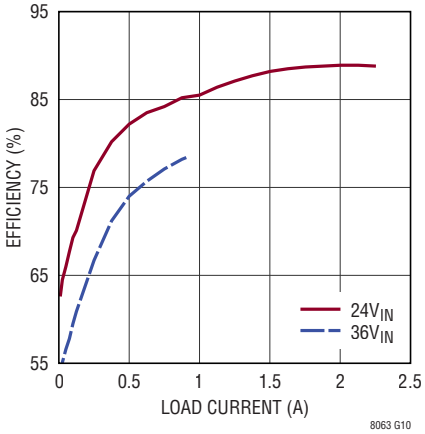


Efficiency, V_{OUT} = 8V

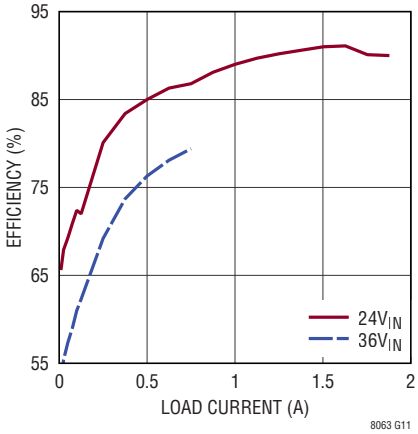


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

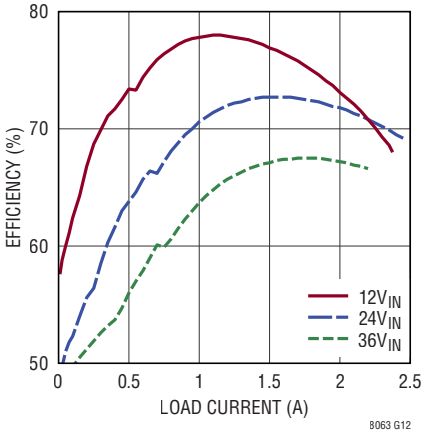
Efficiency, V_{OUT} = 12V



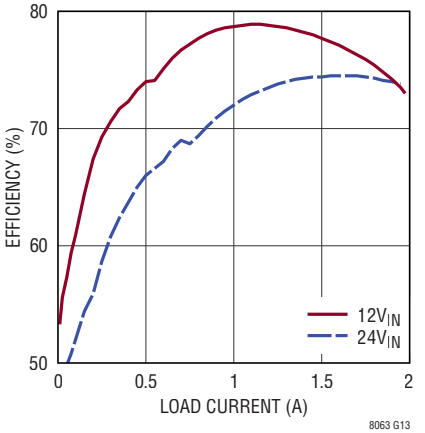
Efficiency, V_{OUT} = 15V



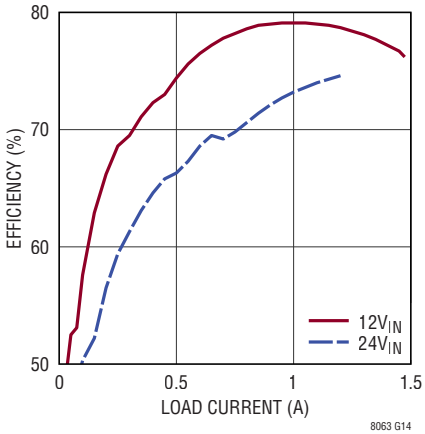
Efficiency, V_{OUT} = –3.3V



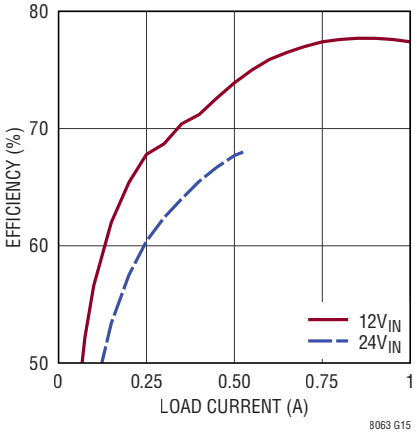
Efficiency, V_{OUT} = –5V



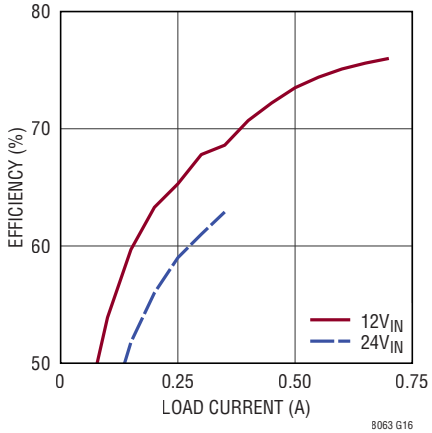
Efficiency, V_{OUT} = –8V



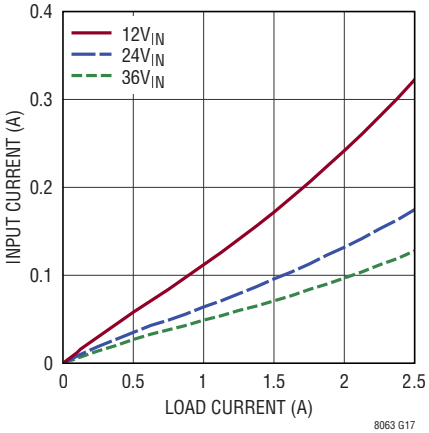
Efficiency, V_{OUT} = –12V



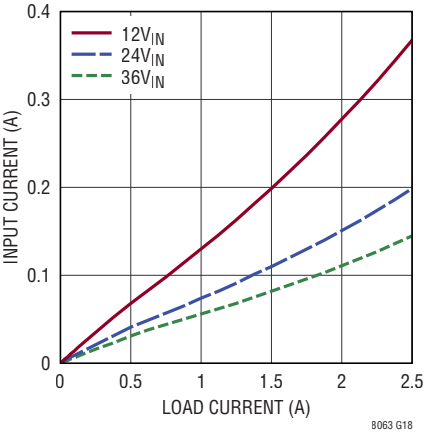
Efficiency, V_{OUT} = –15V



Input vs Load Current, V_{OUT} = 1V

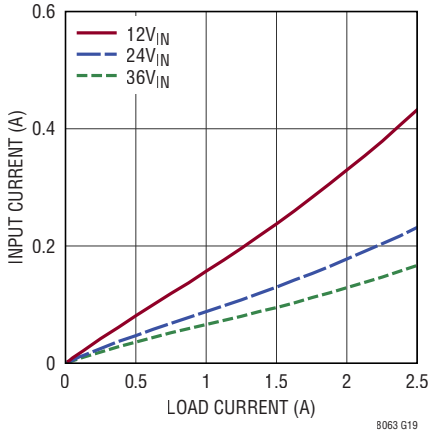


Input vs Load Current, V_{OUT} = 1.2V

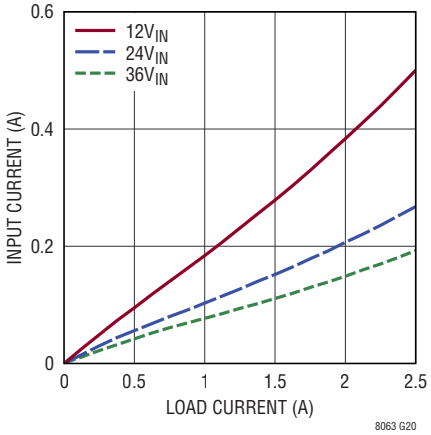


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

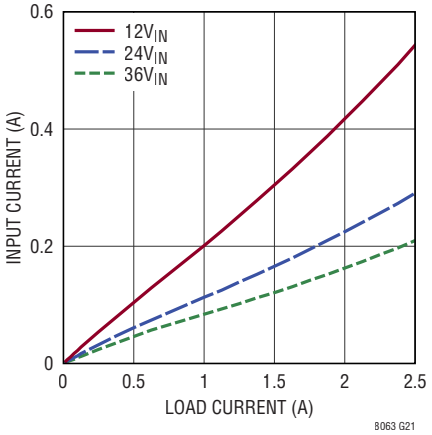
Input vs Load Current
V_{OUT} = 1.5V



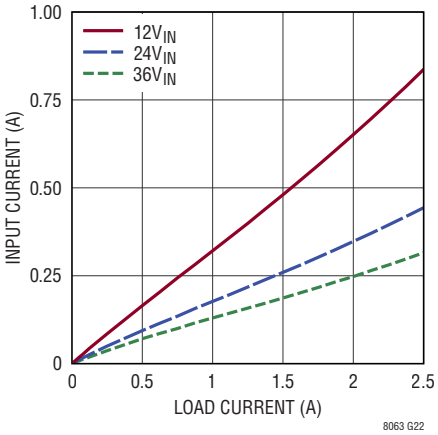
Input vs Load Current
V_{OUT} = 1.8V



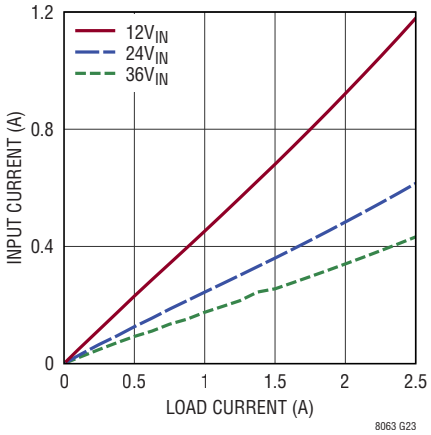
Input vs Load Current
V_{OUT} = 2V



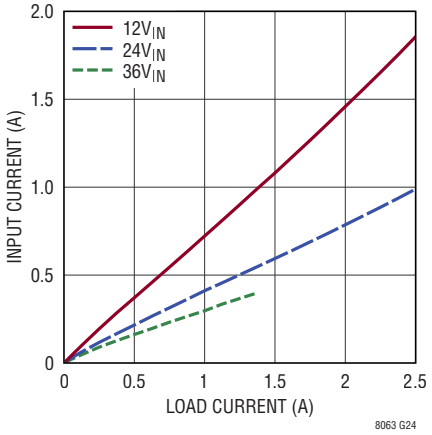
Input vs Load Current
V_{OUT} = 3.3V



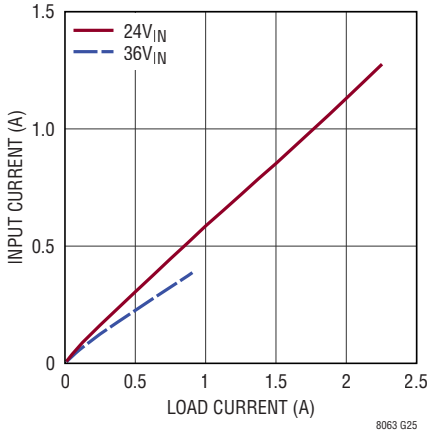
Input vs Load Current
V_{OUT} = 5V



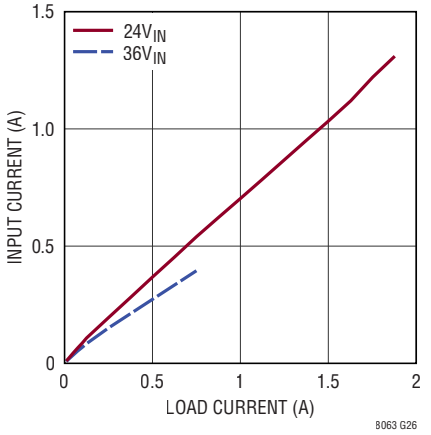
Input vs Load Current
V_{OUT} = 8V



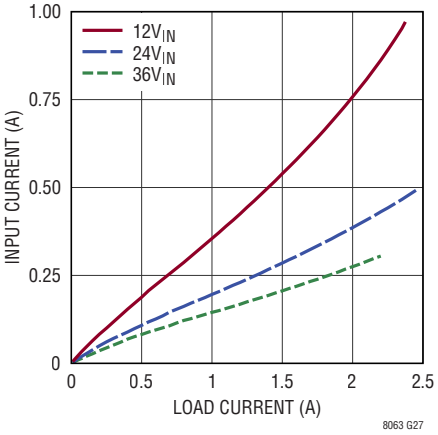
Input vs Load Current
V_{OUT} = 12V



Input vs Load Current
V_{OUT} = 15V

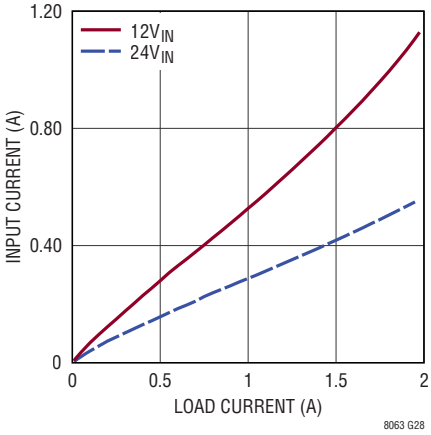


Input vs Load Current
V_{OUT} = –3.3V

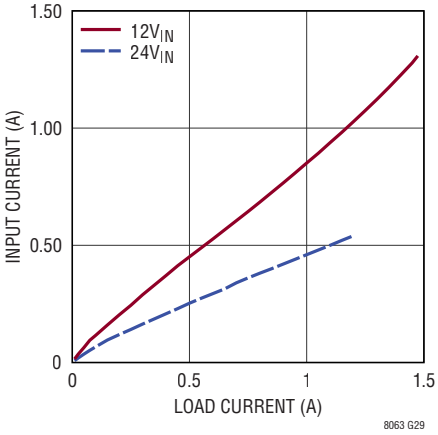


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

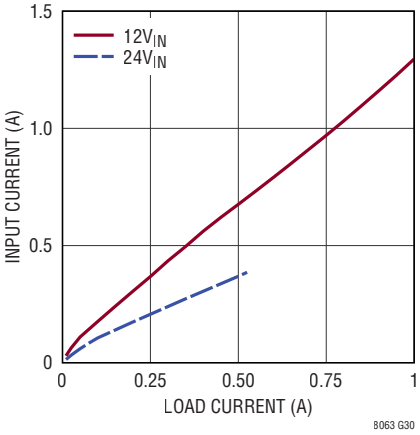
Input vs Load Current
V_{OUT} = –5V



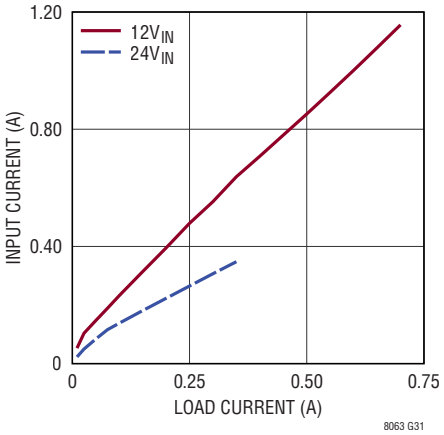
Input vs Load Current
V_{OUT} = –8V



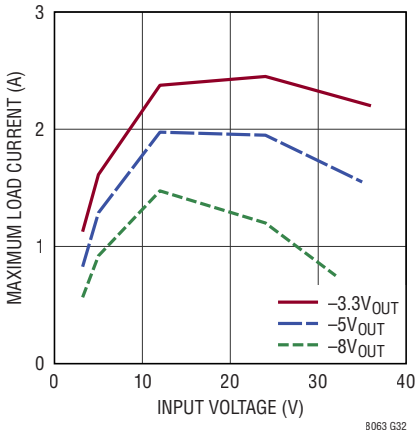
Input vs Load Current
V_{OUT} = –12V



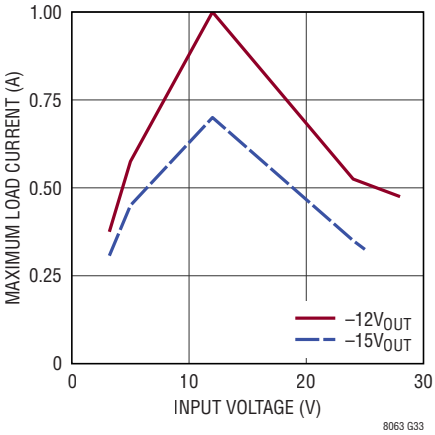
Input vs Load Current
V_{OUT} = –15V



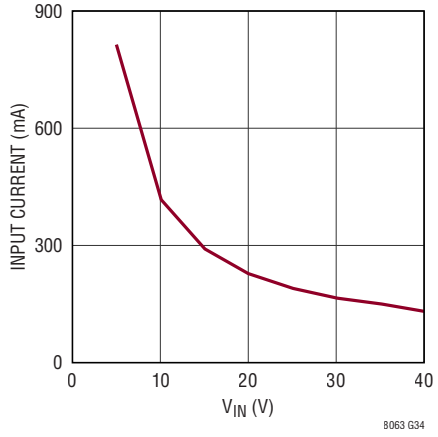
Maximum Load Current vs V_{IN}



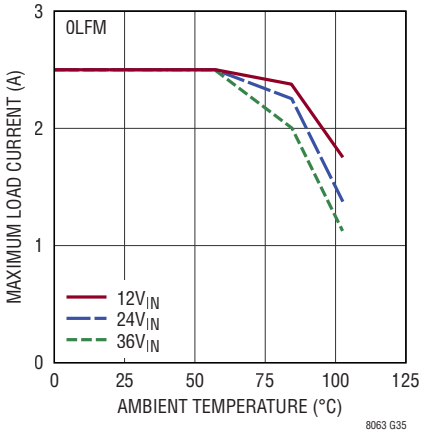
Maximum Load Current vs V_{IN}



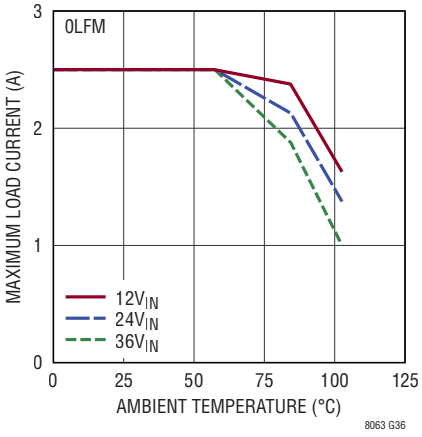
Input Current vs V_{IN}
V_{OUT} Short Circuited



Derating, V_{OUT} = 1V,
DC2494A Demo Board

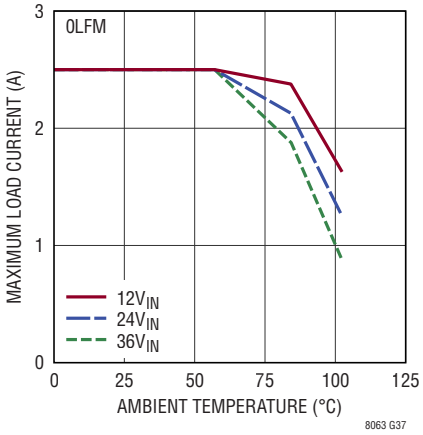


Derating, V_{OUT} = 1.2V,
DC2494A Demo Board

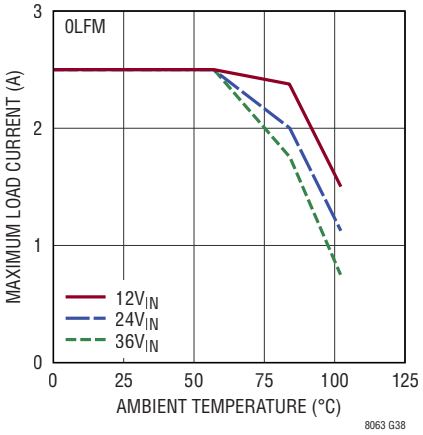


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

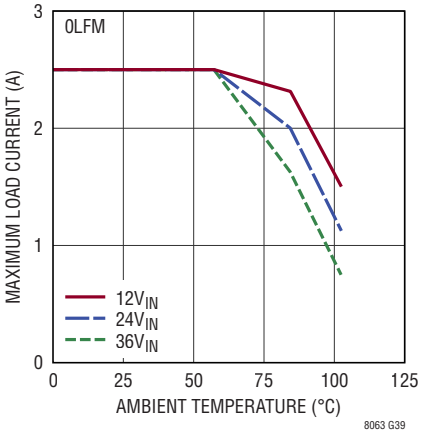
Derating, V_{OUT} = 1.5V, DC2494A Demo Board



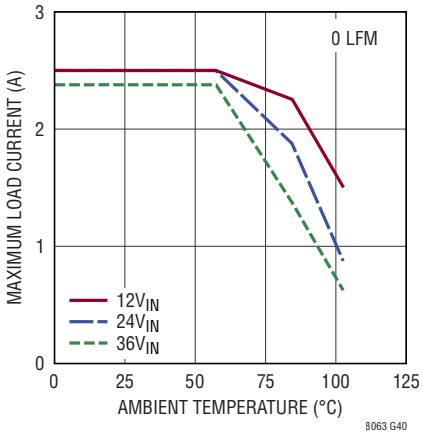
Derating, V_{OUT} = 1.8V, DC2494A Demo Board



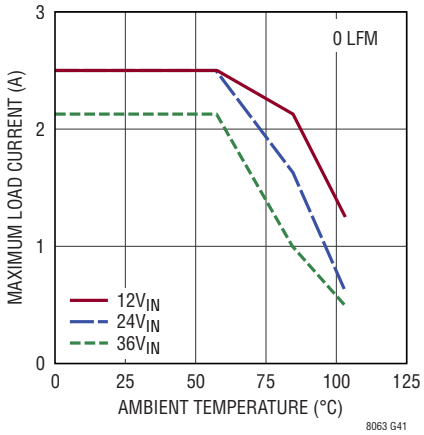
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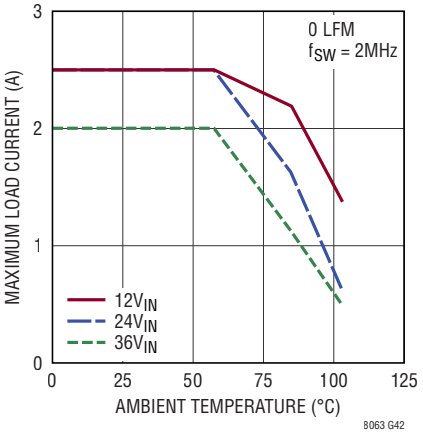
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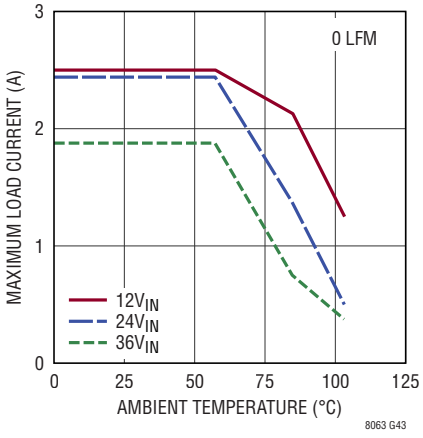
Derating, V_{OUT} = 3.3V, DC2494A Demo Board



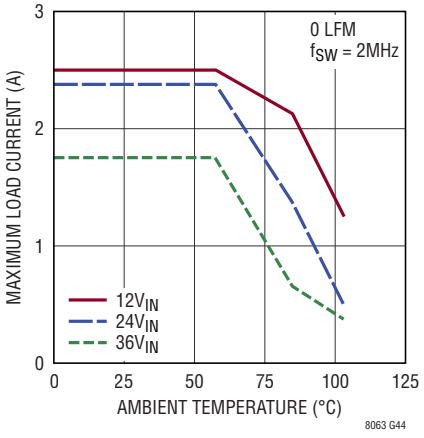
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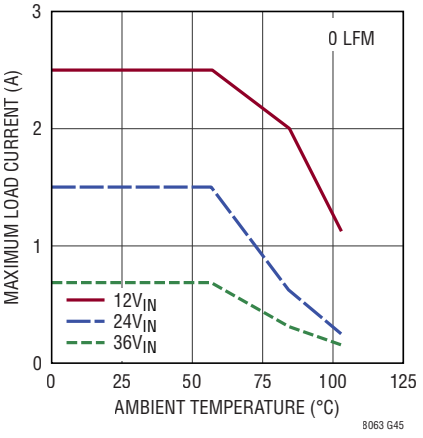
Derating, V_{OUT} = 5V, DC2494A Demo Board



Derating, V_{OUT} = 5V, DC2494A Demo Board

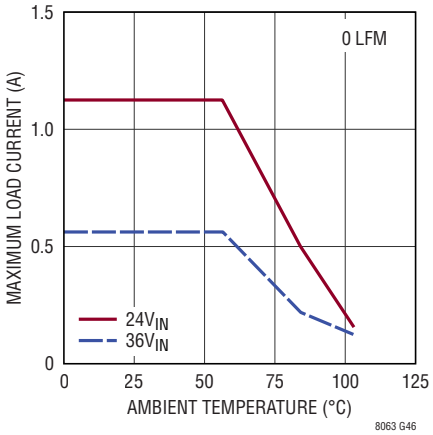


Derating, V_{OUT} = 8V, DC2494A Demo Board

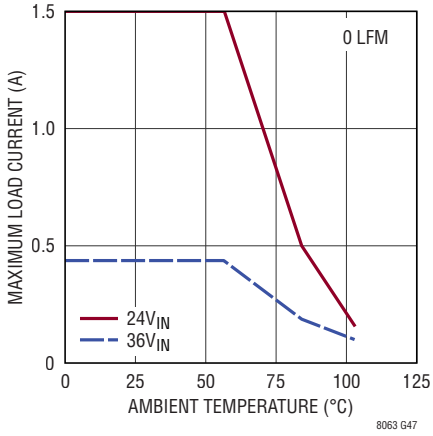


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

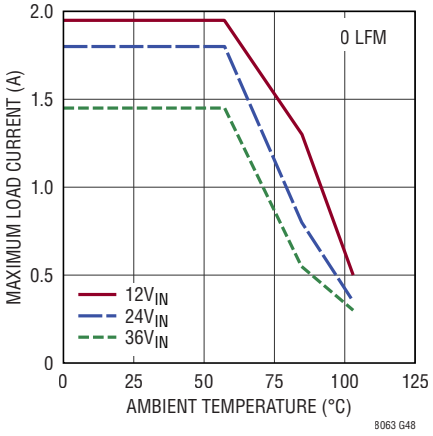
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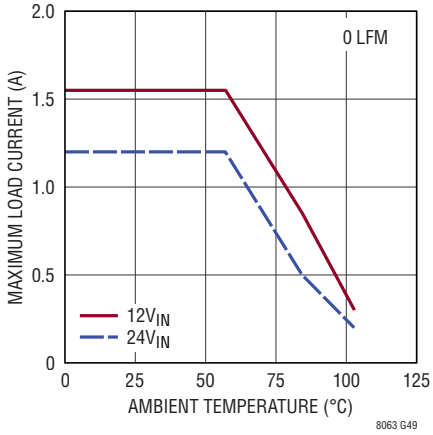
Derating, V_{OUT} = 15V, DC2494A Demo Board



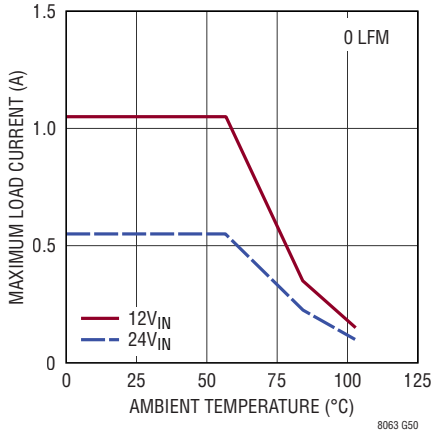
Derating, V_{OUT} = –3.3V, DC2494A Demo Board



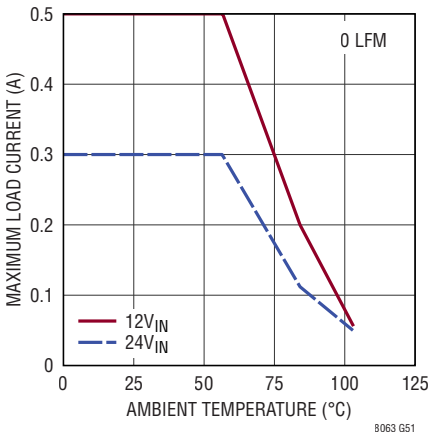
Derating, V_{OUT} = –5V, DC2494A Demo Board



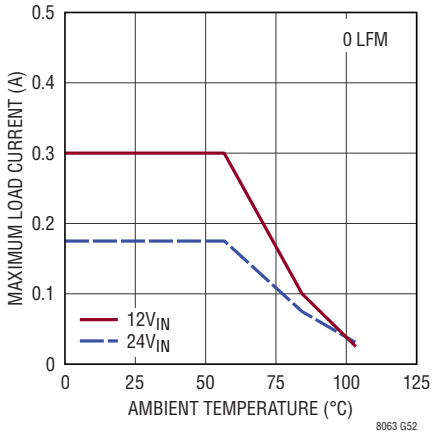
Derating, V_{OUT} = –8V, DC2494A Demo Board



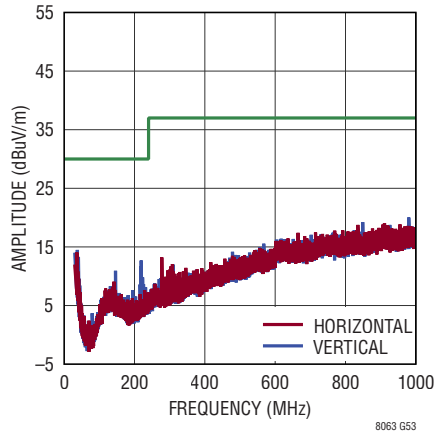
Derating, V_{OUT} = –12V, DC2494A Demo Board



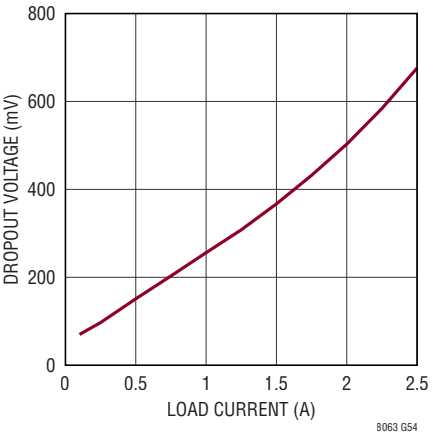
Derating, V_{OUT} = –15V, DC2494A Demo Board



CISPR22 Class B Emissions DC2494A Demo Board, V_{OUT} = 5V, C9 = 0.1µF, No EMI Filter, 1A Load



Dropout Voltage vs Load Current V_{OUT} = 5V



PIN FUNCTIONS

GND (Bank 1, A1, A4): Tie these GND pins to a local ground plane below the LTM8063 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8063 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details.

V_{IN} (Bank 2): V_{IN} supplies current to the LTM8063's internal regulator and to the internal power switches. These pins must be locally bypassed with an external, low ESR capacitor; see Table 1 for recommended values.

V_{OUT} (Bank 3): Power Output Pins. Apply the output filter capacitor and the output load between these pins and GND pins.

RUN (Pin B3): Pull the RUN pin below 0.9V to shut down the LTM8063. Tie to 1.2V or more for normal operation. If the shutdown feature is not used, tie this pin to the V_{IN} pin.

RT (Pin C1): The RT pin is used to program the switching frequency of the LTM8063 by connecting a resistor from this pin to ground. The Applications Information section of the data sheet includes a table to determine the resistance value based on the desired switching frequency. Minimize capacitance at this pin. Do not drive this pin.

SYNC (Pin B2): External clock synchronization input and operational mode. This pin programs four different operating modes:

1. Burst Mode® Operation. Tie this pin to ground for Burst Mode operation at low output loads—this will result in ultralow quiescent current.
2. Pulse-skipping mode. Float this pin for pulse-skipping mode. This mode offers full frequency operation down to low output loads before pulse skipping occurs.
3. Spread spectrum mode. Tie this pin high (between 2.9V and 4.2V) for pulse-skipping mode with spread spectrum modulation.
4. Synchronization mode. Drive this pin with a clock source to synchronize to an external frequency. During synchronization the part will operate in pulse-skipping mode.

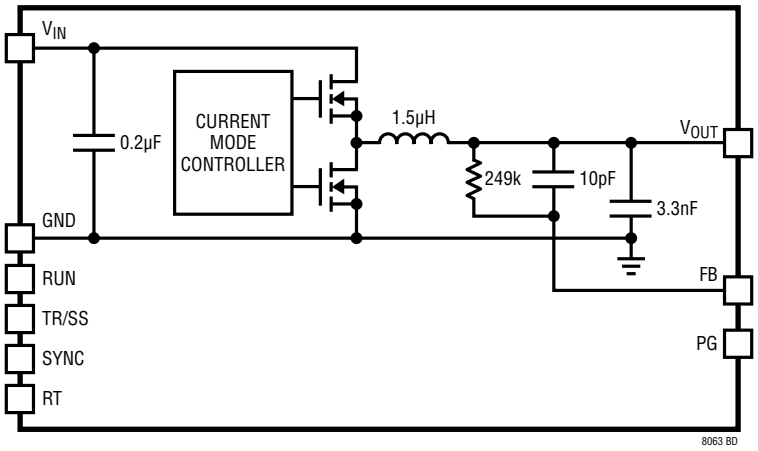
PG (Pin B1): The PG pin is the open-collector output of an internal comparator. PG remains low until the FB pin voltage is within about 10% of the final regulation voltage. The PG signal is valid when V_{IN} is above 3.2V. If V_{IN} is above 3.2V and RUN is low, PG will drive low. If this function is not used, leave this pin floating.

FB (Pin A2): The LTM8063 regulates its FB pin to 0.77V. Connect the adjust resistor from this pin to ground. The value of R_{FB} is given by the equation $R_{FB} = 192.73/(V_{OUT} – 0.774)$, where R_{FB} is in kΩ.

TR/SS (Pin A3): The TR/SS pin is used to provide a soft-start or tracking function. The internal 2µA pull-up current in combination with an external capacitor tied to this pin creates a voltage ramp. If TR/SS is less than about 0.77V, the FB voltage tracks to this value. The soft-start ramp time is approximated by the equation $t = 0.39 \bullet C$ where C is in µF. For tracking, tie a resistor divider to this pin from the tracked output. This pin is pulled to ground with an internal MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating if the tracking function is not needed.

BLOCK DIAGRAM

LTM8063 Block Diagram



OPERATION

The LTM8063 is a stand-alone non-isolated step-down switching DC/DC power supply that can deliver up to 2.5A. The continuous current is determined by the internal operating temperature. It provides a precisely regulated output voltage programmable via one external resistor from 0.8V to 15V. The input voltage range is 3.2V to 40V. Given that the LTM8063 is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current. A simplified Block Diagram is given above.

The LTM8063 contains a current mode controller, power switching elements, power inductor and a modest amount of input and output capacitance. The LTM8063 is a fixed frequency PWM regulator. The switching frequency is set by simply connecting the appropriate resistor value from the RT pin to GND.

The RUN pin is used to place the LTM8063 in shutdown, disconnecting the output and reducing the input current to a few µA.

To enhance efficiency, the LTM8063 automatically switches to Burst Mode operation in light or no load situations. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current to just a few µA.

The oscillator reduces the LTM8063's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the output current during start-up and overload.

The TR/SS node acts as an auxiliary input to the error amplifier. The voltage at FB servos to the TR/SS voltage until TR/SS goes above 0.77V. Soft-start is implemented by generating a voltage ramp at the TR/SS pin using an external capacitor which is charged by an internal constant current. Alternatively, driving the TR/SS pin with a signal source or resistive network provides a tracking function. Do not drive the TR/SS pin with a low impedance voltage source. See the Applications Information section for more details.

The LTM8063 contains a power good comparator which trips when the FB pin is at about 90% to 110% of its regulated value. The PG output is an open-drain transistor that is off when the output is in regulation, allowing an external resistor to pull the PG pin high. The PG signal is valid when V_{IN} is above 3.2V. If V_{IN} is above 3.2V and RUN is low, PG will drive low.

The LTM8063 is equipped with a thermal shutdown that inhibits power switching at high junction temperatures. The activation threshold of this function is above the maximum temperature rating to avoid interfering with normal operation, so prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device

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For most applications, the design process is straightforward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended, C_{IN}, C_{OUT}, R_{FB} and R_T values.
3. Apply the C_{FF} (from V_{OUT} to F_B) as required.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current is limited by junction temperature, the relationship between the input and output voltage magnitude and polarity and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

The maximum frequency (and attendant R_T value) at which the LTM8063 should be allowed to switch is given in Table 1 in the Maximum f_{SW} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the f_{SW} column. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

Table 1. Recommended Component Values and Configuration (T_A = 25°C)

V_{IN}	V_{OUT}	R_{FB} (kΩ)	C_{IN}[2]	C_{OUT}	C_{FF}	f_{SW}	R_T (kΩ)	MAX f_{SW}	MIN R_T (kΩ)
3.2 to 40	0.77V	Open	1µF 50V 0805 X5R	100µF 4V 0805 X5R	27pF	600kHz	73.2	600kHz	73.2
3.2 to 40	1.0V	845	1µF 50V 0805 X5R	100µF 4V 0805 X5R	10pF	700kHz	60.4	725kHz	59
3.2 to 40	1.2V	453	1µF 50V 0805 X5R	100µF 4V 0805 X5R		800kHz	52.3	850kHz	48.7
3.2 to 40	1.5V	267	1µF 50V 0805 X5R	100µF 4V 0805 X5R		800kHz	52.3	1MHz	41.2
3.2 to 40	1.8V	187	1µF 50V 0805 X5R	100µF 4V 0805 X5R		900kHz	47.5	1.2MHz	33.2
3.3 to 40V[1]	2.0V	154	1µF 50V 0805 X5R	100µF 4V 0805 X5R		1MHz	41.2	1.3MHz	29.4
3.8 to 40V[1]	2.5V	113	1µF 50V 0805 X5R	47µF 4V 0805 X5R		1.2MHz	33.2	1.6MHz	23.7
5 to 40V[1]	3.3V	75	1µF 50V 0805 X5R	47µF 4V 0805 X5R		1.2MHz	33.2	2MHz	18.2
6.5 to 40V[1]	5V	45.3	1µF 50V 0805 X5R	22µF 6.3V 0805 X5R		1.4MHz	27.4	2.2MHz	15.8
10.5 to 40V[1]	8V	26.7	1µF 50V 0805 X5R	10µF 10V 0805 X5R		1.8MHz	20.5	2.2MHz	15.8
18.5 to 40V[1]	12V	17.4	1µF 50V 0805 X5R	10µF 16V 0805 X7S		1.8MHz	20.5	2.2MHz	15.8
22 to 40V[1]	15V	13.7	1µF 50V 0805 X5R	10µF 25V 1206 X7R		2MHz	18.2	2.2MHz	15.8
3.2 to 36V[1]	–3.3V	75	1µF 50V 0805 X5R	47µF 4V 0805 X5R		1.2MHz	33.2	2MHz	18.2
3.2 to 35V[1]	–5V	45.3	1µF 50V 0805 X5R	22µF 6.3V 0805 X5R		1.4MHz	27.4	2.2MHz	15.8
3.2 to 32V[1]	–8V	26.7	1µF 50V 0805 X5R	10µF 10V 0805 X5R		1.8MHz	20.5	2.2MHz	15.8
3.2 to 28V[1]	–12V	17.4	1µF 50V 0805 X5R	10µF 16V 0805 X7S		1.8MHz	20.5	2.2MHz	15.8
3.2 to 25V[1]	–15V	13.7	1µF 50V 0805 X5R	10µF 25V 1206 X7R		2MHz	18.2	2.2MHz	15.8

1. The LTM8063 may be capable of lower input voltages but may skip switching cycles.
2. An input bulk capacitor is required

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Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

Ceramic capacitors are also piezoelectric. In Burst Mode operation, the LTM8063's switching frequency depends on the load current, and can excite a ceramic capacitor at audio frequencies, generating audible noise. Since the LTM8063 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear.

If this audible noise is unacceptable, use a high performance electrolytic capacitor at the output. It may also be a parallel combination of a ceramic capacitor and a low cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8063. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LTM8063 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Frequency Selection

The LTM8063 uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 2.2MHz by using a resistor tied from the RT pin to ground. Table 2 provides a list of R_T resistor values and their resultant frequencies.

Table 2. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.2	232
0.3	150
0.4	110
0.5	88.7
0.6	73.2
0.7	60.4
0.8	52.3
1.0	41.2
1.2	33.2
1.4	27.4
1.6	23.7
1.8	20.5
2.0	18.2
2.2	15.8

Operating Frequency Trade-Offs

It is recommended that the user apply the optimal R_T value given in Table 1 for the input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8063 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8063 if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

Maximum Load

The maximum practical continuous load that the LTM8063 can drive, while rated at 2A, actually depends upon both the internal current limit and the internal temperature.

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The internal current limit is designed to prevent damage to the LTM8063 in the case of overload or short-circuit. The internal temperature of the LTM8063 depends upon operating conditions such as the ambient temperature, the power delivered, and the heat sinking capability of the system. For example, if the LTM8063 is configured to regulate at 1.2V, it may continuously deliver 2.5A from $12V_{IN}$ if the ambient temperature is controlled to less than 55°C. This is higher than the 2A continuous rating. Please see the "Derating, V_{OUT} = 1.2V" curve in the Typical Performance Characteristics section. Similarly, if the output voltage is 15V and the ambient temperature is 100°C, the LTM8063 will deliver less than 100mA from $36V_{IN}$, which is less than the 2A continuous rating.

Load Sharing

The LTM8063 is not designed to load share.

Burst Mode Operation

To enhance efficiency at light loads, the LTM8063 automatically switches to Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LTM8063 delivers single cycle bursts of current to the output capacitor followed by sleep periods where most of the internal circuitry is powered off and energy is delivered to the load by the output capacitor. During the sleep time, V_{IN} quiescent current is greatly reduced, so, as the load current decreases towards a no load condition, the percentage of time that the LTM8063 operates in sleep mode increases and the average input current is greatly reduced, resulting in higher light load efficiency.

Burst Mode operation is enabled by tying SYNC to GND.

Minimum Input Voltage

The LTM8063 is a step-down converter, so a minimum amount of headroom is required to keep the output in regulation. Keep the input above 3.2V to ensure proper operation. Voltage transients or ripple valleys that cause the input to fall below 3.2V may turn off the LTM8063.

Output Voltage Tracking and Soft-Start

The LTM8063 allows the user to adjust its output voltage ramp rate by means of the TR/SS pin. An internal 2µA pulls up the TR/SS pin to about 2.4V. Putting an external capacitor on TR/SS enables soft starting the output to reduce current surges on the input supply. During the soft-start ramp the output voltage will proportionally track the TR/SS pin voltage. For output tracking applications, TR/SS can be externally driven by another voltage source. From 0V to 0.77V, the TR/SS voltage will override the internal 0.77V reference input to the error amplifier, thus regulating the FB pin voltage to that of the TR/SS pin. When TR/SS is above 0.77V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. The TR/SS pin may be left floating if the function is not needed.

An active pull-down circuit is connected to the TR/SS pin which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the RUN pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Pre-Biased Output

As discussed in the Output Voltage Tracking and Soft-Start section, the LTM8063 regulates the output to the FB voltage determined by the TR/SS pin whenever TR/SS is less than 0.77V. If the LTM8063 output is higher than the target output voltage, the LTM8063 will attempt to regulate the output to the target voltage by returning a small amount of energy back to the input supply. If there is nothing loading the input supply, its voltage may rise. Take care that it does not rise so high that the input voltage exceeds the absolute maximum rating of the LTM8063.

Frequency Foldback

The LTM8063 is equipped with frequency foldback which acts to reduce the thermal and energy stress on the internal power elements during a short circuit or output overload condition. If the LTM8063 detects that the output has fallen out of regulation, the switching frequency is reduced as a function of how far the output is below the target voltage. This in turn limits the amount of energy that can

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be delivered to the load under fault. During the start-up time, frequency foldback is also active to limit the energy delivered to the potentially large output capacitance of the load. When a clock is applied to the SYNC pin, the SYNC pin is floated or held high, the frequency foldback is disabled, and the switching frequency will slow down only during overcurrent conditions.

Synchronization

To select low ripple Burst Mode operation, tie the SYNC pin below about 0.4V (this can be ground or a logic low output). To synchronize the LTM8063 oscillator to an external frequency, connect a square wave (with about 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.5V.

The LTM8063 will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will pulse skip to maintain regulation. The LTM8063 may be synchronized over a 200kHz to 2.2MHz range. The R_T resistor should be chosen to set the switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R_T should be selected for 500kHz.

For some applications it is desirable for the LTM8063 to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. The first is that the clock stays awake at all times and all switching cycles are aligned to the clock. The second is that full switching frequency is reached at lower output load than in Burst Mode operation. These two differences come at the expense of increased quiescent current. To enable pulse-skipping mode, the SYNC pin is floated.

The LTM8063 features spread spectrum operation to further reduce EMI/EMC emissions. To enable spread spectrum operation, apply between 2.9V and 4.2V to the SYNC pin. In this mode, triangular frequency modulation is used to vary the switching frequency between the value programmed by R_T to about 20% higher than that value. The modulation frequency is about 3kHz. For example, when the LTM8063 is programmed to 2MHz, the frequency will vary from 2MHz to 2.4MHz at a 3kHz rate. When spread spectrum operation is selected, Burst Mode operation is disabled, and the part will run in pulse-skipping mode.

The LTM8063 does not operate in forced continuous mode regardless of SYNC signal.

Negative Output

The LTM8063 is capable of generating a negative output voltage by connecting its V_{OUT} to system GND and the LTM8063 GND to the negative voltage rail. An example of this is shown in the Typical Applications section. The most versatile way to generate a negative output is to use a dedicated regulator that was designed to generate a negative voltage, but using a buck regulator like the LTM8063 to generate a negative voltage is a simple and cost effective solution, as long as certain restrictions are kept in mind.

Figure 1 shows a typical negative output voltage application. Note that LTM8063 V_{OUT} is tied to system GND and input power is applied from V_{IN} to LTM8063 V_{OUT}. As a result, the LTM8063 is not behaving as a true buck regulator, and the maximum output current depends upon the input voltage. In the example shown in the Typical Applications section, there is an attending graph that shows how much current the LTM8063 can deliver for given input voltages.

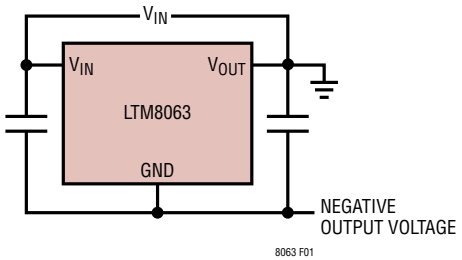


Figure 1. The LTM8063 Can Be Used to Generate a Negative Voltage

Note that this configuration requires that any load current transient will directly impress the transient voltage onto the LTM8063 GND, as shown in Figure 2, so fast load transients can disrupt the LTM8063's operation or even cause damage.

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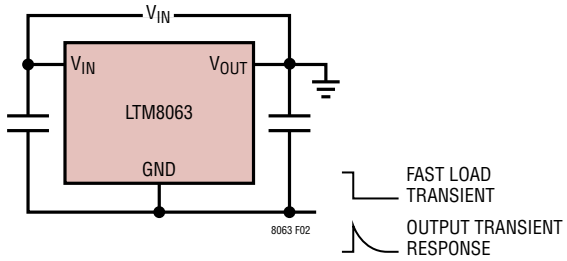


Figure 2. Any Output Voltage Transient Appears on LTM8063 GND

The C_{IN} and C_{OUT} capacitors in Figure 3 form an AC divider at the negative output voltage node. If V_{IN} is hot-plugged or rises quickly, the resultant V_{OUT} will be a positive transient, which may be unhealthy for the application load. An anti-parallel Schottky diode may be able to prevent this positive transient from damaging the load. The location of this Schottky diode is important. For example, in a system where the LTM8063 is far away from the load, placing the Schottky diode closest to the most sensitive load component may be the best design choice. Carefully evaluate whether the negative buck configuration is suitable for the application.

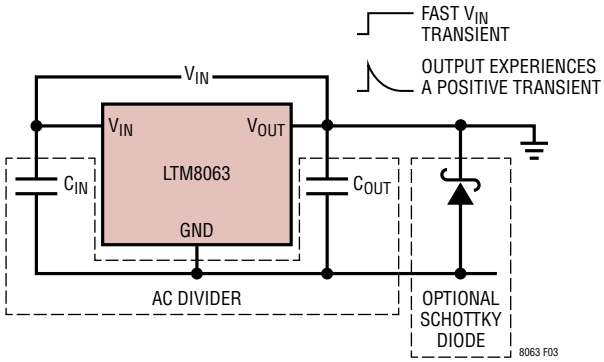


Figure 3. A Schottky Diode Can Limit the Transient Caused by a Fast Rising V_{IN} to Safe Levels

Shorted Input Protection

Care needs to be taken in systems where the output is held high when the input to the LTM8063 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode ORed with the LTM8063's output. If the V_{IN} pin is allowed to float and the RUN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LTM8063's internal circuitry pulls its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUN pin, the internal current drops to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, parasitic diodes inside the LTM8063 can pull large currents from the output through the V_{IN} pin. Figure 4 shows a circuit that runs only when the input voltage is present and that protects against a shorted or reversed input.

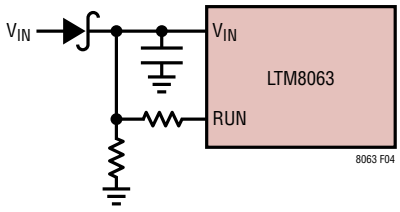


Figure 4. The Input Diode Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LTM8063 Runs Only When the Input Is Present

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8063. The LTM8063 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 5 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

A few rules to keep in mind are:

1. Place C_{FF}, R_{FB} and R_T as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8063.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM8063.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground currents flow directly adjacent to or underneath the LTM8063.

APPLICATIONS INFORMATION

5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8063.

6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 5. The LTM8063 can benefit from the heat-sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

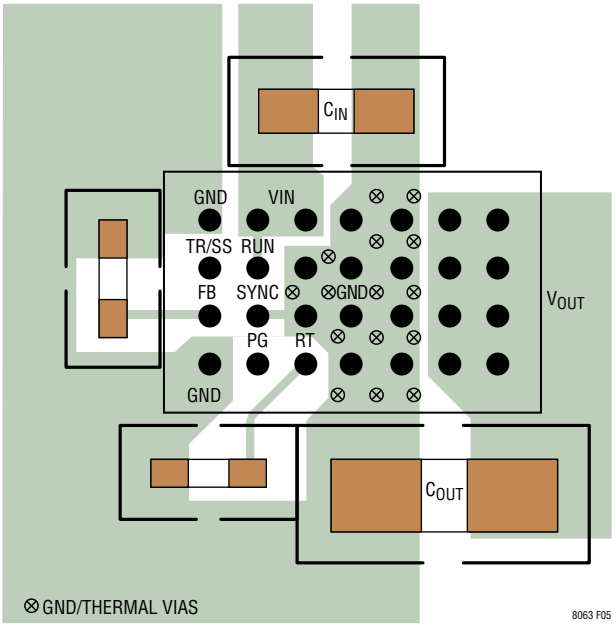


Figure 5. Layout Showing Suggested External Components, GND Plane and Thermal Vias

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8063. However, these capacitors can cause problems if the LTM8063 is plugged into a live supply (see Linear Technology Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8063 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8063's rating and damaging the part. If the input supply is poorly controlled or the LTM8063 is hot-plugged into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is add an electrolytic bulk cap to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit.

Thermal Considerations

The LTM8063 output current may need to be derated if it is required to operate in a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The derating curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by the LTM8063 mounted to a 58cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use FEA (Finite Element Analysis) to predict thermal performance. To that end, Page 2 of the data sheet typically gives four thermal coefficients:

θ_{JA} – Thermal resistance from junction to ambient

$\theta_{JCbottom}$ – Thermal resistance from junction to the bottom of the product case

θ_{JCtop} – Thermal resistance from junction to top of the product case

θ_{JB} – Thermal resistance from junction to the printed circuit board.

APPLICATIONS INFORMATION

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased below:

θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

$\theta_{JCbottom}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JB} is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule regulator. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in the product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A simplified graphical representation of these thermal resistances is given in Figure 6. The blue resistances are contained within the µModule regulator, and the green are outside.

The die temperature of the LTM8063 must be lower than the maximum rating, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8063. The bulk of the heat flow out of the LTM8063 is through the bottom of the package and the pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

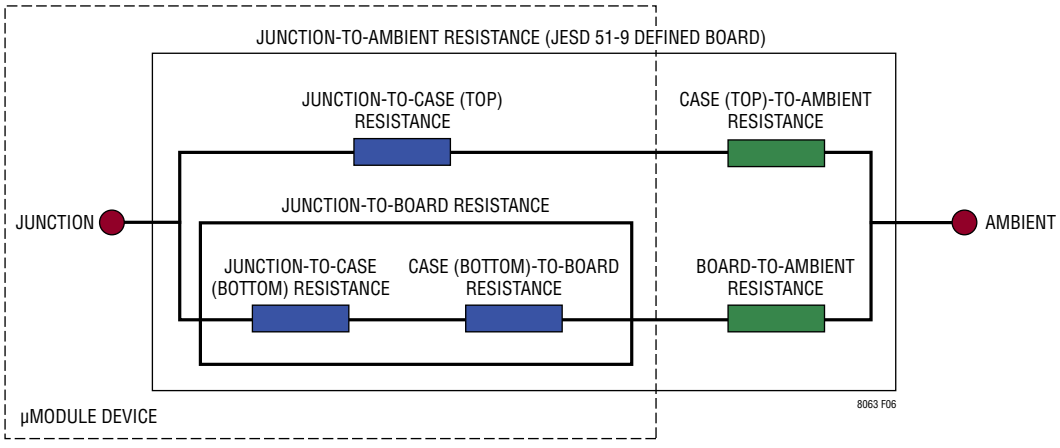
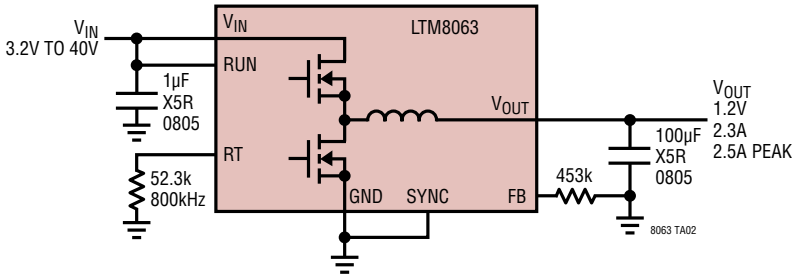


Figure 6. Simplified Graphical Representation of the Thermal Resistance Between the Device Junction and Ambient

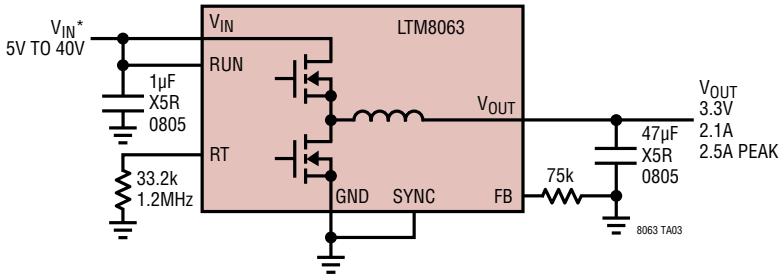
TYPICAL APPLICATIONS

1.2V_{OUT} from 3.2V_{IN} to 40V_{IN} Step-Down Converter



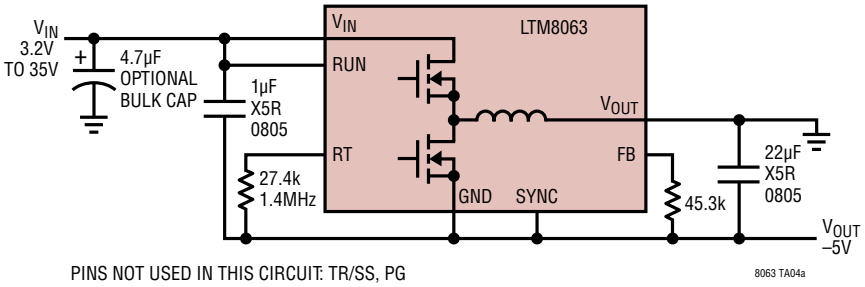
PINS NOT USED IN THIS CIRCUIT: TR/SS, PG

3.3V_{OUT} from 5V_{IN} to 40V_{IN} Step-Down Converter



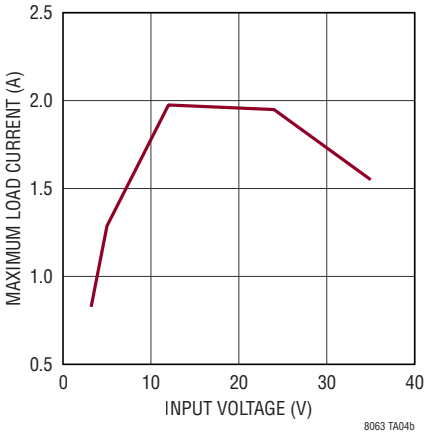
PINS NOT USED IN THIS CIRCUIT: TR/SS, PG
*V_{IN} MAY BE AS LOW AS 3.6V WITH OFF-CYCLE SKIPPING

–5V_{OUT} from 3.2V_{IN} to 35V_{IN} Positive to Negative Converter

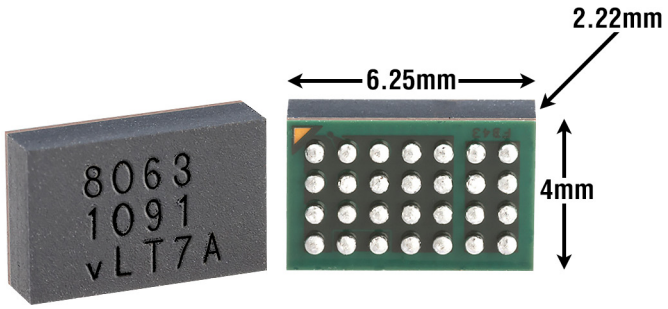


PINS NOT USED IN THIS CIRCUIT: TR/SS, PG

Maximum Load Current vs V_{IN}



PACKAGE PHOTO



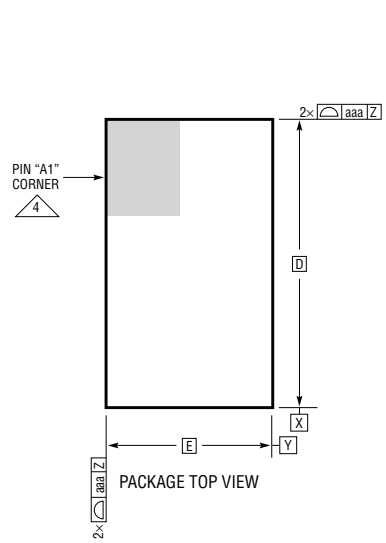
PACKAGE DESCRIPTION

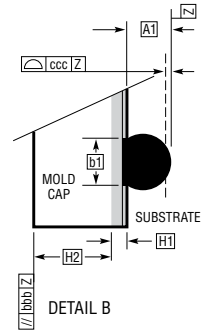
Table 3. LTM8063 Pinout (Sorted by Pin Number)

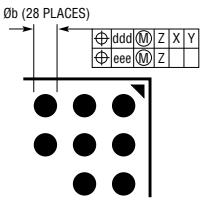
PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME
A1	GND	B1	PG	C1	RT	D1	GND	E1	GND	F1	V_{OUT}	G1	V_{OUT}
A2	FB	B2	SYNC	C2	GND	D2	GND	E2	GND	F2	V_{OUT}	G2	V_{OUT}
A3	TR/SS	B3	RUN	C3	GND	D3	GND	E3	GND	F3	V_{OUT}	G3	V_{OUT}
A4	GND	B4	V_{IN}	C4	V_{IN}	D4	GND	E4	GND	F4	V_{OUT}	G4	V_{OUT}

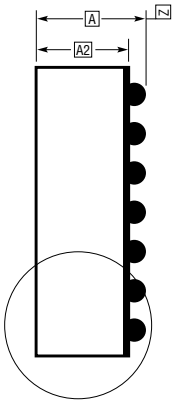
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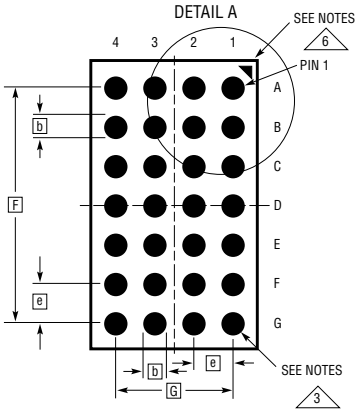
BGA Package
28-Lead (6.25mm × 4mm × 2.22mm)
(Reference LTC DWG # 05-08-1517 Rev A)

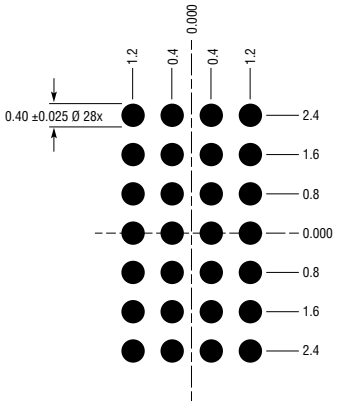






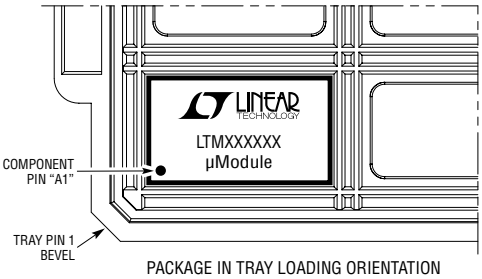






DIMENSIONS				
SYMBOL	**MIN**	**NOM**	**MAX**	**NOTES**
A	2.02	2.22	2.42	
A1	0.30	0.40	0.50	BALL HT
A2	1.72	1.82	1.92	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		6.25		
E		4.00		
e		0.80		
F		4.80		
G		2.40		
H1	0.27	0.32	0.37	SUBSTRATE THK
H2	1.45	1.50	1.55	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 28				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



BGA 28 0517 REV A

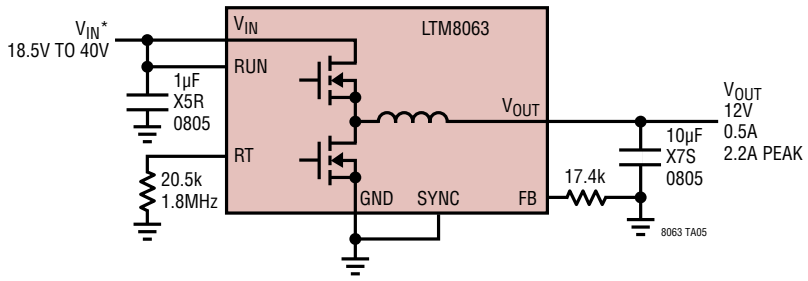
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	02/18	Initial cap sentence (e.g.: Update to curve G04 in the Typical Performance Characteristics section).	4, 5
B	02/18	Changed I_{OUT} from 2.5A to 2A for Output Voltage Ripple test.	3
		Added V_{IN} = 8V to Switching Frequency consideration.	3
		Changed 2.5A to 2A in first paragraph.	15
		Corrected pin name of pin B2 from FB to PG.	18
C	06/19	Changed θ_{JA} from 36.5°C/W to 41.5°C/W.	2
		Changed $\theta_{JCbottom}$ from 10.4°C/W to 13°C/W.	2
		Changed θ_{JCtop} from 37.1°C/W to 52.4°C/W.	2
		Changed θ_{JB} from 10.8°C/W to 16.3°C/W.	2
		Added LTM8063IY SnPb to Order Information.	2
		Changed V_{IN} transient to rising edge.	17

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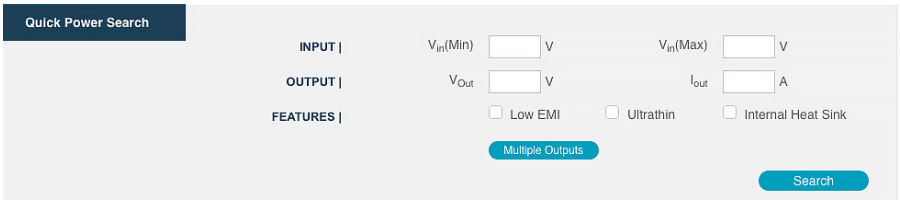
TYPICAL APPLICATION

12V_{OUT} from 18.5V_{IN} to 40V_{IN} Step Down Converter



PINS NOT USED IN THIS CIRCUIT: TR/SS, PG
*V_{IN} MAY BE AS LOW AS 12.6V WITH OFF-CYCLE SKIPPING

DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8053	40V, 3.5A Step-Down µModule Regulator	3.4V ≤ V_{IN} ≤ 40V. 0.97V ≤ V_{OUT} ≤ 15V. 6.25mm x 9mm x 3.32mm BGA Package.
LTM8032	36V, 2A Low EMI Step-Down µModule Regulator	3.6V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 10V. EN55022B Compliant.
LTM8033	36V, 3A Low EMI Step-Down µModule Regulator	3.6V ≤ V_{IN} ≤ 36V. 0.8V ≤ V_{OUT} ≤ 24V. EN55022B Compliant.
LTM8026	36V, 5A CVCC Step-Down µModule Regulator	6V ≤ V_{IN} ≤ 36V. 1.2V ≤ V_{OUT} ≤ 24V. Constant Voltage Constant Current Operation.
LTM4613	36V, 8A Low EMI Step-Down µModule Regulator	5V ≤ V_{IN} ≤ 36V. 3.3V ≤ V_{OUT} ≤ 15V. EN55022B Compliant.
LTM8027	60V, 4A Step-Down µModule Regulator	4.5V ≤ V_{IN} ≤ 60V, 2.5V ≤ V_{OUT} ≤ 24V.
LTM8050	58V, 2A Step-Down µModule Regulator	3.6V ≤ V_{IN} ≤ 58V, 0.8V ≤ V_{OUT} ≤ 24V.
LTM8003	3.5A Version of LTM8002, 40V, 3.5A, I_Q = 25µA FMEA Compliant	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 18V, 6.25mm × 9mm × 3.32 BGA Package.
LTM8065	40V, 2.5A Silent Switcher Step-Down µModule Regulator	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 18V, 6.25mm × 6.25mm × 2.32mm BGA Package.

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