36V_{IN}, UltraFast, Low Output Noise 5A µModule Regulator

FEATURES

- **High Performance 5A Linear Regulator with Switching Step-Down Converter for High Efficiency**
- **Digitally Programmable V_{OUT}: 0.8V to 1.8V**
- **Input Voltage Range: 6V to 36V**
- **Very Tight Tolerance Over Temperature, Line, Load and Transient Response**
- **Low Output Noise: 40µV_{RMS} (10Hz to 100kHz)**
- **Parallel Multiple Devices for 10A or More**
- **Accurate Programmable Current Limit to Allow Asymmetric Power Sharing**
- Analog Output Margining: ±10% Range
- Synchronization Input
- Stable with Low ESR Ceramic Output Capacitors
- 15mm × 15mm × 4.92mm Surface Mount BGA Package
- SnPb or RoHS Compliant Finish

APPLICATIONS

- FPGA and DSP Supplies
- High Speed I/O
- ASIC and Microprocessor Supplies
- Servers and Storage Devices

DESCRIPTION

The LTM®8028 is a 36V_{IN}, 5A µModule® regulator, consisting of an UltraFast™ 5A linear regulator preceded by a high efficiency switching regulator. In addition to providing tight output regulation, the linear regulator automatically controls the output voltage of the switcher to provide optimal efficiency and headroom for dynamic response.

The output voltage is digitally selectable in 50mV increments over a 0.8V to 1.8V range. An analog margining function allows the user to adjust system output voltage over a continuous ±10% range, and a single-ended feedback sense line may be used to mitigate IR drops due to parasitic resistance.

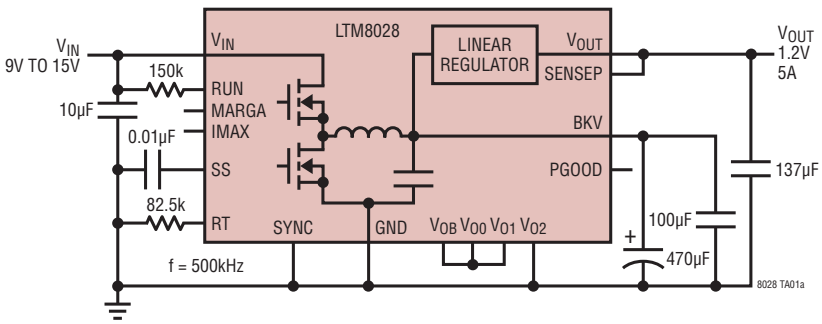
The LTM8028 is packaged in a compact (15mm × 15mm × 4.92mm) overmolded ball grid array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8028 is available with SnPb (BGA) or RoHS compliant terminal finish.

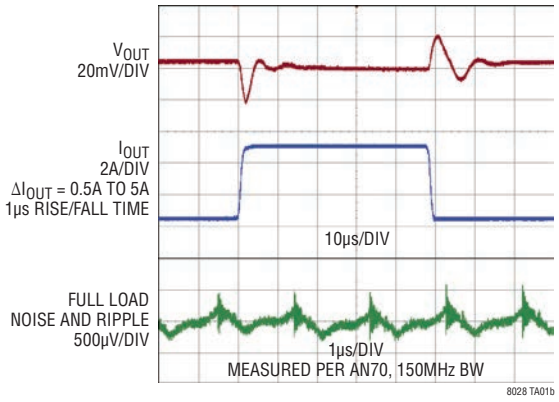
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TYPICAL APPLICATION

Low Output Noise, 1.2V, 5A µModule Regulator



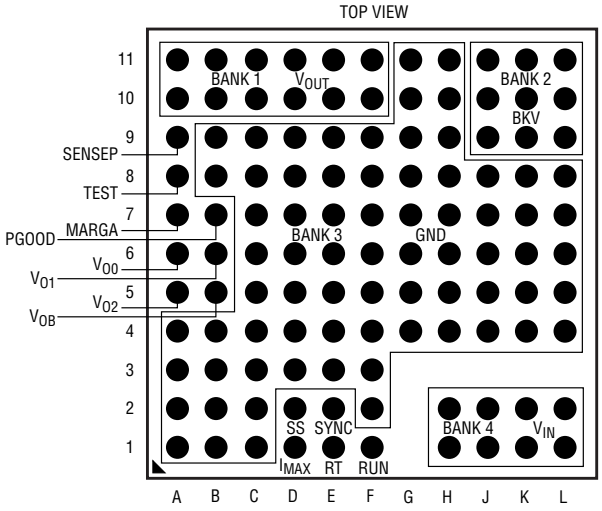


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 4)

V_{IN} 40V
V_{OUT}.....3V
RUN, SS, SYNC 6V
Current Into RUN 100µA
V_{OB}, V_{O0}, V_{O1}, V_{O2}, TEST,
PGOOD, SENSEP, MARGA.....4V
RT, BKV, I_{MAX} 3V
Maximum Operating Junction Temperature
(Note 2)..... 125°C
Peak Solder Reflow Body Temperature ..... 245°C
Maximum Storage Temperature..... 125°C

PIN CONFIGURATION



BGA PACKAGE
114 PADS (15mm × 15mm × 4.92mm)
T_{JMAX} = 125°C, θ_{JA} = 17.7°C/W,
θ_{JB} = 6.0°C/W, θ_{JCtop} = 15°C/W,
$\theta_{JCbottom}$ = 6.0°C/W

θ VALUES DETERMINED PER JEDEC 51-9, 51-12
WEIGHT = 1.8 GRAMS

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE			
LTM8028EY#PBF	SAC305 (RoHS)	LTM8028Y	e1	BGA	3	–40°C to 125°C
LTM8028IY#PBF	SAC305 (RoHS)	LTM8028Y	e1	BGA	3	–40°C to 125°C
LTM8028IY	SnPb (63/37)	LTM8028Y	e0	BGA	3	–40°C to 125°C
LTM8028MPY#PBF	SAC305 (RoHS)	LTM8028Y	e1	BGA	3	–55°C to 125°C
LTM8028MPY	SnPb (63/37)	LTM8028Y	e0	BGA	3	–55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Pb-free and Non-Pb-free Part Markings:
  www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures:
  www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings:
  www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, RUN = 3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage					6	V
Output DC Voltage		●	0.788	0.8	0.812	V
		●	0.985	1.0	1.015	V
		●	1.182	1.2	1.218	V
		●	1.477	1.5	1.523	V
		●	1.773	1.8	1.827	V
Output DC Current	V_{OUT} = 1.8V				5	A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, RUN = 3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current Into V_{IN}	RUN = 0V No load			1 35		µA mA
Line Regulation	6V < V_{IN} < 36V, I_{OUT} = 10mA	●			1	mV
Load Regulation	0.01A < I_{OUT} < 5A, V_{OUT} = 0.8V, BKV = 1.05V, RUN = 0V	 ●		–1.5	–3 –5.5	mV mV
	0.01A < I_{OUT} < 5A, V_{OUT} = 1.0V, BKV = 1.25V, RUN = 0V	 ●		–2	–4 –7.5	mV mV
	0.01A < I_{OUT} < 5A, V_{OUT} = 1.2V, BKV = 1.45V, RUN = 0V	 ●		–2	–4 –7.5	mV mV
	0.01A < I_{OUT} < 5A, V_{OUT} = 1.5V, BKV = 1.75V, RUN = 0V	 ●		–2.5	–5 –9	mV mV
	0.01A < I_{OUT} < 5A, V_{OUT} = 1.8V, BKV = 2.05V, RUN = 0V	 ●		–3	–7 –13	mV mV
Sense Pin Current	V_{OUT} = 0.8V V_{OUT} = 1.8V			50 300		µA µA
Switching Frequency	R_T = 40.2k R_T = 200k			1000 200		kHz kHz
RUN Pin Current	RUN = 1.45V			5.5		µA
RUN Threshold Voltage (Falling)		●	1.49	1.55	1.61	V
RUN Input Hysteresis				130		mV
I_{MAX} Pin Current	I_{MAX} = 0.75V			125		µA
I_{MAX} Current Limit Accuracy	I_{MAX} = 1.5V I_{MAX} = 0.75V		5.0 2.20		6.1 3.6	A A
SS Pin Current				11		µA
SYNC Input Threshold	f_{SYNC} = 500kHz		0.6		1.3	V
SYNC Bias Current	SYNC = 0V				1	µA
V_{OB} Voltage				3.3		V
V_{Ox} Input Low Threshold	V_{OB} = 3.3V	●			0.25	V
V_{Ox} Input High Threshold	V_{OB} = 3.3V	●	3.05			V
V_{Ox} Input Z Range	V_{OB} = 3.3V	●	0.75		2.4	V
V_{Ox} Input Current High					40	µA
V_{Ox} Input Current Low					40	µA
MARGA Pin Current	MARGA = 0V			3.5		µA
PGOOD Threshold	$V_{OUT(NOMINAL)}$ = 1.0V, V_{OUT} Rising $V_{OUT(NOMINAL)}$ = 1.0V, V_{OUT} Falling			0.9 0.85		V V
Output Voltage Noise (Note 3)	V_{OUT} = 1.8V, C_{OUT} = 137µF, 5A Load, BW = 10Hz to 100kHz			40		$µV_{RMS}$

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

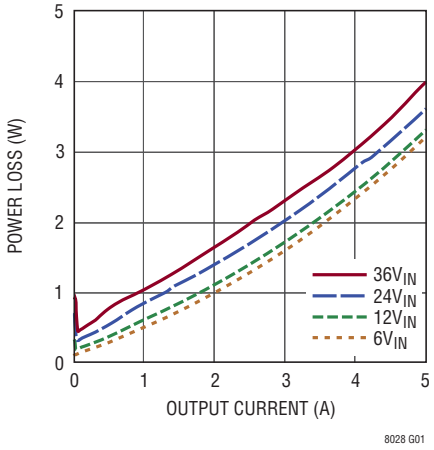
Note 2: The LTM8028E is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8028I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8028MP is guaranteed to meet specifications over the full –55°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: Guaranteed by design, characterization and correlation with statistical process controls.

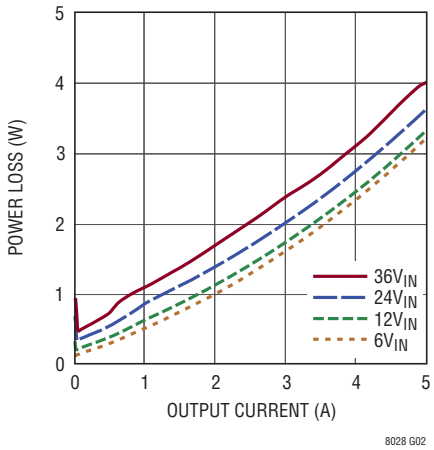
Note 4: Unless otherwise stated, the absolute minimum voltage is zero.

TYPICAL PERFORMANCE CHARACTERISTICS

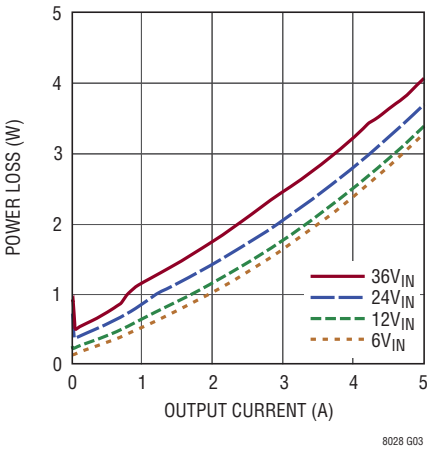
Power Loss vs Output Current, 0.8V_{OUT}



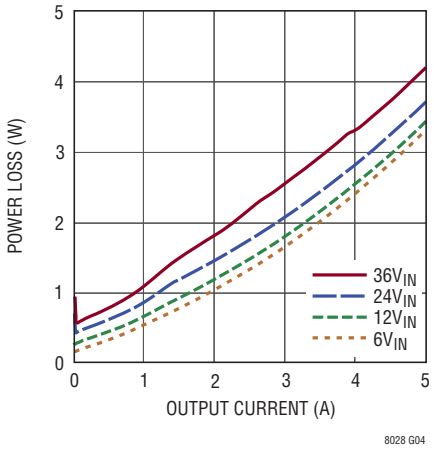
Power Loss vs Output Current, 1V_{OUT}



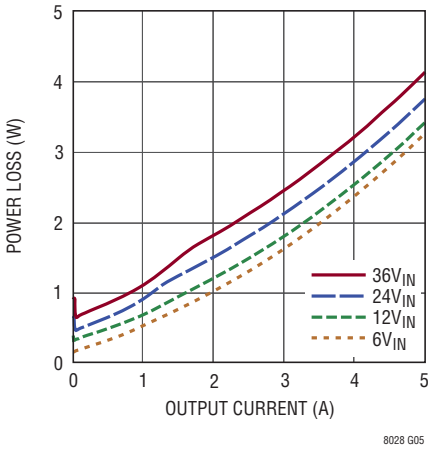
Power Loss vs Output Current, 1.2V_{OUT}



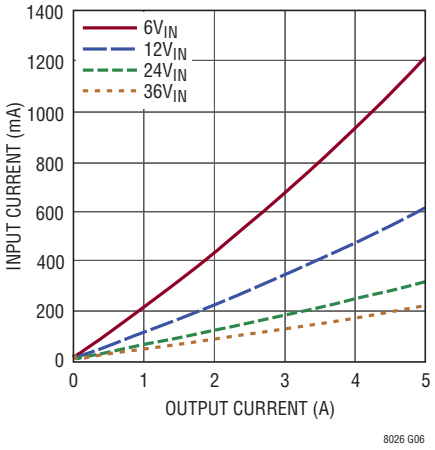
Power Loss vs Output Current, 1.5V_{OUT}



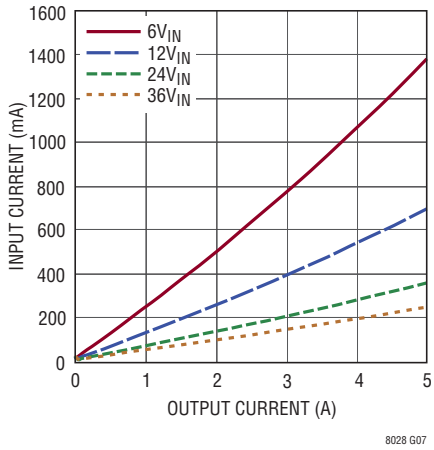
Power Loss vs Output Current, 1.8V_{OUT}



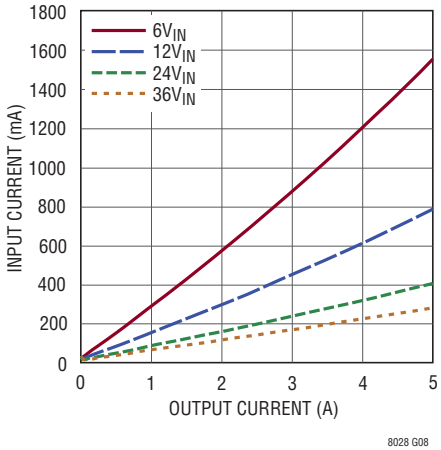
Input Current vs Output Current, 0.8V_{OUT}



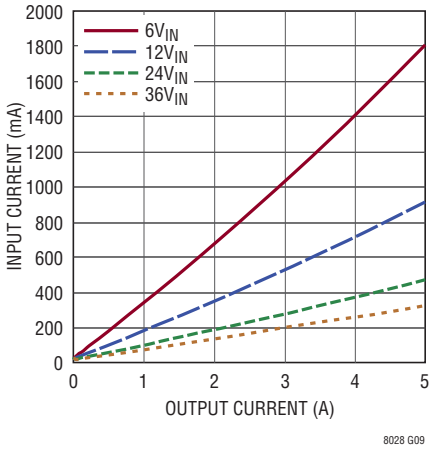
Input Current vs Output Current, 1V_{OUT}



Input Current vs Output Current, 1.2V_{OUT}

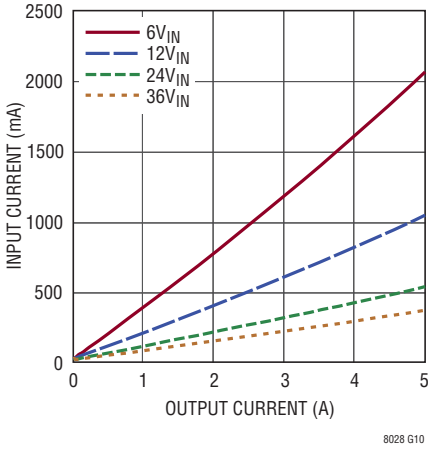


Input Current vs Output Current, 1.5V_{OUT}

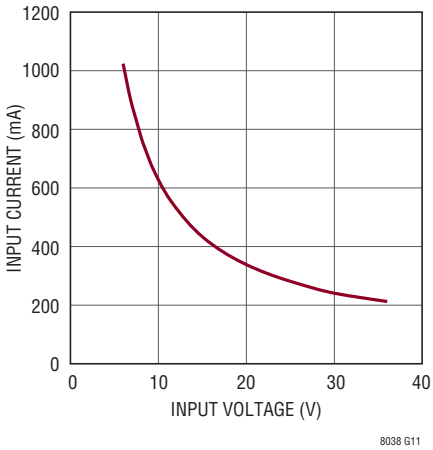


TYPICAL PERFORMANCE CHARACTERISTICS

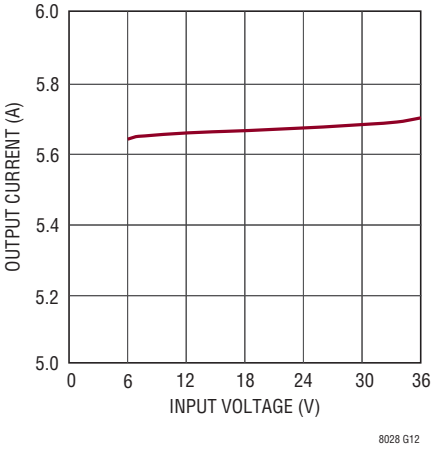
Input Current vs Output Current, 1.8V_{OUT}



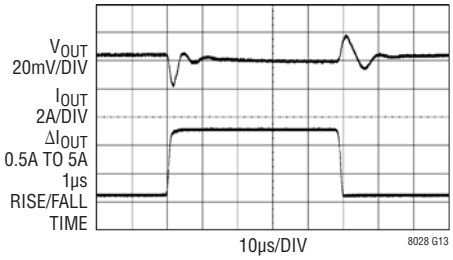
Input Current vs Input Voltage, Output Shorted



Output Current vs Input Voltage, Output Shorted

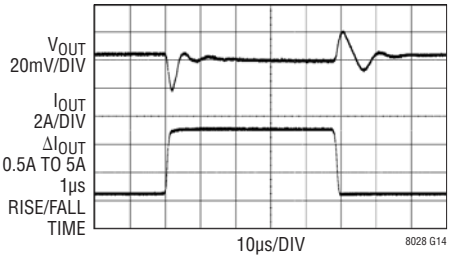


Transient Response, Demo Board, 1V



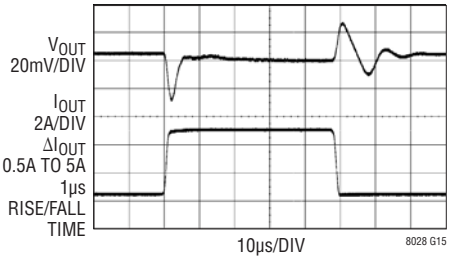
C_{OUT} = 100µF + 22µF + 10µF + 4.7µF

Transient Response, Demo Board, 1.2V



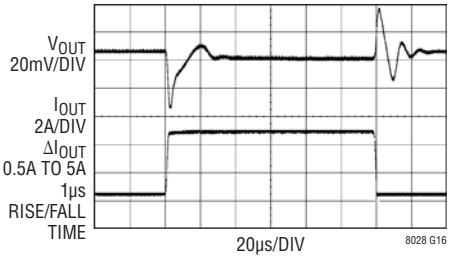
C_{OUT} = 100µF + 22µF + 10µF + 4.7µF

Transient Response, Demo Board, 1.5V



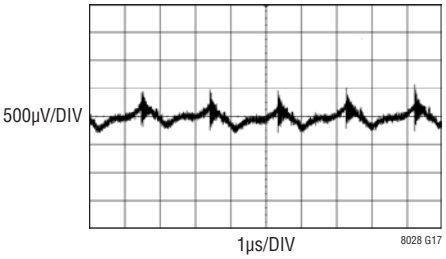
C_{OUT} = 100µF + 22µF + 10µF + 4.7µF

Transient Response, Demo Board, 1.8V



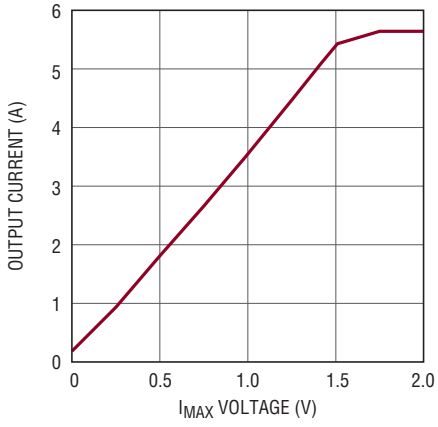
C_{OUT} = 100µF + 22µF + 10µF + 4.7µF

Output Noise, 1.8V_{OUT}



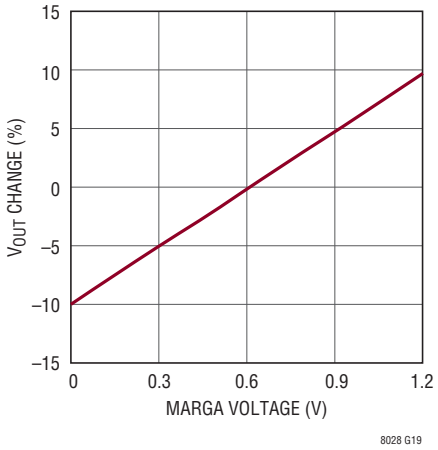
MEASURED WITH HP461A AMPLIFIER
(150MHz BW) AT J5 BNC CONNECTOR
ON DC1738 DEMO BOARD
f_{SW} = 500kHz
C_{OUT} = 137µF
5A LOAD

Output Current vs I_{MAX} Voltage, 12V_{IN}

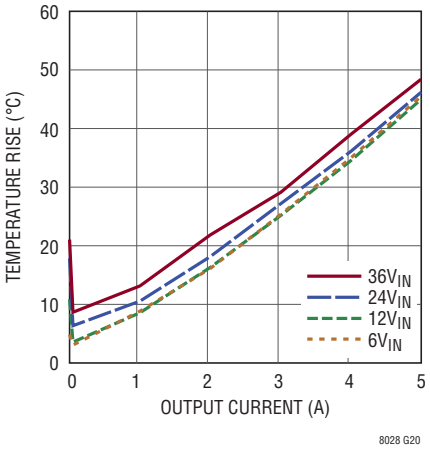


TYPICAL PERFORMANCE CHARACTERISTICS

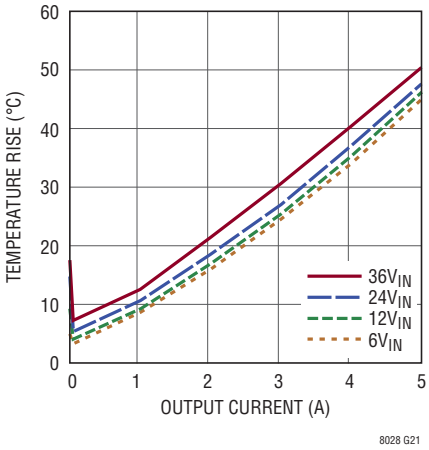
Output Voltage Change vs MARGA Voltage, 1V_{OUT}



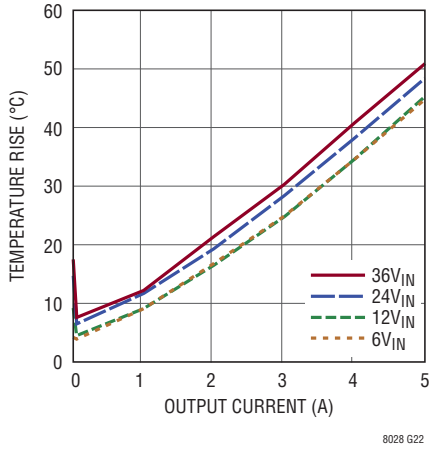
Temperature Rise vs Output Current, 0.8V_{OUT}



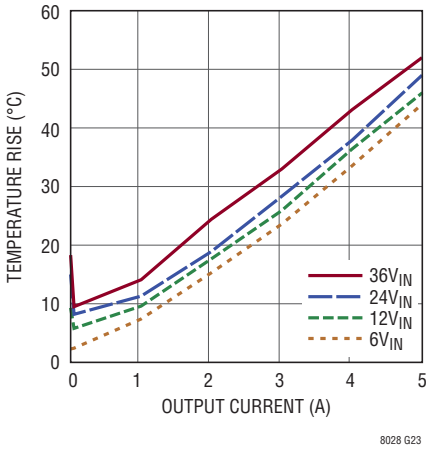
Temperature Rise vs Output Current, 1V_{OUT}



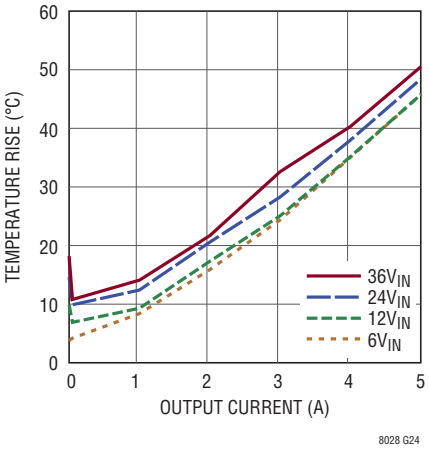
Temperature Rise vs Output Current, 1.2V_{OUT}



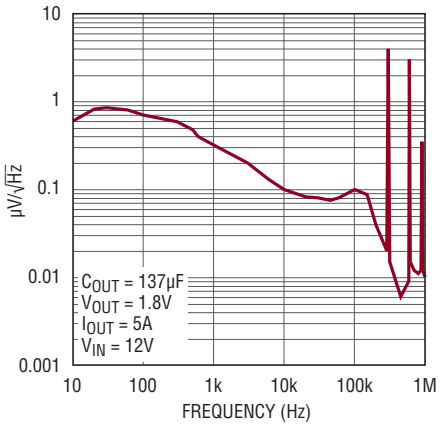
Temperature Rise vs Output Current, 1.5V_{OUT}



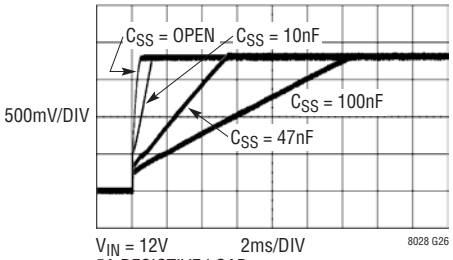
Temperature Rise vs Output Current, 1.8V_{OUT}



Output Noise Spectral Density



Soft-Start Waveform vs C_{SS}



PIN FUNCTIONS

V_{OUT} (Bank 1): Power Output Pins. Apply the output filter capacitor and the output load between these and the GND pins.

BKV (Bank 2): Buck Regulator Output. Apply the step-down regulator's bulk capacitance here (refer to Table 1). Do not connect this to the load. Do not drive a voltage into BKV.

GND (Bank 3): Tie these GND pins to a local ground plane below the LTM8028 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8028 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details.

V_{IN} (Bank 4): The V_{IN} pin supplies current to the LTM8028's internal regulator and to the internal power switch. This pin must be locally bypassed with an external, low ESR capacitor; see Table 1 for recommended values.

V_{O0}, V_{O1}, V_{O2} (Pin A6, Pin B6, Pin A5): Output Voltage Select. These three-state pins combine to select a nominal output voltage from 0.8V to 1.8V in increments of 50mV. See Table 2 in the Applications Information section that defines the V_{O2}, V_{O1} and V_{O0} settings versus V_{OUT}.

MARGA (Pin A7): Analog Margining: This pin margins the output voltage over a continuous analog range of ±10%. Tying this pin to GND adjusts output voltage by –10%. Driving this pin to 1.2V adjusts output voltage by 10%. A voltage source or a voltage output DAC is ideal for driving this pin. If the MARGA function is not used, either float this pin or terminate with a 1nF capacitor to GND.

TEST (Pin A8): Factory Test. Leave this pin open.

SENSEP (Pin A9): Kelvin Sense for V_{OUT}. The SENSEP pin is the inverting input to the error amplifier. Optimum regulation is obtained when the SENSEP pin is connected to the V_{OUT} pins of the regulator. In critical applications, the resistance of PCB traces between the regulator and the load can cause small voltage drops, creating a load regulation error at the point of load. Connecting the SENSEP pin at the load instead of directly to V_{OUT} eliminates this voltage error. The SENSEP pin input bias current depends on the selected output voltage. SENSEP pin input current varies from 50µA typically at V_{OUT} = 0.8V to 300µA typically at V_{OUT} = 1.8V. SENSEP must be connected to V_{OUT}, either locally or remotely.

V_{OB} (Pin B5): Bias for V_{O0}, V_{O1}, V_{O2}. This is a 3.3V source to conveniently pull up the V_{O0}, V_{O1}, V_{O2} pins, if desired. If not used, leave this pin floating.

PGOOD (Pin B7): Power Good. Open drain signal that will be high impedance if:

- The output rises above 90% of the target voltage
- The output stays above 85% of target voltage
- The output linear regulator does not overheat

Please see the Application Information section for more details. If not used, tie PGOOD to GND.

I_{MAX} (Pin D1): Sets the Maximum Output Current. Connect a resistor/ NTC thermistor network to the I_{MAX} pin to reduce the maximum regulated output current of the LTM8028 in response to temperature. This pin is internally pulled up to 2V through a 10k resistor, and the control voltage range is 0V to 1.5V.

SS (Pin D2): The Soft-Start Pin. Place an external capacitor to ground to limit the regulated current during start-up conditions. The soft-start pin has an 11µA charging current.

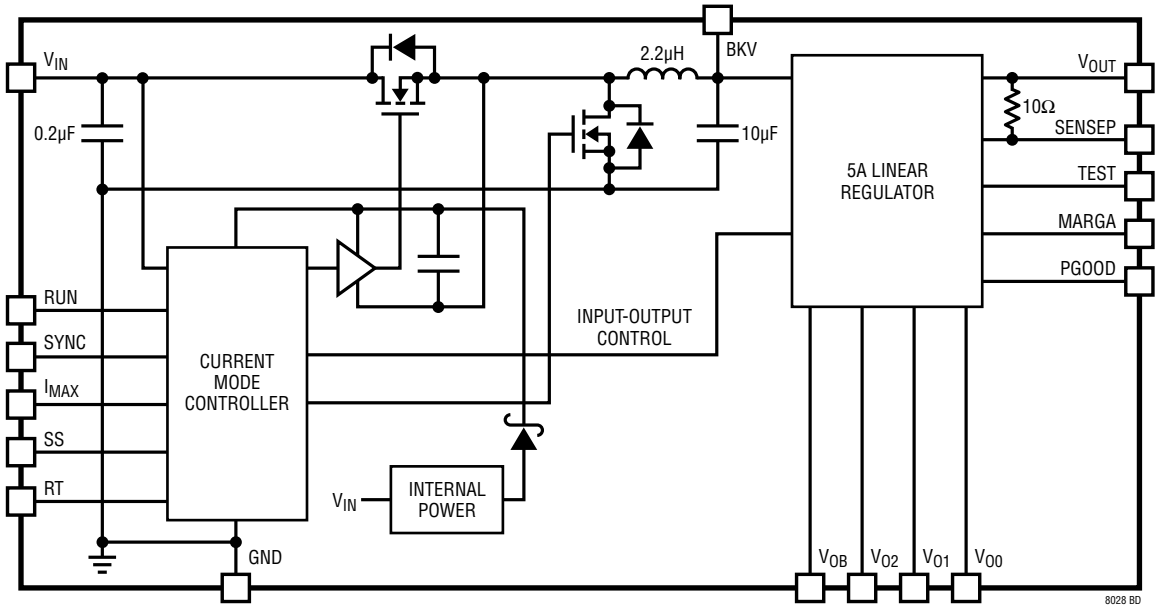
RT (Pin E1): The RT pin is used to program the switching frequency of the LTM8028's buck regulator by connecting a resistor from this pin to ground. The Applications Information section of the data sheet includes a table to determine the resistance value based on the desired switching frequency. When using the SYNC function, set the frequency to be 20% lower than the SYNC pulse frequency. Do not leave this pin open.

PIN FUNCTIONS

SYNC (Pin E2): Frequency Synchronization Pin. This pin allows the switching frequency to be synchronized to an external clock. The RT resistor should be chosen to operate the internal clock at 20% slower than the SYNC pulse frequency. This pin should be grounded when not in use. Do not leave this pin floating. When laying out the board, avoid noise coupling to or from the SYNC trace. See the Synchronization section in Applications Information.

RUN (Pin F1): The RUN pin acts as an enable pin and turns off the internal circuitry at 1.55V. The pin does not have any pull-up or pull-down, requiring a voltage bias for normal part operation. The RUN pin is internally clamped, so it may be pulled up to a voltage source that is higher than the absolute maximum voltage of 6V, provided the pin current does not exceed 100µA.

BLOCK DIAGRAM



OPERATION

Current generation FPGA and ASIC processors place stringent demands on the power supplies that power the core, I/O and transceiver channels. Power supplies that power these processors have demanding output voltage specifications, especially at low voltages, where they require tight tolerances, small transient response excursions, low noise and high bandwidth to achieve the lowest bit-error rates. This can be accomplished with some high performance linear regulators, but this can be inefficient for high current and step-down ratios.

The LTM8028 is a 5A high efficiency, UltraFast transient response linear regulator. It integrates a buck regulator with a high performance linear regulator, providing a precisely regulated output voltage digitally programmable from 0.8V to 1.8V. As shown in the Block Diagram, the LTM8028 contains a current mode controller, power switches, power inductor, linear regulator, and a modest amount of capacitance. To achieve high efficiency, the integrated buck regulator is automatically controlled (Input-Output Control on the Block Diagram) to produce the optimal voltage headroom to balance efficiency, tight regulation and transient response at the linear regulator output.

Figure 1 is a composite graph of the LTM8028's power loss compared to the theoretical power loss of a traditional linear regulator. Note that the power loss (left hand Y axis) is plotted on the log scale. For $1.2V_{OUT}$ at 5A and $24V_{IN}$ the LTM8028 only loses 4W, while the traditional linear regulator theoretically dissipates over 110W.

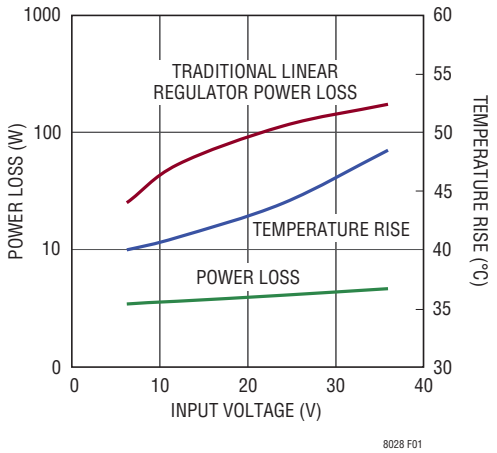


Figure 1. This Graph Shows the Full Load Power Loss and Temperature Rise of the LTM8028 over a Range of Input Voltages. Compare These Numbers to a Traditional Linear Regulator Powering the Same Load an Operating Condition. Note the Log Scale for Power Loss.

The LTM8028 switching buck converter utilizes fixed-frequency, forced continuous current mode control to regulate its output voltage. This means that the switching regulator will stay in fixed frequency operation even as the LTM8028 output current falls to zero. The LTM8028 has an analog control pin, I_{MAX}, to set the maximum allowable current output of the LTM8028. The analog control range of I_{MAX} is from 0V to 1.5V. The RUN pin functions as a precision shutdown pin. When the voltage at the RUN pin is lower than 1.55V, switching is terminated. Below this threshold, the RUN pin sinks 5.5µA. This current can be used with a resistor between RUN and V_{IN} to set the hysteresis. During start-up, the SS pin is held low until the part is enabled, after which the capacitor at the soft-start pin is charged with an 11µA current source. The switching frequency is determined by a resistor at the RT pin. The LTM8028 may also be synchronized to an external clock through the use of the SYNC pin.

The output linear regulator supplies up to 5A of output current with a typical dropout voltage of 85mV. Its high bandwidth provides UltraFast transient response using low ESR ceramic output capacitors, saving bulk capacitance, PCB area and cost. The output voltage for the LTM8028 is digitally selectable in 50mV increments over a 0.8V to 1.8V range, and analog margining function allows the user to adjust system output voltage over a continuous ±10% range. It also features a remote sense pin for accurate regulation at the load, and a PGOOD circuit that indicates whether the output is in or out of regulation or if an internal fault has occurred.

The LTM8028 is equipped with a thermal shutdown to protect the device during momentary overload conditions. It is set above the 125°C absolute maximum internal temperature rating to avoid interfering with normal specified operation, so internal device temperatures will exceed the absolute maximum rating when the overtemperature protection is active. So, continuous or repeated activation of the thermal shutdown may impair device reliability. During thermal shutdown, all switching is terminated and the SS pin is driven low.

APPLICATIONS INFORMATION

For most applications, the design process is straight forward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply 10µF to V_{IN} and the recommended R_T value ($R_{T(OPTIMAL)}$ in Table 1). Lower R_T values (resulting in a higher operating frequency) may be used to reduce the output ripple. Do not use values below $R_{T(MIN)}$.
3. Apply a parallel combination of a 100µF ceramic and a 470µF electrolytic to BKV. The Sanyo OS-CON 6SEP-C470M or United Chemi-Con APXF6R3ARA471MH80G work well for the electrolytic capacitor, but other devices with an ESR about 10mΩ may be used.
4. Apply a minimum of 37µF to V_{OUT}. As shown in Table 1, this is usually a parallel combination of 4.7µF, 10µF and 22µF capacitors.
5. Apply an additional 100µF capacitor to V_{OUT} if very small (2%) transient response is required.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current is limited by junction temperature, the relationship between the input and output voltage magnitude and polarity and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

The maximum frequency (and attendant R_T value) at which the LTM8028 should be allowed to switch is given in Table 1 in the f_{MAX} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the $f_{OPTIMAL}$ column. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

Programming Output Voltage

Three tri-level input pins, V_{O2}, V_{O1} and V_{O0}, select the value of output voltage. Table 2 illustrates the 3-bit digital word-to-output voltage resulting from setting these pins *high, low* or allowing them to float. These pins may be tied *high* or *low* by either pin-strapping them to V_{OB} or driving them

Table 1: Recommended Component Values and Configuration (T_A = 25°C)

V_{IN}	V_{OUT}	$f_{OPTIMAL}$	$R_{T(OPTIMAL)}$	f_{MAX}	$R_{T(MIN)}$
6V to 36V	0.8V	200kHz	200k	250kHz	165k
6V to 36V	1.0V	250kHz	165k	280kHz	150k
6V to 36V	1.2V	250kHz	165k	315kHz	133k
6V to 36V	1.5V	250kHz	165k	333kHz	127k
6V to 36V	1.8V	315kHz	133k	385kHz	107k
9V to 15V	0.8V	250kHz	165k	650kHz	61.9k
9V to 15V	1.0V	280kHz	150k	750kHz	53.6k
9V to 15V	1.2V	300kHz	143k	800kHz	49.9k
9V to 15V	1.5V	315kHz	133k	1MHz	40.2k
9V to 15V	1.8V	350kHz	118k	1MHz	40.2k
18V to 36V	0.8V	200kHz	200k	250kHz	165k
18V to 36V	1.0V	250kHz	165k	280kHz	150k
18V to 36V	1.2V	250kHz	165k	315kHz	133k
18V to 36V	1.5V	250kHz	165k	333kHz	127k
18V to 36V	1.8V	315kHz	133k	385kHz	107k
C_{IN}:		10µF, 50V, 1210			
C_{BKV}:		100µF, 6.3V, 1210 + 470µF, 6.3V Low ESR Electrolytic			
C_{OUT}:		4.7µF, 4V, 0603 + 10µF, 10V, 0805 + 22µF, 10V, 0805			
C_{OUT} (Optional):		100µF, 6.3V, 1210			

Note: An input bulk capacitor is required.

APPLICATIONS INFORMATION

with digital ports. Pins that float may either actually float or require logic that has *Hi-Z* output capability. This allows the output voltage to be dynamically changed if necessary. The output voltage is selectable from a minimum of 0.8V to a maximum of 1.8V in increments of 50mV.

Table 2. V_{O2} to V_{O0} Setting vs Output Voltage

V_{O2}	V_{O1}	V_{O0}	$V_{OUT(NOM)}$	V_{O2}	V_{O1}	V_{O0}	$V_{OUT(NOM)}$
0	0	0	0.80V	Z	0	1	1.35V
0	0	Z	0.85V	Z	Z	0	1.40V
0	0	1	0.90V	Z	Z	Z	1.45V
0	Z	0	0.95V	Z	Z	1	1.50V
0	Z	Z	1.00V	Z	1	0	1.55V
0	Z	1	1.05V	Z	1	Z	1.60V
0	1	0	1.10V	Z	1	1	1.65V
0	1	Z	1.15V	1	X	0	1.70V
0	1	1	1.20V	1	X	Z	1.75V
Z	0	0	1.25V	1	X	1	1.80V
Z	0	Z	1.30V				

X = Don't Care, 0 = Low, Z = Float, 1 = High

Capacitor Selection Considerations

The C_{IN}, C_{BKV} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

The output capacitance for BKV given in Table 1 specifies an electrolytic capacitor. Ceramic capacitors may also be used in the application, but it may be necessary to use more of them. Many high value ceramic capacitors have a large voltage coefficient, so the actual capacitance of the component at the desired operating voltage may be only a fraction of the specified value. Also, the very low ESR of ceramic capacitors may necessitate an additional capacitor for acceptable stability margin.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8028. A ceramic input capacitor combined with trace or cable inductance forms a high Q (under damped) tank circuit. If the LTM8028 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Why Do Multiple, Small Value Output Capacitors Connected in Parallel Work Better?

The parasitic series inductance (ESL) and resistance (ESR) of a capacitor can have a detrimental impact on the transient and ripple/noise response of a linear regulator. Employing a number of capacitors in parallel will reduce this parasitic impedance and improve the performance of the linear regulator. In addition, PCB vias can add significant inductance, so the fundamental decoupling capacitors must be mounted on the same copper plane as the LTM8028.

The most area efficient parallel capacitor combination is a graduated 4/2/1 scale capacitances of the same case size, such as the 37µF combination in Table 1, made up of 22µF, 10µF and 4.7µF capacitors in parallel. Capacitors with small case sizes have larger ESR, while those with larger case sizes have larger ESL. As seen in Table 1, the optimum case size is 0805, followed by a larger, fourth bulk energy capacitor, case sized 1210. In general, the large fourth capacitor is required only if very tight transient response is required.

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Output Voltage Margining

The LTM8028's analog margining pin, MARGA, provides a continuous output voltage adjustment range of ±10%. It margins V_{OUT} by adjusting the internal 600mV reference voltage up and down. Driving MARGA with 600mV to 1.2V provides 0% to 10% of adjustment. Driving MARGA with 600mV to 0V provides 0% to –10% of adjustment. If unused, allow MARGA to float or bypass this pin with a 1nF capacitor to GND. Note that the analog margining function does not adjust the PGOOD threshold. Therefore, negative analog margining may trip the PGOOD comparator and toggle the PGOOD flag.

Power Good

PGOOD pin is an open-drain NMOS digital output that actively pulls low if any one of these fault modes is detected:

- V_{OUT} is less than 90% of $V_{OUT(NOMINAL)}$ on the rising edge of V_{OUT}.
- V_{OUT} drops below 85% of $V_{OUT(NOMINAL)}$ for more than 25µs.
- Internal faults such as loss of internal housekeeping voltage regulation, reverse-current on the power switch and excessive temperature.

SENSEP and Load Regulation

The LTM8028 provides a Kelvin sense pin for V_{OUT}, allowing the application to correct for parasitic package and PCB IR drops. If the load is far from the LTM8028, running a separate line from SENSEP to the remote load will correct for IR voltage drops and improve load regulation. SENSEP is the only voltage feedback that the LTM8028 uses to regulate the output, so it must be connected to V_{OUT}, either locally or at the load. In some systems, a loss of feedback signal equates to a loss of output control, potentially damaging the load. If the SENSEP signal is inadvertently disconnected from the load, internal safety circuits in the LTM8028 prevent the output from running away. This also limits the amount of correction to about 0.2V.

Bear in mind that the linear regulator of the LTM8028 is a high bandwidth power device. If the load is very far from the LTM8028, the parasitic impedance of the remote connection may interfere with the internal control loop and adversely affect stability. If SENSEP is connected to a remote load, the user must evaluate the load regulation and dynamic load response of the LTM8028.

Short-Circuit and Overload Recovery

Like many IC power regulators, the internal linear regulator has safe operating area (SOA) protection. The safe area protection decreases current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage up to the absolute maximum voltage rating.

Under maximum I_{LOAD} and maximum V_{IN}-V_{OUT} conditions, the internal linear regulator's power dissipation peaks at about 1.5W. If ambient temperature is high enough, die junction temperature will exceed the 125°C maximum operating temperature. If this occurs, the LTM8028 relies on two additional thermal safety features. At about 145°C, the device is designed to make the PGOOD output pull low providing an early warning of an impending thermal shutdown condition. At 165°C typically, the LTM8028 is designed to engage its thermal shutdown and the output is turned off until the IC temperature falls below the thermal hysteresis limit. The SOA protection decreases current limit as the in-to-out voltage increases and keeps the power dissipation at safe levels for all values of input-to-output voltage.

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Reverse Voltage

The LTM8028 incorporates a circuit that detects if BKV decreases below V_{OUT}. If this voltage condition is detected, internal circuitry turns off the drive to the internal linear regulator's pass transistor, thereby turning off the output. This circuit's intent is to limit and prevent back-feed current from V_{OUT} to V_{IN} if the input voltage collapses due to a fault or overload condition. Do not apply a voltage to BKV.

Programming Switching Frequency

The LTM8028 has an operational switching frequency range between 200kHz and 1MHz. This frequency is programmed with an external resistor from the RT pin to ground. Do not leave this pin open under any condition. The RT pin is also current limited to 60µA. See Table 3 for resistor values and the corresponding switching frequencies.

Table 3. R_T Resistor Values and Their Resultant Switching Frequencies

SWITCHING FREQUENCY (MHz)	R_T (kΩ)
1	40.2
0.750	53.6
0.5	82.5
0.3	143
0.2	200

Switching Frequency Trade-Offs

It is recommended that the user apply the optimal R_T value given in Table 1 for the input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. A higher switching frequency, for example, will yield a smaller output ripple, while a lower frequency will reduce power loss. Switching too fast, however, can generate excessive heat and even possibly damage the LTM8028 in fault conditions. Switching too slow can result in a final design that has too much output capacitance or sub-harmonic oscillations that cause excessive ripple. In all cases, stay below the stated maximum frequency (f_{MAX}) given in Table 1.

Switching Frequency Synchronization

The nominal switching frequency of the LTM8028 is determined by the resistor from the RT pin to GND and may be set from 200kHz to 1MHz. The internal oscillator may also be synchronized to an external clock through the SYNC pin. The external clock applied to the SYNC pin must have a logic low below 0.25V and a logic high greater than 1.25V. The input frequency must be 20% higher than the frequency determined by the resistor at the RT pin. The duty cycle of the input signal needs to be greater than 10% and less than 90%. Input signals outside of these specified parameters will cause erratic switching behavior and subharmonic oscillations. When synchronizing to an external clock, please be aware that there will be a fixed delay from the input clock edge to the edge of switch. The SYNC pin must be tied to GND if the synchronization to an external clock is not required. When SYNC is grounded, the switching frequency is determined by the resistor at the RT pin.

Soft-Start

The soft-start function controls the slew rate of the power supply output voltage during start-up. A controlled output voltage ramp minimizes output voltage overshoot, reduces inrush current from the V_{IN} supply, and facilitates supply sequencing. A capacitor connected from the SS pin to GND programs the slew rate. The capacitor is charged from an internal 11µA current source to produce a ramped output voltage.

Maximum Output Current Adjust

To adjust the regulated load current, an analog voltage is applied to the I_{MAX} pin. Varying the voltage between 0V and 1.5V adjusts the maximum current between the minimum and the maximum current, 5.6A typical. Above 1.5V, the control voltage has little effect on the regulated inductor current. A graph of the output current versus I_{MAX} voltage is given in the Typical Performance Characteristics

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section. There is a 10k resistor internally connected from a 2V reference to the I_{MAX} pin, so the current limit can be set as shown in Figure 2 with the following equation:

$$R_{IMAX} = \frac{10 \bullet I_{MAX}}{7.467 - I_{MAX}}\ k\Omega$$

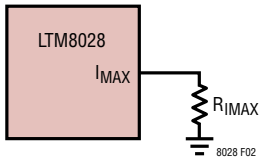


Figure 2. Setting The Output Current Limit, I_{MAX}

Thermal Shutdown

At about 145°C, the LTM8028 is designed to make the PGOOD output pull low providing an early warning of an impending thermal shutdown condition. At 165°C typically, the LTM8028 is designed to engage its thermal shutdown, discharge the soft-start capacitor and turn off the output until the internal temperature falls below the thermal hysteresis limit. When the part has cooled, the part automatically restarts. Note that this thermal shutdown is set to engage at temperatures above the 125°C absolute maximum internal operating rating to ensure that it does not interfere with functionality in the specified operating range. This means that internal temperatures will exceed the 125°C absolute maximum rating when the overtemperature protection is active, so repeated or prolonged operation under these conditions may impair the device's reliability.

UVLO and Shutdown

The LTM8028 has an internal UVLO that terminates switching, resets all logic, and discharges the soft-start capacitor for input voltages below 4.2V. The LTM8028 also has a precision RUN function that enables switching when the voltage at the RUN pin rises to 1.68V and shuts down the LTM8028 when the RUN pin voltage falls to 1.55V. There is also an internal current source that provides 5.5µA of pull-down current to program additional UVLO hysteresis. For RUN rising, the current source is sinking 5.5µA until RUN = 1.68V, after which it turns off. For RUN falling, the current source is off until the RUN = 1.55V, after which it sinks 5.5µA. The following equations determine the voltage divider resistors for programming the falling UVLO voltage and rising enable voltage (V_{ENA}) as configured in Figure 3.

$$R1 = \left(\frac{1.55 \bullet R2}{UVLO - 1.55}\right)$$

$$R2 = \frac{V_{ENA} - 1.084 \bullet UVLO}{5.5\mu A}$$

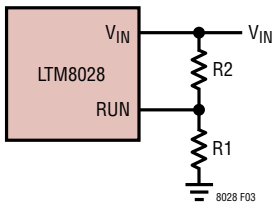


Figure 3. UVLO Configuration

The RUN pin has an absolute maximum voltage of 6V. To accommodate the largest range of applications, there is an internal Zener diode that clamps this pin, so that it can be pulled up to a voltage higher than 6V through a resistor that limits the current to less than 100µA. For applications where the supply range is greater than 4:1, size R2 greater than 375k.

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8028. The LTM8028 is nevertheless a switching power supply, and care must be taken to

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minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 4 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

A few rules to keep in mind are:

1. Place the R_T resistor as close as possible to its respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8028.
3. Place the C_{OUT} capacitors as close as possible to the V_{OUT} and GND connection of the LTM8028.
4. Place the C_{IN}, C_{BKV} and C_{OUT} capacitors such that their ground current flow directly adjacent or underneath the LTM8028.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8028.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 4. The LTM8028 can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

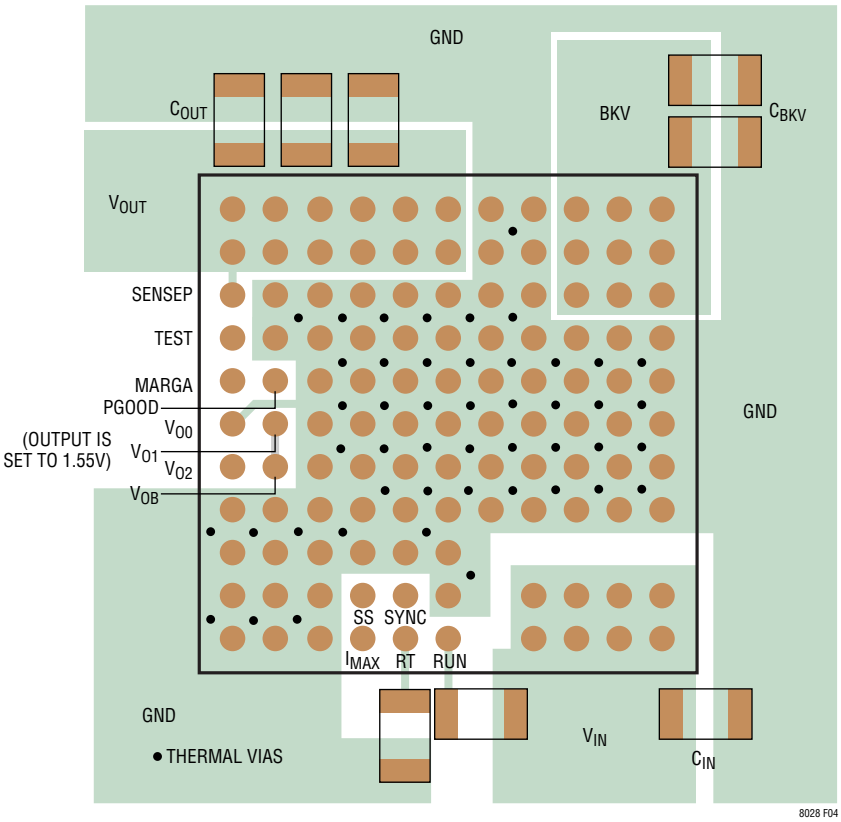


Figure 4. Layout Showing Suggested External Components, GND Plane and Thermal Vias

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Load Sharing

Each LTM8028 features an accurate current limit that enables the use of multiple devices to power a load heavier than 5A. This is accomplished by simply tying the V_{OUT} terminals of the LTM8028s together, and set the outputs of the parallel units to the same voltage. There is no need to power the µModule regulators from the same power supply. That is, the application can use multiple LTM8028s, each powered from separate input voltage rails and contribute a different amount of current to the load as dictated by the programmed current limit. Keep in mind that the paralleled LTM8028s will not share current equally. In most cases, one LTM8028 will provide almost all the load until its current limit is reached, and then the other unit or units will start to provide current. This might be an unacceptable operating condition in other power regulators, but the accurate current loop of the LTM8028 controls the electrical and thermal performance of each individual µModule regulator. This prevents the oscillations, thermal runaway and other issues that other regulators might suffer. An example of two LTM8028s connected in parallel to deliver 1.8V at 10A, while powered from two disparate power sources, is given in the Typical Applications section. A graph of the output current delivered from each µModule regulator is given below in Figure 5.

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8028. However, these capacitors can cause problems if the LTM8028 is plugged into a live input supply (see Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8028 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8028's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM8028 into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is to add an electrolytic bulk capacitor to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is physically large.

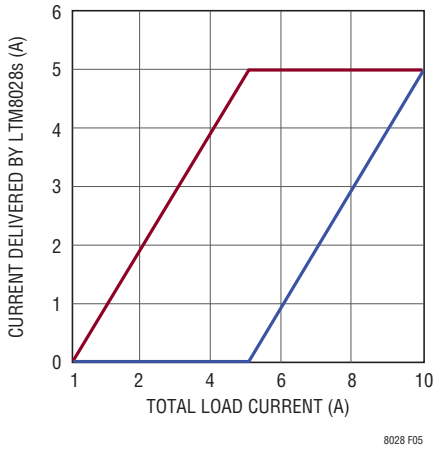


Figure 5. In Most Cases Where Paralleled LTM8028s are Used, One µModule Will Deliver All of The Load Current Until Its Current Limit Is Reached, Then The Other Unit(s) Will Provide Current. The Tightly Controlled Output Current Prevents Oscillations and Thermal Runaway Observed In Other Types of Regulators

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Thermal Considerations

The LTM8028 relies on two thermal safety features. At about 145°C, the device is designed to pull the PGOOD output *low* providing an early warning of an impending thermal shutdown condition. At 165°C typically, the LTM8028 is designed to engage its thermal shutdown and the output is turned off until the IC temperature falls below the thermal hysteresis limit. Note that these temperature thresholds are above the 125°C absolute maximum rating to avoid interfering with normal operation. Thus, prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device.

The LTM8028 output current may need to be derated if it is required to operate in a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by the LTM8028 mounted to a 58cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use finite element analysis (FEA) to predict thermal performance. To that end, the Pin Configuration of the data sheet typically gives four thermal coefficients:

θ_{JA} – Thermal resistance from junction to ambient

$\theta_{JCbottom}$ – Thermal resistance from junction to the bottom of the product case

θ_{JCtop} – Thermal resistance from junction to top of the product case

θ_{JBoard} – Thermal resistance from junction to the printed circuit board.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased below:

θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

$\theta_{JCbottom}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JB} is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a 2-sided, 2-layer board. This board is described in JESD 51-9.

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Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule regulator. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in the product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A graphical representation of these thermal resistances is given in Figure 6:

The blue resistances are contained within the µModule regulator, and the green are outside.

The die temperature of the LTM8028 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8028. The bulk of the heat flow out of the LTM8028 is through the bottom of the module and the LGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

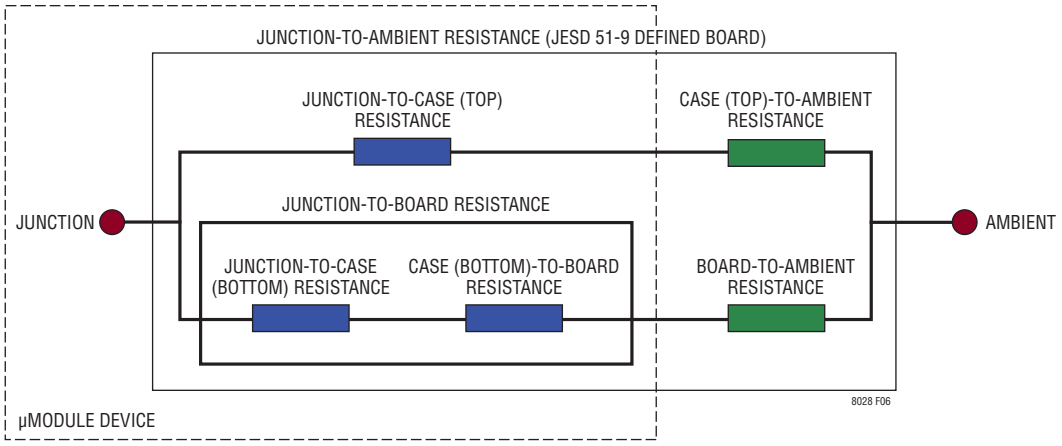
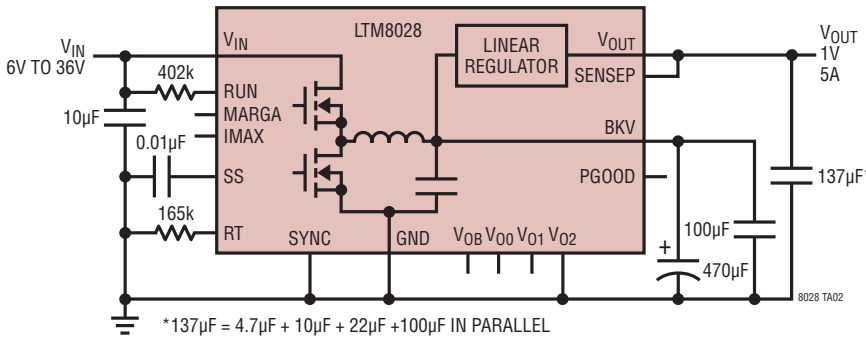


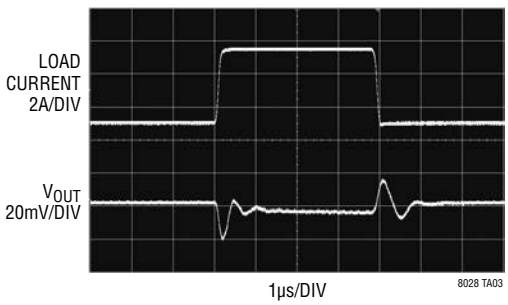
Figure 6. Thermal Model of µModule

TYPICAL APPLICATIONS

1V at 5A Regulator with 2% Transient Response

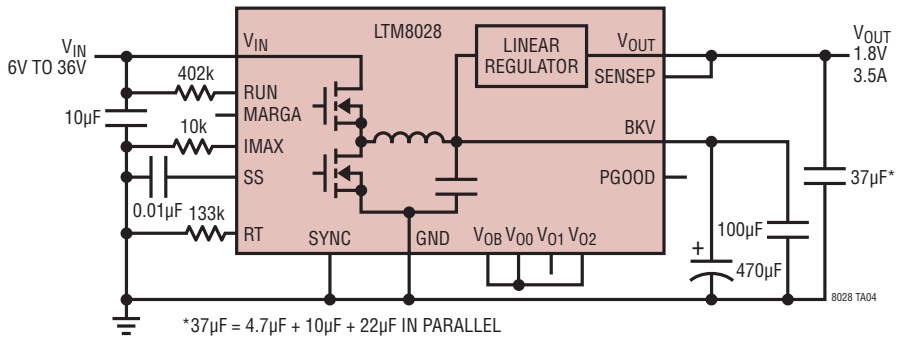


Transient Response from 0.5A to 5A, 1µs Load Current Rise and Fall Time, $12V_{IN}$

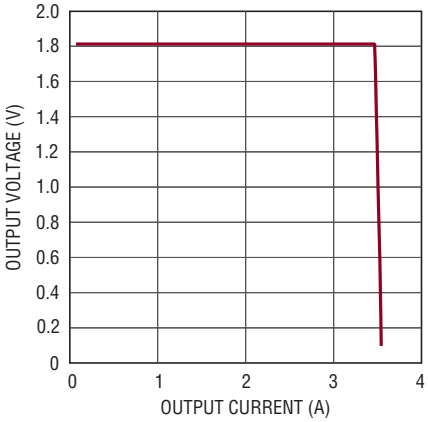


TYPICAL APPLICATIONS

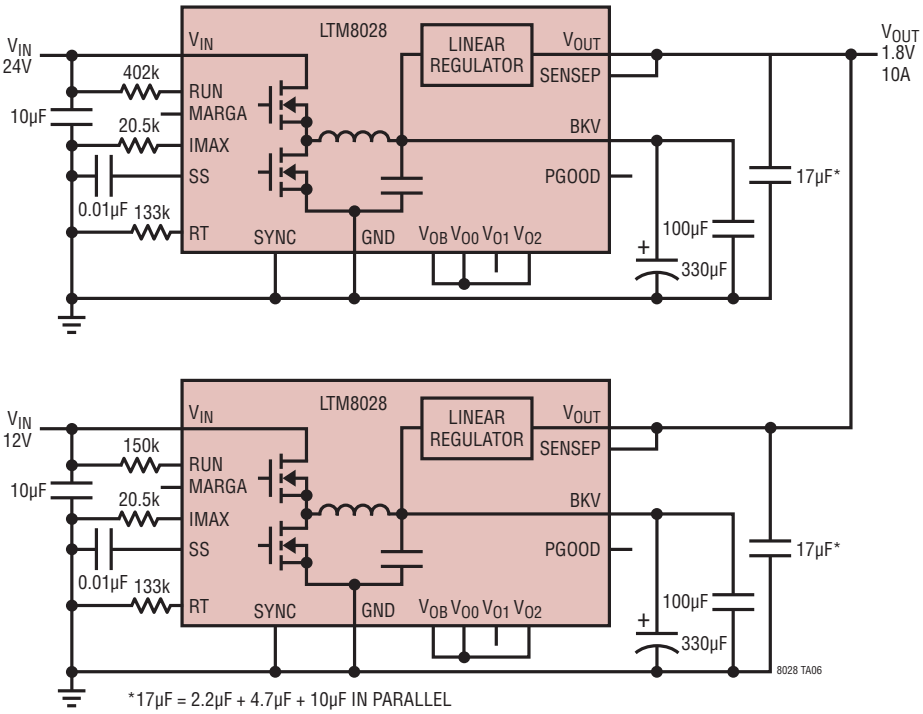
1.8V Regulator with 3.5A Current Limit



Output Voltage vs Current

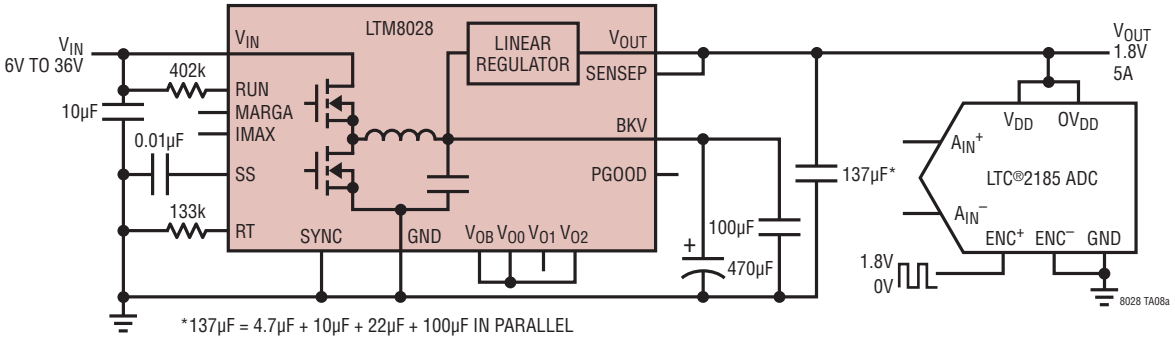


1.8V, 10A with Two LTM8028s Powered from Two Different Sources Each µModule Regulator Is Limited to Provide a Maximum of 5A

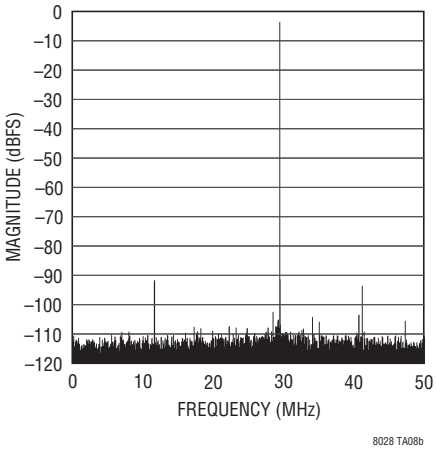


TYPICAL APPLICATIONS

Low Noise LTM8028 Powering 16-Bit, 125Msps ADC



32k-Point FFT, f_{IN} = 70.3MHz, –1dBFS, 100Msps



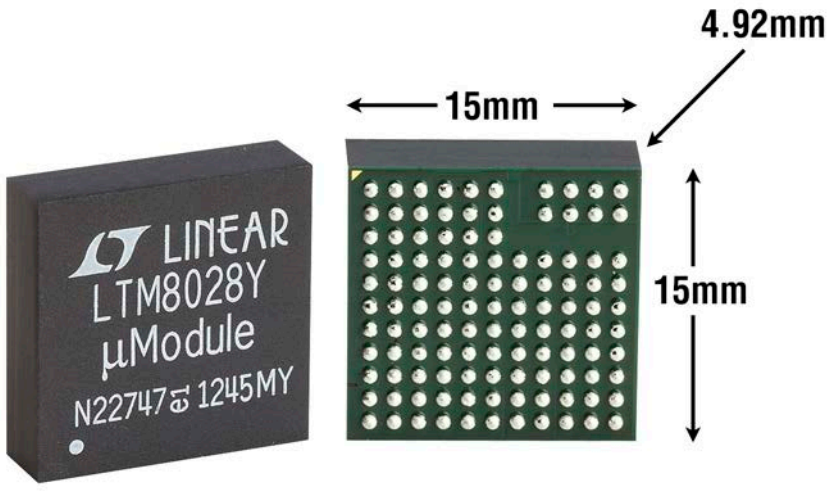
PACKAGE DESCRIPTION

Table 3. Pin Assignment Table (Arranged by Pin Number)

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	GND	B1	GND	C1	GND	D1	I_{MAX}	E1	RT	F1	RUN
A2	GND	B2	GND	C2	GND	D2	SS	E2	SYNC	F2	GND
A3	GND	B3	GND	C3	GND	D3	GND	E3	GND	F3	GND
A4	GND	B4	GND	C4	GND	D4	GND	E4	GND	F4	GND
A5	V_{O2}	B5	V_{OB}	C5	GND	D5	GND	E5	GND	F5	GND
A6	V_{O0}	B6	V_{O1}	C6	GND	D6	GND	E6	GND	F6	GND
A7	MARGA	B7	PGOOD	C7	GND	D7	GND	E7	GND	F7	GND
A8	TEST	B8	GND	C8	GND	D8	GND	E8	GND	F8	GND
A9	SENSEP	B9	GND	C9	GND	D9	GND	E9	GND	F9	GND
A10	V_{OUT}	B10	V_{OUT}	C10	V_{OUT}	D10	V_{OUT}	E10	V_{OUT}	F10	V_{OUT}
A11	V_{OUT}	B11	V_{OUT}	C11	V_{OUT}	D11	V_{OUT}	E11	V_{OUT}	D11	V_{OUT}

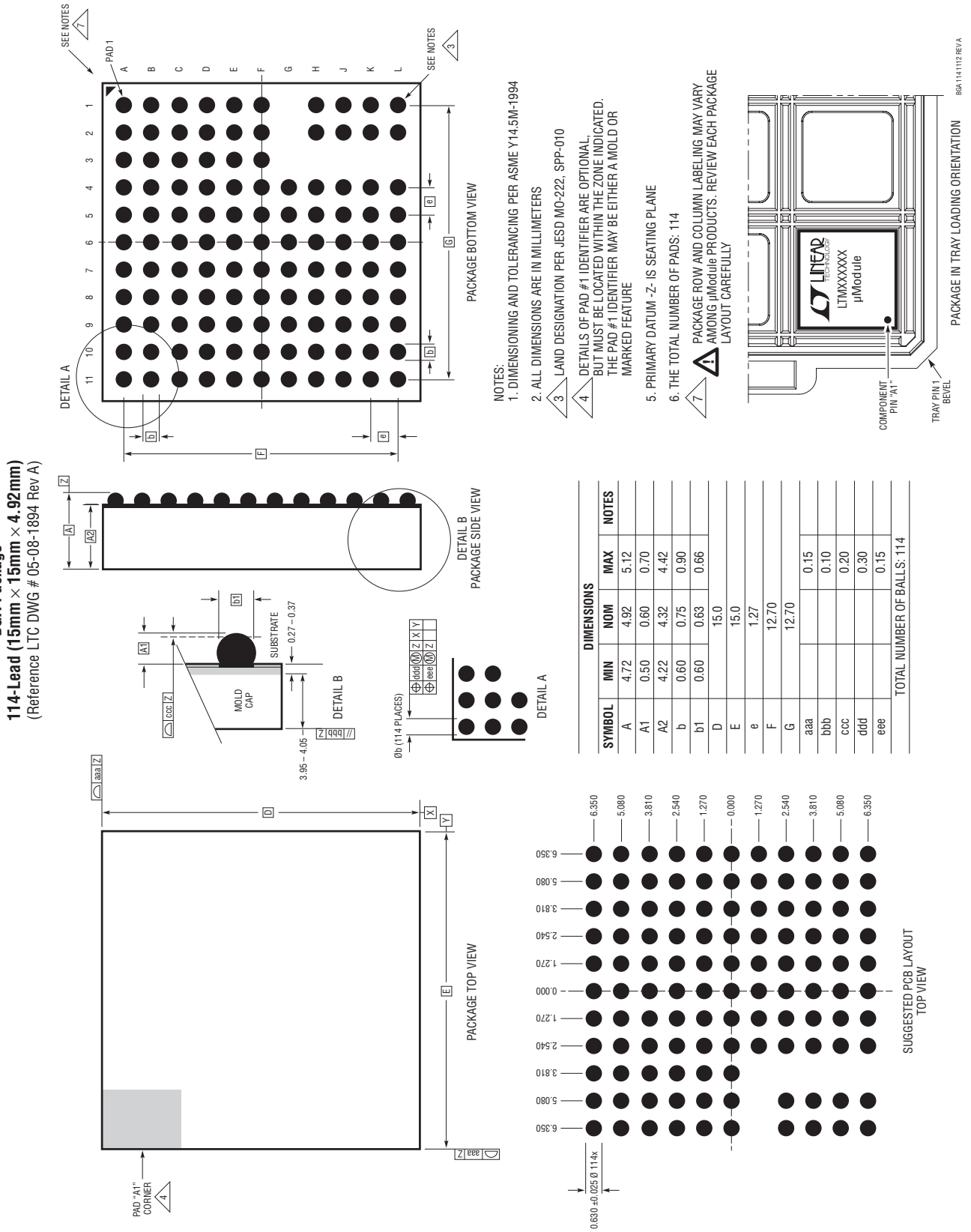
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAM	PIN	NAME
G1	–	H1	V_{IN}	J1	V_{IN}	K1	V_{IN}	L1	V_{IN}
G2	–	H2	V_{IN}	J2	V_{IN}	K2	V_{IN}	L2	V_{IN}
G3	–	H3	–	J3	–	K3	–	L3	–
G4	GND	H4	GND	J4	GND	K4	GND	L4	GND
G5	GND	H5	GND	J5	GND	K5	GND	L5	GND
G6	GND	H6	GND	J6	GND	K6	GND	L6	GND
G7	GND	H7	GND	J7	GND	K7	GND	L7	GND
G8	GND	H8	GND	J8	GND	K8	GND	L8	GND
G9	GND	H9	GND	J9	BKV	K9	BKV	L9	BKV
G10	GND	H10	GND	J10	BKV	K10	BKV	L10	BKV
G11	GND	H11	GND	J11	BKV	K11	BKV	L11	BKV

PACKAGE PHOTO



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.72	4.92	5.12	
A1	0.50	0.60	0.70	
A2	4.22	4.32	4.42	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.0		
E		15.0		
e		1.27		
F		12.70		
G		12.70		
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 114				

REVISION HISTORY

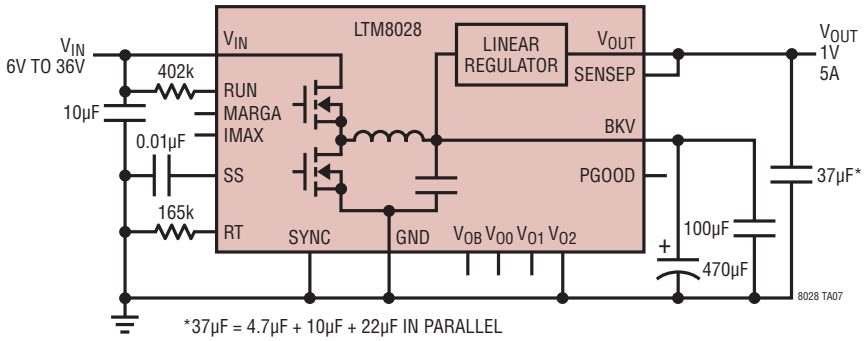
REV	DATE	DESCRIPTION	PAGE NUMBER
A	2/14	Added SnPb BGA package option	1, 2
B	5/14	SYNC Input Threshold MIN: from 0.8V to 0.6V; MAX: from 1.2V to 1.3V Add PGOOD description	3 7

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

1V at 5A Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8032	Step-Down µModule Regulator, EN55022B Compliant	$3.6V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 10V$, 2A
LTM4613	Step-Down µModule Regulator, EN55022B Compliant	$5V \le V_{IN} \le 36V$, $3.3V \le V_{OUT} \le 15V$, 8A
LTM8027	60V, 4A Step-Down µModule Regulator	$4.5V \le V_{IN} \le 60V$, $2.5V \le V_{OUT} \le 24V$, 4A
LTM8048	Isolated µModule Converter	725V Isolation, $3.1V \le V_{IN} \le 32V$, $1.2V \le V_{OUT} \le 12V$, 300mA
LTM4615	Triple Output Step-Down µModule Regulator	$2.375V \le V_{IN} \le 5.5V$, $0.8V \le V_{OUT} \le 5.5V$, 4A, 4A, 1.5A
LTM4620	Dual 13A, Single 26A Step-Down µModule Regulator	$4.5V \le V_{IN} \le 16V$, $0.6V \le V_{OUT} \le 2.5V$, Up to 100A Current Sharing

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTM8028
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