36V, 3A Step-Down µModule Regulator

FEATURES

- **Complete Step-Down Switch Mode Power Supply**
- **Wide Input Voltage Range: 3.6V to 36V**
- **Up to 3A Output Current**
- **Parallelable for Increased Output Current**
- **0.8V to 24V Output Voltage**
- **Selectable Switching Frequency: 200kHz to 2.4MHz**
- Current Mode Control
- SnPb or RoHS Compliant Finish
- Programmable Soft-Start
- 9mm × 15mm × 4.32mm LGA and 9mm × 15mm × 4.92mm BGA Packages

APPLICATIONS

- Automotive Battery Regulation
- Power for Portable Products
- Distributed Supply Regulation
- Industrial Supplies
- Wall Transformer Regulation

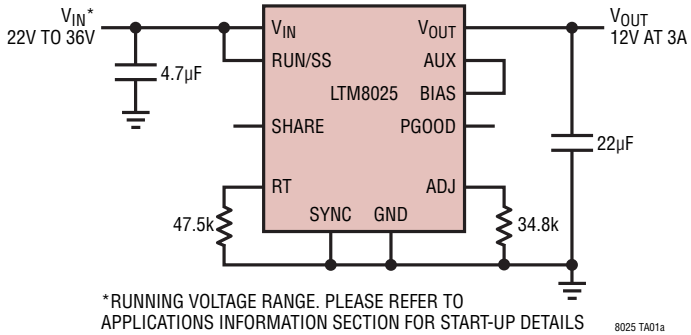
DESCRIPTION

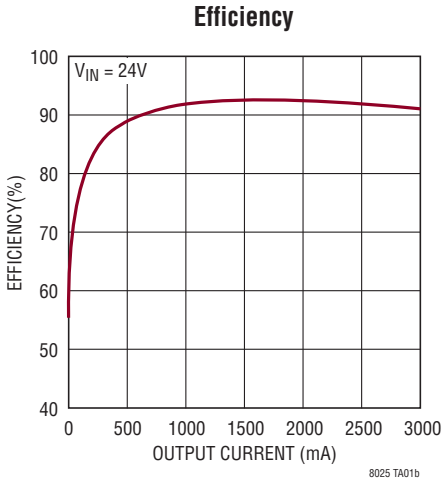
The LTM®8025 is a 36V_{IN}, 3A step-down µModule® (micromodule) converter. Included in the package are the switching controller, power switches, inductor and all support components. Operating over an input voltage range of 3.6V to 36V, the LTM8025 supports an output voltage range of 0.8V to 24V and a switching frequency range of 200kHz to 2.4MHz, each set by a single resistor. Only the bulk input and output filter capacitors are needed to finish the design.

The LTM8025 is packaged in a thermally enhanced, compact (9mm × 15mm) and low profile over-molded land grid array (LGA) and ball grid array (BGA) packages suitable for automated assembly by standard surface mount equipment. The LTM8025 is available with SnPb (BGA) or RoHS compliant terminal finish.

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TYPICAL APPLICATION

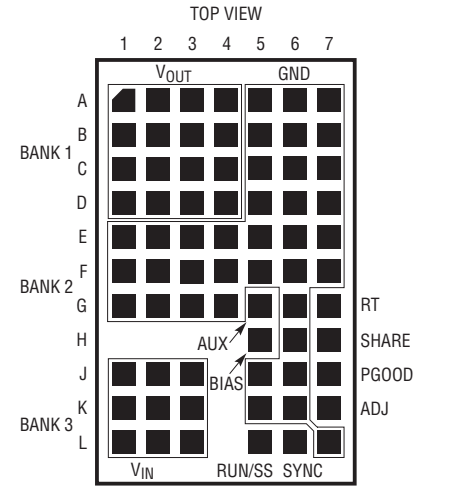




ABSOLUTE MAXIMUM RATINGS (Note 1)

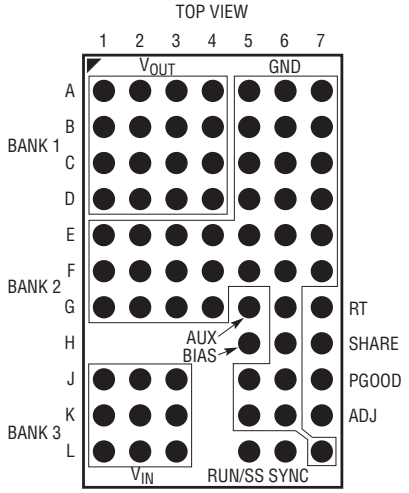
V_{IN}, RUN/SS Voltage.....36V
ADJ, RT, SHARE Voltage.....6V
V_{OUT}, AUX.....25V
PGOOD, SYNC.....30V
BIAS.....25V
V_{IN} + BIAS.....56V
Maximum Junction Temperature (Note 2) ..... 125°C
Solder Temperature..... 245°C

PIN CONFIGURATION



LGA PACKAGE
70-PIN (9mm × 15mm × 4.32mm)

T_{JMAX} = 125°C, θ_{JA} = 24.4°C/W, $\theta_{JC(BOTTOM)}$ = 11.5°C/W,
$\theta_{JC(TOP)}$ = 42.7°C/W, θ_{JB} = 18.7°C/W
θ VALUES DETERMINED PER JESD51-9, MAX OUTPUT POWER
WEIGHT = 1.8 GRAMS



BGA PACKAGE
70-PIN (9mm × 15mm × 4.92mm

T_{JMAX} = 125°C, θ_{JA} = 24.4°C/W, $\theta_{JC(BOTTOM)}$ = 11.5°C/W,
$\theta_{JC(TOP)}$ = 42.7°C/W, θ_{JB} = 18.7°C/W
θ VALUES DETERMINED PER JESD51-9, MAX OUTPUT POWER
WEIGHT = 1.8 GRAMS)

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (NOTE 2)
		DEVICE	FINISH CODE			
LTM8025EV#PBF	Au (RoHS)	LTM8025V	e4	LGA	3	–40°C to 125°C
LTM8025IV#PBF	Au (RoHS)	LTM8025V	e4	LGA	3	–40°C to 125°C
LTM8025MPV#PBF	Au (RoHS)	LTM8025MPV	e4	LGA	3	–55°C to 125°C
LTM8025EY#PBF	SAC305 (RoHS)	LTM8025Y	e1	BGA	3	–40°C to 125°C
LTM8025IY#PBF	SAC305 (RoHS)	LTM8025Y	e1	BGA	3	–40°C to 125°C
LTM8025IY	SnPb (63/37)	LTM8025Y	e0	BGA	3	–40°C to 125°C
LTM8025MPY#PBF	SAC305 (RoHS)	LTM8025Y	e1	BGA	3	–55°C to 125°C
LTM8025MPY	SnPb (63/37)	LTM8025Y	e0	BGA	3	–55°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, RUN/SS = 12V, BIAS = 3V unless otherwise noted. (Note 2)

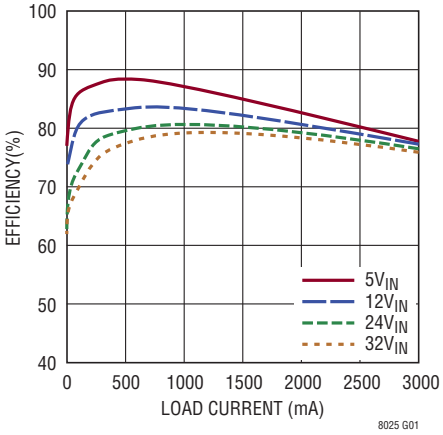
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●			3.6	V
Output DC Voltage	R_{ADJ} Open R_{ADJ} = 16.9k; V_{IN} = 36V			0.8 24		V V
Output DC Current	V_{OUT} = 3.3V		0		3	A
Quiescent Current into V_{IN}	RUN/SS = 0V Not Switching BIAS = 0V, Not Switching			0.01 25 85	1 60 150	µA µA µA
Quiescent Current into BIAS	RUN/SS = 0V Not Switching BIAS = 0V, Not Switching			0.01 65 0	0.5 120 5	µA µA µA
Line Regulation	5.5V < V_{IN} < 36V, I_{OUT} = 1A			0.3		%
Load Regulation	0A < I_{OUT} < 3A			0.4		%
Output Voltage Ripple (RMS)	0A < I_{OUT} < 3A			10		mV
Switching Frequency	R_T = 45.3k			775		kHz
Voltage (at ADJ Pin)		 ●	775 770	790	805 810	mV mV
Current Out of ADJ Pin	ADJ = 1V, V_{OUT} = 0V			2		µA
Minimum BIAS Voltage for Proper Operation				2	2.8	V
RUN/SS Pin Current	RUN/SS = 2.5V			5	10	µA
RUN Input High Voltage			2.5			V
RUN Input Low Voltage					0.2	V
PGOOD Threshold (at ADJ Pin)	V_{OUT} Rising			710		mV
PGOOD Leakage Current	PGOOD = 30V			0.1	1	µA
PGOOD Sink Current	PGOOD = 0.4V		200	700		µA
SYNC Input Low Threshold	f_{SYNC} = 550kHz				0.5	V
SYNC Input High Threshold	f_{SYNC} = 550kHz		0.7			V
SYNC Bias Current	SYNC = 0V			0.1		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

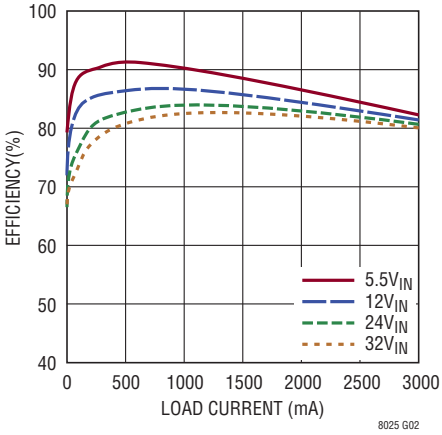
Note 2: The LTM8025E is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8025I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8025MP is guaranteed to meet specifications over the full –55°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

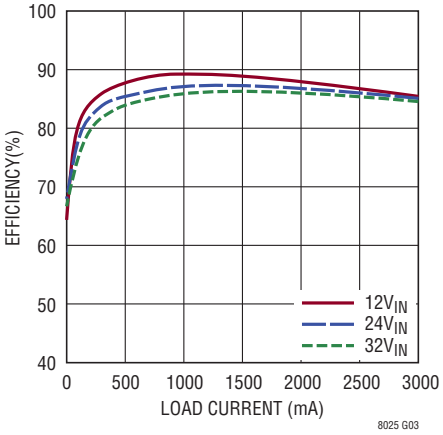
2.5V_{OUT} Efficiency



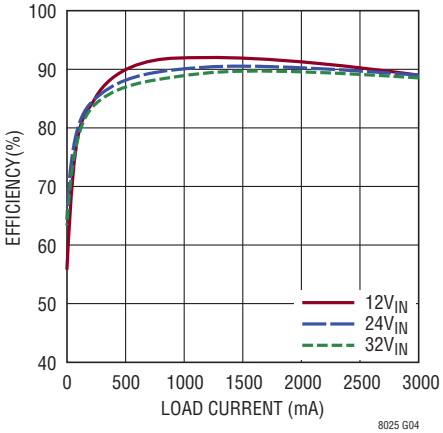
3.3V_{OUT} Efficiency



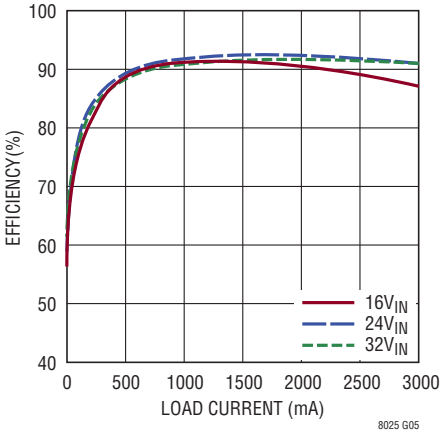
5V_{OUT} Efficiency



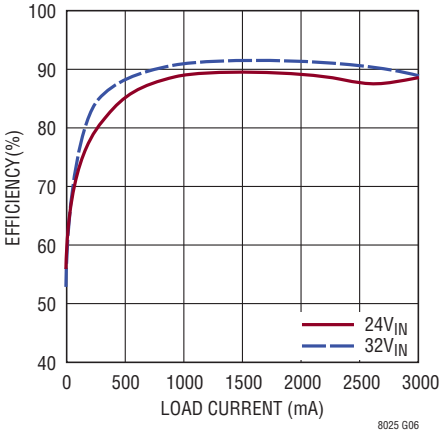
8V_{OUT} Efficiency



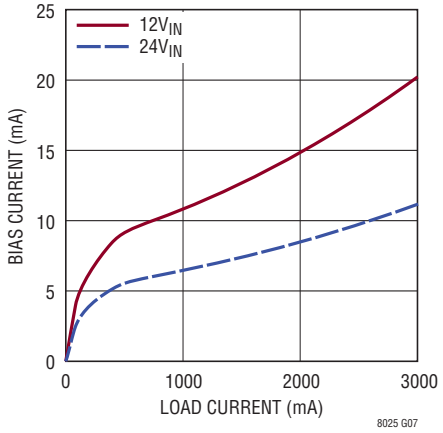
12V_{OUT} Efficiency



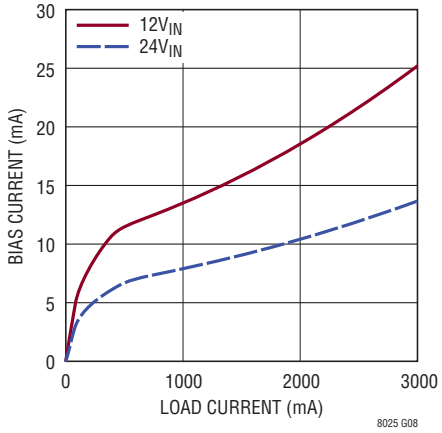
18V_{OUT} Efficiency



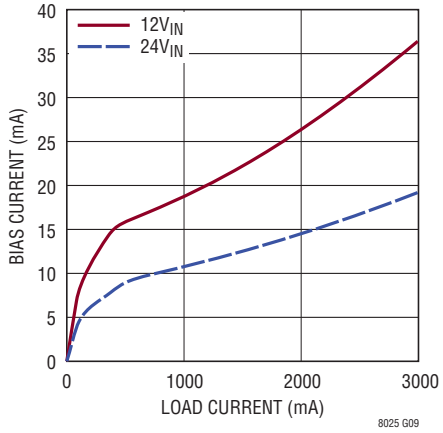
Bias Current vs Load Current 2.5V_{OUT}



Bias Current vs Load Current 3.3V_{OUT}

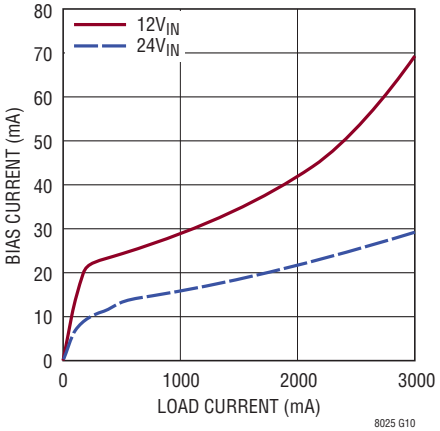


Bias Current vs Load Current 5V_{OUT}

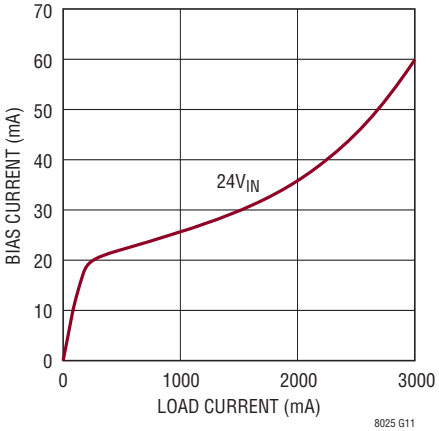


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

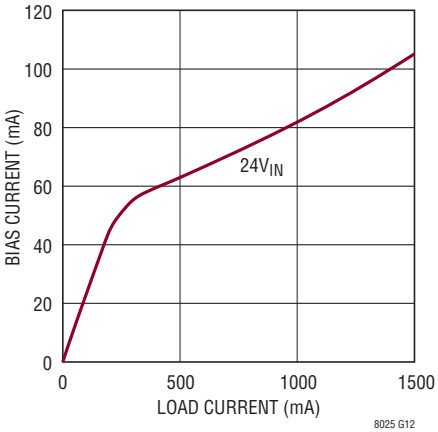
Bias Current vs Load Current 8V_{OUT}



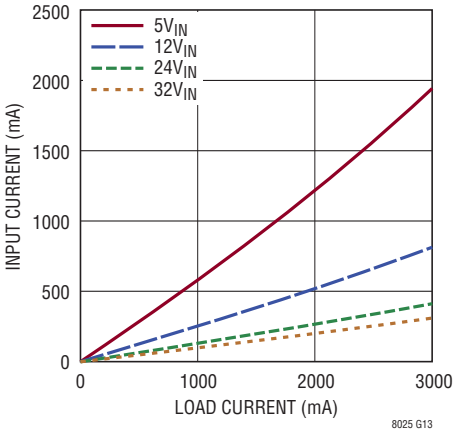
Bias Current vs Load Current 12V_{OUT}



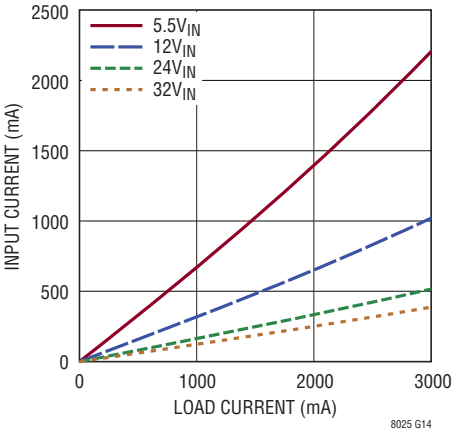
Bias Current vs Load Current 18V_{OUT}



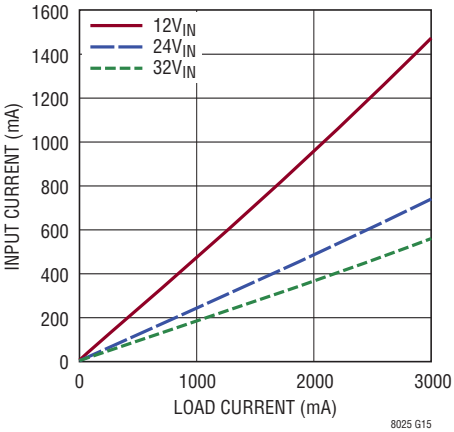
Input Current vs Load Current 2.5V_{OUT}



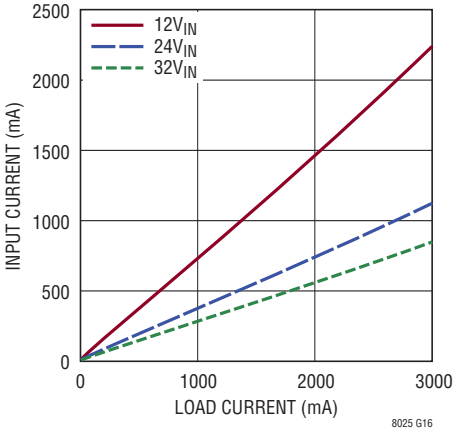
Input Current vs Load Current 3.3V_{OUT}



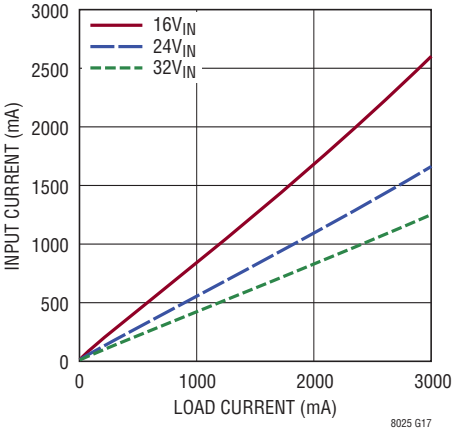
Input Current vs Load Current 5V_{OUT}



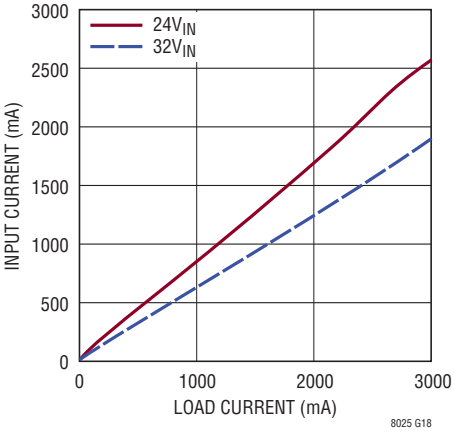
Input Current vs Load Current 8V_{OUT}



Input Current vs Load Current 12V_{OUT}

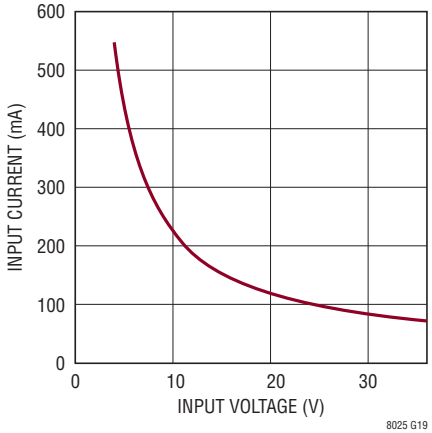


Input Current vs Load Current 18V_{OUT}

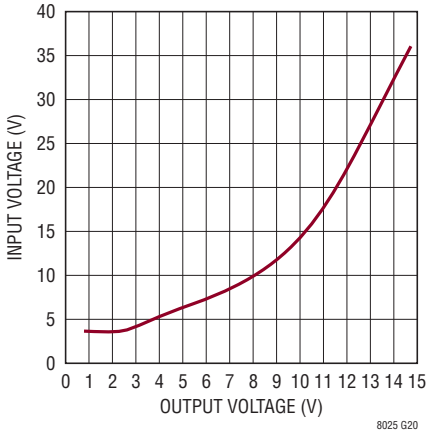


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

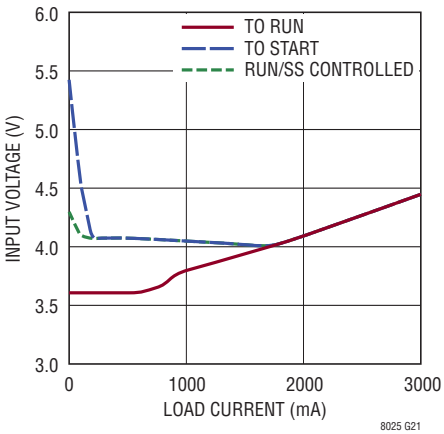
Input Current vs Input Voltage Output Shorted



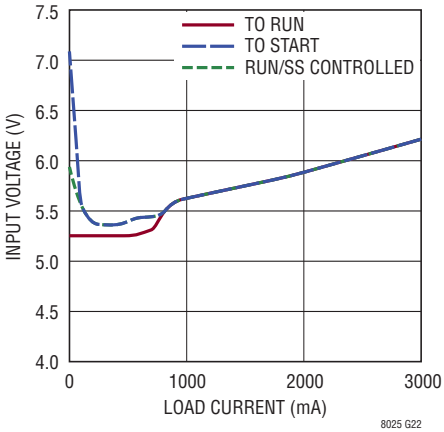
Minimum Input Running Voltage vs V_{OUT}, I_{OUT} = 3A



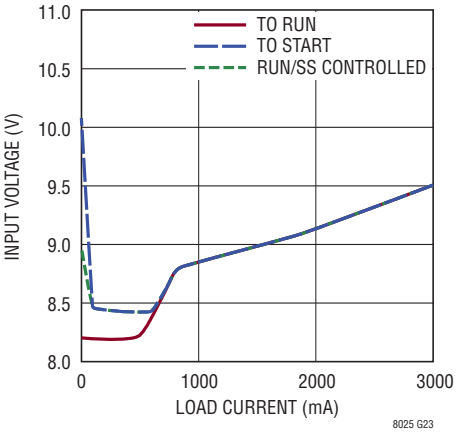
Minimum Input Voltage vs Load Current, 3.3V_{OUT}



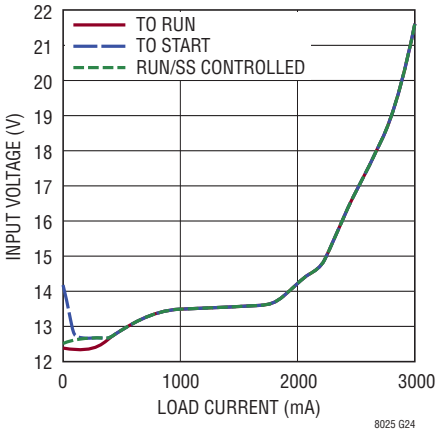
Minimum Input Voltage vs Load Current, 5V_{OUT}



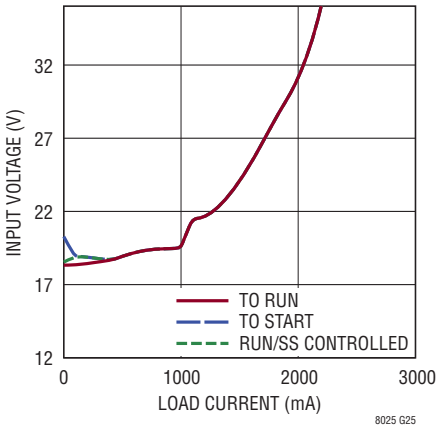
Minimum Input Voltage vs Load Current, 8V_{OUT}



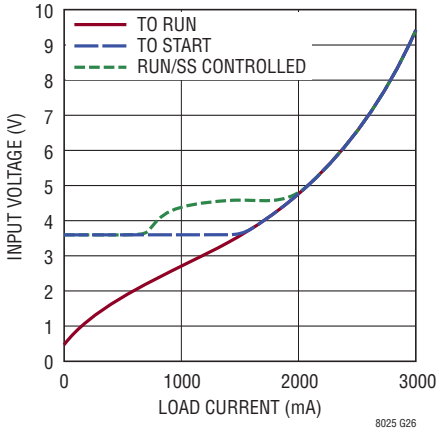
Minimum Input Voltage vs Load Current, 12V_{OUT}



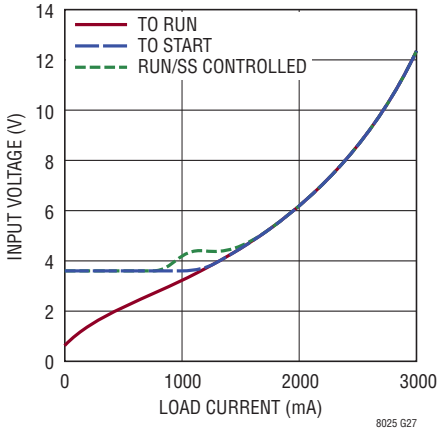
Minimum Input Voltage vs Load Current, 18V_{OUT}



Minimum Input Voltage vs Load Current, –3.3V_{OUT}

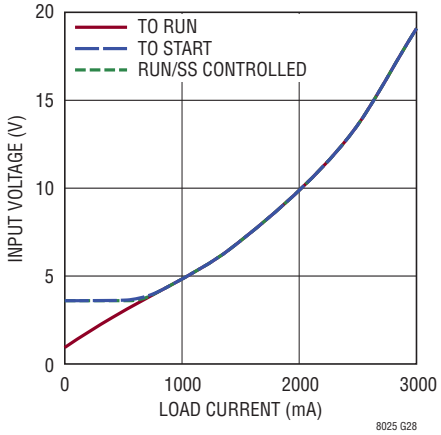


Minimum Input Voltage vs Load Current, –5V_{OUT}

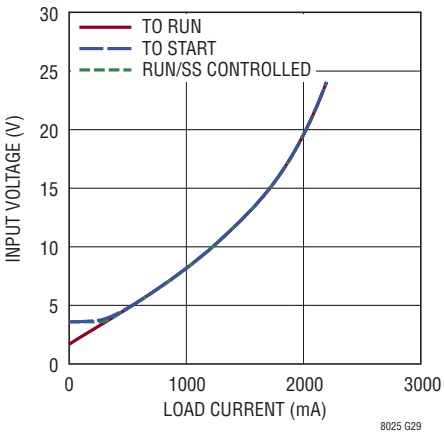


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

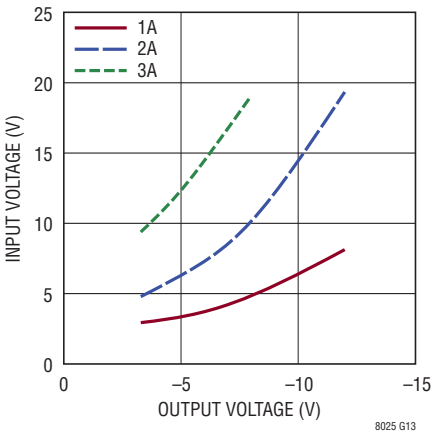
Minimum Input Voltage vs Load Current, –8V_{OUT}



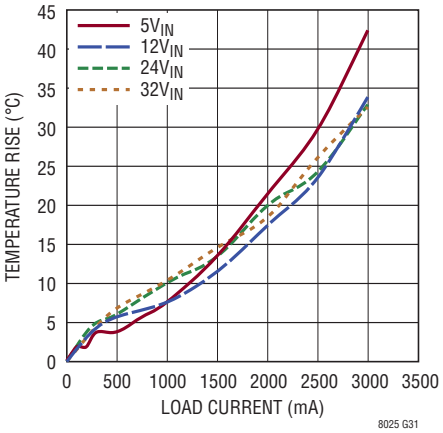
Minimum Input Voltage vs Load Current, –12V_{OUT}



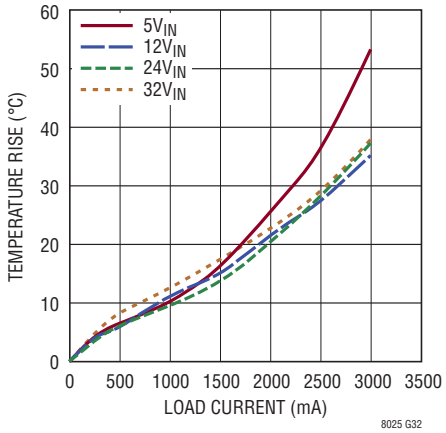
Minimum Input Voltage vs Negative V_{OUT}



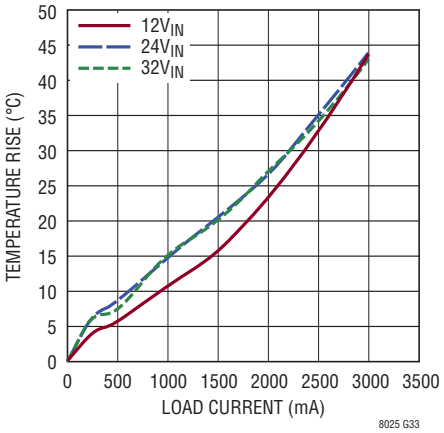
Junction Temperature Rise vs Load Current, 2.5V_{OUT}



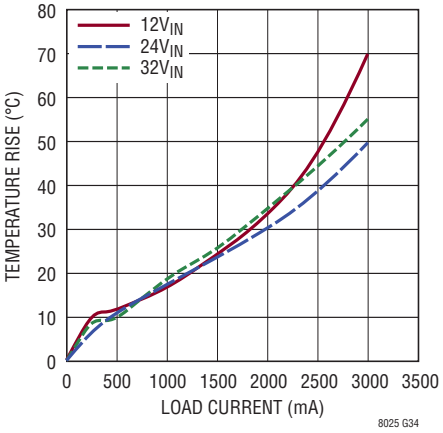
Junction Temperature Rise vs Load Current, 3.3V_{OUT}



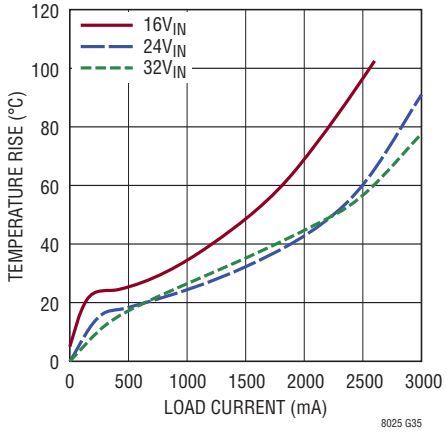
Junction Temperature Rise vs Load Current, 5V_{OUT}



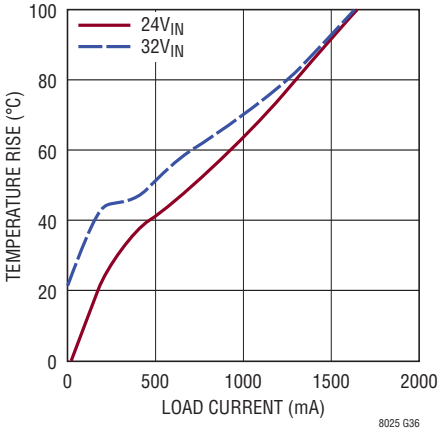
Junction Temperature Rise vs Load Current, 8V_{OUT}



Junction Temperature Rise vs Load Current, 12V_{OUT}



Junction Temperature Rise vs Load Current, 18V_{OUT}



PIN FUNCTIONS

V_{OUT} (Bank 1): Power Output Pins. Apply the output filter capacitor and the output load between these pins and GND pins.

GND (Bank 2): Tie these GND pins to a local ground plane below the LTM8025 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8025 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Return the feedback divider (R_{ADJ}) to this net.

V_{IN} (Bank 3): The V_{IN} pin supplies current to the LTM8025's internal regulator and to the internal power switch. This pin must be locally bypassed with an external, low ESR capacitor; see Table 1 for recommended values.

AUX (Pin G5): Low Current Voltage Source for BIAS. In many designs, the BIAS pin is simply connected to V_{OUT}. The AUX pin is internally connected to V_{OUT} and is placed adjacent to the BIAS pin to ease printed circuit board routing. Although this pin is internally connected to V_{OUT}, it is not intended to deliver a high current, so do **not** draw current from this pin to the load. If this pin is not tied to BIAS, leave it floating.

BIAS (Pin H5): The BIAS pin connects to the internal power bus. Connect to a power source greater than 2.8V and less than 25V. If the output is greater than 2.8V, connect this pin there. If the output voltage is less, connect this to a voltage source between 2.8V and 25V. Also, make sure that BIAS + V_{IN} is less than 56V.

RUN/SS (Pin L5): Pull the RUN/SS pin below 0.2V to shut down the LTM8025. Tie to 2.5V or more for normal operation. If the shutdown feature is not used, tie this pin to the V_{IN} pin. RUN/SS also provides a soft-start function; see the Applications Information section.

SYNC (Pin L6): This is the external clock synchronization input. Ground this pin for low ripple Burst Mode operation at low output loads. Tie to a stable voltage source greater than 0.7V to disable Burst Mode operation. Do not leave this pin floating. Tie to a clock source for synchronization. Clock edges should have rise and fall times faster than 1µs. See the Synchronization section in Applications Information.

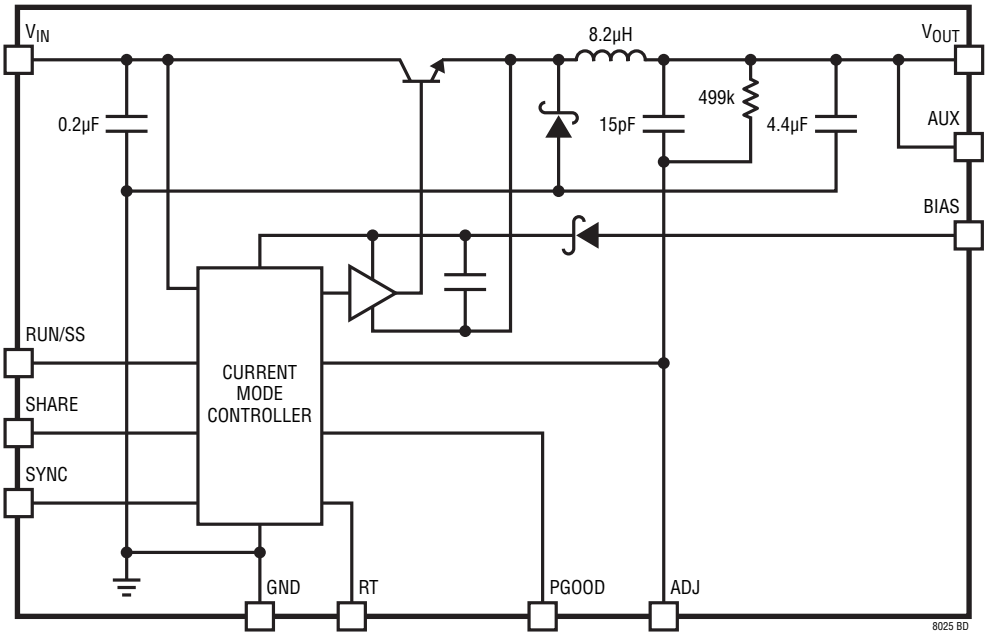
RT (Pin G7): The RT pin is used to program the switching frequency of the LTM8025 by connecting a resistor from this pin to ground. Table 2 gives the resistor values that correspond to the resultant switching frequency. Minimize the capacitance at this pin.

SHARE (Pin H7): Tie this to the SHARE pin of another LTM8025 when paralleling the outputs. Otherwise, do not connect.

PGOOD (Pin J7): The PGOOD pin is the open-collector output of an internal comparator. PGOOD remains low until the ADJ pin is within 10% of the final regulation voltage. PGOOD output is valid when V_{IN} is above 3.6V and RUN/SS is high. If this function is not used, leave this pin floating.

ADJ (Pin K7): The LTM8025 regulates its ADJ pin to 0.79V. Connect the adjust resistor from this pin to ground. The value of R_{ADJ} is given by the equation $R_{ADJ} = 394.21/(V_{OUT} – 0.79)$, where R_{ADJ} is in kΩ.

BLOCK DIAGRAM



OPERATION

The LTM8025 is a standalone nonisolated step-down switching DC/DC power supply that can deliver up to 3A of output current. This module provides a precisely regulated output voltage programmable via one external resistor from 0.8V to 25V. The input voltage range is 3.6V to 36V. Given that the LTM8025 is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current.

As shown in the Block Diagram, the LTM8025 contains a current mode controller, power switching element, power inductor, power Schottky diode and a modest amount of input and output capacitance. The LTM8025 is a fixed frequency PWM regulator. The switching frequency is set by simply connecting the appropriate resistor value from the RT pin to GND.

An internal regulator provides power to the control circuitry. The bias regulator normally draws power from the V_{IN} pin, but if the BIAS pin is connected to an external voltage higher than 2.8V, bias power will be drawn from the external source (typically the regulated output voltage). This improves efficiency. The RUN/SS pin is used to place the LTM8025 in shutdown, disconnecting the output and reducing the input current to less than 1µA.

To further optimize efficiency, the LTM8025 automatically switches to Burst Mode® operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current to 50µA in a typical application.

The oscillator reduces the LTM8025's operating frequency when the voltage at the ADJ pin is low. This frequency foldback helps to control the output current during start-up and overload.

The LTM8025 contains a power good comparator which trips when the ADJ pin is at roughly 90% of its regulated value. The PGOOD output is an open-collector transistor that is off when the output is in regulation, allowing an external resistor to pull the PGOOD pin high. Power good is valid when the LTM8025 is enabled and V_{IN} is above 3.6V.

The LTM8025 is equipped with a thermal shutdown that will inhibit power switching at high junction temperatures. The activation threshold of this function, however, is above 125°C to avoid interfering with normal operation. Thus, prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device.

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For most applications, the design process is straight forward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT}, R_{ADJ} and R_T values.
3. Connect BIAS as indicated.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current is limited by junction temperaturetemperature, the relationship between the input and output voltage magnitude and polarity and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

The maximum frequency (and attendant R_T value) at which the LTM8025 should be allowed to switch is given in Table 1 in the f_{MAX} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the $f_{OPTIMAL}$ column. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

Ceramic capacitors are also piezoelectric. In Burst Mode operation, the LTM8025's switching frequency depends on the load current, and can excite a ceramic capacitor at audio frequencies, generating audible noise. Since the LTM8025 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear.

If this audible noise is unacceptable, use a high performance electrolytic capacitor at the output. It may also be a parallel combination of a ceramic capacitor and a low cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8025. A ceramic input capacitor combined with trace or cable inductance forms a high Q (under damped) tank circuit. If the LTM8025 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Frequency Selection

The LTM8025 uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 2.4MHz by using a resistor tied from the RT pin to ground. Table 2 provides a list of R_T resistor values and their resultant frequencies.

APPLICATIONS INFORMATION

Table 1. Recommended Component Values and Configuration (T_A = 25°C)

V_{IN}	V_{OUT}	C_{IN}	C_{OUT}	R_{ADJ}	BIAS	$f_{OPTIMAL}$	$R_{T(OPTIMAL)}$	f_{MAX}	$R_{T(MIN)}$
3.6V to 36V	0.8V	10µF, 50V, 1210	4× 100µF, 6.3V, 1210	Open	2.8V to 25V	230kHz	182k	250kHz	169k
3.6V to 36V	1V	10µF, 50V, 1210	4× 100µF, 6.3V, 1210	1.87M	2.8V to 25V	240kHz	174k	285kHz	147k
3.6V to 36V	1.2V	10µF, 50V, 1210	4× 100µF, 6.3V, 1210	953k	2.8V to 25V	255kHz	162k	315kHz	130k
3.6V to 36V	1.5V	10µF, 50V, 1210	4× 100µF, 6.3V, 1210	549k	2.8V to 25V	270kHz	154k	360kHz	113k
3.6V to 36V	1.8V	10µF, 50V, 1210	3× 100µF, 6.3V, 1210	383k	2.8V to 25V	285kHz	147k	420kHz	95.3k
4.1V to 36V	2.5V	4.7µF, 50V, 1206	2× 100µF, 6.3V, 1210	226k	2.8V to 25V	300kHz	137k	540kHz	71.5k
5.3V to 36V	3.3V	4.7µF, 50V, 1206	100µF, 6.3V, 1210	154k	AUX	345kHz	118k	675kHz	54.9k
7.5V to 36V	5V	4.7µF, 50V, 1206	100µF, 6.3V, 1206	93.1k	AUX	425kHz	93.1k	950kHz	36.5k
10.5V to 36V	8V	4.7µF, 50V, 1206	47µF, 16V, 1210	54.9k	AUX	550kHz	69.8k	1.45MHz	20.5k
16V to 36V	12V	2.2µF, 50V, 1206	22µF, 16V, 1210	34.8k	AUX	760kHz	47.5k	2.3MHz	9.09k
23V to 36V	18V	2.2µF, 50V, 1206	22µF, 25V, 1812	22.6k	AUX	800kHz	44.2k	2.4MHz	8.25k
31V to 36V	24V	1µF, 50V, 1206	22µF, 25V, 1812	16.5k	2.8V to 25V	1MHz	34k	2.4MHz	8.25k
3.6V to 15V	0.8V	10µF, 25V, 1210	4× 100µF, 6.3V, 1210	Open	V_{IN}	230kHz	182k	575kHz	66.5k
3.6V to 15V	1V	10µF, 25V, 1210	4× 100µF, 6.3V, 1210	1.87M	V_{IN}	240kHz	174k	660kHz	56.2k
3.6V to 15V	1.2V	10µF, 25V, 1210	4× 100µF, 6.3V, 1210	953k	V_{IN}	255kHz	162k	760kHz	47.5k
3.6V to 15V	1.5V	10µF, 25V, 1210	4× 100µF, 6.3V, 1210	549k	V_{IN}	270kHz	154k	840kHz	42.2k
3.6V to 15V	1.8V	10µF, 25V, 1210	4× 100µF, 6.3V, 1210	383k	V_{IN}	285kHz	147k	1.0MHz	34k
4.1V to 15V	2.5V	4.7µF, 16V, 1206	2× 100µF, 6.3V, 1210	226k	V_{IN}	300kHz	137k	1.3MHz	23.7k
5.3V to 15V	3.3V	4.7µF, 16V, 1206	100µF, 6.3V, 1206	154k	AUX	345kHz	118k	1.6MHz	17.8k
7.5V to 15V	5V	4.7µF, 16V, 1206	100µF, 6.3V, 1206	93.1k	AUX	425kHz	93.1k	2.4MHz	8.25k
10.5V to 15V	8V	2.2µV, 25V, 1206	47µF, 16V, 1210	54.9k	AUX	550kHz	69.8k	2.4MHz	8.25k
9V to 24V	0.8V	4.7µF, 25V, 1206	4× 100µF, 6.3V, 1210	Open	V_{IN}	270kHz	154k	360kHz	113k
9V to 24V	1V	4.7µF, 25V, 1206	4× 100µF, 6.3V, 1210	1.87M	V_{IN}	285kHz	147k	410kHz	97.6k
9V to 24V	1.2V	4.7µF, 25V, 1206	4× 100µF, 6.3V, 1210	953k	V_{IN}	295kHz	140k	475kHz	82.5k
9V to 24V	1.5V	4.7µF, 25V, 1206	4× 100µF, 6.3V, 1210	549k	V_{IN}	310kHz	133k	550kHz	69.8k
9V to 24V	1.8V	4.7µF, 25V, 1206	3× 100µF, 6.3V, 1210	383k	V_{IN}	330kHz	124k	620kHz	60.4k
9V to 24V	2.5V	4.7µF, 25V, 1206	100µF, 6.3V, 1206	226k	V_{IN}	345kHz	118k	800kHz	44.2k
9V to 24V	3.3V	4.7µF, 25V, 1206	100µF, 6.3V, 1206	154k	AUX	425kHz	93.1k	1MHz	34k
9V to 24V	5V	4.7µF, 25V, 1206	47µF, 16V, 1210	93.1k	AUX	500kHz	76.8k	1.4MHz	21.5k
10.5V to 24V	8V	2.2µF, 25V, 1206	22µF, 16V, 1210	54.9k	AUX	590kHz	64.9k	2.2MHz	9.76k
16V to 24V	12V	2.2µF, 50V, 1206	22µF, 16V, 1210	34.8k	AUX	760kHz	47.5k	2.3MHz	9.09k
23V to 24V	18V	2.2µF, 50V, 1206	22µF, 25V, 1812	22.6k	AUX	800kHz	44.2k	2.4MHz	8.25k
18V to 36V	0.8V	1µF, 50V, 1206	4× 100µF, 6.3V, 1210	Open	2.8V to 25V	230kHz	182k	250kHz	169k
18V to 36V	1V	1µF, 50V, 1206	4× 100µF, 6.3V, 1210	1.87M	2.8V to 25V	240kHz	174k	285kHz	147k
18V to 36V	1.2V	1µF, 50V, 1206	4× 100µF, 6.3V, 1210	953k	2.8V to 25V	255kHz	162k	315kHz	130k
18V to 36V	1.5V	1µF, 50V, 1206	4× 100µF, 6.3V, 1210	549k	2.8V to 25V	270kHz	154k	360kHz	113k
18V to 36V	1.8V	1µF, 50V, 1206	3× 100µF, 6.3V, 1210	383k	2.8V to 25V	300kHz	137k	420kHz	95.3k
18V to 36V	2.5V	1µF, 50V, 1206	100µF, 6.3V, 1206	226k	2.8V to 25V	345kHz	118k	540kHz	71.5k
18V to 36V	3.3V	1µF, 50V, 1206	100µF, 6.3V, 1206	154k	AUX	385kHz	105k	675kHz	54.9k
18V to 36V	5V	1µF, 50V, 1206	47µF, 16V, 1210	93.1k	AUX	500kHz	76.8k	950kHz	36.5k
18V to 36V	8V	2.2µF, 50V, 1206	22µF, 16V, 1210	54.9k	AUX	550kHz	69.8k	1.45MHz	20.5k
18V to 36V	12V	2.2µF, 50V, 1206	22µF, 16V, 1210	34.8k	AUX	760kHz	47.5k	2.3MHz	9.09k
4.75V to 32V	–3.3V	4.7µF, 50V, 1206	100µF, 6.3V, 1210	154k	AUX	345kHz	118k	675kHz	54.9k
7V to 31V	–5V	4.7µF, 50V, 1206	100µF, 6.3V, 1210	93.1k	AUX	425kHz	93.1k	950kHz	36.5k
15V to 28V	–8V	4.7µF, 50V, 1206	47µF, 16V, 1210	54.9k	AUX	550kHz	69.8k	1.45MHz	20.5k
20V to 24V	–12V	4.7µF, 50V, 1206	22µF, 16V, 1210	34.8k	AUX	760kHz	47.5k	2.3MHz	9.09k

Note: An input bulk capacitance is required. Do not allow V_{IN} + BIAS to exceed 56V. Refer to the Typical Performance Characteristics section for load conditions.

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Table 2. Switching Frequency vs R_T Value

SWITCHING FREQUENCY	R_T VALUE
0.2MHz	215kΩ
0.3MHz	137kΩ
0.4MHz	100kΩ
0.5MHz	76.8kΩ
0.6MHz	63.4kΩ
0.7MHz	52.3kΩ
0.8MHz	44.2kΩ
0.9MHz	38.3kΩ
1MHz	34.0kΩ
1.2MHz	26.7kΩ
1.4MHz	21.5kΩ
1.6MHz	17.8kΩ
1.8MHz	14.7kΩ
2MHz	12.1kΩ
2.2MHz	9.76kΩ
2.4MHz	8.25kΩ

Operating Frequency Tradeoffs

It is recommended that the user apply the optimal R_T value given in Table 1 for the input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8025 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8025 if the output is overloaded or short circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

BIAS Pin Considerations

The BIAS pin is used to provide drive power for the internal power switching stage and operate other internal circuitry. For proper operation, it must be powered by at least 2.8V. If the output voltage is programmed to 2.8V or higher, BIAS may be simply tied to AUX. If V_{OUT} is less than 2.8V, BIAS can be tied to V_{IN} or some other voltage source. If the BIAS pin voltage is too high, the efficiency of the LTM8025 may suffer. The optimum BIAS voltage is dependent upon many factors, such as load current, input voltage, output voltage and switching frequency, but 4V to 5V works well in many applications. In all cases, ensure that the maximum voltage at the BIAS pin is less than 25V and that the sum of V_{IN} and BIAS is less than 56V. If BIAS power is applied from a remote or noisy voltage source, it may be necessary to apply a decoupling capacitor locally to the pin.

Load Sharing

Two or more LTM8025's may be paralleled to produce higher currents. To do this, tie the V_{IN}, ADJ, V_{OUT} and SHARE pins of all the paralleled LTM8025's together. To ensure that paralleled modules start up together, the RUN/SS pins may be tied together, as well. If the RUN/SS pins are not tied together, make sure that the same valued soft-start capacitors are used for each module. Current sharing can be improved by synchronizing the LTM8025s. An example of two LTM8025s configured for load sharing is given in the Typical Application section.

Burst Mode Operation

To enhance efficiency at light loads, the LTM8025 automatically switches to Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LTM8025 delivers single cycle bursts of current to the output capacitor followed by sleep periods where the output power is delivered to the load by the output capacitor. In addition, V_{IN} and BIAS quiescent currents are each reduced to microamps during the sleep time. As the load current decreases towards a no load condition, the percentage of time that the LTM8025 operates in sleep mode increases and the average input current is greatly reduced, resulting in higher efficiency.

Burst Mode operation is enabled by tying SYNC to GND. To disable Burst Mode operation, tie SYNC to a stable voltage above 0.7V. *Do not leave the SYNC pin floating.*

Minimum Input Voltage

The LTM8025 is a step-down converter, so a minimum amount of headroom is required to keep the output in regulation. In addition, the input voltage required to turn

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on is higher than that required to run, and depends upon whether the RUN/SS is used. As shown in the Typical Performance Characteristics section, the minimum input voltage to run a 3.3V output at light load is only about 3.6V, but, if the RUN/SS is pulled up to V_{IN}, it takes 5.5V_{IN} to start. If the LTM8025 is enabled with the RUN/SS pin, the minimum voltage to start at light loads is lower, about 4.3V. Similar curves detailing this behavior of the LTM8025 for other outputs are also included in the Typical Performance Characteristics section.

Soft-Start

The RUN/SS pin can be used to soft-start the LTM8025, reducing the maximum input current during start-up. The RUN/SS pin is driven through an external RC filter to create a voltage ramp at this pin, as shown in Figure 1. By choosing an appropriate RC time constant, the peak start-up current can be reduced to the current that is required to regulate the output, with no overshoot. Choose the value of the resistor so that it can supply at least 20µA when the RUN/SS pin reaches 2.5V.

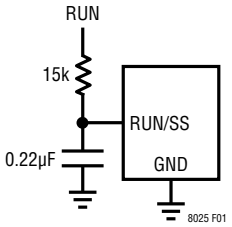


Figure 1. To Soft-Start the LTM8025, Add a Resistor and Capacitor to the RUN/SS Pin

Frequency Foldback

The LTM8025 is equipped with frequency foldback which acts to reduce the thermal and energy stress on the internal power elements during a short circuit or output overload condition. If the LTM8025 detects that the output has fallen out of regulation, the switching frequency is reduced as a function of how far the output is below the target voltage. This in turn limits the amount of energy that can be delivered to the load under fault. During the start-up time, frequency foldback is also active to limit the energy delivered to the potentially large output capacitance of the load.

Synchronization

The internal oscillator of the LTM8025 can be synchronized by applying an external 250kHz to 2MHz clock to the SYNC pin. Do not leave this pin floating. When synchronizing the LTM8025, select an R_T resistor value that corresponds to an operating frequency 20% lower than the intended synchronization frequency (see the Frequency Selection section).

In addition to synchronization, the SYNC pin controls Burst Mode behavior. If the SYNC pin is driven by an external clock, or pulled up above 0.7V, the LTM8025 will not enter Burst Mode operation, but will instead skip pulses to maintain regulation instead.

Shorted Input Protection

Care needs to be taken in systems where the output will be held high when the input to the LTM8025 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode ORed with the LTM8025's output. If the V_{IN} pin is allowed to float and the SHDN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LTM8025's internal circuitry will pull its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUN/SS pin, the input current will drop to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, then parasitic diodes inside the LTM8025 can pull large currents from the output through the V_{IN} pin. Figure 2 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8025. The LTM8025 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified

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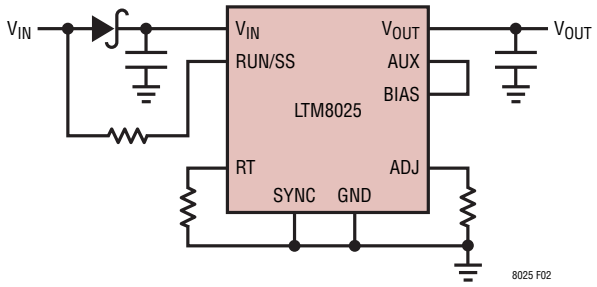


Figure 2. The Input Diode Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LTM8025 Runs Only When the Input is Present.

operation with a haphazard or poor layout. See Figure 3 for a suggested layout. Ensure that the grounding and heatsinking are acceptable.

1. Place the R_{ADJ} and R_T resistors as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8025.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM8025.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground current flow directly adjacent or underneath the LTM8025.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8025.
6. For good heatsinking, use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 3. The LTM8025 can benefit from the heatsinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

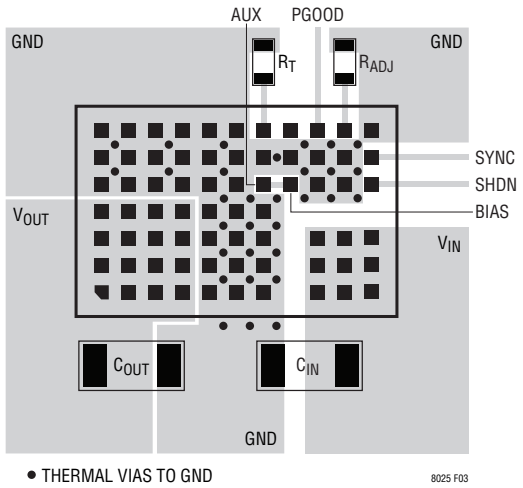


Figure 3. Layout Showing Suggested External Components, GND Plane and Thermal Vias.

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8025. However, these capacitors can cause problems if the LTM8025 is plugged into a live supply (see Linear Technology Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8025 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8025's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM8025 into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is to add an electrolytic bulk capacitor to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit.

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Thermal Considerations

The LTM8025 output current may need to be derated if it is required to operate in a high ambient temperature or deliver a large amount of continuous power. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by a LTM8025 mounted to a 58cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

The junction to air and junction to board thermal resistances given in the Pin Configuration diagram may also be used to estimate the LTM8025 internal temperature. These thermal coefficients are determined for maximum output power per JESD 51-9 "JEDEC Standard, Test Boards for Area Array Surface Mount Package Thermal Measurements" through analysis and physical correlation. Bear in mind that the actual thermal resistance of the LTM8025 to the printed circuit board depends upon the design of the circuit board.

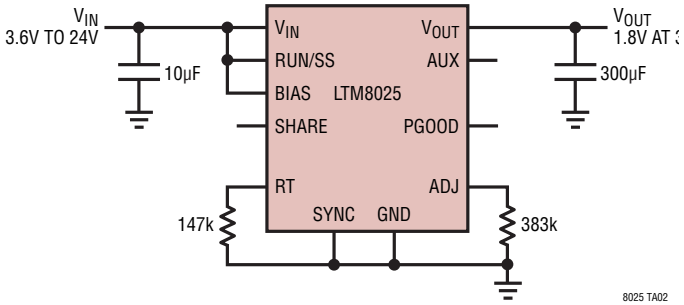
The die temperature of the LTM8025 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8025. The bulk of the heat flow out of the LTM8025 is through the bottom of the module and the LGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

The LTM8025 is equipped with a thermal shutdown that will inhibit power switching at high junction temperatures. The activation threshold of this function, however, is above 125°C to avoid interfering with normal operation. Thus, it follows that prolonged or repetitive operation under a condition in which the thermal shutdown activates necessarily means that the internal components are subjected to temperatures above the 125°C rating for prolonged or repetitive intervals, which may damage or impair the reliability of the device.

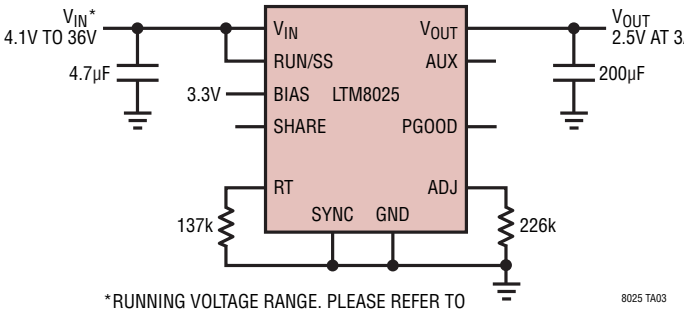
Finally, be aware that at high ambient temperatures the internal Schottky diode will have significant leakage current increasing the quiescent current of the LTM8025.

TYPICAL APPLICATIONS

1.8V Step-Down Converter

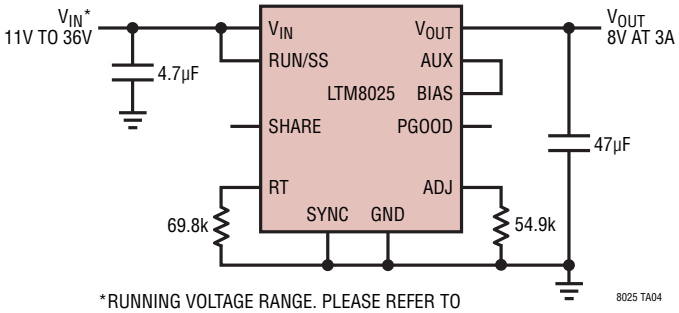


2.5V Step-Down Converter



*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION SECTION FOR START-UP DETAILS

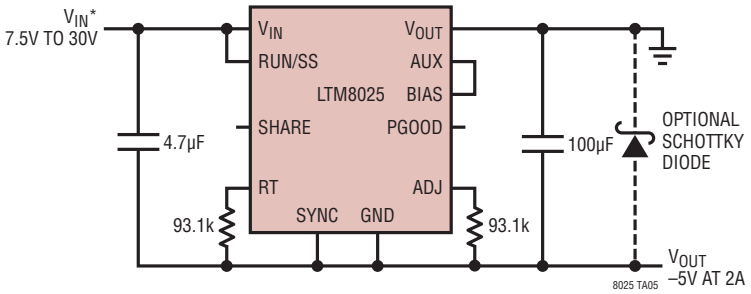
8V Step-Down Converter



*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION SECTION FOR START-UP DETAILS

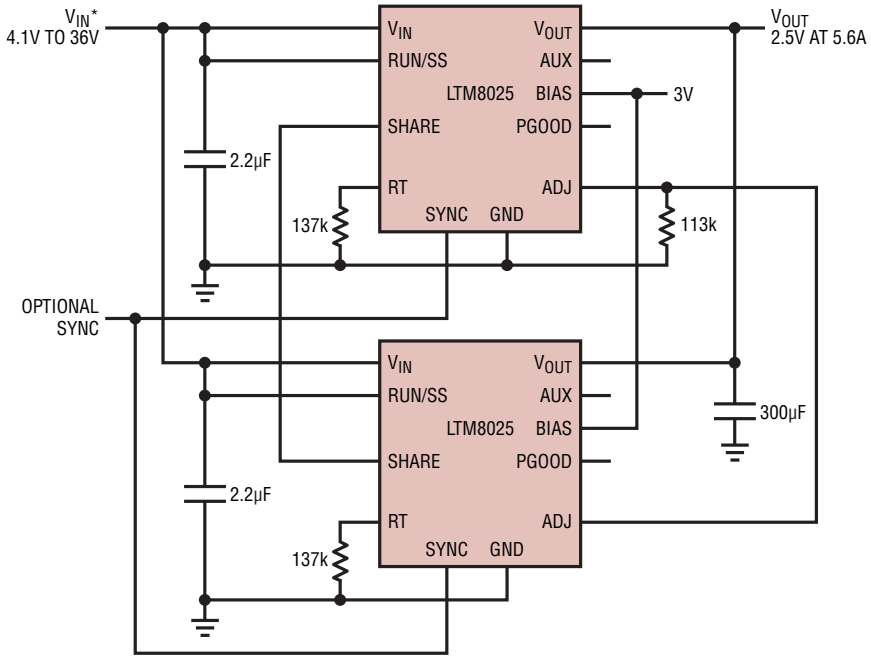
TYPICAL APPLICATIONS

–5V Negative Output Converter



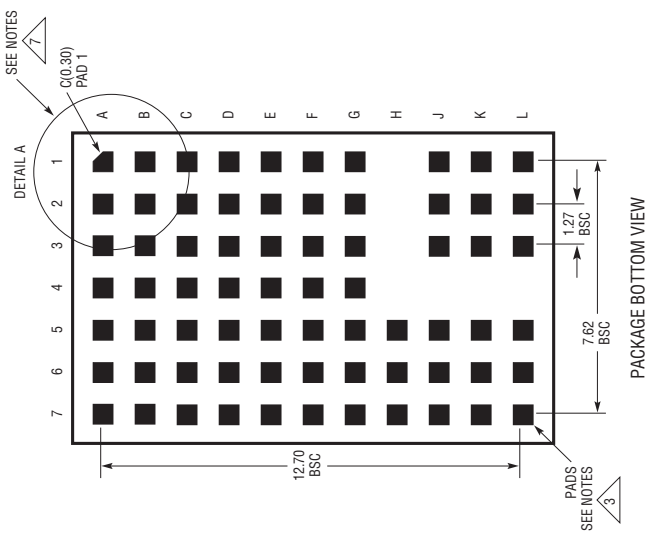
*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION SECTION FOR START-UP DETAILS

Two LTM8025s in Parallel, 2.5V at 5.5A

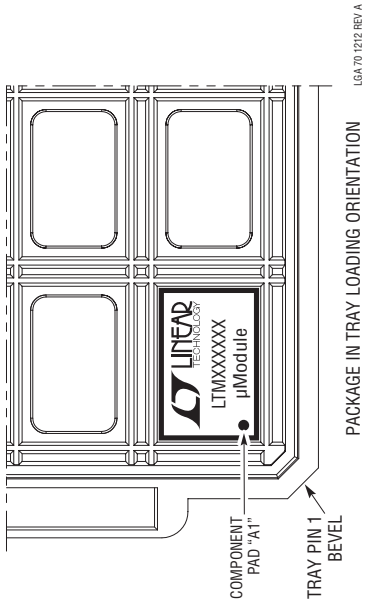


*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION SECTION FOR START-UP DETAILS
NOTE: SYNCHRONIZE THE TWO MODULES TO AVOID BEAT FREQUENCIES, IF NECESSARY. OTHERWISE, TIE EACH SYNC TO GND

PACKAGE DESCRIPTION

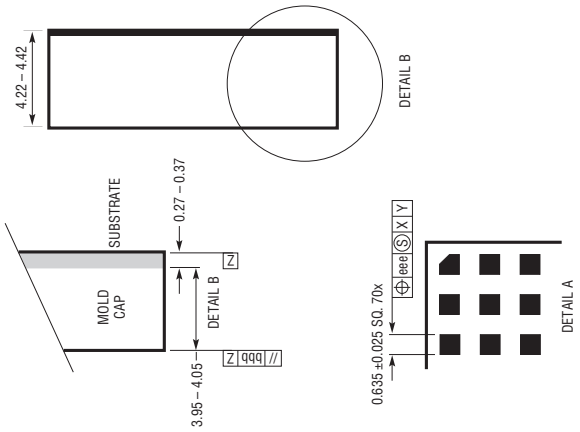


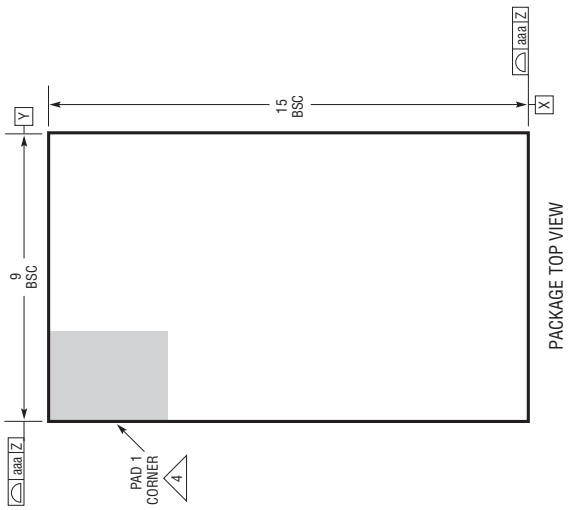
PACKAGE BOTTOM VIEW



PACKAGE IN TRAY LOADING ORIENTATION

LGA Package
70-Lead (15mm × 9mm × 4.32mm)
(Reference LTC DWG # 05-08-1817 Rev A)

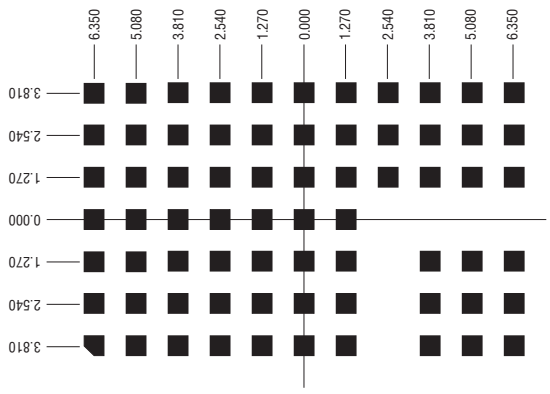




PACKAGE TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND DESIGNATION PER JESD MO-222, SPP-010
4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE TOTAL NUMBER OF PADS: 70
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

SYMBOL	TOLERANCE
aaa	0.15
bbb	0.10
eee	0.05

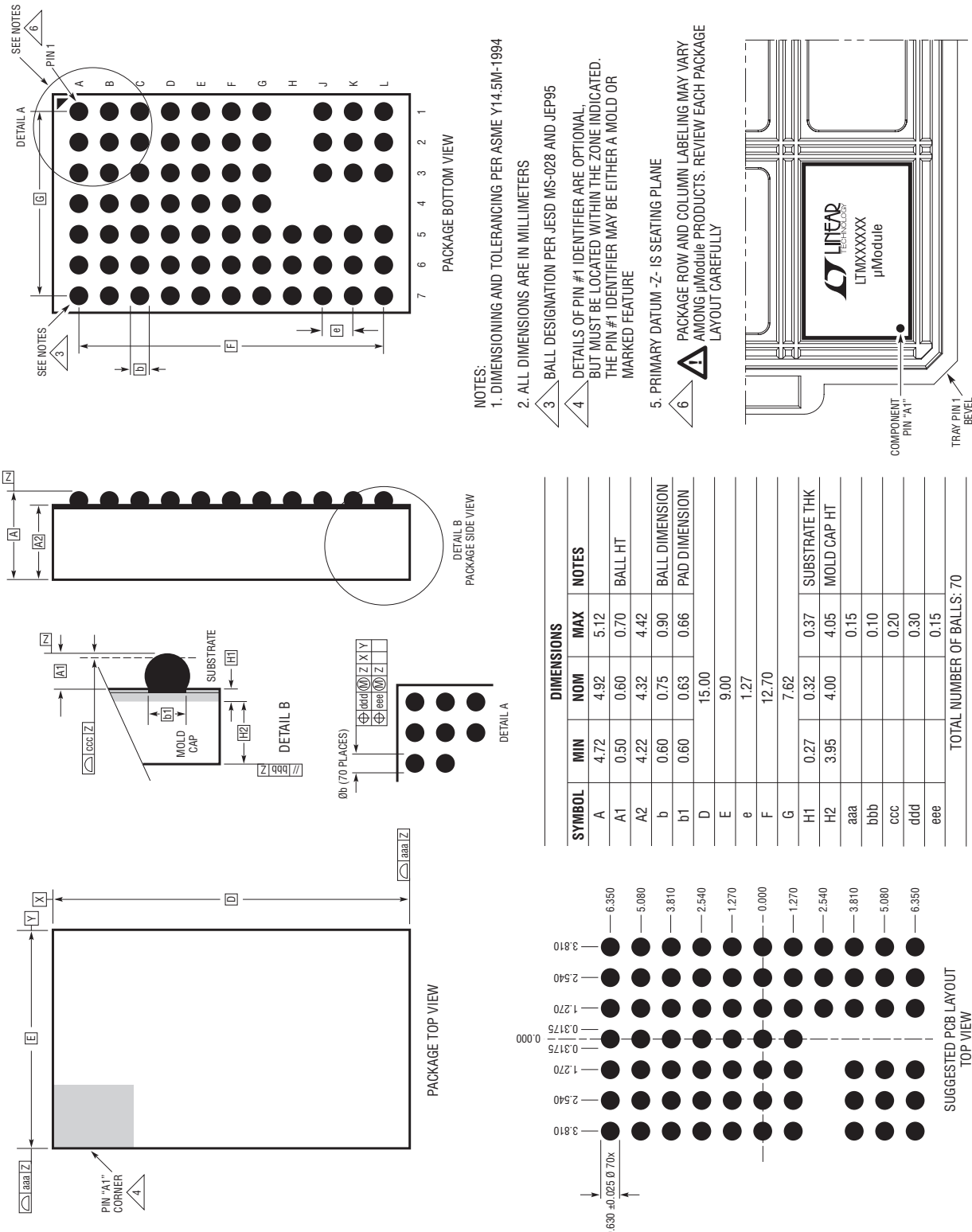


SUGGESTED PCB LAYOUT
TOP VIEW

Rev. D

PACKAGE DESCRIPTION

BGA Package
70-Lead (15mm × 9mm × 4.92mm)
(Reference LTC DWG# 05-08-1918 Rev B)



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.72	4.92	5.12	
A1	0.50	0.60	0.70	BALL HT
A2	4.22	4.32	4.42	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		15.00		
E		9.00		
e		1.27		
F		12.70		
G		7.62		
H1	0.27	0.32	0.37	SUBSTRATE THK
H2	3.95	4.00	4.05	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 70				

PACKAGE DESCRIPTION

Pin Assignment Table
(Arranged by Pin Number)

PIN NAME	PIN NAME	PIN NAME	PIN NAME	PIN NAME	PIN NAME
A1 V_{OUT}	B1 V_{OUT}	C1 V_{OUT}	D1 V_{OUT}	E1 GND	F1 GND
A2 V_{OUT}	B2 V_{OUT}	C2 V_{OUT}	D2 V_{OUT}	E2 GND	F2 GND
A3 V_{OUT}	B3 V_{OUT}	C3 V_{OUT}	D3 V_{OUT}	E3 GND	F3 GND
A4 V_{OUT}	B4 V_{OUT}	C4 V_{OUT}	D4 V_{OUT}	E4 GND	F4 GND
A5 GND	B5 GND	C5 GND	D5 GND	E5 GND	F5 GND
A6 GND	B6 GND	C6 GND	D6 GND	E6 GND	F6 GND
A7 GND	B7 GND	C7 GND	D7 GND	E7 GND	F7 GND

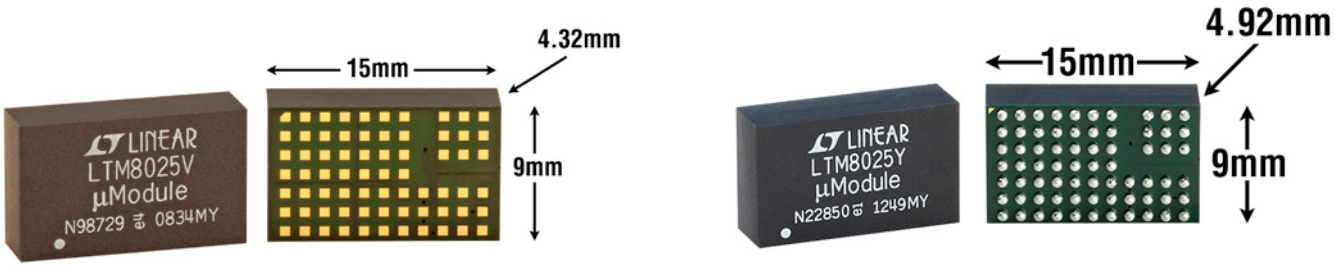
PIN NAME	PIN NAME	PIN NAME	PIN NAME	PIN NAME
G1 GND	H1 -	J1 V_{IN}	K1 V_{IN}	L1 V_{IN}
G2 GND	H2 -	J2 V_{IN}	K2 V_{IN}	L2 V_{IN}
G3 GND	H3 -	J3 V_{IN}	K3 V_{IN}	L3 V_{IN}
G4 GND	H4 -	J4 -	K4 -	L4 -
G5 AUX	H5 BIAS	J5 GND	K5 GND	L5 RUN/SS
G6 GND	H6 GND	J6 GND	K6 GND	L6 SYNC
G7 RT	H7 SHARE	J7 PGOOD	K7 ADJ	L7 GND

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	2/10	Changed to “Current Out of ADJ Operation” in Electrical Characteristics	3
		Additions to Table 1	11
		Changes to “Shorted Input Protection” section	13
		Changes to Related Parts Table	20
B	8/13	Added BGA package	1, 2, 19
C	2/14	Added SnPb BGA option	1, 2
D	2/19	Added new link for product	1
		Changed V_{IN} 3.2V to 3.6V in the Electrical Characteristics table	3

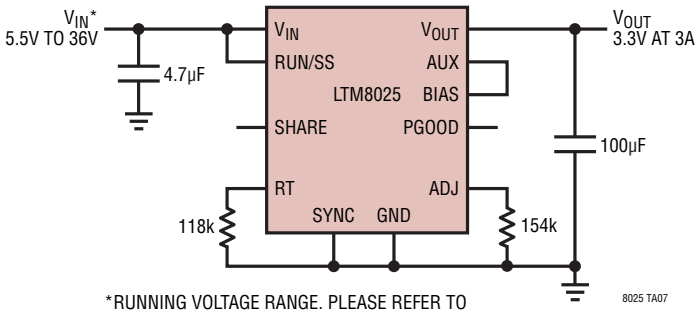
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PACKAGE PHOTOGRAPHY



TYPICAL APPLICATION

3.3V Step-Down Converter



*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION SECTION FOR START-UP DETAILS

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4600/ LTM4602	10A and 6A DC/DC µModule	Pin Compatible, 4.5V ≤ V_{IN} ≤ 28V, 15mm × 15mm × 2.8mm LGA Package
LTM4601/ LTM4603	12A and 6A DC/DC µModule	Pin Compatible; Remote Sensing; PLL, Tracking and Margining, 4.5V ≤ V_{IN} ≤ 28V
LTM4604A	4A, Low V_{IN} DC/DC µModule	2.375V ≤ V_{IN} ≤ 5.5V, 0.8V ≤ V_{OUT} ≤ 5V, 9mm × 15mm × 2.3mm LGA Package
LTM4606	Low EMI 6A, 28V DC/DC µModule	4.5V ≤ V_{IN} ≤ 28V, 0.6V ≤ V_{OUT} ≤ 5V, 15mm × 15mm × 2.8mm LGA Package
LTM8020	200mA, 36V DC/DC µModule	4V ≤ V_{IN} ≤ 36V, 1.25V ≤ V_{OUT} ≤ 5V, 6.25mm × 6.25mm × 2.32mm LGA Package
LTM8022/ LTM8023	1A and 2A, 36V DC/DC µModule	Pin Compatible 3.6V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 10V, 11.25mm × 9mm × 2.82mm LGA Package
LTM8027	60V, 4A DC/DC µModule	4.5V ≤ V_{IN} ≤ 60V; 2.5V ≤ V_{OUT} ≤ 24V, 15mm × 15mm × 4.32mm LGA Package

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